

fixed: clk/sysd0, jtag, u22 footprint

**Dossytronics**

Sheet: /UI/

File: UI.sch

**Title: Mk.3 Blitter FPGA development board**

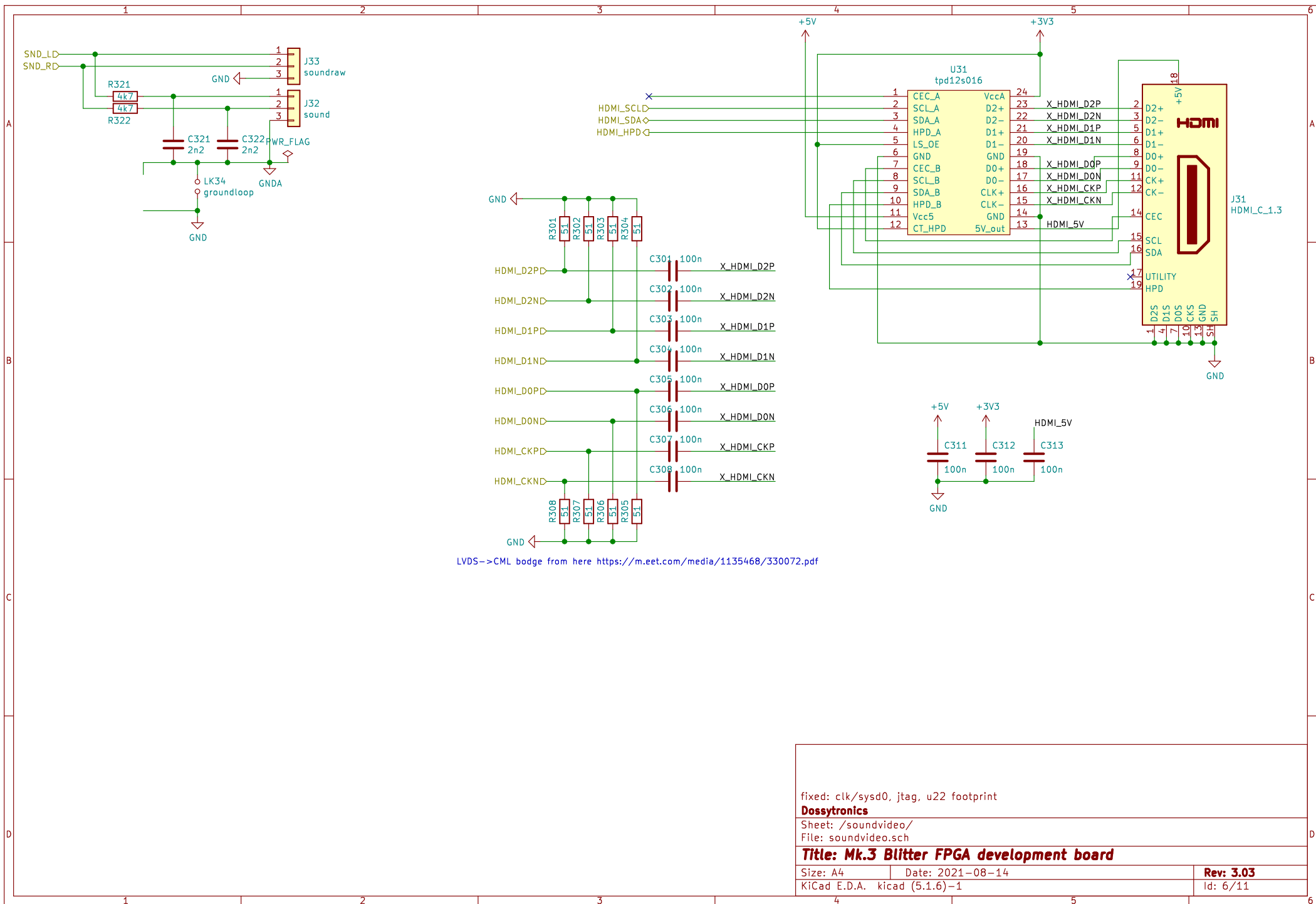
Size: A4

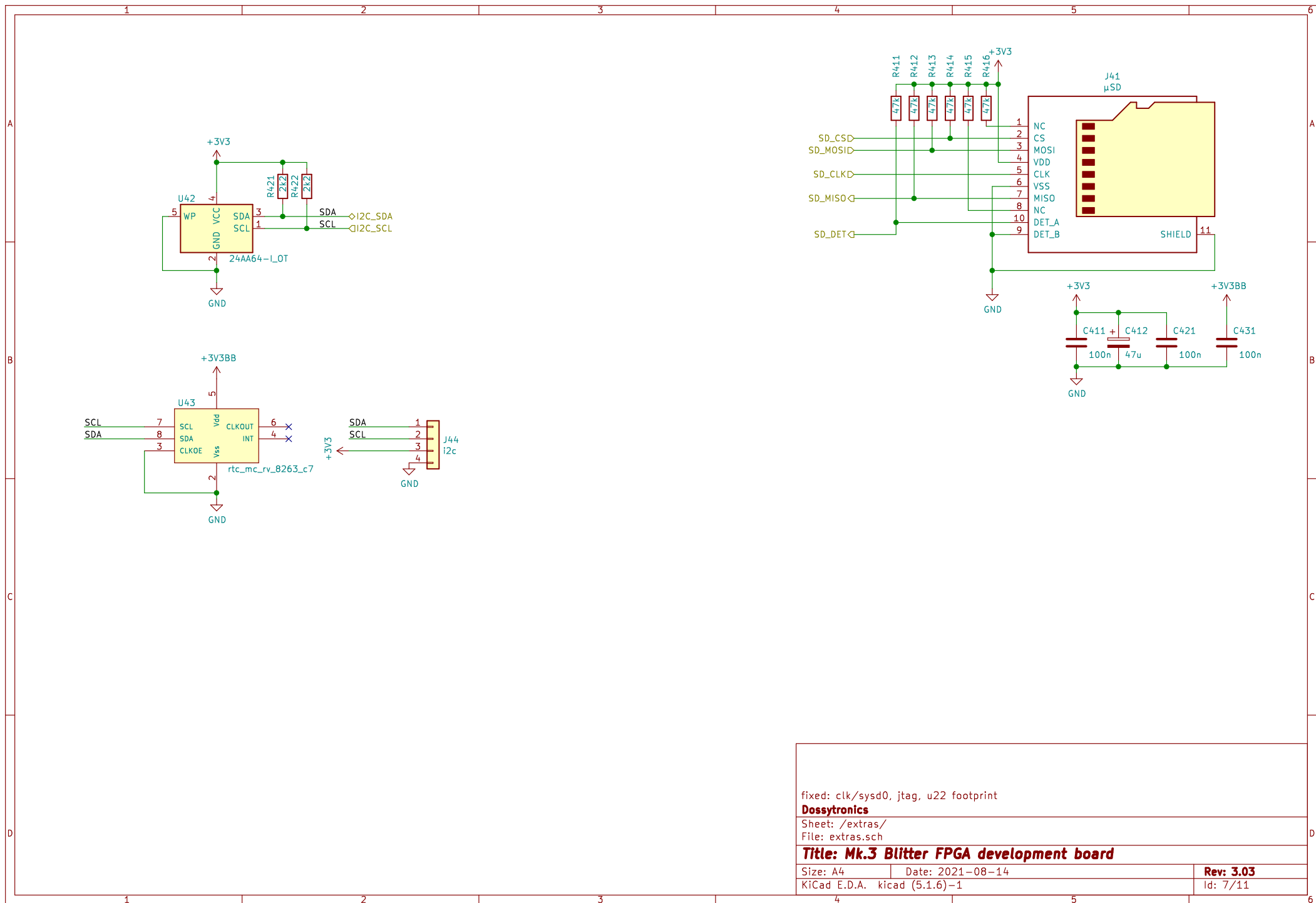
Date: 2021-08-14

**Rev: 3.03**

KiCad E.D.A. kicad (5.1.6)-1

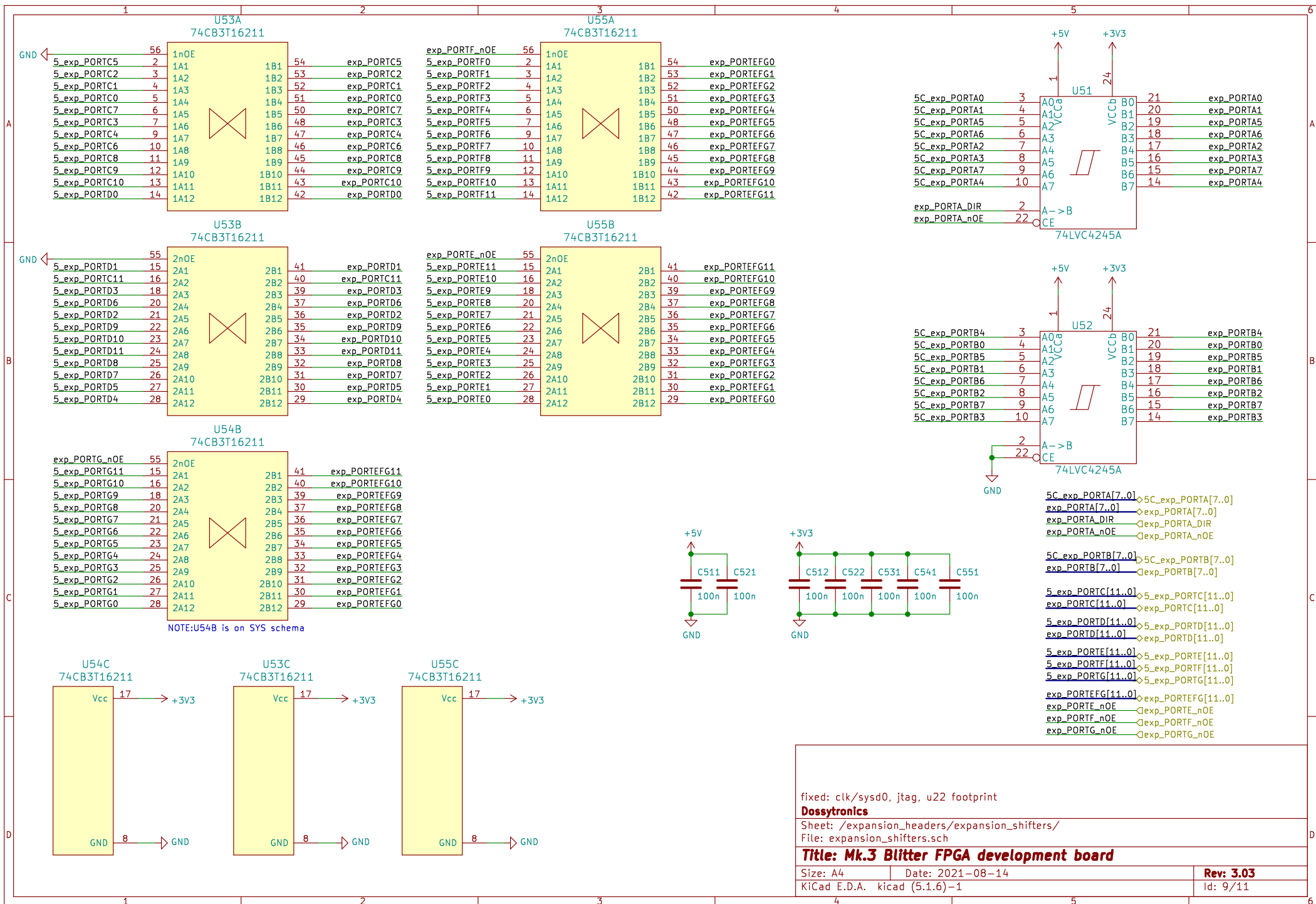
Id: 5/11





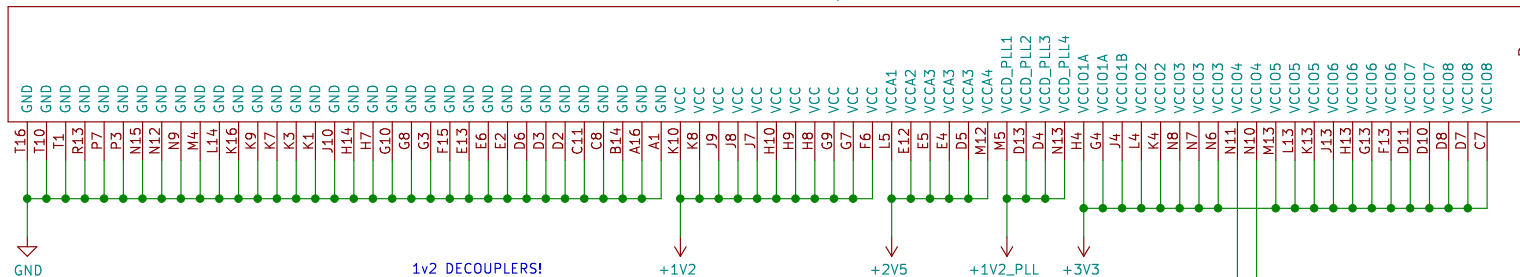
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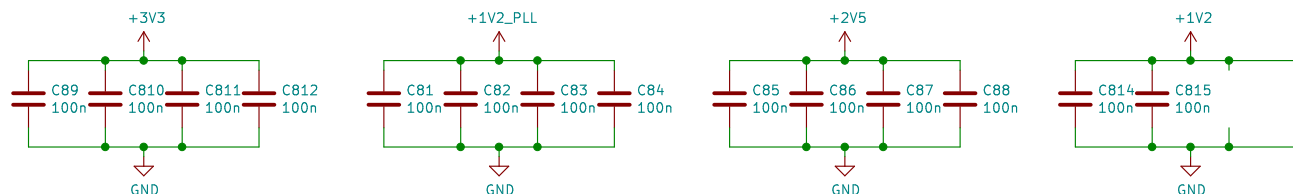


# U8A

## 10M16DCF256I7G\_mk3pinstest

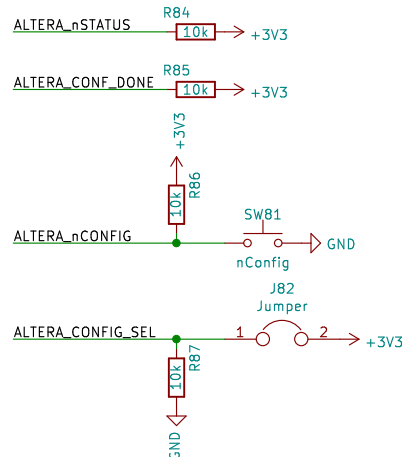
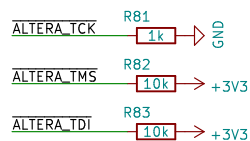
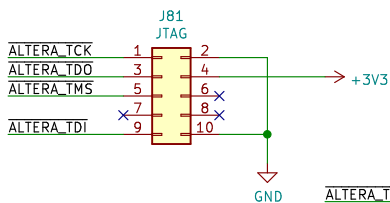
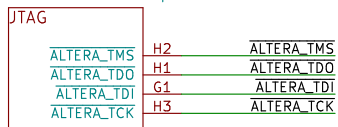


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# U8G

## 10M16DCF256I7G\_mk3pinstest



fixed: clk/sysd0, jtag, u22 footprint

**Dossytronics**

Sheet: /fpga\_power/

File: fpga\_power.sch

**Title: Mk.3 Blitter FPGA development board**

Size: A4 Date: 2021-08-14

KiCad E.D.A. kicad (5.1.6)-1

**Rev: 3.03**

Id: 10/11

