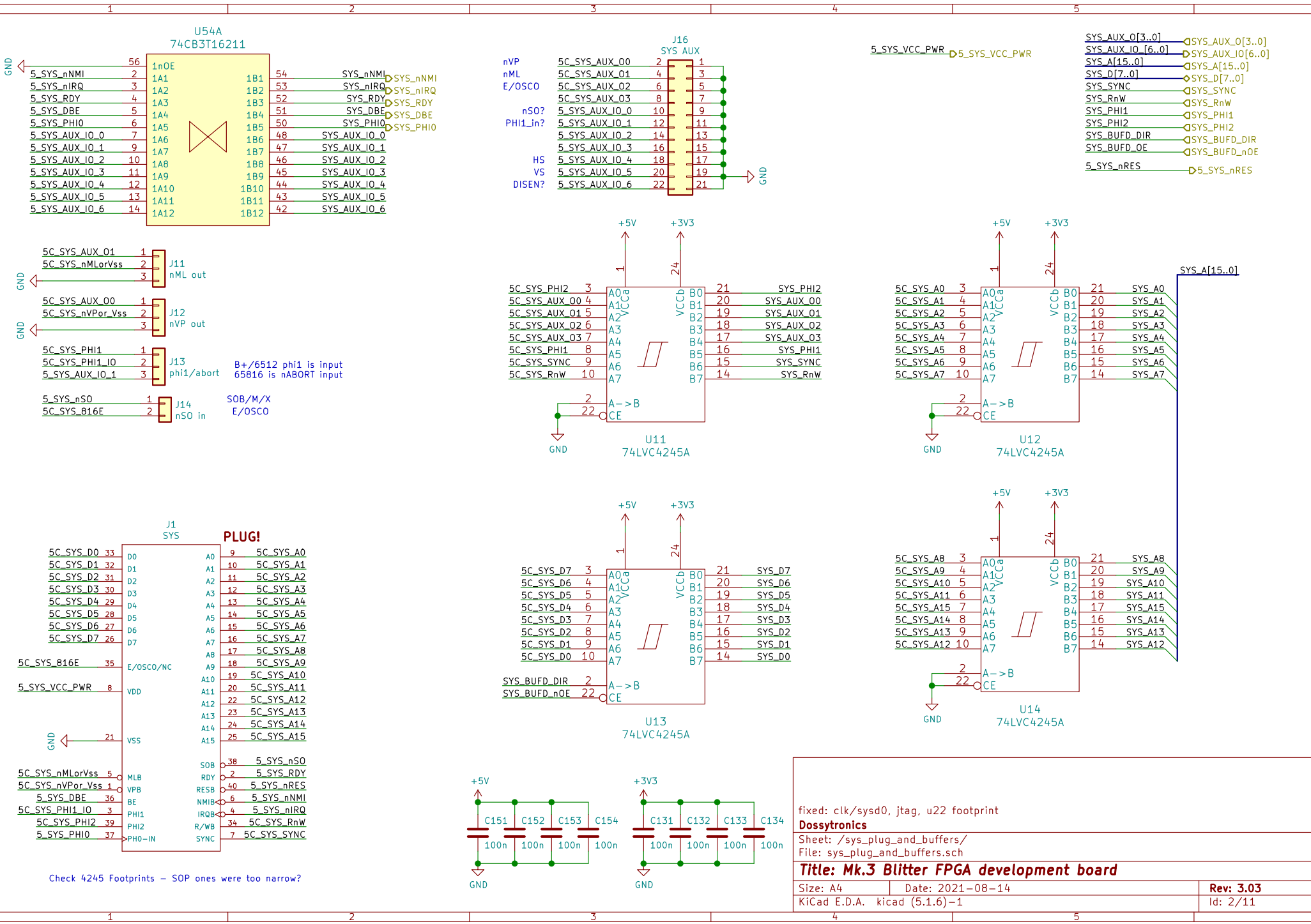
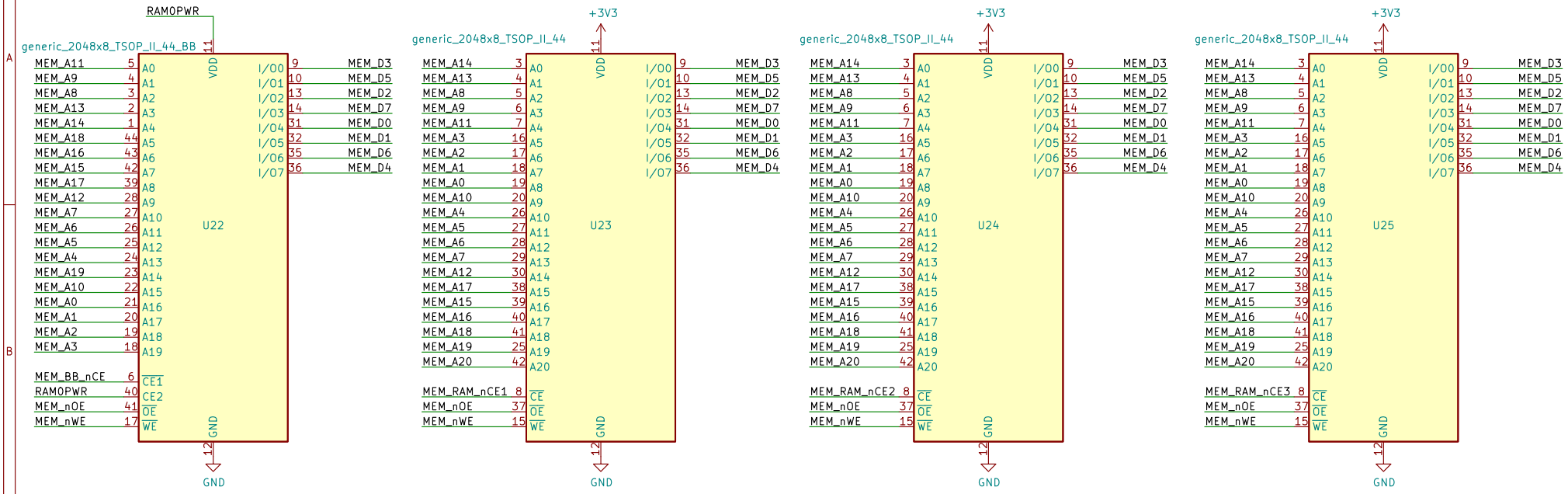
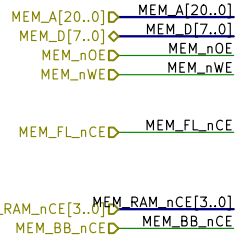
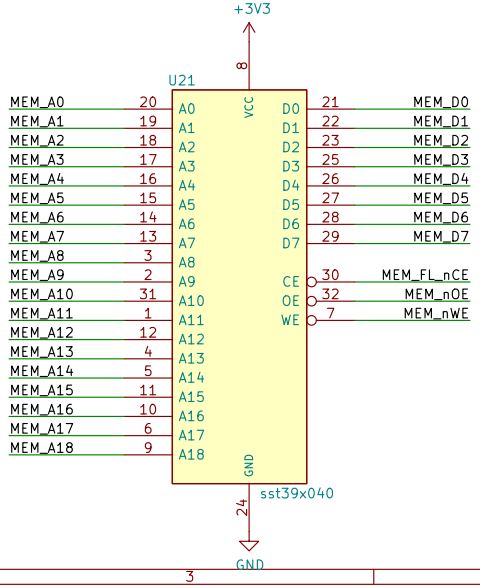
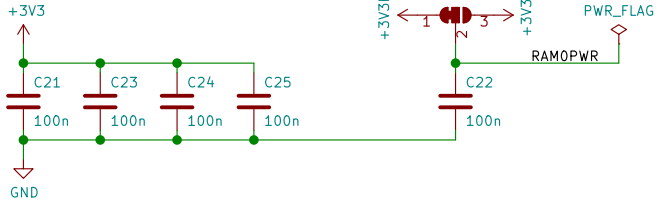

Sheet: sys_plug_and_buffers
SYS_A[15..0]
SYS_D[7..0]
SYS_SYNC
SYS_RnW
SYS_PHI1
SYS_PHI2
SYS_BUFD_DIR
SYS_BUFD_nOE
SYS_RDY
5_SYS_nRES
SYS_nNMI
SYS_nIRQ
SYS_PHI0
SYS_DBE
5_SYS_VCC_PWR
SYS_AUX_IO[6..0]
SYS_AUX_O[3..0]
1
File: sys_plug_and_buffers.sch
Sheet: memory
MEM_A[20..0]
MEM_D[7..0]
MEM_nOE
MEM_nWE
MEM_FL_nCE
MEM_RAM_nCE[3..0]
MEM_BB_nCE
2
File: memory.sch
Sheet: expansion_headers
exp_PORTA[7..0]
exp_PORTA_DIR
exp_PORTA_nOE
exp_PORTB[7..0]
exp_PORTC[11..0]
exp_PORTD[11..0]
exp_PORTEFG[11..0]
exp_PORTE_nOE
exp_PORTF_nOE
exp_PORTG_nOE
5
File: expansion_headers.sch
Sheet: UI
LED[3..0]
btnuser[1..0]
6
File: UI.sch
Sheet: fpga_top
MEM_A[20..0]
MEM_D_io[7..0]
MEM_nOE
MEM_nWE
MEM_FL_nCE
MEM_RAM_nCE[3..0]
SYS_A[15..0]
SYS_D[7..0]
SYS_SYNC
SYS_RnW
SYS_PHI1
SYS_PHI2
SYS_BUFD_DIR
SYS_BUFD_nOE
SYS_RDY
SYS_nNMI
SYS_nIRQ
SYS_PHI0
SYS_DBE
SYS_AUX_IO[6..0]
SYS_AUX_O[3..0]
exp_PORTA[7..0]
exp_PORTA_DIR
exp_PORTA_nOE
exp_PORTB[7..0]
exp_PORTC[11..0]
exp_PORTD[11..0]
exp_PORTEFG[11..0]
exp_PORTE_nOE
exp_PORTF_nOE
exp_PORTG_nOE
HDMI_D0P
HDMI_D0N
HDMI_D1P
HDMI_D1N
HDMI_D2P
HDMI_D2N
HDMI_CKP
HDMI_CKN
HDMI_SCL
HDMI_SDA
HDMI_HPD
SND_L
SND_R
SD_CS
SD_MOSI
SD_CLK
SD_MISO
SD_DET
I2C_SCL
I2C_SDA
LED[3..0]
SUP_nRES
CLK_48M
ALTERA_nSTATUS
ALTERA_nCONFIG
ALTERA_CONF_DONE
ALTERA_CONFIG_SEL
btnuser[1..0]
File: fpga_top.sch
Sheet: fpga_power
ALTERA_nSTATUS
ALTERA_nCONFIG
ALTERA_CONF_DONE
ALTERA_CONFIG_SEL
File: fpga_power.sch
5_SYS_VCC_PWR
5_SYS_nRES
SUP_nRES
MEM_BB_nCE_BB
MEM_RAM_nCEO
CLK_48M
9
Sheet: power
File: power.sch
HDMI_D0P
HDMI_D0N
HDMI_D1P
HDMI_D1N
HDMI_D2P
HDMI_D2N
HDMI_CKP
HDMI_CKN
HDMI_SCL
HDMI_SDA
HDMI_HPD
SND_L
SND_R
3
Sheet: soundvideo
File: soundvideo.sch
SD_CS
SD_MOSI
SD_CLK
SD_MISO
SD_DET
I2C_SDA
I2C_SCL
4
Sheet: extras
File: extras.sch
fixed: clk/sysd0, jtag, u22 footprint
Dossytronics
Sheet: /
File: blit-cpu-mk3.sch
Title: Mk.3 Blitter FPGA development board
Size: A4
Date: 2021-08-14
Rev: 3.03
KiCad E.D.A. kicad (5.1.6)-1
Id: 1/11


U54A
74CB3T16211
1nOE
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
1A9
1A10
1A11
1A12
1B1
1B2
1B3
1B4
1B5
1B6
1B7
1B8
1B9
1B10
1B11
1B12
5_SYS_nNMI
5_SYS_nIRQ
5_SYS_RDY
5_SYS_DBE
5_SYS_PHI0
5_SYS_AUX_IO_0
5_SYS_AUX_IO_1
5_SYS_AUX_IO_2
5_SYS_AUX_IO_3
5_SYS_AUX_IO_4
5_SYS_AUX_IO_5
5_SYS_AUX_IO_6
SYS_nNMI
SYS_nIRQ
SYS_RDY
SYS_DBE
SYS_PHI0
SYS_AUX_IO_0
SYS_AUX_IO_1
SYS_AUX_IO_2
SYS_AUX_IO_3
SYS_AUX_IO_4
SYS_AUX_IO_5
SYS_AUX_IO_6
J16
SYS AUX
nVP
nML
E/OSCO
nSO?
PHI1_in?
HS
VS
DISEN?
5C_SYS_AUX_O0
5C_SYS_AUX_O1
5C_SYS_AUX_O2
5C_SYS_AUX_O3
5_SYS_AUX_IO_0
5_SYS_AUX_IO_1
5_SYS_AUX_IO_2
5_SYS_AUX_IO_3
5_SYS_AUX_IO_4
5_SYS_AUX_IO_5
5_SYS_AUX_IO_6
5_SYS_VCC_PWR
5_SYS_VCC_PWR
SYS_AUX_O[3..0]
SYS_AUX_IO_[6..0]
SYS_A[15..0]
SYS_D[7..0]
SYS_SYNC
SYS_RnW
SYS_PHI1
SYS_PHI2
SYS_BUFD_DIR
SYS_BUFD_OE
5_SYS_nRES
SYS_AUX_O[3..0]
SYS_AUX_IO[6..0]
SYS_A[15..0]
SYS_D[7..0]
SYS_SYNC
SYS_RnW
SYS_PHI1
SYS_PHI2
SYS_BUFD_DIR
SYS_BUFD_nOE
5_SYS_nRES
5C_SYS_AUX_O1
5C_SYS_nMLorVss
J11
nML out
5C_SYS_AUX_O0
5C_SYS_nVPor_Vss
J12
nVP out
5C_SYS_PHI1
5C_SYS_PHI1_IO
5_SYS_AUX_IO_1
J13
phi1/abort
B+/6512 phi1 is input
65816 is nABORT input
5_SYS_nSO
5C_SYS_816E
J14
nSO in
SOB/M/X
E/OSCO
U11
74LVC4245A
5C_SYS_PHI2
5C_SYS_AUX_O0
5C_SYS_AUX_O1
5C_SYS_AUX_O2
5C_SYS_AUX_O3
5C_SYS_PHI1
5C_SYS_SYNC
5C_SYS_RnW
SYS_PHI2
SYS_AUX_O0
SYS_AUX_O1
SYS_AUX_O2
SYS_AUX_O3
SYS_PHI1
SYS_SYNC
SYS_RnW
U12
74LVC4245A
5C_SYS_A0
5C_SYS_A1
5C_SYS_A2
5C_SYS_A3
5C_SYS_A4
5C_SYS_A5
5C_SYS_A6
5C_SYS_A7
SYS_A0
SYS_A1
SYS_A2
SYS_A3
SYS_A4
SYS_A5
SYS_A6
SYS_A7
SYS_A[15..0]
U13
74LVC4245A
5C_SYS_D7
5C_SYS_D6
5C_SYS_D5
5C_SYS_D4
5C_SYS_D3
5C_SYS_D2
5C_SYS_D1
5C_SYS_D0
SYS_BUFD_DIR
SYS_BUFD_nOE
SYS_D7
SYS_D6
SYS_D5
SYS_D4
SYS_D3
SYS_D2
SYS_D1
SYS_D0
U14
74LVC4245A
5C_SYS_A8
5C_SYS_A9
5C_SYS_A10
5C_SYS_A11
5C_SYS_A15
5C_SYS_A14
5C_SYS_A13
5C_SYS_A12
SYS_A8
SYS_A9
SYS_A10
SYS_A11
SYS_A15
SYS_A14
SYS_A13
SYS_A12
J1
SYS
PLUG!
5C_SYS_D0
5C_SYS_D1
5C_SYS_D2
5C_SYS_D3
5C_SYS_D4
5C_SYS_D5
5C_SYS_D6
5C_SYS_D7
5C_SYS_816E
5_SYS_VCC_PWR
5C_SYS_nMLorVss
5C_SYS_nVPor_Vss
5_SYS_DBE
5C_SYS_PHI1_IO
5C_SYS_PHI2
5_SYS_PHI0
5C_SYS_A0
5C_SYS_A1
5C_SYS_A2
5C_SYS_A3
5C_SYS_A4
5C_SYS_A5
5C_SYS_A6
5C_SYS_A7
5C_SYS_A8
5C_SYS_A9
5C_SYS_A10
5C_SYS_A11
5C_SYS_A12
5C_SYS_A13
5C_SYS_A14
5C_SYS_A15
5_SYS_nSO
5_SYS_RDY
5_SYS_nRES
5_SYS_nNMI
5_SYS_nIRQ
5C_SYS_RnW
5C_SYS_SYNC
Check 4245 Footprints – SOP ones were too narrow?
C151
C152
C153
C154
C131
C132
C133
C134
100n
fixed: clk/sysd0, jtag, u22 footprint
Dossytronics
Sheet: /sys_plug_and_buffers/
File: sys_plug_and_buffers.sch
Title: Mk.3 Blitter FPGA development board
Size: A4
Date: 2021-08-14
Rev: 3.03
KiCad E.D.A. kicad (5.1.6)-1
Id: 2/11









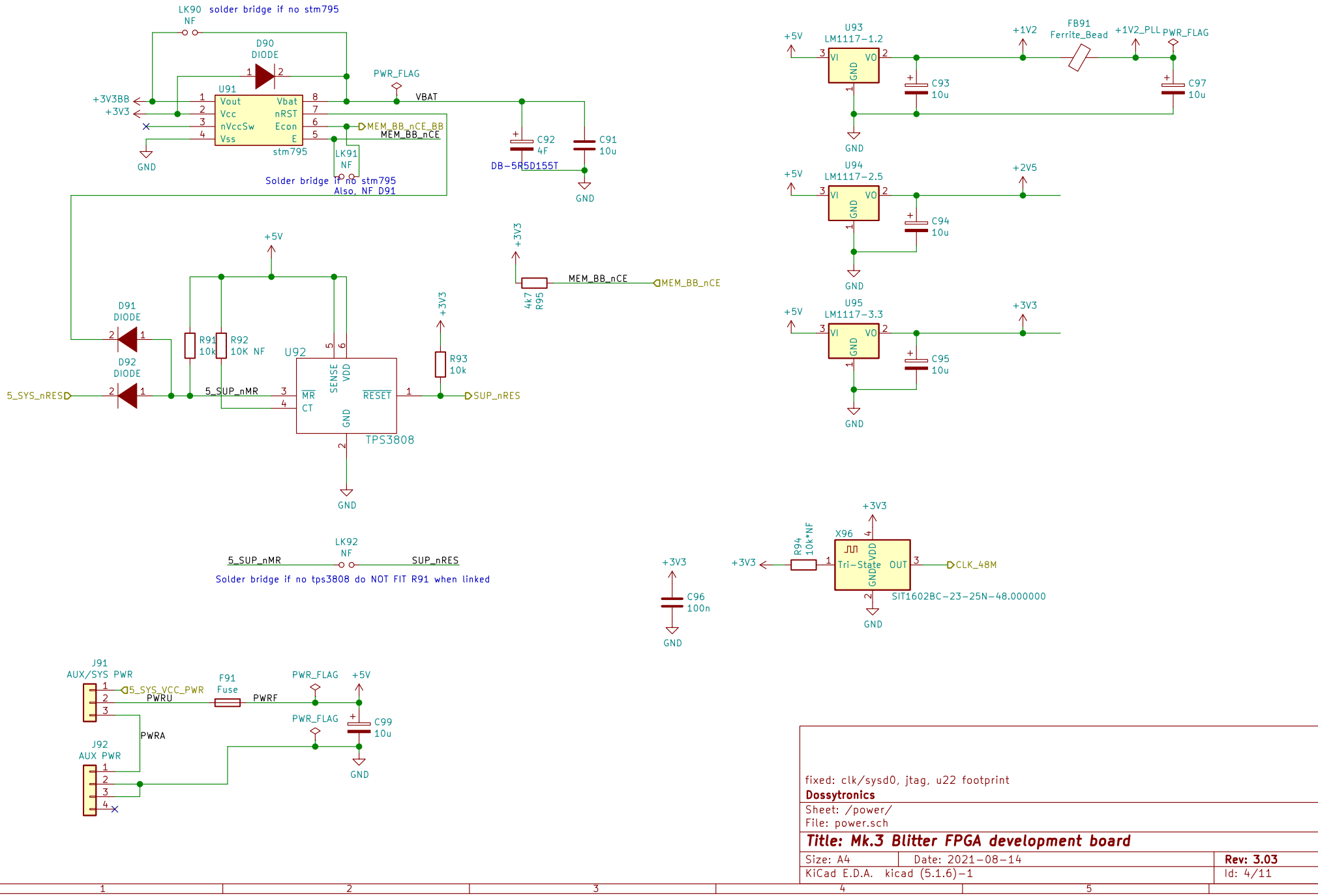
fixed: clk/sysd0, jtag, u22 footprint

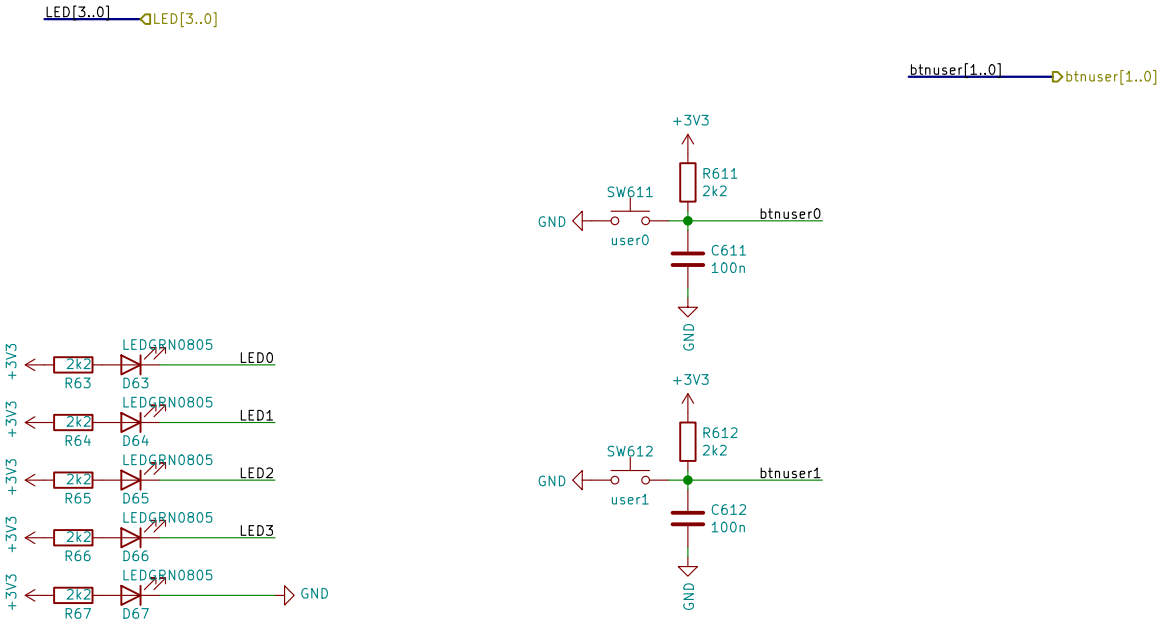
Dossytronics

Sheet: /memory/
File: memory.sch

Title: Mk.3 Blitter FPGA development board

Size: A4	Date: 2021-08-14	**Rev: 3.03**
KiCad E.D.A. kicad (5.1.6)-1		Id: 3/11


LK90 solder bridge if no stm795
NF
D90
DIODE
PWR_FLAG
U91
Vout
Vcc
nVccSw
Vss
Vbat
nRST
Econ
E
stm795
+3V3BB
+3V3
GND
VBAT
MEM_BB_nCE_BB
MEM_BB_nCE
LK91
NF
Solder bridge if no stm795
Also, NF D91
C92
4F
DB-5R5D155T
C91
10u
GND
U93
LM1117-1.2
+5V
VI
VO
GND
+1V2
FB91
Ferrite_Bead
+1V2_PLL
PWR_FLAG
C93
10u
C97
10u
U94
LM1117-2.5
+2V5
C94
10u
U95
LM1117-3.3
+3V3
C95
10u
+3V3
4k7
R95
MEM_BB_nCE
MEM_BB_nCE
D91
DIODE
D92
DIODE
R91
10k
R92
10K NF
U92
SENSE
VDD
MR
CT
RESET
GND
TPS3808
R93
10k
5_SYS_nRES
5_SUP_nMR
SUP_nRES
LK92
NF
5_SUP_nMR
SUP_nRES
Solder bridge if no tps3808 do NOT FIT R91 when linked
C96
100n
R94
10k*NF
X96
Tri-State
OUT
VDD
GND
CLK_48M
SIT1602BC-23-25N-48.000000
J91
AUX/SYS PWR
5_SYS_VCC_PWR
PWRU
F91
Fuse
PWRF
PWR_FLAG
+5V
C99
10u
PWRA
J92
AUX PWR
fixed: clk/sysd0, jtag, u22 footprint
Dossytronics
Sheet: /power/
File: power.sch
Title: Mk.3 Blitter FPGA development board
Size: A4
Date: 2021-08-14
Rev: 3.03
KiCad E.D.A. kicad (5.1.6)-1
Id: 4/11



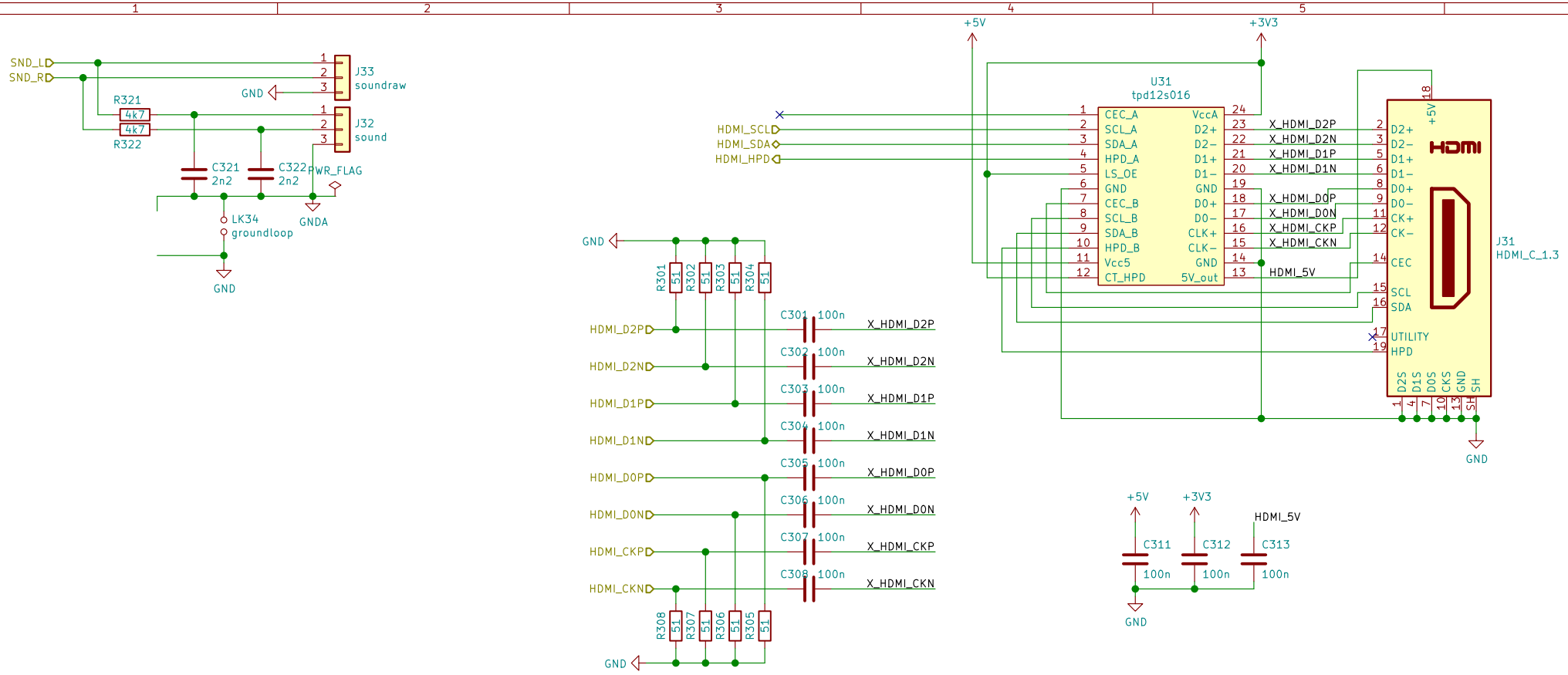
fixed: clk/sysd0, jtag, u22 footprint

Dossytronics

Sheet: /UI/
File: UI.sch

Title: Mk.3 Blitter FPGA development board

Size: A4	Date: 2021-08-14	**Rev: 3.03**
KiCad E.D.A. kicad (5.1.6)-1		Id: 5/11



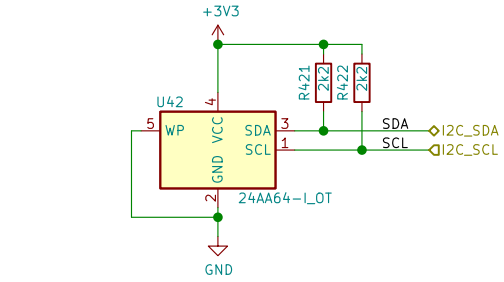
fixed: clk/sysd0, jtag, u22 footprint

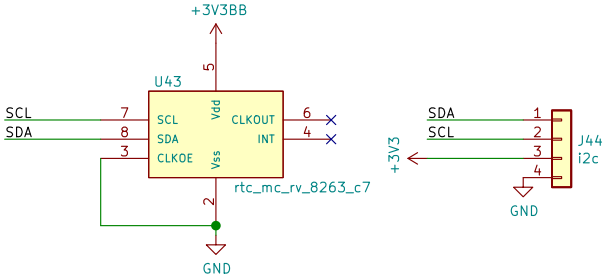
Dossytronics

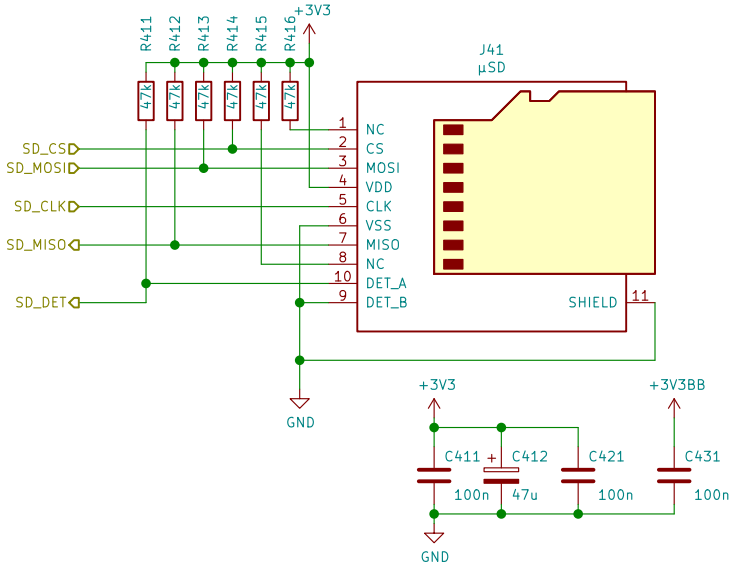
Sheet: /soundvideo/
File: soundvideo.sch

Title: Mk.3 Blitter FPGA development board

Size: A4	Date: 2021−08−14	**Rev: 3.03**
KiCad E.D.A. kicad (5.1.6)−1		Id: 6/11







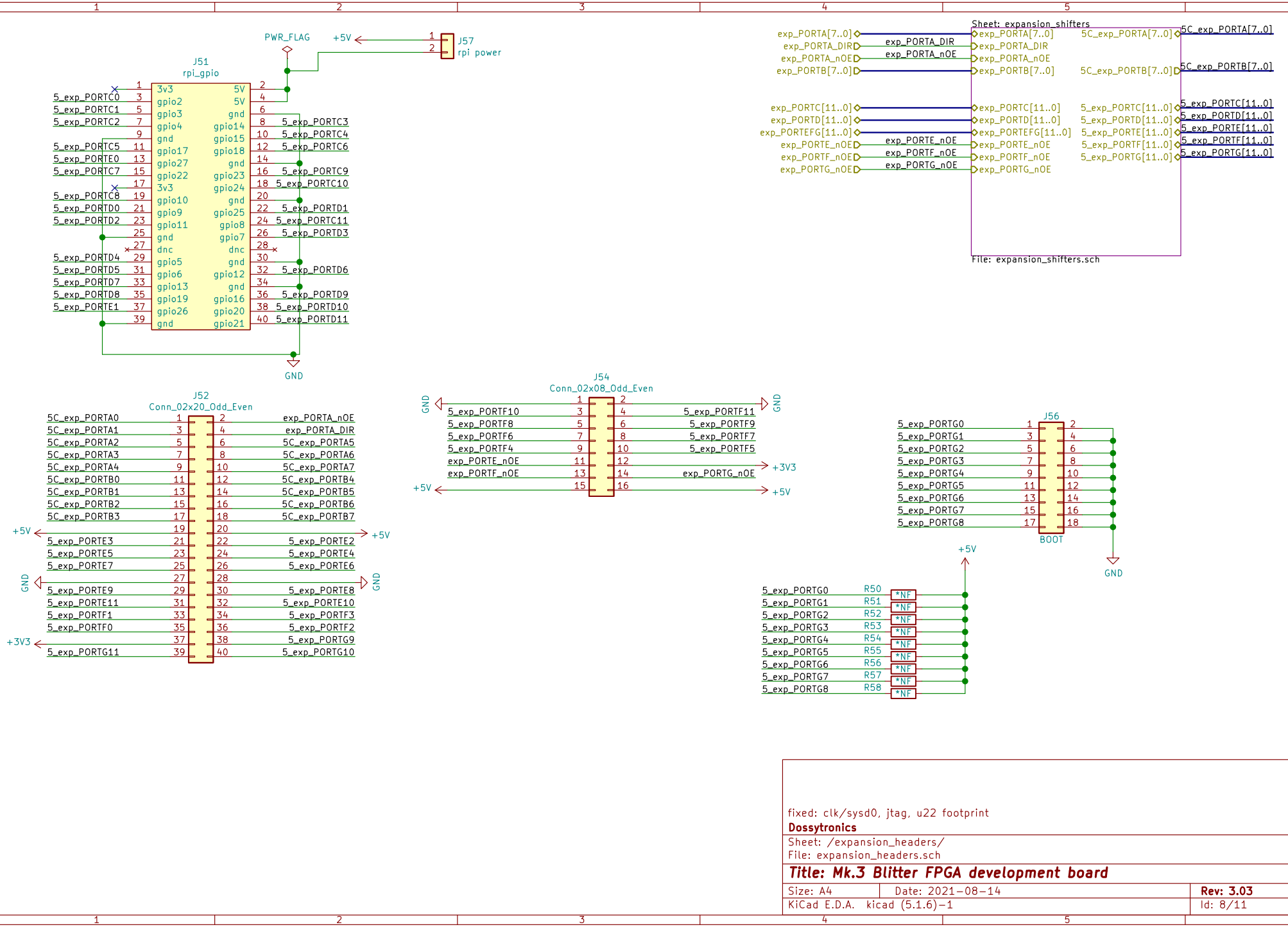
fixed: clk/sysd0, jtag, u22 footprint

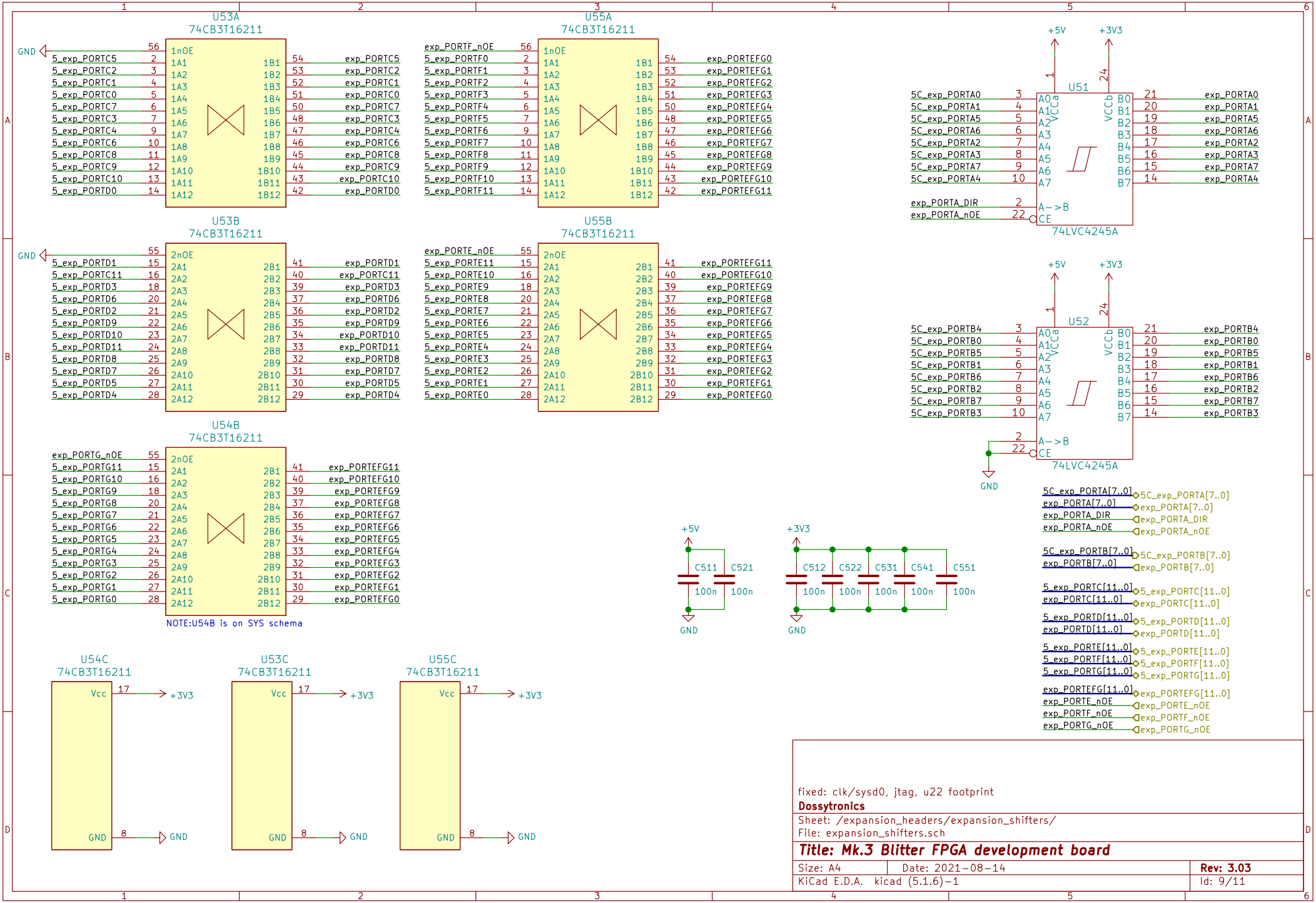
Dossytronics

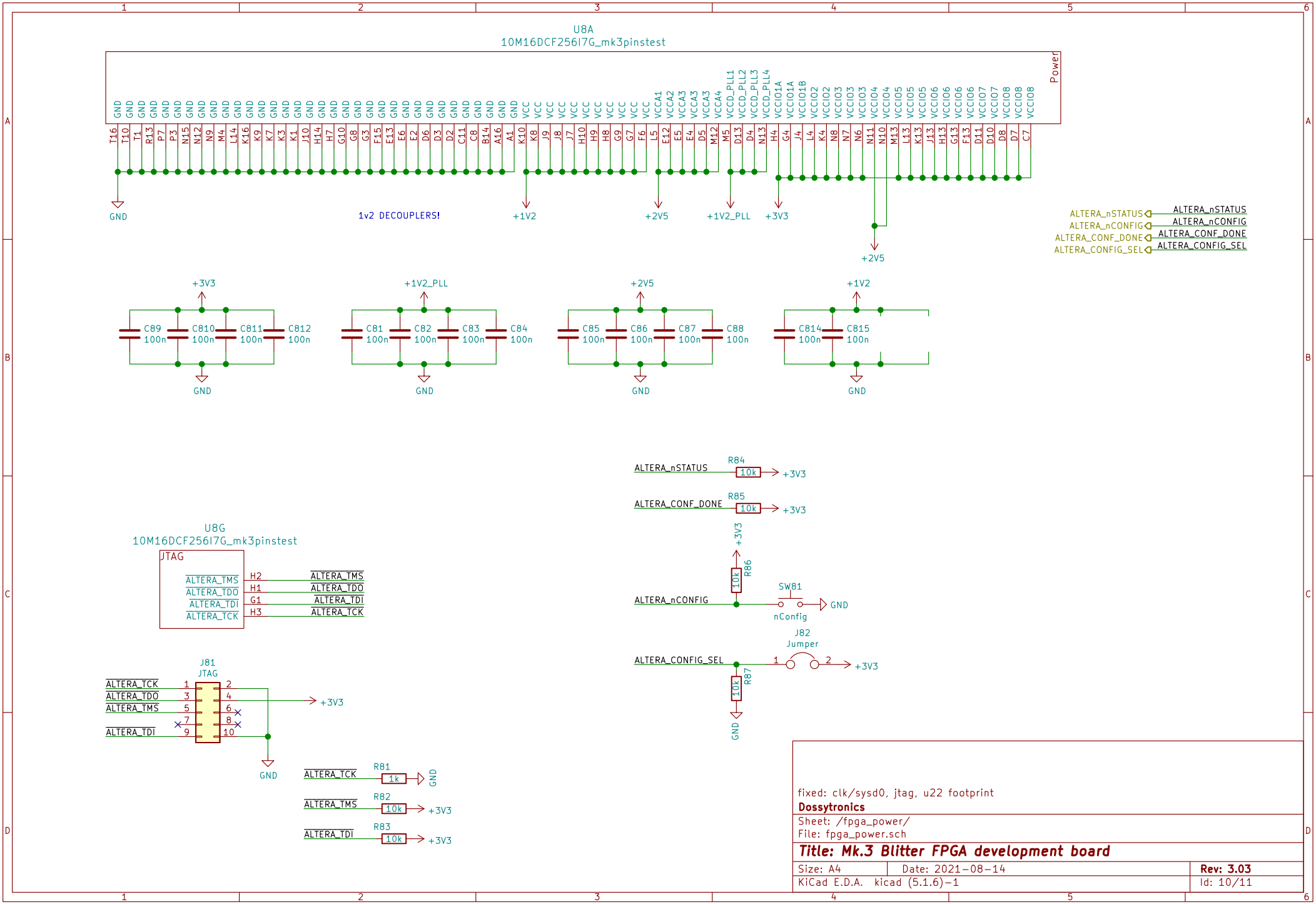
Sheet: /extras/
File: extras.sch

Title: Mk.3 Blitter FPGA development board

Size: A4	Date: 2021-08-14	**Rev: 3.03**
KiCad E.D.A. kicad (5.1.6)-1		Id: 7/11


PWR_FLAG
+5V
J57
rpi power
J51
rpi_gpio
3v3
gpio2
gpio3
gpio4
gnd
gpio17
gpio27
gpio22
3v3
gpio10
gpio9
gpio11
gnd
dnc
gpio5
gpio6
gpio13
gpio19
gpio26
gnd
5V
5V
gnd
gpio14
gpio15
gpio18
gnd
gpio23
gpio24
gnd
gpio25
gpio8
gpio7
dnc
gnd
gpio12
gnd
gpio16
gpio20
gpio21
5_exp_PORTC0
5_exp_PORTC1
5_exp_PORTC2
5_exp_PORTC5
5_exp_PORTE0
5_exp_PORTC7
5_exp_PORTC8
5_exp_PORTD0
5_exp_PORTD2
5_exp_PORTD4
5_exp_PORTD5
5_exp_PORTD7
5_exp_PORTD8
5_exp_PORTE1
5_exp_PORTC3
5_exp_PORTC4
5_exp_PORTC6
5_exp_PORTC9
5_exp_PORTC10
5_exp_PORTD1
5_exp_PORTC11
5_exp_PORTD3
5_exp_PORTD6
5_exp_PORTD9
5_exp_PORTD10
5_exp_PORTD11
GND
Sheet: expansion_shifters
exp_PORTA[7..0]
exp_PORTA_DIR
exp_PORTA_nOE
exp_PORTB[7..0]
exp_PORTC[11..0]
exp_PORTD[11..0]
exp_PORTEFG[11..0]
exp_PORTE_nOE
exp_PORTF_nOE
exp_PORTG_nOE
exp_PORTA[7..0]
exp_PORTA_DIR
exp_PORTA_nOE
exp_PORTB[7..0]
exp_PORTC[11..0]
exp_PORTD[11..0]
exp_PORTEFG[11..0]
exp_PORTE_nOE
exp_PORTF_nOE
exp_PORTG_nOE
5C_exp_PORTA[7..0]
5C_exp_PORTB[7..0]
5_exp_PORTC[11..0]
5_exp_PORTD[11..0]
5_exp_PORTE[11..0]
5_exp_PORTF[11..0]
5_exp_PORTG[11..0]
5C_exp_PORTA[7..0]
5C_exp_PORTB[7..0]
5_exp_PORTC[11..0]
5_exp_PORTD[11..0]
5_exp_PORTE[11..0]
5_exp_PORTF[11..0]
5_exp_PORTG[11..0]
File: expansion_shifters.sch
J52
Conn_02x20_Odd_Even
5C_exp_PORTA0
5C_exp_PORTA1
5C_exp_PORTA2
5C_exp_PORTA3
5C_exp_PORTA4
5C_exp_PORTB0
5C_exp_PORTB1
5C_exp_PORTB2
5C_exp_PORTB3
5_exp_PORTE3
5_exp_PORTE5
5_exp_PORTE7
5_exp_PORTE9
5_exp_PORTE11
5_exp_PORTF1
5_exp_PORTF0
5_exp_PORTG11
exp_PORTA_nOE
exp_PORTA_DIR
5C_exp_PORTA5
5C_exp_PORTA6
5C_exp_PORTA7
5C_exp_PORTB4
5C_exp_PORTB5
5C_exp_PORTB6
5C_exp_PORTB7
5_exp_PORTE2
5_exp_PORTE4
5_exp_PORTE6
5_exp_PORTE8
5_exp_PORTE10
5_exp_PORTF3
5_exp_PORTF2
5_exp_PORTG9
5_exp_PORTG10
+5V
+5V
GND
GND
+3V3
J54
Conn_02x08_Odd_Even
5_exp_PORTF10
5_exp_PORTF8
5_exp_PORTF6
5_exp_PORTF4
exp_PORTE_nOE
exp_PORTF_nOE
5_exp_PORTF11
5_exp_PORTF9
5_exp_PORTF7
5_exp_PORTF5
exp_PORTG_nOE
GND
GND
+3V3
+5V
+5V
J56
5_exp_PORTG0
5_exp_PORTG1
5_exp_PORTG2
5_exp_PORTG3
5_exp_PORTG4
5_exp_PORTG5
5_exp_PORTG6
5_exp_PORTG7
5_exp_PORTG8
BOOT
GND
+5V
R50
R51
R52
R53
R54
R55
R56
R57
R58
*NF
fixed: clk/sysd0, jtag, u22 footprint
Dossytronics
Sheet: /expansion_headers/
File: expansion_headers.sch
Title: Mk.3 Blitter FPGA development board
Size: A4
Date: 2021-08-14
Rev: 3.03
KiCad E.D.A. kicad (5.1.6)-1
Id: 8/11


U53A
74CB3T16211
GND
5_exp_PORTC5
5_exp_PORTC2
5_exp_PORTC1
5_exp_PORTC0
5_exp_PORTC7
5_exp_PORTC3
5_exp_PORTC4
5_exp_PORTC6
5_exp_PORTC8
5_exp_PORTC9
5_exp_PORTC10
5_exp_PORTD0
exp_PORTC5
exp_PORTC2
exp_PORTC1
exp_PORTC0
exp_PORTC7
exp_PORTC3
exp_PORTC4
exp_PORTC6
exp_PORTC8
exp_PORTC9
exp_PORTC10
exp_PORTD0
U55A
74CB3T16211
exp_PORTF_nOE
5_exp_PORTF0
5_exp_PORTF1
5_exp_PORTF2
5_exp_PORTF3
5_exp_PORTF4
5_exp_PORTF5
5_exp_PORTF6
5_exp_PORTF7
5_exp_PORTF8
5_exp_PORTF9
5_exp_PORTF10
5_exp_PORTF11
exp_PORTEFG0
exp_PORTEFG1
exp_PORTEFG2
exp_PORTEFG3
exp_PORTEFG4
exp_PORTEFG5
exp_PORTEFG6
exp_PORTEFG7
exp_PORTEFG8
exp_PORTEFG9
exp_PORTEFG10
exp_PORTEFG11
U53B
74CB3T16211
GND
5_exp_PORTD1
5_exp_PORTC11
5_exp_PORTD3
5_exp_PORTD6
5_exp_PORTD2
5_exp_PORTD9
5_exp_PORTD10
5_exp_PORTD11
5_exp_PORTD8
5_exp_PORTD7
5_exp_PORTD5
5_exp_PORTD4
exp_PORTD1
exp_PORTC11
exp_PORTD3
exp_PORTD6
exp_PORTD2
exp_PORTD9
exp_PORTD10
exp_PORTD11
exp_PORTD8
exp_PORTD7
exp_PORTD5
exp_PORTD4
U55B
74CB3T16211
exp_PORTE_nOE
5_exp_PORTE11
5_exp_PORTE10
5_exp_PORTE9
5_exp_PORTE8
5_exp_PORTE7
5_exp_PORTE6
5_exp_PORTE5
5_exp_PORTE4
5_exp_PORTE3
5_exp_PORTE2
5_exp_PORTE1
5_exp_PORTE0
exp_PORTEFG11
exp_PORTEFG10
exp_PORTEFG9
exp_PORTEFG8
exp_PORTEFG7
exp_PORTEFG6
exp_PORTEFG5
exp_PORTEFG4
exp_PORTEFG3
exp_PORTEFG2
exp_PORTEFG1
exp_PORTEFG0
U54B
74CB3T16211
exp_PORTG_nOE
5_exp_PORTG11
5_exp_PORTG10
5_exp_PORTG9
5_exp_PORTG8
5_exp_PORTG7
5_exp_PORTG6
5_exp_PORTG5
5_exp_PORTG4
5_exp_PORTG3
5_exp_PORTG2
5_exp_PORTG1
5_exp_PORTG0
exp_PORTEFG11
exp_PORTEFG10
exp_PORTEFG9
exp_PORTEFG8
exp_PORTEFG7
exp_PORTEFG6
exp_PORTEFG5
exp_PORTEFG4
exp_PORTEFG3
exp_PORTEFG2
exp_PORTEFG1
exp_PORTEFG0
NOTE:U54B is on SYS schema
U54C
74CB3T16211
Vcc
GND
+3V3
GND
U53C
74CB3T16211
Vcc
GND
+3V3
GND
U55C
74CB3T16211
Vcc
GND
+3V3
GND
+5V
+3V3
U51
5C_exp_PORTA0
5C_exp_PORTA1
5C_exp_PORTA5
5C_exp_PORTA6
5C_exp_PORTA2
5C_exp_PORTA3
5C_exp_PORTA7
5C_exp_PORTA4
exp_PORTA_DIR
exp_PORTA_nOE
exp_PORTA0
exp_PORTA1
exp_PORTA5
exp_PORTA6
exp_PORTA2
exp_PORTA3
exp_PORTA7
exp_PORTA4
74LVC4245A
+5V
+3V3
U52
5C_exp_PORTB4
5C_exp_PORTB0
5C_exp_PORTB5
5C_exp_PORTB1
5C_exp_PORTB6
5C_exp_PORTB2
5C_exp_PORTB7
5C_exp_PORTB3
exp_PORTB4
exp_PORTB0
exp_PORTB5
exp_PORTB1
exp_PORTB6
exp_PORTB2
exp_PORTB7
exp_PORTB3
74LVC4245A
GND
+5V
C511
C521
100n
100n
GND
+3V3
C512
C522
C531
C541
C551
100n
100n
100n
100n
100n
GND
5C_exp_PORTA[7..0]
exp_PORTA[7..0]
exp_PORTA_DIR
exp_PORTA_nOE
5C_exp_PORTB[7..0]
exp_PORTB[7..0]
5_exp_PORTC[11..0]
exp_PORTC[11..0]
5_exp_PORTD[11..0]
exp_PORTD[11..0]
5_exp_PORTE[11..0]
5_exp_PORTF[11..0]
5_exp_PORTG[11..0]
exp_PORTEFG[11..0]
exp_PORTE_nOE
exp_PORTF_nOE
exp_PORTG_nOE
fixed: clk/sysd0, jtag, u22 footprint
Dossytronics
Sheet: /expansion_headers/expansion_shifters/
File: expansion_shifters.sch
Title: Mk.3 Blitter FPGA development board
Size: A4
Date: 2021-08-14
Rev: 3.03
KiCad E.D.A. kicad (5.1.6)-1
Id: 9/11


U8A
10M16DCF256I7G_mk3pinstest
Power
1v2 DECOUPLERS!
GND
+1V2
+2V5
+1V2_PLL
+3V3
ALTERA_nSTATUS
ALTERA_nCONFIG
ALTERA_CONF_DONE
ALTERA_CONFIG_SEL
C89 100n
C810 100n
C811 100n
C812 100n
C81 100n
C82 100n
C83 100n
C84 100n
C85 100n
C86 100n
C87 100n
C88 100n
C814 100n
C815 100n
U8G
10M16DCF256I7G_mk3pinstest
JTAG
ALTERA_TMS H2
ALTERA_TDO H1
ALTERA_TDI G1
ALTERA_TCK H3
J81
JTAG
R84 10k
R85 10k
R86 10k
SW81
nConfig
J82
Jumper
R87 10k
R81 1k
R82 10k
R83 10k
fixed: clk/sysd0, jtag, u22 footprint
Dossytronics
Sheet: /fpga_power/
File: fpga_power.sch
Title: Mk.3 Blitter FPGA development board
Size: A4
Date: 2021-08-14
Rev: 3.03
KiCad E.D.A. kicad (5.1.6)-1
Id: 10/11


U8B
10M16DCF256I7G_mk3pinstest
IOBank_8
ALTERA_nSTATUS F7
ALTERA_nCONFIG E8
ALTERA_CONF_DONE E7
ALTERA_CONFIG_SEL F8
exp_PORTF_nOE B3
exp_PORTE_nOE A3
exp_PORTEFG_io_9 B8
exp_PORTEFG_io_8 A8
exp_PORTEFG_io_7 B7
exp_PORTEFG_io_6 A7
exp_PORTEFG_io_5 B6
exp_PORTEFG_io_4 A6
exp_PORTEFG_io_3 B5
exp_PORTEFG_io_2 A5
exp_PORTEFG_io_11 B9
exp_PORTEFG_io_10 A9
exp_PORTEFG_io_1 B4
exp_PORTEFG_io_0 A4
exp_PORTA_nOE_o C5
exp_PORTA_io_7 B12
exp_PORTA_io_6 D9
exp_PORTA_io_5 C9
exp_PORTA_io_3 C10
exp_PORTA_io_2 F9
exp_PORTA_io_1 E9
exp_PORTA_io_0 C6
SYS_AUX_io_6 A10
SYS_AUX_io_5 B10
SYS_AUX_io_4 A11
SYS_AUX_io_2 B11
SYS_AUX_io_0 A12
MEM_A_o_10 A2
U8C
10M16DCF256I7G_mk3pinstest
IOBank_7
exp_PORTB_o_7 F11
exp_PORTB_o_6 A14
exp_PORTB_o_5 B13
exp_PORTB_o_4 A13
exp_PORTB_o_3 A15
exp_PORTB_o_2 C13
exp_PORTB_o_1 D12
exp_PORTB_o_0 C12
exp_PORTA_io_4 E11
SYS_AUX_io_3 F10
SYS_AUX_io_1 E10
BTNUSER_i_1 F12
U8L
10M16DCF256I7G_mk3pinstest
IOBank_4
SD_MISO_i R11
SD_DET_i T12
NOTCONN R12
NOTCONN T13
HDMI_D2_o(n) M11
HDMI_D2_o L10
HDMI_D1_o(n) M10
HDMI_D1_o L9
HDMI_D0_o(n) P13
HDMI_D0_o P12
HDMI_CK_o(n) P10
HDMI_CK_o P11
U8E
10M16DCF256I7G_mk3pinstest
IOBank_6
exp_PORTG_nOE B16
SYS_nNMI_i B15
SYS_nIRQ_i C16
SYS_nDBE_i D16
SYS_RDY_i C15
SYS_PHI0_i D15
SYS_D_io_7 E15
SYS_D_io_6 F16
SYS_D_io_5 G15
SYS_D_io_4 G16
SYS_D_io_3 H11
SYS_D_io_2 G14
SYS_D_io_1 H12
SYS_BUF_D_nOE_o F14
SYS_BUF_D_DIR_o E16
SYS_A_o_9 H16
SYS_A_o_8 H15
SYS_A_o_7 J15
SYS_A_o_6 K15
SYS_A_o_15 J12
SYS_A_o_11 J16
SYS_A_o_10 J14
LED_o_3 G12
LED_o_2 E14
LED_o_1 G11
LED_o_0 D14
CLK_48M_i J11
BTNUSER_i_0 C14
U8K
10M16DCF256I7G_mk3pinstest
IOBank_3
exp_PORTD_io_9 R1
exp_PORTD_io_6 T2
exp_PORTD_io_2 R2
exp_PORTD_io_10 P2
exp_PORTD_io_0 N5
exp_PORTC_io_9 P5
exp_PORTC_io_8 P6
exp_PORTC_io_7 T4
exp_PORTC_io_6 R3
exp_PORTC_io_5 T6
exp_PORTC_io_4 T3
exp_PORTC_io_3 R4
exp_PORTC_io_2 R6
exp_PORTC_io_10 P4
exp_PORTC_io_1 T5
exp_PORTC_io_0 R5
SYS_D_io_0 P8
SUP_nRESET_i R8
SND_R_o T9
SND_L_o M9
SD_MOSI_o T11
SD_CS_o R10
SD_CLK_o P9
NOTCONN M7
MEM_RAM_nCE_o_3 M8
MEM_RAM_nCE_o_2 M6
MEM_A_o_20 R7
MEM_A_o_19 T7
MEM_A_o_15 L8
MEM_A_o_12 L7
I2C_SDA_io R9
I2C_SCL_o T8
U8I
10M16DCF256I7G_mk3pinstest
IOBank_2
exp_PORTD_io_8 N2
exp_PORTD_io_7 N1
exp_PORTD_io_5 M2
exp_PORTD_io_4 M1
exp_PORTD_io_3 M3
exp_PORTD_io_11 P1
exp_PORTD_io_1 N4
exp_PORTC_io_11 N3
MEM_nWE_o K6
MEM_A_o_7 L6
MEM_A_o_6 L1
MEM_A_o_5 L2
MEM_A_o_4 L3
MEM_A_o_18 K5
MEM_A_o_16 K2
MEM_A_o_13 J6
U8J
10M16DCF256I7G_mk3pinstest
IOBank_5
SYS_SYNC_o N14
SYS_RnW_o M16
SYS_PHI2_o R15
SYS_PHI1_o N16
SYS_A_o_5 L16
SYS_A_o_4 L15
SYS_A_o_3 K14
SYS_A_o_2 L12
SYS_A_o_14 K11
SYS_A_o_13 K12
SYS_A_o_12 L11
SYS_A_o_1 M15
SYS_A_o_0 M14
SYS_AUX_o_3 P15
SYS_AUX_o_2 P16
SYS_AUX_o_1 P14
SYS_AUX_o_0 R16
HDMI_SDA_io R14
HDMI_SCL_o T15
HDMI_HPD_i T14
U8D
10M16DCF256I7G_mk3pinstest
IOBank_1A
exp_PORTA_DIR_o C4
MEM_nOE_o C3
MEM_RAM_nCE_o_0 F5
MEM_FL_nCE_o B2
MEM_D_io_7 B1
MEM_D_io_6 C2
MEM_D_io_5 C1
MEM_D_io_4 D1
MEM_D_io_3 E3
MEM_D_io_2 E1
MEM_D_io_1 F2
MEM_D_io_0 F1
MEM_A_o_8 H5
MEM_A_o_11 G5
MEM_A_o_1 G2
MEM_A_o_0 F4
U8H
10M16DCF256I7G_mk3pinstest
IOBank_1B
MEM_RAM_nCE_o_1 G6
MEM_A_o_9 H6
MEM_A_o_3 J1
MEM_A_o_2 J2
MEM_A_o_17 J3
MEM_A_o_14 J5
MEM_A_o_14
MEM_A_o_17
MEM_A_o_2
MEM_A_o_3
MEM_A_o_9
MEM_RAM_nCE_o_1
MEM_A_o_[20..0]
MEM_D_io_[7..0]
MEM_nOE_o
MEM_nWE_o
MEM_FL_nCE_o
MEM_RAM_nCE_o_[3..0]
MEM_A[20..0]
MEM_D_io[7..0]
MEM_nOE
MEM_nWE
MEM_FL_nCE
MEM_RAM_nCE[3..0]
SD_CS_o
SD_MOSI_o
SD_CLK_o
SD_MISO_i
SD_DET_i
SD_CS
SD_MOSI
SD_CLK
SD_MISO
SD_DET
SYS_A_o_[15..0]
SYS_D_io_[7..0]
SYS_SYNC_o
SYS_RnW_o
SYS_PHI1_o
SYS_PHI2_o
SYS_BUF_D_DIR_o
SYS_BUF_D_nOE_o
SYS_RDY_i
SYS_nNMI_i
SYS_nIRQ_i
SYS_PHI0_i
SYS_nDBE_i
SYS_AUX_io_[6..0]
SYS_AUX_o_[3..0]
SYS_A[15..0]
SYS_D[7..0]
SYS_SYNC
SYS_RnW
SYS_PHI1
SYS_PHI2
SYS_BUFD_DIR
SYS_BUFD_nOE
SYS_RDY
SYS_nNMI
SYS_nIRQ
SYS_PHI0
SYS_DBE
SYS_AUX_IO[6..0]
SYS_AUX_O[3..0]
I2C_SCL_o
I2C_SDA_io
I2C_SCL
I2C_SDA
LED_o_[3..0]
LED[3..0]
SUP_nRESET_i
SUP_nRES
CLK_48M_i
BTNUSER_i_[1..0]
CLK_48M
btnuser[1..0]
ALTERA_nSTATUS
ALTERA_nCONFIG
ALTERA_CONF_DONE
ALTERA_CONFIG_SEL
exp_PORTA_io_[7..0]
exp_PORTA_DIR_o
exp_PORTA_nOE_o
exp_PORTB_o_[7..0]
exp_PORTC_io_[11..0]
exp_PORTD_io_[11..0]
exp_PORTEFG_io_[11..0]
exp_PORTE_nOE_o
exp_PORTF_nOE_o
exp_PORTG_nOE_o
exp_PORTA[7..0]
exp_PORTA_DIR
exp_PORTA_nOE
exp_PORTB[7..0]
exp_PORTC[11..0]
exp_PORTD[11..0]
exp_PORTEFG[11..0]
exp_PORTE_nOE
exp_PORTF_nOE
exp_PORTG_nOE
HDMI_D2_o(n)
HDMI_D2_o
HDMI_D1_o(n)
HDMI_D1_o
HDMI_D0_o(n)
HDMI_D0_o
HDMI_CK_o(n)
HDMI_CK_o
HDMI_SCL_o
HDMI_SDA_io
HDMI_HPD_i
HDMI_D2N
HDMI_D2P
HDMI_D1N
HDMI_D1P
HDMI_D0N
HDMI_D0P
HDMI_CKN
HDMI_CKP
HDMI_SCL
HDMI_SDA
HDMI_HPD
SND_L_o
SND_R_o
SND_L
SND_R
fixed: clk/sysd0, jtag, u22 footprint
Dossytronics
Sheet: /fpga_top/
File: fpga_top.sch
Title: Mk.3 Blitter FPGA development board
Size: A4
Date: 2021-08-14
Rev: 3.03
KiCad E.D.A. kicad (5.1.6)-1
Id: 11/11