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File: CPUSKT\_6x09.sch

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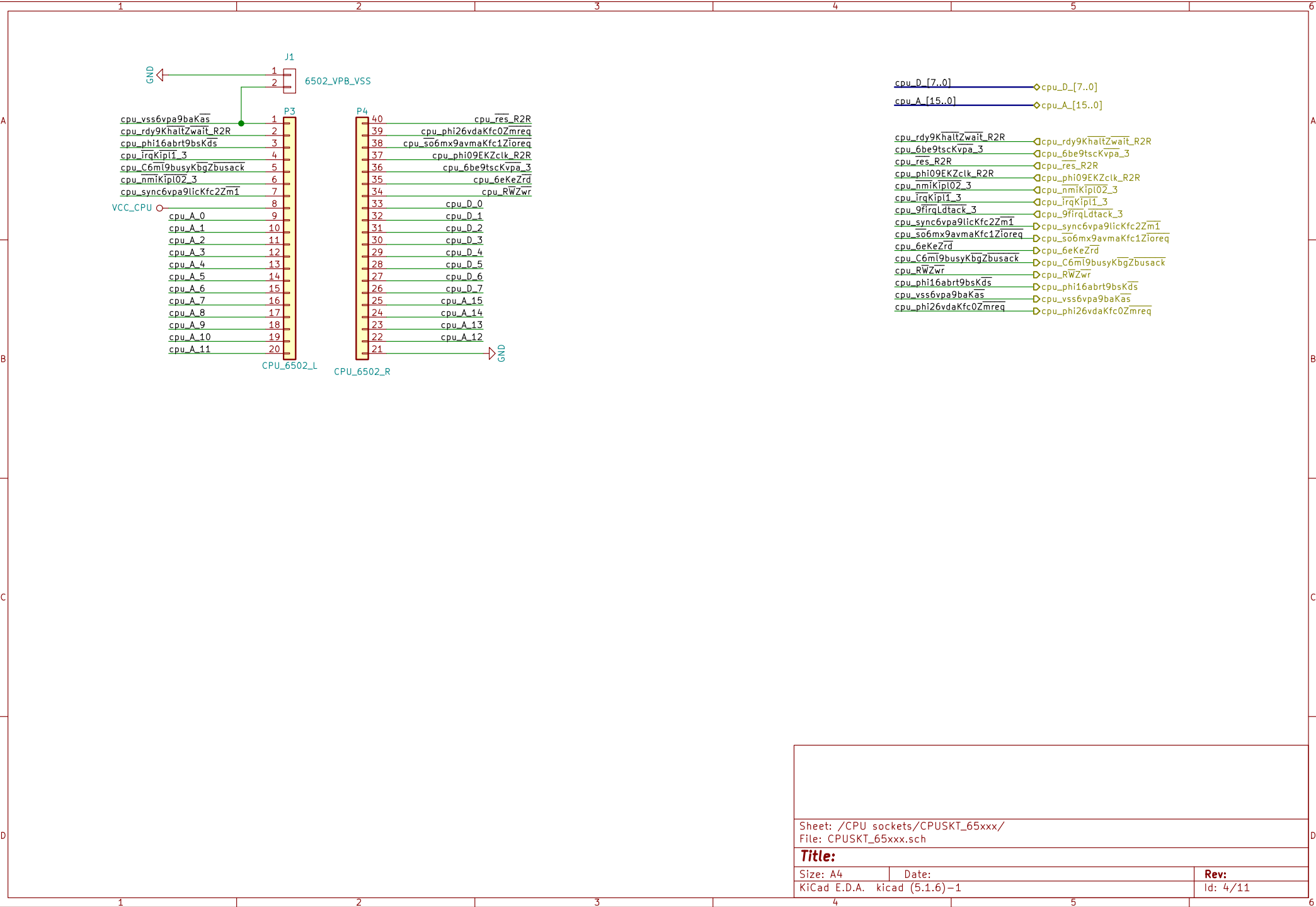
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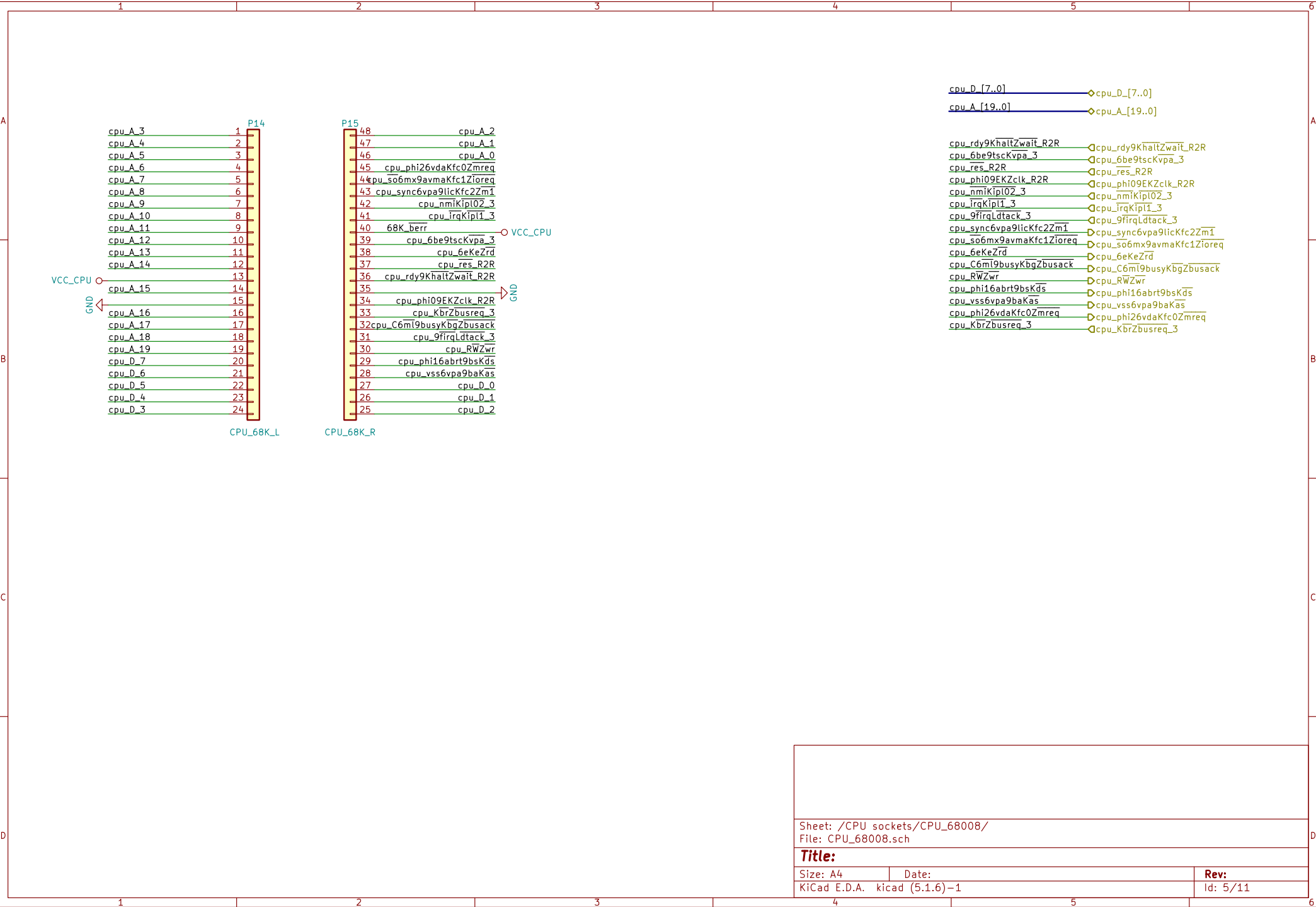
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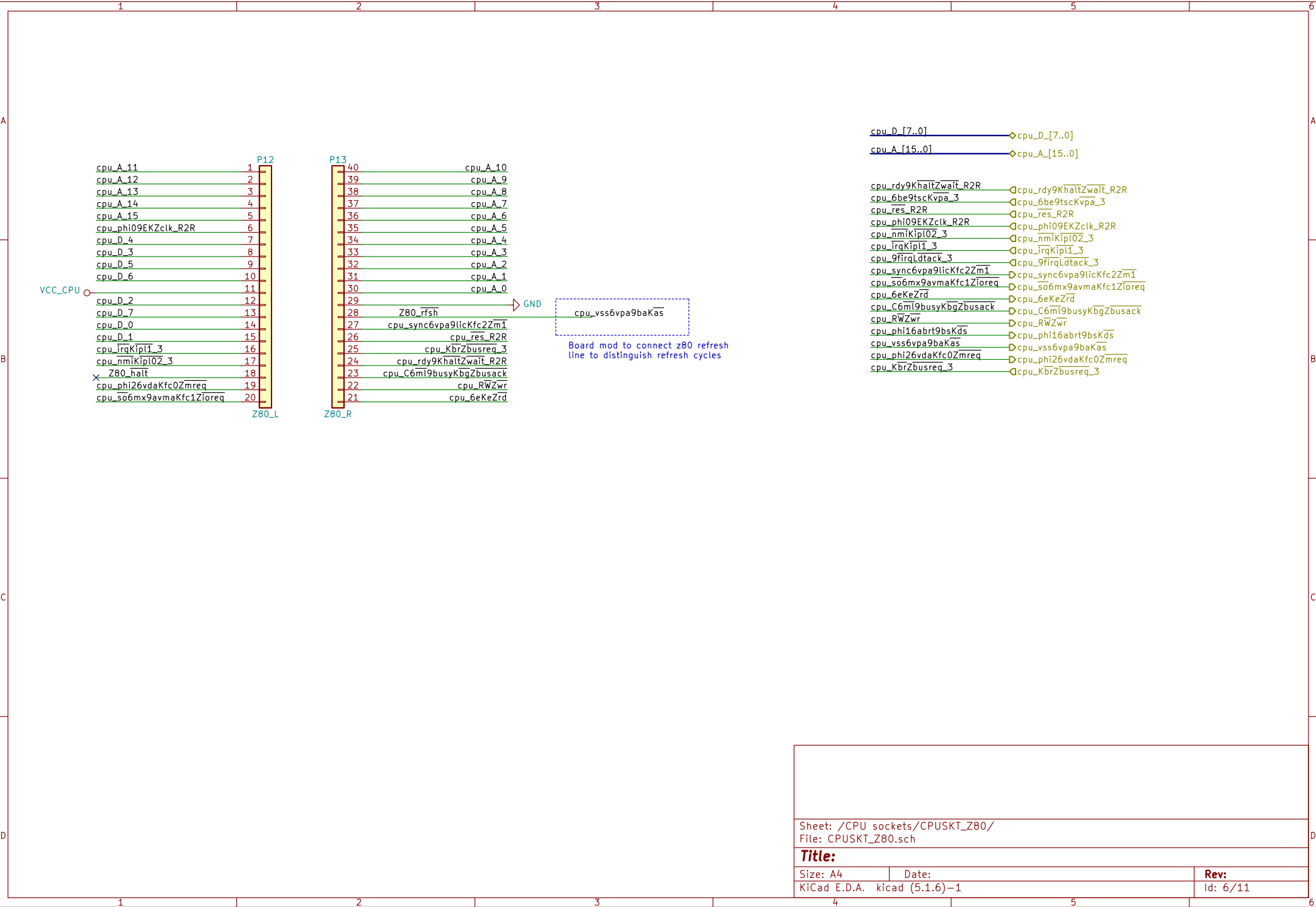
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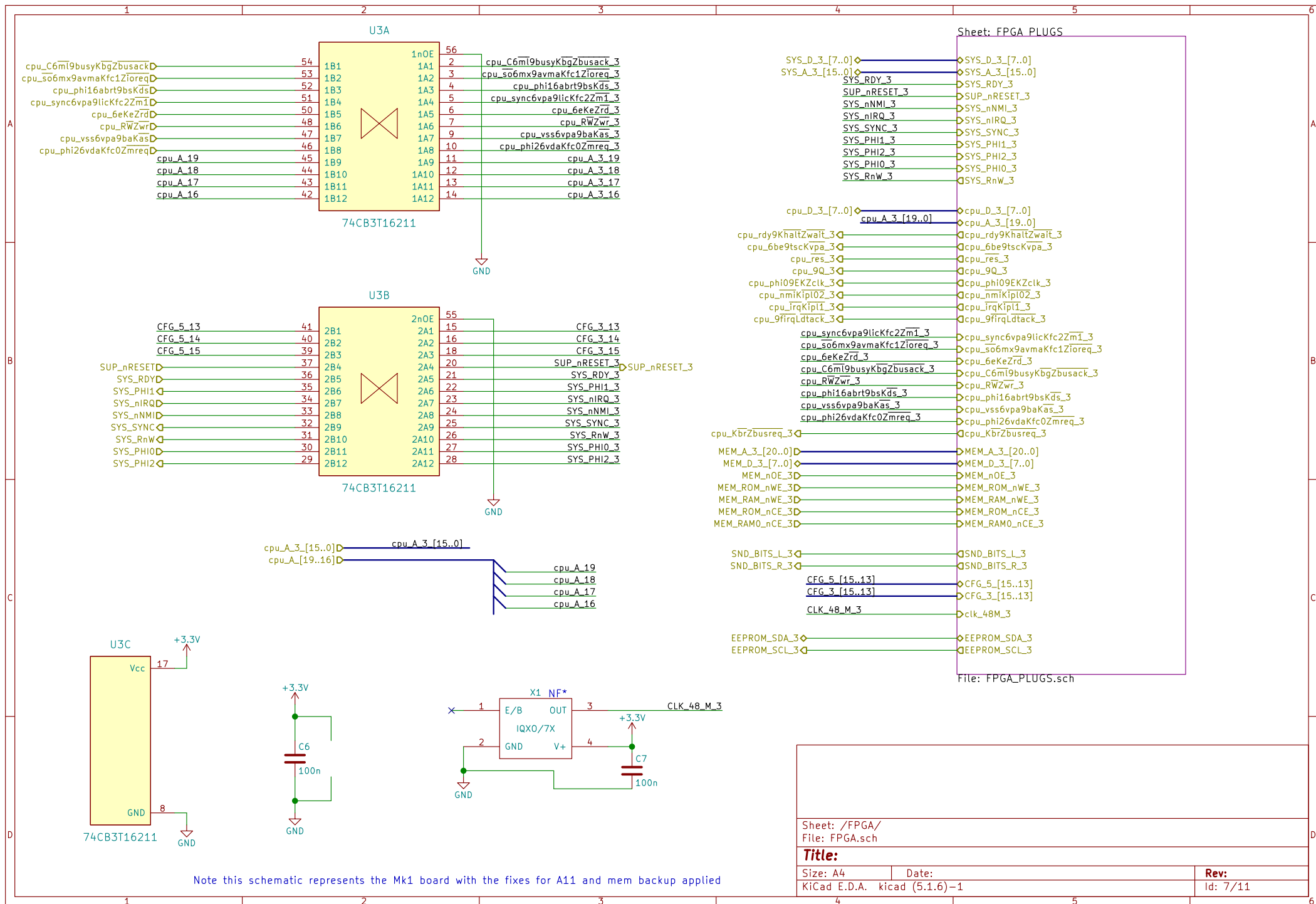
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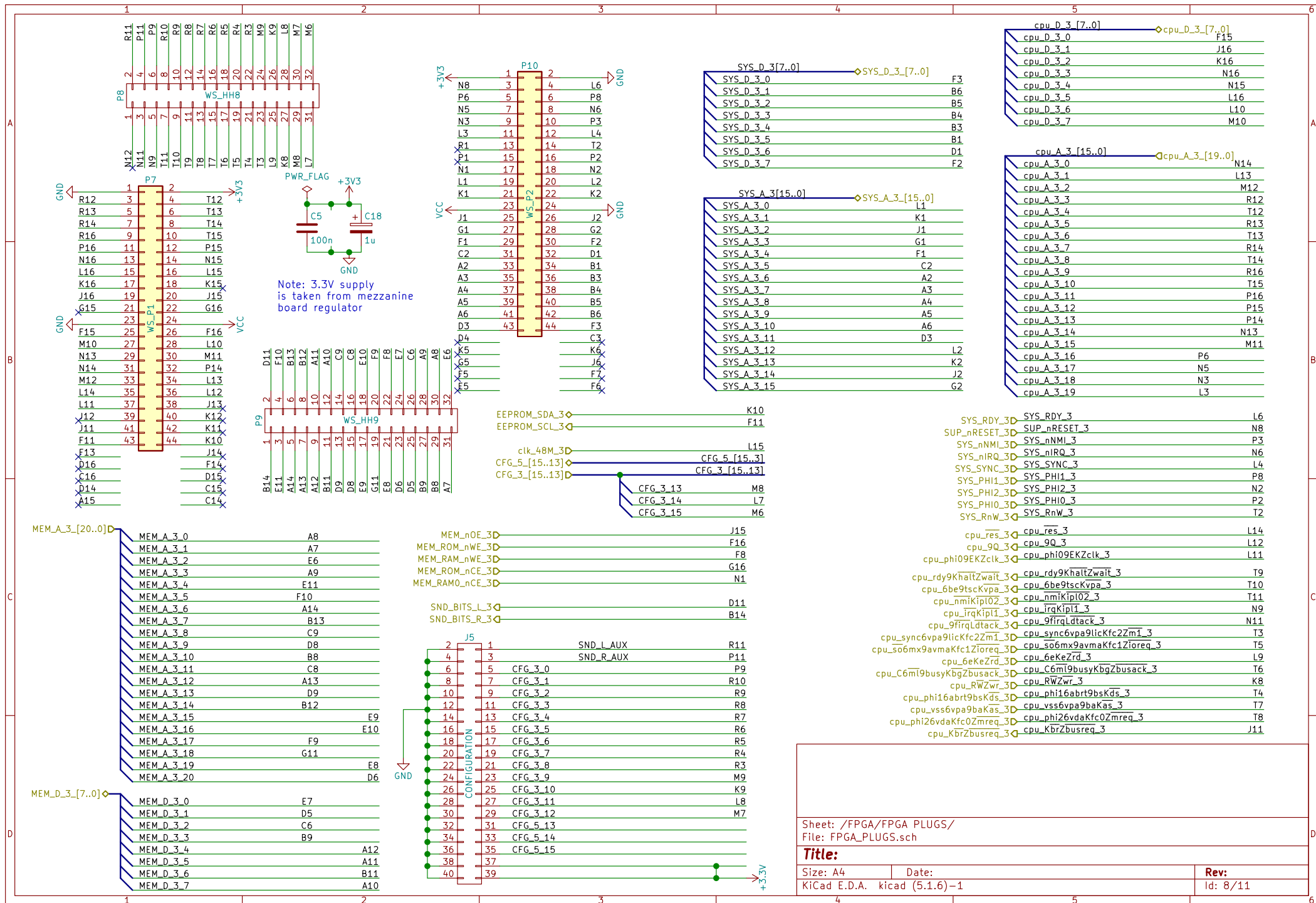
Id: 3/11











Sheet: /FPGA/FPGA PLUGS/  
File: FPGA\_PLUGS.sch

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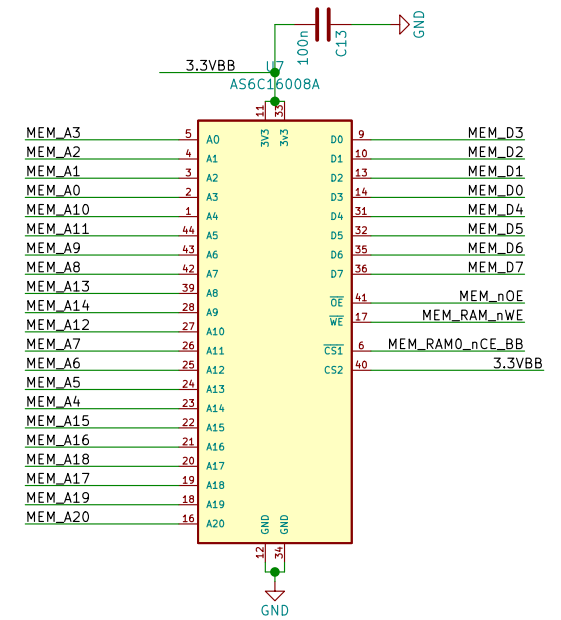
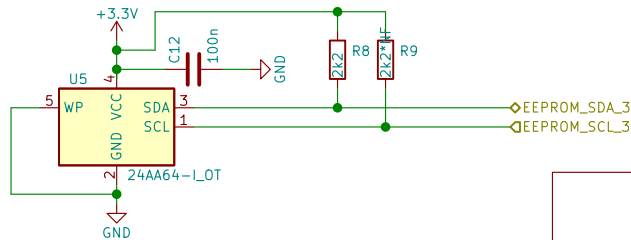
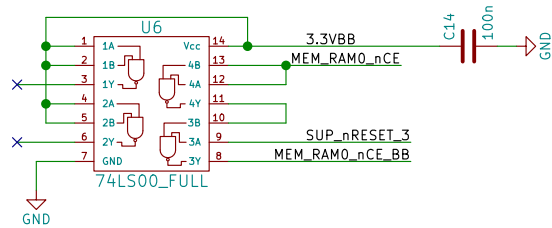
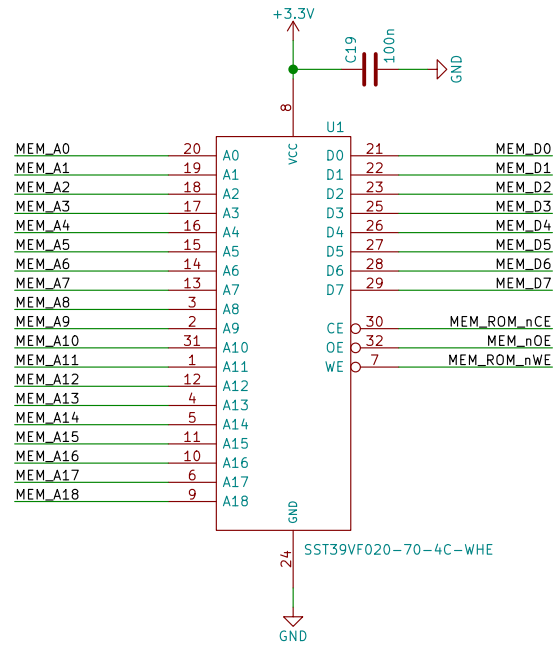
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MEM\_A\_3\_[20..0] > MEM\_A[20..0]  
 MEM\_D\_3\_[7..0] > MEM\_D[7..0]  
 MEM\_nOE\_3 > MEM\_nOE  
 MEM\_ROM\_nWE\_3 > MEM\_ROM\_nWE  
 MEM\_RAM\_nWE\_3 > MEM\_RAM\_nWE  
 MEM\_ROM\_nCE\_3 > MEM\_ROM\_nCE  
 MEM\_RAM0\_nCE\_3 > MEM\_RAM0\_nCE

3.3V\_BB > 3.3VBB  
 SUP\_nRESET\_3 > SUP\_nRESET\_3

Sheet: /memory/  
 File: memory.sch

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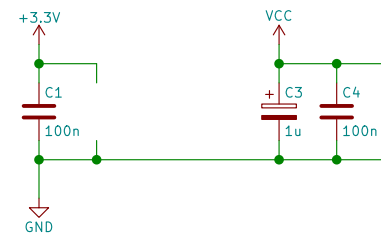
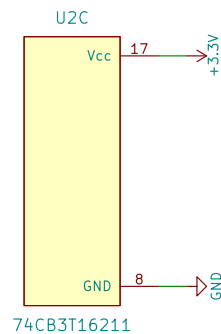
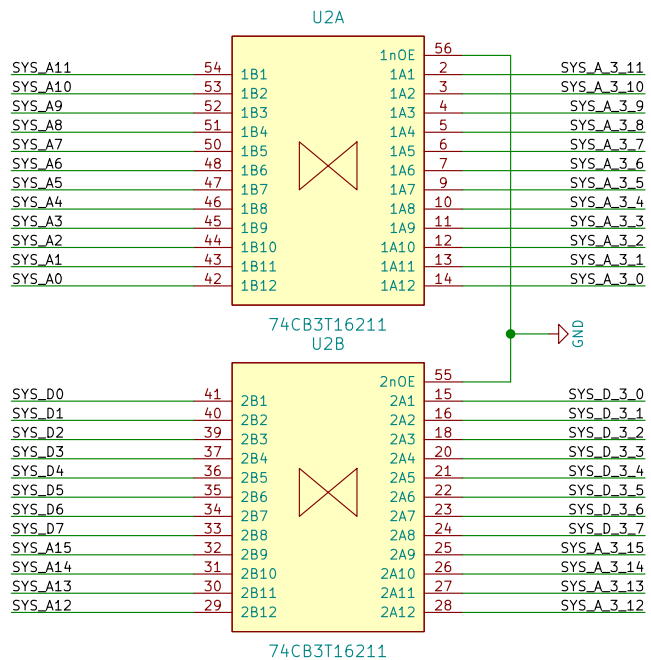
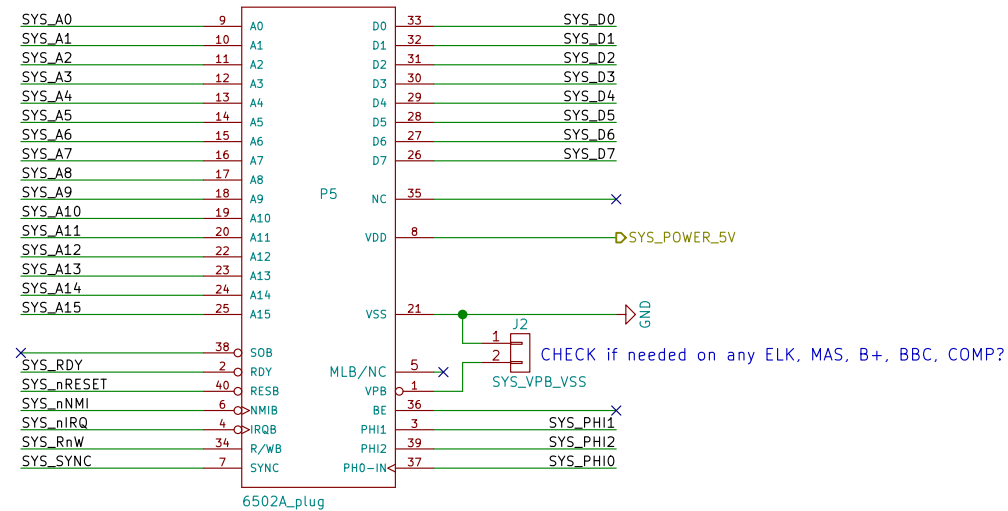
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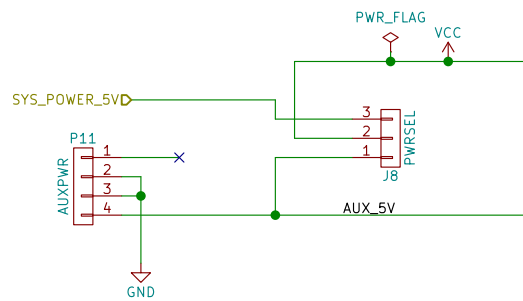
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SYS\_D\_3 [7..0] ◆ SYS\_D\_3 [7..0]  
SYS\_A\_3 [15..0] ◆ SYS\_A\_3 [15..0]

<u>SYS_RDY</u>	▷SYS_RDY
<u>SYS_nRESET</u>	▷SYS_nRESET
<u>SYS_nNMI</u>	▷SYS_nNMI
<u>SYS_nIRQ</u>	▷SYS_nIRQ
<u>SYS_SYNC</u>	▷SYS_SYNC
<u>SYS_PHI1</u>	▷SYS_PHI1
<u>SYS_PHI2</u>	▷SYS_PHI2
<u>SYS_PHI0</u>	▷SYS_PHI0
<u>SYS_RnW</u>	▷SYS_RnW



Size: A4	Date:
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