

# 3

## ML with GPUs

# Topics



Introduction to  
GPUs



CUDA



GPU  
Ecosystem



GPU-based  
ML libraries:  
cuDF, cuML,  
and cuPY



Summary

# The Importance of GPU in ML Computations

- GPU

- A Graphics Processing Unit (GPU) is a specialized circuit engineered for fast processing and image generation for screen display

- History of GPU Evolution

- Primarily crafted for graphic rendering in gaming
- Evolved into powerhouses for parallel processing
- Integral for complex, computation-heavy tasks in machine learning and scientific domains.

- GPU's Transition to General-Purpose Computing

- Transitioned beyond graphics to multifaceted computing applications
- Birth of GPGPU, diversifying GPUs' roles to encompass extensive computational functions.

# The Role of GPU in Modern ML

## GPUs in ML: From Graphics to Machine Learning Powerhouses

- GPUs have transitioned from graphic rendering to key roles in machine learning (ML) and artificial intelligence (AI) innovation.
- Their robust computing capabilities address the demands of intricate ML algorithms, particularly in deep learning.

## Boosting Deep Learning Performance

- The extensive computation required for training and running deep neural networks in deep learning is efficiently managed by GPUs.
- By parallelizing data processing, GPUs have significantly shortened the time to train intricate models.

## Enabling More Complex and Efficient Models

- GPUs have unlocked the potential for larger and more complex models, transforming what's possible in ML.
- This advancement has propelled significant innovations in sectors such as natural language processing, computer vision, and predictive analytics.

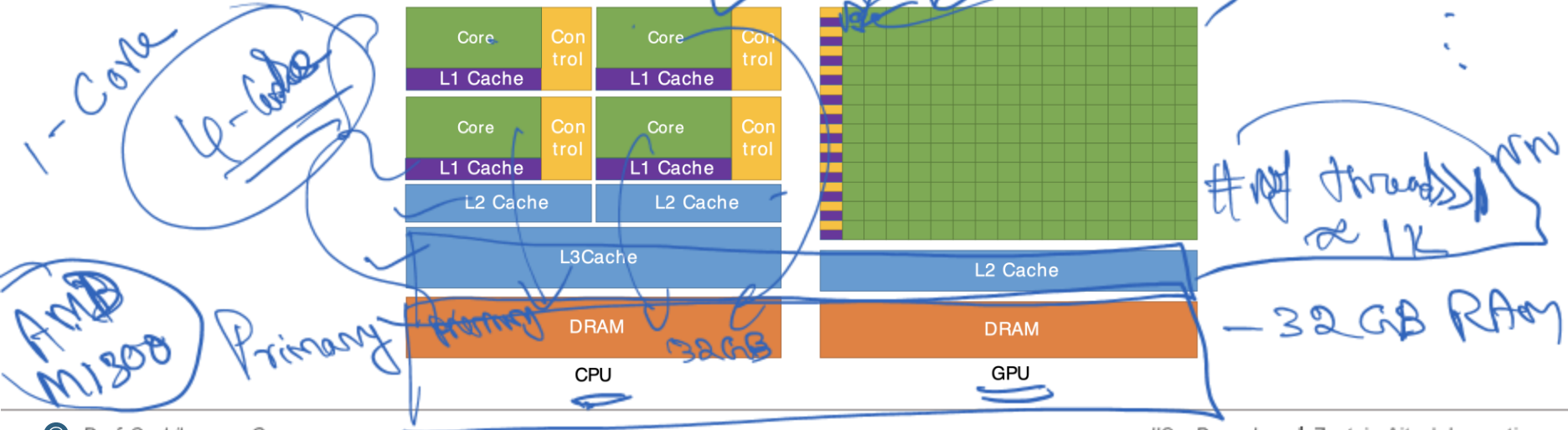
# GPU vs. Traditional Computing

Features	GPU	CPU
<b>Architecture Comparison</b>	Designed for parallel processing, GPUs consist of hundreds of cores capable of handling thousands of threads simultaneously	Optimized for sequential processing, CPUs have fewer cores designed for a wide range of tasks, focusing on single-thread performance.
<b>Processing Capabilities</b>	Excelling in tasks that can be parallelized, making them ideal for matrix operations and data-heavy computations common in ML	Best suited for tasks that require sequential processing and complex decision-making.
<b>Application in ML</b>	Revolutionized the field of deep learning by significantly speeding up the training of large neural networks. Ideal for tasks like image and video processing, neural network training, and large-scale data analyses	More suitable for traditional ML algorithms that don't require intense parallel processing, like decision trees or smaller-scale data processing tasks

# CPU - GPU

- CPU is designed to excel at executing a sequence of operations (threads) as fast as possible (low latency)
- CPU can execute a few tens of these threads in parallel
- GPU is designed to excel at executing thousands of threads in parallel (amortizing the slower single-thread performance to achieve greater throughput)

- SMP - Shared Memory  
- DMQ.





# Benefits of GPUs in Machine Learning

## Enhanced Parallel Processing

- GPUs excel in parallel processing, capable of handling thousands of tasks at once.
- Essential for machine learning, particularly deep learning, where concurrent operations are the norm.

## Speedier Data Handling

- Data processing tasks, like matrix operations crucial to ML, are expedited by GPUs.
- Results in rapid ML model training, facilitating more trials and optimizations in shorter timeframes.

## Large Dataset Management

- Optimized for large dataset manipulation, pivotal in big data and AI initiatives.
- Superior bandwidth and memory features enable faster data handling, beneficial for extensive ML operations.

## Superior Energy Efficiency

- For tasks that can be parallelized, GPUs offer better energy efficiency than CPUs.
- Their power-conscious performance is preferable for sustained, intensive ML.

- **CUDA (Compute Unified Device Architecture)**

- general-purpose parallel computing platform and programming model for NVIDIA GPUs
- allows developers to ~~use~~ C++ as a high-level programming language

- **OpenCL**

- general heterogeneous computing framework
- <https://www.khronos.org/opencl/>

- **OpenACC**

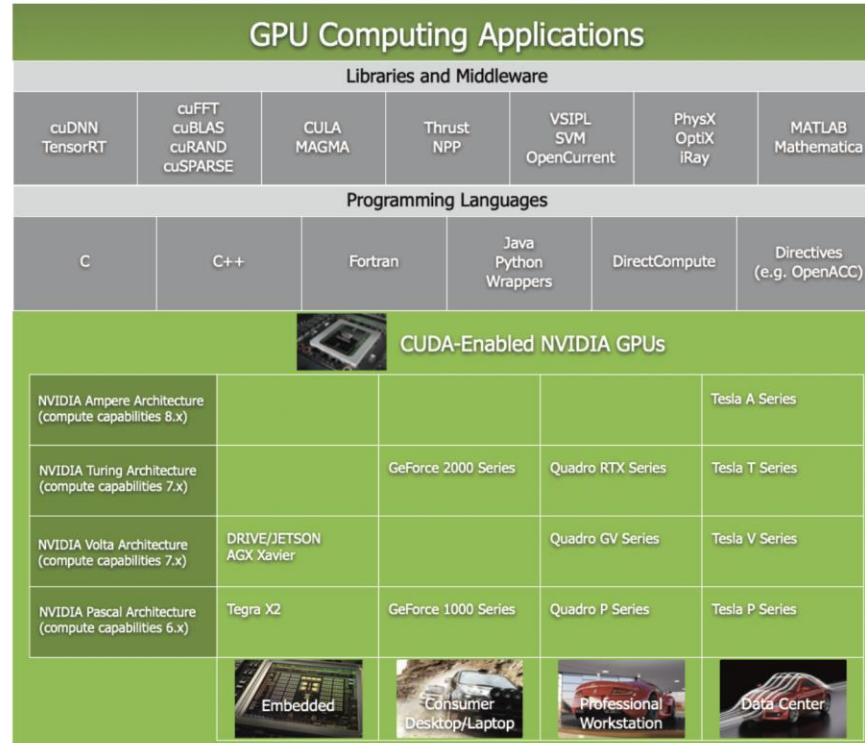
- user-driven directive-based performance-portable parallel programming model
- supports C, C++, Fortran programming language

Note: For python usage: Check [Theano](#), [pyCUDA](#)



# CUDA

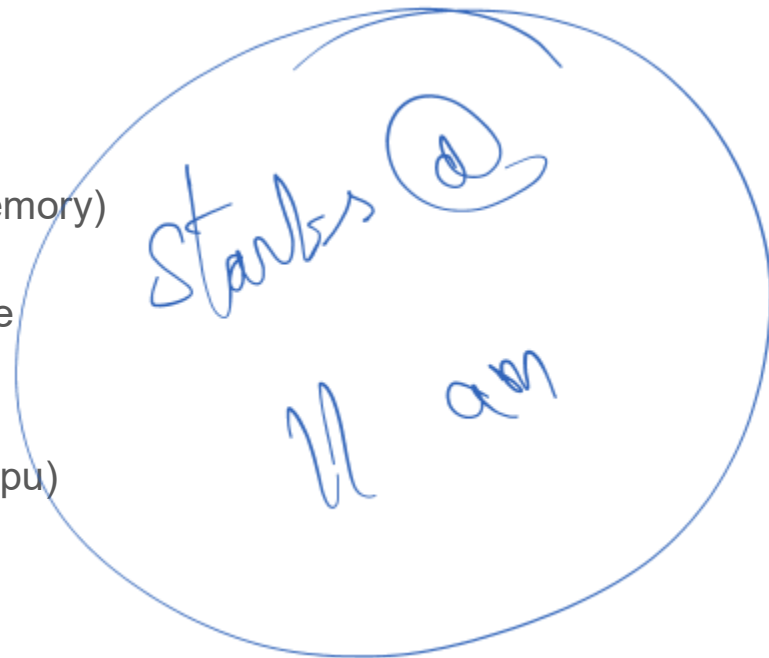
A general-purpose  
parallel computing  
platform and  
programming  
model for NVIDIA  
GPUs



# Scalable Programming Model

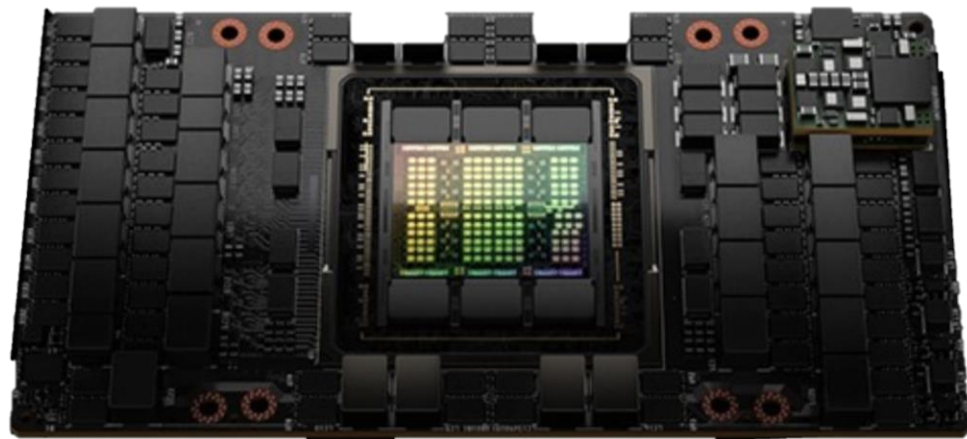
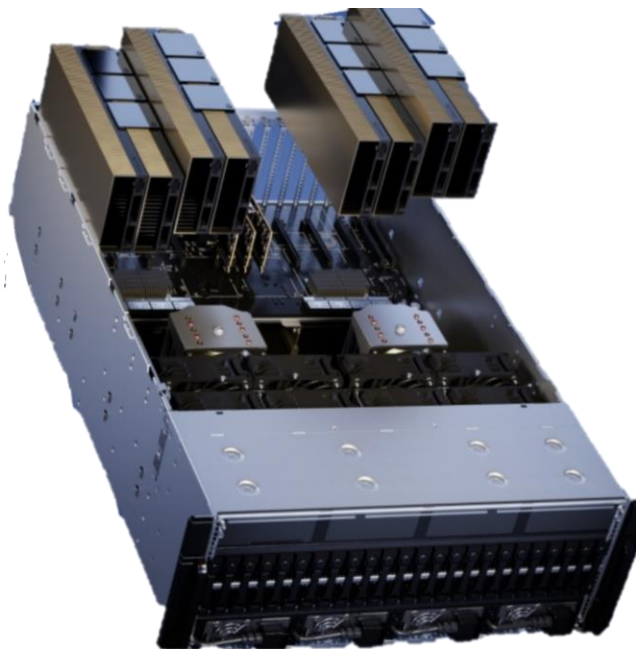
## ⑩ GPU computing: steps involved

- ⑩ Setup inputs on the host (CPU-accessible memory)
- ⑩ Allocate memory for outputs on the host CPU
- ⑩ Allocate memory for inputs on the GPU device
- ⑩ Allocate memory for outputs on the GPU
- ⑩ Copy inputs from host to GPU (slow)
- ⑩ Start GPU kernel (function that executes on gpu)
- ⑩ Copy output from GPU to host (slow)



Note: Unified Memory Architecture in CUDA is a feature that simplifies memory management between the CPU (host) and GPU (device). It provides a single memory space accessible by both the host and the device, allowing them to share data without the need to explicitly transfer it between the host and the device memory.

# GPU: Thread Hierarchy



NVIDIA H100 Tensor Core GPU

<https://www.nvidia.com/en-in/data-center/h100/>

# GPU: Thread Hierarchy

## NVIDIA RTX A6000: Ampere GPU Architecture In-Depth

⑩ 7 GPCs, each with

~~⑩~~ 6 TPCs, each with 2 SMs

⑩ In Total

⑩ 42 TPCs & 84 SMs

⑩ Each SM with

⑩ 128 CUDA (FP32) cores/SM (10752 in total)

⑩ Performs FP32, FP16, INT8, and INT4 precision operations

⑩ 168 FP64, TFLOP rate is 1/64th the TFLOP rate of FP32

⑩ 4 Tensor cores/SM (336 in total, 3<sup>rd</sup> Gen)

⑩ 336 Texture units (Graphics)

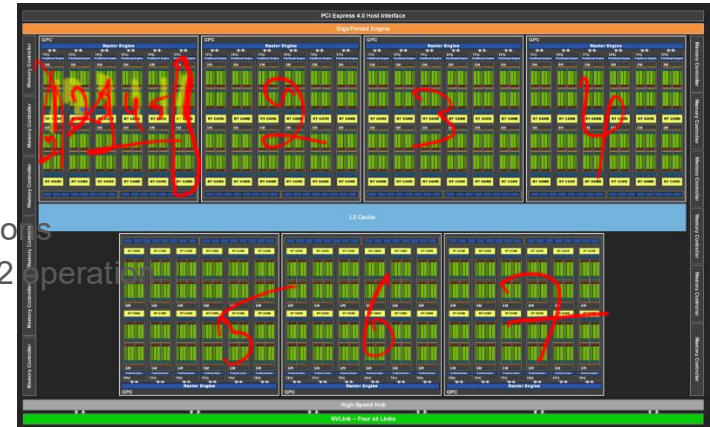
⑩ 84 RT cores (Graphics)

⑩ 38.7 TFLOPs (non-tensor) Peak (FP32, FP16, BF16)

⑩ FP32: 77.4/154.8 TOPS/TFLOPS Tensor TFLOPS Peak

⑩ INT8: 309.7/619.4 TOPS/TFLOPS Tensor TOPS Peak

⑩ INT4: 619.4/1238.6 TOPS/TFLOPS Tensor TOPS Peak

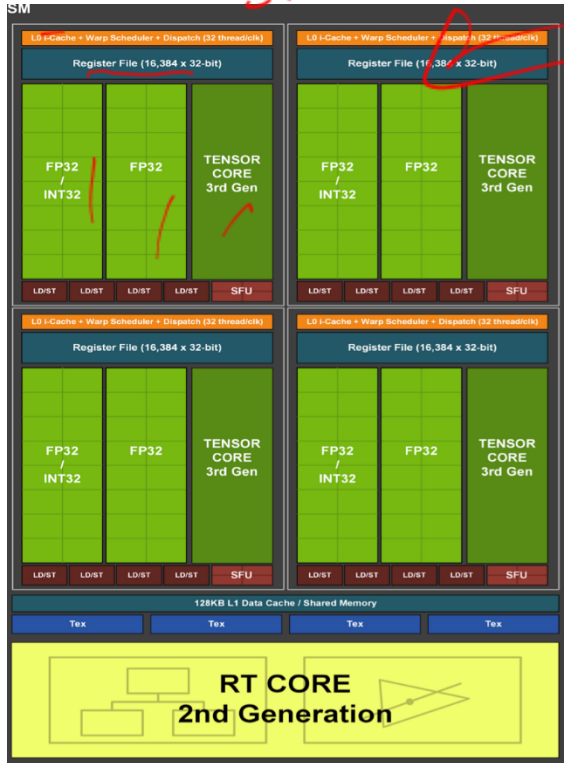


GPC - Graphics Processing Clusters, TPCs - Texture Processing Clusters, SM - Streaming Multiprocessors, Raster Operators (ROPS), and memory controllers

# GPU: Thread Hierarchy

## NVIDIA RTX A6000: Ampere GPU Architecture In-Depth

SM



<https://www.nvidia.com/content/PDF/nvidia-ampere-ga-102-gpu-architecture-whitepaper-v2.pdf>

# GPU: Thread Hierarchy

## NVIDIA RTX A6000: Ampere GPU Architecture In-Depth

### ⑩ CUDA Cores

- ⑩ 128 CUDA cores/SM (10752 in total)
- ⑩ Mixed-precision tensor operations: The cores support efficient tensor operations for AI/ML workloads, including FP32, FP16, INT8, and INT4 precisions.

GPC - Graphics Processing Clusters, TPCs - Texture Processing Clusters, SM - Streaming Multiprocessors, Raster Operators (ROPS), and memory controllers

# Questions

1. GPUs can be classified as shared memory machines. (T/F) T
2. GPU is designed to excel at executing thousands of threads in parallel to achieve low latency (as fast as possible). (T/F) F

CQ-2

# GPU: Hello World

```
void c_hello(){  
    printf("Hello World!\n");  
}  
  
int main() {  
    c_hello();  
    return 0;  
}
```

*Handwritten annotations:*

- in:* (with arrow pointing to the `main` function)
- main func.* (with arrow pointing to the `main` function)
- CPU code* (with arrow pointing to the entire code block)

```
__global__ void cuda_hello(){  
    printf("Hello World from GPU!\n");  
}  
  
int main() {  
    cuda_hello<<<1,1>>>();  
    return 0;  
}
```

*Handwritten annotations:*

- CUDA kernel* (with arrow pointing to the `__global__ void cuda_hello()` function)
- GPU* (with arrow pointing to the `cuda_hello` function)
- CPU code* (with arrow pointing to the `main` function)

`$> nvcc hello.cu -o hello`

<https://cuda-tutorial.readthedocs.io/en/latest/tutorials/tutorial01/>



# GPU: Hello World

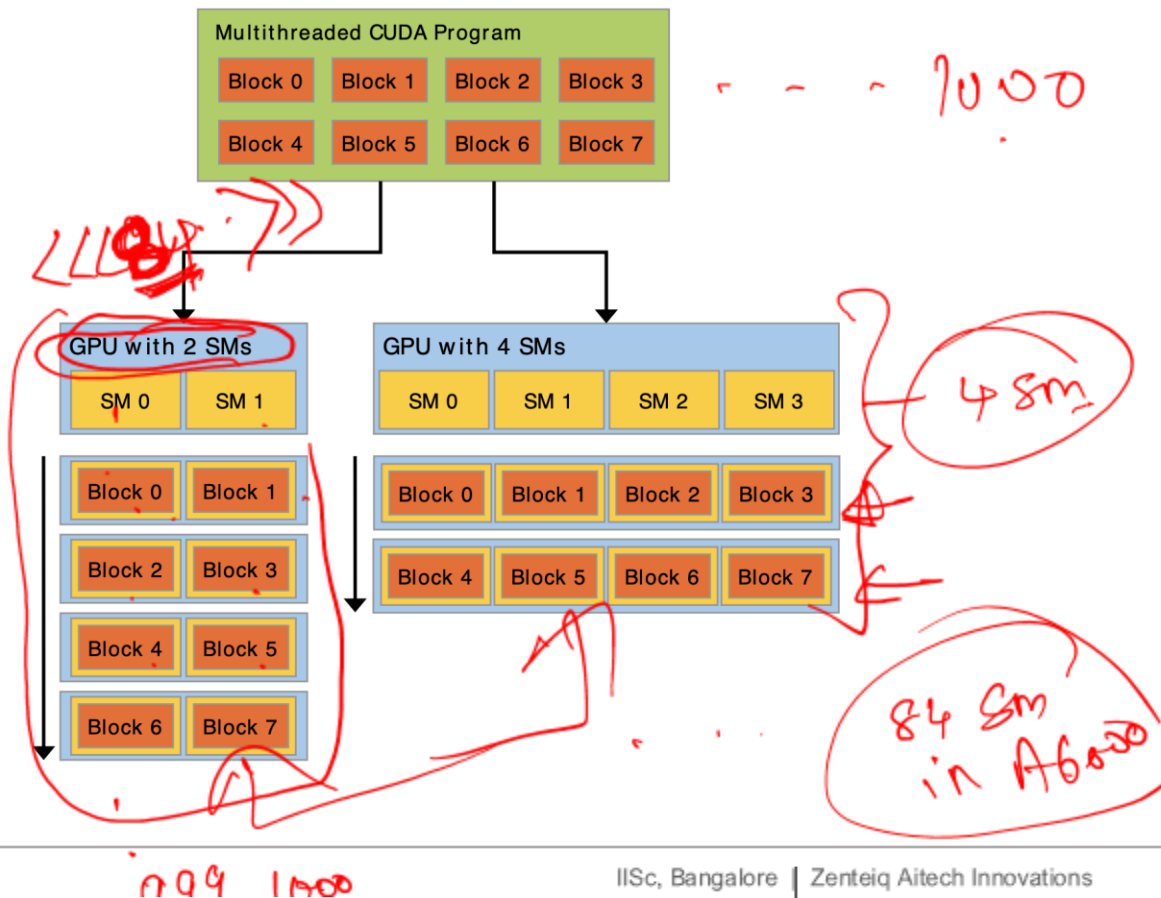
```
__global__ void cuda_hello() {  
    printf("Hello World from GPU!\n");  
}  
  
int main() {  
    cuda_hello<<<1,1>>>();  
    return 0;  
}
```

*Cuda kernel.*

- \_\_global\_\_ specifier indicates a function that runs on device (GPU)
- the CUDA kernel cuda\_hello() can be called from host *[CPU]*
- kernel execution configuration is provided through <<<...>>> syntax, called kernel launch
- the number of GPU threads "M" to be launched in each thread block is indicated through kernel launch: <<<B,M>>>, where "B" is the number of thread blocks

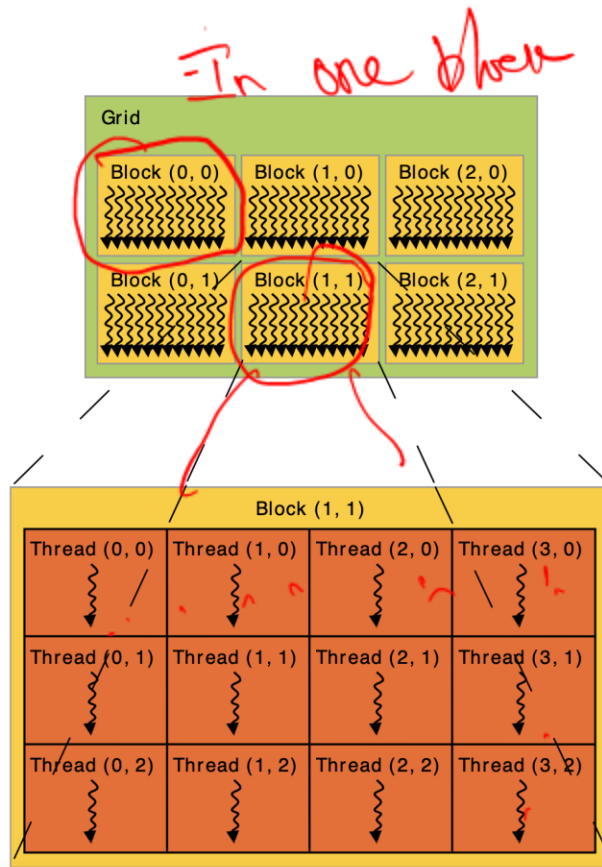
# GPU Computing

- Thread - distributed by the CUDA runtime (threadIdx)
- Block - user defined group of 1 to  $\sim T$  threads (blockIdx)
- Grid - a group of one or more blocks. A grid is created for each CUDA kernel function call.



# GPU Computing

- Thread - distributed by the CUDA runtime (threadIdx)
- Block - user defined group of 1 to ~512 threads (blockIdx)
- Grid - a group of one or more blocks. A grid is created for each CUDA kernel function call.

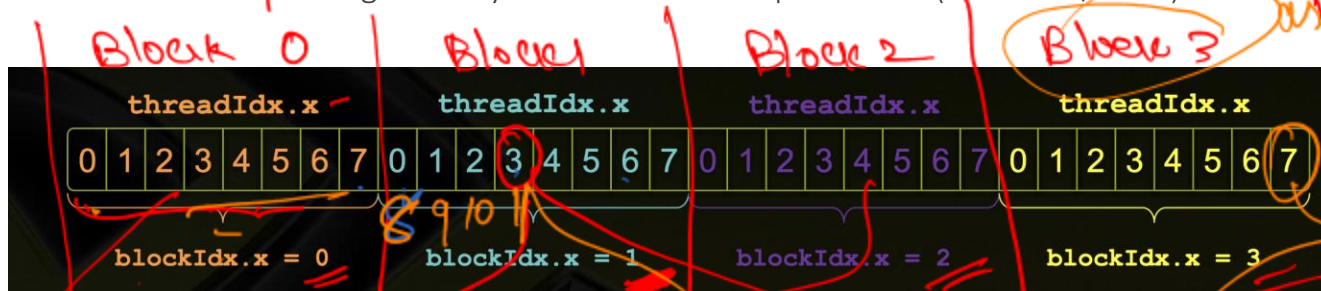


*SM*

# GPU Computing

## Indexing Arrays with Blocks and Threads

- consider indexing an array with one element per thread (8 threads/block)



- with M threads per block, a unique index for each thread is given by:

- $\text{index} = M * \text{blockIdx.x} + \text{threadIdx.x}$

- use the built-in variable `blockDim.x` for threads per block (M)

$= i$  [Global index]

for (i = 1 to 32)

$c[i] = a[i] + b[i]$

each "i" will be

assigned to

a unique

thread

$\begin{pmatrix} 31 \\ 3 \end{pmatrix}$

$c[31] = a[31] + b[31]$

$i = \text{index} = 8 * 4 + 3$

$c[i] = a[i] + b[i] = 11$

# GPU Computing

## Indexing Arrays with Blocks and Threads

- `blockIdx.x`, `blockIdx.y`, `blockIdx.z` built-in variables return the block ID in the x-axis, y-axis, and z-axis of the block
- `threadIdx.x`, `threadIdx.y`, `threadIdx.z` built-in variables return the thread ID in the x-axis, y-axis, and z-axis of the thread in a particular block
- `blockDim.x`, `blockDim.y`, `blockDim.z` built-in variables return the “block dimension” (number of threads in a block in the x-axis, y-axis, and z-axis)

# GPU Computing: Vector addition

```
#define N 1618
#define T 1024
```

```
// Device code
__global__ void VecAdd(int* A, int* B, int* C, int N)
{
    int i = blockDim.x * blockIdx.x + threadIdx.x;
    if (i < N)
        C[i] = A[i] + B[i];
}
```

```
// main code
int main() {
    int a[N], b[N], c[N];
    int *dev_a, *dev_b, *dev_c;
    // initialize a and b with int values
```

```
    size = N * sizeof(int);
    cudaMalloc((void**)&dev_a, size);
    cudaMalloc((void**)&dev_b, size);
    cudaMalloc((void**)&dev_c, size);
```

```
    cudaMemcpy(dev_a, a, size, cudaMemcpyHostToDevice);
    cudaMemcpy(dev_b, b, size, cudaMemcpyHostToDevice);
```

```
    vecAdd<<< (int)ceil(N/T), T >>>>(dev_a, dev_b, dev_c);
```

```
    cudaMemcpy(c, dev_c, size, cudaMemcpyDeviceToHost);
```

```
    cudaFree(dev_a); cudaFree(dev_b); cudaFree(dev_c);
```

```
    exit(0); }
```

$$1024 \times 1 + \frac{1618}{1024}$$

$$\text{Ceil}\left(\frac{N}{T}\right) = \frac{1618}{1024} \approx 2$$

Global index  
# threads: 2048  
A[1618]

range of i: [0 - 2047]

kernel launch  
[1, 2, 1024]

GPU additional overhead

# GPU Computing: Matrix Multiplication

```
void matrixMult (int a[N][N], int b[N][N], int c[N][N], int width)
{
    for (int i = 0; i < width; i++)
        for (int j = 0; j < width; j++) {
            int sum = 0;
            for (int k = 0; k < width; k++) {
                int m = a[i][k];
                int n = b[k][j];
                sum += m * n;
            }
            c[i][j] = sum;
        }
}
```

Can it be parallelized?

# GPU Computing: Matrix Multiplication

```
void matrixMult (int a[N][N], int b[N][N], int c[N][N], int width)
{
    for (int i = 0; i < width; i++)
        for (int j = 0; j < width; j++) {
            int sum = 0;
            for (int k = 0; k < width; k++) {
                int m = a[i][k];
                int n = b[k][j];
                sum += m * n;
            }
            c[i][j] = sum;
        }
}
```

*Cu Block*

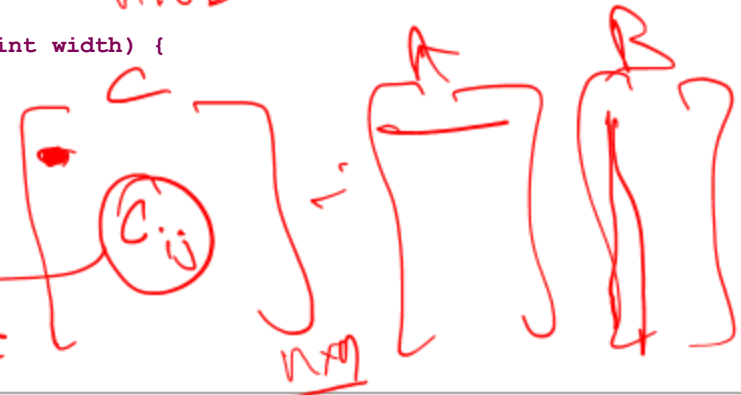
```
// Device code
__global__ void matrixMult (int *a, int *b, int *c, int width) {
    int k, sum = 0;
    int col = threadIdx.x + blockDim.x * blockIdx.x;
    int row = threadIdx.y + blockDim.y * blockIdx.y;
    if (col < width && row < width) {
        for (k = 0; k < width; k++)
            sum += a[row * width + k] * b[k * width + col];
        c[row * width + col] = sum;
    }
}
```

$n^2$  - dot Product

launch  $n^2$  threads  
each thread  
performs one  
dot product

$c[i, j]$   
↑ ↑  
Global index

each  $c_{ij}$  is mapped to  
a thread.





# Asynchronous Concurrent Execution

CUDA exposes the following operations as independent tasks that can operate concurrently with one another:

- \* Computation on the host;
- \* Computation on the device;
- \* Memory transfers from the host to the device;
- \* Memory transfers from the device to the host;
- \* Memory transfers within the memory of a given device;
- \* Memory transfers among devices.

More Details: <https://docs.nvidia.com/cuda/cuda-c-programming-guide/>



EX: Write CUDA parallel code for

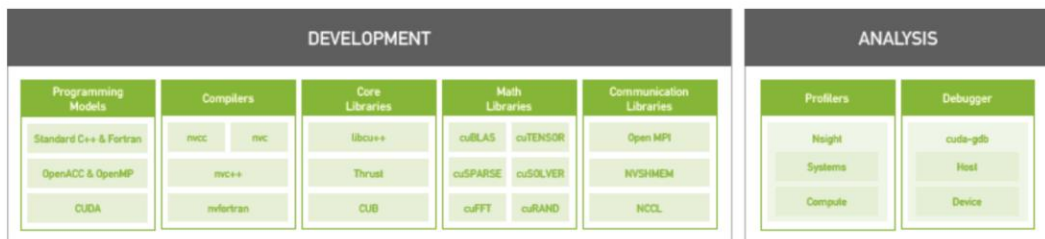
1. Matrix addition
2. Matrix vector multiplication
3. Matrix multiplication

# GPU Computing

## NVIDIA HPC SDK

### A Comprehensive Suite of Compilers, Libraries and Tools for HPC

The NVIDIA HPC Software Development Kit (SDK) includes the proven compilers, libraries and software tools essential to maximizing developer productivity and the performance and portability of HPC applications.



The NVIDIA HPC SDK C, C++, and Fortran compilers support GPU acceleration of HPC modeling and simulation applications with standard C++ and Fortran, OpenACC® directives, and CUDA®. GPU-accelerated math libraries maximize performance on common HPC algorithms, and optimized communications libraries enable standards-based multi-GPU and scalable systems programming. Performance profiling and debugging tools simplify porting and optimization of HPC applications, and containerization tools enable easy deployment on-premises or in the cloud. With support for NVIDIA GPUs and Arm, OpenPOWER, or x86-64 CPUs running Linux, the HPC SDK provides the tools you need to build NVIDIA GPU-accelerated HPC applications.

<https://developer.nvidia.com/hpc-sdk>

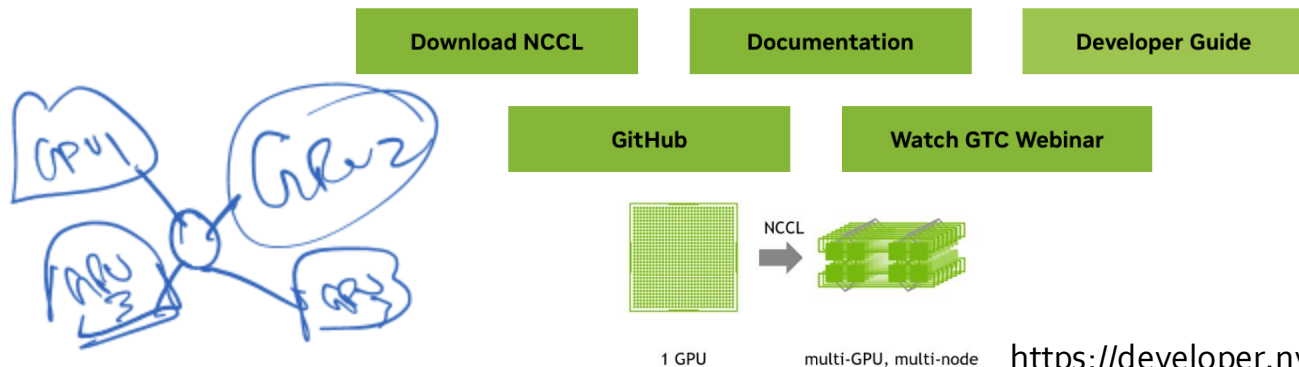
# GPU Computing for Deep Learning

The NVIDIA Collective Communication Library (NCCL) implements multi-GPU and multi-node communication primitives optimized for NVIDIA GPUs and Networking.

NCCL provides routines such as all-gather, all-reduce, broadcast, reduce, reduce-scatter as well as point-to-point send and receive that are optimized to achieve high bandwidth and low latency over PCIe and NVLink high-speed interconnects within a node and over NVIDIA Mellanox Network across nodes.

Leading deep learning frameworks such as Caffe2, Chainer, MxNet, PyTorch and TensorFlow have integrated NCCL to accelerate deep learning training on multi-GPU multi-node systems.

NCCL is available for download as part of the NVIDIA HPC SDK and as a separate package for Ubuntu and Red Hat.

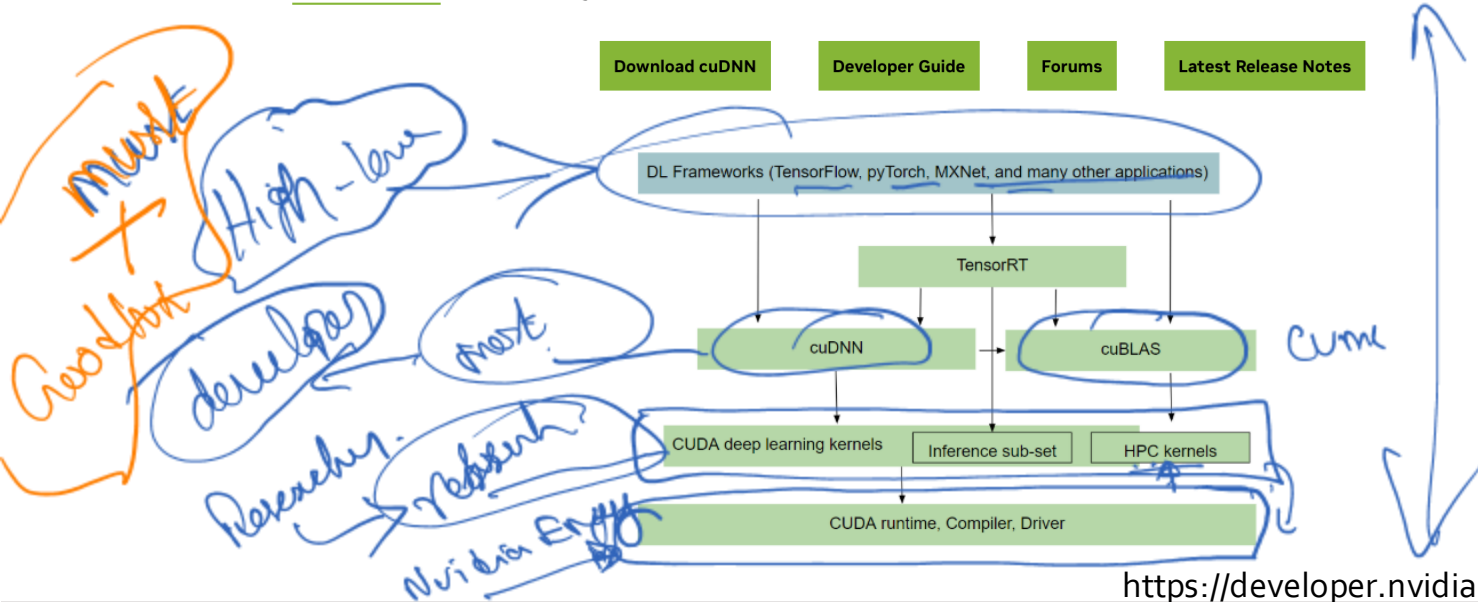


# GPU Computing (cuDNN) in Data Science

Good to know

The NVIDIA CUDA® Deep Neural Network library (cuDNN) is a GPU-accelerated library of primitives for deep neural networks. cuDNN provides highly tuned implementations for standard routines such as forward and backward convolution, pooling, normalization, and activation layers.

Deep learning researchers and framework developers worldwide rely on cuDNN for high-performance GPU acceleration. It allows them to focus on training neural networks and developing software applications rather than spending time on low-level GPU performance tuning. cuDNN accelerates widely used deep learning frameworks, including Caffe2, Chainer, Keras, MATLAB, MxNet, PaddlePaddle, PyTorch, and TensorFlow. For access to NVIDIA optimized deep learning framework containers that have cuDNN integrated into frameworks, visit NVIDIA GPU CLOUD to learn more and get started.



<https://developer.nvidia.com/cudnn>

# GPU Computing (cuDNN) in Data Science

AI / DEEP LEARNING   AUTONOMOUS MACHINES   AUTONOMOUS VEHICLES   DATA SCIENCE   GRAPHICS / SIMULATION   HPC   IVA/IOT   NETWORKING

## AI / Deep Learning



AI and Deep learning are used in the research community and in industry to help solve many big data problems such as computer vision, speech recognition, and natural language processing. The **NVIDIA Deep Learning SDK** provides high-performance tools and libraries to power innovative GPU-accelerated machine learning applications in the cloud, data centers, workstations, and embedded platforms.



### Accelerated Signal Processing with cuSignal

By Adam Thompson | March 5, 2021



### Building a Question and Answering Service Using Natural Language Processing with NVIDIA NGC and Google Cloud

By James Sohn and Chintan Patel | March 3, 2021

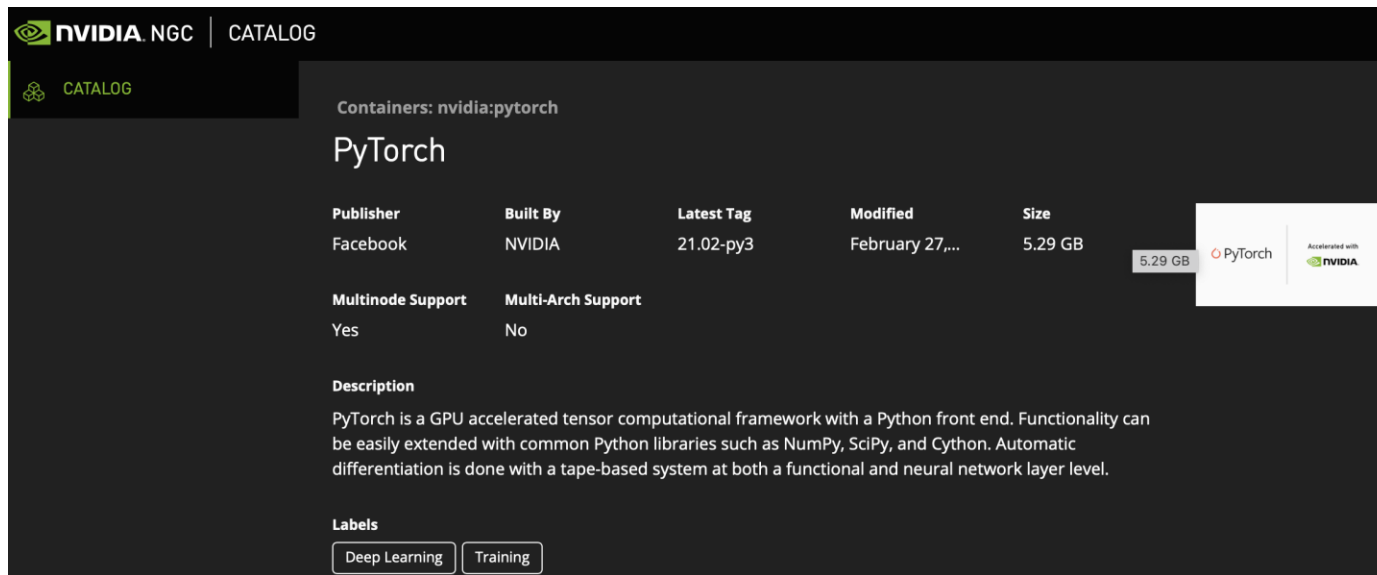


### Pandas DataFrame Tutorial – Beginner's Guide to GPU Accelerated DataFrames in Python

By Tom Drabas | March 3, 2021

Source: <https://developer.nvidia.com/blog/category/artificial-intelligence/>

# GPU Computing (cuDNN) in Data Science



The screenshot displays the NVIDIA NGC Catalog interface for the PyTorch container. The header shows the NVIDIA NGC logo and the word 'CATALOG'. Below the header, the container name 'Containers: nvidia:pytorch' is displayed. The main section is titled 'PyTorch'. A table lists the container's metadata:

Publisher	Built By	Latest Tag	Modified	Size
Facebook	NVIDIA	21.02-py3	February 27, ...	5.29 GB

Below the table, there are two rows of information:

<b>Multinode Support</b>	<b>Multi-Arch Support</b>
Yes	No

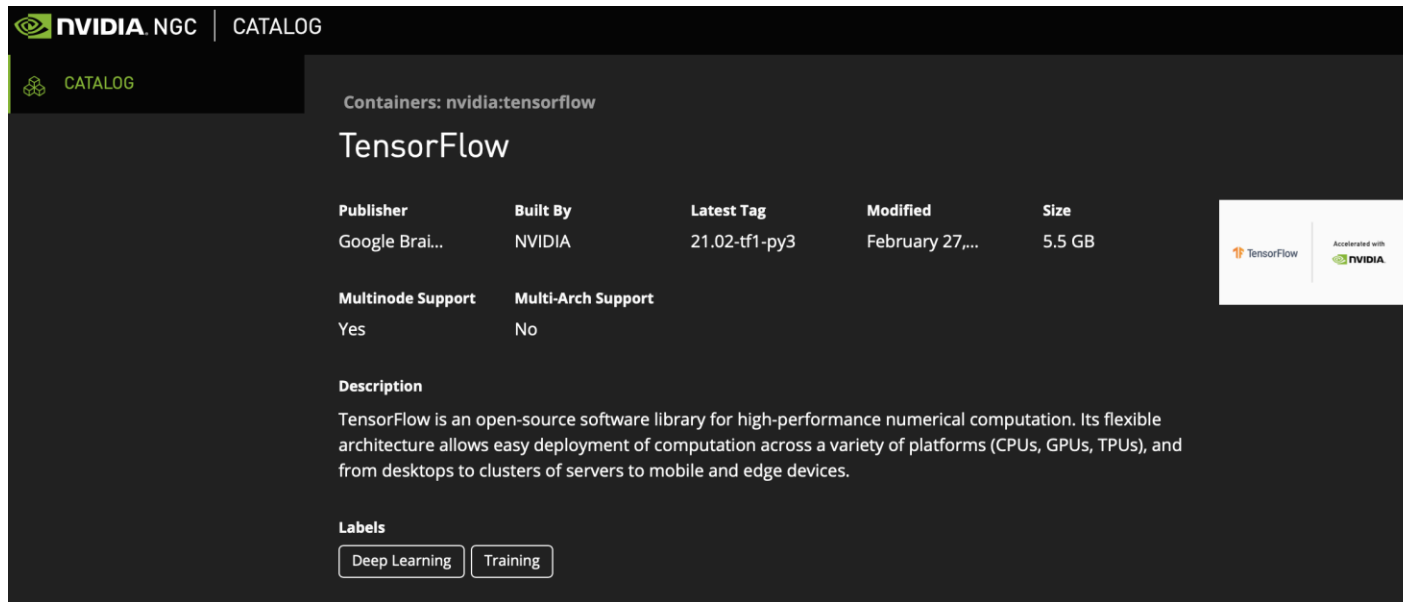
The 'Description' section states: 'PyTorch is a GPU accelerated tensor computational framework with a Python front end. Functionality can be easily extended with common Python libraries such as NumPy, SciPy, and Cython. Automatic differentiation is done with a tape-based system at both a functional and neural network layer level.'

The 'Labels' section shows two tags: 'Deep Learning' and 'Training'.

On the right side of the interface, there is a badge that says '5.29 GB', 'PyTorch', and 'Accelerated with NVIDIA'.

Source: <https://developer.nvidia.com/deep-learning-frameworks>

# GPU Computing (cuDNN) in Data Science



The screenshot displays the NVIDIA NGC CATALOG interface. At the top, the NVIDIA logo and 'NGC CATALOG' are visible. Below this, a sidebar shows 'CATALOG' with a container icon. The main content area is titled 'Containers: nvidia:tensorflow' and 'TensorFlow'. It features a table with the following data:

Publisher	Built By	Latest Tag	Modified	Size
Google Brai...	NVIDIA	21.02-tf1-py3	February 27, ...	5.5 GB

Below the table, there are two columns: 'Multinode Support' (Yes) and 'Multi-Arch Support' (No). A 'Description' section follows, stating: 'TensorFlow is an open-source software library for high-performance numerical computation. Its flexible architecture allows easy deployment of computation across a variety of platforms (CPUs, GPUs, TPUs), and from desktops to clusters of servers to mobile and edge devices.' At the bottom, a 'Labels' section contains two buttons: 'Deep Learning' and 'Training'. On the right side of the interface, there is a logo for 'TensorFlow Accelerated with NVIDIA'.

Source: <https://developer.nvidia.com/deep-learning-frameworks>



# GPU Computing in Data Science

## ▢ Numba for CUDA GPUs

- ▢ Overview
- ▢ Writing CUDA Kernels
- ▢ Memory management
  - Writing Device Functions
- ▢ Supported Python features in CUDA Python
- ▢ Supported Atomic Operations
- ▢ Random Number Generation
- ▢ Device management
  - The Device List
- ▢ Examples
- ▢ Debugging CUDA Python with the the CUDA Simulator
- ▢ GPU Reduction
- ▢ CUDA Ufuncs and Generalized Ufuncs
- ▢ Sharing CUDA Memory
- ▢ CUDA Array Interface (Version 2)
- ▢ External Memory Management (EMM) Plugin interface
- ▢ CUDA Frequently Asked Questions
- ▢ CUDA Python Reference

[Docs](#) » Numba for CUDA GPUs

## Numba for CUDA GPUs

- Overview
  - Terminology
  - Programming model
  - Requirements
    - Supported GPUs
    - Software
      - Setting CUDA Installation Path
  - Missing CUDA Features
- Writing CUDA Kernels
  - Introduction
  - Kernel declaration
  - Kernel invocation
    - Choosing the block size
    - Multi-dimensional blocks and grids
  - Thread positioning
    - Absolute positions
    - Further Reading
- Memory management
  - Data transfer
    - Device arrays

Distribute  
Training

MPI



# Questions

1. GPUs can be used as a stand-alone parallel system. (T/F)
2. CUDA tools can be used in any GPU architecture. (T/F)
3. Parallel computations can be performed on multiple GPUs on single node or multiple GPUs on many nodes . (T/F)
4. CUDA and MPI can be used together for an efficient parallel communication. (T/F)



# GPUs for Machine Learning algorithms



# GPUs for ML

## Parallel Processing Capability

- High Throughput:
  - GPUs are designed to handle thousands of threads simultaneously
  - Exceptionally good at performing large matrix and vector operations
- Parallel Architecture:
  - Have a massively parallel architecture consisting of thousands of smaller, efficient cores designed for handling multiple tasks simultaneously.
  - This is in contrast to CPUs, which have fewer cores optimized for sequential serial processing.

# GPUs for ML

## Optimized for Matrix Operations

for-loops

- Core ML operations involve heavy matrix calculations.
- GPUs are built to perform these operations quickly and efficiently.
- This results in significant speedups in training and inference times for neural networks.

## Accelerated Model Training

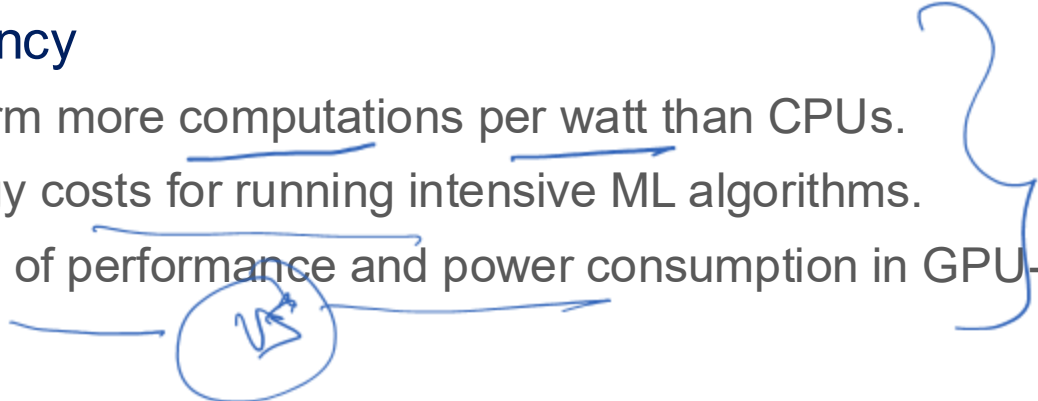
- Traditional CPU cores are optimized for sequential tasks, limiting their speed for ML tasks.
- GPU's parallel processing drastically cuts down model training time, making iterative development and complex model training feasible.

# GPUs for ML

## Scalability for Big Data

- GPUs manage large datasets more efficiently than CPUs.
- Its architecture is suited for scaling up to meet the demands of big data in ML, facilitating faster data processing and insights.

## Energy Efficiency

- GPUs perform more computations per watt than CPUs.
  - Lower energy costs for running intensive ML algorithms.
  - The balance of performance and power consumption in GPU-enabled ML.
- 

# GPUs for ML

## Expansive Software Ecosystem

- Strong Ecosystem for Accelerated Computing
  - Major frameworks: TensorFlow, PyTorch, CUDA.
- Comprehensive GPU Support Optimized for GPU execution.
  - Streamlines development of ML models.
- Optimized Libraries Enhance Performance
  - Linear algebra, Fourier transforms, etc.
  - Facilitate efficient, scalable model development.

# GPUs for ML

## Versatility

- Broad Applicability
  - GPUs accelerate a wide array of ML algorithms, not just deep learning.
- Natural Language Processing (NLP)
  - Language translation, sentiment analysis
  - Faster processing of large language models and datasets
- Computer Vision
  - Image recognition, object detection
  - Real-time processing and analysis of high-resolution images and videos
- Unsupervised Learning
  - Clustering, dimensionality reduction
  - Efficient handling of large-scale datasets for pattern discovery

*Handwritten blue scribbles, possibly representing the letters 'NLP'.*





# GPU Ecosystem Today

## Contributions from Key Players

# GPU Ecosystem Today

- NVIDIA's Dominance
  - NVIDIA plays pioneering role in GPU development for ML and AI.
  - NVIDIA CUDA-X AI is a complete deep learning software stack
  - Setting industry standards in GPU technology.

## NVIDIA Merlin

tag v23.09.00 license apache-2.0 documentation

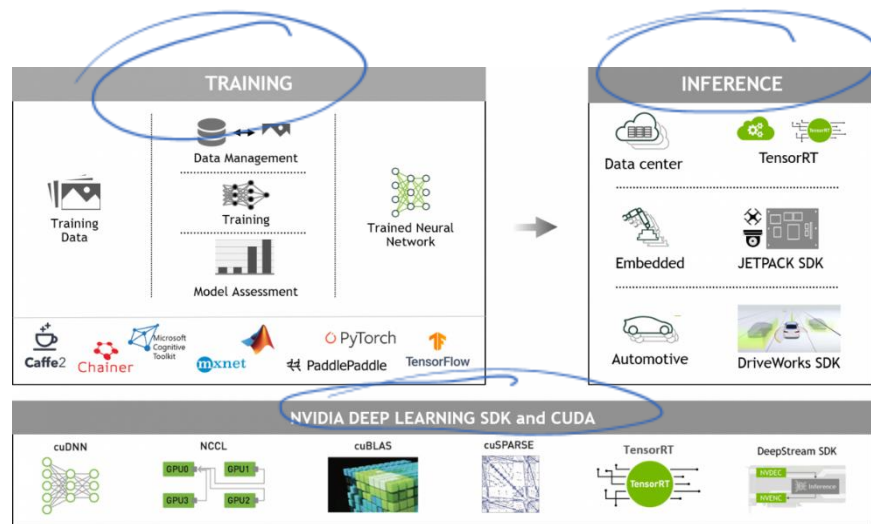
NVIDIA Merlin is an open source library that accelerates recommender systems on NVIDIA GPUs. The library enables data scientists, machine learning engineers, and researchers to build high-performing recommenders at scale. Merlin includes tools to address common feature engineering, training, and inference challenges. Each stage of the Merlin pipeline is optimized to support hundreds of terabytes of data, which is all accessible through easy-to-use APIs. For more information, see [NVIDIA Merlin](#) on the NVIDIA developer web site.

### Benefits

NVIDIA Merlin is a scalable and GPU-accelerated solution, making it easy to build recommender systems from end to end. With NVIDIA Merlin, you can:

- Transform data (ETL) for preprocessing and engineering features.
- Accelerate your existing training pipelines in TensorFlow, PyTorch, or FastAI by leveraging optimized, custom-built data loaders.
- Scale large deep learning recommender models by distributing large embedding tables that exceed available GPU and CPU memory.
- Deploy data transformations and trained models to production with only a few lines of code.

Source: <https://github.com/NVIDIA-Merlin/Merlin>



Source: <https://developer.nvidia.com/deep-learning-software>

# GPU Ecosystem Today

## AMD's Advancements

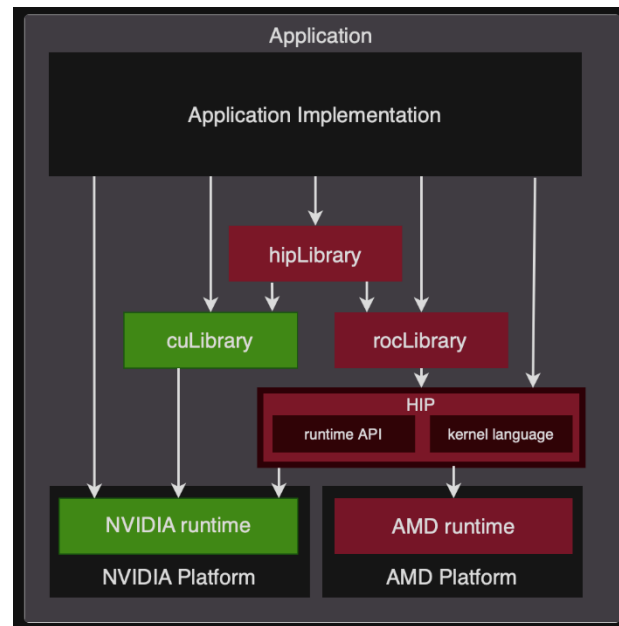
- AMD's focus on open-source platforms.
- ROCm (Radeon Open Compute) platform and its support for deep learning frameworks.
- Providing an alternative to NVIDIA's ecosystem with competitive performance.



Source: <https://www.amd.com/en/products/software/rocm.html>

- **Heterogeneous-computing Interface for Portability (HIP)**

- a C++ runtime API and kernel language that lets developers create portable applications running in heterogeneous systems, using CPUs and AMD GPUs or NVIDIA GPUs from a single source code.
- Provides a simple marshalling language to access either the AMD ROCM back-end, or NVIDIA CUDA back-end, to build and run application kernels.



Source: [https://rocm.docs.amd.com/projects/HIP/en/latest/what\\_is\\_hip.html](https://rocm.docs.amd.com/projects/HIP/en/latest/what_is_hip.html)

# GPU Ecosystem Today

## Intel GaUDI

- Intel's recent efforts in GPU technology for AI and ML, focusing on versatility.
- Intel's Xe architecture GPUs and oneAPI.
- Diversifying the GPU market and offering integrated CPU-GPU solutions.

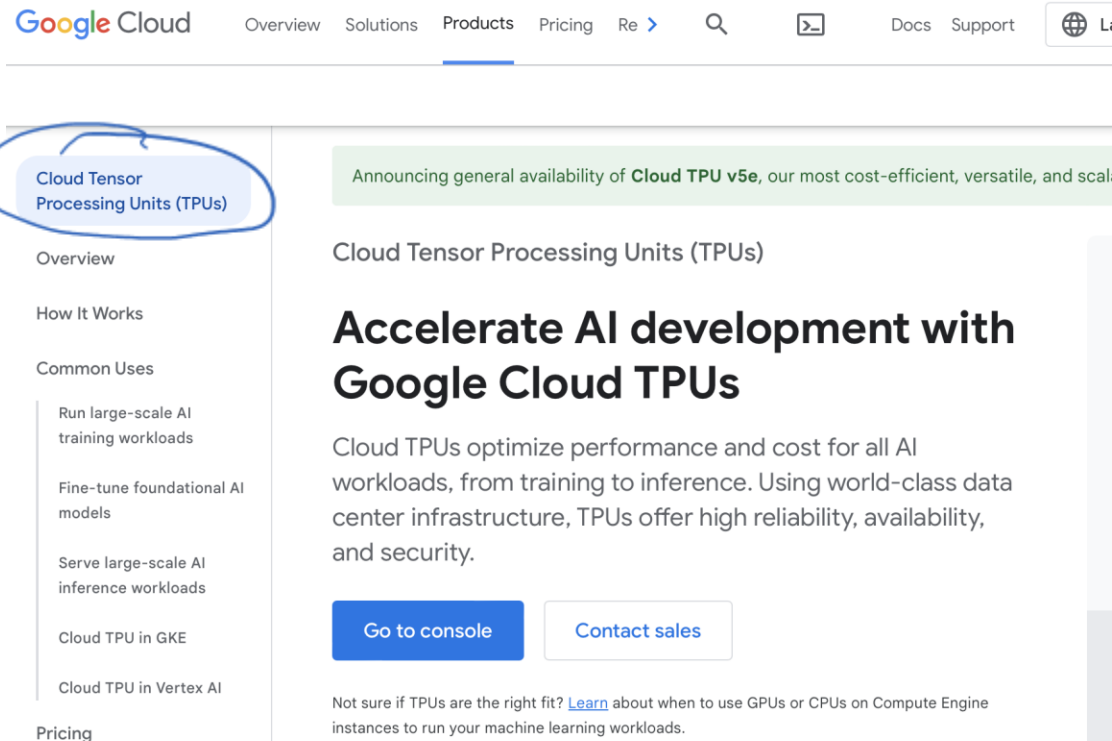
Source: <https://habana.ai/products/>




Source: <https://www.intel.com/content/www/us/en/developer/topic-technology/artificial-intelligence/get-started.html>

# GPU Ecosystem Today

Source:

<https://cloud.google.com/tpu>



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**Cloud Tensor Processing Units (TPUs)**

Overview

How It Works

Common Uses

- Run large-scale AI training workloads
- Fine-tune foundational AI models
- Serve large-scale AI inference workloads
- Cloud TPU in GKE
- Cloud TPU in Vertex AI

Pricing

Announcing general availability of **Cloud TPU v5e**, our most cost-efficient, versatile, and scal

## Cloud Tensor Processing Units (TPUs)

# Accelerate AI development with Google Cloud TPUs

Cloud TPUs optimize performance and cost for all AI workloads, from training to inference. Using world-class data center infrastructure, TPUs offer high reliability, availability, and security.

[Go to console](#) [Contact sales](#)

Not sure if TPUs are the right fit? [Learn](#) about when to use GPUs or CPUs on Compute Engine instances to run your machine learning workloads.

# Nvidia CUDA: Machine Learning Libraries

- **Major ML Libraries Based on CUDA**

- **TensorFlow**: A popular deep learning framework that can utilize CUDA for accelerated model training and inference.
- **PyTorch**: Another widely-used framework for deep learning, leveraging CUDA for faster computation and model experimentation.
- **cuDNN** (CUDA Deep Neural Network library): A GPU-accelerated library for deep neural networks that provides highly tuned implementations for standard routines such as forward and backward convolution, pooling, normalization, and activation layers.
- **RAPIDS**: A suite of open-source software libraries, including cuDF and cuML, for executing end-to-end data science and analytics pipelines entirely on GPUs.



# GPUs for ML

## Summary

- GPUs are critical to machine learning (ML) computations.
- They provide substantial improvements in speed, efficiency, and scalability.
- There are several open-source GPU libraries, mostly aligned with a single hardware vendor.
- With the increasing complexity and size of ML models and datasets, GPUs are set to become increasingly indispensable in ML.