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Ph.D. Thesis

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**Development of Phase Reference Distribution Systems
of Linear Particle Accelerators with Femtosecond Stability**

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Podziękowania

Chciałbym podziękować mojemu opiekunowi dydaktycznemu i promotorowi, dr hab. inż. Krzysztofowi Czubie, za niezawodne wsparcie oraz za możliwość korzystania z jego wieloletniego doświadczenia, co stanowiło nieocenioną pomoc przy pisaniu niniejszej rozprawy doktorskiej. Podziękowania kieruję także do dr hab. inż. Adama Abramowicza.

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Niniejsza rozprawa została napisana na podstawie prac wykonanych w ramach następujących projektów badawczych:

- Prace rozwojowe nad systemami generatorów wzorcowych, synchronizacji oraz sterowania akceleratorów XFEL, FLASH oraz SINBAD-Appendix 4 do umowy DESY-PW. Prace w ramach projektu międzynarodowego współfinansowanego ze środków programu Ministra Nauki i Szkolnictwa Wyższego pn. "PMW" w latach 2020-2021, umowa nr 5083/DESY/2020/0,
- Prace rozwojowe nad systemem dystrybucji sygnału synchronizacji akceleratora SINBAD, oraz modułów syntezatorów częstotliwości. Prace w ramach projektu międzynarodowego współfinansowanego ze środków programu Ministra Nauki i Szkolnictwa Wyższego pn. "PMW" w latach 2019-2020, umowa nr 5028/DESY/2019/0,
- Badania i rozwój systemów RF dla akceleratorów FLASH, SINBAD i XFEL-Appendix 6 do umowy DESY-PW,
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The thesis was developed during work in following projects:

- Developments for Master Oscillator, RF Synchronization and LLRF Systems for XFEL, FLASH and SINBAD Accelerators-Appendix 4 to DESY-WUT agreement. Project co-financed by the Polish Ministry of Science and Higher Education, funds for years 2020-2021, agreement number 5083/DESY/2020/0.
- Developments RF Synchronization System for SINBAD Accelerator and Local Oscillator Modules - co-founded by Polish Ministry of Higher Education, funds for years 2019-2020, agreement number 5028/DESY/2019/0.
- Research and development on RF Systems for FLASH, SINBAD and XFEL Accelerators - Appendix 6 to DESY-WUT agreement.
- Prototype of precise Synchronization System for Linear Accelerators. Research was funded by POB-HEP of Warsaw University of Technology within the Excellence Initiative: Research University (IDUB) programme.

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In memory of my beloved late grandmother, Grażyna Urbańska, who was not given a chance to see this thesis and without whom it would have never been created.

Streszczenie

W rozprawie opisano prace nad rozwojem technologii systemów precyzyjnej synchronizacji liniowych akceleratorów cząstek elementarnych. Przedstawiono w niej m.in. opracowania nowych lub istotnie zmodernizowanych elementów wspomnianych systemów oraz opracowaną przez autora metodykę projektowania zapewniającą uzyskanie wysokiej precyzyji synchronizacji. Metodyka ta została sprawdzona na przykładach opisanych w pracy elementów systemów generacji i dystrybucji sygnałów synchronizacji dla akceleratorów liniowych w ośrodku badawczym DESY w Hamburgu. Moduły opisane w pracy są stosowane w systemach synchronizacji akceleratorów European-XFEL, FLASH2020+ (częstotliwość pracy 1300 MHz) oraz w nowym eksperymencie DESY - SINBAD (częstotliwość 3000 MHz). Opisano także realizowany w ramach projektu PW IDUB prototyp interferometrycznego łącznika stabilizacji fazy, pracujący z sygnałem o częstotliwości 162.5 MHz. Przedstawione w pracy moduły, metody i systemy stanowią autorski wkład w rozwój systemów sterowania dla liniowych akceleratorów cząstek elementarnych.

W części wstępnej rozprawy omówiono problematykę budowania precyzyjnych systemów synchronizacji akceleratorów, ze szczególną uwagą poświęconą projektom, w których zostały wykorzystane rozwiązania opracowane przez autora. Przedstawiono główne założenia pracy, jej organizację oraz jej wkład w rozwój systemów generacji i dystrybucji sygnałów odniesienia w liniowych akceleratorach cząstek elementarnych. Przedstawiono podstawy teoretyczne zjawisk wpływających na parametry synchronizacji modułów akceleratora, w szczególności zjawiska szumu fazowego źródeł sygnałów w.cz i dryfu fazy wprowadzanego przez zastosowane w systemach dystrybucji media transmisyjne i elementy. Następnie omówiono elementy systemów dystrybucji, opracowane dla wymienionych akceleratorów cząstek elementarnych. Przedstawiono rozwiązania umożliwiające syntezę sygnału referencyjnego w.cz o niezwykle małym poziomie szumów fazowych (jitter rzędu 10 fs w paśmie 10 Hz - 1 MHz), czy długoterminowej stałości fazy poniżej 100 fs w układach o długościach kilkudziesięciu metrów. Opracowano precyzyjny moduł stabilizowanego termicznie rozdzielacza sygnału referencyjnego z wbudowanymi obwodami diagnostycznymi, link aktywnej stabilizacji fazy, moduł precyzyjnego konwertera częstotliwości sygnału wzorcowego w.cz oraz technikę izolowania krytycznych elementów systemów dystrybucji od czynników środowiskowych.

W formie załączników przedstawiono także opracowane i współpracowane przez autora metody projektowe i komponenty uzupełniające dla systemów dystrybucji akceleratorów European Spallation Source i SINBAD.

Słowa kluczowe

Sygnal odniesienia, generator wzorcowy, system generacji i dystrybucji sygnału synchronizacji, konwersja częstotliwości, European-XFEL, FLASH2020+, dryf fazy, stabilizacja fazy, szum fazowy, dzielniki mocy w.cz, przesuwni fazy, detektory fazy, liniowe akceleratory cząstek.

Uwaga odnośnie praw autorskich

Zgodnie z umowami zawartymi między Instytutem Systemów Elektronicznych i ośrodkami DESY i ESS oraz ze względu na charakter przedstawionych w pracy rozwiązań i ich wykorzystanie w instalacjach w wyżej wymienionych ośrodkach w niniejszej rozprawie nie zostały przedstawione informacje umożliwiające odtworzenie omawianych urządzeń.

Abstract

The thesis presents the development of phase reference distribution systems (PRDS) and their components used in linear particle accelerators' control systems. The thesis covers new or significantly upgraded modules and components of the phase reference distribution systems and a novel design technique for these components. Results of author's work were successfully used for developing phase reference distribution system components for linear particle accelerators in DESY, Hamburg, i.e for the European-XFEL, the upgraded FLASH2020+ (1.3 GHz frequency), and newly built SINBAD (3.0 GHz frequency) facilities in DESY. The thesis also covers a prototype interferometric phase drift compensating link designed to work at 162.5 MHz, a result of the WUT IDUB grant.

The introductory chapters of the thesis cover the main aspects of PRDS development, and the systems designed in the scope of the thesis are emphasized. The main thesis goals, its layout, and its contribution to the development of linear particle accelerators' PRDS are given. The work covers the theoretical background that defines the most important phenomena which affect and limit the performance of any PRDS, particularly the phase noise of RF signal sources and the impact of phase drifts introduced by reference transmission lines and system components. Then, the designed PRDS components and concepts are described. A new design of the main RF reference oscillator, achieving RF signal's time jitter of 10 fs (in integration range from 10 Hz to 1 MHz), and active phase compensating link for long-term phase stability better than 100 fs are presented. Designed custom RF high power distribution module with embedded diagnostics and high-precision RF frequency converter module are presented. A developed technique for improving the systems' components' invulnerability to environmental factors and distortions is given.

Appendices cover all created design methods and supplementary components for distribution systems, designed and co-designed by the author for the European Spallation Source and SINBAD.

Keywords

RF reference signal, Master Oscillator, Main Oscillator, phase reference distribution system, PRDS, frequency conversion, European-XFEL, FLASH2020+, phase drift, phase stabilization, phase noise, RF power splitters, RF phase shifters, RF phase detectors, linear particle accelerators.

Remark on copyrights

Due to the cooperation agreement and its appendices signed by the Institute of Electronic Systems and DESY, and ESS, but also because of the presented devices' character and their use in mentioned accelerator facilities the thesis does not present any information that would allow reproducing presented devices and modules.

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1. Introduction

Curiosity has always been among the most important factors affecting growth and development in many fields. It motivates people to further analyze and study the surrounding world. It results in revealing more of its secrets, even at the earliest stages, as described, for instance, by Swiss psychologist Jean Piaget, the author of the theory of children's cognitive development [1] or Maria Montessori in her works on the philosophy of education and scientific pedagogy [2]. As the world is quite a complex structure, an obvious idea of research is to divide it into small and easier-to-comprehend parts, perform their observations and tests, and then upon the acquired results, create theoretical models that describe them. Such a very flexible research idea has been used in many applications over the years, especially in physics. As the research in many fields proceeded, it has been inevitable to reach a point when further research, using dividing its object into smaller parts, has no longer been possible without implementing new testing devices and methods. In 1911 Ernest Rutherford published his model describing a single atom, which was then in 1913 updated by Niels Bohr by including quantum effects description and analysis. In the 1920s and 1930s first prototypes of particle accelerators were made to verify the structure of the atomic nucleus. The first prototype of a linear particle accelerator, the so-called linac, was designed in 1928 by R. Wideröe, as a proof of concept of G. Ising [3]. However, the first accelerator able to accelerate particles to energies of about 1.25 MeV was designed three years later, in 1931 by D. Sloan at the University of Berkeley. In the meanwhile, in 1930, the first circular accelerator was made by E. Lawrence at the University of California. Starting from the 1930s, a huge and rapid development in particle accelerators was observed and not only not disturbed, but even boosted, by World War II, when the techniques of ultra-high frequencies advanced rapidly. In the last 60 years, there have been roughly thirty thousand different particle accelerators made around the world [4]) to help in the understanding of high energy physics, but also for the development of everyday applications [4, 5, 6]. A good illustration of the development in particle acceleration is shown in Fig. 1 as the growth of accelerator beam energy over the years.

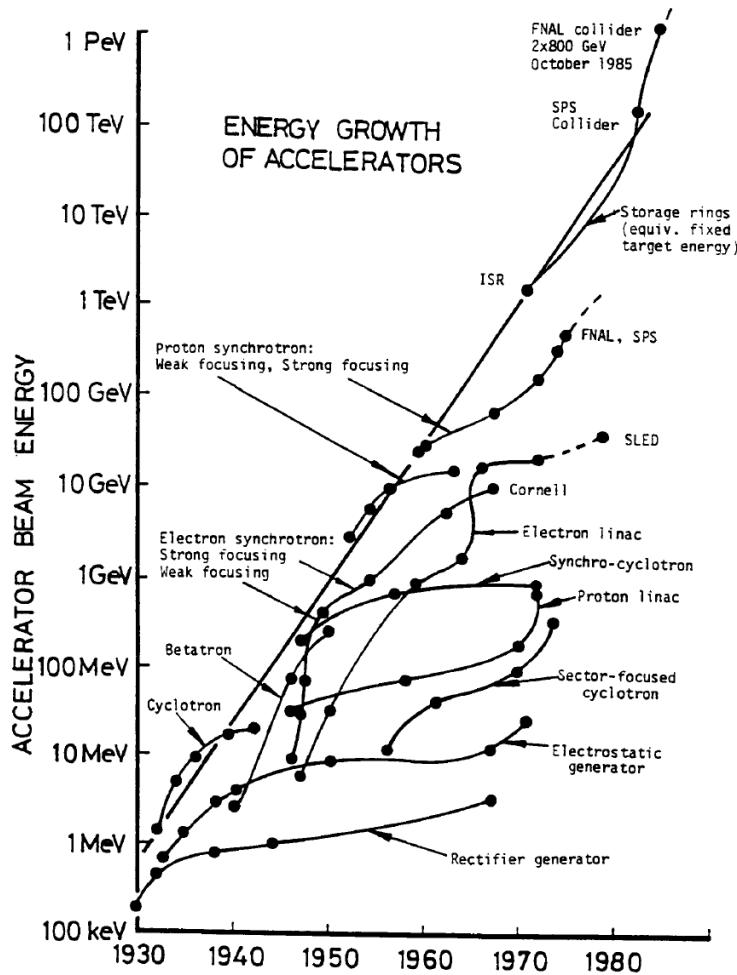


Figure 1: Energy growth of accelerators, a.k.a Livingston Chart, published in [3].

Basic applications of particle accelerators cover experiments in high-energy physics, which will lead to a better understanding of the matter. Accelerators are also used to record the flow of chemical reactions at the sub-atomic level and "slow-motion" in the range of femtoseconds. They are also widely used in the industry, for instance, for ion-implantation in semiconductors in processes of integrated circuits production. Accelerators may also test the material properties used in power engineering and electronics, just to mention the importance of testing the performance of high-voltage and high-power wire insulating materials and heat shrink tubes and packaging [5]. There is much hope for potential applications of accelerators in optimizing nuclear power plants and utilizing radioactive waste. In medicine, they are widely used to detect and treat tumors, de-contaminate surgical tools, and for water purification. Recent years and the COVID-19

pandemic created an opportunity to use particle accelerators to deal with SARS-CoV-2 infection complications and determine the level of lung tissue havoc that affected so many people [7].

It is also important to highlight the business factors of the particle accelerators field as this market is rated to rise by 3.5 billion USD per year, corresponding to an annual growth of ten percent [8]. Only the semiconductor production applications generate year-by-year 1.5 billion USD income. All the production processes using particle accelerators in any way sum up to a total annual value exceeding 500 billion USD in 2010 [8].

Particle accelerators can be divided in terms of the principle of operation:

- Direct voltage accelerators with static EM field, like van der Graaf or Cockcroft-Walton generators, very popular in many industrial applications.
- Alternating field driven accelerators (compliant with Ising's concept), including ones based on resonant acceleration - most modern linacs and circular accelerators.

The subject of this work's further analysis will be linear particle accelerators only, as all the phase reference distribution system components and methods presented have been designed for linacs. A simplified structure of a typical linac is presented in Fig. 2 and is very similar to its first prototype by Ising [3].

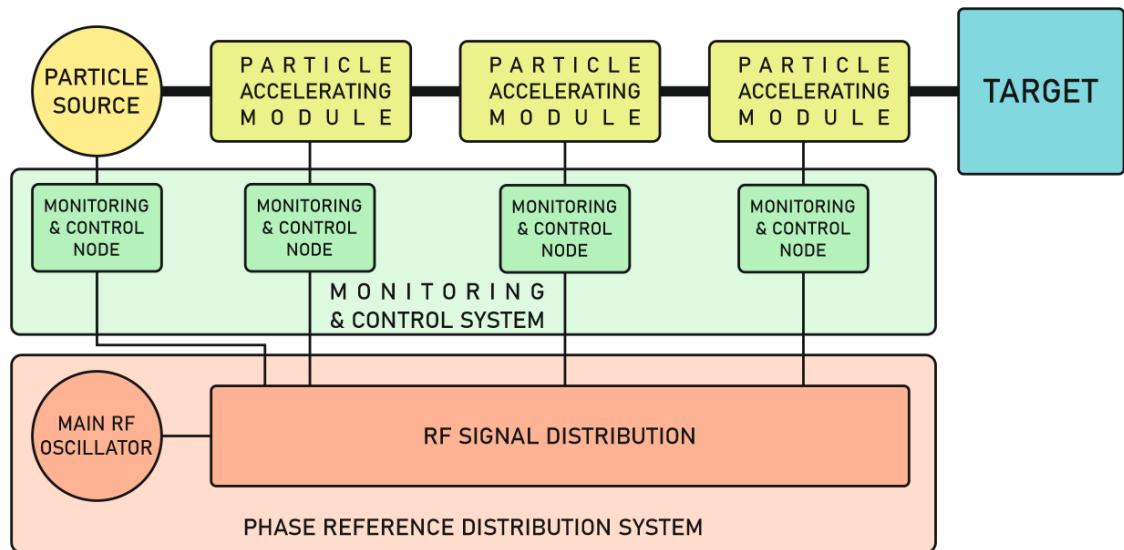


Figure 2: Simplified block diagram of a typical linac, and its control and phase reference distribution systems.

Following main parts of a linac from Fig. 2 can be distinguished:

- A source of particles to be accelerated, also called a gun or RF gun.
- An accelerating module or chain of modules that can accelerate and focus the beam of particles. These may be beam-focusing undulator sections, cryogenic superconductor TESLA-based accelerating cavities [9], [10], or traveling wave structures [10].
- Monitoring and control system for the accelerator's subsystems and modules, which will be further described in the thesis.
- Phase reference distribution system, typically made of:
 - Reference signal generator, often called Master or Main Oscillator (MO) that generates the RF reference signal to be further distributed along accelerator modules and systems.
 - Transmission medium or media that may be used to provide signal made by MO to all accelerators parts - these are mainly coaxial cables, optical fibers, waveguides, often equipped with additional sophisticated systems for phase drift detection and compensation.
 - End-point devices that are used to alter MO signal parameters without losing the synchronization, like custom frequency divider circuits.
- Experiment target that is exposed to an accelerated particle beam and observed by dedicated detectors.

This simplified block diagram shown in Fig. 2 does not reflect the complexity of modern particle accelerators that are often of very significant size, as their lengths often exceed hundreds or even thousands of meters. To ensure their proper work, based on generating particle bunches in a femtosecond timing regime, the dedicated control and monitoring systems must be designed, maintained, and synchronized along the entire accelerator's length to a main RF reference signal. These control systems require very complex, custom-designed, and made components. Selected modules are described in further parts of the thesis.

1.1 Motivation

The rapid growth and development of particle accelerator techniques observed over the last few decades require more and more effort put into accelerator control and synchronization systems. Achieving ultra-focused and ultra-short particle bunches requires very precise timing along the entire accelerator structure, which is often several hundreds of meters long. A properly designed accelerator control system, RF reference signal source, and PRDS are of utmost importance. Achieving time synchronization of several tenths of femtoseconds or less forces engineers and scientists to include phase drift phenomenon in the total PRDS timing budget. A proper selection of PRDS components and compensation methods is crucial for overall performance, and in many cases, these components have to be custom designed to meet all the requirements, especially those related to electron bunches time arrival jitter and time spacing. The thesis concludes the author's experience in phase reference distribution systems and is intended to provide guidelines for the future phase reference distribution system designers.

1.2 Thesis goals and main contribution of the work

A primary goal of this thesis was to identify critical components of a large PRDS and work out novel methods allowing for short and long term, femtosecond level RF phase synchronization of multiple devices. Author presented his research results achieved while working on components for E-XFEL and FLASH PRDS, prototype of a phase drift compensating link at 162.5 MHz and also a prototype structure for SINBAD.

The secondary goal of the thesis was to develop a technology and universal design methods for modern PRDS subcomponents, including thermal stabilization, hermetization, proper shielding, mechanical strength, and improved invulnerability to environmental factors, like vibrations. Developed methods will allow future PRDS designers to minimize signal phase instabilities and assure simplified and robust designs, both in terms of electrical performance and serviceability. A method of designing hermetic metal housings for RF devices is proposed, emphasizing the hermetic RF connection methods for various RF circuits, including high-power ones.

Presented goals and results are an important contribution to the PRDS development and may be used in future projects, not only related to phase reference distribution systems.

1.3 Thesis organization

Chapter 2 is devoted to the theoretical background and description of basic phenomena affecting the PRDS components and system performance. Known sources of phase drifts in coaxial cables and worldwide used methods of their compensation are presented.

Chapter 3 describes selected accelerator facilities worldwide and the PRDS system concepts used there, which was useful during the PRDS prototype structure selection.

Chapter 4 is an introduction to the main contribution part of the thesis. Chapters 5,6 and 7 describe PRDS system components designed for European XFEL and FLASH accelerators in DESY and a prototype of the PRDS link for 162.5 MHz reference signal. Custom frequency converters are presented, including frequency dividing modules for FLASH and XFEL, the FLASH distribution module, and the new FLASH Master Oscillator module.

Chapter 8 presents the PRDS prototype system concept for SINBAD. Methods of phase detection, compensation, and the developed structures of interferometric transmitter and receiver units are given.

The summary and conclusions are given in Chapter 9. The last part of the thesis contains appendices, covering the concept of custom metal housings, and modular RF devices and presents ESS PRDS system components the author has co-designed.

2. Theroretical background

This chapter introduces the theoretical principles of phase reference distribution systems, their subcomponents, and the phenomena that limit their performance. An introduction to linear accelerators' principle of operation, phase reference distribution systems (PRDS,) and RF control systems in linacs is given. A general model of a single-tone harmonic signal is presented and then used to present the basic signal parameter instabilities and fluctuations, of which the phase instabilities are of the most importance in this thesis and therefore are further described, including the types of phase instabilities and their sources, like phase noise introduced by the selected PRDS components or phase drifts in RF transmission media and components, plus the typical compensations methods of these drifts.

2.1 Overview of linacs RF control systems

This part gives an overview of the principle of linac operation. The physics of the particle accelerator is not described in detail, to put the main focus on the RF control system that drives the linac. A more detailed description of the particle acceleration principles is given in [9, 10, 11, 12, 13, 14].

It is generally known that an electromagnetic field is capable of accelerating particles and shaping the curved paths they follow. In particle accelerators, RF fields, generated in standing-wave cavities or Traveling-Wave Structures (TWS), are used to control the beam of accelerated particles and therefore the parameters of these fields are critical for the accelerating process. Photos presenting the cavities and TWS modules used in DESY linear accelerators are shown in Fig. 3, and Fig. 4.



Figure 3: A photo of a standing-wave cavity in TESLA technology, used in DESY linear accelerators. Image source: DESY.



Figure 4: A photo of DESY SINBAD facility TWS modules, under construction in 2018.

As described in [15] The principle of a TWS is that the particle beam travels along the structure synchronously with the phase velocity of the ElectroMagnetic (EM) wave, like a surfer on a water wave. The phase velocity is the rate at which the phase of the wave propagates in space. According to Maxwell's equations, an EM wave traveling along a transverse uniform waveguide has a phase velocity greater than the speed of light. It is necessary for synchronicity, therefore, to reduce the phase velocity of the wave in the structure to the speed of light or less, which may be achieved by inserting regularly-spaced irises or discs.

A TESLA cavity is made of pure niobium and each is made of nine cells (in jargon often named 'doughnuts'). Niobium is a superconductor in ultra-low temperatures. It is worth noting though that the superconducting (in perfect case zero resistance of the conductor) is not preserved in ultra-low temperature for alternating electromagnetic fields, unlike the DC case. The RF fields are able to penetrate the surface of cavities and thus generate heat that must be guided out of the cavity, to keep it in superconducting. Standing wave cavities are organized within accelerating modules. An example of a FLASH accelerating cryomodule, made of eight standing-wave cavities is shown in Fig. 5.

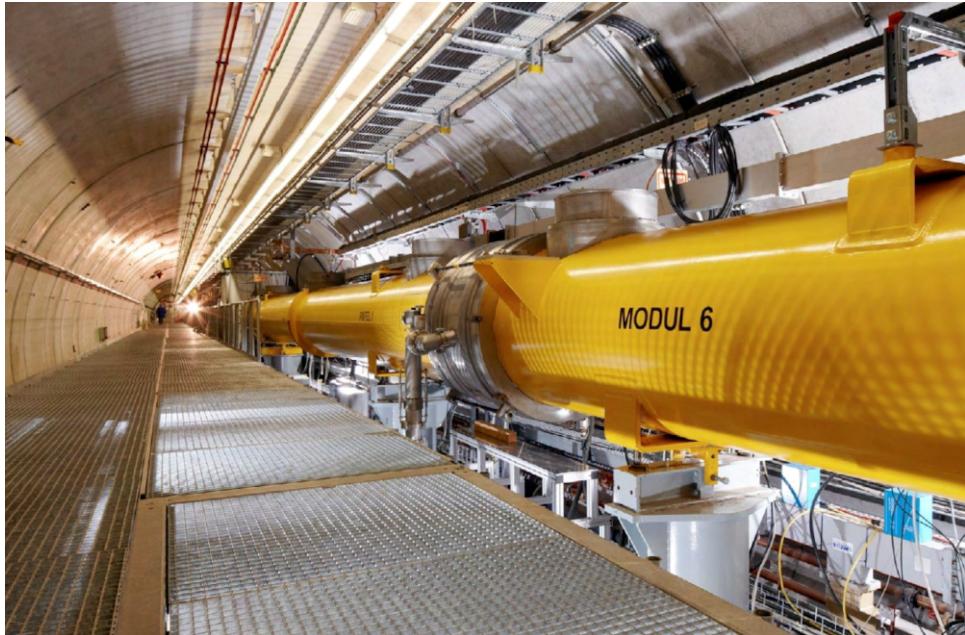


Figure 5: A photo of FLASH cryomodule. Image source: DESY.

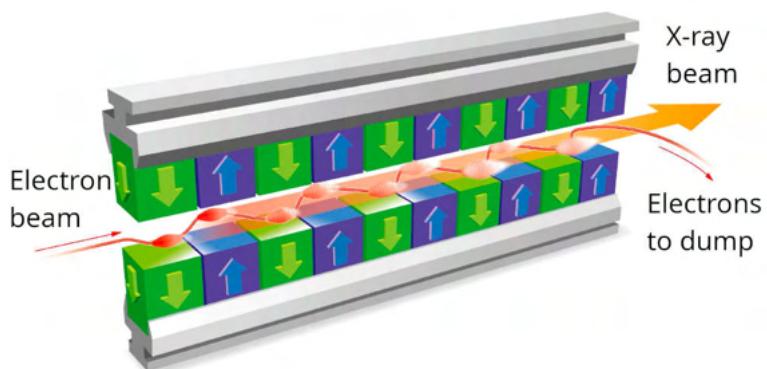


Figure 6: A diagram of E-XFEL undulator.

Linear accelerators are used to generate a high-energy particle beam that is then used to create an ultra-high intensity coherent light beam. Particle beam going through a standing-wave cavity is not equally accelerated. Depending on the phase difference between the particle beam and the accelerating electromagnetic field in the cavity some particles may be accelerated (on-crest acceleration) and some slowed down, which leads to the synthesis of particle bunches [10]. These bunches are then used in systems called Free-Electron Lasers - FELs. The main components are the accelerator, providing bunched particle (electron) beam, and an undulator magnet, as the magnetic field is capable of altering the electrons' trajectory. An FEL is a type of laser. A conventional laser is made of a three-energy-level laser medium, an energy pump, and an optical resonator. The stimulated emission of light is forced between two lower energy states. In a free-electron laser another principle is used. The role of the active laser medium and the energy pump is taken over by the electron beam. Stimulated emission is forced from the higher to lower kinetic energy of the particles. A high energy electron beam (for example 500 MeV electron beam energy means that an electron passed through the voltage of 500 million volts) is then fed to the undulator - a periodic set of electromagnets with alternating polarity (Fig. 6). The magnets route the beam to curves, instead of straight lines, which enables the energy transfer from the electron beam to the light beam. The electric field in the beam is perpendicular to the motion direction of the beam and the force between the electron and the light wave is orthogonal to the electron velocity. To force that energy transfer the electrons must get a transversal velocity and that is why their trajectory is curved by the undulators. This method is particularly useful for the creation of high-energy ultraviolet and x-ray light beams, by using a stochastic process called a self-amplified spontaneous emission (SASE). The ultraviolet and x-ray generation by SASE is possible because in the undulators' input section, incoming electrons produce radiation that is further used as a seed in the undulator's main part. The drive beam for the SASE must have a high peak current, low emittance (ability to maintain a small beam diameter over a long distance), and low energy spread [9]. These requirements are so demanding that only linear accelerators may deliver a proper beam. To generate femtosecond long x-ray pulses the linacs must be equipped with magnetic bunch compressor modules (BCMs). They are used to satisfy the requirement for the high peak current for the drive beam. To generate ultra-short x-ray pulses in a femtosecond regime repeatedly, with tens of

femtosecond intervals between the pulses, all the mentioned linac and FEL modules must be synchronized to a main RF oscillator, also with a femtosecond precision and stability. The monitoring and control of linac and FEL is done with the low- and high-level control systems. The phase reference distribution system maintains the synchronization. The systems are described in the following parts of the chapter.

2.2 Low-Level Radio Frequency control system - the LLRF

Ultra-stable beam requires extraordinary precision in controlling the RF fields in cavities. Particle beam accelerating RF fields are controlled by a Low-Level Radio Frequency (LLRF) system, which measures the parameters of the RF field and beam within the cavity (or TWS) and controls the High-Power Radio Frequency (HPRF) system that drives them [10]. An LLRF node is usually assigned to a single cryomodule or another important part of the accelerator. This means that the LLRF system nodes are distributed along the whole accelerator.

Geng [10] has defined the following requirements for the LLRF system:

- The system must measure and control amplitudes and phases of RF fields and signals precisely (within specified tolerances).
- It supports for remote diagnosis, automation, control of RF fields, and remote maintenance.
- LLRF system ensures the reliability of the entire system, measured with the mean time between failures (MTBF).
- The system must provide a repeatable starting point after the accelerator reboot.

A simple block diagram of a single LLRF node, based on [10] is shown in Fig. 7.

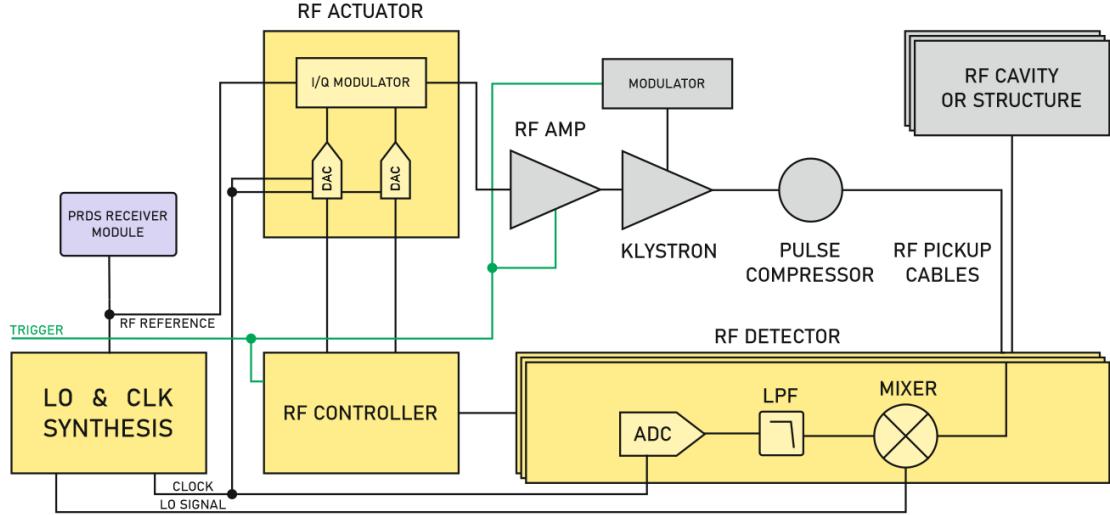


Figure 7: A block diagram of an LLRF system node.

Fraction of the RF cavity field is transported via RF pickup cables and then measured in an RF detector (methods of detection are described in a further part of the chapter). An RF controller provides the feedback and feedforward algorithms to control the field in the cavity, using an RF actuator block. All the LLRF node components use the same RF reference signal, provided by the phase reference distribution system and one of its receivers. LO and CLK synthesis blocks provide signals used by RF detectors for downconversion. A sample diagram of the LLRF system and its supporting systems (like PRDS, and timing system) is presented in Fig. 8 [10]. The PRDS delivers the RF and optical reference signals to all RF nodes and timing system. Timing triggers other subsystems with picosecond precision. All the FEL submodules are synchronized to PRDS signals. By properly adjusting the RF field phases in the following cavities a particle beam experiences the correct conditions for a stable acceleration. All the diagnostics and control features are provided remotely for the user by the control system. Any dangerous conditions or accelerator malfunctions are detected by the protection system that turns the entire machine down.

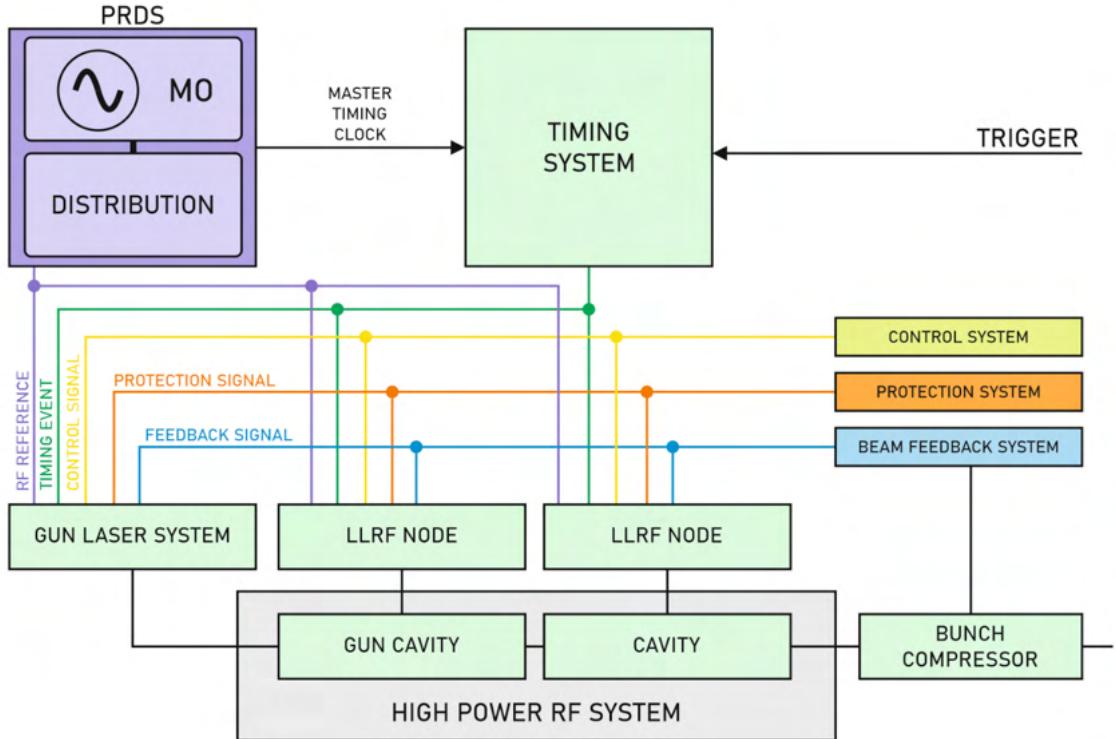


Figure 8: LLRF system node allocation within the linac control systems.

2.3 Introduction to phase reference distribution systems (PRDS)

All the components and modules within the entire accelerator facility have to be driven in proper order and under a strict time regime, which ensures that the charged particles interact with the RF or laser fields as expected. This means that the RF or laser fields must be ready for the beam before it arrives, and the beam itself must be generated in the proper time, so it interacts with RF or laser fields in the proper phase. As described by Geng [10] the timing system and PRDS guarantee the required timing relations between the RF fields and the beam. The timing system is responsible for generating time triggers and events for subsystems. The phase reference distribution system - the PRDS - generates and distributes the reference signal of ultralow phase noise and amplitude stability to all the accelerator substations. The timing system operates therefore in a discrete mode, while the PRDS in a continuous mode - the reference signal is always active and available during accelerator operating time.

In some publications [16] the PRDS is considered as just a part of the bigger RF synchronization system, responsible only for the reference distribution. In other sources [17, 18] the PRDS is assumed to generate the reference and thus the MO is considered a part of the PRDS. The second approach is further used in the thesis.

Gallo [17] and Czuba [18] define the following generic parameters and features of phase reference distribution systems:

- PRDS consists of a reference signal source - Master Oscillator - and a phase stable distribution system.
- PRDS delivers the reference signal to all accelerator subsystems with a strict time regime.
- PRDS generates and monitors the parameters of the reference signal - continuous sinusoid, multi-tone or pulsed.
- PRDS monitors and compensates for introduced distribution system phase drifts, due to thermal gradients along the accelerator.

This part will give a general overview of the PRDS concept. Detailed descriptions, topologies, and examples of PRDSes used worldwide in various research facilities are given in Chapter 3 of the thesis.

A simplified block diagram of a generic PRDS for a linear accelerator, based on [10] is shown in Fig. 9.

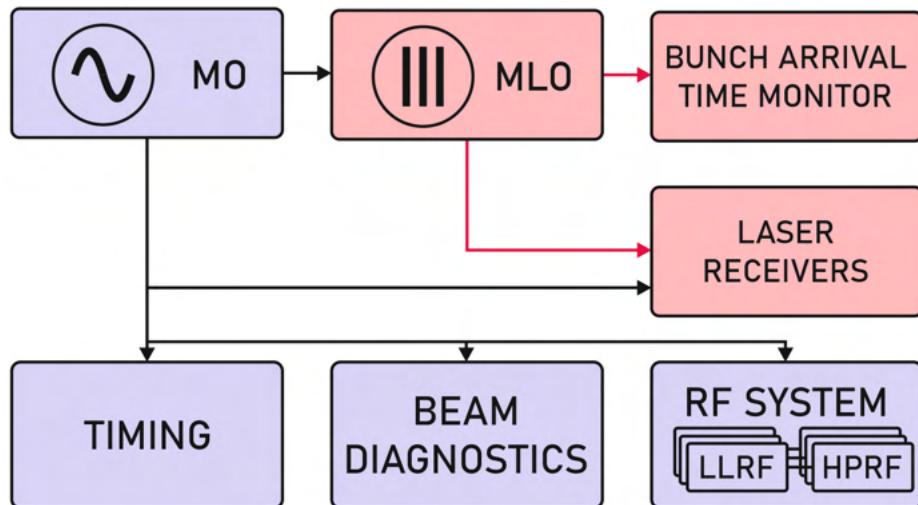


Figure 9: Generic PRDS system block diagram.

PRDS is typically made of a Master (or Main) Oscillator, an ultra-stable ultra-low noise RF reference source, and a distribution network, made of coaxial cables and (in most cases) optical fibers. The distribution network routes the RF reference signal to all the endpoint subsystems, like timing, beam diagnostics, and what is most important, to all LLRF nodes. Each subsystem uses the distributed RF reference to lock to it its local RF or laser signals. In some PRDS optional frequency conversion modules are also used, to further condition the reference signal parameters for the endpoints.

The most important for a PRDS is to deliver the reference signal, without introducing (ideally any) additional phase disturbances. These may be either phase noise or phase drift, both of which are described in detail in the next part of the chapter.

2.4 Harmonic signal and its propagation model

An ideal single-tone harmonic signal, which can be a first approximation of a reference signal from Master Oscillator, may be described by an Eq. (2.1), as described in [19, 20, 21, 22].

$$u(t) = U_0 \cdot \sin(2\pi f_0 \cdot t + \phi_0) \quad (2.1)$$

The model described by Eq. (2.1) is based on an assumption that the signal amplitude U_0 , frequency f_0 , phase $2\pi f_0 t$, and phase deviation ϕ_0 are constant and therefore not affected by any fluctuations, which is oversimplified. An updated model that includes the fluctuations is given in the Eq. (2.2). The model does not include for example parametric noise that affects the signal parameters because of modulation - this will be mentioned in the further part of the chapter.

$$u(t) = (U_0 + \varepsilon(t)) \cdot \sin(2\pi f_0 t + \phi(t)) \quad (2.2)$$

In Eq. (2.2) $\varepsilon(t)$ represents the amplitude instability and $\phi(t)$ phase instability over time. In further parts of the thesis, an assumption is made that the reference signal generated by the MO is amplitude stable (within 0.1 dB) and therefore the amplitude instabilities may be omitted in further discussion and analysis [18].

The phase of the signal presented in Eq. (2.2) (assuming that ϕ_0 is constant and can be omitted) is equal to $\Phi(t) = 2\pi f_0 t$ and is related to the frequency of the signal, as shown in Eq. (2.3)

$$f_0 = \frac{1}{2\pi} \frac{d\Phi(t)}{dt} \quad (2.3)$$

According to [20, 21] following formulas may represent amplitude, phase, and frequency instabilities, without determining their short- or long-term character.

The frequency stability may be considered as a range of frequencies that the measured signal source may generate in a specified measurement time. The frequency instability therefore is defined [21] as:

$$y(t) = \frac{\frac{d\phi(t)}{dt}}{2\pi f_0} \quad (2.4)$$

The frequency instability is related to the speed of signal phase change.

The amplitude instability is defined as a ratio of a deviation of signal amplitude value to the value of the amplitude of the signal, as presented in Eq. (2.5):

$$a(t) = \frac{\varepsilon(t)}{U_0} \quad (2.5)$$

The phase instability is an instantaneous phase deviation, given in units of time and described as Eq. (2.6):

$$x(t) = \frac{\phi(t)}{2\pi f_0} \quad (2.6)$$

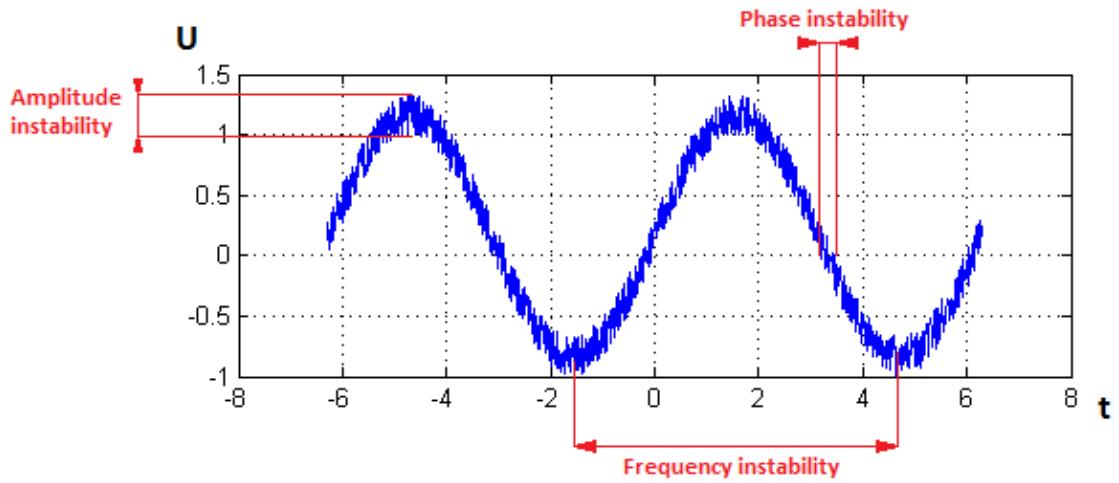


Figure 10: Time plot of real harmonic signal with its instabilities, defined in [21].

The final real single-tone harmonic signal that represents the MO reference signal may be pictured in the time domain as presented in Fig. 10. Fig. 10 presents all the mentioned instabilities, whose sources may be identified as:

- noise phenomena, which affect the short-term signal parameter fluctuations and will be described in further parts of the chapter,
- environmental and aging factors, which introduce long-term fluctuations.

2.5 Types of fluctuations affecting signal performance

One of the main tasks of the LLRF system is to achieve a stable RF field used to drive particle-accelerating structures. For the RF reference signal the required stabilities of amplitude jitter and phase jitter at levels of 1e-4 RMS and 0.01 degree of phase change correspondingly force to include instability and noise models in the process of analysis and design of such systems [10, 17].

A real single-tone harmonic signal with mentioned instabilities may be represented in the frequency domain by a spectrum presented in Fig. 11. It is clear that not the whole power of the signal is distributed in the main tone, but some part is present in the sidebands, due to AM and PM components, which do not have to be equal.

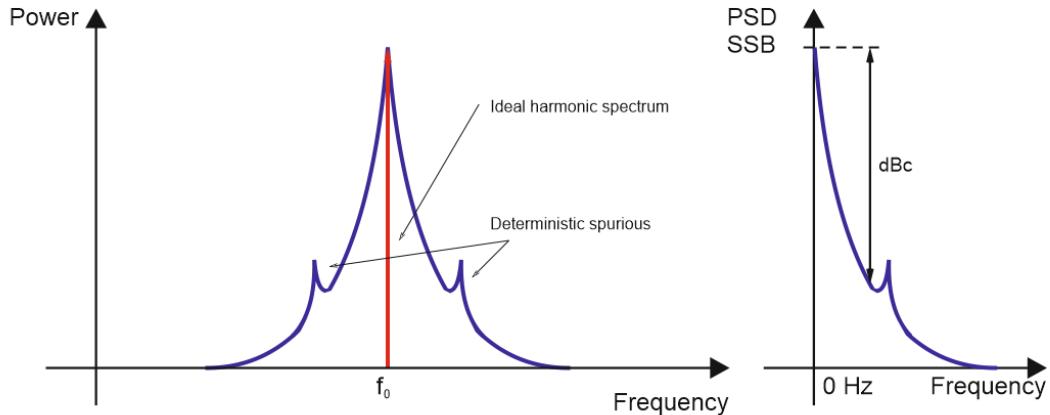


Figure 11: Harmonic signal spectrum and its sideband, caused by phase instabilities.

An ideal harmonic sinewave signal spectrum is a Dirac function, spread into both sidebands, due to mentioned instabilities. In practice, only one of the sidebands is analyzed and most of the further described parameters (unless written otherwise) are assumed to be defined as Single SideBand (SSB). The instabilities of parameters of the reference signal may be caused by both deterministic and random components, which may be long-term and short-term. Long-term frequency stability may be described as phase changes taking

place over some long time, usually hours, days, or more. Short-term phase instabilities include all the instantaneous phase changes that occur in a time interval of seconds. Rohde and Rubiola [23] describe short-term instabilities as ones extending to 1 second, in some cases up to one minute - anything longer is considered a long-term instability, like for example component aging. Another way of distinguishing between short-term and long-term phase instabilities, utilizing cutoff-frequency [10] is presented in the further part of the chapter. The deterministic component gathers not only all external signal disturbances and distortions, further called spurious, but also the long-term phase changes, which are further called phase drifts in the thesis. Random component is made of short-term deviation - phase noise mostly. Phase instabilities may be also considered absolute and relative. Absolute instabilities represent the overall phase noise at the system output and may be measured directly at that output. They include the phase noise introduced by a signal source (in PRDS that is the MO) and all the RF components that are in the signal chain. The relative instabilities may be considered as a phase noise introduced by a selected component in the signal chain or as a way to measure system phase drifts, by taking the output phase change in relation to the input source, which is a way to measure the quality and accuracy of synchronization provided by the PRDS.

2.5.1 Selected definitions and parameters of electrical noise

Electrical noise is an unwanted random fluctuation in electronic devices. For the scope of the thesis, it is assumed that the electronic noise is generated by the device or system under test and all externally coupled noise is considered as external distortion that is not further analyzed. In RF systems, like LLRF or HPRF, the noise limits the final accelerator performance, like for example field stability [10]. The analysis of electrical noise and its sources is an important task during any RF system analysis and design process.

Electrical noise is considered a stationary stochastic process (its statistical parameters do not change over time) and thus should be described using statistical methods and its parameters can be calculated using the measurements performed in the time domain. In the frequency domain, noise parameters are random variables. the Power Spectral Density (PSD), marked further also as $S(f)$ describes the signal power distribution at different frequencies (in a continuous or discrete-sampled way). The unit of PSD, referred to power, is W/Hz , although other references are often used. The PSD of a phase instability is

described by the unit of rad^2/Hz . As presented in [10] the PSD describes the average power of any $x(t)$ noise in a 1 Hz bandwidth at different frequencies in both sidebands and is calculated using Eq. (2.7) and as shown in Fig. 12. It may be also defined for the signal in time domain $x(t)$ as the average of the square of the Fourier transform magnitude over a long time interval [10]. The single sideband (SSB) PSD for the noise $x(t)$ is defined by the Eq. (2.8) and is used in that SSB form in the thesis. The mean value of $x(t)$, which is the power of the noise signal is calculated using Eq. (2.9).

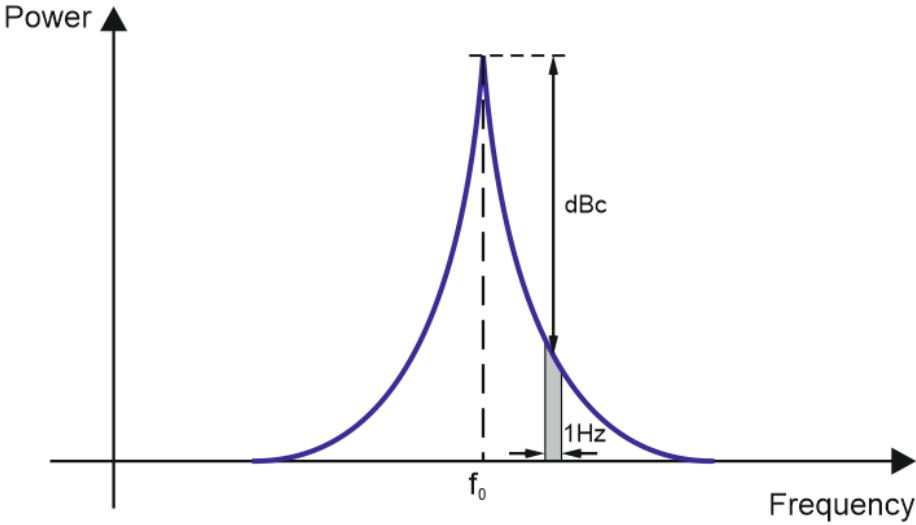


Figure 12: Harmonic signal spectrum and its sideband, caused by phase instabilities.

$$S_{x_{DSB}}(f) = \lim_{T \rightarrow \infty} \frac{1}{T} \left| \int_0^T x(t) e^{-j2\pi ft} dt \right|^2 \quad (2.7)$$

$$S_{x_{SSB}}(f) = S_x(f) = \begin{cases} 2S_{x_{DSB}}(f) & f \geq 0 \\ 0 & f < 0 \end{cases} \quad (2.8)$$

$$\langle x^2(t) \rangle = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{T/2} x^2(t) dt = \int_0^\infty S_x(f) df \quad (2.9)$$

According to the Parseval's theorem, the power of a signal $x(t)$ both in time and frequency domains are equal. Therefore:

$$P = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T |x(t)|^2 dt = \int_0^\infty S_x(f) df \quad (2.10)$$

Another important tool to describe the noise parameters of signals and sources is the Signal to Noise Ratio (SNR). It is described as a ratio of the signal power and noise power and is described by the Eq. (2.11). SNR is the ratio of the output noise power from the circuit to the output noise power from an equivalent, noise-free circuit [23].

$$SNR = \frac{P_S}{P_N} \quad (2.11)$$

The noise factor F is a way to describe the degradation of SNR caused by an element or system measured. It is one of the most important noise parameters of electronic devices and components. Citing the IRE definition the noise factor [24], at a specified input frequency, is a ratio of (1) the total noise power per unit bandwidth at a corresponding output frequency available at the output port when the noise temperature of the input termination is standard (290 K) to (2) that portion of (1) engendered at the input frequency by the input termination. There are several ways to describe the noise factor. One method introduces the SNR degradation definition Eq. (2.12), and the other method uses the PSD concept Eq. (2.13). The Noise Figure (NF) is simply a noise factor F in logarithmic scale, as described in Eq. (2.14).

$$F = \frac{SNR_{INPUT}}{SNR_{OUTPUT}} \quad (2.12)$$

$$F = \frac{S_{OUT}}{S_{IN}G_P} \quad (2.13)$$

$$NF[dB] = 10\log_{10}F \quad (2.14)$$

Another definition of noise factor is given in the Eq. (2.15), where P_{NOUT} is the total noise power at the output of the system (generator and device under test), P_{NGEN} is the total noise power originated from the generator only and P_{NDEV} is the total noise power originated from the device under test only.

$$F = \frac{P_{NOUT}}{P_{NGEN}} = \frac{P_{NGEN} + P_{NDEV}}{P_{NGEN}} = 1 + \frac{P_{NDEV}}{P_{NGEN}} \quad (2.15)$$

For a cascaded set of noisy RF two-port devices, a total noise factor is calculated using the Friis formula in Eq. (2.16)

$$F_{TOTAL} = F_1 + \frac{F_2 - 1}{G_{P1}} + \frac{F_3 - 1}{G_{P1}G_{P2}} + \cdots + \frac{F_n - 1}{G_{P1}G_{P2}\cdots G_{P(n-1)}} \quad (2.16)$$

Following assumptions are made for this formula to work. First, the overall noise factor is referred to the input of the cascade. Next, the component fluctuations are considered to be statistically independent (and therefore not correlated). The last, rather naive, assumption is that all the cascade components are perfectly matched and therefore do not suffer from the power gain reduction caused by reflections.

In terms of PSD value over a wide frequency range, there are several different types of electric noise specified. A Johnson noise, otherwise known as thermal noise or Nyquist noise is caused by thermal fluctuations in a conductor, like a resistor for example, when its temperature is higher than 0 K. There is no need for any external voltage connected to the conductor. This type of noise has a flat power spectral density over a very wide frequency range (up to THz), therefore it is a white noise. At room temperature (290 K) the thermal noise PSD is equal to -174dBm/Hz . For a matched load the thermal noise PSD is defined by the Eq. (2.17).

$$S_{Johnson}(f) = kT \quad (2.17)$$

Another important type of noise in terms of RF noise PSD is $1/f$ noise. This type of noise is also known as flicker noise, or excess noise, and is caused by many factors and slowly changing processes in the conductor or semiconductor structure, like resistor excess noise, electron trapping close to the MOSFET gate, semiconductor aging processes, and others. The PSD of $1/f$ noise is not constant over frequency and is inversely proportional to the frequency, as described by the Eq. (2.18), where A is a constant value and $\alpha \in (0; 4)$ is a noise order number. This type of noise, depending on the value of α may represent white noise, pink noise (PSD dropping by 3dB per octave), or Brownian noise (PSD dropping by 6 dB per octave).

$$S_{\frac{1}{f}}(f) \propto \frac{A}{x^\alpha} \quad (2.18)$$

The influence of selected types of noise is depicted in Fig. 13 and is described by the polynomial law [23, 25], an example is given for the phase noise, described in the next part. Depending on the value of α following types of noise are defined in Fig. 13 [10, 25]:

- $\alpha = 0$ - white phase noise,
- $\alpha = 1$ - flicker phase noise,
- $\alpha = 2$ - white frequency noise,
- $\alpha = 3$ - flicker frequency noise,
- $\alpha = 4$ - frequency random walk [25] or wander [21, 22].

The overall PSD of phase noise may be described as shown in Eq. (2.19) [25]:

$$S_\phi(f) = \sum_{i \leq -4}^0 b_i f^{-i} \quad (2.19)$$

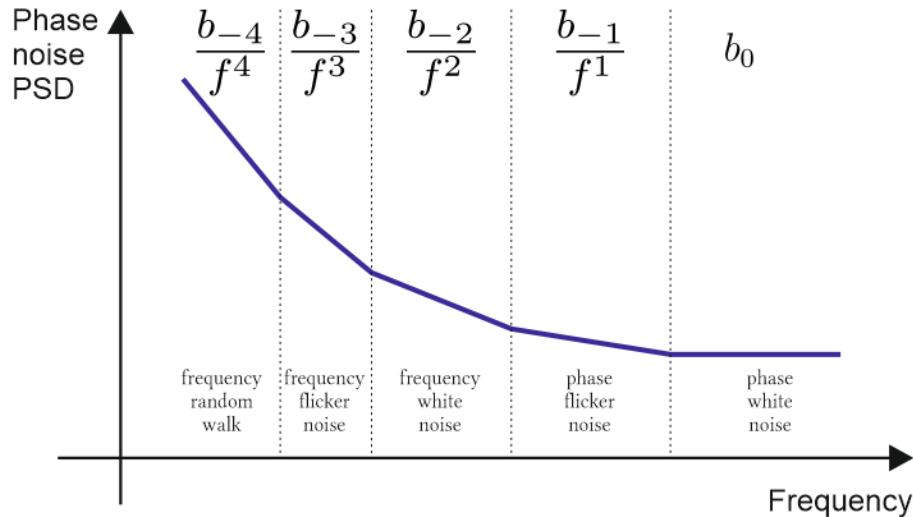


Figure 13: Polynomial law, phase noise PSD distribution over frequency.

There are also other types of noise defined, like burst noise, and shot noise, which are also defined by other noise "colors" (except the Brown's noise), but since they are not of that much importance to phase noise, they are not described in the thesis.

2.5.2 Phase noise and time jitter. Phase drifts

The MO reference signal in PRDS is described by the Eq. (2.2), which may be rewritten to a form that explicitly presents only the phase noise Eq. (2.20) [10] and all the already mentioned instabilities are described by Eq. (2.5), Eq. (2.4) and Eq. (2.6) in time-domain and corresponding PSD values Eq. (2.21) and Eq. (2.22) [21, 22], all in a selected frequency bandwidth BW .

$$u(t) = U_0 \cdot \sin(2\pi f_0 \cdot t + \phi(t)) \approx U_0 \sin(2\pi f_0 t) + U_0 \phi(t) \cos(2\pi f_0 t) \quad (2.20)$$

$$S_\alpha(f) = \alpha_{rms}^2(f) \frac{1}{BW} \quad (2.21)$$

$$S_\phi(f) = \phi_{rms}^2(f) \frac{1}{BW} \quad (2.22)$$

The first component in Eq. (2.20), $U_0 \sin(2\pi f_0 t)$, represents the reference signal and the other component represents phase noise. When the signal described by Eq. (2.20) is applied to some matched resistance R then two powers for the reference signal and phase noise components may be specified as Eq. (2.23) and Eq. (2.24), as is shown in [10] and Fig. 14.

$$P_s = \frac{U_0^2}{2R} \quad (2.23)$$

$$P_\phi = \frac{U_0^2 \Delta \phi_{rms}^2}{2R} \quad (2.24)$$

According to [21, 22] the PSD has been historically used in metrology, however, the prevailing method of phase noise characterization among measurement equipment manufacturers and users of frequency standards is the $\mathcal{L}(f)$, which is defined as the ratio of single sideband power caused by phase noise phase modulation in a 1 Hz bandwidth to the total signal power. The recent definition of $\mathcal{L}(f)$ is given in Eq. (2.25) and valid also for high values (greater than 0.1 rad^2) of mean squared phase deviation $\langle \phi^2(t) \rangle = \int_{f_0}^{\infty} S_\phi(f) df$. It is to be considered as a ratio of the total power in the 1 Hz phase modulation single sideband to the total signal power.

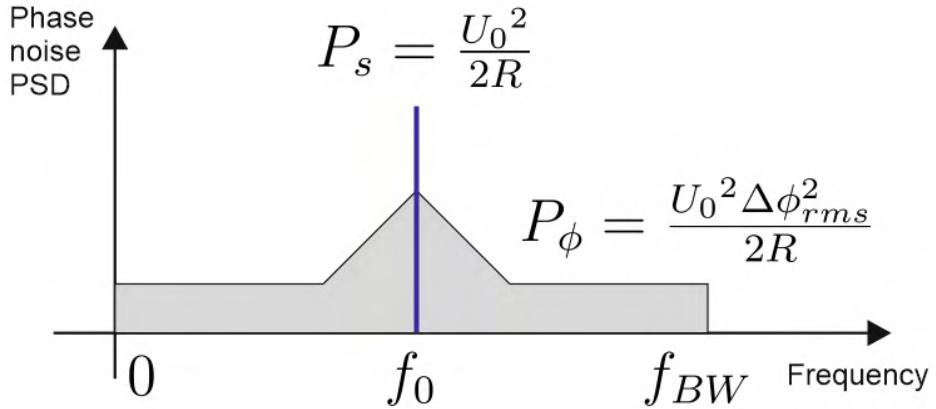


Figure 14: Harmonic signal spectrum and its sideband, caused by phase instabilities.

$$\mathcal{L}(f) \equiv \frac{S_\phi(f)}{2} \left[\frac{\text{rad}^2}{\text{Hz}} \right]_{lin}, \left[\frac{\text{dBc}}{\text{Hz}} \right]_{lin} \quad (2.25)$$

The value of phase noise is determined in relation to the carrier - its frequency and its upper-frequency sideband - using the PSD at the offset frequency. The relative value between the noise power Eq. (2.24) and signal power Eq. (2.23) may be used to represent phase noise, but also to estimate the phase jitter, which is a time-domain representation of the phase noise. According to [21, 22] the timing jitter and wander or frequency random walk are significant changes of the timing signal from its ideal position in time excluding frequency offsets and drifts. Time jitter consists of changes with Fourier frequency higher than 10 Hz, while a wander below 10 Hz. The phase jitter may be calculated using the Eq. (2.26). In general, the one sideband jitter should be calculated only as an integral of phase noise PSD in the selected frequency range, but it is more practical to calculate it in units of seconds, by further taking a square root of that integral.

$$\Delta\phi_{rms} = \sqrt{2 \int_{f_1}^{f_2} S_\phi(f) df} \quad (2.26)$$

If the reference signal and its phase noise are represented as vectors then these vectors are orthogonal and therefore (without amplitude noise vector) the RMS phase jitter is calculated using the SNR and equal to:

$$\Delta\phi_{rms} = \frac{1}{\sqrt{SNR_\phi}} \quad (2.27)$$

Adding the amplitude noise component will add the corresponding amplitude jitter to the Eq. (2.27):

$$\alpha_{rms}^2 + \Delta\phi_{rms} = \frac{1}{SNR} \quad (2.28)$$

The Eq. (2.28) is very useful for estimating the amplitude or phase jitter using the SNR, which may be used for example in ADC calculations. According to [10] and ADC with SNR of 80 dB introduces the phase jitter (which may be considered as phase detection precision) of 0.0057° or amplitude jitter of 10^{-4} .

It is of utmost importance for proper comprehension of the thesis to explicitly distinguish between phase noise and phase drifts. The easiest and most natural is to specify phase noise as short-term phase fluctuations and drift as long-term ones. A more refined division is illustrated in Fig. 15.

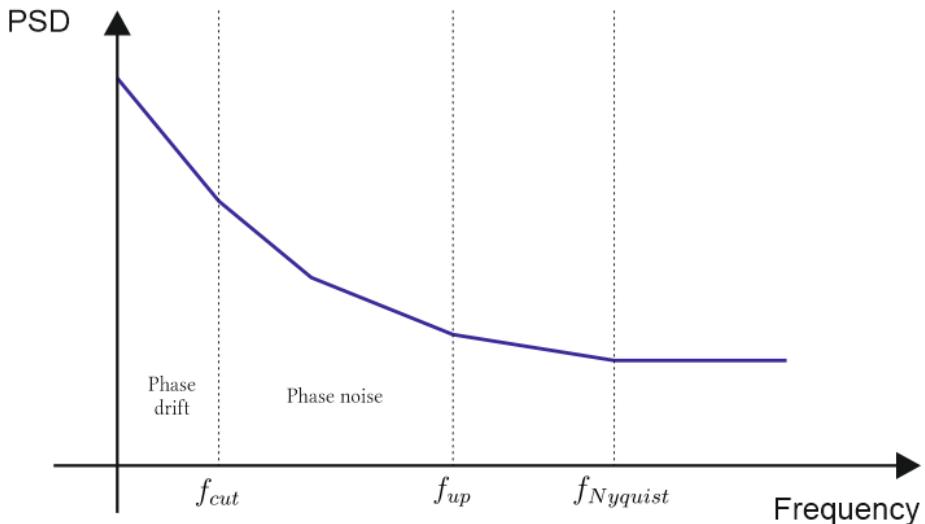


Figure 15: Phase noise and phase drift division, based on cutoff frequencies.

According to Fig. 15 all the phase fluctuations that are observed below the low cutoff frequency (for example 1 Hz) and over several hours or days are to be considered as phase drifts, which naturally describes all slow phase changes. The low cutoff frequency is not strictly defined and may be described for example as a frequency below which the cavity voltage changes may be corrected by the beam-based feedback [10]. The upper cutoff frequency (f_{up}) is described as the cavity's closed-loop bandwidth and should be selected to meet the Nyquist-Shannon theorem ($f_{up} < f_{Nyquist}$).

According to Rubiola [23] the PSD is not a proper tool to describe phase drifts, as the observation time is long and thus the carrier offset is small and PSD plot in that range steep, which leads to a problem in visual interpretation and requires a dynamic level unachievable by the currently available measurement devices.

As described in [26] phase drifts are slow changes of the electrical length of coaxial cables, which are in most cases for simplicity and ease of comparison at different frequencies expressed in units of time - picoseconds and femtoseconds. A coaxial cable of physical length l and dielectric constant ε_r has electrical length at frequency f_0 , expressed in degrees, as described in Eq. (2.29).

$$\Phi[\text{deg}] = \frac{360 \cdot l}{\lambda} = \frac{360 \cdot f_0 \cdot \sqrt{\varepsilon_r}}{c_0} \quad (2.29)$$

In order to express the electrical length in units of time a formula shown in Eq. (2.30) should be used.

In general, the drift of a selected parameter, like the phase of the reference signal, is deterministic and caused by such phenomena as component aging or the impact of environmental factors.

$$\Phi[s] = \frac{l \cdot \sqrt{\varepsilon_r}}{c_0} \quad (2.30)$$

As described by Gallo [17] the boundary limit between the phase noise and phase drift is arbitrary, but in pulsed accelerators a border may be defined according to the repetition rate of the particle bunch trains. This repetition rate (10 - 120 Hz typically) value may be considered a reasonable border between the phase noise (jitter) and phase drifts. Drifts are therefore slower than jitter and may be monitored and corrected - by compensation for example. On the contrary phase noise results in a pulse-to-pulse random scatter of the beam characteristics. It may be minimized by careful design of the Master Oscillator and proper choice of system components, but it cannot be actively corrected.

2.5.3 Phase noise of selected PRDS components

This chapter covers the topic of components' impact on the overall phase noise of the RF cascade. Each element of the system will introduce its own phase noise, therefore it is important to briefly describe the phase noise of selected popular RF components, methods of comparison, and key aspects of components' performance that require attention.

Similarly, as in the Friis formula, the main limiting component in the chain is the signal oscillator and its phase noise. A polynomial law is used to describe the phase noise PSD plots of selected oscillators and may also be used to link the Friis formula with the RF amplifier cascade total phase noise.

Every following element will increase the overall phase noise. In the modern PRDS, the most important elements in the RF reference signal chain are high-power amplifiers, frequency converters, and passive components - attenuators, filters, and directional couplers.

Phase noise of reference oscillators

The phase noise of a typical oscillator is well described by the already mentioned polynomial law and in most cases is a starting point for the further analysis of the overall phase noise of the cascades. There are other methods developed over years to describe the phase noise of oscillators, like the Leeson model, applicable in most cases, yet sometimes prone to errors in more complex applications, therefore it will not be used in the thesis.

A simple way to compare the phase performance of various oscillators is by either comparing the integrated phase jitter (obviously the lower the better) or by comparing the phase noise PSD plots directly. Sample plots for two different output frequencies are given in Fig. 16 and Fig. 17. For 162.5 MHz signals two state-of-the-art oscillators were used - a Wenzel VHF Citrine Plus series OCXO, and the SMB-100A by Rohde & Schwarz. The 1.3 GHz plots present the performance of SMB-100A, a sample linac main oscillator (new FLASH main oscillator in the case). For both frequencies plots also present a general-purpose laboratory RF generator Rigol DSG836, for contrast.

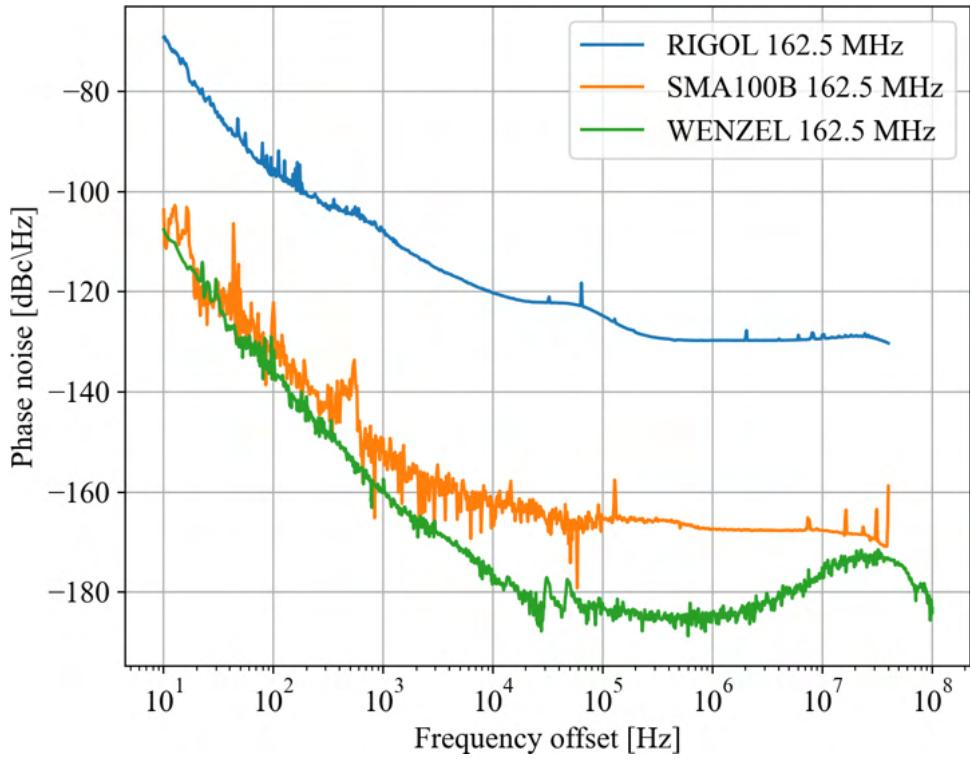


Figure 16: Phase noise PSD plots for selected oscillators at 162.5 MHz.

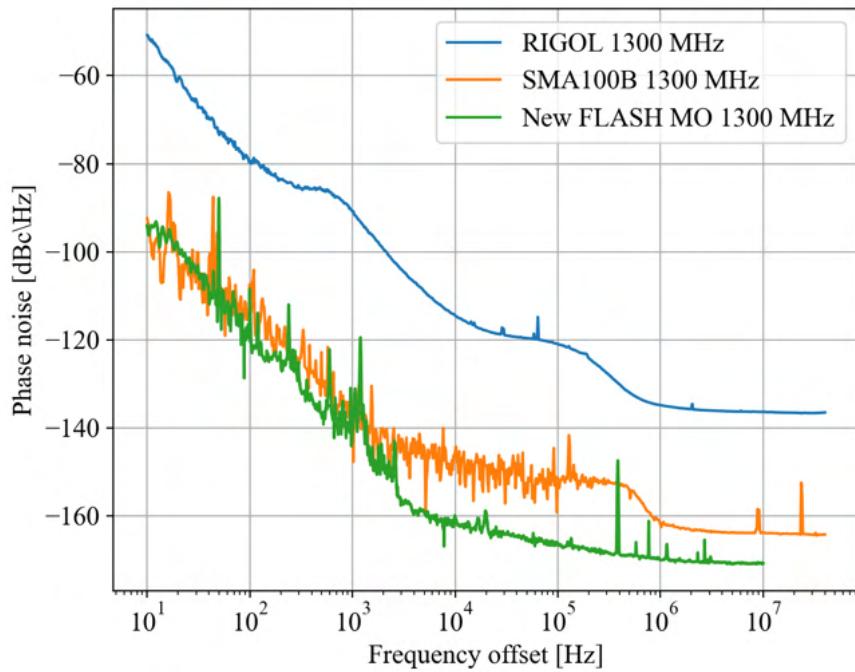


Figure 17: Phase noise PSD plots for selected oscillators at 1.3 GHz.

Presented plots may be described by the polynomial law, however, additional effects are also visible, for example, external distortions (spurious) and the frequency conversion filter shaping circuitry - in PLL modules.

Phase noise introduced by RF amplifiers and attenuators

Phase noise is one of the most important parameters of modern RF amplifiers in many applications. Therefore the analysis of their impact on the overall phase noise performance of the RF system is very important.

Czuba [18] provides a description of a simple model of a phase noise added by an amplifier, based on a research of Puglia [27]. Phase fluctuations caused by an amplifier under analysis are described by a PSD Eq. (2.31). The F_0 is the amplifier's noise factor, k is Boltzmann's constant, T is the temperature in the Kelvin scale and P_{in} is the amplifier's input power.

$$S_\phi(f) = \frac{F_0 k T}{P_{in}} \quad (2.31)$$

The Eq. (2.31) describes the dual sideband spectral density. To get a noise figure $\mathcal{L}(f)$ only one sideband should be considered.

Puglia proposed a method of estimating the total phase noise at the output of the amplifier under analysis, which may be described by a final equation (after SSB correction described by Czuba) Eq. (2.32)

$$\mathcal{L}_O(f) = \mathcal{L}_{in}(f) + \mathcal{L}(f) = \mathcal{L}_{in}(f) + \frac{1}{2} \frac{F_0 k T}{P_{in}} \quad (2.32)$$

Another approach is described by Rubiola in [28], where only white and flicker phase noise is considered, as they are responsible for short-term phase instabilities, a.k.a the phase noise. That assumption significantly simplifies the polynomial law, to the version presented in Eq. (2.33).

$$S_\phi(f) = b_0 + \frac{b_{-1}}{f} \quad (2.33)$$

The white phase noise added to a carrier of power P_0 gives the equation for random phase modulation of the PSD. This is true for amplifiers operating in linear mode, as approaching saturation may cause an increase in the noise factor. Rubiola described and proved by measurements that the white phase noise of amplifiers is inversely proportional to the input power level.

$$b_0 = \frac{FkT_0}{P_0} \quad (2.34)$$

On the contrary, the flicker noise is rather independent of the carrier input power level, which means that the b_{-1} component is constant. Therefore the Friis formula to the total white phase noise of the amplifiers cascade may be written as Eq. (2.35). The total phase noise of that cascade is a simple sum of the flicker noise of the amplifiers. Measurements proving these observations are provided by Rubiola [28].

$$b_0 = [F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots] \frac{kT_0}{P_0} \quad (2.35)$$

Passive RF components may also have an observable impact on the total phase noise of the system. For example, an attenuator placed in the signal path reduces the power of an amplifier's input signals, which leads to a white phase noise increase. Poorly placed attenuators - as the first element in the signal path - will increase the total noise factor of the path, according to the Friis formula. This will lead to the total phase noise increase, according to the Eq. (2.35). It is well known that for an impedance-matched attenuator, the noise factor is equal to the introduced attenuation.

Phase noise introduced by RF frequency converters and PLL circuits

An RF frequency converter is a circuit that alters the input RF signal frequency. The most widely used frequency converters are frequency dividers [10, 29], frequency multipliers, and phase-locked loop circuits (PLL) that may do both frequency division and multiplication, also in the fractional range [30]. In the thesis an integer N divider, multiplier, and PLL circuit will be further described.

A simplified diagram of a frequency converter is given in Fig. 18. An input signal of frequency f_{in} and phase ϕ_{in} is converted to an output signal of frequency f_{out} and phase ϕ_{out} . The frequency ratio $\frac{f_{out}}{f_{in}} = N$.

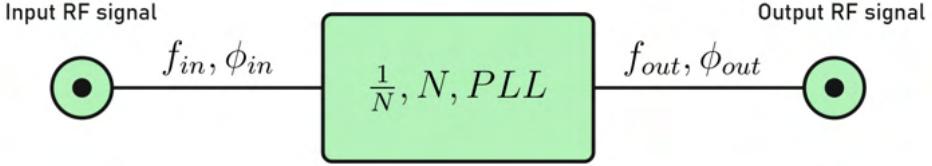


Figure 18: A block diagram of a general frequency converter.

A general theory of frequency modulation may be used to determine the introduced phase noise of the ideal frequency multipliers and dividers. A frequency multiplier in its simplest analog form is a nonlinear circuit that distorts the input signal and thus produces its harmonics, out of which one is filtered as the output signal. A frequency multiplier creates N new output signal cycles for each input signal cycle, which results in frequency multiplication, but also phase multiplication and consequently, the phase instabilities multiplication. The input signal $x(t)$, given by the Eq. (2.1) after multiplication becomes $x_n(t)$:

$$x_n(t) = u(t) = U_0 \cdot \sin(N(2\pi f_0 \cdot t + \phi_0)) = U_0 \cdot \sin(2N\pi f_0 \cdot t + N\phi_0) \quad (2.36)$$

The frequency multiplier affects not only the signal's frequency but also its phase, proportional to N^2 or $20\log_{10}(N)$.

An ideal frequency divider, regardless of its internal structure, produces one output signal cycle per N input signal cycles and thus it acts as a phase instabilities divider. This results in a decrease of the phase noise by $20\log_{10}N$. For real frequency multipliers and dividers, their additive phase noise must be also included, usually an additional few dB.

Real frequency converters are also sensitive to input signal frequency, power level, and conversion factor (division or multiplication). For frequency dividers, interesting results are described by Rutkowski [31]. He described the impact of the input signal power level and division ratio on the total divider's integrated jitter, which increases proportionally to the division ratio and is inversely proportional to the input signal power level.

Czuba [18] describes that a frequency divider may significantly limit the phase noise performance of the PLL synthesizer, due to the increase of its phase noise caused by a division factor, which will be described in the PLL part of the chapter. As an example, HMC974 frequency divider phase noise plots for different division ratios are presented in Fig. 19.

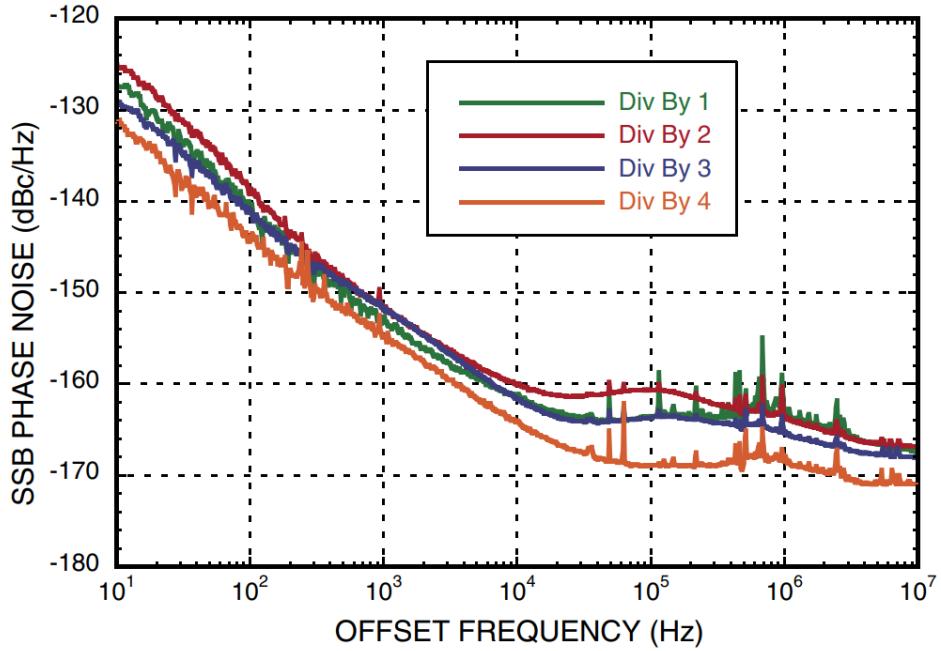


Figure 19: HMC974 frequency divider output phase noise for selected division factors, source: Analog Devices.

Another type of frequency converter is a phase-locked loop - the PLL. It may be used as a frequency converter or as a signal synthesizer, which is one of the most widely used PLL applications. More detailed information on PLL circuits can be found in [30].

A simple block diagram of an analog PLL synthesizer is shown in Fig. 20.

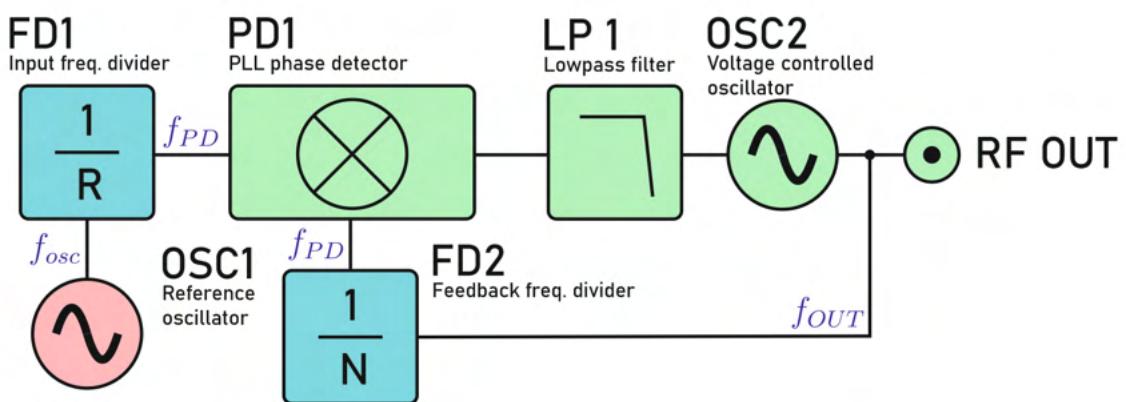


Figure 20: A simple block diagram of a PLL-based synthesizer.

The primary PLL synthesizer components are marked in Fig. 20 in red and green, blue parts are optional. The principle of operation of a PLL synthesizer is based on a phase feedback loop, established by the PD1 phase detector. The PD1 will drive its output (voltage or current, depending on a phase detector type - mixer or charge pump) in a way that ensures that the f_{pd} frequencies are always (in lock state) equal. The input oscillator is used as a reference. Its close-to-carrier phase noise should be lower than the voltage control oscillator's, as they contribute mostly to the total PLL output phase noise in that frequency range. The FD1 frequency divider is used to adjust the OSC1 frequency to fit the input of the PD1 detector - the part is optional and should be omitted if not needed. The low pass filter LP1 not only filters the PD1 output signal but also shapes the total phase noise spectrum by adjusting the loop bandwidth. The Voltage Controlled Oscillator (VCO) OSC2 should provide low phase noise far from the carrier - outside the loop bandwidth. The FD2 frequency divider is used to change the f_{out} frequency. It significantly affects the total output phase noise spectrum and should not be used in ultralow noise applications.

There are many different PLL synthesizer noise models described [18, 32, 33]. A block diagram of a linear model based on [18, 32] is shown in Fig. 21.

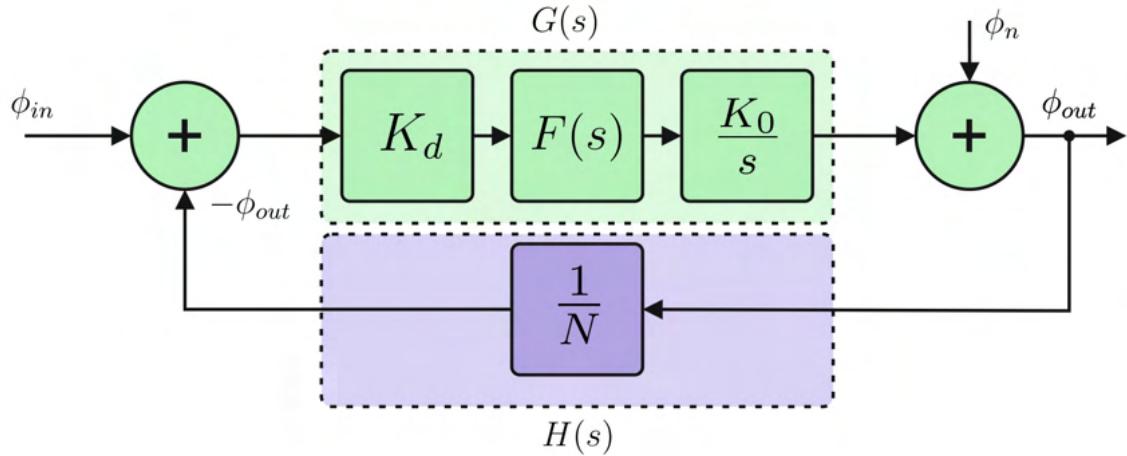


Figure 21: A linear PLL noise model.

In the model shown in Fig. 21 following noise contributions are included:

- K_d - a gain of the phase detector, equal to the ratio of output voltage change to input phase change, the unit is, therefore, $\frac{V}{radian}$.
- $F(s)$ - that is the loop filter transfer function.
- $\frac{K_0}{s}$ - VCO gain, equal to the ratio of output frequency, change to input voltage change, therefore the unit is $\frac{Hz}{V}$. The $\frac{1}{s}$ factor is added to represent the phase, not the frequency.
- ϕ_{in} - which is the phase of the PLL input oscillator signal.
- ϕ_{out} - which is the phase of the PLL output signal.
- ϕ_n - that is the phase noise of a free running VCO.

For the PLL noise model presented in Fig. 21 there are two main sources of phase noise, contributing to the total phase noise performance of the PLL synthesizer. These are the reference input phase noise and VCO phase noise contributions. For the presented PLL noise model the following total transfer function for the input phase noise may be formulated:

$$T_1(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{G(s)}{1 + G(s) \cdot H(s)} \quad (2.37)$$

The PLL synthesizer total transfer function for input phase noise $T(s)$ is made of the forward transfer function $G(s) = \frac{K_d \cdot K_0 \cdot F(s)}{s}$ and the open loop transfer function $G(s) \cdot H(s)$. The $H(s)$ is the feedback loop frequency divider division ratio $\frac{1}{N}$. The PLL synthesizer total transfer function for the input phase is a low-pass characteristic. Therefore for the input phase noise S_{ref} the output phase contribution is described by Eq. (2.38)[32]

$$S_{ref_{out}}(f) = S_{ref}(f) \cdot \left(\frac{1}{H(f)} \right)^2 \cdot \left| \frac{G(f) \cdot H(f)}{1 + G(f) \cdot H(f)} \right|^2 \quad (2.38)$$

For the VCO phase noise, a high-pass total transfer function is used (assuming that this is the only contribution to the total phase noise at the output [18]):

$$T_2(s) = \frac{\phi_{out}}{\phi_n} = \frac{1}{1 + G(s) \cdot H(s)} \quad (2.39)$$

The output phase contribution of the VCO noise is therefore [32]:

$$S_{VCO_{out}}(f) = S_{VCO}(f) \cdot \left| \frac{1}{1 + G(f) \cdot H(f)} \right|^2 \quad (2.40)$$

Other publications specify more detailed models and noise contributors [18], yet they are not within the scope of the thesis.

Under the assumption that the aforementioned PLL output phase noise contribution sources are uncorrelated, the total output phase noise is defined as in Eq. (2.41)

$$S_{\phi_{out}}(f) = S_{ref_{out}}(f) + S_{VCO_{out}}(f) \quad (2.41)$$

Taking into account the presented PLL model formulas, the following guidelines for designing ultralow phase noise PLL synthesizers may be specified:

- The input reference oscillator should have as low close to carrier phase noise as possible, as it is the main contributor to the total output phase noise of the PLL synthesizer at frequency offsets lower than the loop bandwidth.
- The voltage controlled oscillator should have as low far from carrier phase noise (noise floor level) as possible as this is the main contributor to the total output phase noise of the PLL synthesizer at frequency offsets higher than the loop bandwidth.
- The phase detector circuit should work with signals providing enough slew-rate. The higher slew rate is usually the better and this may be achieved by setting f_{pd} high and using high input power level (also for the optional frequency dividers [31]).
- The $\frac{f_{in}}{f_{out}}$ ratio should be kept as close to 1 as possible. This means that no frequency dividers are used, especially in the feedback loop.
- The synthesizer's loop bandwidth should be kept narrow [18], and selected in a way that provides the lowest integrated jitter from both input and voltage-controlled oscillators.

2.5.4 Environmental factors affecting the overall phase noise performance

Environmental factors have a significant and measurable impact on the phase noise performance of many devices, but the most widely known and described is the impact on the oscillators, especially crystal-based and dielectric resonator-based (DROs), which rely not only on electrical but also mechanical factors. Other known devices sensitive to vibrations are RF cables, filters, or capacitors.

Vibration impact on the crystal oscillator phase noise performance is often neglected in public domain papers. Vibrations and mechanical stress may arise in many design cases, like for example vibrating fans or other devices in the system, thermal gradients causing mechanical expansion of metal parts, or poorly designed (if at all in many cases) airflow within the system cabinet or module housing. In ultra-low phase noise applications and measurements in many cases the whole lab room has to be closed for other scientists, as walking around the test setup introduces mechanical vibrations observable in the measurement plots.

Crystal oscillators are tested for their sensitivity to mechanical acceleration and stress. Under mechanical condition change the oscillator frequency changes and the relative frequency shift per unit of acceleration is called g-sensitivity, measured in $\frac{ppb}{g}$, and related to the oscillator's frequency, Q-factor, and type of crystal cut. The g-sensitivity of the oscillator is a tool that converts the impact of random vibrations to the so-called Acceleration Spectral Density $ASD(f)$, measured in PSD units $\frac{g^2}{Hz}$ and then to the phase noise $\mathcal{L}(f)$. The $ASD(f)$ is defined for various mechanical components, like for example for an aircraft propeller in the US military specification MIL-STD-810G.

A very interesting test is presented in [34]. An oscillator-under-test is measured in resting position and under vibration. The oscillator's phase noise under vibration is described by the formula:

$$\mathcal{L}_{vib}(f) = \mathcal{L}_{rest}(f) + \left(\frac{\Gamma T(f) \sqrt{2ASD(f)f_0}}{2f} \right)^2 \quad (2.42)$$

where $\mathcal{L}_{rest}(f)$ is the oscillator's phase noise under no vibration, Γ is the oscillator's g-sensitivity, $ASD(f)$ is the vibration acceleration spectral density, f_0 is the oscillator's frequency, and $T(f)$ is the transmissibility of vibrations, given by:

$$T(f) = \sqrt{\frac{1 + \left(2\xi\frac{f}{f_n}\right)^2}{\left(1 - \left(\frac{f}{f_n}\right)^2 + \left(2\xi\frac{f}{f_n}\right)^2\right)}} \quad (2.43)$$

where ξ is the mechanical damping factor and f_n is the mechanical natural frequency.

An example of vibration impact on a high-quality 1.3 GHz OCXO is shown in Fig. 22. On top of the oscillator an 80 mm diameter fan was placed as a vibration source. The integrated jitter degradation in the range from 10 Hz to 1 MHz is from 53 fs under no vibration to 1534 fs with fan vibration affecting the oscillator (29 times worse). More information on vibration impact on the phase noise of signal sources, particularly crystal-based oscillators, can be found in [35, 36, 37]

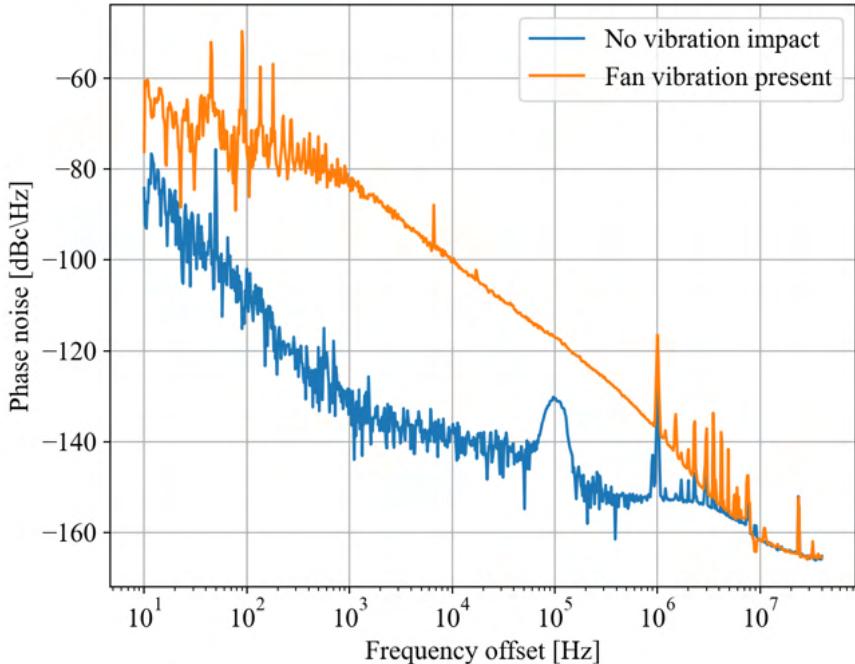


Figure 22: Phase noise PSD degradation caused by the fan vibrations at the low-phase noise crystal oscillator.

Another environmental effect, causing the frequency and phase change is aging, particularly well observed in crystal and dielectric oscillators, due to their electro-mechanical structure. The aging of an oscillator is defined as a change in its oscillation frequency over time. The literature [38, 39] defines two sources of aging and these are mass transfer and stress. Mass transfer is caused by such factors as contamination of the oscillator during

manufacturing, moisture absorption due to broken sealing, migration of plating into the crystal, or epoxy outgassing. Stress is due to package and mounting style, used epoxy and its curing process, or thermal stress during soldering or during work. According to [39, 40] some typical aging curves for crystals may be defined, as shown in Fig. 23.

If the main cause of aging is mass transfer the aging curve approaches $B(t)$. Stress aging is close to the curve $A(t)$, but in most cases, both these factors are contributing, giving the resulting curve of $C(t)$.

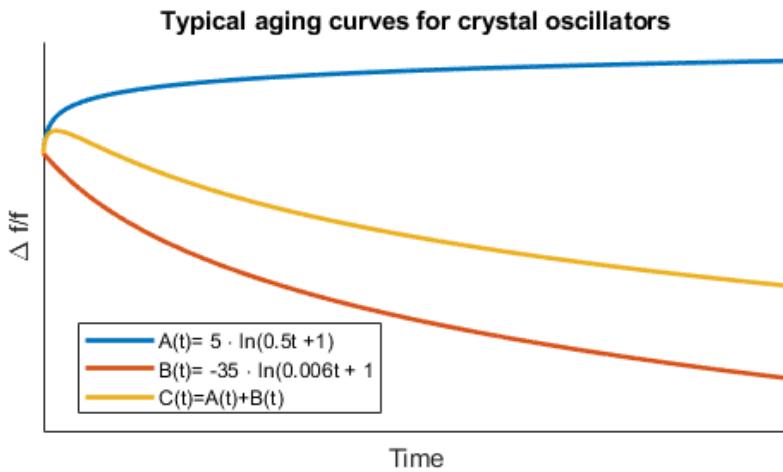


Figure 23: Typical aging curves for crystal oscillators.

2.5.5 Phase drifts in phase reference distribution systems

Phase stability along the particle accelerator is of utmost importance, due to its direct impact on the beam coherence and focus [10, 17, 18]. Therefore not only the main signal oscillator must provide a signal of ultra-low phase noise (short-term contribution to the overall system phase stability), but also the distribution media must introduce as low phase drift as possible (long-term contribution).

In phase reference distribution systems the most commonly used transmission media for reference signals are either coaxial cables or optical fibers. Both have their pros and cons that will be addressed in further parts of the chapter. A typical RF coaxial cable is capable of delivering high-power RF signals at moderate distances of several hundreds of meters. Longer cables introduce significant insertion loss that forces using power regenerating amplifiers and that introduces a significant source of additional phase noise in the

system. Coaxial cables also have a tendency to introduce a significant phase drift, when exposed to temperature change, which is not very uncommon in accelerator facilities. At longer distances and in applications not as demanding for phase noise as RF reference distribution, the optical fibers are used, usually to deliver pulsed laser signals from Master Laser Oscillator (MLO). Optical fibers are usually aligned in a star topology, as they do not introduce that much attenuation at distances of several kilometers. They are also significantly less prone to electromagnetic fields and interferences, which are not uncommon along the linac. As optical fibers are not made of several different materials they are less vulnerable to thermal expansion. When transmitting ultra-low noise laser pulses a critical factor of fiber dispersion arises - its compensation is required. Furthermore, a significant limitation of optical phase distribution is the maximum power delivered via fiber and a very high noise figure of analog RF photonic receivers [10], very often exceeding 20 dB.

A common approach is to merge both mentioned transmission media and benefit from having low phase noise (coaxial cable) and the possibility to measure and compensate for phase jitter (optical fiber). Example systems and prototypes made in that manner are described in [41, 42, 43, 44, 45, 46, 47].

The known sources of phase drift in coaxial cables are:

- Temperature change of the coaxial cable or thermal gradient that affect along the cable.
- Humid working environment that causes moisture absorption by the coax foamed dielectric.
- Mechanical stress that affects the cable.
- Dielectric aging and erosion, that are accelerated by the presence of a gamma field.

A more detailed description of phase drift in PRDS transmission media is presented in [10, 17, 26, 48, 49, 50]. In the thesis, only the phase drifts of coaxial cables and temperature phase drift effects are considered, due to the author's area of work and research. Other sources of phase drift are only addressed.

The thermal vulnerability of coaxial cable may be described using the physical property of materials, which is the thermal expansion coefficient. Physical materials tend to change their mechanical dimensions (length or volume) proportional to the change in their temperature. For a coaxial cable, a natural expansion direction is along its entire length, according to the Eq. (2.44).

$$x_1 = x_0(1 + \alpha\Delta T) \quad (2.44)$$

where x_1 is the physical length after thermal expansion, x_0 is the physical length before expansion, ΔT is the temperature change (assuming that the change is uniform along the whole cable under test), and α is the thermal expansion coefficient, unique for each material. The Eq. (2.44) is only an approximation, because most materials do not expand linearly with temperature. A typical coaxial cable is made of outer insulation, and inner dielectric (for simplicity both are assumed to be made of polytetrafluoroethylene, a.k.a PTFE or Teflon, with thermal expansion coefficient of approx. $124 \cdot \frac{10^{-6}}{T[K]}$), and outer and inner conductors, both made of copper ($\alpha_{copper} = 17 \cdot \frac{10^{-6}}{T[K]}$) or aluminum ($\alpha_{aluminum} = 23.1 \cdot \frac{10^{-6}}{T[K]}$). As the internal dielectric is not made of solid material, but rather a foamed one that may soak water the overall thermal expansion coefficient of PTFE is disturbed by the soaked water ($\alpha_{water} = 69 \cdot \frac{10^{-6}}{T[K]}$). A difference in thermal expansion coefficients leads to nonlinear temperature expansion of the whole coaxial cable. Manufacturers constantly improve their products by introducing phase-stable cable variants (with reduced thermal phase coefficient)[51, 52]. Further reduction of the introduced phase drift may be achieved by using proper compensation techniques, some of which are described in the next part of the chapter.

When analyzing coaxial RF cables the impact of the dielectric type must be also taken into account. There are several different dielectrics used in coaxial cables. Most of them are made of PTFE, some more precise (phase-stable) may be made of fluorinated ethylene propylene - FEP ($\alpha_{FEP} = 80 \cdot \frac{10^{-6}}{T[K]}$). An air coaxial line is also often used, for instance in ESS PRDS [53, 54]. The most commonly used PTFE is cheap, and easy to machine, but suffers from a so-called Teflon-knee phenomenon problem. It is observed that the thermal expansion coefficient of PTFE is abnormal and very high at temperatures from 20 to 30 degrees [55], and this is particularly inconvenient as this is the typical room temperature for accelerator devices (for instance in air-conditioned racks).

The mechanical cable length change, caused by thermal expansion, may be described using coaxial cable phase delay and phase versus temperature coefficient [26, 48, 50]. The phase delay is related to electrical phase length and is the time t_p required for a signal to pass through the cable, according to Eq. (2.45). The temperature vs. phase coefficient describes the phase change Δ_{phi} introduced by the cable per unit length per degree of temperature change, as shown in Eq. (2.46).

$$t_p = \frac{l[m]\sqrt{\varepsilon_r}}{c_0} \quad (2.45)$$

where c_0 is the speed of light in vacuum, ε_r is the relative dielectric constant of the cable dielectric material, and $l[m]$ is the cable length, in meters.

$$\Delta_{phi} = \phi_t \cdot l[m] \cdot \Delta T \quad (2.46)$$

where ϕ_t is the temperature phase coefficient, $l[m]$ is the mechanical length of the cable, given in meters, and ΔT is the temperature change in degrees Celsius or Kelvin.

A sample plot, showing the temperature impact on the cable phase change over several days of observation is shown in Fig. 24. 10 meters of Andrews RFA $\frac{7}{8}''$ test cable was placed in a altering temperature climatic chamber and the phase change across the cable was measured using AD8302 based phase detector module, placed in a second climatic chamber and kept in constant temperature. Measurement cables (marked in blue color) were chosen as short, as possible, of the same length and type, both from the same batch of phase stable SRF .141 cables, as shown in Fig. 25. The presented sample RF cable measurement shows the need for phase compensation as any temperature change will introduce a phase shift in a coaxial-based PRDS. Another assumption may be stated, based on the measurement - two cables of the same type, same length, same connectors, and coming from the same batch (and even spool) should introduce in the same ambient conditions similar (or perfectly equal) phase drifts. Thus in some systems [54] this fact may be used to compensate for some selected coaxial cables phase drifts.

Measurement of phase drifts introduced by other PRDS components (couplers, attenuators, splitters, amplifiers) is very demanding, due to the small size of these components. In many cases, their impact is smaller than the detection boundary of the phase detectors used. An attempt at such measurements was made by Sikora [49], yet the results are purely measurement results of some specific parts and not the general behavioral models.

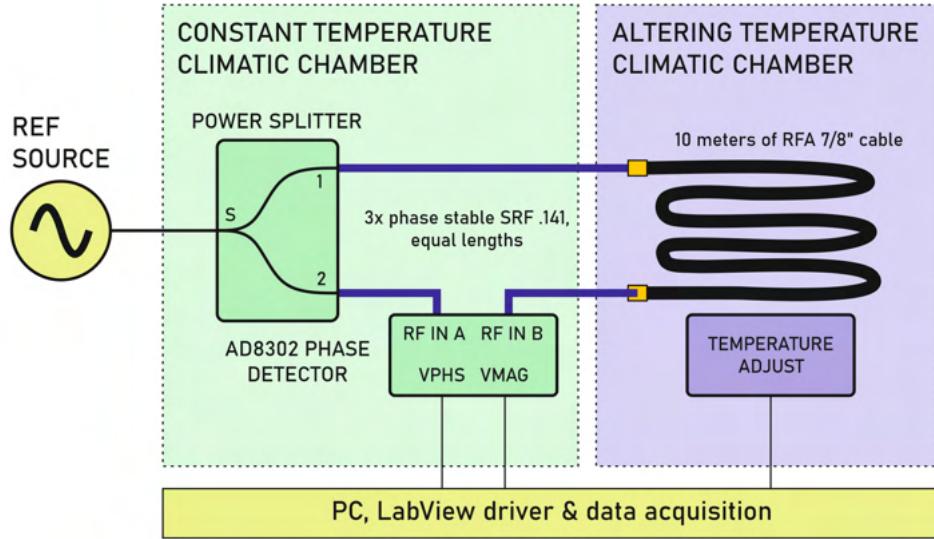


Figure 24: Test setup for coaxial cable phase drift measurement.

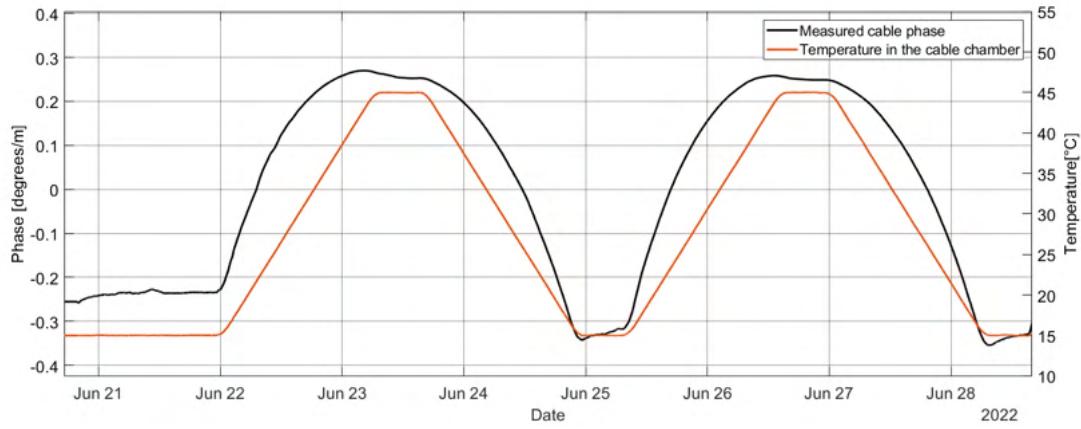


Figure 25: Typical coaxial cable phase drift, caused by temperature change, an example of RFA78 cable.

2.5.6 Phase instabilities influence on LLRF system and beam parameters

The analysis of the impact of phase instabilities introduced by the PRDS to the LLRF and electron beam must be divided into three parts - the MO phase noise contribution, RF distribution phase drift, and RF station noise [10]. In FEL accelerators the stability of the beam arrival time and bunch time duration depends critically on the timing system and thus the phase instabilities of the RF reference. The Self-Amplified Spontaneous

Emission (SASE) intensity depends on the jitter of the bunch time arrival. The Master Oscillator, as a source of the RF reference signal for all RF stations will be a limiting source of phase instabilities affecting the bunch time relations and RF control field phase.

The development of a complete model of phase instabilities' influence on the beam performance is a very demanding and complex task. A full analysis of the noise origins, and what are their impact on the beam and RF field must be performed to specify the RF system requirements. To the author's knowledge the most important publications in the field are [10, 56, 57]. All of them provide a simplified model for the phase instabilities impact analysis.

Geng provides a simple scheme to model the MO phase noise effects on the beam phase. The scheme is shown in Fig. 26.

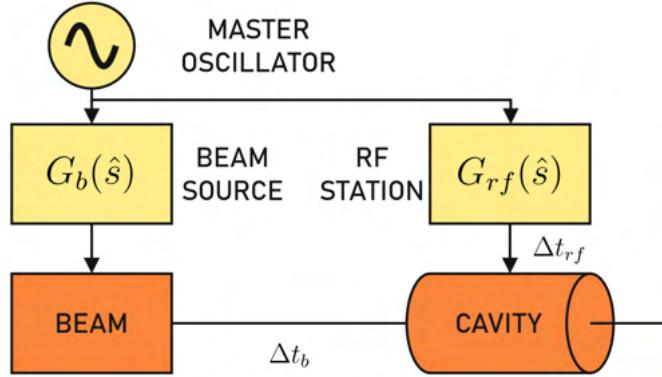


Figure 26: A simple model to determine the MO phase noise impact on the linac beam.

In Geng's model in Fig. 26 MO phase noise $\Delta_{\phi_{MO}}$ is analyzed. It passes through two transfer functions, G_b and G_{rf} , modeling the jitter impact on the beam current and the RF field phase ($\Delta_{\phi_{beam}}$ and $\Delta_{\phi_{rf}}$). RF field drives the beam in a cavity in a finite time - Δt_b models the delay of the phase noise reaching the cavity and is related to the bunch arrival time. The Δt_{rf} component is for the MO phase noise delay in reaching the RF control field voltage. The transfer functions are given in Eq. (2.47), and Eq. (2.48)

$$G_b(\hat{s}) = \frac{\omega_b}{\hat{s} + \omega_b} \exp(-\hat{s}\Delta t_b) \quad (2.47)$$

$$G_{rf}(\hat{s}) = \frac{\omega_B}{\hat{s} + \omega_B} \exp(-\hat{s}\Delta t_{rf}) \quad (2.48)$$

where ω_b and ω_B are the bandwidths of the beam source and the RF station in which they lock to the MO. The beam phase variation may be then calculated as shown in Eq. (2.49):

$$\Delta_{\phi_b} = \Delta_{\phi_{rf}} - \Delta_{\phi_{beam}} = (G_{rf} - G_b) \cdot \Delta_{\phi_{MO}} \quad (2.49)$$

Geng provides an example of SwissFEL analysis. The requirements for the SwissFEL are listed in Table 1. The calculations provided give final requirements for the MO phase noise at selected frequency operating bands, as shown in Table 2.

Table 1: Selected requirements for SwissFEL subsystems [10]

Noise contribution	Notation	Tolerance
S-band amplitude	α_{SB}	1e-4
S-band phase	$\Delta_{\phi_{SB}}$	0.015°
X-band amplitude	α_{XB}	2e-4
X-band phase	$\Delta_{\phi_{XB}}$	0.05°
C-band amplitude	α_{CB}	1e-4
C-band phase	$\Delta_{\phi_{CB}}$	0.03°

Table 2: Calculated MO phase noise requirements for SwissFEL [10]

	S band	C band	X band
Closed-loop bandwidth (f_u [kHz])	480	1350	4220
Maximum MO phase noise ($S_{\phi MOres}$, [$\frac{dB}{rad^2 Hz}$])	-139.3	-137.8	-138.3

Another important contribution is described by Ludwig [57], where an impact of the LLRF control system components and the MO signal and their phase instabilities to the beam jitter is analyzed. A PLL-based model of the LLRF system is applied and transfer functions are calculated for all important phase noise contributors. The system diagram is shown in Fig. 27. The described cavity field phase dependence of each subsystem is given as in Eq. (2.50)

$$\phi_{CAV}(s) = K_{MO}(s)\phi_{MO}(s) + K_{DWC}(s)\phi_{DWC}(s) + K_{MOD}(s)\phi_{MOD}(s) \quad (2.50)$$

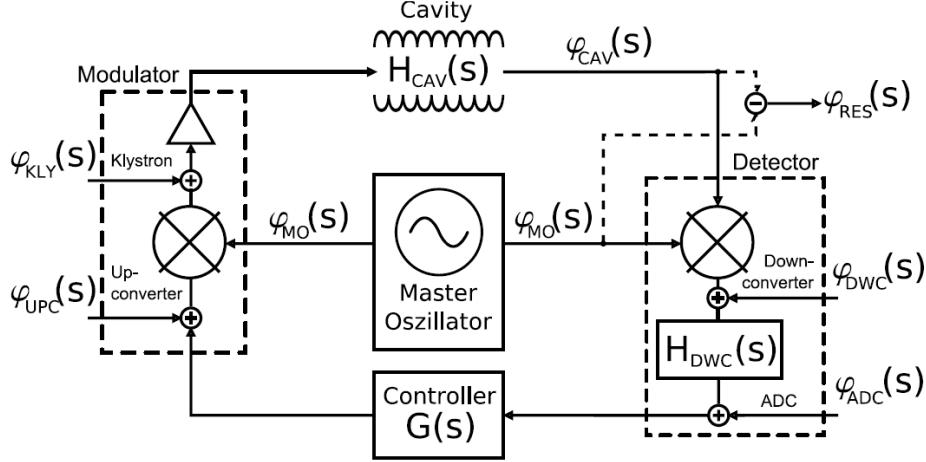


Figure 27: Simplified schematic diagram of a single cavity LLRF system at FLASH. [57]

where transfer functions for each subsystem are defined as in Eq. (2.51), Eq. (2.52), and Eq. (2.53):

$$K_{MO}(s) = H_{CAV}(s) \frac{1 + G(s)H_{DWC}(s)}{1 + H_{CAV}(s)G(s)H_{DWC}(s)} \quad (2.51)$$

$$K_{DWC}(s) = \frac{H_{CAV}(s)G(s)H_{DWC}(s)}{1 + H_{CAV}(s)G(s)H_{DWC}(s)} \quad (2.52)$$

$$K_{MO}(s) = \frac{H_{CAV}(s)}{1 + H_{CAV}(s)G(s)H_{DWC}(s)} \quad (2.53)$$

The residual phase noise between the cavity output and the MO is given in the Eq. (2.54) (assuming the loop bandwidth $\omega'_{12} = g_0\omega_{12}$):

$$S_{\phi,RES}(f) = \left| \frac{s}{s + \omega'_{12}} \right|^2 S_{\phi,MO}(f) + \left| \frac{\omega'_{12}}{s + \omega'_{12}} \right|^2 \left[S_{\phi,DWC}(f) + \frac{1}{g_0^2} S_{\phi,MOD}(f) \right] \quad (2.54)$$

Controller gain g_0 is assumed as constant, ω'_{12} is the control loop bandwidth and ω_{12} is the cavity cut-off frequency. The MO jitter is suppressed by the LLRF control system within the loop bandwidth and the phase noise of the downconverter and the modulator are suppressed outside the loop bandwidth [18, 57].

2.6 Phase and power detection, basic parameters of detectors

RF power and phase detectors (or in general RF detectors, as in modern applications these are often merged together as ADC-based detectors) are used to extract input RF signals parameters (power magnitude or phase difference) and convert them to baseband voltages, currents, or other forms, ready for further signal processing. Therefore an RF detector output is considered as a complex envelope (baseband signal) of the input RF signal [10]. Classic applications utilize analog phase and power detectors, while modern ones tend to use digital solutions. Both have their pros and cons and will be described in this chapter. Due to the scope of the work, only the phase detectors are described.

In modern particle accelerators, their PRDS'es and LLRF systems phase detectors are expected to measure the phase difference between two RF signals as accurately as possible, usually over long periods of time [58]. Therefore their key parameters must be addressed.

A phase detector may be modeled using the following parameters [10]:

- Bandwidth - describes the maximum speed of phase changes that can be detected.
- Accuracy - is used to determine the steady-state error of the detector and is related to the sensing threshold.
- Sensing threshold - it is the minimum phase change that may be detected.
- Linearity - determines the RF detection error, depending on the value of the measured phase difference. It is particularly important in analog phase detectors, as most of them are not able to cover the full 2π phase range.
- SNR - defines the amount of noise introduced at the output by the detector itself.
- Latency - it contributes to the loop delay, when used as for example in PLL circuits.
- Dynamic range - defines the observable phase difference range. For analog phase detectors the dynamic range is usually significantly lower than 2π , while digital phase detectors may cover the full phase detection range of 2π .

- Detector's self drift - describes how the output signal of the detector drifts over time, and environmental factors, mostly temperature change. It introduces an error of phase drift detection and must be known precisely (and compensated if possible) in PRDS applications.
- Slope direction and angle - defines the ratio of the output signal change to input phase difference change. It is particularly important in mixer-based and analog phase detectors.

The simplest solutions to the phase detection problem are analog-based phase detectors, made of RF mixers - either using a single double-balanced mixer, or an analog I/Q demodulator circuit, as shown in Fig. 28.

An RF mixer is a three-port device that utilizes a nonlinear element to perform input signal mixing. A typical double-balanced mixer, made of two baluns and a diode bridge. When fed with input signals $x_{RF}(t) = U_{RF} \sin(2\pi f_{RF} t + \phi_{RF})$, $x_{LO}(t) = U_{LO} \cdot \sin(2\pi f_{LO} t + \phi_{LO})$ the output signal of a mixer is given by a Eq. (2.55):

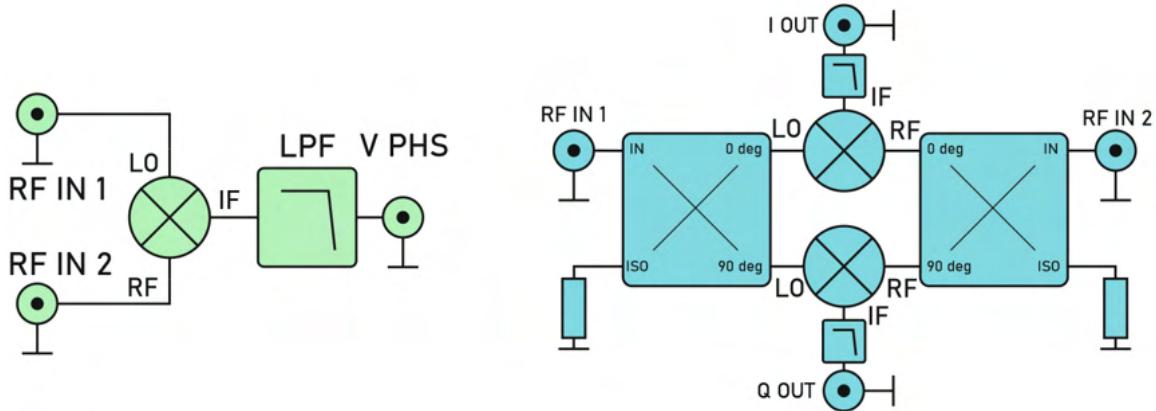


Figure 28: Mixers used in analog phase detector circuits.

$$x_{IF}(t) = x_{RF}(t) \cdot x_{LO}(t) = \frac{U_{RF}U_{LO}}{2} \underbrace{\cos[2\pi(f_{RF} - f_{LO})t + (\phi_{RF} - \phi_{LO})]}_{lower\ sideband} - \frac{U_{RF}U_{LO}}{2} \underbrace{\cos[2\pi(f_{RF} + f_{LO})t + (\phi_{RF} + \phi_{LO})]}_{upper\ sideband} \quad (2.55)$$

When mixer works as a phase detector, usually $f_{RF} = f_{LO}$ and the Eq. (2.55) is simplified to Eq. (2.56)

$$x_{IF}(t) = \frac{U_{RF}U_{LO}}{2} \sin\phi \approx \frac{U_{RF}U_{LO}}{2} |_{for \phi \ll 1 \text{ rad}} \quad (2.56)$$

For the analog I/Q demodulator, the phase difference between input signals may be obtained using the Eq. (2.57). Unlike a single mixer, an analog I/Q demodulator is able to cover the whole 2π phase range. It is however more complicated and thus prone to error, mostly from mixer LO leakage, 3 dB hybrid couplers asymmetry, and lack of balance.

$$\phi = \arctan \left(\frac{I(t)}{Q(t)} \right) \quad (2.57)$$

Another type of analog-based phase detector is an integrated circuit from the Analog Devices company - the AD8302. Its internal structure and output voltage related to the phase change plot are shown in Fig. 29. According to the datasheet [59] it is a fully integrated system for measuring gain/loss and phase in various applications. The high linearity and dynamic range (both phase and power at the input) are achieved by introducing the input logarithmic amplifiers. As both input channel amplifiers are made within the same chip, their thermal drifts are almost the same and mostly compensate for each other. The phase detection curve is similar, yet more linear, to the typical mixer phase detector curve, therefore for proper operation, it requires a proper operating point selection. The AD8302 will be further described in Chapter 4, where all its limitations are described.

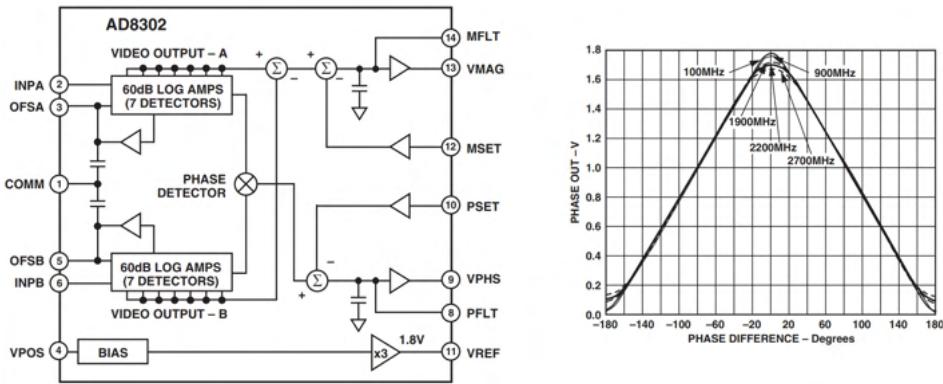


Figure 29: AD8302 internal block diagram and output phase voltage characteristic. Image source: Analog Devices.

A simple analog-based phase detector may be also made of power splitters, like Wilkinson type or resistive. The author has developed two test structures of such phase detectors, based on vector summing of input signals, thus the further used in the thesis name - the vector-phase detectors. A basic structure of such a phase detector is shown in Fig. 30 and a more detailed description is given in Appendices.

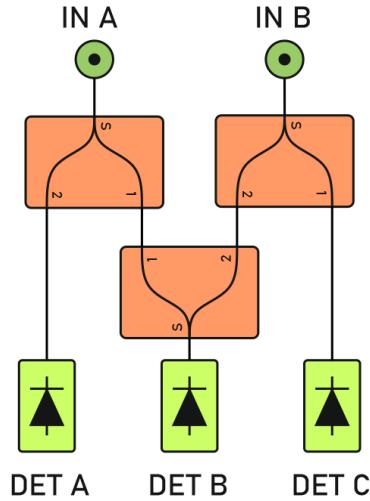


Figure 30: A block diagram of a power splitter-based vector sum phase detector.

Another type of analog based phase detectors are six-ports. The six-port-based detection technique is mature and becomes more and more popular in modern applications, mostly due to its simplicity and small cost. More detailed information on six-ports may be found in the following publications [60, 61, 62, 63, 64, 65, 66, 67]. A basic block diagram of a six-port structure is shown in Fig. 31. The principle of operation is based on a phase-controlled sum of input signals and phase shift them by $\frac{n\pi}{2}$, $n = 1, 2, 3, \dots$ [63].

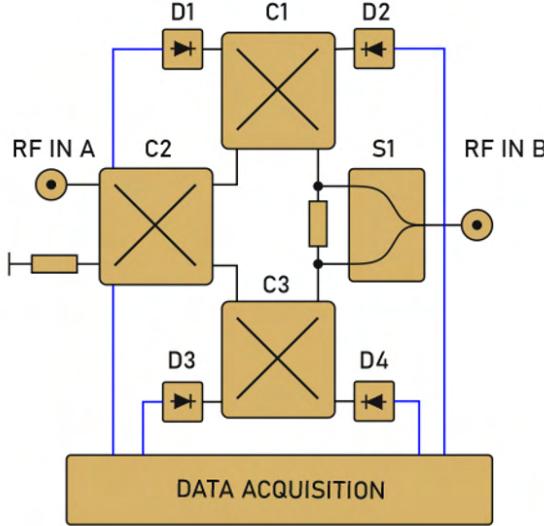


Figure 31: A block diagram of a six-port structure ??.

A six-port may be used as a phase detector [63]. Input signals are phase shifted by $\frac{n\pi}{2}$, $n = 1, 2, 3, \dots$ and then downconverted do DC baseband, using power detectors, giving information about vector B_3 to B_6 lengths (power levels), as shown in Fig. 32. Then the phase difference between P_1 and P_2 is obtained by using Eq. (2.58):

$$\Delta\phi = \arctan\left(\frac{B_3 - B_4}{B_5 - B_6}\right) \quad (2.58)$$

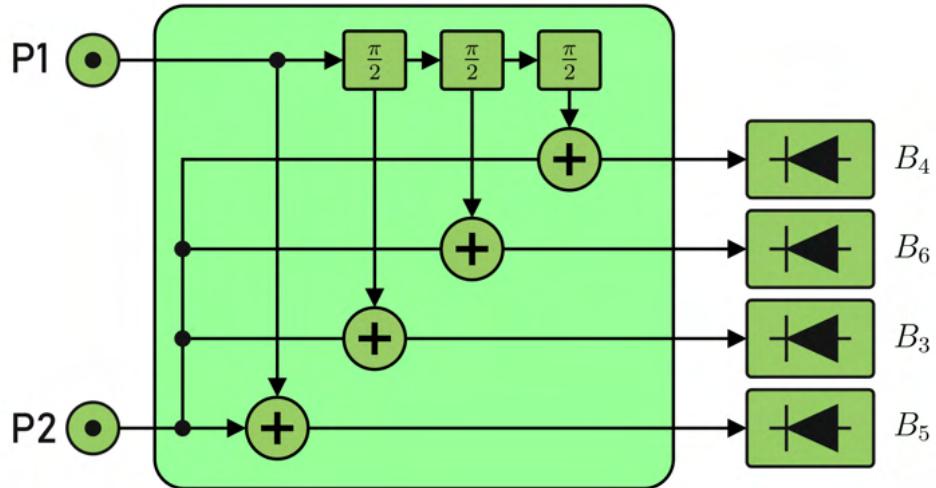


Figure 32: A phase detector application of a sixport [63].

Digital RF methods of phase detection are:

- downconversion and ADC sampling at lower sampling rates,
- direct sampling of RF signals.

In the thesis digital phase detection of digital signals, using, for example, XOR gates is not described, nor analyzed, as it is not within the scope of the work.

Downconverter based phase detector is mixing the RF signal to be measured with an LO signal that has a frequency offset to the RF signal, selected carefully to match the ADC clock signal. The general architecture is presented by Geng [10]. Another way of phase detection based on downconversion is proposed by the author in Fig. 33. Input signals are mixed with a local oscillator - a PLL chip used to synthesize the LO and CLK signals, and a clock signal is obtained by dividing the PLL output frequency. If the LO frequency is set slightly below the input RF frequency, then both RF and IF phases rotate in the same direction and the detection slope is positive [10]. IF outputs of downconversion mixers are filtered and sampled by ADC channels. Since the measured value is the phase difference, the LO phase jitter is a common mode signal and is compensated. The downconversion makes it possible to use the lower sampling frequency ADC and thus reduce the impact of their aperture and clock jitter.

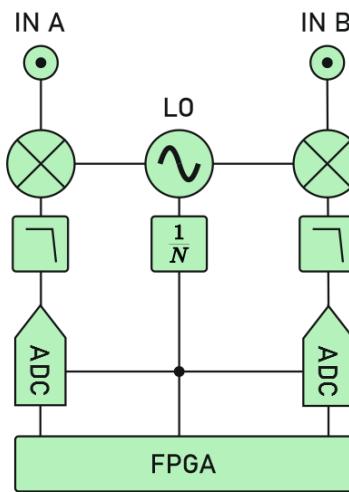


Figure 33: An example of a digital phase detector, based on downconverting principle.

Direct sampling utilizes a fast sampling ADC, where clock jitter and aperture jitter become a significant limitation of phase detection sensing threshold [68]. Typical values of aperture jitter of 40 - 100 fs limit the usage of direct sampling solutions in plasma-based accelerators, where the phase detection requirement is greater than 10 fs. The phase detection error related to the clock jitter is given by $\Delta\phi_{err} = 2\pi f_{RF}\Delta t_{CLK}$. An important issue is also the ADC's SNR. Geng defines the relationship of the amplitude and phase jitter and the SNR of the ADCs as in Eq. (2.59) [10]:

$$\alpha^2_{rms} + \Delta\phi^2_{rms} = \frac{1}{SNR} \quad (2.59)$$

An ADC with SNR of 80 dB (typical ADC with higher input frequency bandwidths have SNR of 60-70 dB) limits the maximum achievable phase measurement resolution to $\Delta\phi^2_{rms} = 0.0057^\circ$, under the assumption that only the phase noise is present. In direct sampling clock frequency is in most cases selected to be lower than the input RF frequency and the frequencies ratio should be selected according to the algorithms used after the sampling.

The following publications describe the topic of RF phase detectors used in PRDS'es and linac RF control systems in a more detailed manner [58, 69, 70, 71, 72, 73, 74, 75].

2.7 RF transmission line phase drift compensation methods

In this part, the methods of phase drift introduced by a coaxial cable, used as a transmission line in a PRDS are described. The need for phase drift compensation is rather obvious - a typical coaxial cable of 10 meters in length at $\Delta T = 1^\circ C$ will introduce several hundreds of femtoseconds of phase drift, which is unacceptable when beam jitter requirement is for example less than 10 fs. The distribution line phase drifts need to be therefore measured and controlled and there are several methods that may be used to compensate for the drifts. This part will not describe in detail the applications of the presented methods but rather show general concepts that are used. The methods used in selected PRDS will be described in the next part of the thesis.

Passive compensation is a group of methods that do not adjust phase components to compensate for the phase drifts. Instead, these methods are foreseen to reduce the impact of the drift-causing effects, mostly temperature change of the coaxial cable used in the distribution system. Phase-stable coaxial cables are often used for shorter connections. In many applications, [53, 54, 76, 77] routed cables are either wrapped with a heating band and insulated for thermal stabilization (Fig. 34) or used in pairs, cut to lengths, to use the fact that same type of cables of the same length should introduce similar (but not always perfectly equal) drift. A temperature distribution across the coaxial cable with the heating band and thermal insulation is presented in Fig. 35[77].

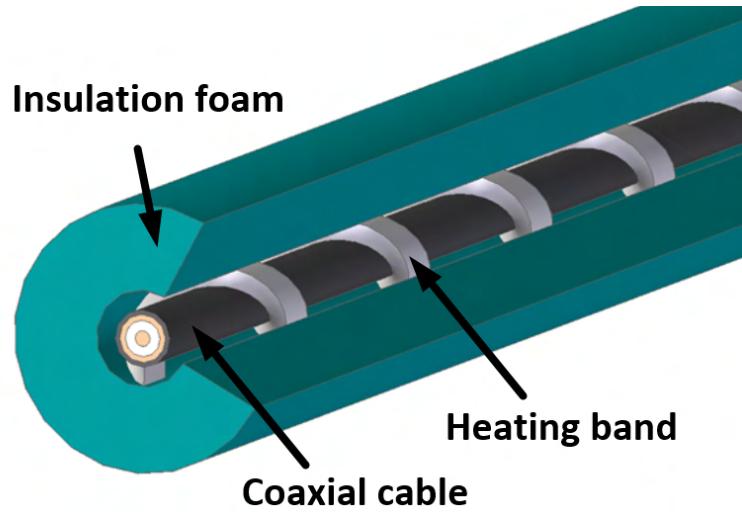


Figure 34: A passive stabilization of coaxial cable phase drifts with temperature stabilization [77].

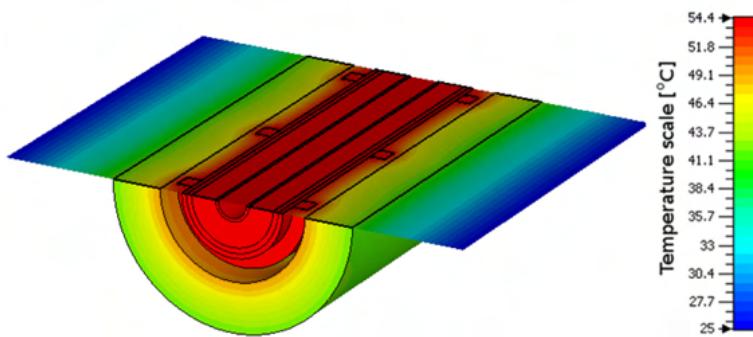


Figure 35: Temperature distribution across the coaxial cable with the temperature stabilization system [77].

Active phase drift compensation methods are based on actuators. These are usually phase shifters, PLL circuits, or vector modulators. Active compensation schemes are designed in many ways, but two will be further described: reflectometric and interferometric. Both methods use the effect of reflected signal propagating through the same RF cable as the forward signal. The result is that the reflected wave encounters the same phase drift but in opposite direction. A phase detector is then used to drive the phase shifter.

An example of such a system is presented by Geng [10] and may be used for both coaxial cables and optical fibers. The drawback of a reflectometer-based active compensation is its point-to-point character. In applications requiring several PRDS receivers in one phase stabilization loop a more convenient approach is based on interferometric stabilization [77, 78, 79]. Interferometric phase stabilization is based on two modules - transmitter and receiver - which are used to create interferometric phase stabilization loops. When properly calibrated such an approach gives a phase drift compensation, described using a phase drift suppression factor, e.g. of more than 100x. Receiver modules are realized in an analog or digital way, depending on the type of phase detection scheme used. A more detailed description of the interferometric active phase stabilization method is given in a further part of the thesis, devoted to the the 162.5 MHz link prototype and XFEL PRDS description.

Alternatively to the classical RF PRDS, optical-based RF solutions are developed [10, 42, 43, 45, 46] in many accelerator facilities. An optical-based pulse laser synchronization is able to deliver ultra-low phase drift, significantly less than 10 fs, at a cost of high close to carrier noise and usually high price. Using laser pulsed optical signal makes it possible to use nonlinear optical methods to measure phase difference and the timing changes in the beam [46]. In such RF-optical synchronization systems, a key role is the Master Laser Oscillator, which is precisely synchronized with the RF Master Oscillator. The laser pulses generated by the MLO are distributed to all the laser receiver modules to serve as a reference for measuring phase drifts of the system. Phase detection is based on Laser-to-RF solution [45, 42, 43], using an integrated Mach-Zehnder modulator. Only such systems allow crossing the boundary of the 10-20 fs phase drift detection sensitivity threshold, which is common for conventional RF-based phase detectors and systems. Examples of such RF-optical PRDS systems are in FLASH and E-XFEL, a prototype system that is currently under development in ESS, based on [41].

Another set of methods may be used to compensate for phase drifts of coaxial pickup cables between cavities and LLRF driving stations. The methods are well described and concluded by Ludwig [80] and are based on:

- reduction of pickup cables length, to reduce the introduced phase drift (calculated per unit length),
- reduction of the number of pickup cables, for example by placing RF field detectors directly at the cavities,
- reference tracking principle, helping to reduce the correlated amplitude and phase noise sources, related to the RF field detectors,
- reference injection, providing an extra calibration phase for the field detector chain,
- adaptive feedforward method, used for iteratively compensating all deterministic sources of drifts.

3. Accelerator research facilities and their phase reference distribution systems

The chapter covers the description of the selected world's accelerator facilities, their phase reference distribution systems, and their submodules. Despite the significant number of such facilities it was decided to cover only selected facilities, important for the topic of the thesis, and the facilities that the author has co-operated with, during several international research projects conducted at the Institute of Electronic Systems. Selected facilities are illustrated in Fig. 36. In the author's opinion, it is also important to mention the facilities located in Poland, like SOLARIS National Synchrotron Radiation Center in Krakow, and PolFEL (currently under construction) in National Center for Nuclear Research in Świerk. The most important FEL facilities in the world are European-XFEL in Germany, LCLS and LCLS-II in the USA, SwissFEL in Switzerland, and Pal-XFEL in South Korea.

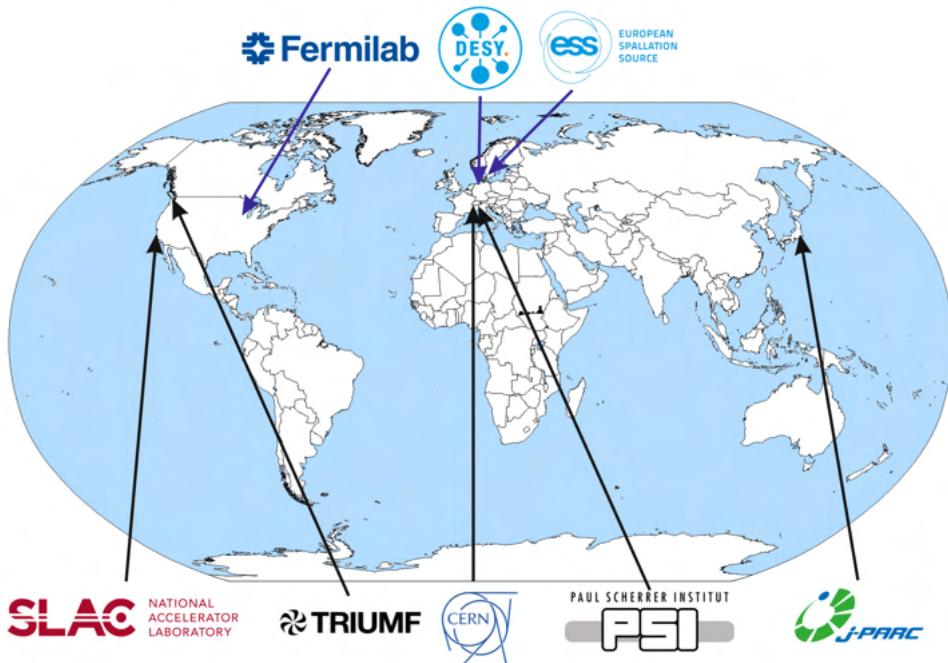


Figure 36: Selected accelerator facilities worldwide.

3.1 DESY accelerator experiments

DESY - Deutsches Elektronen-Synchrotron - is a German research facility, located in Hamburg, and focused since its beginning in the 1960s on particle accelerators. The name of the facility originated from the first accelerator launched in the facility in the 1960s. Nowadays there are several accelerator systems developed and maintained in the facility, like circular (PETRA-III and planned upgrade to PETRA-IV) and linacs, like Freie-eLektronen LASer in Hamburg FLASH and European X-ray Free Electron Laser E-XFEL.

The Institute of Electronic Systems cooperates with DESY for more than 20 years. During that time a significant number of research projects and grants have been realized, and BSc, MSc, and Ph.D. theses were written about these projects. The author contributes to the cooperation between ISE and DESY since 2014 and since then developed many devices and modules for the FLASH and E-XFEL. The most significant contributions are described in further parts of the thesis.

3.1.1 FLASH

The first attempts to create a facility, further known as FLASH, started in 1991 when the first meetings and reports on a standard of superconducting cavities were made - the TESLA technology [9]. At the same time in SLAC research on new sources of coherent X-ray radiation was conducted. In 1994 it was decided to use TESLA technology to create new ultra-bright light sources, to be further used in new FELs. The research was done within the TTF program, which resulted in the first beam of 80 MeV energy in 1997. In 2005 a facility made for the TTF program was officially opened for external experiments and its name changed to FLASH - the Free Electron Laser in Hamburg.

FLASH is a linear electron accelerator feeding an FEL, which creates a coherent light beam in VUV and soft X-ray regimes [81]. In 2007 [12] the wavelength of the light beam reached the water window, enabling more sophisticated biological experiments. Nowadays FLASH is able to deliver up to 8000 light pulses per second [82] for various experiments in the fields of atomic, molecular, and optical physics, chemistry, nanoscience, and further FEL development - in the end FLASH was also foreseen as a test facility before launching a significantly bigger machine - the European XFEL. The linac part of the accelerator is

approx. 120 meters long and the entire facility, including undulators and experimental halls, is 315 meters long. Along the entire linac, and before the undulators there are RF stations, each hosting an LLRF node that controls the selected part of the accelerator or FEL. In total there are more than XX RF stations and other PRDS receivers, and each one requires an RF reference signal or selected frequency, delivered from the Main Oscillator, with as small amplitude and phase distortions as possible. In total the FLASH2020+ PRDS delivers 26 RF channels at 1300 MHz, 10 channels at 108 MHz, and 4 channels at 1517 MHz, with phase jitter of 10 fs, which is one of the best results, so far achieved in DESY. As described in [18], the short-term (1 second) phase deviation should be less than 10 fs, and long-term (1 minute) less than 300 fs, which is due to the designed pulse duration of the beam in range from 10 to 70 fs.

The electron beam is generated by the first element in the FLASH block diagram, shown in Fig. 37 - the RF gun. It feeds the cryomodules and their superconducting cavities, in order to increase the electron beam energy. Each cryomodule is made of 8 cavities, tuned to 1.3 GHz frequency [18]. All the cryomodules are monitored and driven by LLRF system nodes, as described in Chapter 2 and [10]. Synchronization is based on an ultra-stable RF reference signal from the MO. Along the cryomodule path, there are bunch compressor modules that further reduce the spatial distribution of the bunches, which leads to a possibility of X-ray radiation generation in the undulators. At the end of the cryomodules path, there is a collimator reducing the destructive halo effect, which may damage the undulator magnets [9]. Initially, there was only one undulator path after the cryomodule. In 2016 a second undulator line was added, enabling the independent realization of two experiments at the same time [12, 82].

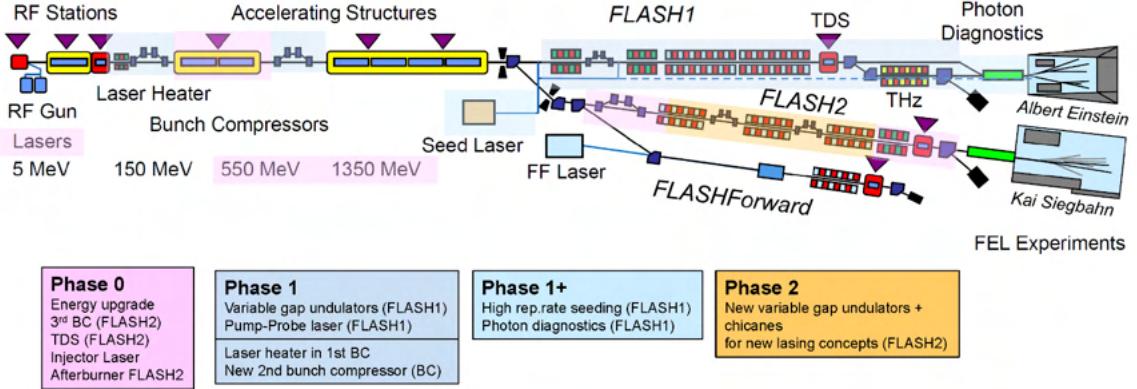


Figure 37: FLASH accelerator block diagram, including upgrades in FLASH2020+ program. Image source: DESY.

FLASH facility was constantly upgraded, in order to maintain operational ability and compete with other soft X-ray FEL facilities. The list of upgrades is presented in [81, 83, 84].

In 2017 a decision was made to further upgrade the existing FLASH facility. FLASH2020+ project covered some major upgrades, like [81]:

- Replacing the fixed gap undulators in FLASH1 line with variable gap undulators for enabling wavelength tuning, variable polarization of photon pulses, and novel lasing schemes. This also gives the ability of fully parallel work of both FLASH1 and FLASH2 lines and increases the available time for user experiments by 40%, due to tuning time reduction.
- Application of external seeding for achieving fully coherent FEL pulses and thus the ability to control both the temporal shape and phase of the pulses. One of the lines will be fully externally seeded at the full repetition rate of FLASH in burst time.
- An increase of accelerator Energy from 1.25 GeV to 1.35 GeV, caused by upgrading two of the old accelerator cavities. With the upgrade FLASH will still be complementary to E-XFEL.
- Providing the ability to generate pulses in an attosecond regime, which leads to synchronization and timing upgrade, done in cooperation with the Institute of Electronic Systems, and described as a part of the thesis.

3.1.2 European XFEL

As described in [85] the main components of the facility are the injector, linear accelerator, beam distribution system, undulators, photon beamlines, and finally the experimental stations. These components are disposed of along a 3.4 km-long tunnel, approx. 15 to 35 meters underground, depending on the location. The XFEL tunnel starts in the DESY facility, Hamburg, and ends in Schenefeld, a town north-west of DESY, as depicted in Fig. 38

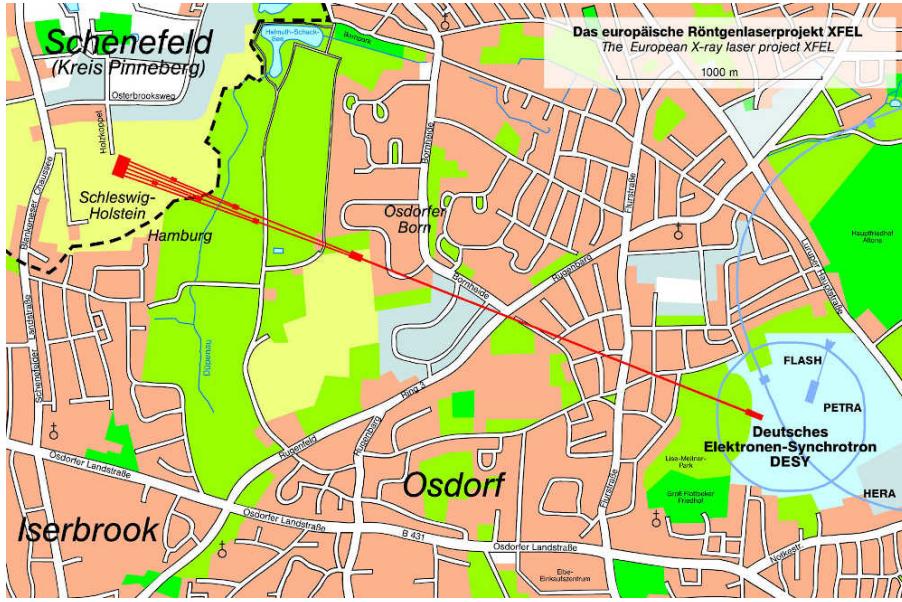


Figure 38: XFEL location and size. Image source: DESY.

The overall layout of the XFEL facility is shown in Fig. 39.

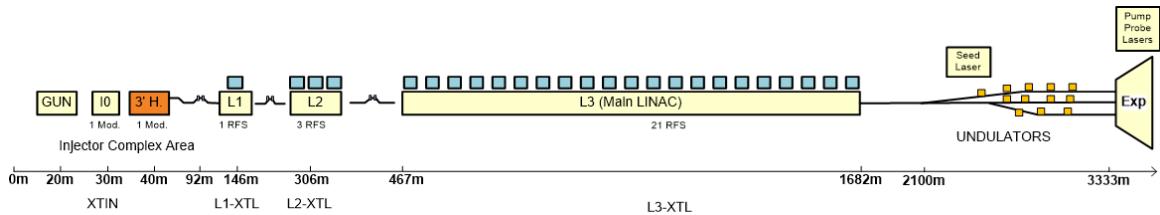


Figure 39: XFEL overall layout diagram. Image source: DESY.

In the injector, an RF gun module forms electron bunches by extracting them with a laser from a photocathode. This beam is then focused and accelerated by the injector's cavities of a total length of 66 meters and transferred to the linac input. Linac part of the

XFEL facility is 1.6 km long and made of 116 cryomodules, each 12 m long [85]. Along the linac part, two bunch compressor modules are placed to shorten the electron bunches to approx 55 um and duration less than 200 fs. At the end of the linac part the electron beam is focused and accelerated to an energy of up to 20 GeV, and then routed by the beam distribution system to one of the two electron beamlines, as shown in Fig. 40. Electron bunches pass then through the undulators. Beamline 1 is routed via undulators SASE1 and 3 and produces hard and soft X-ray photons. After SASE3 undulator electrons are routed to the dump and photons to the experimental area. Beamline 2 is routed via SASE2 undulator and provides hard X-ray photons for experiments, but also a part of the electron beam, the remaining part is routed to the second dump [85].

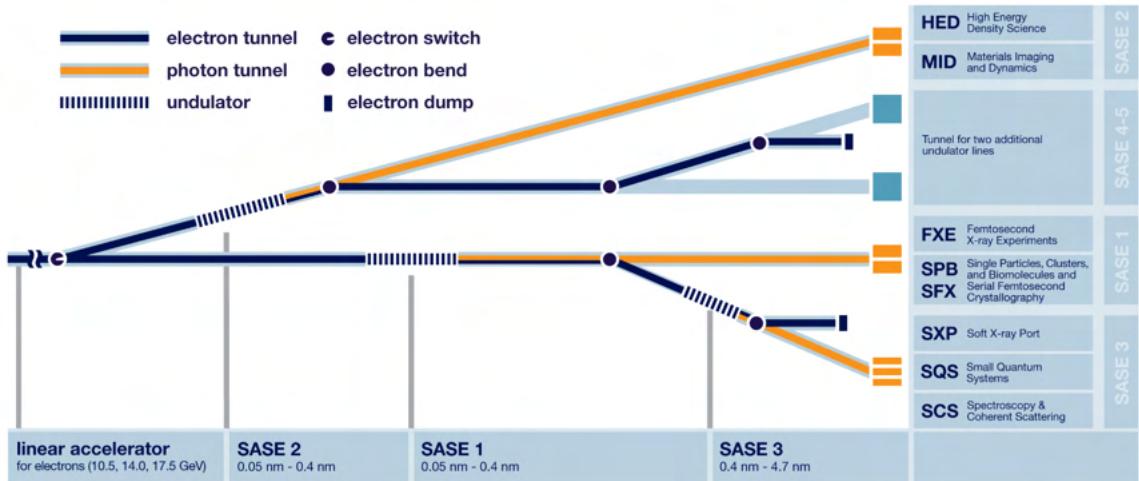


Figure 40: XFEL beamlines, undulators, and photon tunnels layout. Source: E-XFEL website.

The European XFEL was launched for official operation in 2017, after commissioning [86]. It is able to produce up to 27000 hard and soft X-ray pulses per second [42], with tens of femtoseconds adjustable duration, which also defines the strict requirements for the entire synchronization system. Phase or amplitude errors of the RF reference distributed along the over 3 km E-XFEL most critical endpoints (the booster acceleration section and the pump-probe laser system) may cause unwanted changes in the electron beam peak current and variation of the bunch time arrival at the undulators. In the E-XFEL the peak current of the photoinjector is limited to approx. 50 A. In order to boost it to a 5 kA peak the bunch compressors must compress the beam with a compression factor C

of approx 100. An amplitude change of 0.01% of the accelerating field results in a timing jitter of 33 fs at the undulator. Phase variation of the same magnitude will introduce additional 21 fs [85].

Therefore to provide the required phase and amplitude stability of the RF and laser reference the synchronization system for the European XFEL is designed as presented in Fig. 41 [16].

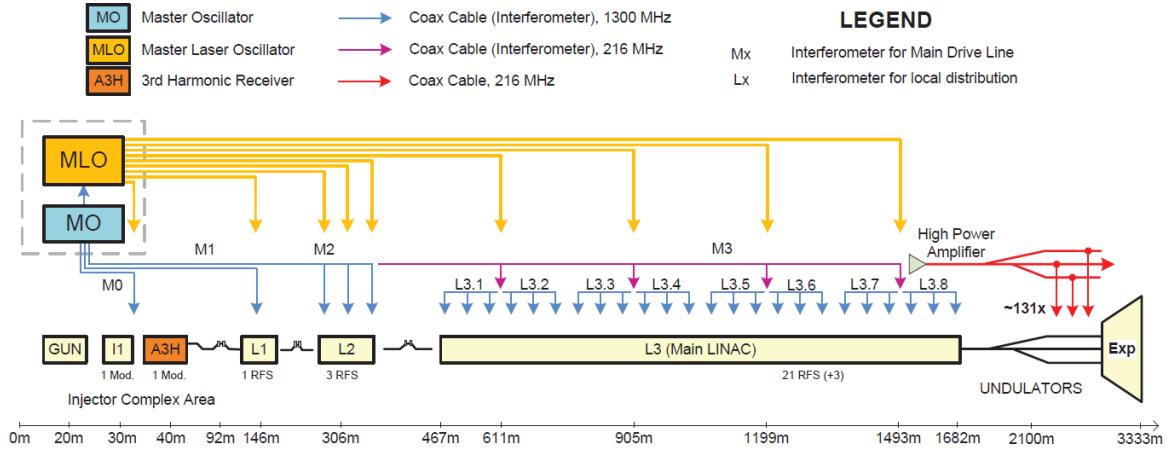


Figure 41: Block diagram of the E-XFEL PRDS.

The 1.3 GHz RF reference signal is synthesized in the MO, based on an ultra-stable 10 MHz GPS reference from GPS disciplined oscillator (GPSDO). The RF reference is then used for the synchronization of all substations, modules, and other reference frequency signals. To ensure robustness and reliability the MO module is multiplied three times and connected via a custom-made RF switch in a redundancy controller module. The redundancy controller is subject to another Ph.D. thesis conducted currently in the Warsaw University of Technology. Master Laser Oscillator (MLO) is locked to the MO. MLO is a mode-locked fiber laser at a wavelength of 1550 nm. The MLO optical reference is then distributed via dispersion-managed optical fiber. RF reference from MO is distributed via coaxial cables, which are the main source of phase drift in the RF distribution system. Therefore to compensate for these drifts both optical synchronization and RF interferometric synchronization schemes were developed and the optical one was finally installed in the system. The PRDS in E-XFEL should deliver phase stable RF signals (1.3 GHz and 216 MHz) for RF stations - 1.3 GHz for the accelerating cavities, and 216 MHz for Beam Position Monitors (BPMs). The phase stability requirements also depend

on the RF station. For injector the short term (1 second) phase jitter should be close to 10 fs, and long-term (1 hour) phase drift less than 100 fs. Similar (30 fs short-term and 100 fs long-term) requirements are for the RF signal in the booster RF station. For linac RF stations the requirements for phase stability are 100 fs short-term and 1000 fs long-term. For 216 MHz receivers the requirements are less demanding. To illustrate the complexity of the PRDS system for the European-XFEL a more detailed block diagram of L1 section PRDS fragment is shown in Fig. 42. The European-XFEL PRDS was planned to use RF interferometric links and optical RF phase compensation for the most demanding RF stations in the system. RF reference signal from E-XFEL Master Oscillator is delivered to the REFM-TP1 box, equipped with an interferometric receiver (TapPoint V2 [50], described briefly in the thesis), and a Frequency divider module [29], delivering 216 MHz signals for all BPM devices in the system. The next RF stations are supplied with RF reference signals via 1.3 GHz interferometric phase compensating loops, in total 23 stations require RF reference signal (injector station, booster station and 21 RF stations along the linac part). Parts designed by the author for the E-XFEL PRDS are marked with orange color and are key components for the E-XFEL operation.

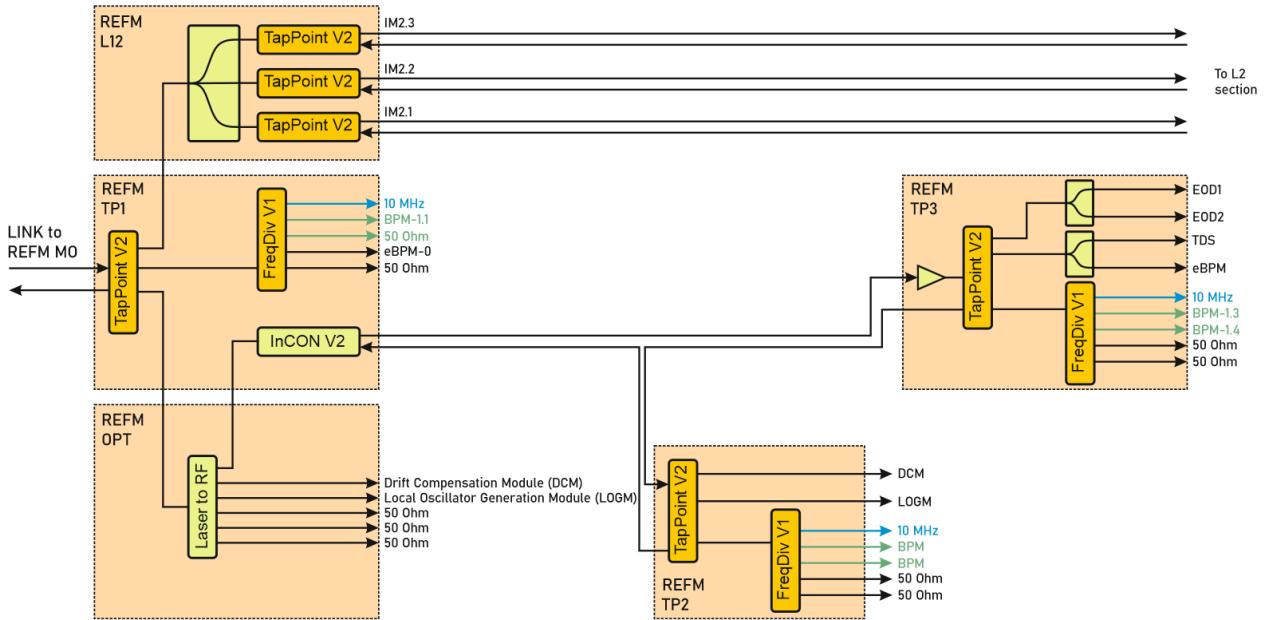


Figure 42: Block diagram of the E-XFEL PRDS, L1 section.

3.1.3 SINBAD

SINBAD is an acronym for Short Innovative Bunches and Accelerators at DESY and stands for a dedicated research and development facility in DESY. Its main purpose is to test the technical boundaries of currently available accelerator technology. Testing advanced Laser-Driven Plasma Wake-Field Acceleration (LWFA), Dielectric Laser Acceleration (DLA), or THz-based acceleration defines completely new design requirements for the accelerator control system and PRDS, as the planned bunch time arrival jitter is to be less than 10 fs, which is ten times less than in, for example, European-XFEL (100 fs).

The general layout of the SINBAD facility is shown in Fig. 43. It is located in the former DORIS accelerator building, completely emptied of all old devices and then fully refurbished and prepared for the new facility, using the race-track shaped tunnel, 300 meters long, with two 70 meters long straight parts [87].

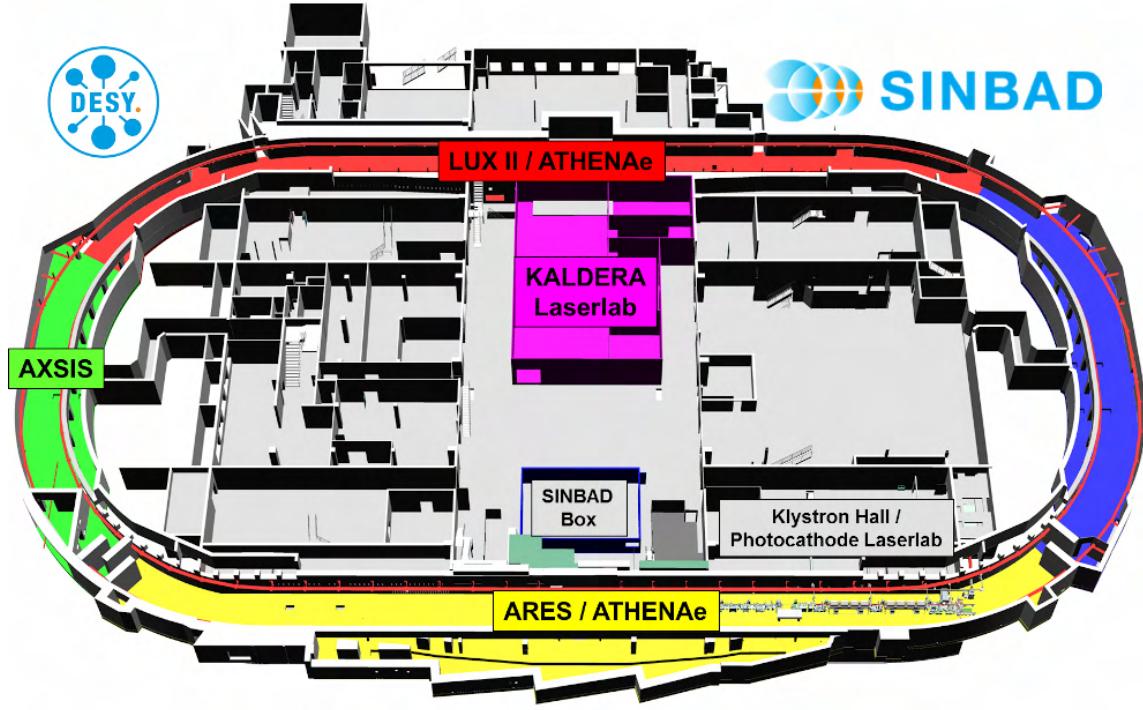


Figure 43: Layout of SINBAD facility. Image source: DESY.

Among several planned experiments in SINBAD, the most important ones are ARES and AXSIS. The AXSIS experiment [87] is planned to develop a THz-laser driven, all-optical, compact X-ray source, based on coherent inverse Compton scattering off a free-electron crystal [15]. It is to be installed in one of the arcs of the SINBAD. The second

mentioned experiment is ARES - Accelerator Research Experiment at SINBAD [88]. It is a linear RF accelerator, based on traveling-wave accelerating structures, operating at approx. 3 GHz, and delivering low charge (pico coulomb level) electron bunches with 100 to 150 MeV energy and femtosecond duration and bunch time arrival jitter. Its structure is shown in Fig. 44 [88, 77].

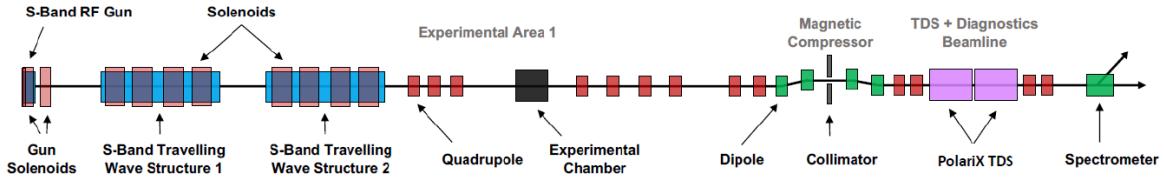


Figure 44: Layout of ARES linac in SINBAD facility. Image source: DESY.

ARES is approx. 70 meters long linear accelerator. The linac part is based on two traveling wave structures, providing energy gain of approx. 77 MeV each.

Third TWS is foreseen as a potential energy upgrade. Each cavity will be fed by an independent RF station (and thus controlled by a separate LLRF node). The accelerating structures are then followed by an optical part, where the beam is matched and then compressed in a bunch compressor. In the end, the beam is routed to the experimental area with a plasma cell for laser wakefield acceleration experiments [15]. In total there are 5 RF receivers for the designed PRDS for SINBAD - one for the optical laser lab, one for the RF GUN and Main Oscillator, and three for the TWS. Since SINBAD is planned for testing the technical boundaries of the current accelerator technology, the requirements for the PRDS are extremely demanding. The short term phase stability (1 second) should be in range of 1 fs (10 times better than in the most demanding RF station of E-XFEL) and long term stability should be better than 10 fs, due to the planned beam time arrival jitter, less than 10 fs. The first beam in ARES was generated and detected at the end of October 2019.

3.2 European Spallation Source

Neutron scattering is a well-developed and used means to get access to fundamental properties of biological matter as well as of physical materials [76]. At the end of the 20th century, it became clear that existing neutron sources are not powerful and there

are not enough of them. As a result, new neutron facilities were developed, and the first finished one was the source at Oak Ridge National Laboratory in the USA in 2006 (SNS). Then, three years later, another source was finished and launched in Japan - the J-PARC facility. In Europe discussions and plans were launched in 2003 and their result is the European Spallation Source facility in Lund, Sweden, planned for being completely operational in 2025. ESS is the most powerful pulsed neutron source in the world, based on the spallation process, which is based on hitting heavy elements with high energy proton beam and thus creating free neutrons. In the ESS the spallation is based on hitting the tungsten target with a 2 GeV pulsed proton beam. The entire ESS specification was based on the two requirements for the beam mostly [76] - the averaged flux of neutrons that should be stronger than conventional neutron sources available and the pulse repetition rate, selected to minimize the efficiency loss. These two requirements caused the use of 5 MW proton beam power and energy per pulse of 357 kJ, which leads to the beam energy of 2.0 GeV. Compared to other neutron facilities in the world - like SNS, SINC in Paul Scherrer Institute in Switzerland, and J-PARC - the ESS provides 30 times higher neutron beam intensity for experiments.

The overall layout of the ESS facility and the block diagram of the ESS linac layout is shown in Fig. 45, and Fig. 46

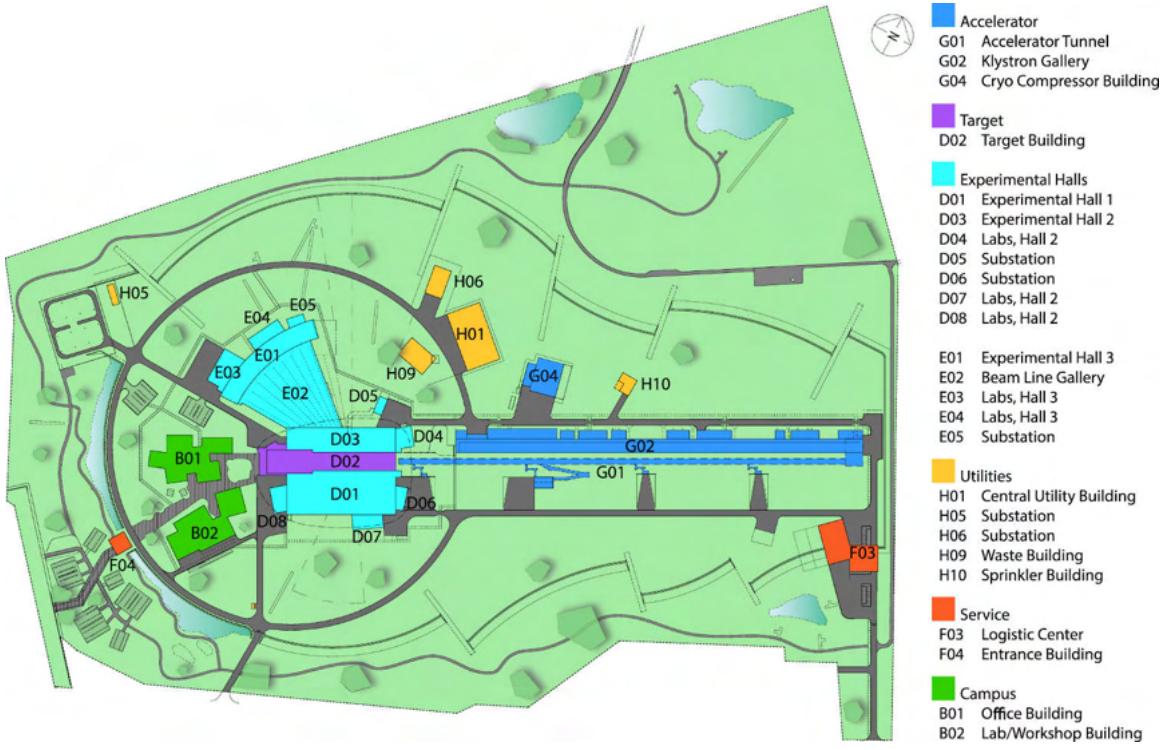


Figure 45: Layout of the ESS facility. Image source: ESS website.

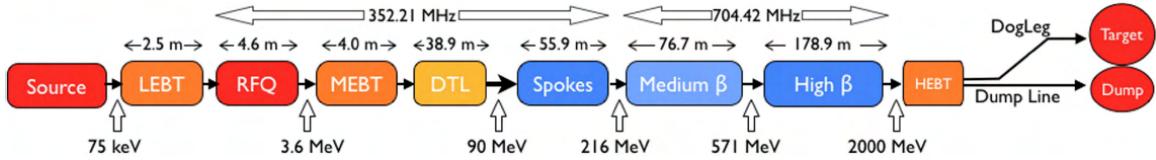


Figure 46: Layout of the ESS linac. Image source: ESS.

The ESS linac is made of both normally conducting and superconducting cavities. The ion source delivers a beam of energy of 75 keV. The beam is then focused and aligned in the low energy beam transport (LEBT), to fit the radio frequency quadrupole (RFQ) and provide continuous diagnostics. The RFQ acts as a bunch compressor and also accelerates the beam to 3.6 MeV with small losses and a minimal emittance growth [76]. Then the medium energy beam transport (MEBT) adjusts the beam before entering the drift tube linac (DTL). The MEBT section is fitted with various detectors, measuring beam current and longitudinal properties, and also adjustable collimators. The DTL accelerates the proton beam to an energy of 90 MeV in five independently powered tanks - each tank in the DTL has its own 2.8 MW powering klystron [76]. After the DTL section, the superconducting part of the linac begins. The first section is the spokes cavities - a set

of 13 cryomodules, each fitted with 2 spokes cavities and a typical tetrode-based power amplifier. Medium and high beta cryomodules are based on elliptical cavities. There are in total 36 medium beta cryomodules and 21 high beta cryomodules that increase the beam energy to the target value of 2 GeV. The beam is then adjusted in a high energy beam transport section (HEBT) to fit the rectangular proton beam window, before hitting a 160 x 60 mm tungsten target or a dump, depending on the operating mode of the linac. During the launching stage, when spallation is not fully configured, the beam is routed to the dump, allowing for a linac calibration. The spallation process creates several low-speed neutron beams that are then directly routed to the experimental area and detectors.

Warsaw University of Technology and the Institute of Electronic Systems collaborate on the ESS project since 2015. ISE is responsible for the design, development, and installation of the Phase Reference Line (PRL) and LLRF part [89]. The installed PRL is shown in Fig. 47.



Figure 47: Phase Reference Line installed in ESS facility - the line with blue boxes, attached to the tunnel ceiling.

The overall PRDS length in ESS is 600 meters. The RF reference signals of 352 and 704 MHz frequencies, are routed from the middle part of the tunnel to its both ends, supplying all the receivers. The PRL is equipped with 56 RF signal splitters, delivering

in total 294 RF reference outputs with power level of +16 dBm each. The phase stability requirements are described as 0.1 degree short-term (per each 3.5 ms pulse) for both frequencies, 0.1 degree for adjacent PRL ports per hours, and 2 degrees long-term between any two points of the PRL.

The author's contribution to ESS and the PRDS description are described in Appendices to the thesis.

3.3 Summary of PRDS requirements in described facilities

The summary of requirements for the phase reference distribution systems for the described facilities are given in the Table 3.

Table 3: The summary of requirements for described facilities' PRDS.

Facility	Length	Number of endpoints	Short-term phase stability requirement	Long-term phase stability requirement
SINBAD	70 m	5 endpoints: laser lab, RF GUN/MO, TWS1, TWS2, TWS3	1 fs (1 second)	10 fs (1 hour)
ESS	600 m	56 splitters along the PRL, 294 RF outputs	0.1 degree (per 3.5 ms pulse)	0.1 degree per hours for adjacent ports 2 degrees per hours for any two ports of the PRL
E-XFEL	1.7 km linac 3.4 km total	23 RF stations: injector, booster, 21 linac RF stations	10 fs (1 second, injector) 30 fs (1 second, booster) 100 fs (1 second, linac part) 60fs to 5.8 ps (216 MHz BPMs)	100 fs (1 hour, injector) 100 fs (1 hour, booster) 1 ps (1 hour, linac) 100 ps (1 hour, BPMs)
FLASH2020+	315 m total 120 m linac	26 outputs at 1300 MHz 10 outputs at 108 MHz 4 outputs at 1517 MHz	10 fs (1 second)	300 fs (1 minute)

4. PRDS components for European XFEL

The chapter describes parts and modules that the author designed and took part in the development of the European XFEL phase reference distribution system. The chapter describes custom frequency divider modules that are used along the entire XFEL facility [29] and parts designed for interferometric phase compensating link prototype, and to be more specific - the automated receiver module [50].

4.1 Frequency divider modules for E-XFEL

In European-XFEL in some selected endpoints there was a requirement to provide reference signal frequencies other than 1.3 GHz, but to keep the new frequency signals in sync with 1.3 GHz. Therefore a resettable frequency divider unit had to be designed and installed in the system. The new module had to provide all required signals with proper power level scaling, but also provide a functionality to reset remotely, via external LVDS differential signal, common to all E-XFEL LLRF modules, like for example Local Oscillator Generation Module (LOGM). The module had to be fully compatible with existing E-XFEL infrastructure and be available as a standalone device, to be mounted in dedicated 19" modules, or as a standalone 19" box. Both solutions were designed, delivered, and installed in E-XFEL in 2016 and 2017 and since then they are in continuous operation.

4.1.1 Requirements and block diagram

The described module had to meet the following requirements:

- Module must work with an input signal of 1.3 GHz frequency and +16 to +21 dBm input power.
- Module must not interrupt the reference signal transfer in the connected line and must not introduce more than 1 dB of reference signal loss in the main signal line.
- Module must provide input/output return loss better than 20 dB.

- Module must provide 2 outputs with the frequency of 216.67 MHz and +7 to +8 dBm output power and one 10 MHz output with a power level of +6.5 to +7.5 dBm.
- Output harmonics at all outputs should be less than -40 dBc.
- Module must be resettable via external LVDS signal, compatible with E-XFEL LLRF signals.
- Module must be supplied with a typical E-XFEL LLRF power supply voltage of +7 V DC.
- 216.67 MHz output signal phase noise should be lower than presented in Section 4.1.1.

Table 4: Requirements for XFEL frequency divider module output 216.67 MHz phase noise spectrum

Offset from 216.67 MHz carrier [Hz]	Phase noise value [$\frac{dBc}{Hz}$]
10	-95
100	-115
1 k	-135
10 k	-140
100 k	-140

The structure of a frequency divider module meeting the above requirements is presented in Fig. 48.

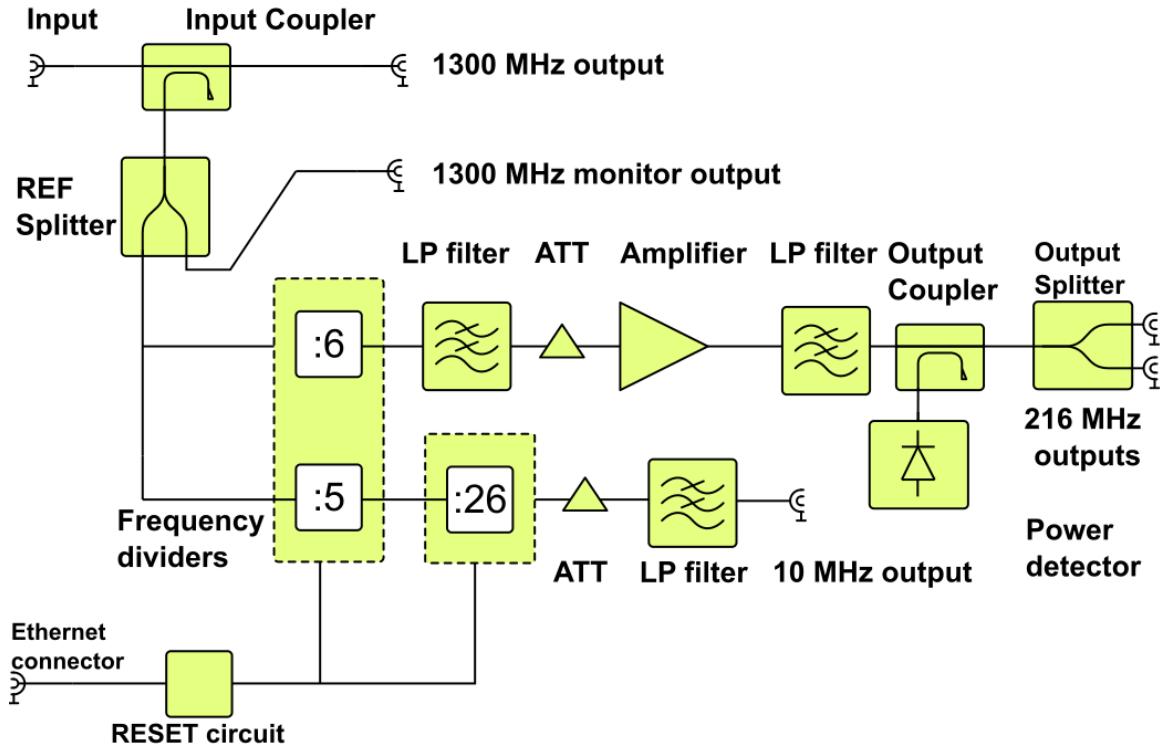


Figure 48: European XFEL Frequency divider module block diagram.

The input reference signal is coupled by an internal surface mount directional coupler and then routed via a power splitter to the double clock divider chip, which may be also used for frequency division of analog RF signals, up to 1.6 GHz. A second output of the REF splitter is used as an optional monitoring connector. The clock divider chip is used to synthesize the 216.67 MHz and 260 MHz signals. 216.67 MHz signal is then filtered and amplified to meet the requirements. The module is fitted with diagnostic circuitry to monitor the output power at 216.67 MHz outputs and the overall temperature of the module. The 260 MHz signal is used with another clock divider chip to synthesize the 10 MHz signal. Both clock divider chips are connected to the reset circuit chip, realized using LVDS to LVCMOS converter and a few 74LVC series logic gates.

The described frequency divider module was manufactured as a standalone RF-shielded module, in a custom metal housing and is presented in Fig. 49.

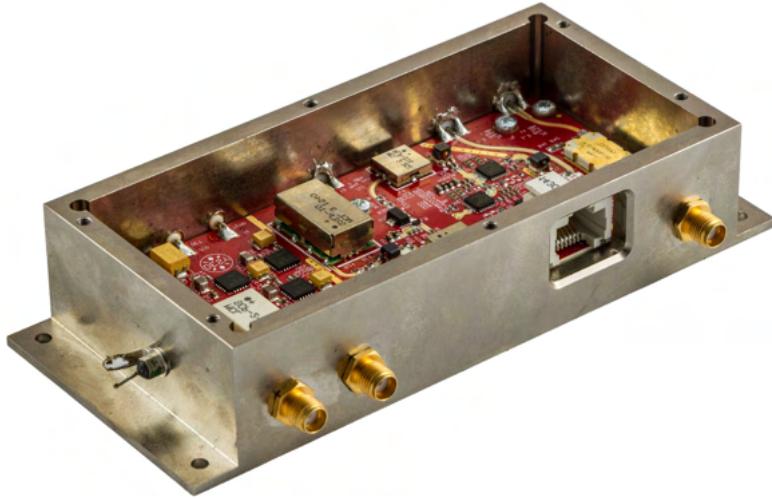


Figure 49: European XFEL Frequency divider module.

All the RF connectors are threaded SMA. At the time of designing the module, such connectors were used in circuits designed in ISE, however, they are not the best solution for routing RF signals in housings. First of all the diameter of the mounting thread and its pitch are the same as for the SMA thread ($\frac{1}{4} - 36UNS$), so the force applied to the connector is comparable to the force used for tightening it in the housing, which may lead to uncontrolled untightening of the connector and result in a destruction of a PCB. To solve the problem author has developed a solution for using a 4-hole flange SMA connectors, fitted with extra moisture sealing. The method is described in the Appendices to the thesis and may be found useful in any metal RF-shielded housing design.

The module presented above was also delivered as a standalone 19" box, according to the specification and order from DESY. These boxes are installed in European XFEL and one of them is shown in Fig. 50. In total 70 modules were manufactured and delivered to DESY.

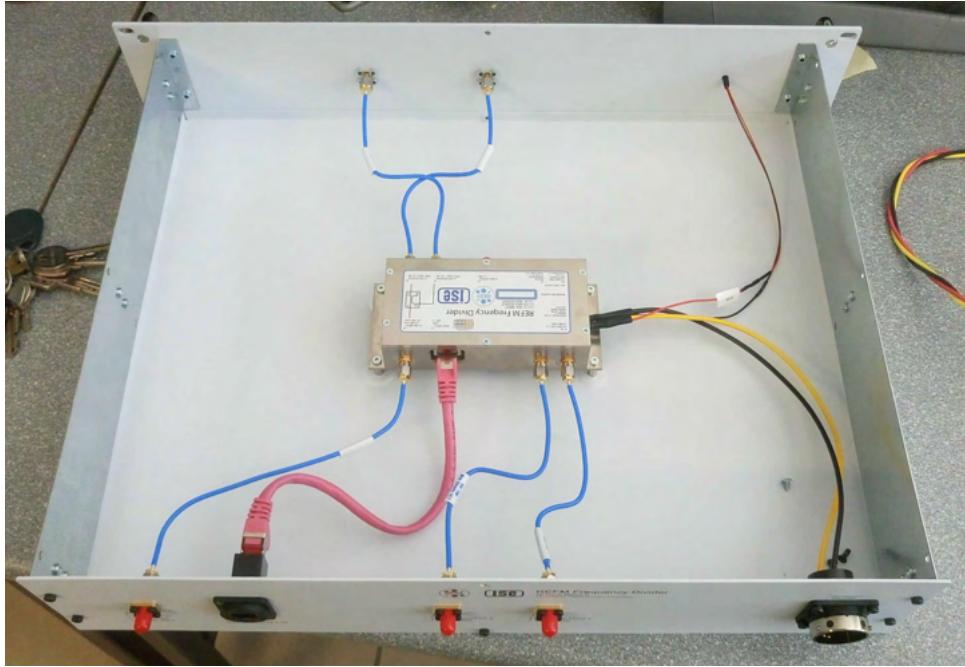


Figure 50: European XFEL Frequency divider 19" box, without the top lid.

4.1.2 Test results

Tests were performed for each of the manufactured modules and reports were delivered to DESY as proof of meeting the requirements of every delivered device. During tests, the return losses of 1.3 GHz and 216.67 MHz lines were tested, as well as mainline insertion loss, spectral purity, and phase noise PSD. A sample 1.3 GHz mainline loss of a standalone FreqDiv module is shown in Fig. 51. At 1.3 GHz the insertion loss is slightly above 0.7 dB and meets the requirements. Modules delivered as 19" boxes, due to additional internal RF coaxial cables and feed-throughs introduce approx. 0.9 dB IL in the worst case.

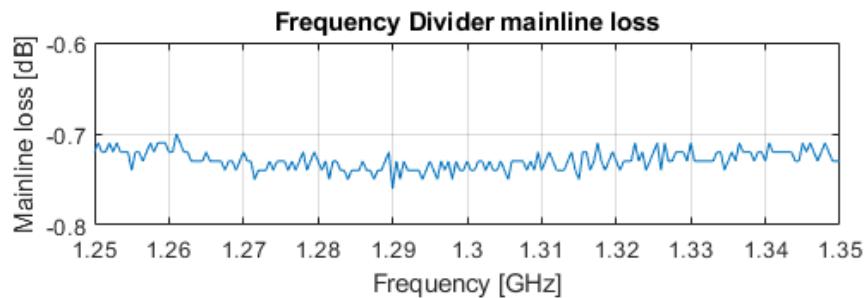


Figure 51: European XFEL Frequency divider introduced insertion loss plot vs frequency [29].

Return losses (presented using S11) at 1.3 GHz and 216.67 MHz ports are shown in Fig. 52, and Fig. 53. The results are far better than those specified in the requirements and prove that all the components in the RF signal lines are designed correctly.

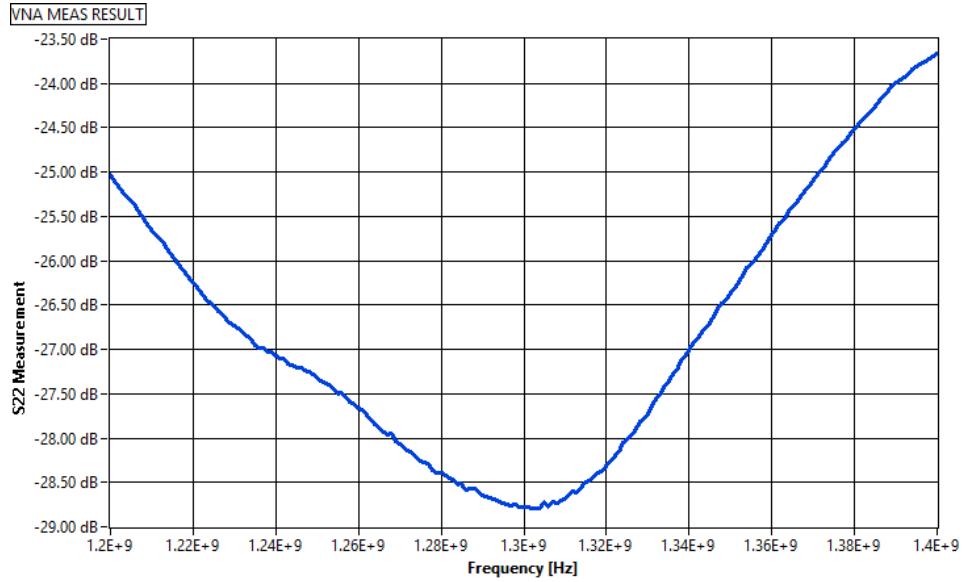


Figure 52: XFEL FreqDiv 1.3 GHz port S11 plot.

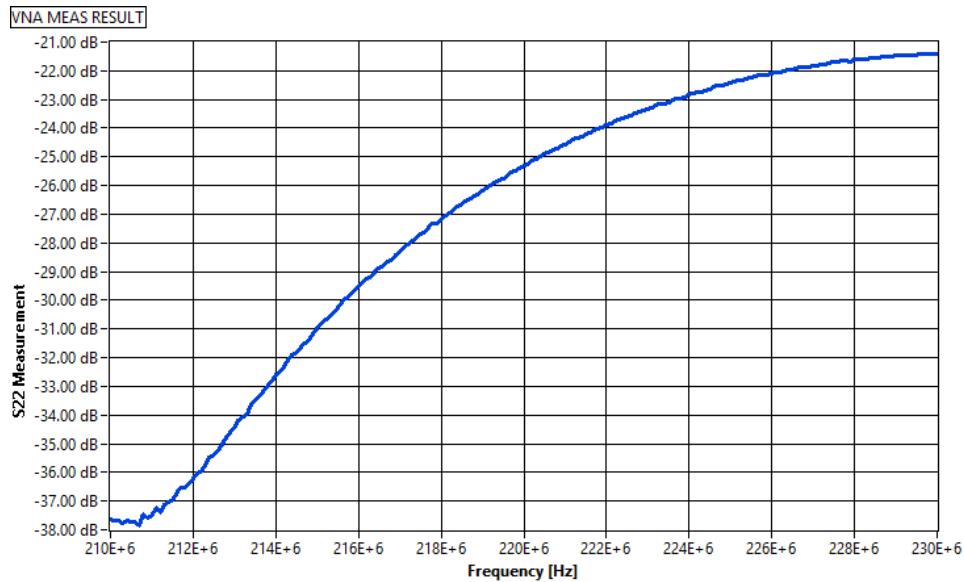


Figure 53: XFEL FreqDiv 216.67 MHz port S11 plot.

Spectral purity, defined in requirements as the difference in dBc between the main signal tone and second and third harmonics, is presented in Fig. 54. All the manufactured modules meet the spectral purity requirement, due to the output RF filtering stages, which had to be implemented due to the output types of AD9515 - the chip provides one differential LVDS / LVCMOS output and one differential LVPECL output.

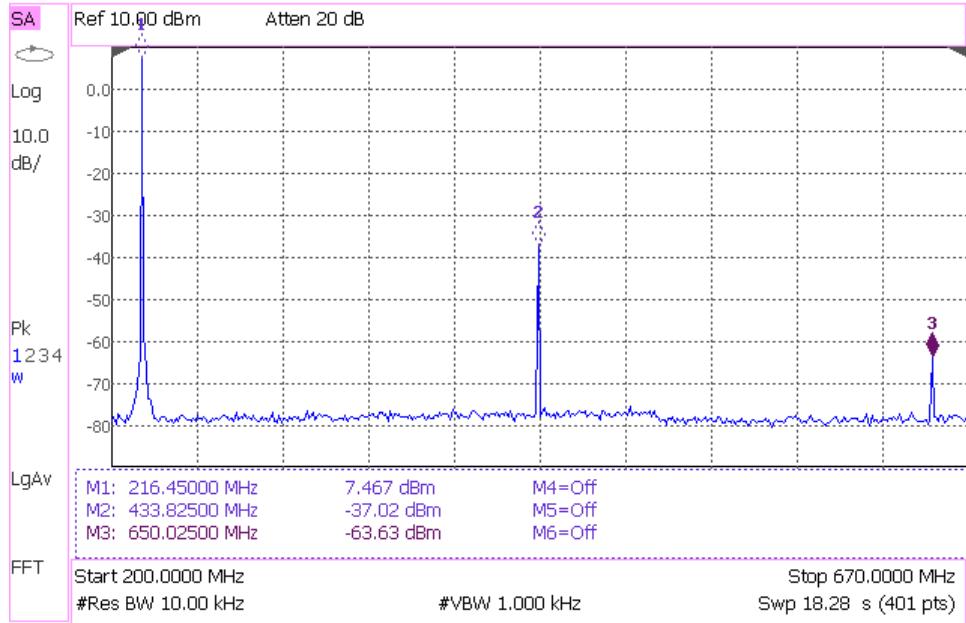


Figure 54: XFEL FreqDiv 216.67 MHz signal spectrum, showing first three harmonics [29].

The phase noise measurement results are presented in Fig. 55, and Fig. 56. The requirement plot is shown for 1.3 GHz, all signal plots are scaled, according to the frequency scaling factor. For frequency offsets greater than approx. 2 kHz all the requirements are met. For offset values closer to the carrier requirements violations are observed, yet their source was found to be the used RF laboratory Master Oscillator. No violations are observed in additive phase noise plots.

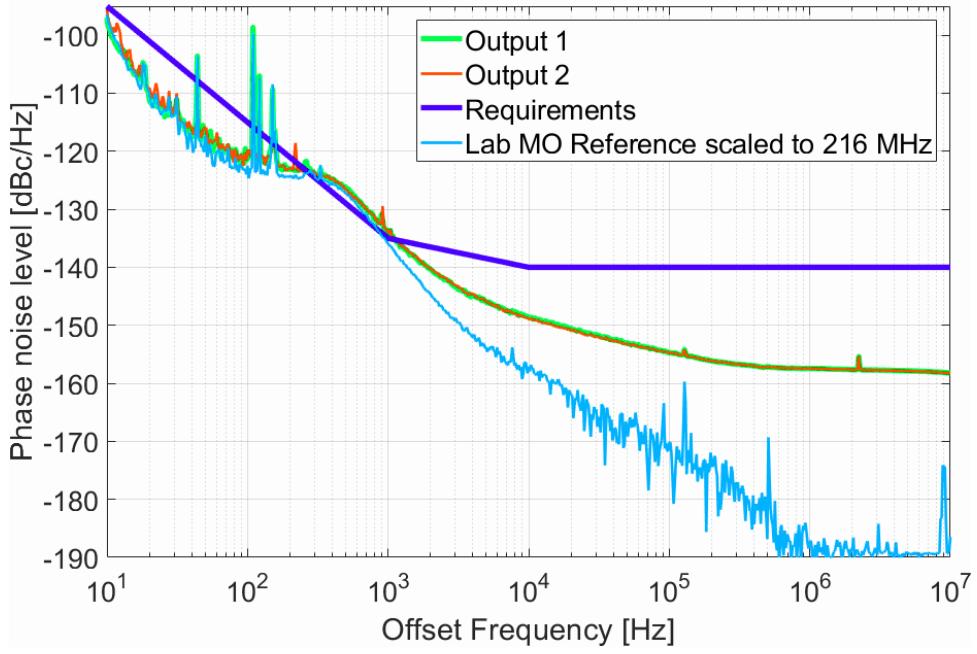


Figure 55: XFEL FreqDiv 216.67 MHz signal phase noise plot vs requirements [29].

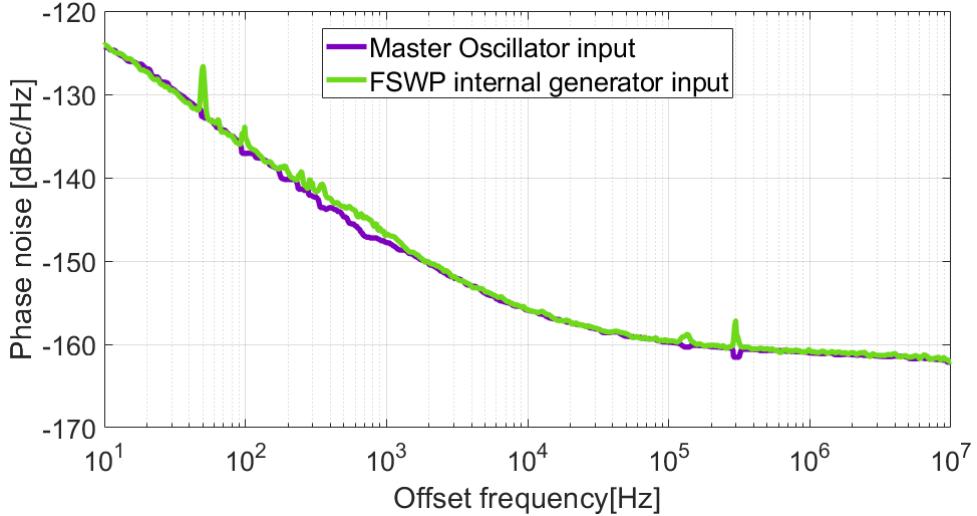


Figure 56: XFEL FreqDiv 216.67 MHz additive phase noise plot.

In the end, the module met all the requirements and was successfully installed in the European XFEL facility. For more than 1 year the modules worked flawlessly. During the first service shutdown, around the year 2018, it turned out that one of the installed modules during shutdown destroyed a high-power amplifier, driving the beam position monitor (BPM) circuits. After a detailed investigation, the author has found that the problem was caused by the used clock divider chip. The AD9515, under no input signal,

creates a random full-scale output digital signal that destroyed the amplifiers. The author has also noticed that no such behavior is observed when an RF signal is present, or when the whole FreqDiv module is under reset. Therefore the applied solution for the European XFEL was a change of shutdown strategy - before shutting down the RF all the FreqDiv modules must be placed in the reset state. Monitoring of input RF power level is the task for the LLRF circuitry. After fixing the described problem all the modules work without problems till the day of writing the thesis. For the FLASH facility, the module was redesigned to overcome the problems found. The solution is described in the next section of the chapter, devoted to the FLASH2020+ PRDS update.

4.2 Interferometer for E-XFEL

As a part of the European XFEL collaboration project that the author participated in, a prototype of interferometric phase drift compensating link was proposed [79] and based on the concept presented by Chase and Cullerton [78]. The entire link is a subject of a Ph.D. thesis by Dominik Sikora. The author's contribution is the hardware design of an automated interferometric link receiver module [50], as a Master thesis. That Master thesis was awarded a third price for the best Master thesis topic in the 22nd International Microwave and Radar Conference MIKON 2018. The transmitter module was a subject of the MSc thesis of Dawid Kołcz [90]. Both modules are used to form an interferometric link and are presented in Fig. 57, Fig. 58. The prototype interferometric link was successfully assembled and tested in laboratory conditions. During laboratory tests the achieved phase drift suppression factor, limited by the performance of the phase detectors, was from 10 ps to 50 fs - 200x [79]. Similar systems are successfully developed and presented in [91, 92].



Figure 57: E-XFEL interferometer InCON V2 transmitter module.



Figure 58: E-XFEL interferometer TapPoint V2 receiver module.

5. PRDS components and design methods for FLASH2020

The chapter describes all the work done for the upgrade of FLASH2020+ PRDS components. The old and updated system structures are presented. All the designed and installed hardware is described and test results for the most important system parameters are presented and discussed. Due to the ongoing commercial production preparation and details of the bilateral agreement between DESY and ISE, no information leading to the full device reconstruction is presented. Therefore in the thesis information about the exact models of parts used is not published.

5.1 The structure of updated PRDS for FLASH

The previous PRDS structure was proposed by Czuba and Weddig and described in [18]. The RF generation and distribution part is presented in Fig. 59. All the endpoints are connected to the PRDS components via coaxial cable net, without any passive nor active phase drift compensation methods, except for pickup cables in LLRF nodes, as described by Ludwig [80].

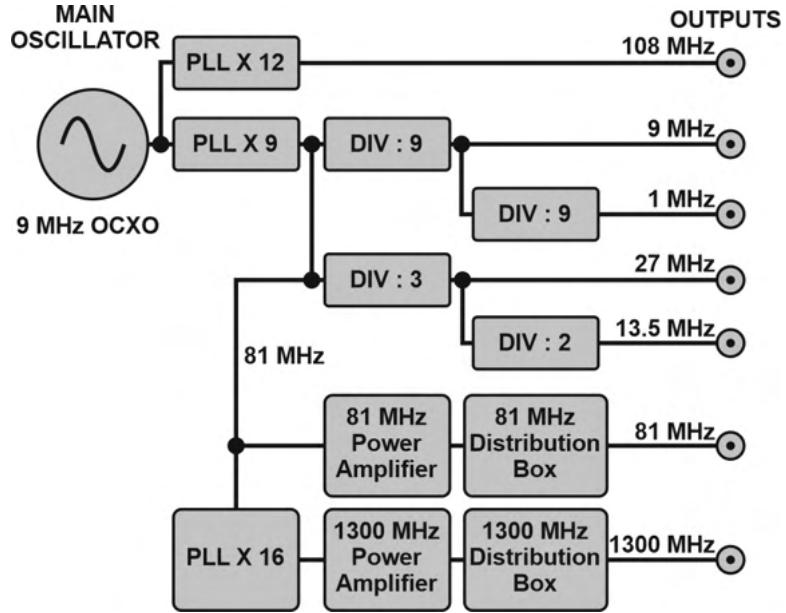


Figure 59: Old FLASH PRDS scheme.

All the reference signals were derived from an ultra-stable 9 MHz OCXO. Higher frequencies were obtained by using PLL signal synthesizers and frequency dividers, providing a set of signal frequencies from 1 MHz to 1.3 GHz. At the time of development this system was state-of-the-art and offered extraordinary performance, yet over years it became obsolete, some frequencies were not needed anymore in FLASH, the aging effects of used crystal oscillators became noticeable, and last, but not least, it occupied three 19" rack cabinets. Between these cabinets, all the power and RF signals had to be distributed, which was not the best solution in terms of robustness, but also maintenance and service repairs. Therefore, after more than 15 years of operation, during the FLASH2020+ shutdown, a decision was made to completely redesign the Master Oscillator, and distribution modules, reorganize the frequency conversion scheme, and rearrange the cabling layout in the facility. This task was performed by a team, formed with DESY and ISE engineers. DESY was responsible for the on-site upgrades and ISE developed the 19" hardware.

The updated structure of FLASH2020+ PRDS is presented in Fig. 60.

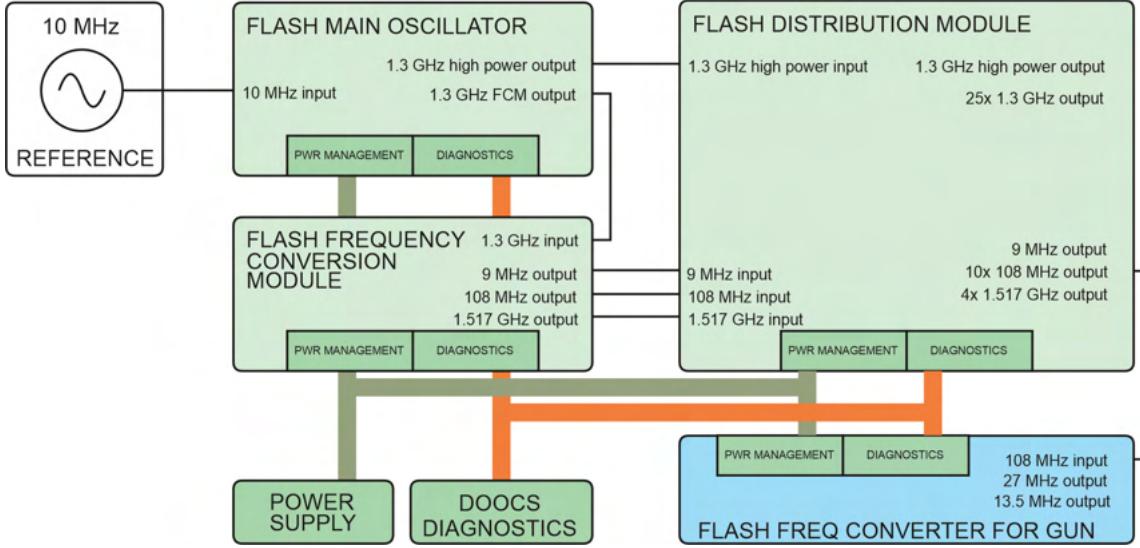


Figure 60: Upgraded FLASH PRDS scheme.

The structure of a system originated from a solution designed in ISE and used in European XFEL Master Oscillator and Distribution module [93]. All the design bottlenecks and problems were identified and fixed in the upgraded design for FLASH. An ultra-stable 10 MHz reference is obtained from the GPS disciplined oscillator (GPSDO). This signal is used by a newly designed Main Oscillator module (FLASH MO) that synthesizes 1.3 GHz high-power signals and delivers them to the Frequency Conversion Module (FLASH FCM) that synthesizes most of the required signal frequencies. Then all the signals are routed to the DIStribution Module (DISM), which routes the signals to all the RF coaxial cables and via these to all the FLASH endpoints. The only box designed by DESY is the Frequency Conversion Module for RF GUN in FLASH (FLASH FCM GUN) - this box will not be described in the thesis. Its structure is similar to the FLASH FCM module, as both boxes share the same critical components, designed by the author of the thesis. All the modules are designed as 19" boxes, to be then installed in a single 19" rack cabinet. All the modules are compatible with DESY LLRF power delivery scheme and diagnostics, therefore may be easily used in other DESY accelerators, and also in other facilities. At the moment of writing the thesis the designed modules are planned to be manufactured by the industry and sold by DESY to other interested facilities worldwide.

5.2 FLASH2020+ PRDS requirements

The system requirements for a new PRDS for FLASH originated from the old system, and were both strict- and soft-defined, and are presented in Table 5 [94].

Table 5: Upgraded FLASH PRDS requirements

1300 MHz main reference signal	
Output frequency	1300.000000 MHz
Number of outputs	25 low power, 1 high power
Power level at HP output	+44 dBm approx.
Power levels at LP outputs	+20 to +26 dBm
Phase stability (jitter)	less than 10 fs RMS, (10 Hz - 1 MHz)
Frequency stability	better than 10^{-12} (hours-days)
Amplitude stability	better than 0.1%
108 MHz reference signal	
Output frequency	$1300 \text{ MHz} \cdot \frac{1}{12} = 108.(3) \text{ MHz}$
Number of outputs	10
Output power levels	+10 to +23 dBm
1517 MHz reference signal	
Output frequency	$1300 \text{ MHz} \cdot \frac{7}{6} = 1516.(6) \text{ MHz}$
Number of outputs	4
Output power levels	+17 dBm
9 MHz reference signal	
Output frequency	$1300 \text{ MHz} \cdot \frac{1}{144} = 9.02(7) \text{ MHz}$
Number of outputs	1
Output power levels	$5V_{pp}$ at 50 Ohm load

The requirement for the MO was to deliver only the 1.3 GHz reference signal. All other signal frequencies are synthesized by the FCM module and then distributed by a DISM module. DISM must provide a minimum of 25 low-level 1.3 GHz reference signal outputs and one high-power output. The phase stability of the MO 1.3 GHz reference signal, integrated into the frequency offset range from 10 Hz to 1 MHz should be 10 fs RMS max. The designed new PRDS system for FLASH meets these requirements.

5.3 Master Oscillator module for FLASH2020+

The newly designed Master Oscillator 19" module for FLASH is presented in Fig. 61. It has been designed as a standalone 19" box, 5U height, fully compatible with existing DESY 19" hardware. The front panel hosts diagnostic alphanumeric displays that provide continuous information about the device status and output power levels. The diagnostic functionality is governed by a Temperature Monitor and Control Board (TMCB), placed vertically, at the right side of the panel. Front panel SMA connectors provide monitoring of the most important internal RF signals. To the left, there is an additional slot for a potential upgrade, based on the installation of a vector modulator card. This functionality was not installed at the time of writing the thesis.



Figure 61: New FLASH MO module for FLASH2020+ upgrade.

The module was designed using completely new and improved components in comparison to the European XFEL Master Oscillator module. Key components were delivered by third-party companies. The author's contribution was the complete concept and methodology of designing vibration and thermal stress-proof generation systems, and the mechanical design of the module. The presented design approach is novel and may be used in other applications. Electrical integration was handled by Bartosz Gąsowski and assembly was by Tomasz Owczarek.

5.3.1 MO internal structure

The internal structure of the FLASH MO originated from the existing design of European XFEL MO [93] and is presented in Fig. 62.



Figure 62: New FLASH MO block diagram.

The 10 MHz is provided by an external commercial GPS disciplined oscillator module. Then this signal is used by a 100 MHz PLL-based multiplier that synthesizes the 100 MHz reference signal, and then another non-PLL-based x13 multiplier is used to create a 1.3 GHz signal. This signal is used as a reference for a 1.3 GHz PLL synthesizer driving an ultra-stable Dielectric Resonator-based Oscillator (DRO). The last part of the block diagram is the custom high-power amplifier module that delivers the +48 dBm of output power at the 1.3 GHz output port of the FLASH MO module.

The structure of the FLASH MO was carefully analyzed to minimize all sources of introduced time jitter. A mathematical model describing the structure is presented and compared to an obvious solution of synthesis of the 1.3 GHz signal using a 10 MHz signal - via 130x multiplier based on the PLL circuit. Such circuit must introduce a frequency divider in the signal feedback loop and its impact is further analyzed. Using the theory of signal modulation and assuming that all noise sources are not correlated (or the system

is considered as linear time-invariant) and thus the total impact may be analyzed as an arithmetical sum of each source contribution for the typical approach, based on a single PLL multiplier, as described by the Eq. (5.1).

$$\begin{aligned} S_{\phi_{tot}}(f) &= S_{ref_{out}}(f) + S_{PHD_{out}}(f) + S_{FDIV_{out}}(f) + S_{DRO_{out}}(f) = \\ &= [S_{ref}(f) + S_{PHD}(f) + S_{FDIV}(f)] \cdot \frac{1}{H(f)^2} \left| \frac{G(f)H(f)}{1+G(f)H(f)} \right|^2 + \\ &\quad + S_{DRO}(f) \cdot \left| \frac{1}{1+G(f)H(f)} \right|^2 \end{aligned} \quad (5.1)$$

$S_{\phi_{tot}}(f)$ is the total phase noise spectral density at the output of the 1.3 GHz DRO-based PLL. $S_{ref_{out}}(f)$, $S_{PHD_{out}}(f)$, $S_{FDIV_{out}}(f)$, $S_{DRO_{out}}(f)$ are the phase noise spectral densities originating from the reference source, phase detector, frequency divider and the DRO. By replacing the PLL feedback loop frequency divider with an ultra-low noise multiplier of a reference signal the total phase noise at the output of the MO is reduced. This is because of two things - the removal of the N^2 factor from the noise contribution of the phase detector, and the complete removal of the frequency divider's impact, which is in general the most important factor that limits the in-loop phase noise floor level (far from the carrier). While a good frequency multiplier might be comparable with the best frequency dividers in terms of the phase noise floor, the multiplier's effective noise contribution $S_{MULT}(f)$ is not scaled by the N^2 factor. The 100 MHz PLL multiplier uses the signal of a high-performance 100 MHz OCXO and filters the far-from carrier GPSDO phase noise. The formula describing the FLASH MO total phase noise is therefore as shown in Eq. (5.2).

$$\begin{aligned} S_{\phi_{tot}}(f) &= S_{ref_{out}}(f) + S_{MULT_{out}}(f) + S_{PHD_{out}}(f) + S_{DRO_{out}}(f) = \\ &= [S_{ref}(f) \cdot N^2 + S_{PHD}(f) + S_{MULT}(f)] \cdot \left| \frac{G(f)}{1+G(f)} \right|^2 + S_{DRO}(f) \cdot \left| \frac{1}{1+G(f)} \right|^2 \end{aligned} \quad (5.2)$$

To demonstrate the phase noise PSD impact of mentioned sources measurements in the FLASH MO were made and the results are presented in Fig. 63, all the contributions are frequency scaled for presenting in a single figure.

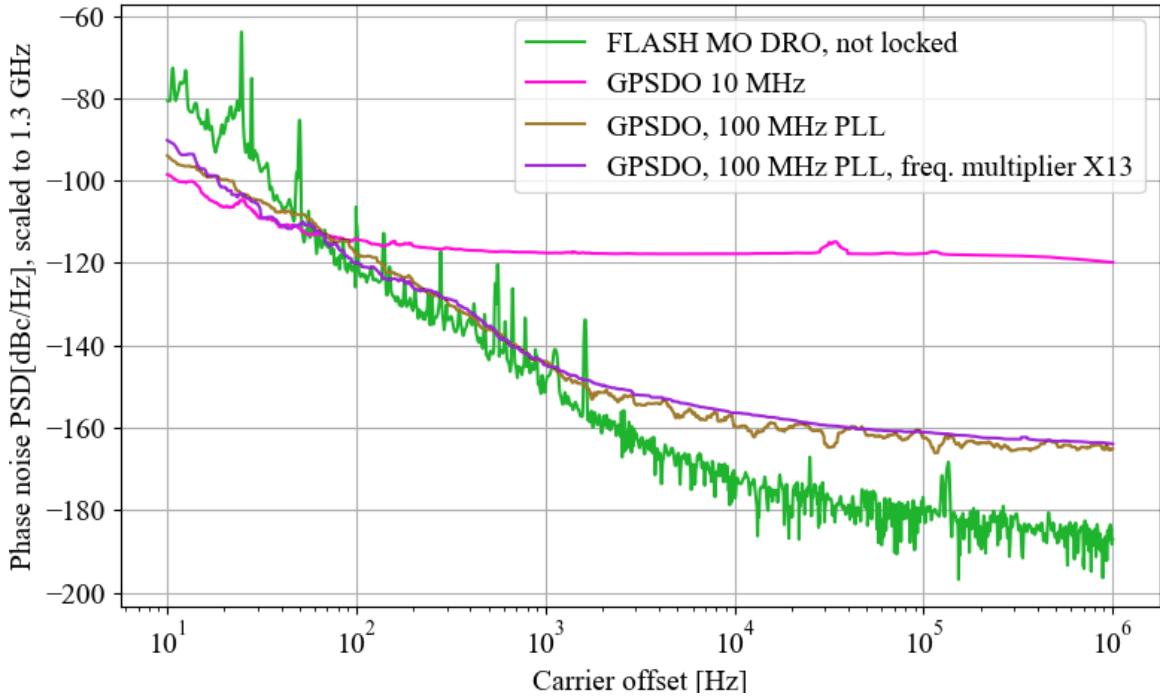


Figure 63: Phase noise PSD plots for selected FL-MO1300 components and their cascades.

The 1.3 GHz DRO phase noise PSD plot shows that the DRO provides exceptionally low jitter for far from carrier frequency offsets. The 10 MHz GPSDO signal on the contrary delivers outstanding PN PSD performance for close to carrier frequency offsets, where most of the timing jitter is integrated. The last two plots to comment from Fig. 63 are the cascade results. It may be noticed that introducing the x13 non-PLL multiplier to the cascade of GPSDO and 100 MHz PLL multiplier does not cause significant degradation of the overall phase noise of the cascade, therefore is an optimal solution to be used in FLASH MO 1.3 GHz synthesizer.

5.3.2 MO mechanical concept and design methodology

As previously described the FLASH MO module is based on 100 MHz OCXO and 1.3 GHz DRO, both of which are known to be extremely fragile to vibration and temperature change. Therefore all the known sources of vibration and thermal stress had to be identified and minimized. The FLASH MO was required to be in 19" box format, to be then mounted in a rack cabinet. That rack is equipped with an air conditioning system that maintains low humidity and stabilizes the temperature. However, all the installed modules in the rack cabinet are considered to be sources of both temperature change (heat

sources) and vibration, as most are equipped with fans. To avoid all potential problems with the environmental (rack cabinet) impact the 19" box had to be designed thoughtfully. The new MO structure, developed according to the new method is presented in Fig. 64.

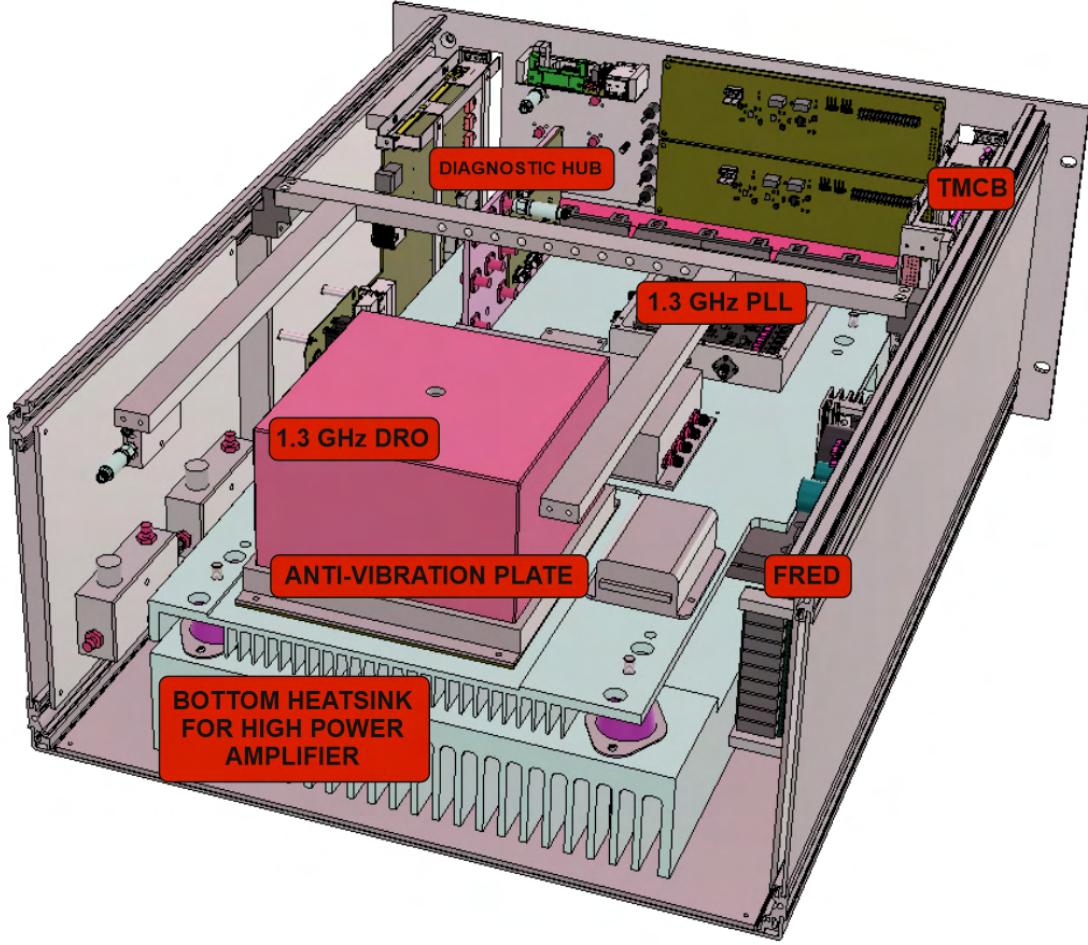


Figure 64: Internal mechanical structure of FLASH MO.

The internal structure is divided into several layers. The most important parts are the bottom heatsink and the anti-vibration plate. The bottom heatsink acts as a cooling part for the high-power amplifier after the DRO but is also on purpose chosen to be as big and heavy, as possible. Because of its location, at the very bottom of the box, it acts as a stable mounting plate and helps to reduce the vibration impact. The heatsink is mounted directly to the bottom plate of the box, creating air-sealed compartments, between its ribs. To provide a controlled airflow in the box, which will go through the heatsinks and not through the entire box, causing the thermal stresses, the bottom heatsink is connected with frontal fans via a 3D-printed air collector. This guides the airflow through the

heatsink only. The fans are installed on the front panel with antivibration pads and the air collector, nor the heatsink, has direct contact with the fans. All the RF cables used in the module are extra-flexible, to reduce vibration transfer through RF cables.

On top of the heatsink, there is another plate installed, marked as an anti-vibration plate. This feature is achieved by placing the plate on four anti-vibration dampers. All the vibration-sensitive parts, including the DRO and OCXO modules, are installed on the antivibration plate. To prevent any thermal stress on the DRO it is mounted to the antivibration plate with a special insulating pad with air pockets and placed in a custom 3D-printed insulating cap. To protect the DRO against potential mechanical stress and damage, by placing other boxes on top of the FLASH MO 19" module, the box is fitted with aluminum bars that protect the top of the DRO.

All other modules, like the power management module (FRED) and diagnostic controller (TMCB) are placed on the sidewalls of the box, to optimize the occupied space within the box and to increase spacing between them and the vibration-sensitive part of the module. All the RF cables are routed via a custom copper-based diagnostic hub, which serves a function of a star topology ground distribution in the box, preventing the creation of unwanted ground loops, especially in the RF section. Such cable routing strategy has one more significant advantage - it greatly improves the serviceability and simplifies the assembly and further maintenance of the box. Both sidewalls, front and rear panels, and all the electronics they carry, may be easily detached by removing a few connections and bolts in the box. Then the outer part of the box may be removed and there is easy access to all the internal components, as shown in Fig. 65. In contrast, the design of E-XFEL MO is presented - that box was not designed for easy maintenance and service, as shown in Fig. 66. For transportation purposes, the antivibration plate may be mounted to the base heatsink using transport bolts that provide a rigid connection and protect against antivibration dampers damage during transport.

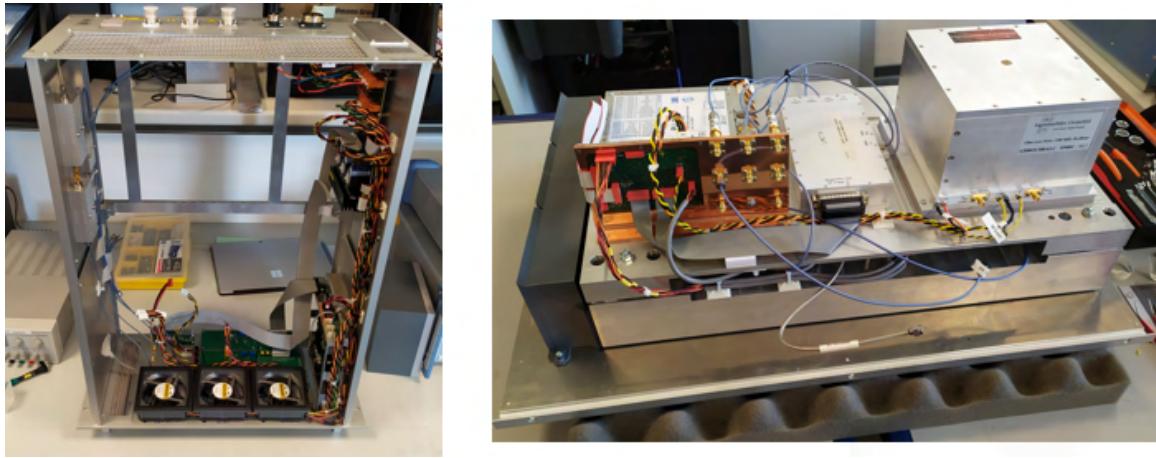


Figure 65: Assembling the new FLASH MO and illustration of easy access.

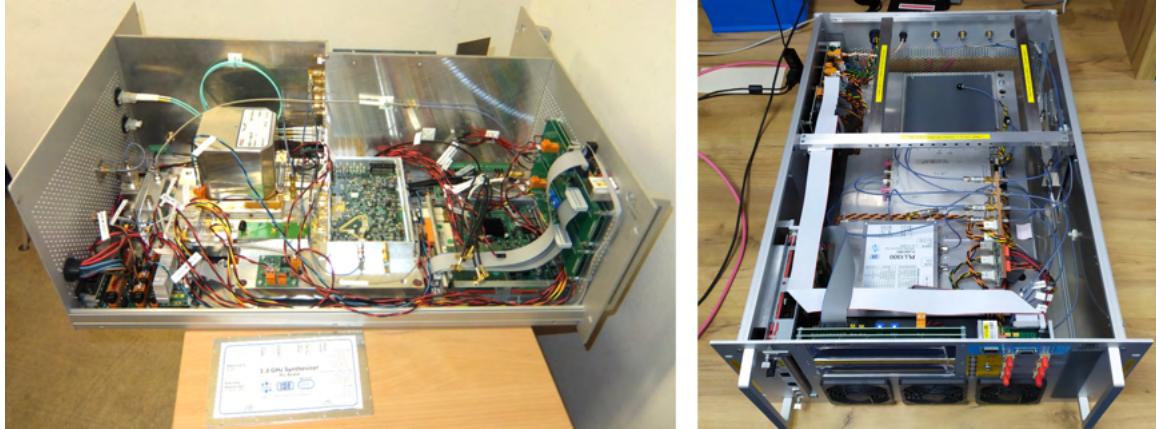


Figure 66: Internal view of the E-XFEL MO (left photo) as an example of not optimal mechanical design, compared to the new FLASH MO design (right photo).

5.3.3 FLASH2020 MO test results

Two prototypes of FLASH MO were manufactured and then installed in FLASH. The third prototype module was foreseen as a Laboratory Master Oscillator upgrade and was in assembly at the time of writing the thesis. Tests of the installed in FLASH prototypes were done both in Warsaw and then in DESY, as verification before the installation. During tests, due to the lack of a GPSDO 10 MHz source in Warsaw, a high-quality RF signal generator Rohde & Schwarz SMB100A was used as a 10 MHz reference. The phase noise plots were collected using Rohde & Schwarz FSWP analyzer and are presented in Fig. 67.

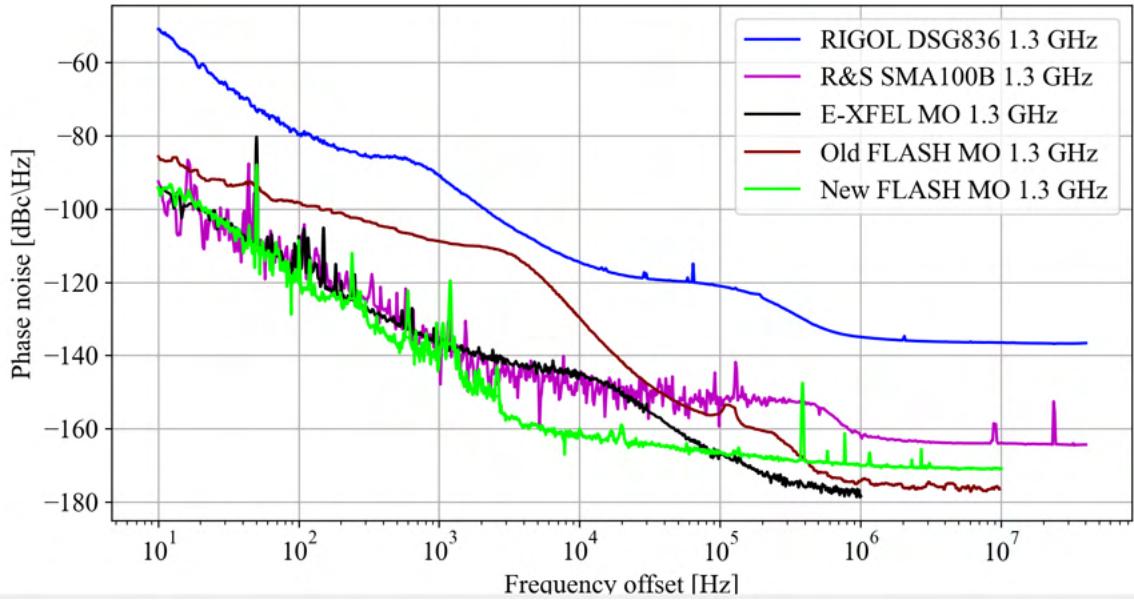


Figure 67: Phase noise PSD of 1.3 GHz FLASH MO output signal, compared with other 1.3 GHz signal sources.

To verify the outstanding FLASH MO phase noise performance and check if it meets the requirements a total time jitter was calculated at 10.7 fs in the range from 10 Hz to 1 MHz and 0.8 fs in the range from 1 kHz to 1 MHz frequency offset from the carrier. A slight improvement may be observed when the 10 MHz reference is replaced with the GPSDO, as the phase noise results higher by 0.7 fs than specified in the requirements come from the 10 MHz reference and not the FLASH MO. When compared to E-XFEL MO (19.5 fs in integration range from 10 Hz to 1 MHz) an improvement of almost 2x is observable, and almost 6x when compared to the old FLASH MO design (55.9 fs in the same integrating range). The new design of FLASH MO delivers the lowest integrated jitter so far achieved in DESY modules and one of the best available now in the world (when compared for example with R& S SMB100A, considered to be one of the best currently available RF signal generators in the world in terms of phase noise).

5.4 FLASH2020 DISM module

The next 19" module designed for FLASH2020+ PRDS upgrade is the distribution module DISM. It is a 19" 5U high box containing custom-made hermetic and thermally stabilized high power splitter modules with embedded diagnostic circuits, which is a novel approach to the problem of reference signal distribution. Solutions known to the author are based on commercially available power splitters and external diagnostic circuits, and there are no such power splitters with presented functionality so far designed. The photo of the DISM module is presented in Fig. 68.



Figure 68: Photo of FLASH DISM 19" module. Front view.

The internal structure is simple, yet its complexity unfolds in detail and custom-made internal devices. The block diagram of DISM is presented in Fig. 69 and the internal modules description is presented in Fig. 70.

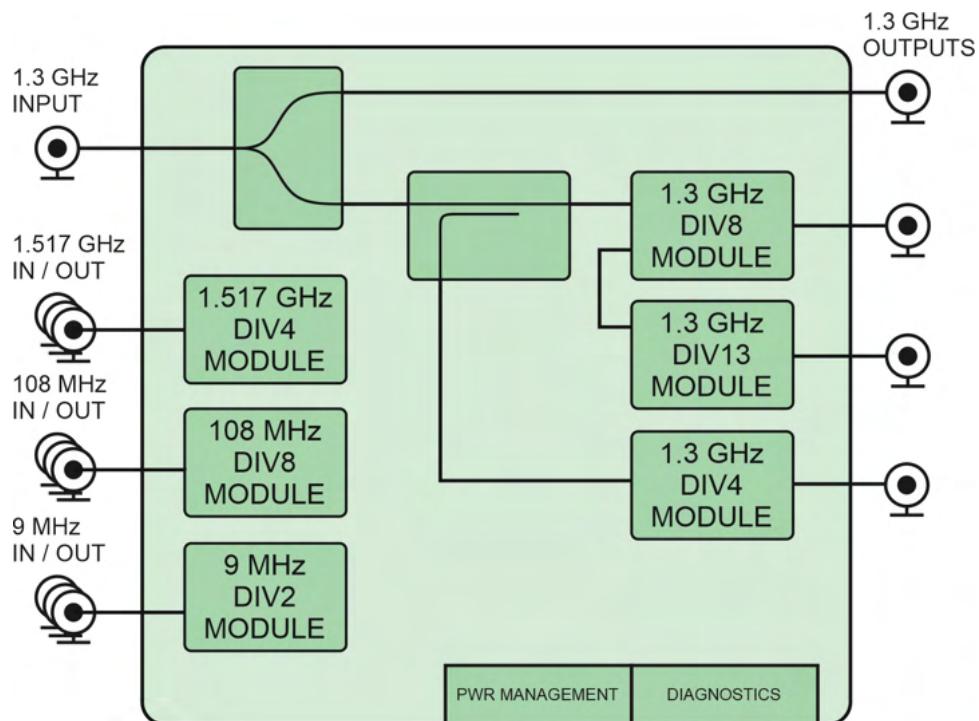


Figure 69: FLASH DISM block diagram.

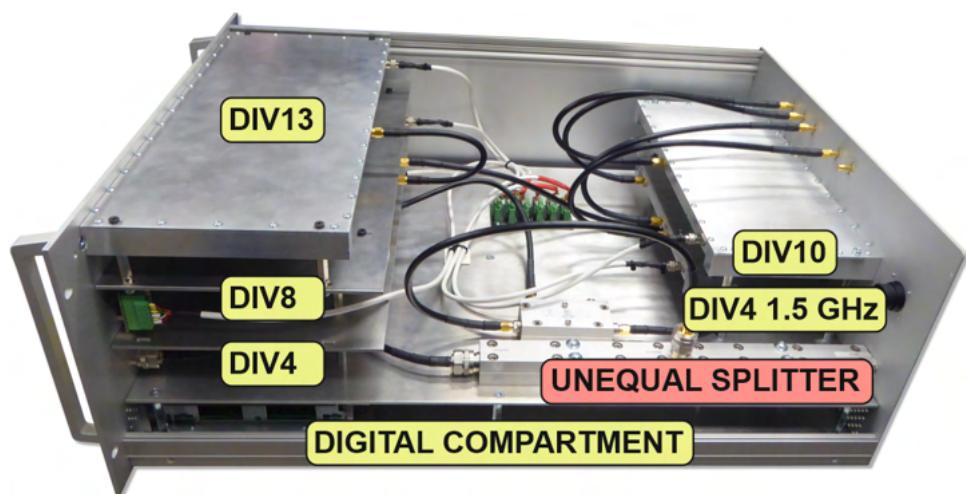


Figure 70: Internal view of new FLASH DISM module.

The high power 1.3 GHz signal from MO output is delivered to the DISM input and to the internal, commercial unequal power splitter that delivers high power output to the front panel of the DISM. The second output of the unequal splitter output feeds the coupler and the main, custom-made multi-output power splitter devices. Reference

signals of other frequencies are routed directly to corresponding custom power splitters. All the modules are power supplied and managed by DESY common devices - already mentioned FRED and TMCB modules.

5.4.1 Structure selection, simulation, and prototyping

DISM had to provide more than 20 RF outputs at a minimum of +20 dBm, therefore DISM power splitters at 1.3 GHz have to work with high power input power level (+44 dBm approx.). To design a robust solution extensive tests on prototypes had to be made. Several tests were conducted, including testing the SMA connector assembly, described in Appendices. The power splitter structures had also to be designed exclusively for the design. Due to the high power input and low thermal impact on phase shift introduced by the splitters the planar Wilkinson-type power splitters were chosen. Two and three output power splitter prototypes were calculated [95] and then simulated and optimized to achieve the best performance. Two output structures were designed as multistage to extend the operating bandwidth and make the final tree structure easier to match at all outputs. The structures were tested for insertion loss, and matching, but also for a temperature change under full power operation. All the tests were positive, introduced losses were approx. 0.2 to 0.3 dB above the ideal and under full power operation splitters were not hotter than +50 degrees Celsius. Prototype splitters are presented in Fig. 71. Test results are presented in Fig. 72, and Fig. 73.

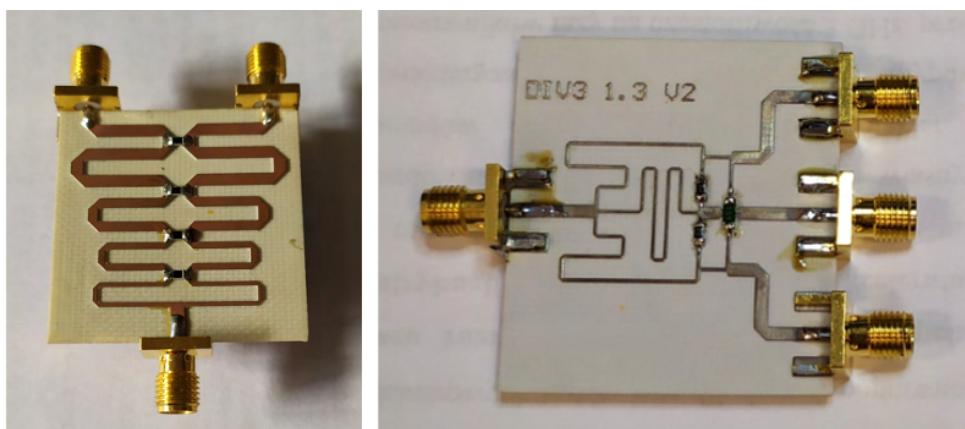


Figure 71: Prototype structures for DISM custom power splitters.

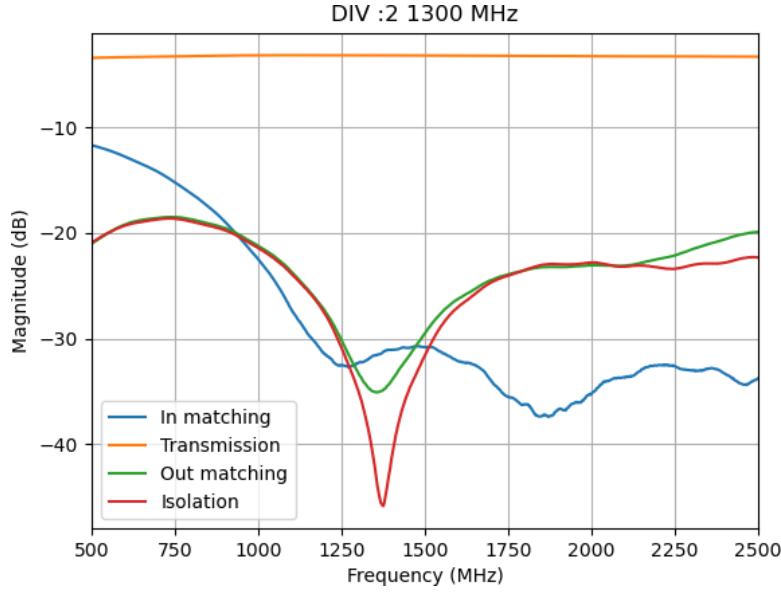


Figure 72: Prototype 2 output splitter scattering parameters. Input at port 1, outputs at ports 2 and 3.

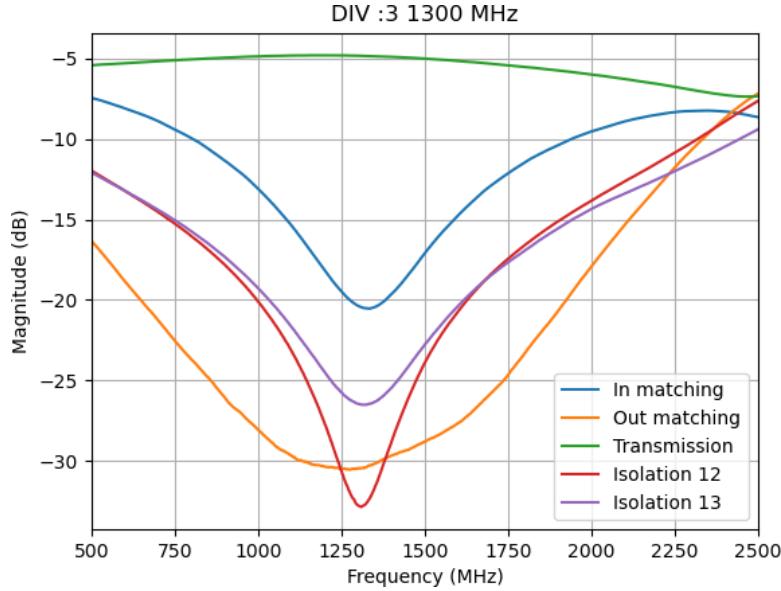


Figure 73: Prototype 3 output splitter scattering parameters. Input at port 1, outputs at ports 2,3 and 4.

The achieved results are very good. For the two output splitter structure, the insertion loss is about 3.2 dB, matching the input and outputs at 1.3 GHz is better than 30 dB. After 12 hours of operation under full power input signal, the temperature of the structure at its hottest point was approx. +50 degrees Celsius. The results for the 3 output structures

are not as good as for the two outputs and this is because the structure was optimized for the multi-output final designs and therefore is intended to work as a middle splitter in the splitter tree structure.

5.4.2 Temperature and humidity stable power splitter modules for DISM

Final power splitter modules for DISM are presented in Fig. 74.

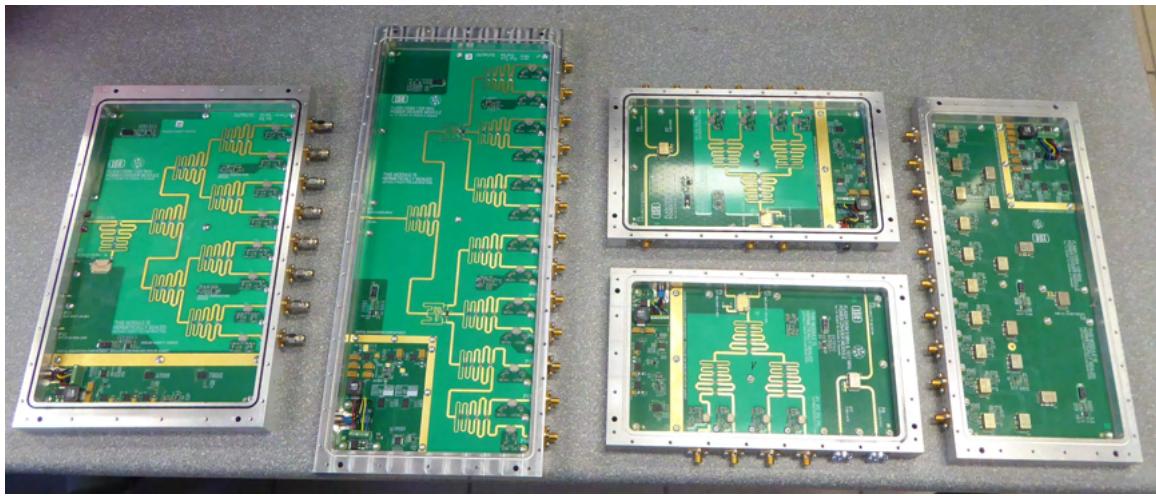


Figure 74: Custom high power hermetic power splitter modules for DISM. Starting from the left: DIV8, DIV13, 2x DIV4, and DIV108.

In total 4 different designs of power splitters were made. The DIV8 is a main power splitter that works with a +44 dBm input 1.3 GHz signal. It provides eight +26 dBm 1.3 GHz outputs and delivers power to the DIV13 module, with a similar structure, but designed for more outputs. Since the designed 2 output power splitters are wideband, the DIV4 module works with 1.3 GHz and 1.517 GHz signals, which is why two modules per DISM are used. DIV4 module also hosts a simple resistive splitter for a 9 MHz signal. DIV108 module provides 10 outputs at 108 MHz and is made using commercially available transformer power splitters - microstrip power splitters at 108 MHz are impractically large.

Every output of the power splitters (except the 9 MHz branch) is fitted with an analog reflectometer circuit that constantly monitors forward (output) and reverse (returning or reflected) signals. Such an approach provides all the diagnostic information - the output power level and rough information about output VSWR - if it's too large an alarm is

raised by the controlling TMCB module. All the modules are equipped with one or more 16-output 16-bit ADC to monitor all the important voltage levels and transmit them back to the controller via I2C. Every module is equipped with an I2C switch circuit that assigns a main I2C address for every power splitter in the DISM, therefore there is no problem with too small I2C address space. Placing the ADCs inside the power splitters allowed to reduce the total cabling inside the DISM box - every module is connected only to the power supply and I2C via a single hermetic circular 6-pin connector. Modules are enclosed in custom-made hermetic housings (design methodology described in Appendices).

5.4.3 DISM 19 inch module

The internal layout of the DISM 19" module is shown in Fig. 70. It is a result of a deep analysis of the existing box - similar in function - the distribution module for European XFEL. Its internal structure was not properly analyzed and therefore the result was a significant number (more than 50) of RF cables, DC power cables, and tens of SMA feed-throughs per box. After analysis of the existing design following requirements were stated for the new design for FLASH:

- DISM 19" module must not be higher than 5U.
- To reduce the required number of RF cables and SMA feed-throughs all the power splitters should be attached directly to the front and rear panels.
- Digital components (TMCB, FRED) and their cabling should be located in a separate, shielded compartment.

To further simplify the design and further maintenance it has been decided that all the modules should use the same diagnostic circuitry and communication protocols. As a result, a DISM 19" module is divided into two separate compartments. The bottom compartment hosts all the digital and control circuits and their cabling. All the power and control cables for the power splitters are routed via a central crossbar board. Power splitters are connected with 6-wire cables to the crossbar board, which provides +7V DC and I2C communication. The RF power splitters are attached to the front and rear panels. They are also vertically spaced, to keep free space for future upgrades of thermal stabilization. In total, the FL-DISM module provides 26 outputs at 1.3 GHz, four outputs at 1.517 GHz, ten outputs at 108 MHz, and two outputs at 9 MHz.

5.4.4 DISM test results

Testing of assembled DISM modules included verification of matching and insertion loss of every power splitter. The matching of every connector and insertion loss between input and every output were measured and showed repeatable and expected results. The test procedure included also the verification of the diagnostics. Each module responds with all the reflectometer power detector readouts and internal temperature and humidity sensor readouts, and then a text report is generated as shown in Fig. 75.

ADC1	CH	DIV_OUT	PANEL	DESC	VALUE	READ
	CH 0	RET1	P44		0.63	
	CH 1	FWD1	P44		0.75	
	CH 2	RET2	P45		0.66	
	CH 3	FWD2	P45		0.81	
	CH 4	RET3	P46		0.65	
	CH 5	FWD3	P46		0.81	
	CH 6	RET4	P47		0.66	
	CH 7	FWD4	P47		0.79	
	CH 8	HUM	XX		0.45	
	CH 9	TEMP	XX		0.70	
	CH10	XX	XX		1.02	
	CH11	XX	XX		1.02	
	CH12	XX	XX		1.02	
	CH13	XX	XX		1.02	
	CH14	XX	XX		1.02	
	CH15	XX	XX		1.02	
ADC1 Temperature : 27.09 deg C						
Temp and Hum Sensor HDC						
Temp: 28.33						
Hum: 4.79						

Figure 75: Sample report, generated from DIV4 in DISM.

Matching and insertion loss of DISM DIV modules (example of DIV8 modules and 1.3 GHz ports) are presented in Fig. 76, and Fig. 77.

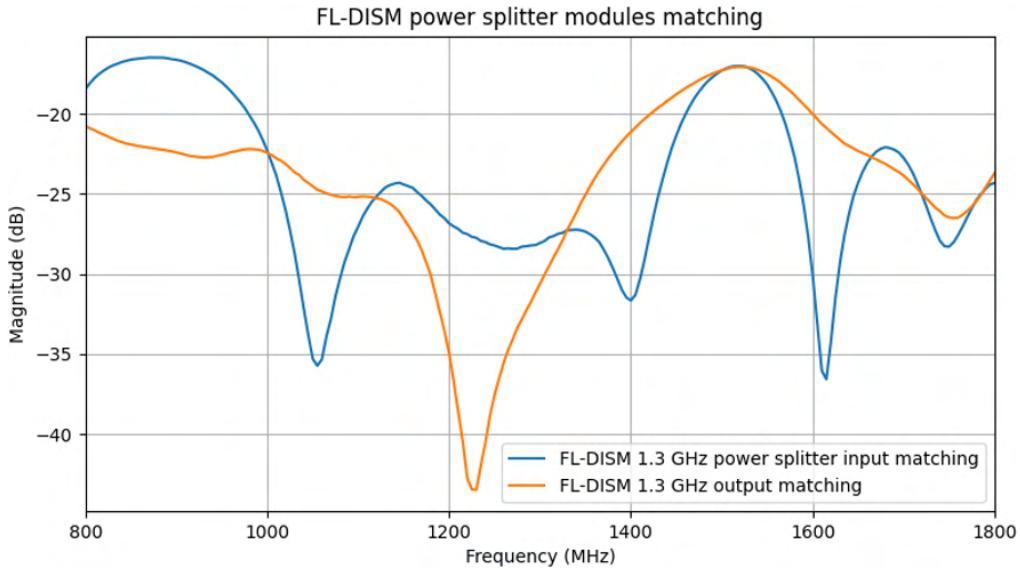


Figure 76: Matching of input and output 1.3 GHz ports in DIV8 module of DISM.

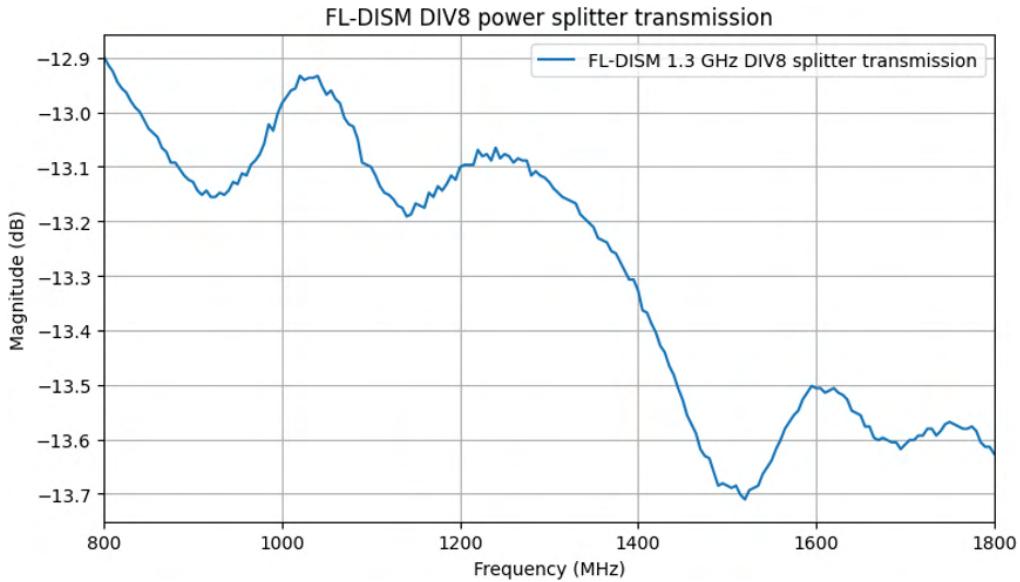


Figure 77: Transmission between input and output at 1.3 GHz inDIV8 module of DISM.

Achieved matching is very good and ensures that no significant reflections of the 1.3 GHz reference signal are caused by the DISM module. Insertion loss of 13.1 dB is close to the ideal value of 12 dB, and the difference of 1.1 dB is caused by the transmission lines in the DIV8 module and an additional 0.2 dB added above the ideal 3 dB by each of the power splitting structures.

5.5 FLASH2020 Frequency Conversion Module

The last of the newly designed modules for the FLASH2020+ PRDS upgrade is the frequency conversion module FLASH FCM. It is realized as a 19" box, 3U high, shown in Fig. 78.



Figure 78: FLASH Frequency Conversion Module (FCM).

The function of the FCM is to convert the input 1.3 GHz reference signal to low phase-noise 108.(3) MHz and 9 MHz signals, further distributed via DISM. The internal block diagram of the FCM is shown in Fig. 79.

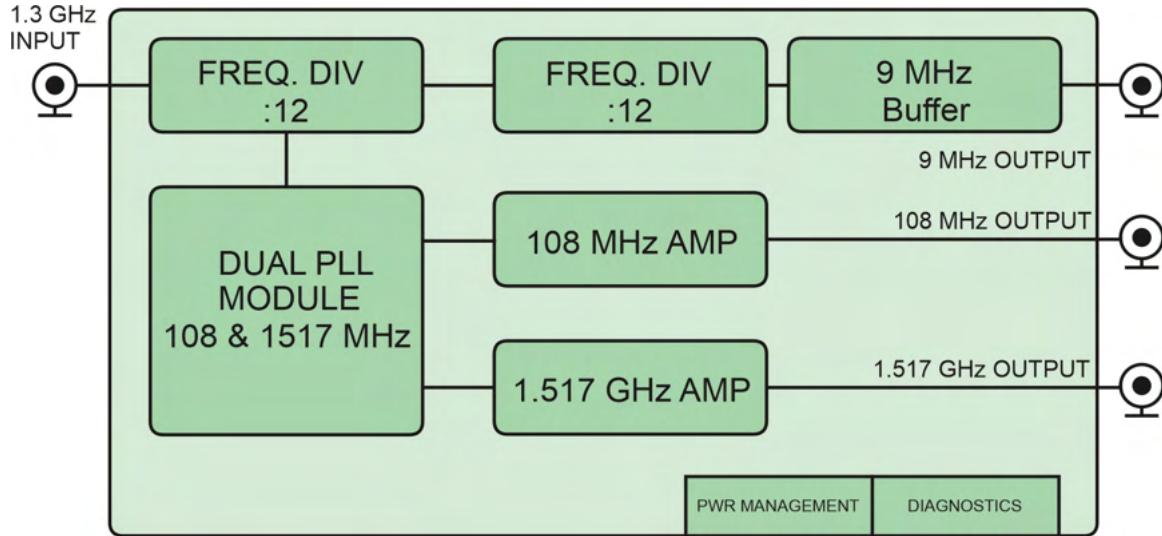


Figure 79: FLASH Frequency Conversion Module block diagram.

The FCM is based on an upgraded design of the E-XFEL FreqDiv module. The new design is more universal, as it lacks the conditioning circuits, and rather provides broadband outputs that may be fitted with external amplifiers and filters. The new module is also significantly smaller, but the most important changes are the implementation of an input interlock and a dedicated resetting circuit, designed exclusively for the FLASH timing system. The input interlock circuit constantly monitors the input power level and if an insufficient input signal power level is applied the whole frequency divider unit is kept in reset, and unlocking is possible only if a high enough (hysteresis) signal is applied to the input. The new design of the frequency divider, called frequency divider module (FDM) is shown in Fig. 80. Thanks to its universal character it may be easily used in other applications. Two FDM modules are used to synthesize 108.(3) MHz and 9 MHz signals. 9 MHz signal is then conditioned in a custom buffer amplifier that is able to deliver 0-5V square wave at 50 Ohm load. Synthesized 108.(3) MHz signal is used as a reference for a Dual-PLL module (designed by Bartosz Gąsowski, the author has proposed the antivibration solution, housing concept, and design) that synthesizes low phase noise 108.(3) MHz and 1517 MHz signals. The module is based on two independent PLL circuits. The 108.(3) MHz circuit is based on an ultra-low phase noise OCXO, which due to its high vulnerability to vibrations must be mounted on spring dampers. The 1517 MHz signal, which is less important, is synthesized with a PLL based on a surface mount oscillator. The used synthesis scheme for 108.(3) MHz allowed to avoid the use of frequency dividers

in the PLL feedback loop and thus, use the full potential of the OCXO used, especially in close to carrier range. A picture of the Dual-PLL module is shown in Fig. 81. The output 108.(3) MHz and 1517 MHz signals are then amplified using a third party low phase-noise power amplifiers and routed to the output ports of the FCM 19" box.

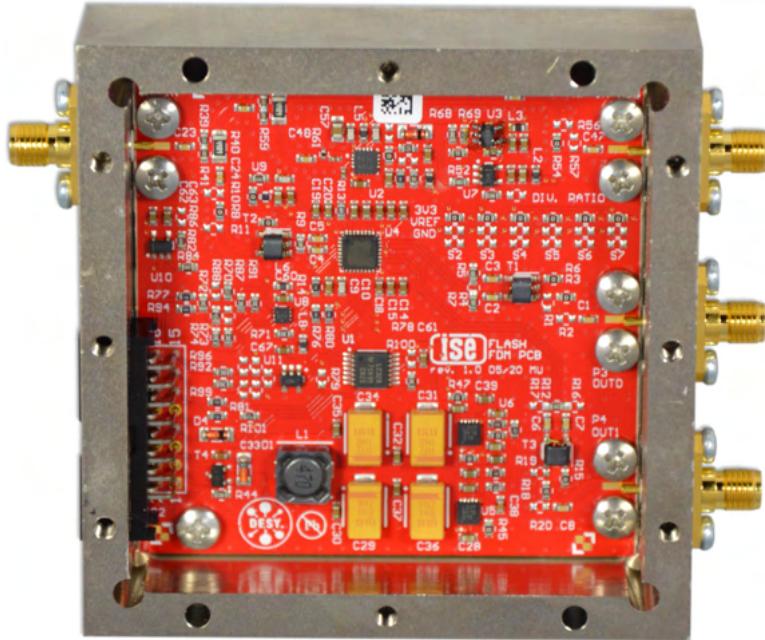


Figure 80: FLASH Frequency Divider Module.

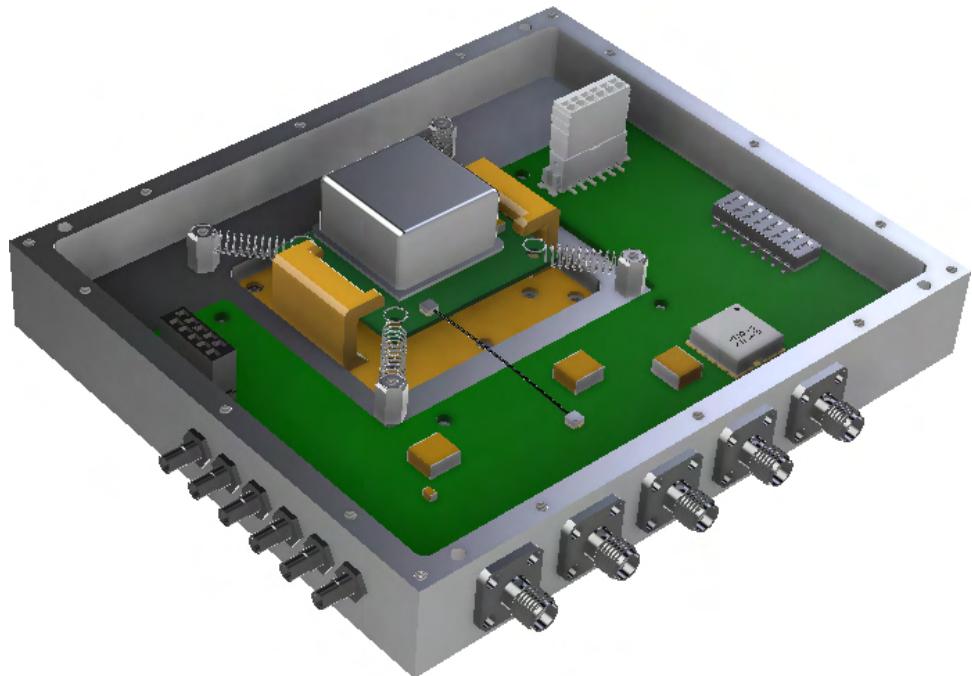


Figure 81: FLASH FCM Dual-PLL module.

5.5.1 Test results

The most important test results for the FCM boxes are the phase noise power spectral densities of 108.(3) MHz and 1517 MHz reference signals, synthesized by the module. The achieved results are compared with similar signals, synthesized by an old version of the FLASH PRDS. Corresponding plots are shown in Fig. 82, and Fig. 83. The integrated jitter for comparison is presented in Table 6.

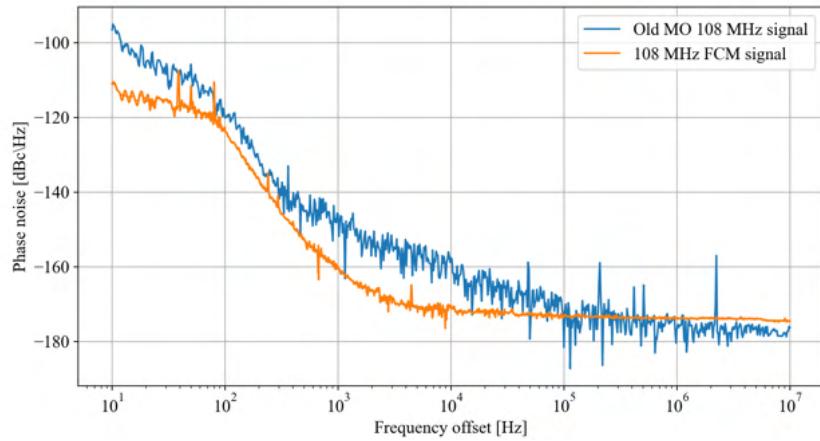


Figure 82: 108.(3) MHz phase noise PSD plots for old and new FLASH PRDS.

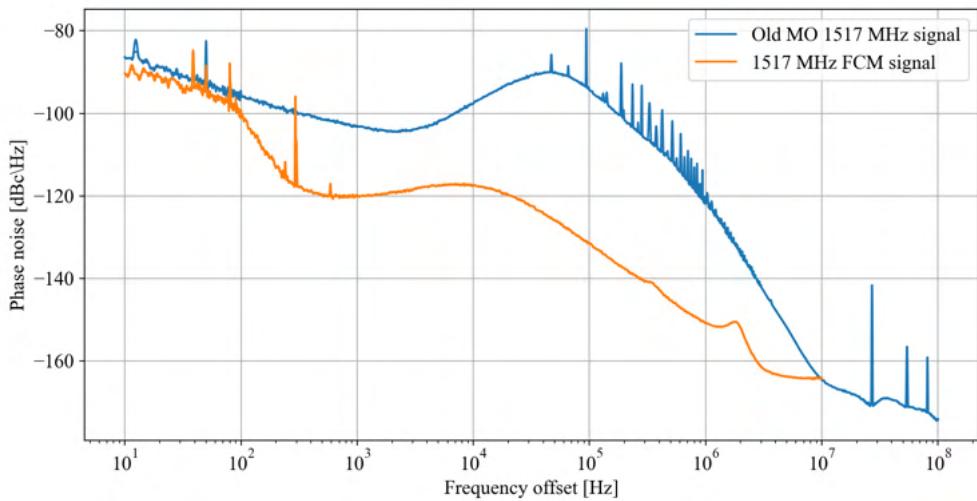


Figure 83: 1517 MHz phase noise PSD plots for old and new FLASH PRDS.

Table 6: Comparison of 108.(3) and 1517 signals phase noise PSD synthesized by old FLASH MO and new FLASH PRDS

Integrated jitter from 10 Hz to 1 MHz carrier offset			
	Old FLASH MO	New FLASH PRDS	Improvement ratio
108.(3) MHz	86.1 fs	27.8 fs	3.1 x
1517 MHz	1390 fs	45.8 fs	30.3 x
Integrated jitter from 1 kHz to 1 MHz carrier offset			
	Old FLASH MO	New FLASH PRDS	Improvement ratio
108.(3) MHz	6.3 fs	4.4 fs	1.4 x
1517 MHz	1.39 ps	35.9 fs	38.7 x

An explicit improvement is visible for both signal frequencies, and of particular importance is the effect of 108.(3) OCXO in the range from 10 Hz to 100 kHz offsets from the carrier.

6. Interferometric link prototype for 162.5 MHz PRDS

In 2021 a WUT internal project was granted to provide a working prototype of a single interferometric link for a 162.5 MHz PRDS. The author's contribution is the complete prototype design and coordination of prototype realization, done by Andžej Šerlat. This part describes the link prototype design concept, points out the key aspects of the design, and presents the realized prototype and test results.

6.1 Prototype link design

The design is based on an interferometric solution, proposed by Chase and Cullerton [78]. The idea is to send a reference signal via a transmitter module through interferometric loops. The transmitter begins and ends each loop, monitors and stabilizes the phase difference introduced by the loop, and creates the reflected signal. Each receiver (multiple receivers may be connected to a single interferometer loop) samples both the forward and reflected reference signals and performs a vector sum in a combiner circuit, as illustrated in Fig. 84. For the prototype link the 162.5 MHz part was verified in a system presented in a block diagram in Fig. 85.

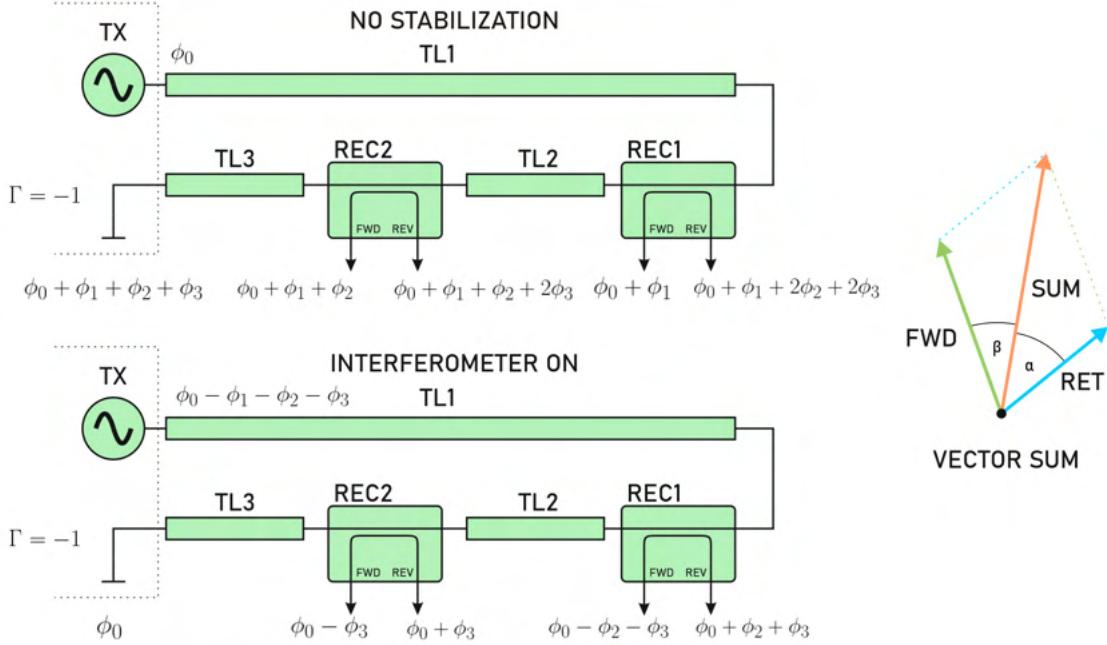


Figure 84: Principle of operation of an interferometer-based phase stabilization link.

For a complete description of the principle of operation of an interferometric phase stabilization link, two cases need to be analyzed. [50, 78, 79]. First, under no stabilization, and second when the phase stabilization is active. When interferometric stabilization is disabled a reference signal is transmitted by the TX (transmitter) to the interferometer loop, made of (in the described example) two receivers and three transmission lines. Each line introduces its phase shift and phase drift (for simplicity both modeled as ϕ_x , where x stands for the line number in Fig. 84). A reference signal propagates through the loop and is probed in the forward direction by the receivers. Then at the end of the loop, the signal is reflected (for simplicity the 180-degree phase shift is omitted as it is a systematic component) and goes back to the loop, where it is probed in the reverse direction by the receivers. Receivers perform a vector sum of both forward and reverse signals, producing an output signal. When no stabilization is active in the loop that output signal is not phase stable. In the second case, when the stabilization is active, the signal reaching the short at the end of the loop is probed by the transmitter module and a proper phase correction is applied. Thus the TX output signal with active stabilization is $\phi_0 - \phi_1 - \phi_2 - \phi_3$. By going through the loop contributions of each transmission line are compensated and the signal is then reflected to the receivers. As a result, the vector sum is phase stable. Two critical conditions must be met to make the described circuit

work. First - the transmitter module must provide constant phase change between the end of the loop. The second critical condition is to ensure that both signals reaching the combiner in the receiver module are equal in amplitude and the receiver is calibrated in the optimal position. An optimal position is a case when the phase difference between the forward and reverse signals is close to zero or 180 degrees - then the phase drifts do not change the total phase change of the phase stable output signal of the receiver. The detailed block diagram of a prototype interferometric link is shown in Fig. 85.

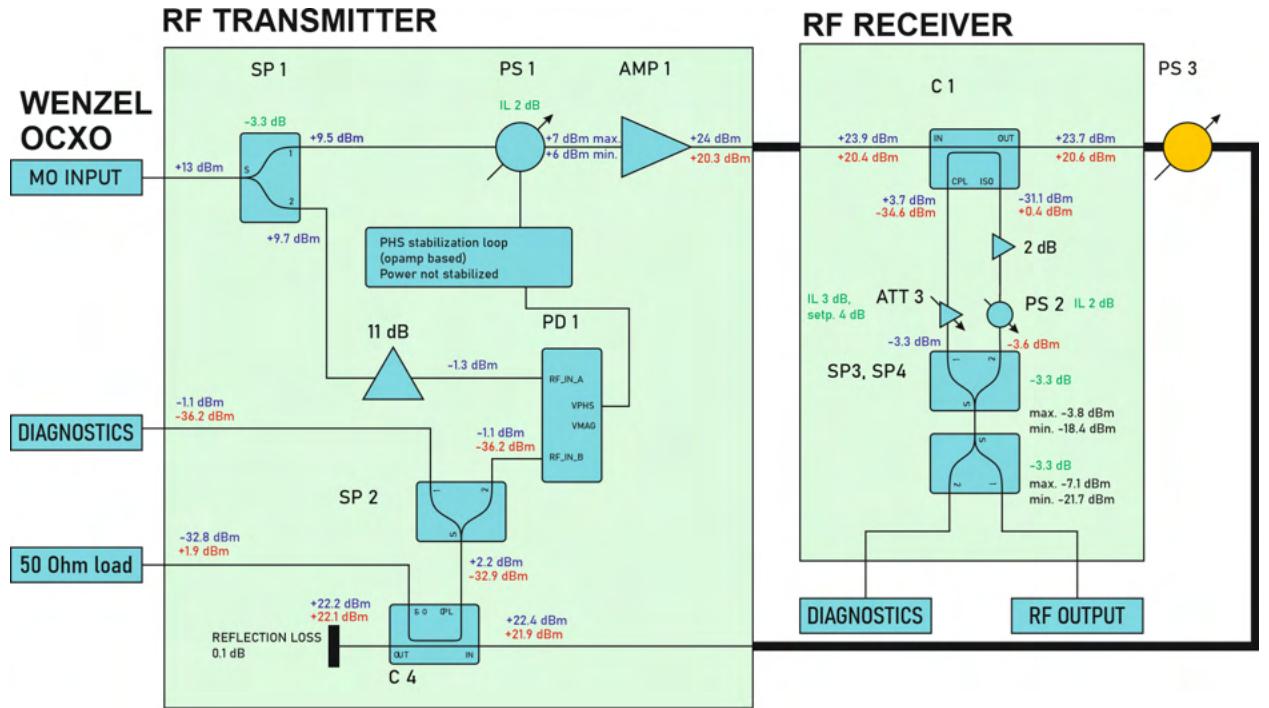


Figure 85: Prototype interferometric link working at 162.5 MHz.

The prototype link is made of a single transmitter and a single receiver module, connected using a 10 meter long RG58 coaxial cable. Part of the reference signal is used to monitor the phase difference (and change) introduced by the loop (function of PD 1 phase detector). The other part of the reference signal is routed via a phase shifter (phase actuator in the transmitter) to the RF amplifier for power gain and isolation of the reverse signal. The reference signal is routed via RF cables to the receiver module and then back to the transmitter, via an optional (yet recommended) phase shifter PS3, which is used to simulate drifts but also to set the optimal setpoint for each of the receivers in the loop. The receiver probes forward and reverse reference signals, adjusts their amplitudes, and performs vector sum, thus creating a phase-stable output signal.

The impact of subcomponent parameters on the overall phase compensating performance was analyzed. To meet the second requirement both forward and reverse signals must be adjusted in amplitude. The reverse signal in the worst case may be attenuated almost two times more than the forward signal, which leads to two potential problems that have to be taken into account when designing interferometric phase compensation links. The first one is the introduced attenuation of the RF cable in the loop - big attenuation will lead to a significant reduction of reverse signal power. This will attenuate the forward signal in the receiver as any additional amplifier will introduce its phase drifts that will not be able to compensate. The final result will be a low power level at the output of the receiver. The second, more important effect, is the finite value of directivity of used couplers. The problem is related to the first one. Not only does the big attenuation cause the low reverse signal, but the finite directivity introduces a forward leakage signal that will interfere with the reverse signal in the receiver. Couplers with poor directivity (experimentally selected limit is 30 dB) will lead to a significant reduction of phase drift compensation in the receiver. Both effects were simulated (based on simulations done by D. Sikora for E-XFEL) and their impact on the total achievable suppression factor (ratio of phase change in the main interferometer loop to the phase change at the output of the receiver module, compared to the transmitter input signal). Results for a 50 meter long cable are presented in Fig. 86, Fig. 87, Fig. 88, and Fig. 89.

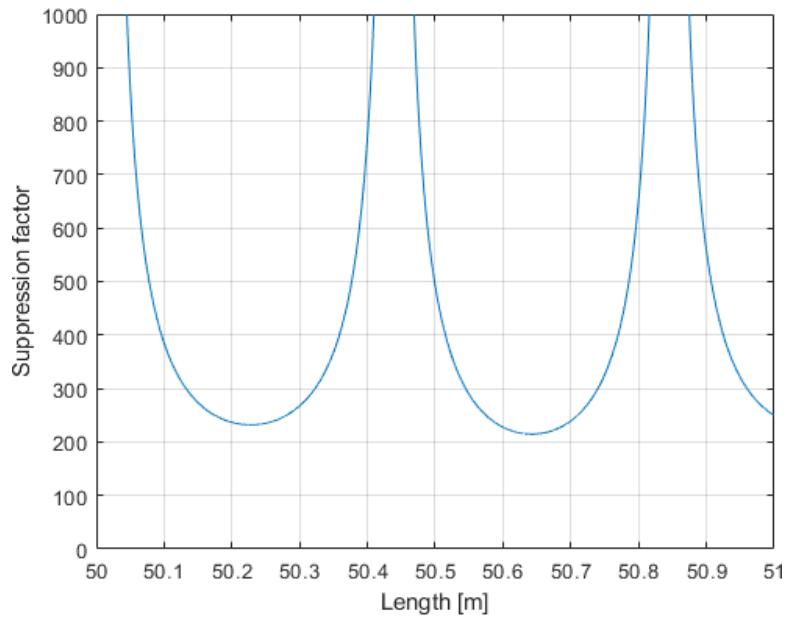


Figure 86: Interferometer loop coaxial cable attenuation impact on the suppression factor of the phase drift compensating link. Cable introducing 1 dB per 100 meters length.

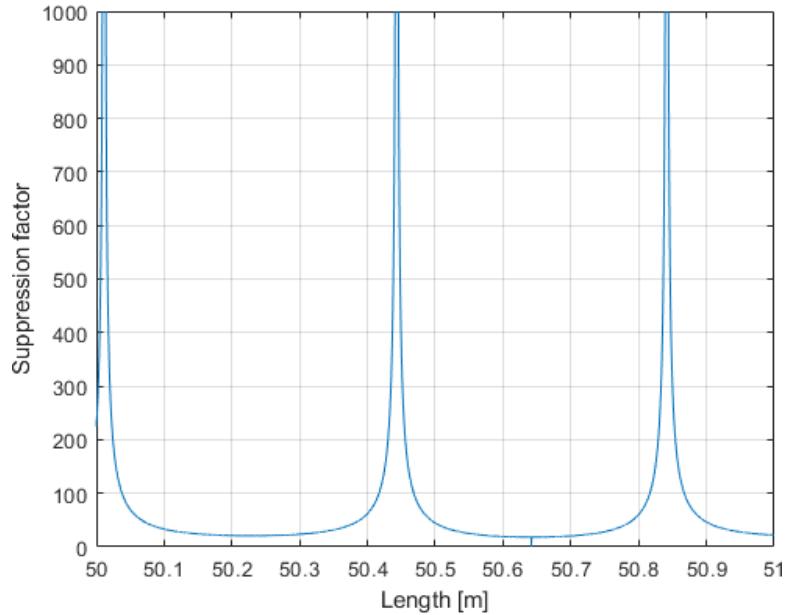


Figure 87: Interferometer loop coaxial cable attenuation impact on the suppression factor of the phase drift compensating link. Cable introducing 10 dB per 100 meters length.

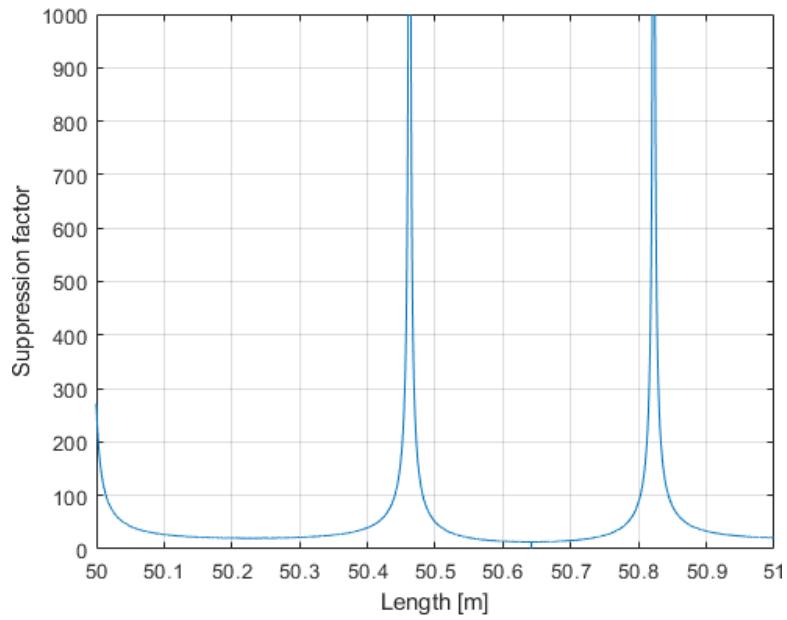


Figure 88: Interferometer loop coupler directivity impact on the suppression factor of the phase drift compensating link. Directivity = 20 dB.

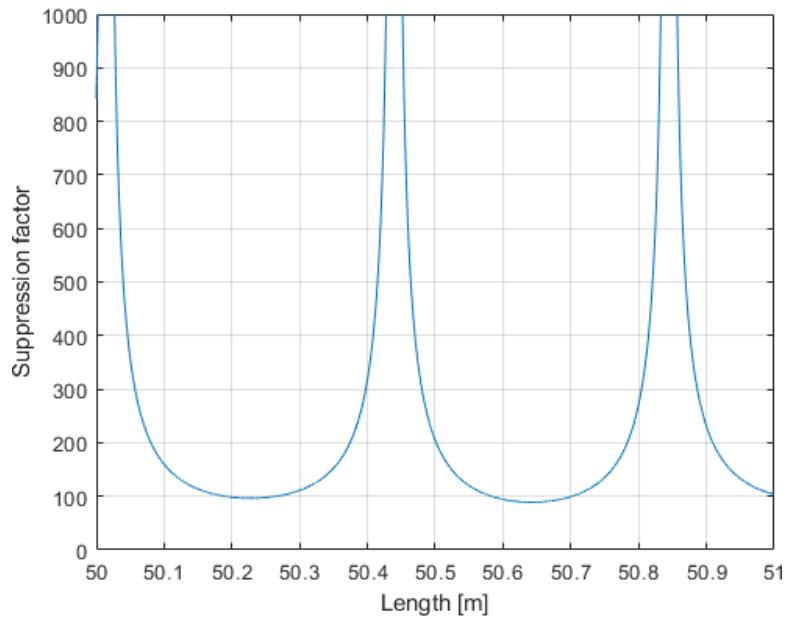


Figure 89: Interferometer loop coupler directivity impact on the suppression factor of the phase drift compensating link. Directivity = 35 dB.

The presented simulation results show that both RF coaxial cable attenuation and couplers' directivity are key parameters that limit the total performance of the phase compensating link. For higher attenuation and lower directivity values, the total suppression factor plots show that the peaks of SF (suppression factor) are narrower and the floor level of SF is lower. Peaks in the plot represent the optimal setpoints for the receivers - harder to calibrate and maintain the calibration for narrow ones. The lower floor level means that when the system is out of calibration the provided phase suppression is poor. The need for low attenuation cables (meaning large cross-section coaxial cables) and very high directivity couplers are required.

6.1.1 Prototype realization and test results

Both transmitter and receiver prototypes were done as two 19" 1U boxes, presented in Fig. 90, and Fig. 91.

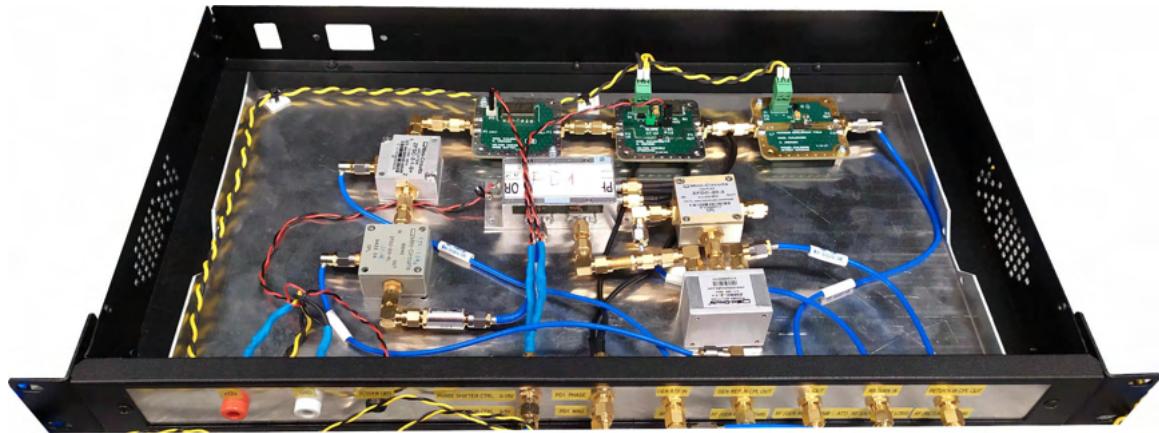


Figure 90: 162.5 MHz interferometer transmitter prototype.



Figure 91: 162.5 MHz interferometer receiver prototype.

The author has developed a measurement program and the testing was done by Andzej Serlat, in a custom-made LabView-based application. One transmitter and one receiver were used to assemble an interferometric link. Instead of a long RF cable an external mechanical phase shifter was used to simulate the phase drifts introduced by the cable. The results are presented in Fig. 92. Then the 10 meters long RG-58 coaxial cable was used as a phase drift source and the external phase shifter was used as a calibrating element, to set the optimal operating point for the receiver. The results are presented in Fig. 93.

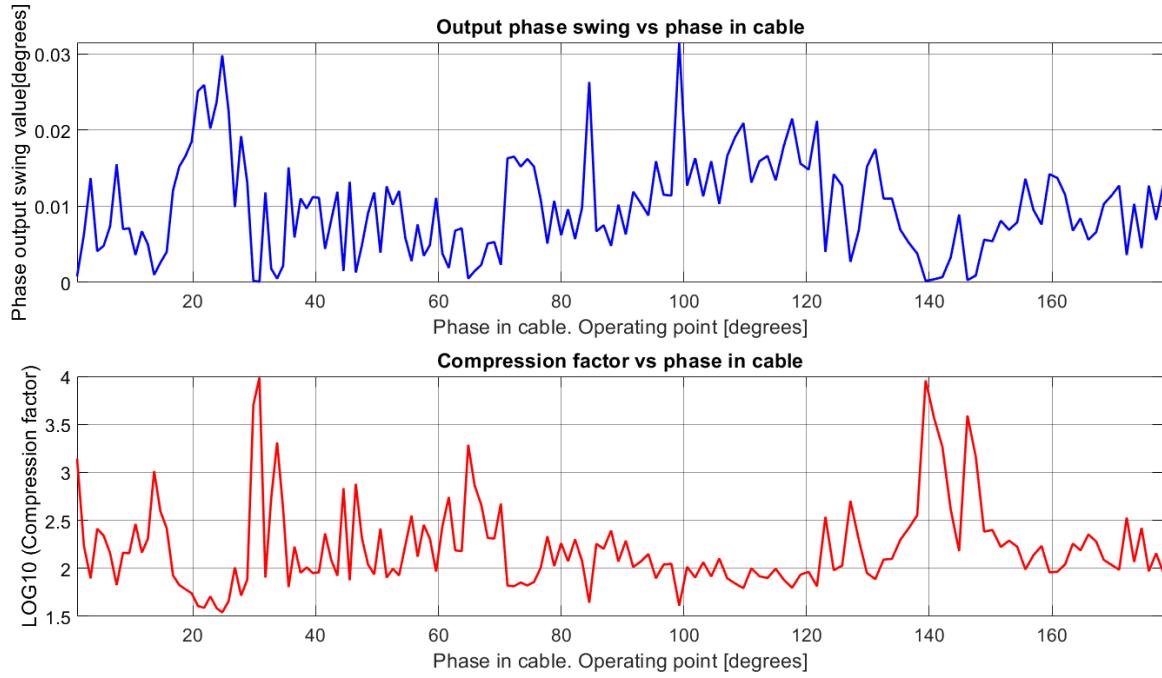


Figure 92: Suppression factor and optimal RF cable lengths for interferometer loops.

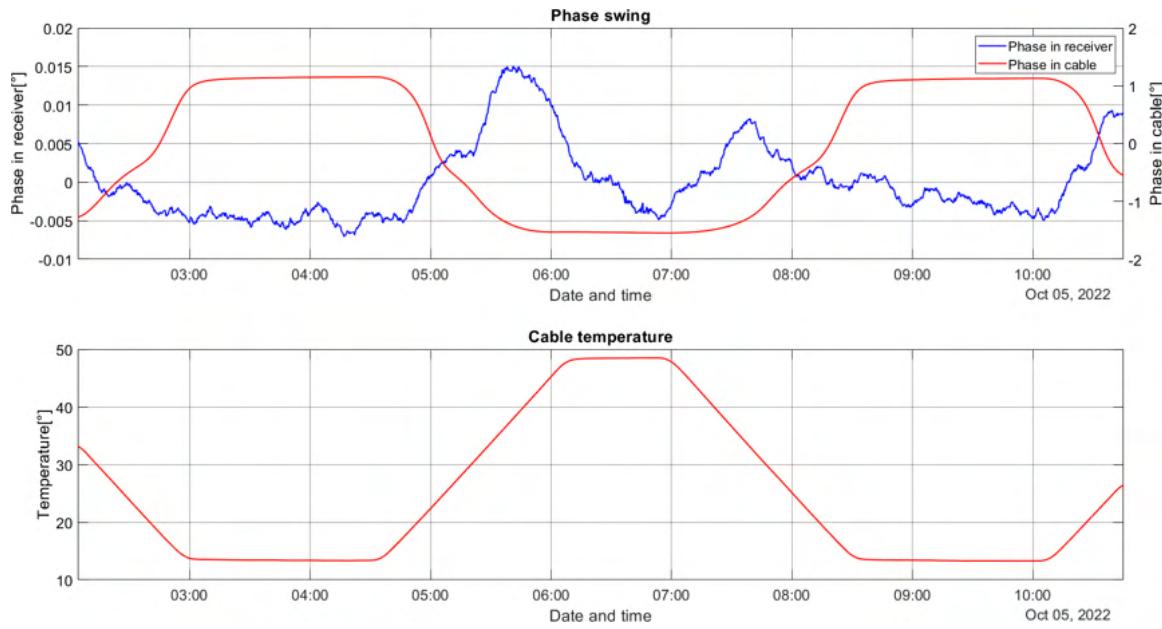


Figure 93: Phase change at the interferometer receiver output vs phase change in the interferometer loop cable and the temperature vs time plot.

The measurement and simulation results are similar. In both cases, the explicit peaks of the suppression factor and floor range are observed. Peaks are spaced regularly, approx. every 90 degrees. Only two peaks are presented, due to the limited phase adjustment range introduced by the mechanical phase shifter. Peak values of suppression factor exceed 1000 x, yet in most cases, it is possible to maintain the suppression level at least of 100 x at floor level, which is far simpler to calibrate than the peaks. The presented test results prove that the design concept is correct, realized simulations pointed out the most critical aspects of the design. The realized prototype is a good starting point for the future development of phase reference distribution systems, working with the base reference frequency of 162.5 MHz.

7. PRDS components for SINBAD

The chapter describes all the modules and research done during work on the development of the SINBAD phase reference distribution system. The general requirements are described, including the required system topology and principle of operation, based on interferometric phase compensating links. Work done included a complete design of a coaxial cable network for ARES, a temporary coaxial distribution design that uses the designed final cabling concept and is successfully installed in ARES, and all the research that the author has conducted to verify the possible and achievable performance of analog-based interferometer design. The chapter is finished with a description of the prototype interferometer link modules, the transmitter, and the receiver that the author designed and manufactured. The modules were under test at the moment of writing the thesis and are planned to be finished in 2023.

7.1 PRDS system requirements and concept

The requirements for the PRDS in ARES were based on the bunch arrival time jitter requirements. In ARES, working with the 2.998 GHz RF reference signal the short-term bunch time arrival jitter should be better than 10 fs, which corresponds to approx. 0.01 degree. Another requirement was to use the interferometric phase compensation scheme, at the time verified in DESY in E-XFEL prototype [79]. The key problems that were addressed during the conceptual phase. First of all, a long-term jitter of 10 fs requires that the phase drift introduced by the PRDS should be significantly less (less than 5 fs). Such demanding requirement causes that second and third-order effects, which were negligible in E-XFEL or PIP-II prototypes, must be taken into account. First of all the matching of the entire interferometer loop, and all the RF cables, should be kept at a level better than 35 dB, which is almost impossible to achieve in a whole 70 meter long distribution link. Selection of almost perfectly matched components is not enough, as all the RF cables and interconnects must also be matched better than 35 dB, which is impossible. To maintain as low introduced attenuation as possible a 7/8" phase-stable coaxial cable

had to be used. Bigger cross-section cable cannot be used, due to its maximum operating frequency, limited by the cross-section mechanical dimension. Such cables in most cases have corrugated shielding to bend the cable. This shielding introduces impedance distortion, which is presented for LCF38-50J RFS cable in Fig. 94. The periodic distortion of matching is caused by the periodic shielding diameter change and introduced by that change in the standing wave in the measured cable. The presented measurement shows that achieving the required matching of 35 dB is not possible, even if the cable lengths are tuned to perfectly fit the minima of the presented matching plot.

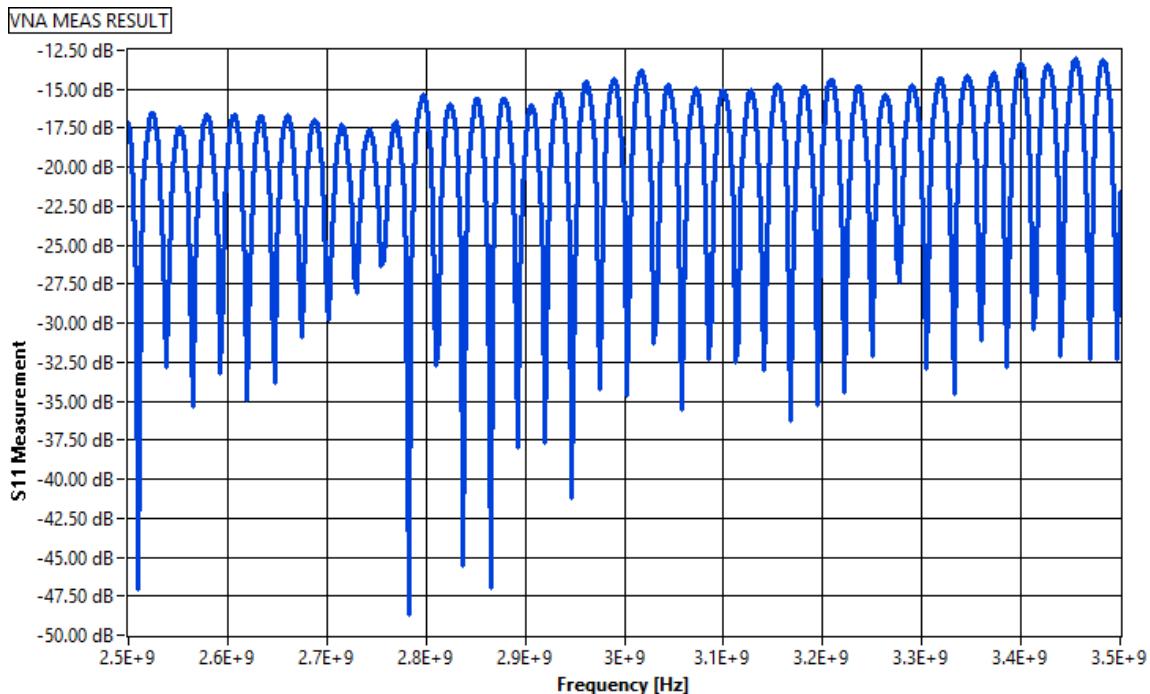


Figure 94: Example matching plot for corrugated shielding 3/8" coaxial cable.

The second requirement necessary to achieve total phase drift in the system less than 5 fs is to use the ultra-high directivity couplers. Required directivity values of approx. 50 dB is not achievable by conventional directional couplers. Couplers should also provide as low insertion loss and as low coupling factor as possible, which are mutually exclusive conditions. The best found (in terms of directivity) coupler was Narda 3022, providing directivity better than 30 dB at 3.0 GHz. There are solutions for planar high directivity couplers [96], yet they were rejected due to the author's experience with these designs, which are very sensitive to temperature change and require tuning in-circuit for each coupler (more than 20 couplers would have to be adjusted at the same time).

The last limitation found is the performance of the phase difference detectors. Both analog and digital solutions were considered the two most important for the interferometric links parameters - the minimum detectable phase difference (further called in the chapter the phase resolution) and a "self-introduced phase drift phenomenon", which is a long-term change of the phase detection signal, caused by the phase detector only. Digital solutions described in the literature [58, 74, 75] show the theoretical resolution of 5 fs, yet the prototype system introduces more than 40 fs phase drift. Furthermore, the analog-based interferometers were already under development in DESY and the author had experience with them [79], therefore it was decided to follow the analog path of phase detection. Analog phase detector circuits of various types were analyzed by the author and the results are described in the chapter. These results may be found very useful for other applications, as they clearly show the boundary of phase resolution than may be reached with these circuits.

The analysis of the requirements showed that it is impossible to meet them. Therefore another approach was taken - it was decided to perform the limitation analysis of the analog phase detectors and then try to realize an analog-detection-based interferometer link prototype that will show the phase drift compensation boundaries. Analysis of the phase detectors and successful attempts of creating new variants of phase detectors was coordinated by the author and realized by two MSc students, Grzegorz Pietrzykowski, and Krzesimir Grajewski. At the time of writing the thesis that analysis was done and the interferometer prototype was under tests and therefore is not fully described in the thesis.

7.1.1 Cabling design

A complete cabling design was designed by the author and Frank Ludwig, DESY. In SINBAD the RF distribution was located in the basement, directly under the ARES linac, as shown in Fig. 95. Cabling was designed to provide interferometric links between the Master Oscillator rack, Laser Injector room, TWS1/GUN, TWS2, and TWS3 racks. The last, the TWS3 rack, was considered an upgrade, therefore the cabling had to provide an RF way to close the interferometer loop at the TWS2 rack. The proposed interferometer layout is presented in Fig. 96 [77]. All the cables used in the system are RFS LCF 7/8" and LCF 1/2", due to size, introduced insertion loss, and maximum operating frequency.

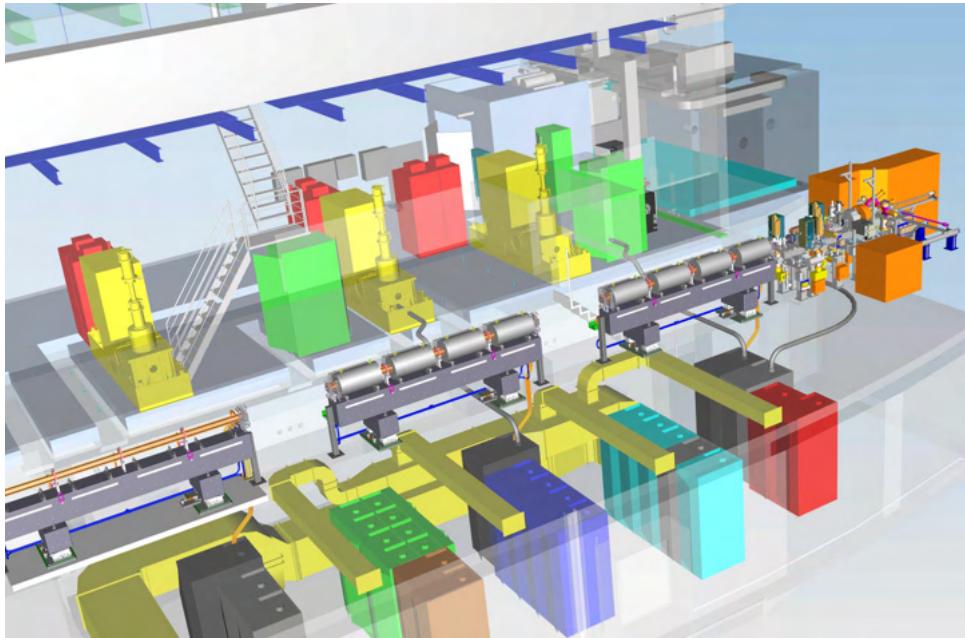


Figure 95: SINBAD basement with the PRDS and LLRF racks and upper ARES tunnel.
Image source: DESY.

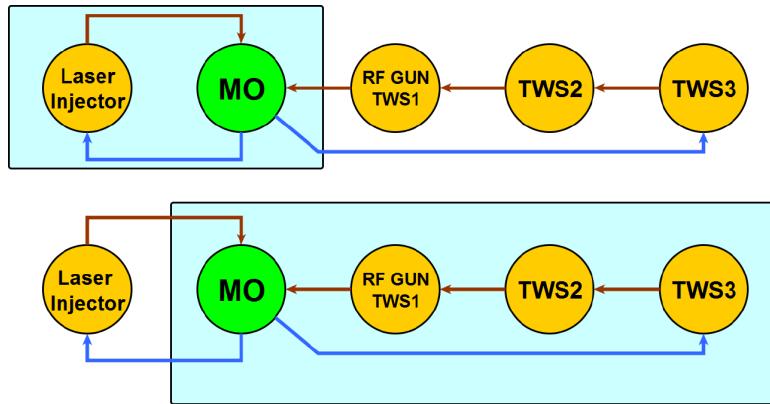


Figure 96: Proposed SINBAD interferometers layout.

The designed cable layout provides all the cabling for the mentioned interferometer links and all potential upgrades. It is also redundant - two sets of interferometer links cables were installed to provide a temporary distribution network and a set of interferometer cables, for interferometric links development that do not disturb the linac operation. The proposed structure of the temporary coaxial cable layout is shown in Fig. 97. The complete cabling diagram is a subject of a non-disclosure agreement and therefore cannot be published in the thesis.

The Master Oscillator in SINBAD temporary PRDS is a Rohde Schwarz SMB100A signal generator, with a high-power output option installed. In the final design, there is a plan to install third-party MO and high-power amplifier (HPA) units. Then the signal from the MO is distributed in the REFM-MO Dummy module, which serves a similar function to the FLASH DISM 19" module, but without any diagnostics. Every endpoint LLRF station (rack) is handled by the REFM-TP0 dummy module, which provides RF reference to the universal local oscillator generation module (UniLOGM, the design is a BSc thesis of the author) and drift compensation module (DCM). All the RF cables are used from the final cabling topology.

SINBAD Temporary RF distribution diagram

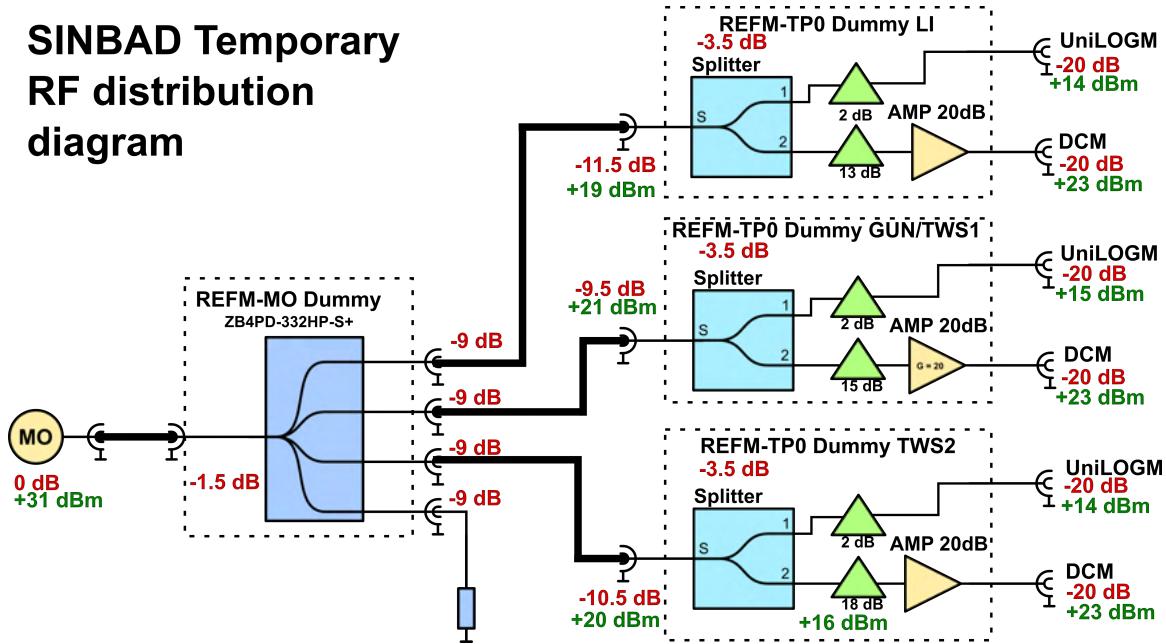


Figure 97: Designed temporary RF distribution for SINBAD.

7.2 Selected analog phase-detection methods and their performance

As already described several different analog phase difference detection methods were proposed and tested for their potential use in SINBAD PRDS. The main motivation is the performance and limitations introduced by the AD8302 chip - the phase detector widely used in phase reference distribution system components designed by ISE.

The AD8302 is a very versatile chip [97], able to detect phase and power differences between its inputs. In PRDS the most widely used functionality is phase detection. The upper-frequency limit described in the datasheet is 2.7 GHz. The author has successfully tested the AD8302 and proved its correct work at 3.0 GHz, but at such frequency, several additional problems arise. The first, and the most obvious problem is the reduction of the dynamic range of the part, presented in the Analog Devices datasheet and Fig. 98. It is clear that with the rise of input frequency, the dynamic range is reduced and cannot be calculated using the datasheet factor of 10 mV per degree of phase difference.

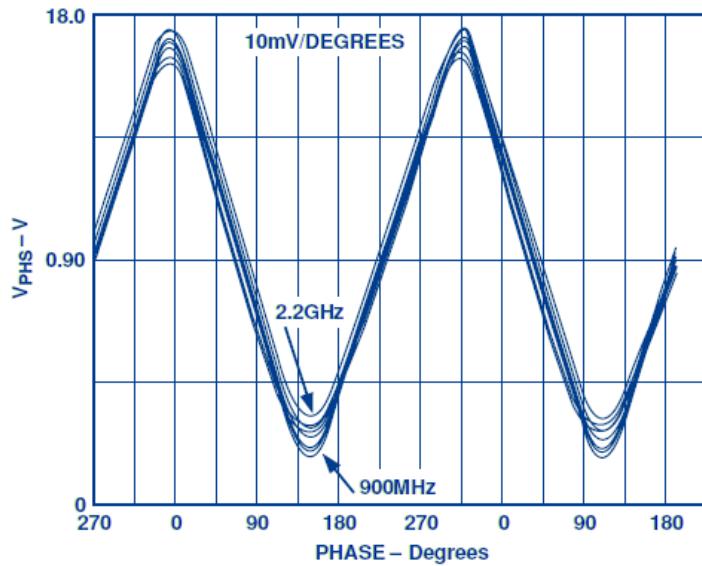


Figure 98: Frequency limitations of AD8302. Source: Analog Devices.

The next problem that the author has investigated is the impact of the input power difference on the phase detection curve of the AD8302. For this purpose, the phase detector was tested with 1.3 GHz and 3.0 GHz signals. In both cases the frequency

difference between the input channels was set to about 1 kHz and the voltage plots were recorded using a Hameg HMO2524 oscilloscope - that is why plots in Fig. 99 are scaled in time units.

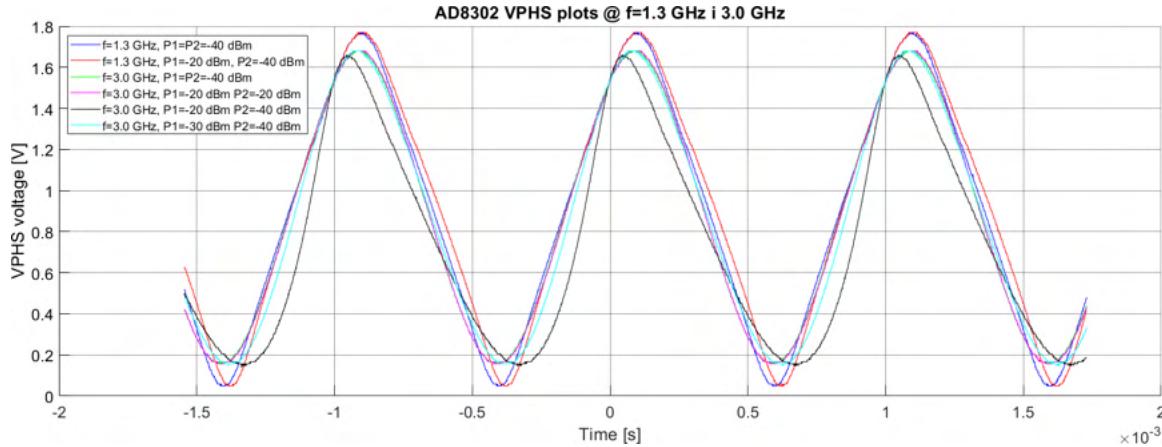


Figure 99: Measured frequency and power limitations of AD8302.

For a 1.3 GHz input signal, it can be observed that the input power level barely affects the shape of the VPHS curve, but when the power difference is big, then a small asymmetry of the curve can be observed. This effect may affect the performance of the phase detection and cause an error. Special care should be taken to ensure that the input power levels for the detector are comparable. For 3.0 GHz frequency, the voltage range is reduced and the output can swing between around 0.2 V to 1.6V. Therefore the scaling factor given by the manufacturer is no longer valid and equals around 8.5 mV/degree. Another important remark refers to the power difference impact, which is significantly bigger for 3.0 GHz signals than for 1.3 GHz and must be taken into account. Furthermore, it is particularly important to correctly determine the slope of detection, as for different input power levels the slopes are not equal.

Finally, the AD8302 is introducing, as many integrated circuits, its long-term drift of the output DC voltage, proportional to the input phase change. This drift is then directly read as a phase drift of a circuit that AD8302 measures, while in fact, its source is the phase detector. The phenomenon was observed by the author and tested in a setup shown in Fig. 100.

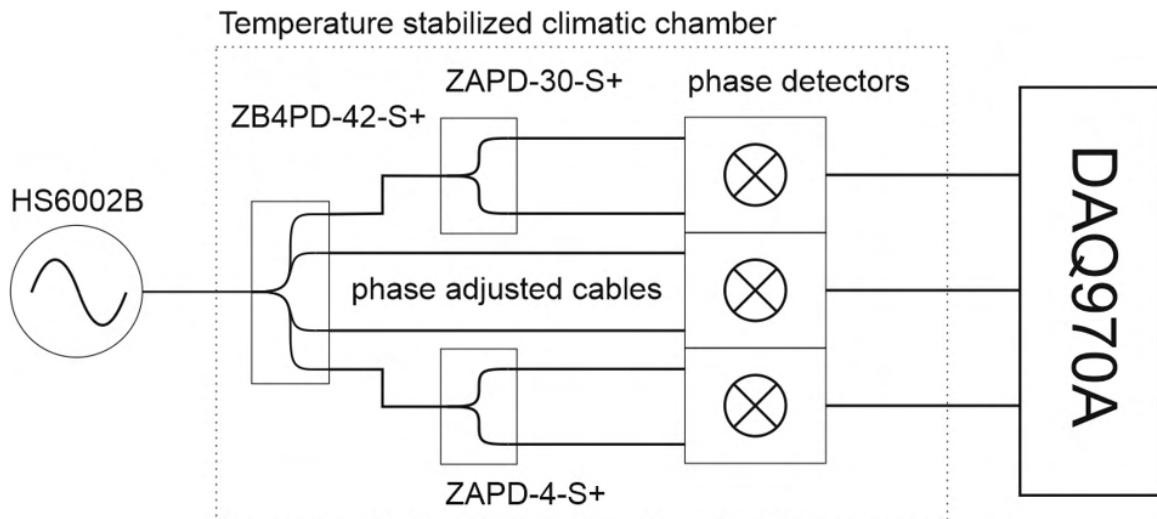


Figure 100: Test stand to measure the self-drift of AD8302.

The 3.0 GHz RF signal from the Holzworth HS6002B generator was routed to a set of power splitters. These power splitters were used to provide constant phase differences to three AD8302 phase detector modules. The operating points were chosen to the middle of the detection range (around 1.0 V) to ensure the detection in the linear range of the detection plot. All the power splitters and phase detectors were kept in a climatic chamber and the internal temperature was stabilized at 41.2 degrees Celsius, to keep the chamber well insulated from the ambient temperature change. AD8302 output voltages were measured using 6.5 digit Keysight DAQ970A data acquisition module, but to exclude its potential impact on the measurement precision the tests were also conducted using a Keysight HP3458A 8.5-digit multimeter, one of the best and most precise multimeters available on the market. Temperature measurement and its trend line are presented in Fig. 101 and measured self drift of AD8302 output voltage (VPHS output) in Fig. 102.

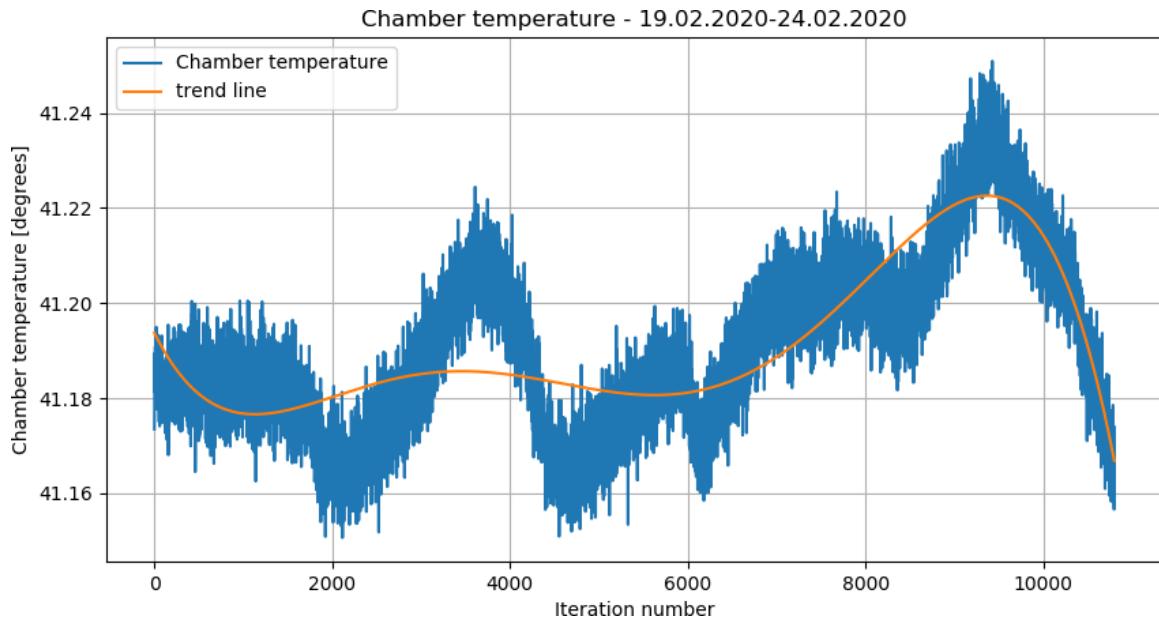


Figure 101: Temperature in the test stand climatic chamber during AD8302 tests.

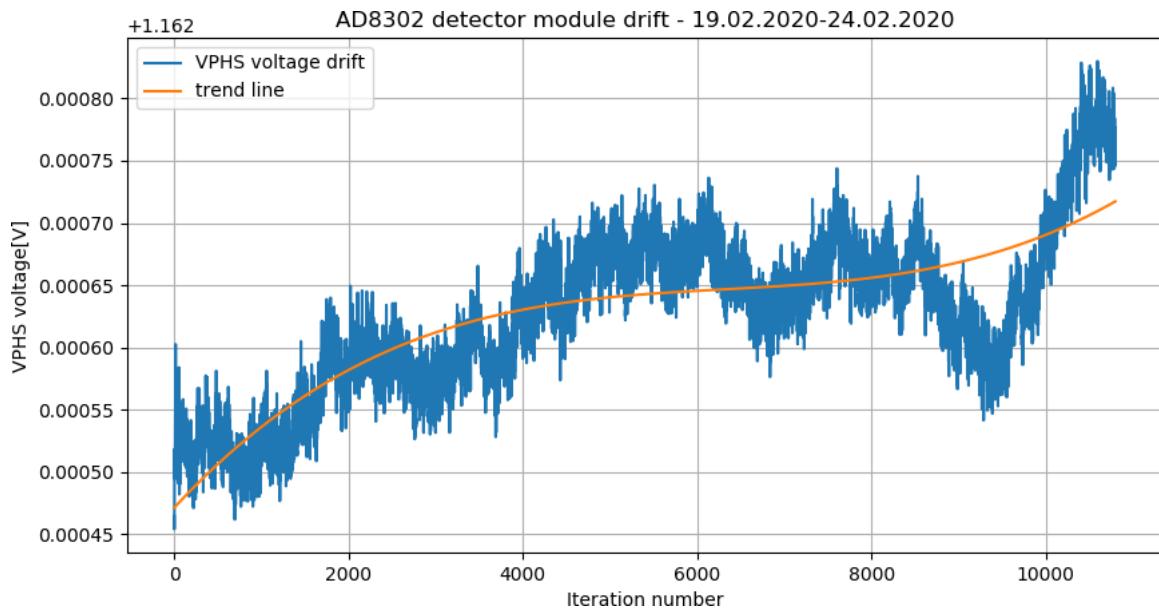


Figure 102: Test stand to measure the self-drift of AD8302.

The reference signal power level was chosen in a way that provides approx. -10 to -14 dBm to the phase detectors inputs. Taking into account the detection plots shown in Fig. 99 the scaling factor of 8.6 mV per degree phase change at 3.0 GHz is obtained. 1 mV of VPHS change is therefore equal to about 105.6 fs. The observation period shown in Fig. 101, and Fig. 102 was 5 days. The maximum deviation of VPHS voltage observed is

about 340 uV, which corresponds to approx. 36 fs of the self-drift of the phase detector. This means that any long-term phase drift detection less than 36 fs cannot be observed correctly with that type of phase detector.

The presented results were a motivation for further work on different ways of phase detection that might be found useful in interferometric links. Three methods were proposed. The first one is based on a custom six-port-based structure [98, 99], the second on a classic mixer-based phase detector, and the last on a vector-phase detector, described in Appendices.

The concept of using a six-port structure to measure phase difference in interferometric phase stabilization link was proposed by the author, based on [63] and realized as an MSc thesis by Grzegorz Pietrzykowski. The final module is based on high-dynamic range power detectors and realized as a small RF PCB module shown in Fig. 103.

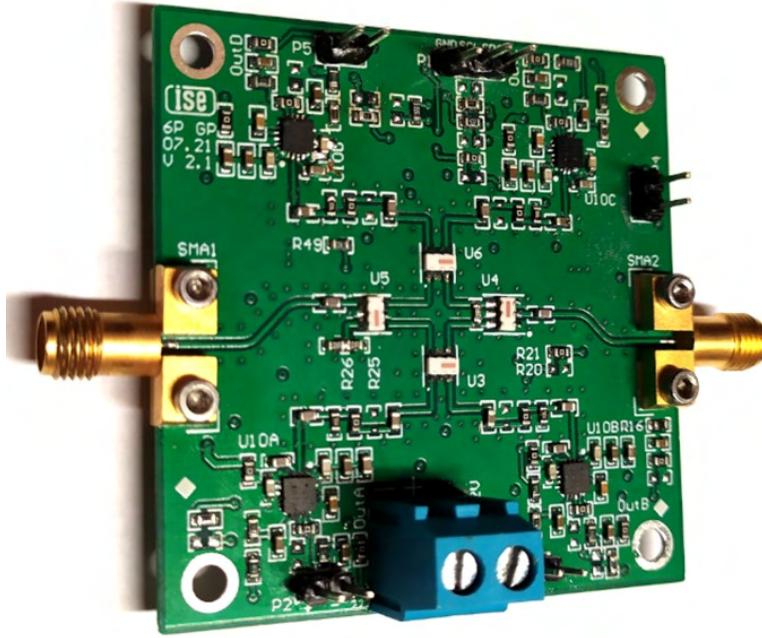


Figure 103: Realized prototype of six-port based phase detector for interferometric phase drift compensating links.

All the tested phase detectors were analyzed in a test stand shown in Fig. 104.

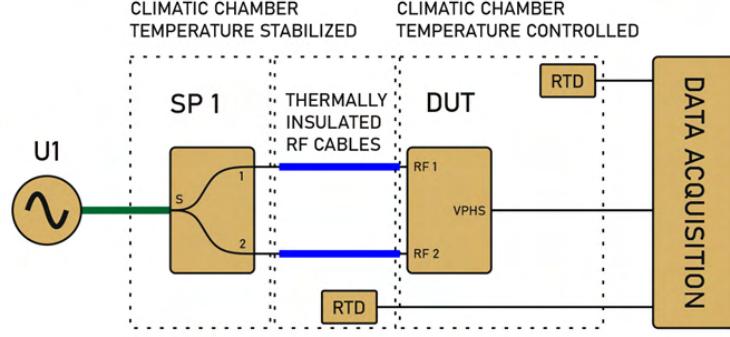


Figure 104: Test stand to measure temperature impact on phase detectors output signals [99].

A reference signal U_1 is split in a thermally stable power splitter SP1 (thus assumed as phase drift free) and then, via thermally insulated 50 cm long coaxial cables routed to a phase detector under test (DUT). All variable temperatures are measured with proper PT100 temperature sensors and a data acquisition unit. Plots presenting temperature impact on selected phase detectors are presented in Fig. 105, and Fig. 106.

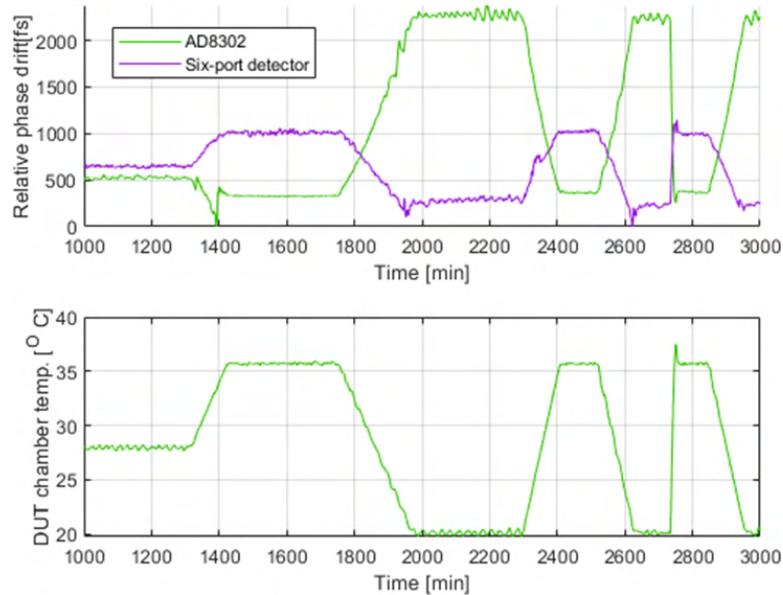


Figure 105: Temperature influence on the phase detection of AD8302 and designed six-port structure [99].

Temperature impact on MAC-42MH+ mixer

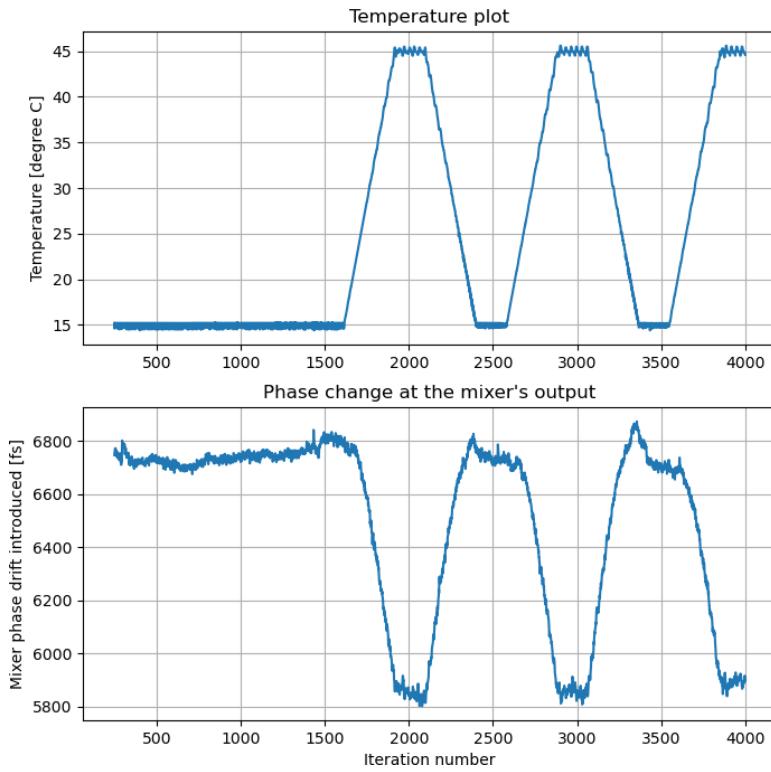


Figure 106: Temperature influence on the phase detection of MAC42-MH+ double balanced mixer.

The AD8302 phase detector chip and the prototype sixport structure were measured for temperature change of 15 degrees. The achieved results present that the developed sixport detector is less prone to temperature change and introduces significantly smaller self drift at its output. Unlike AD8302 it is easily frequency scalable, as both passive and active RF components may be replaced for a higher frequency range. In temperature stable conditions and in the frequency range within AD8302 operating range the introduced phase drift in stable ambient temperature is higher than the AD8302 (approx. 80 fs compared to 36-40 fs for AD8302), but still better than for the passive double-balanced mixer detector (approx. 100 fs). It is worth noting though that the mixer detector is significantly less prone to temperature change (approx. 400 fs for temperature change of 30 degrees). The presented results also explicitly show the necessity of temperature stabilization of phase detectors to achieve proper phase detection performance. For the SINBAD interferometer prototype, due to size mostly, the AD8302 was chosen as a phase

detector module. Both transmitter and receiver modules are designed to be thermally stabilized and for that the AD8302 is the smallest and introduces the lowest self drift at the output, yet still higher than required long term stability for the system.

7.3 Interferometric phase drift detection and compensation link prototype

For the prototype, interferometric phase drift compensating link for SINBAD two modules were designed. The interferometer transmitter module - InCON30 - and receiver module - TapPoint30. The overall diagram of a single receiver interferometer is shown in Fig. 107.

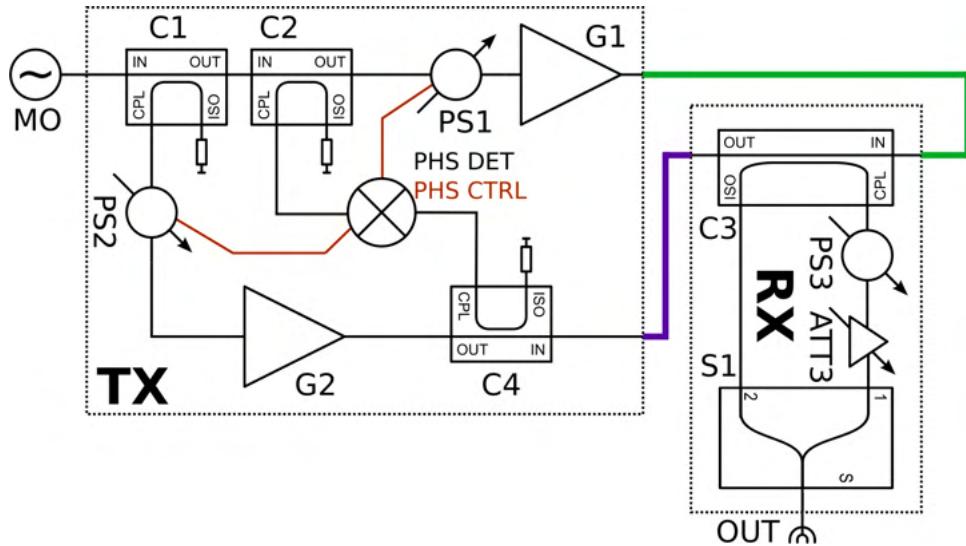


Figure 107: A block diagram of a single receiver interferometer link for SINBAD [77].

A reference signal from the MO is sampled for two purposes. The first is to provide a reference for a phase detector that keeps the phase difference between the interferometer loop ends constant. Secondly, a fraction of the reference signal coupled by C1 is then adjusted in phase by PS2 and amplified by G2 to form an artificial short signal - equal in phase as the normal signal reflected from an ordinary short circuit, but higher in power, which helps to set the optimal operating point for the receiver module. The receiver samples both forward and reflected signals and combines them to form a phase stable output, used to stabilize the output phase of the TapPoint output signal line.

The transmitter module is presented in Fig. 108 and the receiver in Fig. 109.

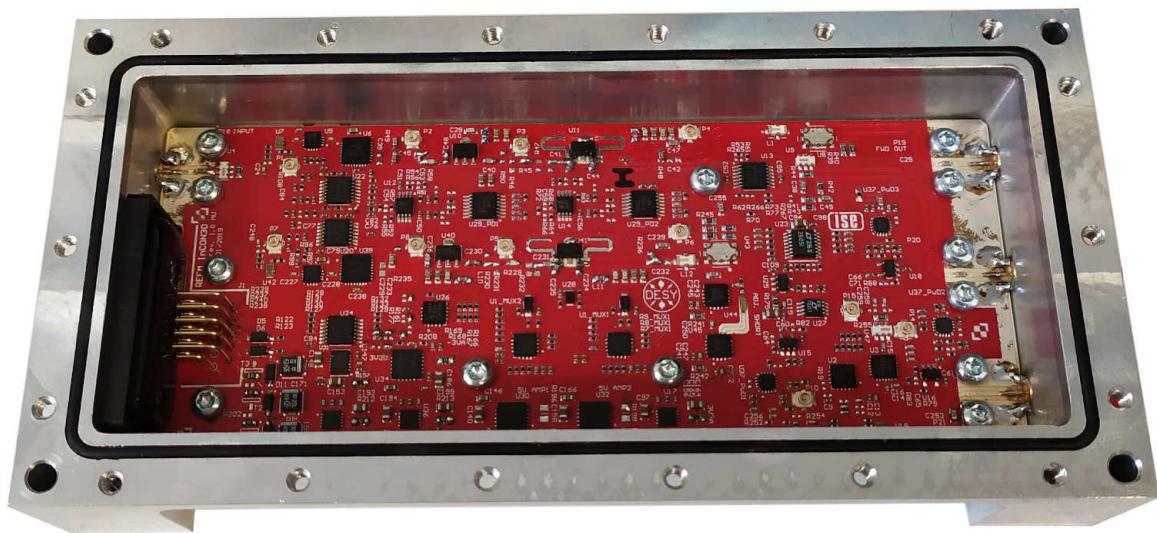


Figure 108: SINBAD interferometer transmitter module - InCON30.

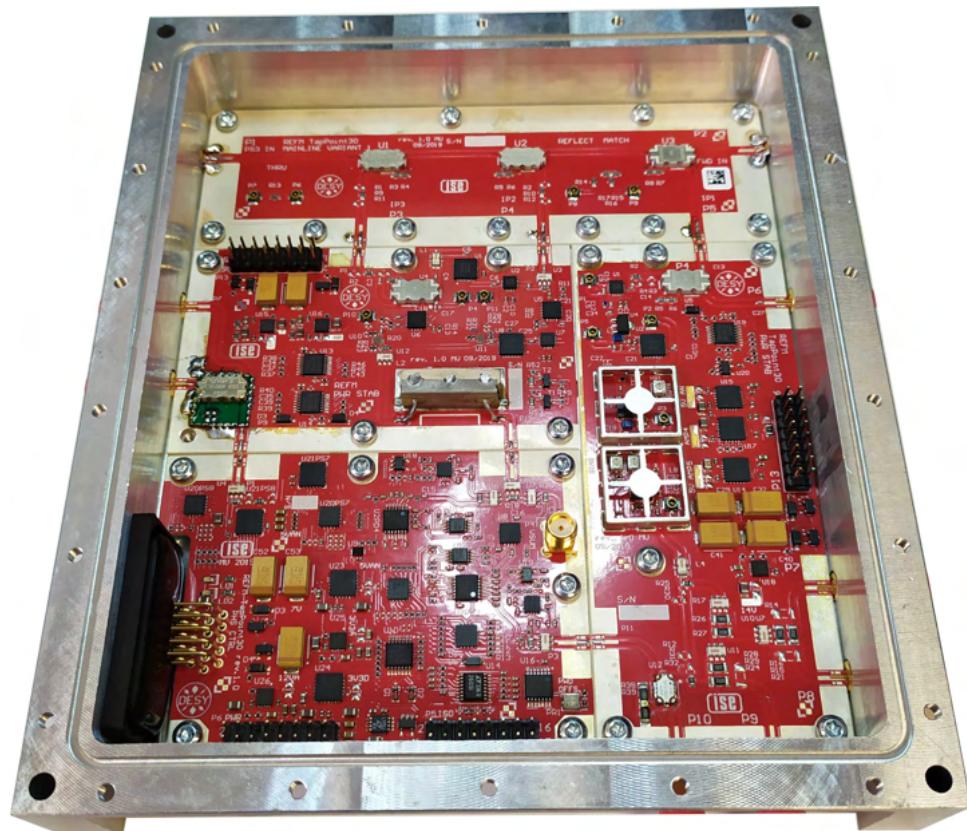


Figure 109: SINBAD interferometer receiver module - TapPoint30.

8. Summary

The thesis concludes the over 5 years of work on the PRDS components for linear particle accelerators in DESY, and ESS facilities. The thesis goals are achieved. The primary goal, of identifying critical PRDS components and developing new methods for the design and synchronization at the femtosecond level in the accelerator facilities is done by presenting systems and components made for DESY and ESS. The mentioned contribution is also a proof of reaching the secondary thesis goal - the development of technology and universal design methods for modern PRDS subcomponents, with thermal stabilization, hermetization, shielding and improved invulnerability to environmental factors and stress.

The theoretical background, describing the most important aspects of PRDS is described, followed by a brief introduction to selected linac facilities. Then in the following 4 chapters author presents his contribution to PRDS in the described facilities.

First, the contribution to the development of the phase reference distribution system for European XFEL is presented, where author designed a prototype of automated receiver module for interferometric phase compensating link. The receiver is a part of an interferometric link, able to compensate long-term phase drifts with a 200 x suppression factor, from 10 ps to 50 fs. At the same time, the author developed, manufactured and tested a custom, ultra low-noise, RF reference frequency divider modules. Over 60 modules were produced, and 50 of them are in constant operation, installed along the entire European XFEL facility [10, 29], providing low-frequency reference signal for selected E-XFEL endpoints, like BPMs or the injector.

Then the most important contribution of the thesis is presented - the complete PRDS upgrade for FLASH2020+. Work on the upgrade was conducted in the years 2020-2022 and resulted in a completely new, state-of-the-art PRDS, based on an ultra-low phase noise (10 fs time jitter in integration range from 10 Hz to 1 MHz) 1.3 GHz Main Oscillator, custom high power multi-output distribution module with embedded diagnostics, and a complete frequency conversion module of the reference signal. The developed upgrade provides 10 fs phase noise RF reference signal to all the FLASH endpoints, which is a remarkable improvement, when compared to old FLASH MO (55.9 fs) and the E-XFEL

MO (19.5 fs). The author's contribution includes a design of a Main Oscillator, together with Bartosz Gąsowski, who was responsible for the integration of RF electronic components within the box. The author has also developed a complete design of the RF reference signal distribution module, based on custom, multi-output, hermetic, and optionally thermally stabilized power splitter modules with embedded diagnostic circuitry. Developed modules deliver RF reference via coaxial cables to all FLASH endpoints, and are a novel contribution to the field of PRDS. To the author's best knowledge, there were no distribution modules with such a superior performance and embedded diagnostics reported in the literature. For the frequency conversion modules, the author has developed upgraded, universal frequency dividers, with extended reset circuitry and input interlock circuit, protecting against lack of input RF signal. They are significantly smaller than the previous version, used in E-XFEL, and due to their universal character, they may be easily adopted for other phase reference distribution systems.

The author's contribution is also the development of design methods for ultra-fragile RF generators in terms of mechanics and isolation from ambient distortions. The developed methods helped to achieve outstanding phase noise parameters of the system, significantly simplified the manufacturing, and improved the serviceability. These methods were successfully implemented in the frequency conversion module for FLASH2020+.

Developments for the FLASH2020+ upgrade done by the author are important contribution to the field of phase reference distribution systems for linear particle accelerators - an unquestionable argument in favor of this statement is an ongoing commercialization process of delivered designs in DESY. Small series production is planned for other DESY systems, and potentially for other particle accelerator facilities worldwide.

Chapter 6 covers the work done as a part of a WUT internal project, devoted to the development of an interferometric phase drift compensating link - a prototype for 162.5 MHz RF reference signal. The author has designed a structure of the system, performed all the RF budget calculations, and verified the concept in simulations. The prototype was then assembled and tested by Andžej Šerlat, and the test results are presented in the thesis, proving the ability to compensate for phase drifts introduced by coaxial cables by a factor of over 100 x.

The last part of the thesis describes the author's contribution to the SINBAD PRDS development in DESY, which was the design of an redundant and universal RF cabling system. The author has designed a distribution system that has been successfully installed in SINBAD. Based on requirements stated by DESY author has proposed a structure of the PRDS, utilizing interferometric loops, and for this purpose designed and manufactured the prototype transmitter and receiver modules for the system. At the moment of writing the thesis, these modules were under test.

A part of the work done for SINBAD was realized as an international co-founded project, that author led and successfully finished. An author's team has managed to deliver several PRDS components, described in the Appendices. Due to the very strict and hard-to-meet requirements author has investigated and presented key limitations of component parameters that directly limit the achievable long-term phase stability of the stabilized RF reference signal. This research shows a current boundary of phase detection precision by analog RF phase difference detectors. The research results will be further used in other systems that are planned to be realized in the next few years. All the supplementary modules and parts that the author has co-designed (including the PRDS components for ESS) are described in Appendices.

Additional results of the author's thesis are two finished MSc theses, one MSc, and one BSc theses currently under development.

Plans for future research include the development of new PRDS systems within planned ISE cooperation with Fermilab, the development of test procedures in European Spallation Source, and the finalization of tests of the SINBAD interferometer prototype.

9. Appendices

This chapter contains all the supplementary modules the author has designed or co-designed during work related to the thesis. At first, a concept of hermetic housings is presented, which was developed initially for European XFEL hermetic RF components and later adopted for other projects at ISE.

Next, the ESS phase reference distribution system components are presented. These are placed in appendices as the author, in most cases, was responsible for some part of the project, which is explicitly described in further parts of the chapter.

Another important topic in Appendices is the phase shifter development the author has done over the last few years, mainly for SINBAD PRDS. It presents two types of phase shifters, one based on commercial mechanical solutions and the other using varactor diodes as phase-tuning elements.

Next, the custom high-power 3 GHz amplifier with embedded self-phase-drift compensation circuitry is presented. The author has developed the general concept of the module and then guided the MSc student during his development of the amplifier.

The last appendix covers the developed prototypes of the author's concept of passive phase detectors, realized using power splitters or, in simpler variants, only resistors.

9.1 Concept of custom hermetic metal housings for RF devices

It is of utmost importance for the selected components of phase reference distribution systems to be held in stable conditions, not harmed by environmental changes, as any ambient temperature or humidity drift may directly impact PRDS performance and introduce additional phase drifts. These were determined during work on European XFEL PRDS components, done with Dominik Sikora and Paweł Jatczak. At that time author designed a custom, hermetic metal housing for the XFEL TapPoint interferometer receiver module. The requirements for the housing were:

- Isolate the electronics from ambient changes, both temperature and humidity.
- Keep the module's thermal capacity as low as possible to be able to quickly heat and cool it down.
- Maintain good return loss at RF ports (better than 25 dB) and good RF grounding.
- Provide DC power and control signals to the module.
- Implement the internal housing thermal sensors.
- Make the housing compatible with TEC modules-based thermal stabilization systems.
- Make the housing as simple to manufacture as possible.

The designed housing proved its value, and the general concept was then adopted in several other modules for different accelerators' PRDS'es:

- European XFEL TapPoint modules [50].
- FLASH2020 DISM divider modules - 10 modules in total have been manufactured and installed in new FLASH PRDS.
- SINBAD PRDS system components - InCON30 and TapPoint30 housings.
- ESS PDC module [100].

- ESS Split Box module, a part of every TapPoint unit - 70 modules have been manufactured and installed along the ESS accelerator [54].

An example of a housing compatible with the concept is shown in Fig. 110.

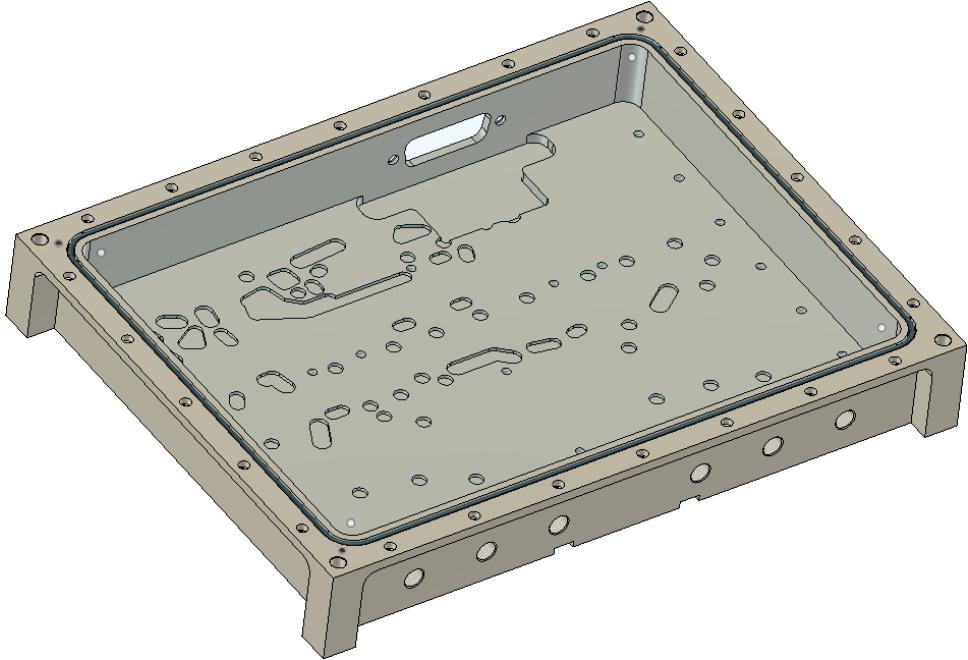


Figure 110: ESS PDC housing, an example compatible with the presented housing concept.

A hermetic housing is made of two major parts - a housing body and a cover assembled using screws and cover sealing, similar to a solution used in car engines. Such an approach ensures that the top cover is properly sealed. All the input/output connectors will be in custom, hermetic versions shown in Fig. 111.

Good RF grounding of the module is maintained in two ways. First, the PCB's bottom solder and bottom overlay must be empty, except the non-GND vias (these are covered with solder mask by design). Then the housing must have the bottom part milled properly, creating an insulating space directly under the non-GND vias and, thus, protecting the module from shorts. Such an approach provides good RF grounding and a very good thermal connection. Keeping the thermal capacity of the housing as low as possible is done by milling the side walls of the housing.

The concept was further improved in FLASH2020 DISM divider modules by replacing the hermetic SMA connectors with standard, 4-hole flange connectors that provide significantly better mechanical robustness. The housing features around the SMA connectors



Figure 111: Commercial IP67 sealed SMA connector.

were altered, and standard rubber o-ring sealings were introduced. This way, the housing is still sealed, and there is no more need for using custom sealed SMA connectors (a more cost-effective solution). Details are shown in Fig. 112. Presented alteration also lets to easily plunge unused connectors while maintaining required parameters. Additional TEC thermal stabilization is possible by adding an extra thermal insulating layer and an additional heatsink for the TEC module, as shown in Fig. 113.



Figure 112: FLASH2020 sealed connectors in DISM modules.

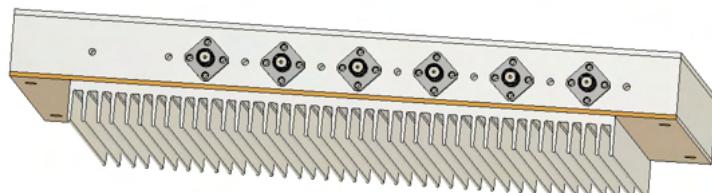


Figure 113: Additional TEC thermal stabilization upgrade for DISM dividers' housings.

To verify the performance of the presented solution and prove the required return loss level, a custom jig was done, as shown in Fig. 114. The substrate used for the jig's PCB is the same as for the FLASH2020 DISM divider PCBs, as same as connectors and rubber o-ring sealings. The housing wall thickness is the same as in the final divider housing design. The presented solution was measured to have a return loss better than 25 dB), as shown in Fig. 115

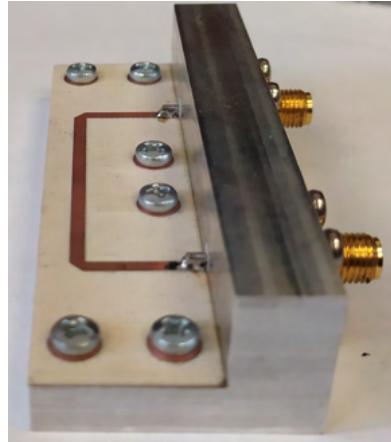


Figure 114: FLASH2020 housing connector test jig.

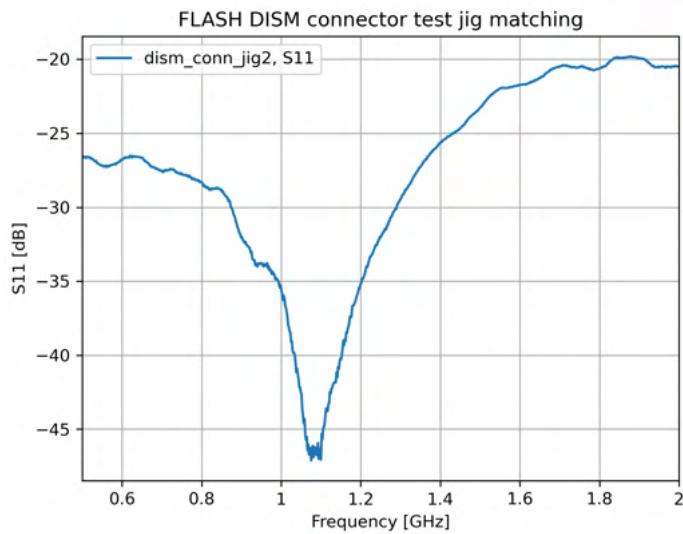


Figure 115: Return loss measured with the connector test jig.

9.2 ESS diplexer modules

The author has also supported ISE work on the development of ESS PRDS in Sweden by creating the following parts of the system:

- housing and PCB design for high power diplexer module [101],
- housing and PCB design for TapPoints' Split Box modules [54],
- housing design for PDC control module [100].

A simplified PRDS block diagram is shown in Fig. 116.

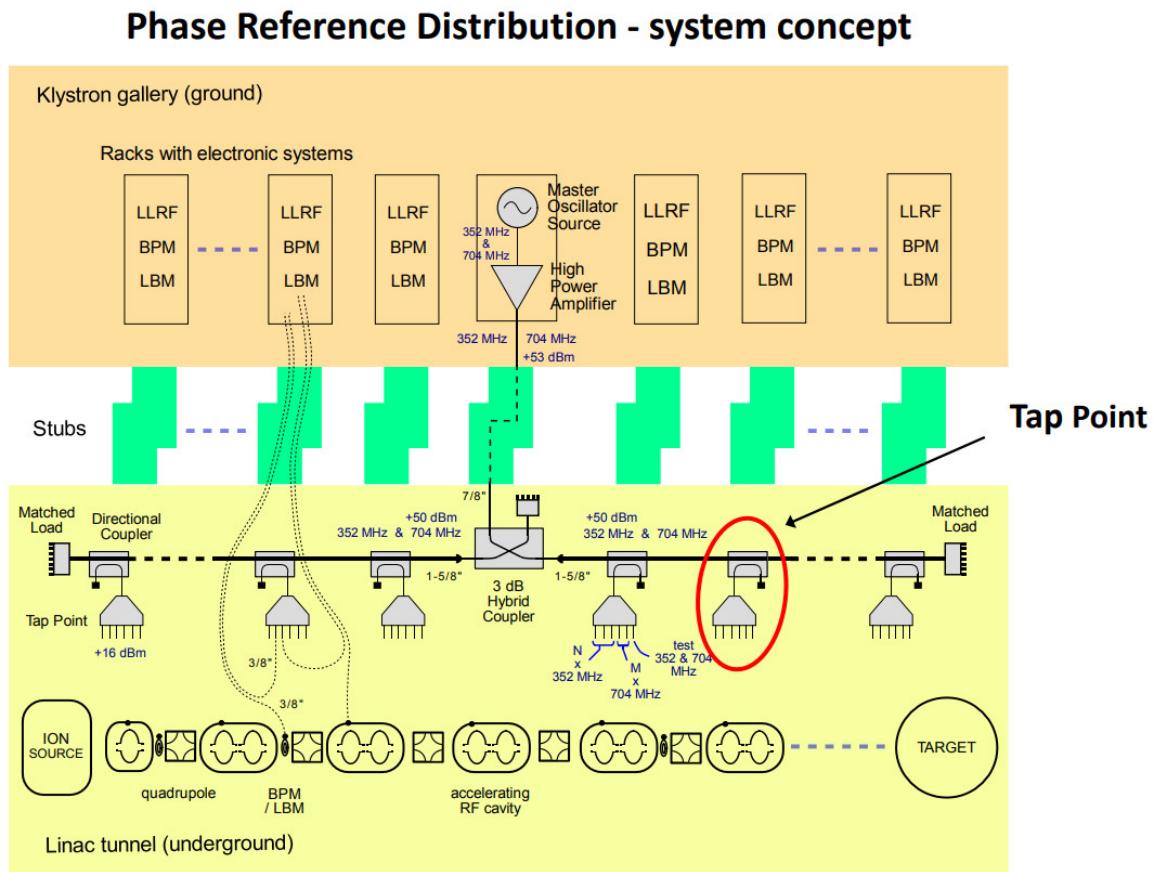


Figure 116: A simplified block diagram of ESS PRDS [54].

Due to radiation, the electronic control systems of the ESS accelerator are held in a separate room and are connected to the accelerator via 50m long stubs. Reference signals are generated by a two-channel Master Oscillator module and are then amplified to roughly 200W power and combined by a custom high-power diplexer [101] that the author also co-designed. Such an approach allows transmitting both reference signal frequencies via a single coaxial cable. A two-tone reference signal is then split into two PRDS branches by a 3 dB hybrid coupler mounted in the middle of the accelerator. Each accelerator section couples a fraction of reference signals via TapPoint modules, as shown in Fig. 116.

9.2.1 High power diplexer module

The high-power diplexer module's task is to combine two 200W reference signals into a single, two-tone high-power signal, as described in detail in [101]. A. Abramowicz has done it by designing a planar diplexer filter structure, utilizing half-wave resonators and quarter-wave impedance inverters. The author's task was to design a PCB and a hermetic housing for the diplexer. The assembled high-power diplexer module is presented in Fig. 117. In total, three modules have been made.

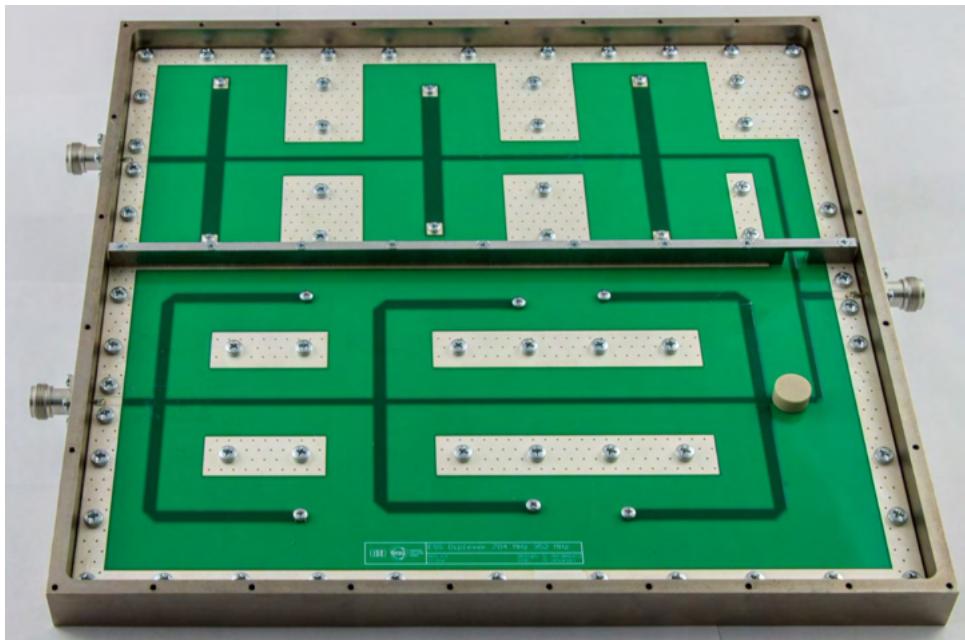


Figure 117: High power diplexer module.

9.2.2 Configurable diplexer module

ESS TapPoint's function has been presented in Fig. 116. The module is shown in Fig. 118 [54].

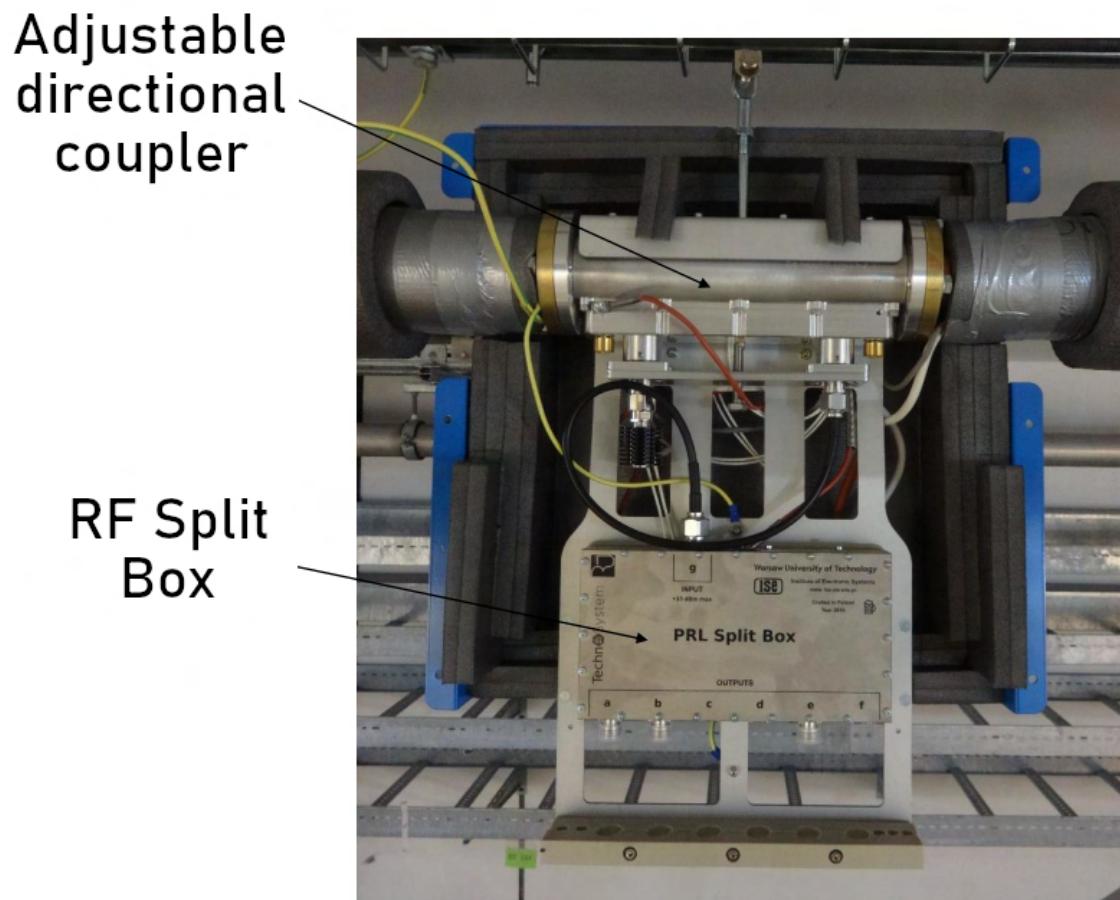


Figure 118: ESS TapPoint module, showing the directional coupler and RF Split Box module that the author co-designed.

Key components of each TapPoint module at ESS are an adjustable directional coupler and a custom RF Split Box module that filters both reference signals' tones and divides them into selected outputs.

M. Żukocinski and the author have designed the RF Split Box module. The author's contribution is the design of internal PCBs (shown in Fig. 119) and the housing design (shown in Fig. 120). Both are foreseen and designed so it is possible to reconfigure the whole module by swapping the PCBs positions. M. Żukocinski has designed the module concept and simulated the diplexer structures.

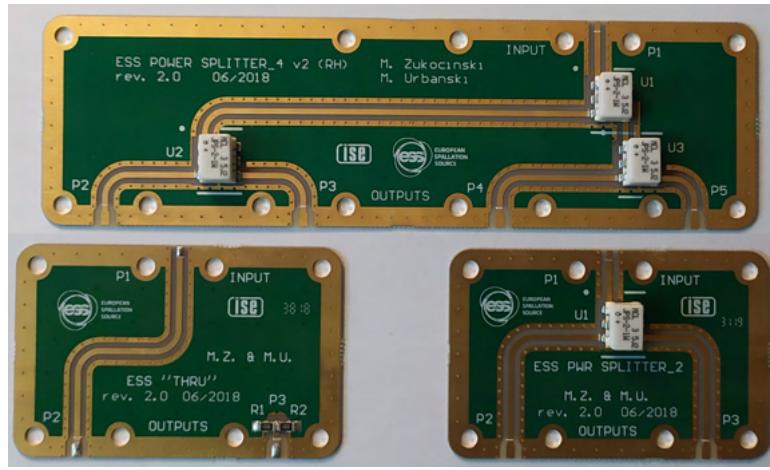


Figure 119: RF Split Box PCBs, designed by the author.

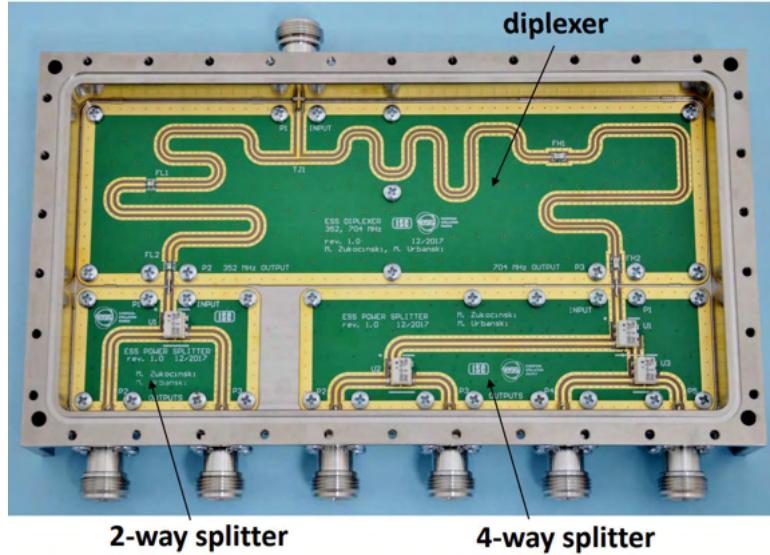


Figure 120: RF Split Box internal view.

9.3 Phase shifters

A part of the author's work on phase reference system components for FLASH, XFEL, and SINBAD was related to various phase shifter structures design. Two different phase shifters for two different applications are presented in the thesis. First is the modification of the mechanical phase shifter that makes the very small phase changes (less than 0.01 degree at 3.0 GHz that corresponds to approx. 10 fs) possible. Second is the set of varactor base phase shifters that the author developed with Bartłomiej Kola in response to the lack of commercial voltage-controlled phase shifter IC working at 3.0 GHz, with good input and output matching.

9.3.1 Modification of a commercial mechanical phase shifter

When a phase reference distribution system prototype is done, it has to be tested to verify its performance. For this purpose, there is a need to have a very stable and precise phase-shifting element that will emulate the phase-drifting transmission line. As the drifts measured are to be close to 10 fs, it is then required that the phase shifter can introduce such a small phase change. Considering several phase shifting structures and the author's experience in developing European XFEL interferometric link components, it has been decided to use a mechanical phase shifter. It provides a constant phase change, is quite repeatable, and introduces very small transmission loss. When equipped with a motor, it becomes a useful device that may be remotely controlled. In the European-XFEL interferometer prototype, a standard brushless motor and a potentiometer were used to drive and monitor the phase shifter position, which was unreliable. To avoid such problems again, the author has used a stepper-motor-based commercially available Narda ATM P1604-SM24 phase shifter and equipped it with a custom-made stepper motor driver with the micro-stepping feature. The designed stepper motor driver can divide a single step up to 128 micro-steps. Thus the minimum phase shift change is further reduced. During measurements, it was noticed that the reliable (due to mechanical imperfections) step division ratio is 16, which corresponds to approx. 0.004 degrees at 3.0 GHz. Further reducing the phase change is most likely possible, yet impossible to verify now due to the finite performance of available phase detectors. The author's modified phase shifter is shown in Fig. 121 and Fig. 122. Phase shifter driver PCB is based on AVR ATMega8

microcontroller and AMIS-30543 stepper motor driver IC. Firmware is written in Arduino IDE and communicates via a USB-UART converter. The housing for the module was 3D printed.

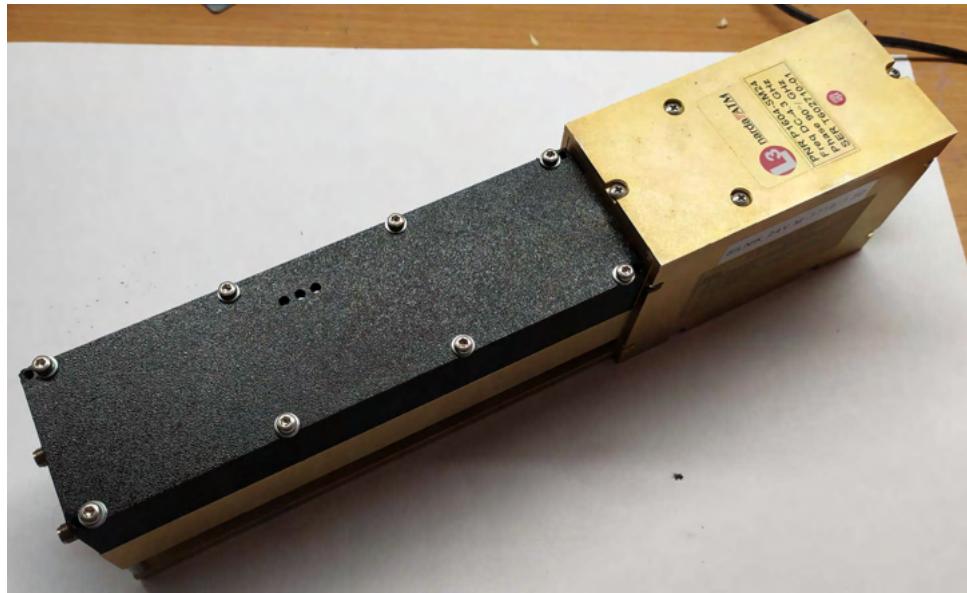


Figure 121: Modified mechanical phase shifter, generating ultra-small phase changes.

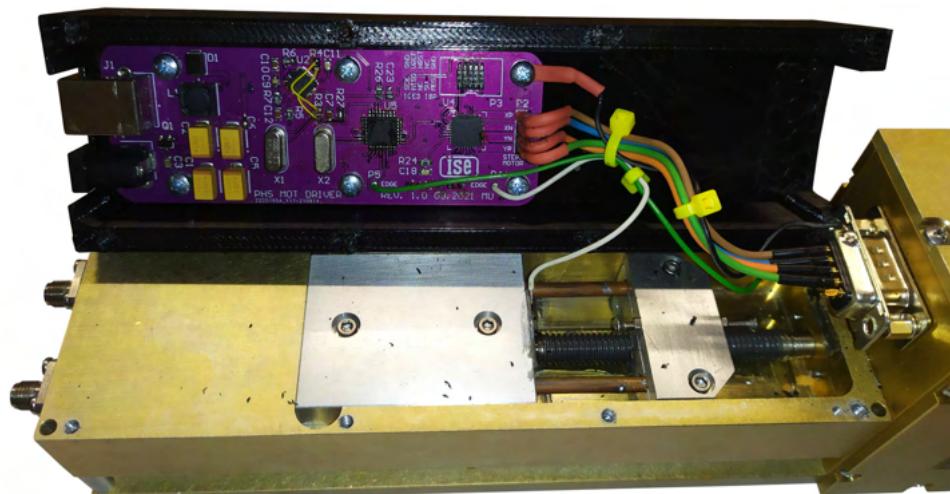


Figure 122: Mechanical phase shifter driver circuit.

9.3.2 Varactor-based reflection phase shifters

European XFEL interferometer link components used analog voltage-controlled phase shifter ICs, manufactured by Hittite. At the time of these XFEL modules' development, the ICs were on the obsolescence list, together with all other phase shifter ICs from Hittite, which was, at the time, the only significant supplier of such devices. It became obvious that for the development of SINBAD PRDS components, another approach had to be developed. For the most critical components, the obsolete 3.0 GHz phase shifter ICs were ordered in advance to store them in the DESY warehouse, but all supplementary modules had to use different phase shifters. This is why the author developed custom varactor-based phase shifter modules, inspired by a publication [102]. Phase shifters should meet the following requirements:

- return loss measured at all ports better than 15 dB,
- insertion loss better than 4 dB at any phase shift setting,
- selected phase shifters should be able to work with input signals up to +30 dBm,
- voltage driving range should be from 0 to 15V, and phase shift range should be at least 120 degrees,
- physical dimensions should be small, as the phase shifters should be easily applicable in other modules,
- tuning speed should be faster than in mechanical phase shifter.

Prototypes were made using a typical FR4 substrate and a compact 3 dB hybrid coupler [103, 104]. Varactor diodes are biased with DC voltage, which alters their capacitance and, thus, the reflection coefficient. The input signal coming to the input port of the 3 dB coupler is reflected with an altered phase and then transmitted back to the output port. Prototypes designed for 1.3 and 3.0 GHz frequencies are shown in Fig. 123 and Fig. 124 respectively. A small layout redesign resulted in the creation of an easily applicable phase shifter, as shown in the example application in the REFM30 AMP module in Fig. 125. Varactor branches were redesigned to fit a small PCB soldered on top of the 3 dB hybrid coupler.

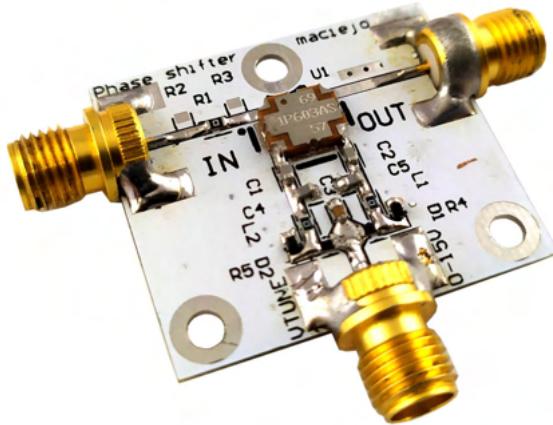


Figure 123: A prototype of 1.3 GHz phase shifter.

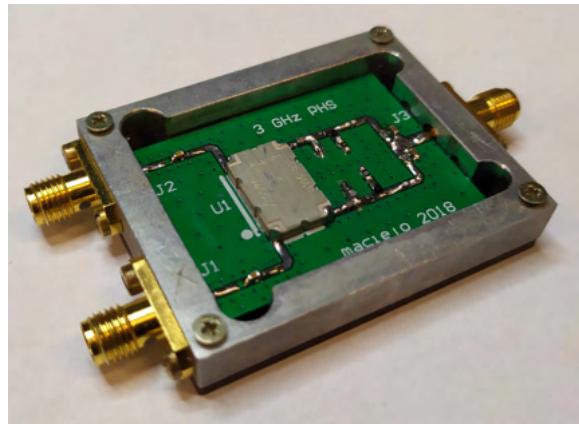


Figure 124: A prototype of 3.0 GHz phase shifter.



Figure 125: An example of designed phase shifter application in REFM30 AMP module.

Similar phase shifting structures were designed as standalone modules, planned to replace mechanical phase shifters directly in the interferometric link's main transmission line. Two types of phase shifters, utilizing four and six-diode structures, were designed

and manufactured, with the support and help of Bartłomiej Kola, based on [102]. These structures were designed to provide a phase shift range better than 180 degrees and maintain return loss better than 15 dB. Prepared prototypes are shown in Fig. 126, Fig. 127 and their test results are shown in Fig. 128 and Fig. 129. In the worst case, the achieved phase shift range is better than 200 degrees, and S11 is better than -17 dB. Presented phase shifters were not finally used in the system because they tend to saturate when operating with the high power input signal, around +21 dBm, but they are still valuable modules that may be used in many other circuits, not only PRDS applications.

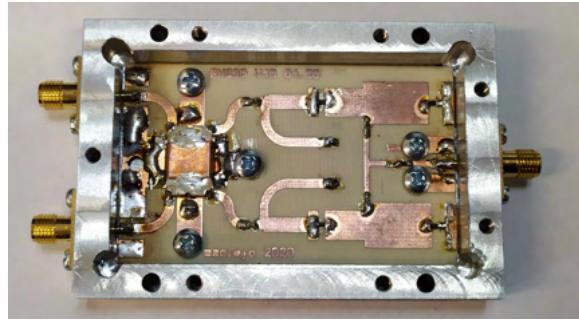


Figure 126: 3.0 GHz 4-diode varactor phase shifter prototype

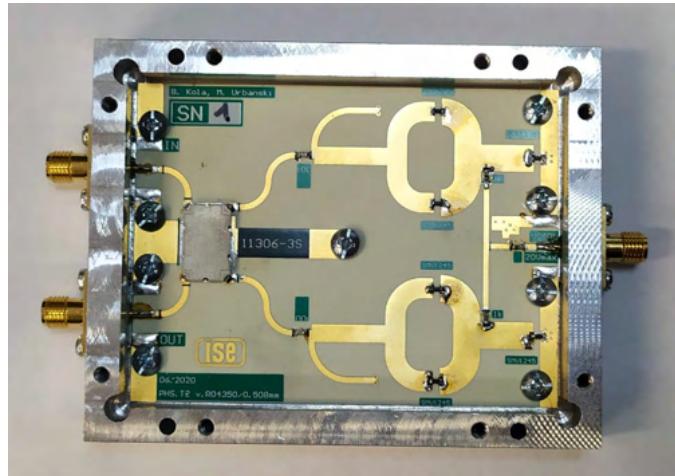


Figure 127: 3.0 GHz 6-diode varactor phase shifter prototype.

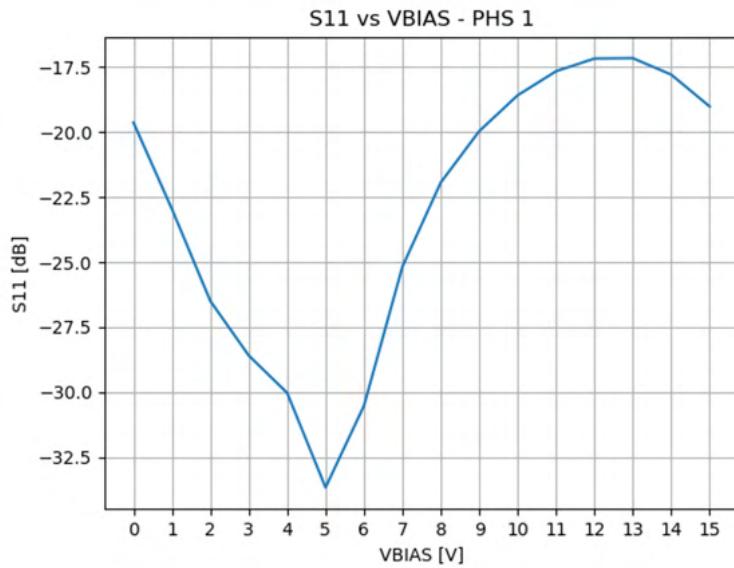


Figure 128: S11 vs. bias voltage for 3.0 GHz 6-diode phase shifter.

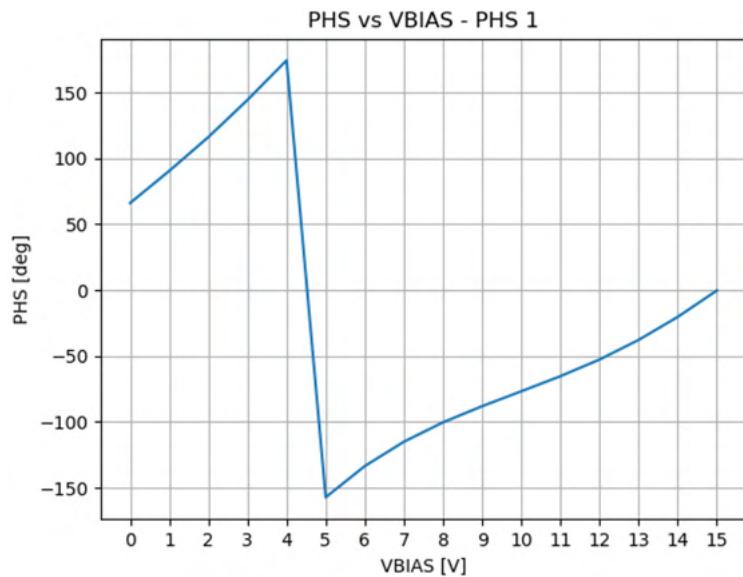


Figure 129: S21 phase of 3.0 GHz 6-diode phase shifter.

9.4 Vectorphase detector

The author proposed a simple phase detector that may be realized using the concept of the vector sum of input phasors. A principle of operation and basic schematics are shown in Fig. 130 a,b, and c.

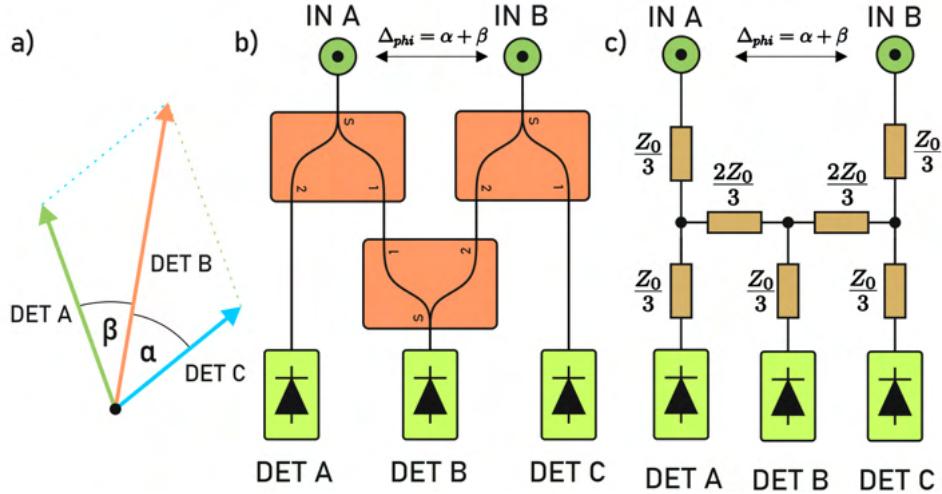


Figure 130: A block diagram of a power splitter-based vector sum phase detector.

Knowing the output voltages of detectors A, B, and C, it is possible, using the law of cosines, to calculate the value of the angle between vectors A (green) and C (blue), using Eq. (9.1):

$$\gamma = \alpha + \beta = \arccos \left(\frac{DET\ B^2 - DET\ A^2 - DET\ C^2}{2 \cdot DET\ B \cdot DET\ C} \right) \quad (9.1)$$

The vector B (red) is the combiner's output signal. A structure given in Fig. 130 b may be further reduced to a variant shown in Fig. 130 c, where power splitters are realized as a resistive star topology. For the cost of bigger insertion loss (approx. 12 dB at vector B and 6 dB at vectors A and C) and lower isolation, it offers a very broad frequency range of operation, limited only by the resistors parasitics and used transmission lines. A phase detector based on this concept may be easily implemented in interferometric phase compensation links described in the thesis.

The author has developed two prototypes of presented phase detectors, shown in Fig. 131, and Fig. 132.

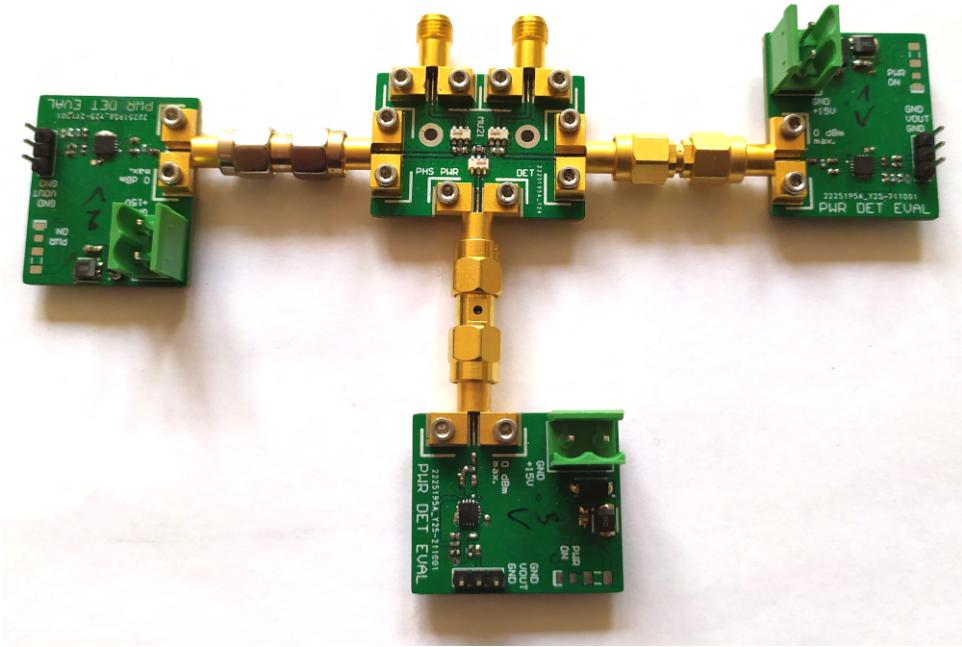


Figure 131: A vectorphase detector, based on RF power splitters (SCN-2-35+).

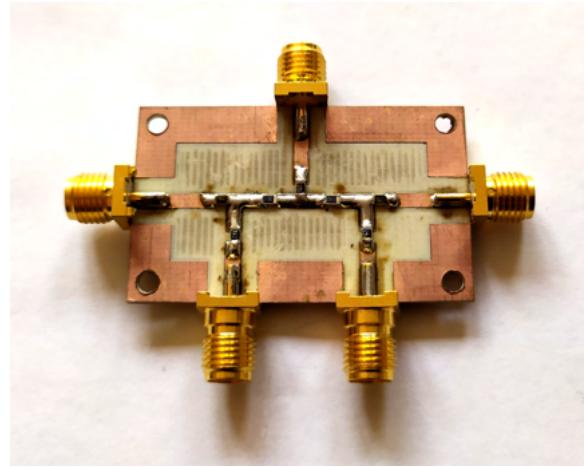


Figure 132: A vectorphase detector, based on resistor network.

The measured results that prove the correctness of proposed calculations and operation of detectors are shown in Fig. 133.

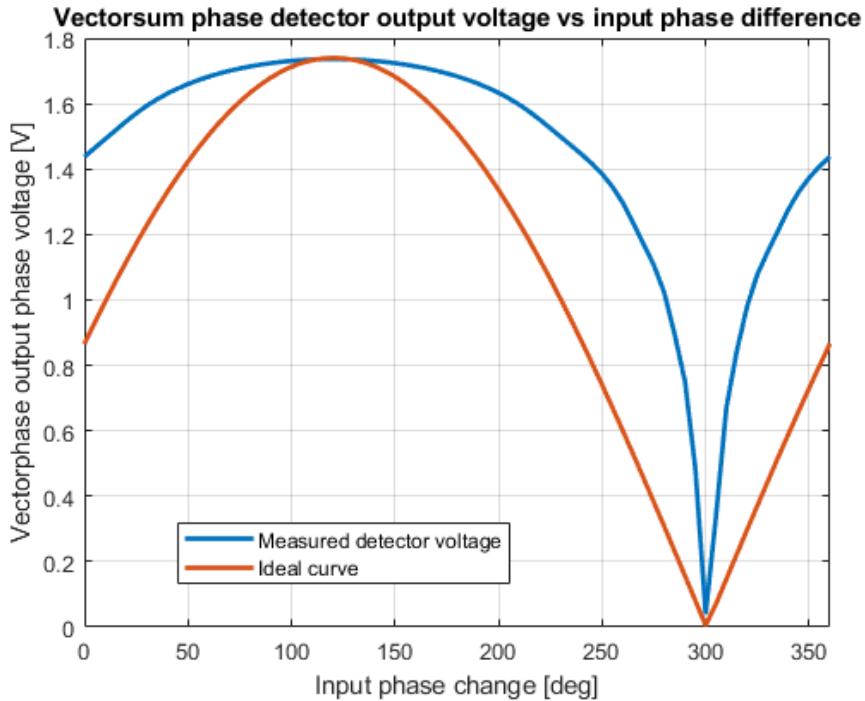


Figure 133: A vectorphase detector combiner output voltage, measured and ideal.

The measured curve shape is similar to the ideal, calculated from the law of cosines, yet additional effects, shaping the plot are observed. The main limitations that are not included in the simple model described by the Eq. (9.1) are:

- finite return loss of used power splitters,
- insertion loss introduced by the power splitters,
- finite isolation of the power splitters. Because of that, detectors A and B do not measure constant power across the whole input phase detection range,
- imbalance in introduced insertion loss,
- power detectors' nonlinearity.

Author's list of contributions

1. Maciej Urbański, et. al., *An Upgrade of RF Reference Generation and Distribution Modules for FLASH2020+*, in peer review, 2023
2. Dominik Sikora, et. al., *Phase Drift Compensating RF Link for Femtosecond Synchronization of E-XFEL*, IEEE Transactions on Nuclear Science, 2020, DOI: 10.1109/TNS.2020.2966018
3. Maciej Urbański, Grzegorz Pietrzykowski, Krzysztof Czuba, *Custom Six-Port Structure For RF Phase Drift Long-Term Detection*, 2022 24th International Microwave and Radar Conference (MIKON), Gdańsk, Poland, 2022, pp. 1-3, DOI: 10.23919/MIKON54314.2022.9924875
4. Dominik Sikora, et. al., *RF Connection from Master Oscillator to Phase Reference Line in European Spallation Source*, 2020 23rd International Microwave and Radar Conference (MIKON), Warsaw, Poland, 2020, pp. 162-164, DOI: 10.23919/MIKON48703.2020.9253790
5. Maciej Urbański, et. al., *The concept of the RF phase reference distribution system for SINBAD accelerator research facility*, 2018 22nd International Microwave and Radar Conference (MIKON), Poznań, Poland, 2018, pp. 385-387, DOI: 10.23919/MIKON.2018.8405233
6. Maciej Urbański, et. al., *Frequency divider module for the European XFEL phase reference signal distribution system*, 2018 22nd International Microwave and Radar Conference (MIKON), Poznań, 2018, pp. 631-633, DOI: 10.23919/MIKON.2018.8405309
7. Maciej Urbański, Bartłomiej Kola, Krzysztof Czuba, *Voltage Driven Phase Shifters for Phase Reference Distribution System in SINBAD*, 2020 23rd International Microwave and Radar Conference (MIKON), Warsaw 2020, DOI: 10.23919/MIKON48703.2020.9253786
8. Bartosz Gąsowski, et. al., *Concept of Master Oscillator Upgrade for FLASH*, 2020 23rd International Microwave and Radar Conference (MIKON), DOI: 10.23919/MIKON48703.2020.9253858

9. Julien Branlard, et. al., *Installation and First Commissioning of the LLRF System for the European XFEL*, 8th International Particle Accelerator Conference,

DOI: 10.18429/JACoW-IPAC2017-THOAA3

10. Maciej Grzegrzółka, et. al., *Status of Control and Synchronization Systems Development at Institute of Electronic Systems*, 17th International Conference on Accelerator and Large Experimental Physics Control Systems (ICALEPCS 2019)

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