

Reasoning about capability machines using logical relations

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Road map

Capability Machine

Formalisation

Example program

Logical Relation

Example revisited

Current work

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Current work

Why should I care about capability machines?

Current low-level protection mechanisms

- ▶ Coarse-grained compartmentalisation
- ▶ Expensive context switches
- ▶ Well-suited for high-level applications
- ▶ Does not scale well

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Capability machines

- ▶ Fine-grained compartmentalisation
- ▶ Cheap compartments
- ▶ Fine-grained sharing
- ▶ Well-suited for applications with need for many compartments

Capabilities

What is a capability?

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- ▶ *Unforgeable* token of authority

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What is a capability in a capability machine?

- ▶ Unforgeable pointer

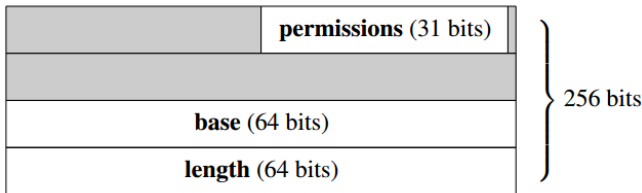


Figure: CHERI capability [1]

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- ▶ Range of memory

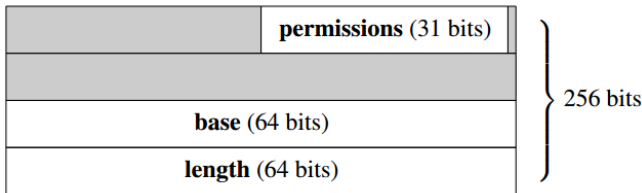


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What is a capability in a capability machine?

- ▶ Unforgeable pointer
- ▶ Range of memory
- ▶ Permission

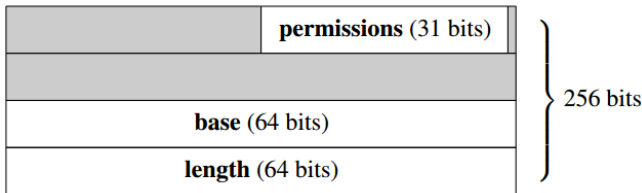


Figure: CHERI capability [1]

Capability permissions

- ▶ Read
- ▶ Write
- ▶ Execute

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 - ▶ Used by distrusting pieces of code to cross security domains
 - ▶ Modularisation

Capability machine instructions

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 - ▶ No instruction generates new capability
 - ▶ Manipulation of capabilities cannot result in authority amplification

Capability machine overview

- ▶ Capabilities

Capability machine overview

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- ▶ Heap and registers

Capability machine overview

- ▶ Capabilities
 - ▶ Permissions
 - ▶ Range of authority
- ▶ Capability aware instructions
- ▶ Heap and registers
 - ▶ Can contain data and capabilities

Road map

Capability Machine

Formalisation

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Current work

Formalisation

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- ▶ Allows us to reason formally
- ▶ May make some abstractions
- ▶ Needs to stay true to a real system
- ▶ This formalisation is of a capability machine (not CHERI or the M-Machine)

Formalisation - Permissions

Permissions

- ▶ To simplify matters, we only allow certain combinations of permissions

$$\text{Perm} \stackrel{\text{def}}{=} \{ \quad \quad \quad \}$$

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- ▶ No permissions, read only, read-write,

$$\text{Perm} \stackrel{\text{def}}{=} \{o, \text{ro}, \text{rw}, \quad \}$$

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Formalisation - Permissions

Permissions

- ▶ To simplify matters, we only allow certain combinations of permissions
- ▶ No permissions, read only, read-write, read-execute, enter, read-write-execute

$$\text{Perm} \stackrel{\text{def}}{=} \{o, ro, rw, rx, e, rwx\}$$

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$$\text{Addr} \stackrel{\text{def}}{=} \mathbb{N}$$

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$$\text{Addr} \stackrel{\text{def}}{=} \mathbb{N}$$

$$\text{Cap} \stackrel{\text{def}}{=} \text{Perm} \times \text{Addr} \times \text{Addr}$$

Formalisation - Capabilities

Capability

- ▶ Permission
- ▶ Range of authority
- ▶ Pointer

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Example: (e, 30, 42, 30)

Formalisation - Words and register file

Words

Word $\stackrel{def}{=}$

Formalisation - Words and register file

Words

- ▶ Capability

$$\text{Word} \stackrel{\text{def}}{=} \text{---}$$

Formalisation - Words and register file

Words

- ▶ Capability

$$\text{Word} \stackrel{\text{def}}{=} \text{Cap}$$

Formalisation - Words and register file

Words

- ▶ Capability
- ▶ Data (and instructions)

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$$\text{Word} \stackrel{\text{def}}{=} \text{Cap} + \mathbb{Z}$$

Formalisation - Words and register file

Words

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- ▶ In the real machine capabilities are tagged

$$\text{Word} \stackrel{\text{def}}{=} \text{Cap} + \mathbb{Z}$$

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Words

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$$\text{Word} \stackrel{\text{def}}{=} \text{Cap} + \mathbb{Z}$$

Register file

$$\text{Reg} \stackrel{\text{def}}{=}$$

Formalisation - Words and register file

Words

- ▶ Capability
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$$\text{Word} \stackrel{\text{def}}{=} \text{Cap} + \mathbb{Z}$$

Register file

- ▶ Assume finite set of registers $\text{RegisterName} \ni \text{pc}$

$$\text{Reg} \stackrel{\text{def}}{=}$$

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Words

- ▶ Capability
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$$\text{Word} \stackrel{\text{def}}{=} \text{Cap} + \mathbb{Z}$$

Register file

- ▶ Assume finite set of registers $\text{RegisterName} \ni \text{pc}$

$$\text{Reg} \stackrel{\text{def}}{=} \text{RegisterName} \rightarrow \text{Word}$$

Formalisation - Heap and configurations

Heap

$$\text{Heap} \stackrel{\text{def}}{=}$$

Formalisation - Heap and configurations

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- ▶ Map from Addr to Word

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Heap

- ▶ Map from Addr to Word

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Configuration

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$$\text{Conf} \stackrel{\text{def}}{=}$$

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Heap

- ▶ Map from Addr to Word

$$\text{Heap} \stackrel{\text{def}}{=} \text{Addr} \rightarrow \text{Word}$$

Configuration

- ▶ Executable configuration

$$\text{Conf} \stackrel{\text{def}}{=} \text{Reg} \times \text{Heap}$$

Formalisation - Heap and configurations

Heap

- ▶ Map from Addr to Word

$$\text{Heap} \stackrel{\text{def}}{=} \text{Addr} \rightarrow \text{Word}$$

Configuration

- ▶ Executable configuration
- ▶ Successfully halted configuration

$$\text{Conf} \stackrel{\text{def}}{=} \text{Reg} \times \text{Heap}$$

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$$\text{Conf} \stackrel{\text{def}}{=} \text{Reg} \times \text{Heap} \quad + \{ \textit{halted} \} \times \text{Heap}$$

Formalisation - Heap and configurations

Heap

- ▶ Map from Addr to Word

$$\text{Heap} \stackrel{\text{def}}{=} \text{Addr} \rightarrow \text{Word}$$

Configuration

- ▶ Executable configuration
- ▶ Successfully halted configuration
- ▶ Failed configuration

$$\text{Conf} \stackrel{\text{def}}{=} \text{Reg} \times \text{Heap} + \{ \textit{failed} \} + \{ \textit{halted} \} \times \text{Heap}$$

Formalisation - Instructions

Syntax

Instructions ::=

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$$rn ::= n \mid r$$

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Formalisation - Instructions

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Formalisation - Instructions

Syntax

- ▶ The normal instructions

$$\begin{aligned} rn &::= n \mid r \\ \text{Instructions} &::= \text{jmp } r \mid \text{jnz } r \ rn \mid \text{move } r \ rn \mid \\ &\quad \text{load } r \ r \mid \text{store } r \ r \mid \text{plus } r \ rn \ rn \end{aligned}$$

Formalisation - Instructions

Syntax

- ▶ The normal instructions
- ▶ The capability manipulation instructions

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Formalisation - Instructions

Syntax

- ▶ The normal instructions
- ▶ The capability manipulation instructions
- ▶ Instructions for stopping the machine

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Formalisation - Operational Semantics (1)

Execution relation

$$\rightarrow \subseteq (\text{Reg} \times \text{Heap}) \times \text{Conf}$$

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$$\Phi.\text{reg}(\text{pc}) = (\text{perm}, \text{base}, \text{end}, a)$$

$$\text{executionAllowed}(\Phi)$$

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$$\frac{\text{executionAllowed}(\Phi) \quad i = \Phi.\text{heap}(a)}{\Phi \rightarrow i}$$

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Formalisation - Operational Semantics (2)

$$\llbracket \text{load } r_1 \ r_2 \rrbracket (\Phi) =$$

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$$w = \Phi.\text{heap}(r_2)$$

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Formalisation - Operational Semantics (2)

$$w = \Phi.\text{heap}(a) \quad \Phi.\text{reg}(r_2) = (\text{perm}, \text{base}, \text{end}, a)$$

$$\llbracket \text{load } r_1 \ r_2 \rrbracket (\Phi) = \Phi[\text{reg}.r_1 \mapsto w]$$

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$$\overline{\text{updatePc}(\Phi) = \Phi[\text{reg}.pc \mapsto \quad]}$$

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$$\Phi.\text{reg}(\text{pc}) = (\text{perm}, \text{base}, \text{end}, a)$$

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$$\frac{w = \Phi.\text{heap}(a) \quad \Phi.\text{reg}(r_2) = (\text{perm}, \text{base}, \text{end}, a) \quad \text{perm} \in \{\text{ro}, \text{rw}, \text{rx}, \text{rwx}\} \quad \text{base} \leq a \leq \text{end}}{\llbracket \text{load } r_1 \ r_2 \rrbracket (\Phi) = \text{updatePc}(\Phi[\text{reg}.r_1 \mapsto w])}$$

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Formalisation - Operational Semantics (3)

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- ▶ Need a *failed* case for each of the rules
- ▶ The operational semantics of the remaining instructions defined in a similar fashion

Road map

Capability Machine

Formalisation

Example program

Logical Relation

Example revisited

Current work

Example program

- ▶ High-level programs - ML style

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let f = fun adv =>  
    let l = 1 in  
    adv();  
    assert (l == 1)
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```
let f = fun adv =>  
    let l = 1 in  
    adv();  
    assert (l == 1)
```

Lemma

Given any program `adv`, `f(adv)` either runs forever, ends up in the *failed* configuration, or halts in a configuration where the assertion flag is 0.

Road map

Capability Machine

Formalisation

Example program

Logical Relation

Example revisited

Current work

Logical Relation - What is it

Logical relations in general

- ▶ Strong proof method

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- ▶ Can be used when a direct proof does not suffice
 - ▶ e.g., strong normalisation for STLC
- ▶ Can be used to reason about programs written in “real” programming languages
- ▶ Extensional - not interested in what happens during the execution, only interested in the result

Logical Relation

What we hope to achieve

- ▶ Any program will respect the limitations of the capability system.

Logical Relation

The property of this logical relation

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The property of this logical relation

- ▶ Any capability such that
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 - ▶ the execution will either
 - ▶ diverge

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Logical Relation

The property of this logical relation

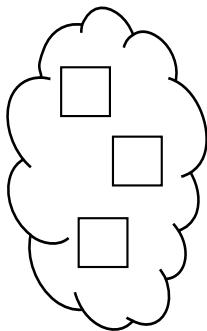
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Logical Relation - Worlds, modelling the heap

World

- ▶ Collection of regions with invariants (e.g. $h(27) \mapsto 5$)

W

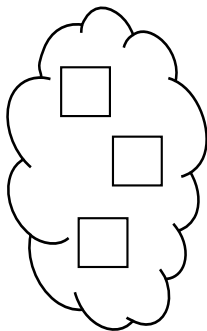


Logical Relation - Worlds, modelling the heap

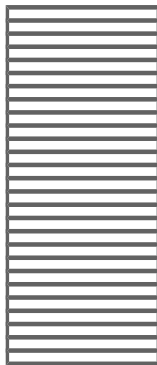
World

- ▶ Collection of regions with invariants (e.g. $h(27) \mapsto 5$)
- ▶ Model of the heap

W



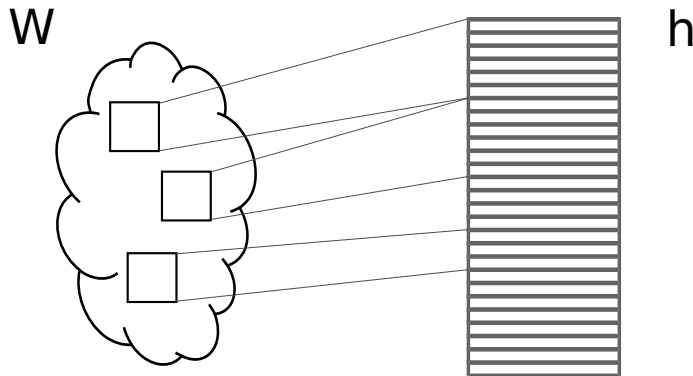
h



Logical Relation - Worlds, modelling the heap

Heap satisfaction

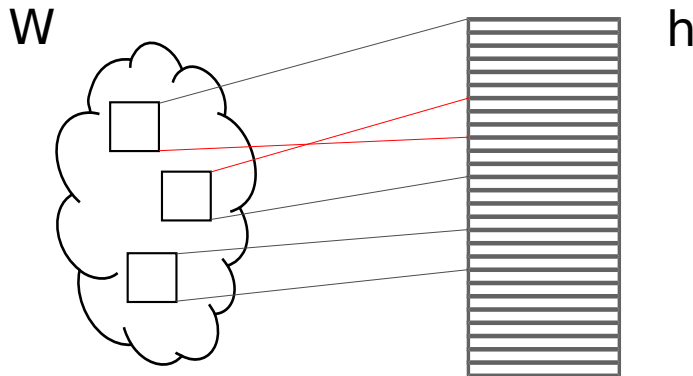
- ▶ Regions model parts of the heap



Logical Relation - Worlds, modelling the heap

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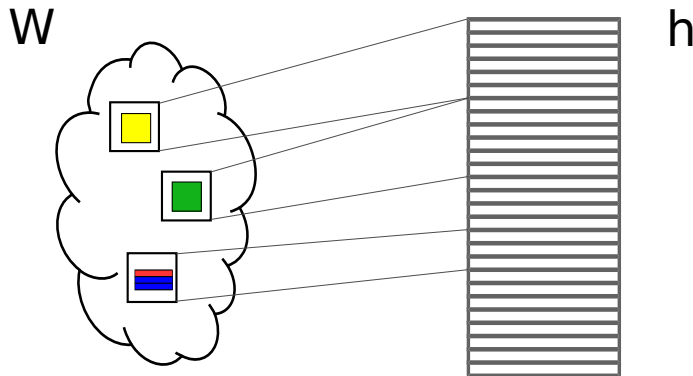
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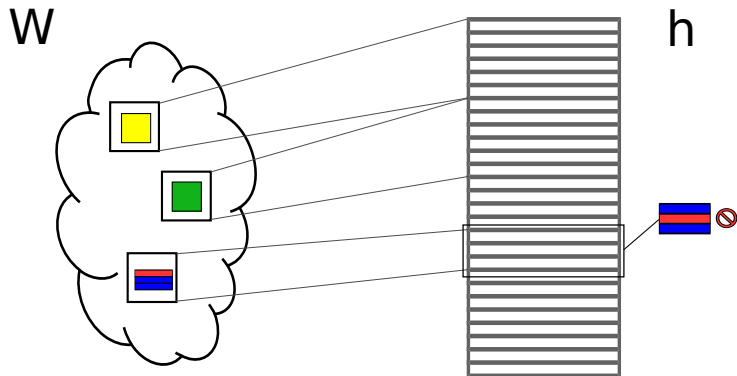
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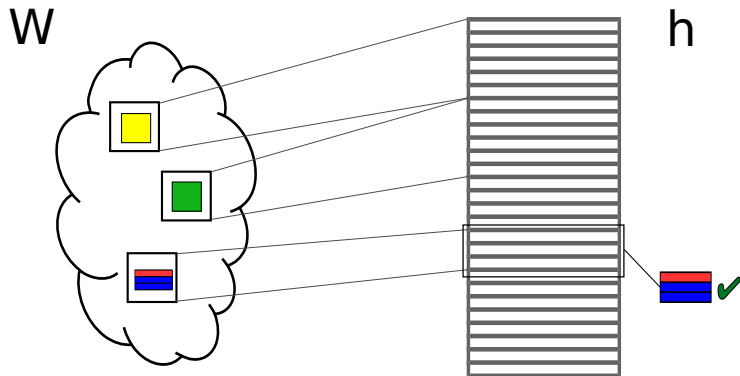
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Logical Relation - Worlds, modelling the heap

Heap satisfaction

- ▶ Regions model parts of the heap
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- ▶ $h : W$

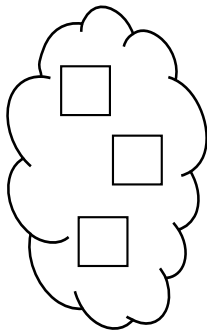


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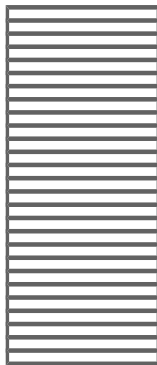
Future World

- ▶ Heap changes over time, worlds have to cope with this:
- ▶ W
 - ▶ Same regions as before

W



h

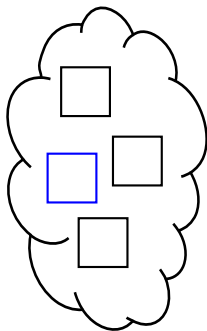


Logical Relation - Worlds, modelling the heap

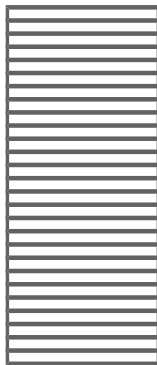
Future World

- ▶ Heap changes over time, worlds have to cope with this:
- ▶ $W' \sqsupseteq W$
 - ▶ Same regions as before
 - ▶ New region(s)

W'



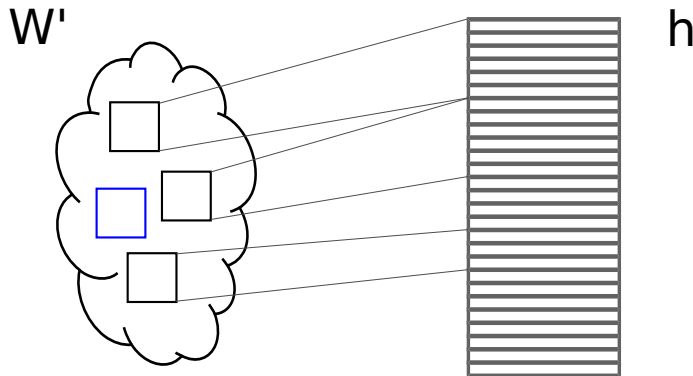
h



Logical Relation - Worlds, modelling the heap

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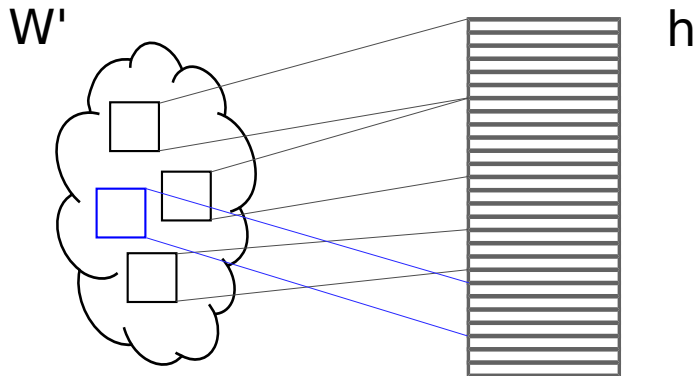
- ▶ Old regions model the same parts of the heap as before



Logical Relation - Worlds, modelling the heap

Future World

- ▶ Old regions model the same parts of the heap as before
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Logical Relation

The property of this logical relation

- ▶ Any capability such that
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Logical Relation - Observation relation

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$$\forall h : W.$$

$$(\text{reg}[\text{pc} \mapsto c], h) \in \mathcal{O}(W)\}$$

Logical Relation - Register-file relation

“Well-behaved” register-file

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Logical Relation - Register-file relation

“Well-behaved” register-file

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Logical Relation - Register-file relation

“Well-behaved” register-file

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Logical Relation - Register-file relation

“Well-behaved” register-file

- ▶ All registers but the pc-register
 - ▶ pc was overwritten in the \mathcal{E} anyway
- ▶ should contain a “well-behaved” word

$$\mathcal{R} \stackrel{\text{def}}{=} \lambda W. \{ \text{reg} \mid \forall r \in \text{RegisterName} \setminus \{\text{pc}\}. \\ \text{reg}(r) \in \mathcal{V}(W) \}$$

Logical Relation - Value relation

“Well-behaved words”

$$\begin{aligned} \mathcal{V} \stackrel{\text{def}}{=} & \lambda W. \{i \mid i \in \mathbb{Z}\} \cup \\ & \{(o, \text{base}, \text{end}, a)\} \cup \\ & \{(ro, \text{base}, \text{end}, a) \mid \} \cup \\ & \{(rw, \text{base}, \text{end}, a) \mid \} \cup \\ & \{(rx, \text{base}, \text{end}, a) \mid \} \cup \\ & \{(e, \text{base}, \text{end}, a) \mid \} \cup \\ & \{(rwx, \text{base}, \text{end}, a) \mid \} \end{aligned}$$

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Logical Relation - Value relation

“Well-behaved words”

$$\begin{aligned} \mathcal{V} \stackrel{\text{def}}{=} & \lambda W. \{i \mid i \in \mathbb{Z}\} \cup \\ & \{(o, \text{base}, \text{end}, a)\} \cup \\ & \{(ro, \text{base}, \text{end}, a) \mid \text{readCondition}(\text{base}, \text{end}, W)\} \cup \\ & \{(rw, \text{base}, \text{end}, a) \mid \text{readCondition}(\text{base}, \text{end}, W) \wedge \\ & \quad \text{writeCondition}(\text{base}, \text{end}, W)\} \cup \\ & \{(rx, \text{base}, \text{end}, a) \mid \text{readCondition}(\text{base}, \text{end}, W) \wedge \\ & \quad \text{executeCondition}(\text{base}, \text{end}, W)\} \cup \\ & \{(e, \text{base}, \text{end}, a) \mid \quad \quad \quad \cup \\ & \{(rwx, \text{base}, \text{end}, a) \mid \text{readCondition}(\text{base}, \text{end}, W) \wedge \\ & \quad \text{writeCondition}(\text{base}, \text{end}, W) \wedge \\ & \quad \text{executeCondition}(\text{base}, \text{end}, W)\} \end{aligned}$$

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Logical Relation - Execute and enter conditions

Execution condition

$$\textit{executeCondition}(\textit{base}, \textit{end}, W) \stackrel{\textit{def}}{=}$$

Logical Relation - Execute and enter conditions

Execution condition

- ▶ May be used at any point in the future

$$\begin{aligned} \text{executeCondition}(\text{base}, \text{end}, W) &\stackrel{\text{def}}{=} \\ &\forall W' \sqsubseteq W. \end{aligned}$$

Logical Relation - Execute and enter conditions

Execution condition

- ▶ May be used at any point in the future
- ▶ Can be executed from any address in the range of authority

$$\begin{aligned} \text{executeCondition}(\text{base}, \text{end}, W) &\stackrel{\text{def}}{=} \\ &\forall W' \sqsubseteq W. \\ &\forall a \in [\text{base}, \text{end}]. \end{aligned}$$

Logical Relation - Execute and enter conditions

Execution condition

- ▶ May be used at any point in the future
- ▶ Can be executed from any address in the range of authority
- ▶ Should produce a “well-behaved” result, i.e., it should be in the \mathcal{E} -relation

$$\begin{aligned} \text{executeCondition}(\text{base}, \text{end}, W) &\stackrel{\text{def}}{=} \\ &\forall W' \sqsupseteq W. \\ &\forall a \in [\text{base}, \text{end}]. \\ &(\text{rx}, \text{base}, \text{end}, a) \in \mathcal{E}(W') \end{aligned}$$

Logical Relation - Execute and enter conditions

Enter condition

$enterCondition(base, end, a, W) \stackrel{def}{=}$

Logical Relation - Execute and enter conditions

Enter condition

- ▶ May be used at any point in the future

$$\text{enterCondition}(\text{base}, \text{end}, a, W) \stackrel{\text{def}}{=} \\ \forall W' \sqsubseteq W.$$

Logical Relation - Execute and enter conditions

Enter condition

- ▶ May be used at any point in the future
- ▶ Can only be executed from the specified address

$$\text{enterCondition}(\text{base}, \text{end}, a, W) \stackrel{\text{def}}{=} \\ \forall W' \sqsubseteq W.$$

Logical Relation - Execute and enter conditions

Enter condition

- ▶ May be used at any point in the future
- ▶ Can only be executed from the specified address
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$$\begin{aligned} \text{enterCondition}(\text{base}, \text{end}, a, W) &\stackrel{\text{def}}{=} \\ &\forall W' \sqsubseteq W. \\ &(\text{rx}, \text{base}, \text{end}, a) \in \mathcal{E}(W') \end{aligned}$$

Logical Relation - Read and write conditions

Read condition

- ▶ World models heap, so it describes what we might read

$$readCondition(base, end, W) \stackrel{def}{=}$$

Logical Relation - Read and write conditions

Read condition

- ▶ World models heap, so it describes what we might read
- ▶ Some region should govern the part of the heap we can read from

$$\text{readCondition}(\text{base}, \text{end}, W) \stackrel{\text{def}}{=} \\ \exists r \in \text{RegionName}.$$

Logical Relation - Read and write conditions

Read condition

- ▶ World models heap, so it describes what we might read
- ▶ Some region should govern the part of the heap we can read from
- ▶ The region may govern a larger part of the heap

$$\begin{aligned} readCondition(base, end, W) &\stackrel{def}{=} \\ &\exists r \in \text{RegionName}. \\ &\exists [base', end'] \supseteq [base, end]. \end{aligned}$$

Logical Relation - Read and write conditions

Read condition

- ▶ The region should be subset of the standard region $\iota_{base', end'}$

$$\begin{aligned} readCondition(base, end, W) &\stackrel{def}{=} \\ &\exists r \in \text{RegionName}. \\ &\exists [base', end'] \supseteq [base, end]. \\ &W(r) \subseteq \iota_{base', end'} \end{aligned}$$

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 - ▶ All the words in the heap segment should be in the \mathcal{V} -relation

Logical Relation - Read and write conditions

Read condition

- ▶ The region should be subset of the standard region $\iota_{base', end'}$
- ▶ Intuition:
 - ▶ If untrusted code got this capability, then it should only be able to read “well-behaved” words.

$$\begin{aligned} readCondition(base, end, W) &\stackrel{def}{=} \\ &\exists r \in \text{RegionName}. \\ &\exists [base', end'] \supseteq [base, end]. \\ &W(r) \subseteq \iota_{base', end'} \end{aligned}$$

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Logical Relation - Read and write conditions

Write condition

- ▶ World should describe what we are allowed write

$$\text{writeCondition}(\text{base}, \text{end}, W) \stackrel{\text{def}}{=}$$

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Logical Relation - Read and write conditions

Write condition

- ▶ World should describe what we are allowed write
- ▶ Some region governs the part of the heap we may write to

$$\begin{aligned} \text{writeCondition}(\text{base}, \text{end}, W) &\stackrel{\text{def}}{=} \\ &\exists r \in \text{RegionName}. \\ &\exists [\text{base}', \text{end}'] \supseteq [\text{base}, \text{end}]. \end{aligned}$$

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Write condition

- ▶ The region should be *superset* of the standard region $\iota_{base', end'}$

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- ▶ $\iota_{base', end'}$ is a standard region that requires
 - ▶ Range of heap segment to be $[base', end']$
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Write condition

- ▶ The region should be *superset* of the standard region $\iota_{base', end'}$
- ▶ Intuition:
 - ▶ If untrusted code got this capability, then it can at least write something well-behaved, but also other things.

$$\begin{aligned} writeCondition(base, end, W) &\stackrel{def}{=} \\ &\exists r \in \text{RegionName}. \\ &\exists [base', end'] \supseteq [base, end]. \\ &W(r) \supseteq \iota_{base', end'} \end{aligned}$$

- ▶ $\iota_{base', end'}$ is a standard region that requires
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 - ▶ All the words in the heap segment should be in the \mathcal{V} -relation

Fundamental theorem of logical relations

Lemma (FTLR)

For all $W \in \text{World}$ and $c \in \text{Caps}$,

$$c \in \mathcal{E}(W).$$

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Fundamental theorem of logical relations

Lemma (FTLR)

For all $W \in \text{World}$ and $c \in \text{Caps}$,

$$c \in \mathcal{E}(W).$$

- ▶ The pc-register can be accessed like any other register
- ▶ Capability must behave when used for read/write

Fundamental theorem of logical relations

Lemma (FTLR)

For all $W \in \text{World}$, $perm \in \text{Perm}$, and $base, end, a \in \text{Addr}$,

if

$perm = \text{rx}$ and $\text{readCondition}(W, base, end)$,

or

$perm = \text{rwx}$ and $\text{read-/writeCond}(W, base, end)$

then

$(perm, base, end, a) \in \mathcal{E}(W)$.

Road map

Capability Machine

Formalisation

Example program

Logical Relation

Example revisited

Current work

Example: local state revisited

Lemma

Given any program adv , $f(\text{adv})$ either runs forever, ends up in the *failed* configuration, or halts in a configuration where the assertion flag is 0.

```
let f = fun adv =>
  let l = 1 in
  adv();
  assert (l == 1)
```

Example: local state revisited

Proof sketch

- ▶ Assuming `adv` is only code and given as enter capability

```
let f = fun adv =>  
    let l = 1 in  
    adv();  
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```

Example: local state revisited

Proof sketch

- ▶ Assuming `adv` is only code and given as enter capability
- ▶ Run program until just after the jump to `adv`

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let f = fun adv =>  
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Example: local state revisited

Proof sketch

- ▶ Assuming `adv` is only code and given as enter capability
- ▶ Run program until just after the jump to `adv`
- ▶ Define world with the following regions:

```
let f = fun adv =>  
    let l = 1 in  
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Example: local state revisited

Proof sketch

- ▶ Assuming `adv` is only code and given as enter capability
- ▶ Run program until just after the jump to `adv`
- ▶ Define world with the following regions:
 - ▶ `f` code remains unchanged

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- ▶ Run program until just after the jump to `adv`
- ▶ Define world with the following regions:
 - ▶ `f` code remains unchanged
 - ▶ `l` remains 1
 - ▶ standard region governs `adv`

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- ▶ Assuming `adv` is only code and given as enter capability
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 - ▶ `f` code remains unchanged
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- ▶ Use FTLR on `adv` capability

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let f = fun adv =>  
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Example: local state revisited

Proof sketch (continued)

- ▶ Use FTLR on adv capability

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let f = fun adv =>  
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Example: local state revisited

Proof sketch (continued)

- ▶ Use FTLR on adv capability
- ▶ By design, the heap satisfies the world

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let f = fun adv =>  
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Example: local state revisited

Proof sketch (continued)

- ▶ Use FTLR on adv capability
- ▶ By design, the heap satisfies the world
- ▶ Register-file in \mathcal{R} -relation:

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Example: local state revisited

Proof sketch (continued)

- ▶ Use FTLR on adv capability
- ▶ By design, the heap satisfies the world
- ▶ Register-file in \mathcal{R} -relation:
 - ▶ All registers but two contain 0, so trivial.

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Proof sketch (continued)

- ▶ Use FTLR on adv capability
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 - ▶ One is pc-register, so we don't care about it.

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let f = fun adv =>  
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    adv();  
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```


Example: local state revisited

Proof sketch (continued)

- ▶ Use FTLR on `adv` capability
- ▶ By design, the heap satisfies the world
- ▶ Register-file in \mathcal{R} -relation:
 - ▶ All registers but two contain 0, so trivial.
 - ▶ One is `pc`-register, so we don't care about it.
 - ▶ The other is the continuation (passed as `enter` capability), so *enterCondition* must hold

```
let f = fun adv =>
  let l = 1 in
  adv();
  assert (l == 1)
```

Example: local state revisited

Proof sketch (continued)

- ▶ World highlights:
 - ▶ `f` code remains unchanged
 - ▶ `l` remains 1
 - ▶ assertion flag is 0
- ▶ The continuation satisfies *enterCondition*:

```
let f = fun adv =>  
    let l = 1 in  
    adv();  
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```

Example: local state revisited

Proof sketch (continued)

- ▶ World highlights:
 - ▶ `f` code remains unchanged
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 - ▶ assertion flag is 0
- ▶ The continuation satisfies *enterCondition*:
 - ▶ In a future world, the continuation must be in \mathcal{E}

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let f = fun adv =>  
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Proof sketch (continued)

- ▶ World highlights:
 - ▶ `f` code remains unchanged
 - ▶ `l` remains 1
 - ▶ assertion flag is 0
- ▶ The continuation satisfies *enterCondition*:
 - ▶ In a future world, the continuation must be in \mathcal{E}
 - ▶ Executing from continuation, `l` is still 1, so assertion does not fail.

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Example: local state revisited

Proof sketch (continued)

- ▶ World highlights:
 - ▶ `f` code remains unchanged
 - ▶ `l` remains 1
 - ▶ assertion flag is 0
- ▶ The continuation satisfies *enterCondition*:
 - ▶ In a future world, the continuation must be in \mathcal{E}
 - ▶ Executing from continuation, `l` is still 1, so assertion does not fail.
 - ▶ Execution halts and assertion flag is 0

```
let f = fun adv =>  
    let l = 1 in  
    adv();  
    assert (l == 1)
```

Example: local state revisited

Proof sketch (continued)

- ▶ Backtracking a lot, we have just shown that the register-file was in the \mathcal{R} -relation

```
let f = fun adv =>  
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    adv();  
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```

Example: local state revisited

Proof sketch (continued)

- ▶ Backtracking a lot, we have just shown that the register-file was in the \mathcal{R} -relation
- ▶ By $\text{adv} \in \mathcal{E}$: execution diverges, fails, or terminates without the assertion failing.

```
let f = fun adv =>  
    let l = 1 in  
    adv();  
    assert (l == 1)
```

Example: local state revisited

Lemma

Given any program adv , $f(\text{adv})$ either runs forever, ends up in the *failed* configuration, or halts in a configuration where the assertion flag is 0.

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```


Road map

Capability Machine

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Current work

What are we working on now?

```
let f = fun adv =>  
  let l = 0 in  
    adv();  
    assert(l == 0);  
    l := 1;  
    adv()
```

What are we working on now?

```
let f = fun adv =>  
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    adv();  
    assert(l == 0);  
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```

- Assuming standard calling convention, can we show that the assertion never fails?

What are we working on now?

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let f = fun adv =>  
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```

- ▶ Assuming standard calling convention, can we show that the assertion never fails?
 - ▶ No,

What are we working on now?

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let f = fun adv =>  
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- ▶ Assuming standard calling convention, can we show that the assertion never fails?
 - ▶ No, `adv` may save the continuation from the first call

What are we working on now?

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let f = fun adv =>  
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    l := 1;  
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```

- ▶ Assuming standard calling convention, can we show that the assertion never fails?
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Local capabilities

What are we working on now?

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let f = fun adv =>  
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    adv();  
    assert(l == 0);  
    l := 1;  
    adv()
```

- ▶ Assuming standard calling convention, can we show that the assertion never fails?
 - ▶ No, `adv` may save the continuation from the first call

Local capabilities

- ▶ *local/global* capabilities

What are we working on now?

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let f = fun adv =>  
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    assert(l == 0);  
    l := 1;  
    adv()
```

- ▶ Assuming standard calling convention, can we show that the assertion never fails?
 - ▶ No, *adv* may save the continuation from the first call

Local capabilities

- ▶ *local/global* capabilities
- ▶ *permit write local* capabilities

What are we working on now?

```
let f = fun adv =>  
  let l = 0 in  
    adv();  
    assert(l == 0);  
    l := 1;  
    adv()
```

- ▶ Assuming standard calling convention, can we show that the assertion never fails?
 - ▶ No, *adv* may save the continuation from the first call

Local capabilities

- ▶ *local/global* capabilities
- ▶ *permit write local* capabilities
- ▶ *Local* capabilities can only be stored through *permit write local* capabilities

Questions?

References

- [1] Jonathan Woodruff, Robert N.M. Watson, David Chisnall, Simon W. Moore, Jonathan Anderson, Brooks Davis, Ben Laurie, Peter G. Neumann, Robert Norton, and Michael Roe. The cheri capability model: Revisiting risc in an age of risk. In *International Symposium on Computer Architecture*, pages 457–468, Piscataway, NJ, USA, 2014. IEEE Press.