Tales of Belgium: Reasoning about Capability Machines using Logical Relations

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Road map

Capability Machine

Formalisation

Example, Macros, and Stack Discipline

Logical Relation

Conclusion

Leuven

Leuven

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Conclusion

Why should I care about capability machines?

Current low-level protection mechanisms

- Coarse-grained compartmentalisation
- Expensive context switches
- Well suited for high-level applications
- Does not scale well
- E.g., virtual memory

Why should I care about capability machines?

Capability machines

- Fine-grained compartmentalisation
- Cheap compartments
- Fine-grained sharing
- Well suited for applications with need for many compartments

Capabilities

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What is a capability in a capability machine?

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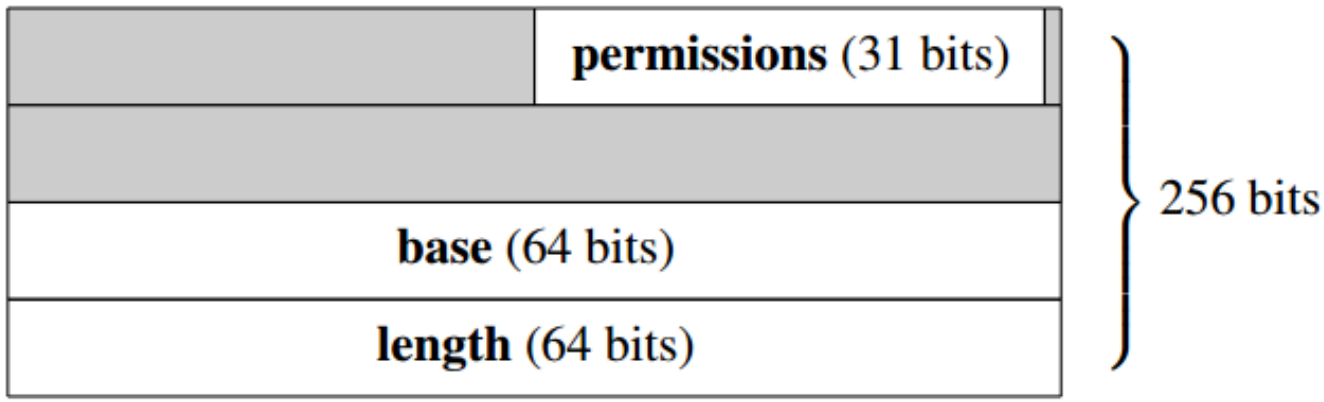

Figure: CHERI capability [1]

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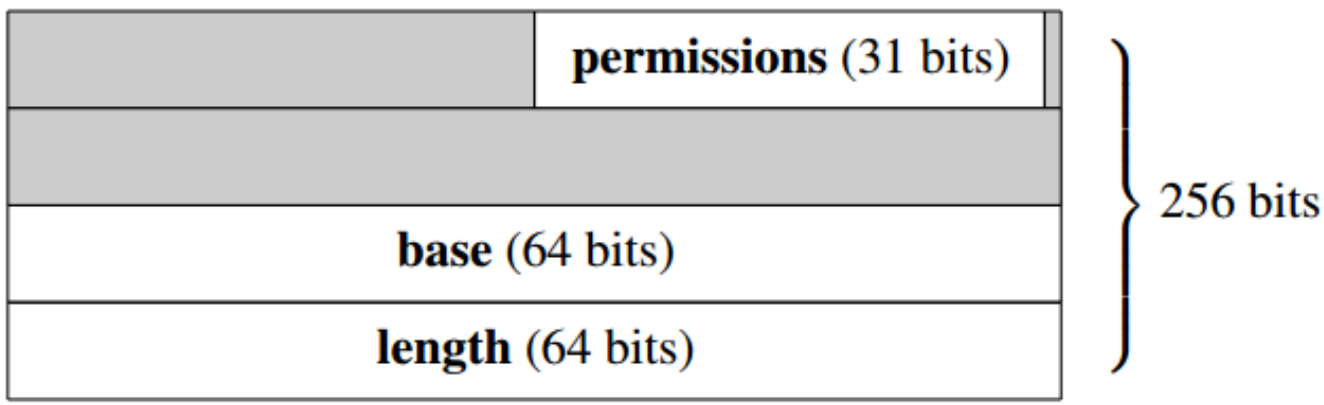

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- Range of memory
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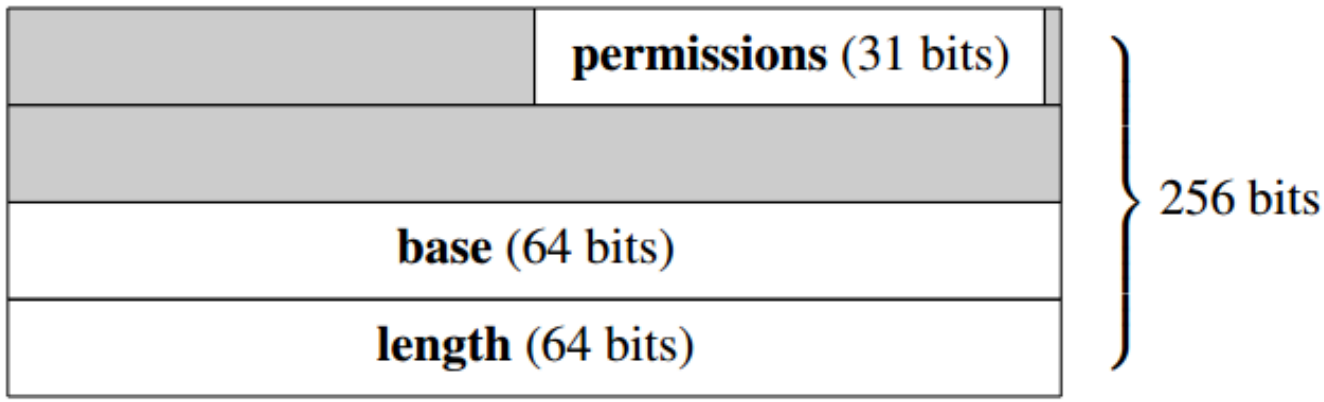

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- Read
- Write
- Execute

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  - Used by distrusting pieces of code to cross security boundaries
  - Modularisation

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  - `lea`, `restrict`, `subseg`
  - No instruction generates new capability
  - Manipulation of capabilities cannot result in authority amplification

Capability machine overview

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- Capability aware instructions
- Memory and registers
  - Can contain data and capabilities
  - Capabilities tagged

Simple capability machine limitations

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  - Does not scale to other types of permissions

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- Only pwl-capabilities can write local capabilities.
- Gives simple temporal revocation, but
  - requires no global pwl-capabilities
  - enforcement depends on programming discipline.

Brussels

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Formalisation - Permissions

Permissions

- To simplify matters, we only allow certain combinations of permissions

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$$\mathrm{Perm} \stackrel{def}{=} \{\mathrm{o}, \qquad\qquad\qquad\qquad\qquad\qquad \}$$

Formalisation - Permissions

Permissions

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- No permissions, read only,

$$\mathrm{Perm} \stackrel{def}{=} \{\mathrm{o}, \mathrm{ro}, \qquad\qquad\qquad\qquad\qquad \}$$

Formalisation - Permissions

Permissions

- To simplify matters, we only allow certain combinations of permissions
- No permissions, read only, read-write,

$$\mathrm{Perm} \stackrel{def}{=} \{\mathrm{o}, \mathrm{ro}, \mathrm{rw}, \qquad\qquad\qquad\qquad \}$$

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$$\mathrm{Perm} \stackrel{def}{=} \{\mathrm{o}, \mathrm{ro}, \mathrm{rw}, \qquad \mathrm{rx}, \qquad\qquad \}$$

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Formalisation - Permissions

Permissions

- To simplify matters, we only allow certain combinations of permissions
- No permissions, read only, read-write, read-'write-local' read-execute, enter, read-write-execute, read-'write-local'-execute

$$\mathrm{Perm} \stackrel{def}{=} \{\mathrm{o}, \mathrm{ro}, \mathrm{rw}, \mathrm{rwl}, \mathrm{rx}, \mathrm{e}, \mathrm{rwx}, \mathrm{rwlx}\}$$

Formalisation - Permissions

Permissions ordering

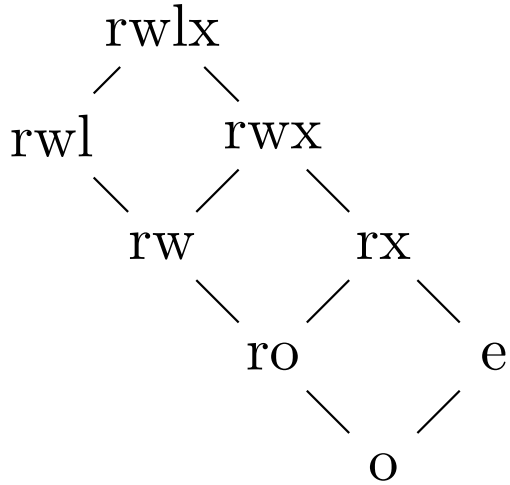

Figure: Permission hierarchy

Formalisation - Locality

Locality

$$\text{Global} ::= \{\text{global}, \text{local}\}$$

Locality ordering

$$\begin{array}{c} \text{global} \\ | \\ \text{local} \end{array}$$

Figure: Locality hierarchy

Formalisation - Capabilities

Capability

$$\mathrm{Cap} \stackrel{def}{=}$$

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$$\mathrm{Addr} \stackrel{def}{=} \mathbb{N}$$

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Formalisation - Capabilities

Capability

- Permission and locality
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- Pointer

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Example: $((\mathrm{e}, \mathrm{local}), 30, 42, 30)$

Formalisation - Words and register file

Words

$$\mathrm{Word} \stackrel{def}{=}$$

Formalisation - Words and register file

Words

- Capability

$$\text{Word} \stackrel{def}{=}$$

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Words

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Register file

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- Assume finite set of registers $\mathrm{RegisterName} \ni \mathrm{pc}$

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Register file

- Assume finite set of registers $\mathrm{RegisterName} \ni \mathrm{pc}$

$$\mathrm{Reg} \stackrel{def}{=} \mathrm{RegisterName} \to \mathrm{Word}$$

Formalisation - Memory and configurations

Memory

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Formalisation - Memory and configurations

Memory

- Map from Addr to Word

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- Failed configuration

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Formalisation - Instructions

Syntax

$$\text{Instructions} \quad ::=$$

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\begin{array}{rcl}
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 & & \texttt{gete}\ r\ r \mid \texttt{geta}\ r\ r
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Formalisation - Instructions

Syntax

- The normal instructions
- The capability manipulation instructions
- Instructions to stop the machine

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 & & \texttt{gete}\ r\ r \mid \texttt{geta}\ r\ r \mid \texttt{fail} \mid \texttt{halt}
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Formalisation - Operational Semantics (2)

$$[\![\texttt{store}\ r_1\ r_2]\!](\Phi) =$$

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$$w = \Phi.\mathrm{reg}(r_2)$$

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Formalisation - Operational Semantics (2)

$$\frac{w = \Phi.\mathrm{reg}(r_2) \qquad \Phi.\mathrm{reg}(r_1) = (perm, base, end, a)}{[\![\texttt{store}\ r_1\ r_2]\!](\Phi) = \qquad \Phi[\mathrm{mem}.a \mapsto w]}$$

Formalisation - Operational Semantics (2)

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- The operational semantics of the remaining instructions is defined in a similar fashion

Antwerp

Road map

Capability Machine

Formalisation

Example, Macros, and Stack Discipline

Logical Relation

Conclusion

The “awkward” example

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g = fun _ =>
      let x = 0 in
      fun adv =>
        x := 0;
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- Need to define some macros to make a readable translation.

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  - allocates a *fresh* piece of memory of size n
  - leaves a global capability with rwx permission in register r

The “awkward” example (naive translation)

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`scall` $r(\bar{r}_{args}, \bar{r}_{priv})$

- $\bar{r}_{args}$ list of argument registers
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- r register to jump to

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  - Upon return: Run the on stack restoration code
  - Return address in caller-code: Restore "private" state

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        x := 0;
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- `mclear` *r*

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g = fun _ =>
      let x = 0 in
      fun adv =>
        x := 0;
        adv();
        x := 1;
        adv();
        assert(x == 1)
```

---

g : malloc r_2 1
store r_2 0
move pc r_3
lea r_3 ...
crtcls $[(x, r_2)]$ r_3

jmp r_0

f : store x 0
scall $r_1([], [r_0, r_1])$
store x 1
scall $r_1([], [r_0])$
load r_1 x
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The "awkward" example (final version)

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---

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crtcls [(x, r2)] r3
rclear RN \ {pc, r0, r1}
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```

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  - If it looks like a stack, works like a stack, and quacks like a stack, then it is probably a stack.
- In the presence of an untrusted stack capability, only use global callbacks.

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Bruges

Road map

Capability Machine

Formalisation

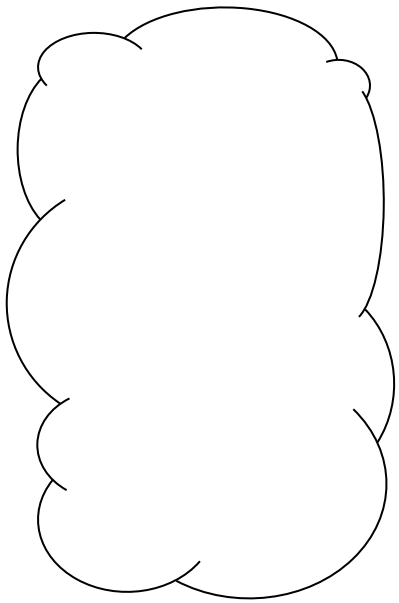
Example, Macros, and Stack Discipline

Logical Relation

Conclusion

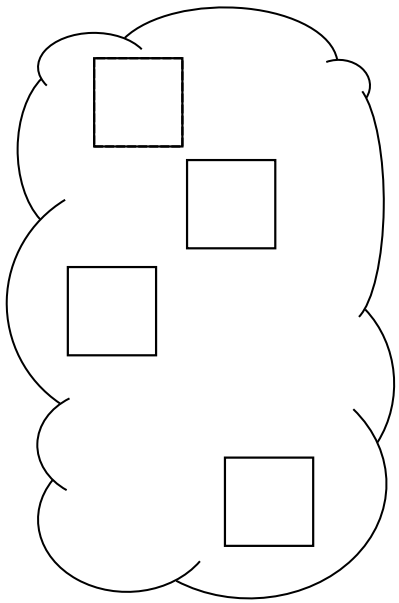
Worlds

World



Worlds

World



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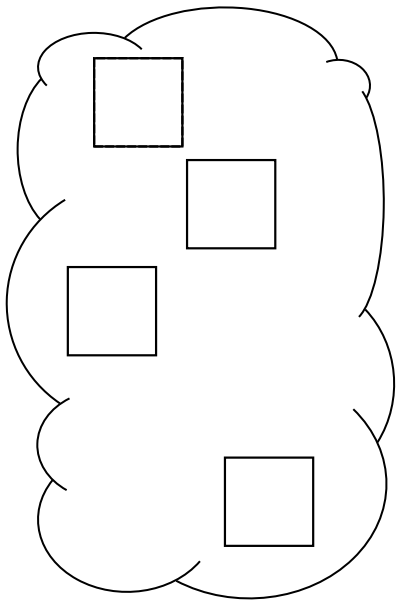
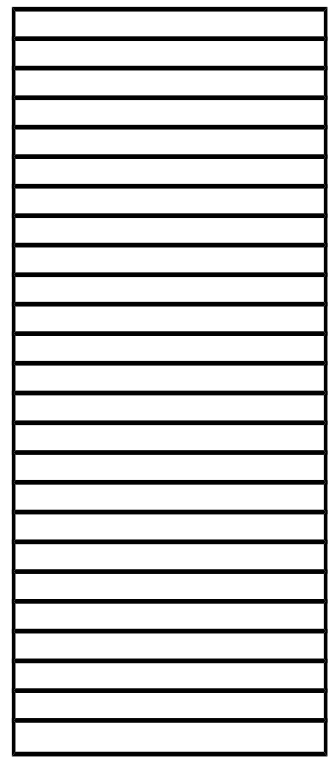
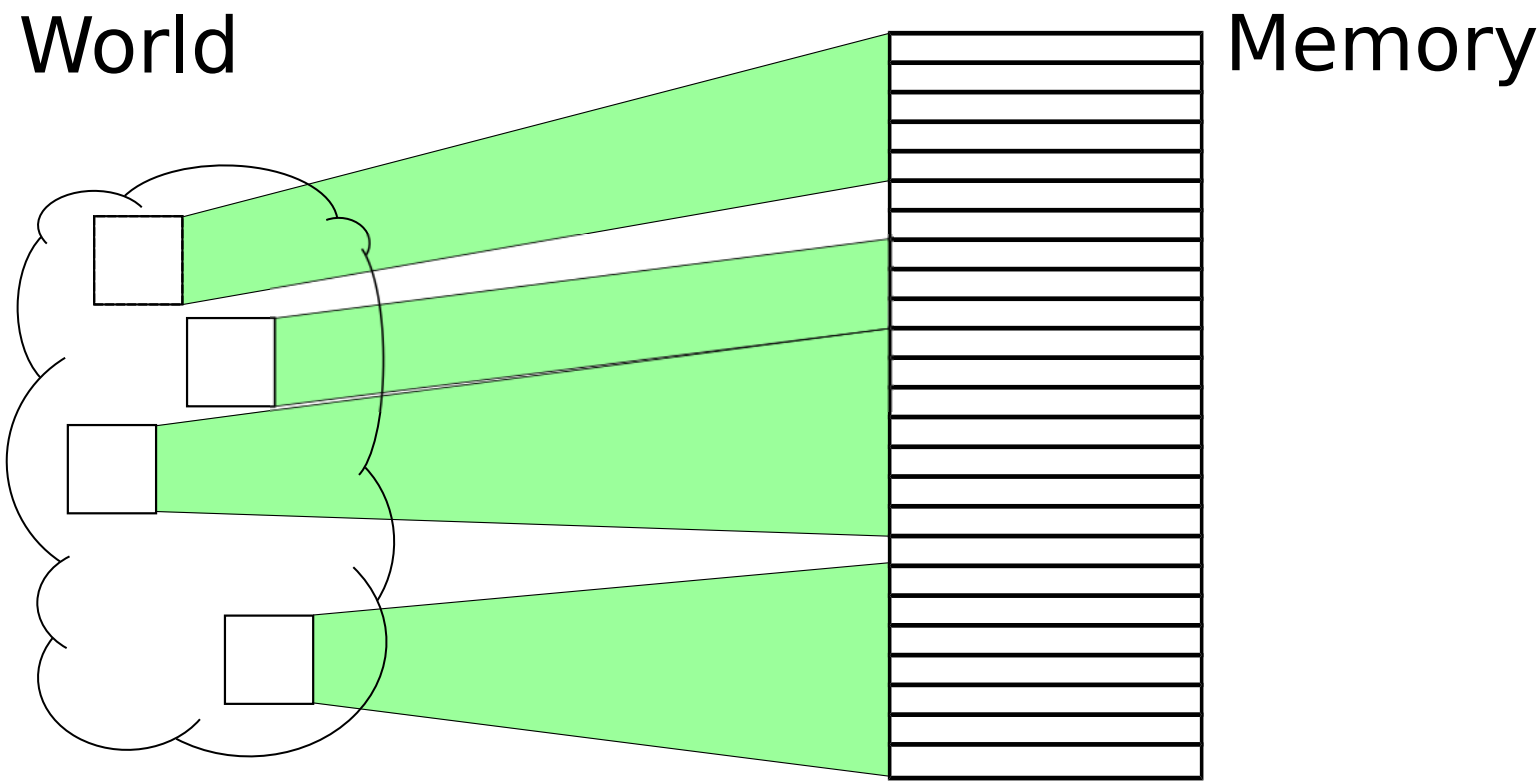




Memory

Worlds



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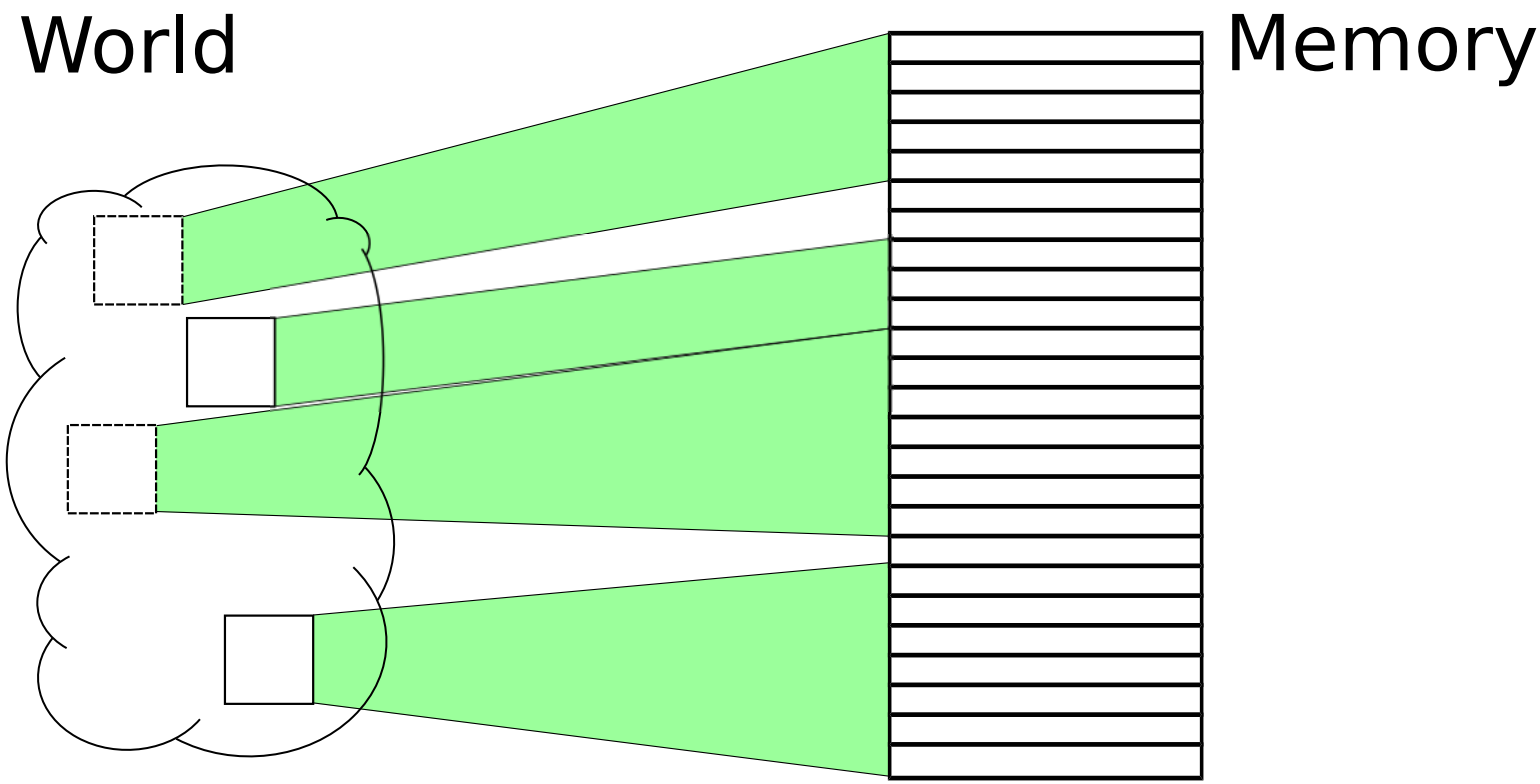

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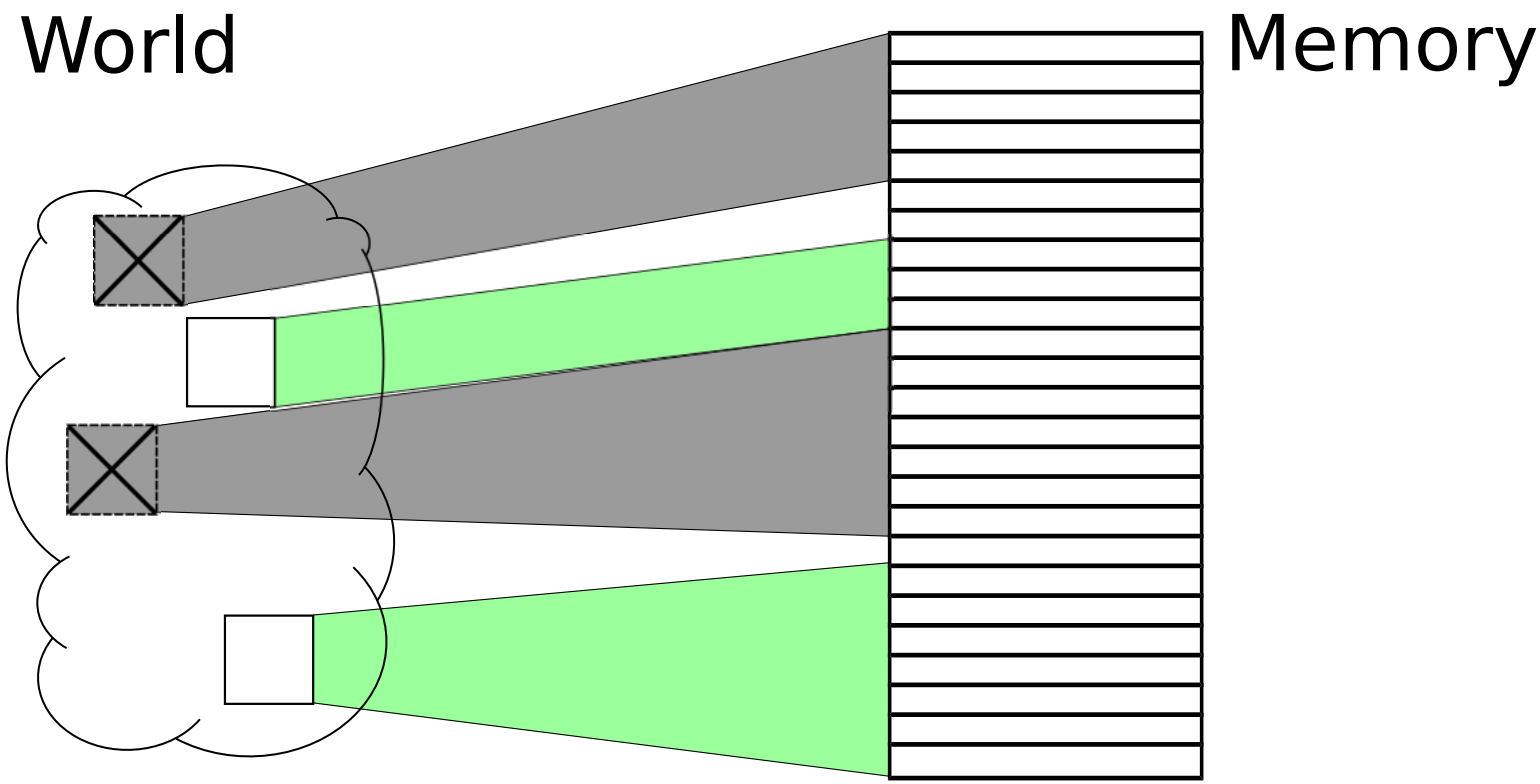

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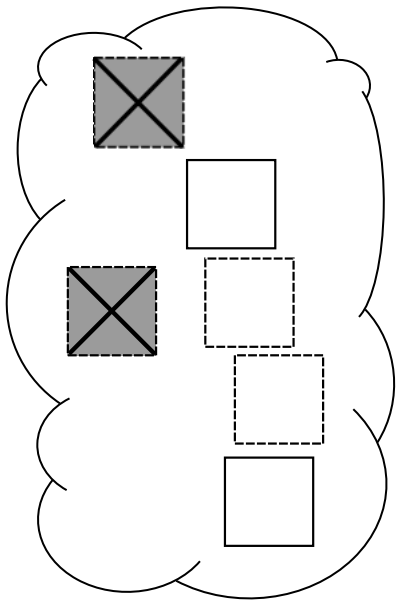

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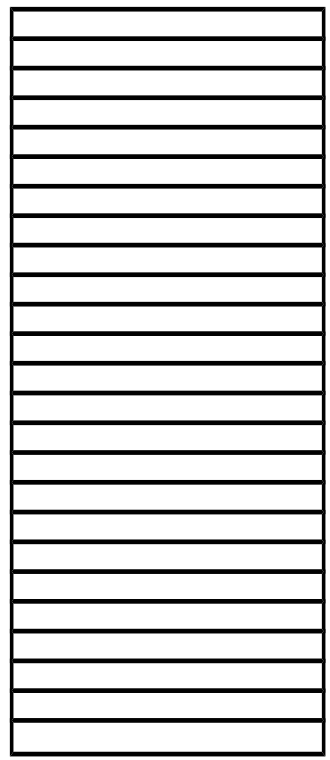

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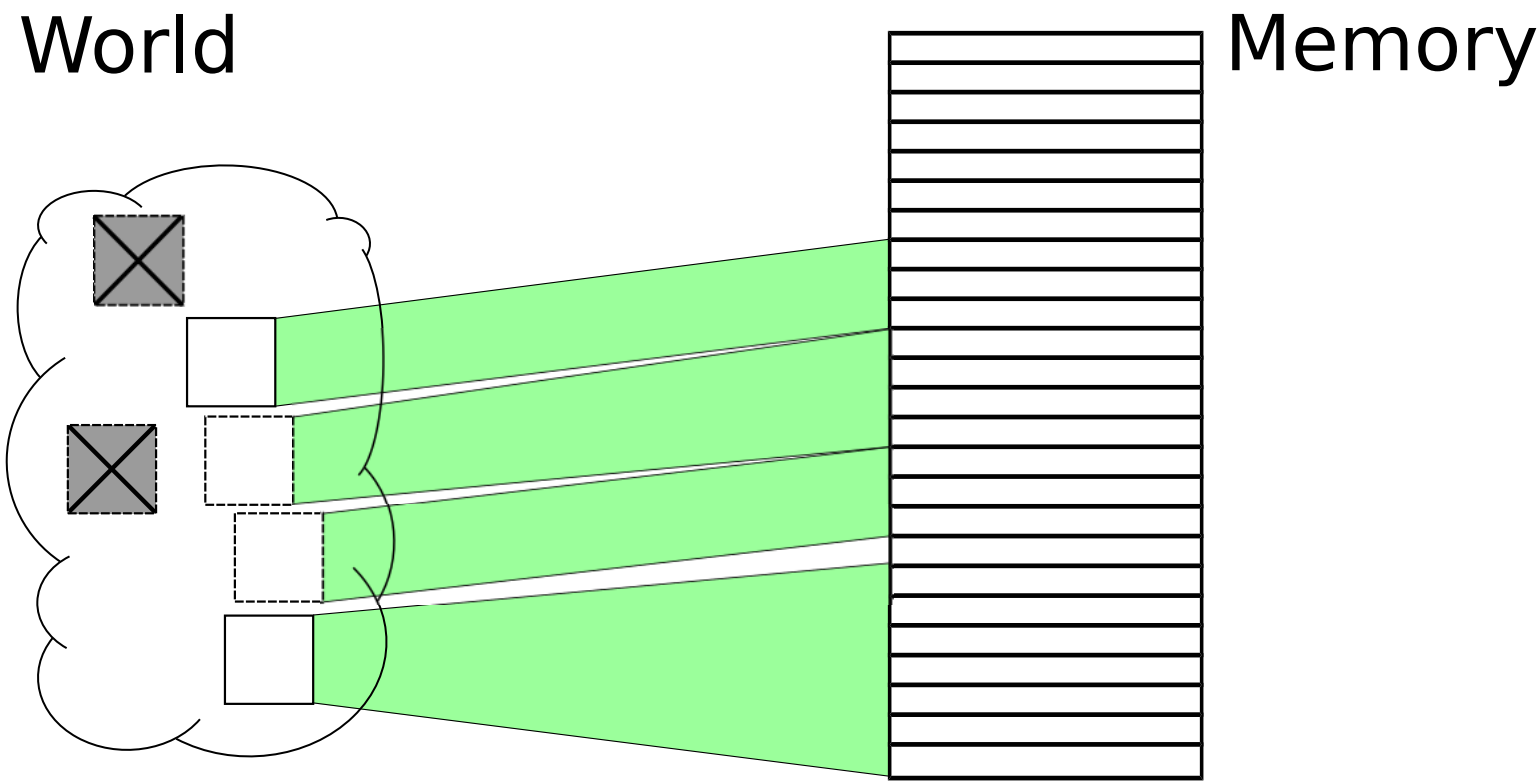

Worlds

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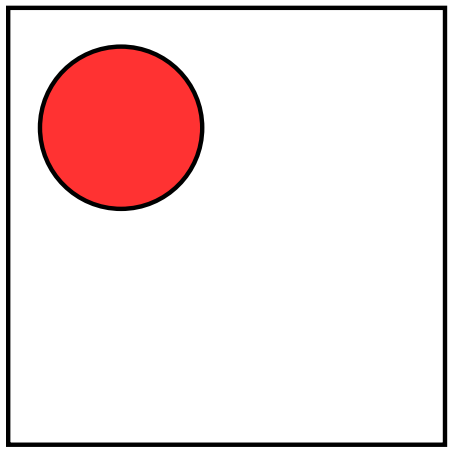
Regions

Region



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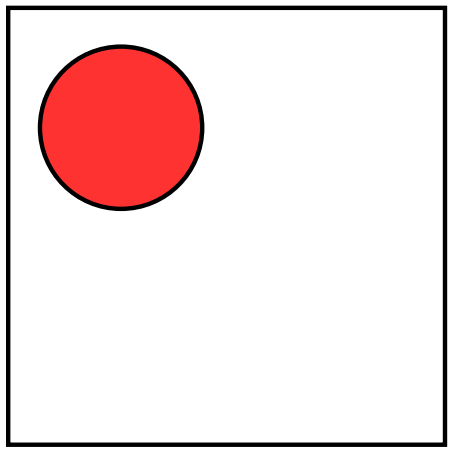

Memory cell

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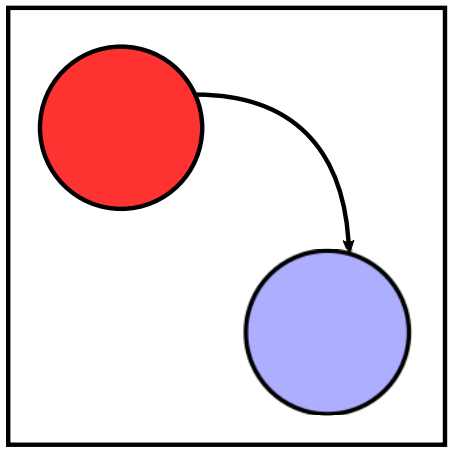

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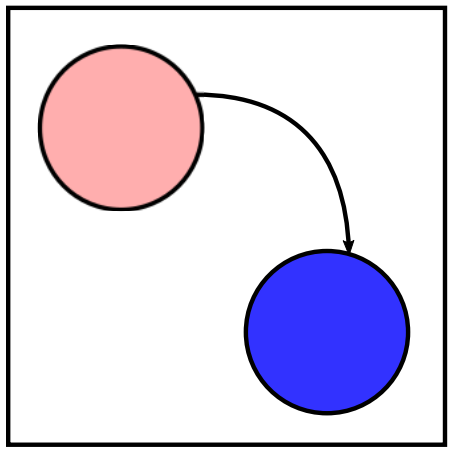

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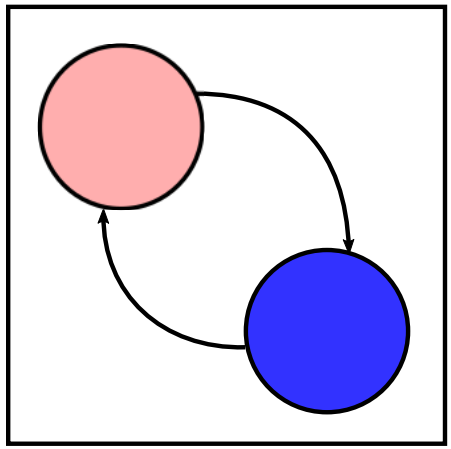

Memory cell

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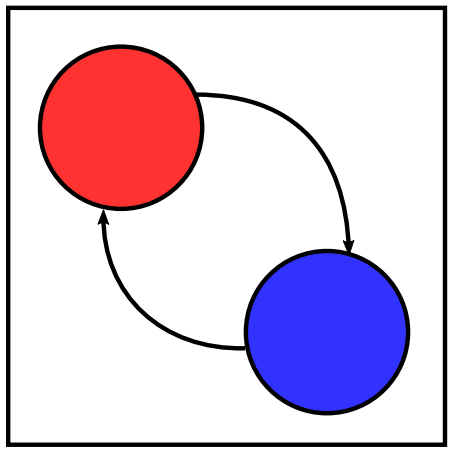

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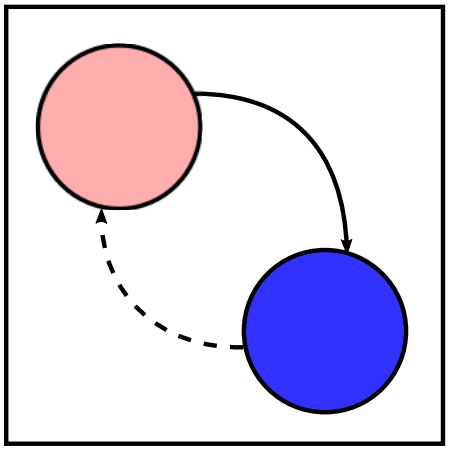

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Logical Relation

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Observation relation

- Executable configurations that produce desired results.

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- Register-files with "well-behaved" words.
- On jump, the contents of the register-file can be seen as the arguments.

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- On jump, the contents of the register-file can be seen as the arguments.

$$\mathcal{R} : \mathrm{World} \xrightarrow[\sqsupseteq^{pub}]{mon} \mathrm{Pred}(\mathrm{Reg})$$

$$\mathcal{R}(W) \stackrel{def}{=} \{reg \mid \forall r \in \mathrm{RegisterName} \setminus \{\mathrm{pc}\}. \\ reg(r) \in \mathcal{V}(W)\}$$

Expression relation

- Words that produce admissable results when "executed".

$$\mathcal{E} : \mathrm{World} \to \mathrm{Pred}(\mathrm{Word})$$

$$\mathcal{E}(W) \stackrel{def}{=}$$

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$$\forall ms : W.$$

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$$\mathcal{E}(W) \stackrel{def}{=} \{c \mid \forall reg \in \mathcal{R}(W).\ \forall ms : W.\ (reg[\mathrm{pc} \mapsto pc], ms) \in \mathcal{O}(W)\}$$

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$\mathcal{V}$-relation

- All integers (data) are in the $\mathcal{V}$-relation

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- Global capabilities
  - Must respect $\sqsupseteq^{priv}$
  - Authority only over memory segments governed by permanent region.
- Local capabilities
  - Must respect $\sqsupseteq^{pub}$
  - Authority over memory segments governed by either permanent or temporary regions

Read condition

$$
\begin{aligned}
&\mathit{readCondition}(g, W, \mathit{base}, \mathit{end}) = \\
&\quad \{(\mathit{base}, \mathit{end}) \mid \exists r \in \mathit{localityReg}(g, W). \\
&\qquad\qquad \exists [\mathit{base}', \mathit{end}'] \supseteq [\mathit{base}, \mathit{end}]. \\
&\qquad\qquad\quad W(r) \subset \iota^{\mathit{pwl}}_{\mathit{base}', \mathit{end}'}\}
\end{aligned}
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$$
H^{\mathit{pwl}} : \mathrm{Addr}^2 \to \mathrm{State} \to (\mathrm{Wor}_{\sqsupseteq^{\mathit{pub}}} \xrightarrow{\mathit{mon},\ \mathit{ne}} \mathrm{Pred}(\mathrm{MemSegment}))
$$

$$
H^{\mathit{pwl}}_{\mathit{base},\mathit{end}}\ s\ \hat{W} \stackrel{\mathit{def}}{=} \left\{ \mathit{ms} \;\middle|\; \begin{array}{l} \mathrm{dom}(\mathit{ms}) = [\mathit{base}, \mathit{end}] \wedge \\ \forall a \in [\mathit{base}, \mathit{end}].\ \mathit{ms}(a) \in \mathcal{V}(\hat{W}) \end{array} \right\}
$$

Write condition

$$
\begin{aligned}
&\mathit{writeCondition}(\iota, g, W, \mathit{base}, \mathit{end}) = \\
&\quad \{(\mathit{base}, \mathit{end}) \mid \exists r \in \mathit{localityReg}(g, W). \\
&\qquad\qquad \exists [\mathit{base}', \mathit{end}'] \supseteq [\mathit{base}, \mathit{end}]. \\
&\qquad\qquad\quad W(r) \supset \iota_{\mathit{base}', \mathit{end}'} \}
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Conditions on execution

$$
\begin{aligned}
&\mathit{executeCondition}(g, W, \mathit{perm}, \mathit{base}, \mathit{end}) = \\
&\quad \{(\mathit{perm}, \mathit{base}, \mathit{end}) \mid \forall W' \sqsupseteq W. \\
&\qquad\qquad \forall a \in [\mathit{base}, \mathit{end}]. \\
&\qquad\qquad\quad ((\mathit{perm}, g), \mathit{base}, \mathit{end}, a) \in \mathcal{E}(W')\}
\end{aligned}
$$

Conditions on execution

$$executeCondition(g, W, perm, base, end) =$$
$$\{(perm, base, end) \mid \forall W' \sqsupseteq W.$$
$$\forall a \in [base, end].$$
$$((perm, g), base, end, a) \in \mathcal{E}(W')\}$$

where $g = \mathrm{local} \Rightarrow \sqsupseteq = \sqsupseteq^{pub}$

and $g = \mathrm{global} \Rightarrow \sqsupseteq = \sqsupseteq^{priv}$

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&\mathit{executeCondition}(g, W, \mathit{perm}, \mathit{base}, \mathit{end}) = \\
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&\qquad\qquad \forall a \in [\mathit{base}, \mathit{end}]. \\
&\qquad\qquad\quad ((\mathit{perm}, g), \mathit{base}, \mathit{end}, a) \in \mathcal{E}(W')\}
\end{aligned}$$

$$\begin{aligned}
&\mathit{enterCondition}(g, W, \mathit{base}, \mathit{end}, a) = \\
&\quad \{(\mathit{base}, \mathit{end}, a) \mid \forall W' \sqsupseteq W. \\
&\qquad\qquad ((\mathrm{rx}, g), \mathit{base}, \mathit{end}, a) \in \mathcal{E}(W')\}
\end{aligned}$$

where $g = \mathrm{local} \Rightarrow \sqsupseteq = \sqsupseteq^{\mathit{pub}}$

and $g = \mathrm{global} \Rightarrow \sqsupseteq = \sqsupseteq^{\mathit{priv}}$

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Value relation

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& \{((\mathrm{o}, g), base, end, a)\} \cup \\
& \{((\mathrm{e}, g), base, end, a) \mid \\
& \quad enterCondition(g, W, base, end, a)\} \cup \\
& \{((\mathrm{rwlx}, g), base, end, a) \mid \\
& \quad readCondition(g, W, base, end) \wedge \\
& \quad writeCondition(\iota^{pwl}, g, W, base, end) \wedge \\
& \quad executeCondition(g, W, \mathrm{rwlx}, base, end)\} \cup
\end{aligned}$$

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& \quad writeCondition(\iota^{pwl}, g, W, base, end) \wedge \\
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& \quad \ldots
\end{aligned}$$

Fundamental Theorem of Logical Relations (FTLR)

Lemma (FTLR)

For all $W \in \mathrm{World}$ *and* $c \in \mathit{Caps}$,

$$c \in \mathcal{E}(W).$$

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- The pc-register can be accessed like any other register

Fundamental Theorem of Logical Relations (FTLR)

Lemma (FTLR)

For all $W \in \mathrm{World}$ *and* $c \in \mathit{Caps}$,

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- The pc-register can be accessed like any other register
- Capability must behave when used for read/write

Fundamental Theorem of Logical Relations (FTLR)

Lemma (FTLR)

For all $W \in \mathrm{World}$, $g \in \mathrm{Global}$, *perm* $\in \mathrm{Perm}$, *and* *base*, *end*, $a \in \mathrm{Addr}$,
if

$$\mathit{perm} = \mathrm{rx} \text{ and } \mathit{readCondition}(g, W, \mathit{base}, \mathit{end}),$$

or

$$\mathit{perm} = \mathrm{rwx} \text{ and } \mathit{readCondition}(W, \mathit{base}, \mathit{end})$$
$$\text{and } \mathit{writeCondition}(\iota^{\mathit{nwl}}, g, W, \mathit{base}, \mathit{end})$$

or

$$\ldots$$

then

$$(\mathit{perm}, \mathit{base}, \mathit{end}, a) \in \mathcal{E}(W).$$

The awkward example

- Using the logical relation, we can prove well-bracketedness for for the awkward example.

```
g = fun _ =>
      let x = 0 in
      fun adv =>
        x := 0;
        adv();
        x := 1;
        adv();
        assert(x == 1)
```

The awkward example

- Using the logical relation, we can prove well-bracketedness for for the awkward example.
- The proof will have to wait for another time.

```
g = fun _ =>
      let x = 0 in
      fun adv =>
        x := 0;
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        assert(x == 1)
```

Namur

Road map

Capability Machine

Formalisation

Example, Macros, and Stack Discipline

Logical Relation

Conclusion

Conclusion

- With a simple capability system and reasonable conventions, we can enforce well-bracketedness.
- Using known logical relation techniques, we can reason about programs for a simple capability machine.

Questions?

Questions?

- Chocolates in the kitchen.

References

[1] Jonathan Woodruff, Robert N.M. Watson, David Chisnall, Simon W. Moore, Jonathan Anderson, Brooks Davis, Ben Laurie, Peter G. Neumann, Robert Norton, and Michael Roe. The cheri capability model: Revisiting risc in an age of risk. In *International Symposium on Computer Architecuture*, pages 457–468, Piscataway, NJ, USA, 2014. IEEE Press.