

Tales of Belgium: Reasoning about Capability Machines using Logical Relations

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Road map

Capability Machine

Formalisation

Example, Macros, and Stack Discipline

Logical Relation

Conclusion

Leuven



Leuven

Leuven



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Why should I care about capability machines?

Current low-level protection mechanisms

- ▶ Coarse-grained compartmentalisation
- ▶ Expensive context switches
- ▶ Well suited for high-level applications
- ▶ Does not scale well
- ▶ E.g., virtual memory

Why should I care about capability machines?

Capability machines

- ▶ Fine-grained compartmentalisation
- ▶ Cheap compartments
- ▶ Fine-grained sharing
- ▶ Well suited for applications with need for many compartments

Capabilities

What is a capability?

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What is a capability in a capability machine?

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What is a capability in a capability machine?

- ▶ Unforgeable pointer

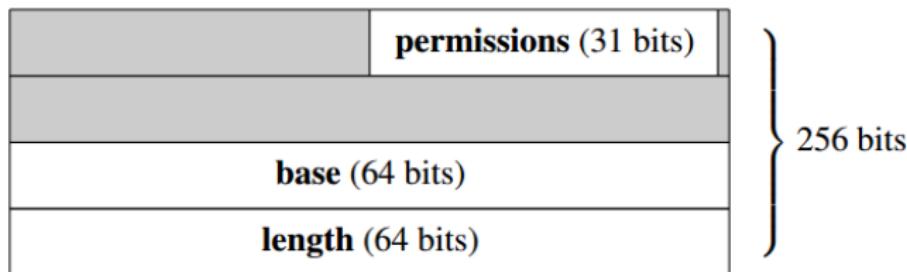


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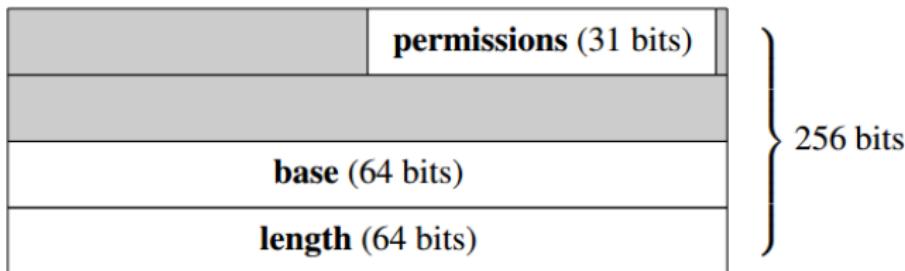


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- ▶ Permission

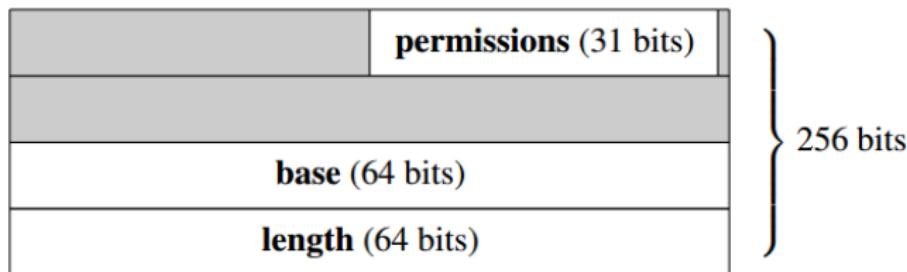


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Capability permissions

- ▶ Read
- ▶ Write
- ▶ Execute

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 - ▶ Modularisation

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 - ▶ No instruction generates new capability
 - ▶ Manipulation of capabilities cannot result in authority amplification

Capability machine overview

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 - ▶ Permissions

Capability machine overview

- ▶ Capabilities
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Capability machine overview

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 - ▶ Permissions
 - ▶ Range of authority
- ▶ Capability aware instructions
- ▶ Memory and registers
 - ▶ Can contain data and capabilities
 - ▶ Capabilities tagged

Simple capability machine limitations

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- ▶ Issues:
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 - ▶ Does not scale to other types of permissions

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- ▶ Gives simple temporal revocation, but
 - ▶ requires no global pwl-capabilities
 - ▶ enforcement depends on programming discipline.

Brussels



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Formalisation - Permissions

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- ▶ To simplify matters, we only allow certain combinations of permissions

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Formalisation - Permissions

Permissions

- ▶ To simplify matters, we only allow certain combinations of permissions
- ▶ No permissions, read only, read-write,

$$\text{Perm} \stackrel{\text{def}}{=} \{\text{o}, \text{ro}, \text{rw}, \}$$

Formalisation - Permissions

Permissions

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- ▶ No permissions, read only, read-write, read-execute,

$$\text{Perm} \stackrel{\text{def}}{=} \{ \text{o}, \text{ro}, \text{rw}, \quad \text{rx}, \quad \}$$

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Formalisation - Permissions

Permissions

- ▶ To simplify matters, we only allow certain combinations of permissions
- ▶ No permissions, read only, read-write, read-'write-local'
read-execute, enter, read-write-execute,
read-'write-local'-execute

$$\text{Perm} \stackrel{\text{def}}{=} \{\text{o}, \text{ro}, \text{rw}, \text{rwl}, \text{rx}, \text{e}, \text{rwx}, \text{rwlx}\}$$

Formalisation - Permissions

Permissions ordering

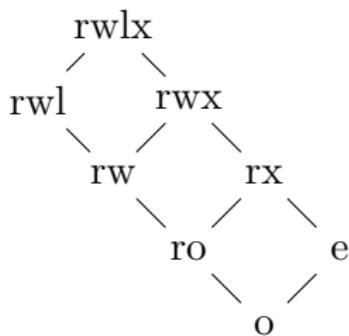


Figure: Permission hierarchy

Formalisation - Locality

Locality

Global ::= {global, local}

Locality ordering



Figure: Locality hierarchy

Formalisation - Capabilities

Capability

$\text{Cap} \stackrel{\text{\tiny def}}{=}$

Formalisation - Capabilities

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- ▶ Permission and locality

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$$\text{Cap} \stackrel{\text{\tiny def}}{=} (\text{Perm} \times \text{Global})$$

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- ▶ Range of authority

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Formalisation - Capabilities

Capability

- ▶ Permission and locality
- ▶ Range of authority
- ▶ Pointer

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Example: ((e, local), 30, 42, 30)

Formalisation - Words and register file

Words

Word $\stackrel{\text{def}}{=}$

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- ▶ Data (and instructions)

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Register file

$$\text{Reg} \stackrel{\text{def}}{=}$$

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$$\text{Reg} \stackrel{\text{def}}{=} \text{RegisterName} \rightarrow \text{Word}$$

Formalisation - Memory and configurations

Memory

$\text{Mem} \stackrel{\text{def}}{=}$

Formalisation - Memory and configurations

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- ▶ Map from Addr to Word

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$$\text{Conf} \stackrel{\text{def}}{=} \text{Reg} \times \text{Mem}$$

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Configuration

- ▶ Executable configuration
- ▶ Successfully halted configuration

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- ▶ The normal instructions
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```
rv ::= n | r
Instructions ::= jmp r | jnz r rv | move r rv |
                load r r | store r r | plus r rv rv |
                lea r rv | restrict r r rv |
                subseg r rv rv |
                getp r r | getl r r | getb r r |
                gete r r | geta r r
```

Formalisation - Instructions

Syntax

- ▶ The normal instructions
- ▶ The capability manipulation instructions
- ▶ Instructions to stop the machine

$rv ::= n \mid r$

Instructions $::= \text{jmp } r \mid \text{jnz } r \text{ } rv \mid \text{move } r \text{ } rv \mid$
 $\text{load } r \text{ } r \mid \text{store } r \text{ } r \mid \text{plus } r \text{ } rv \text{ } rv \mid$
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 $subseg\ r\ rv\ rv \mid$
 $getp\ r\ r \mid getl\ r\ r \mid getb\ r\ r \mid$
 $gete\ r\ r \mid geta\ r\ r \mid fail \mid halt$

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Execution relation

$$\rightarrow \subseteq (\text{Reg} \times \text{Mem}) \times \text{Conf}$$

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$$\frac{\text{executionAllowed}(\Phi) \quad i = \Phi.\text{mem}(a)}{\Phi \rightarrow \llbracket i \rrbracket(\Phi)}$$

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Formalisation - Operational Semantics (2)

$$\frac{\begin{array}{c} w = \Phi.\text{reg}(r_2) \quad \Phi.\text{reg}(r_1) = ((perm, g), base, end, a) \\ perm \in \{\text{rw}, \text{rwl}, \text{rwx}, \text{rwlx}\} \\ base \leq a \leq end \quad w = ((_, \text{local}), _, _, _) \end{array}}{\llbracket \text{store } r_1 \; r_2 \rrbracket(\Phi) = \Phi[\text{mem}.a \mapsto w]}$$

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$$\frac{w = \Phi.\text{reg}(r_2) \quad \Phi.\text{reg}(r_1) = ((perm, g), base, end, a) \\ perm \in \{\text{rw}, \text{rwl}, \text{rwx}, \text{rwlx}\} \\ base \leq a \leq end \quad w = ((_, \text{local}), _, _, _) \Rightarrow perm \in \{\text{rwl}, \text{rwlx}\}}{\llbracket \text{store } r_1 \ r_2 \rrbracket(\Phi) = \Phi[\text{mem}.a \mapsto w]}$$

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$$w = \Phi.\text{reg}(r_2) \quad \Phi.\text{reg}(r_1) = ((\text{perm}, g), \text{base}, \text{end}, a) \\ \text{perm} \in \{\text{rw}, \text{rwl}, \text{rwx}, \text{rwlx}\}$$

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$$\frac{\Phi.\text{reg}(\text{pc}) = ((\text{perm}, g), \text{base}, \text{end}, a) \quad \text{newPc} = (\text{perm}, \text{base}, \text{end}, a + 1)}{\text{updatePc}(\Phi) = \Phi[\text{reg.pc} \mapsto \text{newPc}]}$$

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- ▶ Need a *failed* case for each of the rules
- ▶ The operational semantics of the remaining instructions is defined in a similar fashion

Antwerp



Road map

Capability Machine

Formalisation

Example, Macros, and Stack Discipline

Logical Relation

Conclusion

The “awkward” example

```
g = fun _ =>
  let x = 0 in
  fun adv =>
    x := 0;
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    x := 1;
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    assert(x == 1)
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- ▶ Show for any reasonable `adv` that the assertion never fails for `adv(g)`.
- ▶ Need to define some macros to make a readable translation.

Macros

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- ▶ `malloc $r n$`
 - ▶ allocates a *fresh* piece of memory of size n
 - ▶ leaves a global capability with rwx permission in register r

The “awkward” example (naive translation)

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g = fun _ =>
  let x = 0 in
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<pre>g = fun _ => let x = 0 in fun adv => x := 0; adv(); x := 1; adv(); assert(x == 1)</pre>	<hr/>	<pre>f : store x 0 jmp r1 store x 1 jmp r1 load r1 x assert r1 1 jmp r0</pre>
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Stack and stack capability

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- ▶ Only place one can store local capabilities
- ▶ When a stack is available, we assume it is in register r_{stk}

Macros (1)

`scall $r(\bar{r}_{args}, \bar{r}_{priv})$`

- ▶ \bar{r}_{args} list of argument registers
- ▶ \bar{r}_{priv} list of “private” registers
- ▶ r register to jump to

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 - ▶ stack capability
 - ▶ Create protected return pointer
 - ▶ Restrict stack capability to unused part
 - ▶ Clear the part of the stack we release control over
 - ▶ Clear unused registers
 - ▶ Jump to r
 - ▶ Upon return: Run the on stack restoration code
 - ▶ Return address in caller-code: Restore “private” state

The “awkward” example (naive translation)

```
g = fun _ =>
    let x = 0 in
    fun adv =>
        x := 0;
        adv();
        x := 1;
        adv();
        assert(x == 1)
```

```
f : store x 0
                jmp r1
                store x 1
```

```
g : malloc r2 1
    store r2 0
    move pc r3
    lea r3 ...
    crtcls [(x, r2)] r3
    jmp r0
```

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      store r2 0
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```

```
f :   store x 0
      scall r1([], [r0, r1])
      store x 1
      scall r1([], [r0])
      load r1 x
      assert r1 1
      jmp r0
```

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g :   malloc r2 1
      store r2 0
      move pc r3
      lea r3 ...
      crtcls [(x, r2)] r3
      jmp r0 !
```

```
f :   store x 0
      scall r1([], [r0, r1])
      store x 1
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      load r1 x
      assert r1 1
      jmp r0 !
```

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 - ▶ Clear all the registers in *r̄*.

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load r1 x
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```

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      crtcls [(x, r2)] r3
      rclear RN \ {pc, r0, r1}
      jmp r0
```

```
f :  store x 0
      scall r1([], [r0, r1])
      store x 1
      scall r1([], [r0])
      load r1 x
      assert r1 1
      rclear RN \ {r0, pc}
      jmp r0
```

The “awkward” example (naive translation)

```
g = fun _ =>
  let x = 0 in
  fun adv =>
    x := 0;
    adv();
    x := 1;
    adv();
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g :  malloc r2 1
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The “awkward” example (final version)

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      store x 1
      scall r1([], [r0])
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 - ▶ If it looks like a stack, works like a stack, and quacks like a stack, then it is probably a stack.
- ▶ In the presence of an untrusted stack capability, only use global callbacks.

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Bruges



Road map

Capability Machine

Formalisation

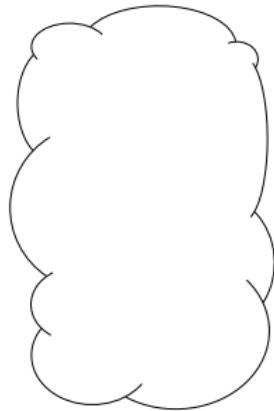
Example, Macros, and Stack Discipline

Logical Relation

Conclusion

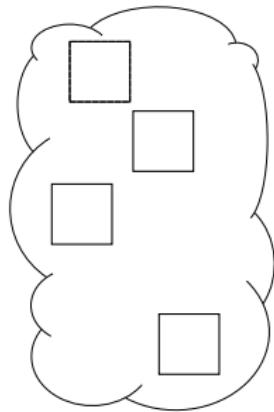
Worlds

World



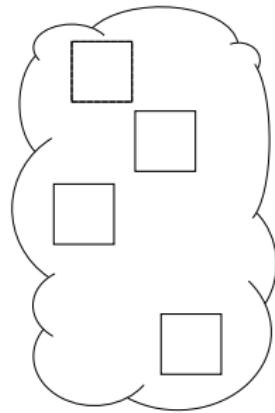
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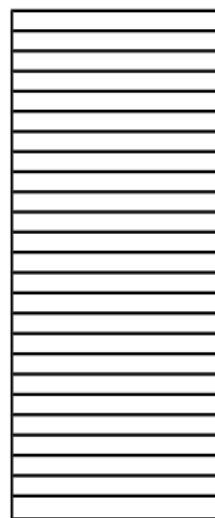


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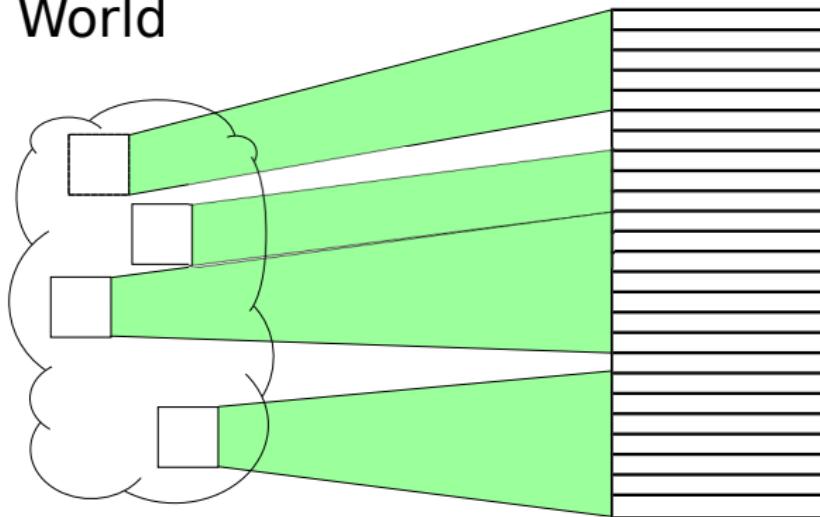
Memory



Worlds

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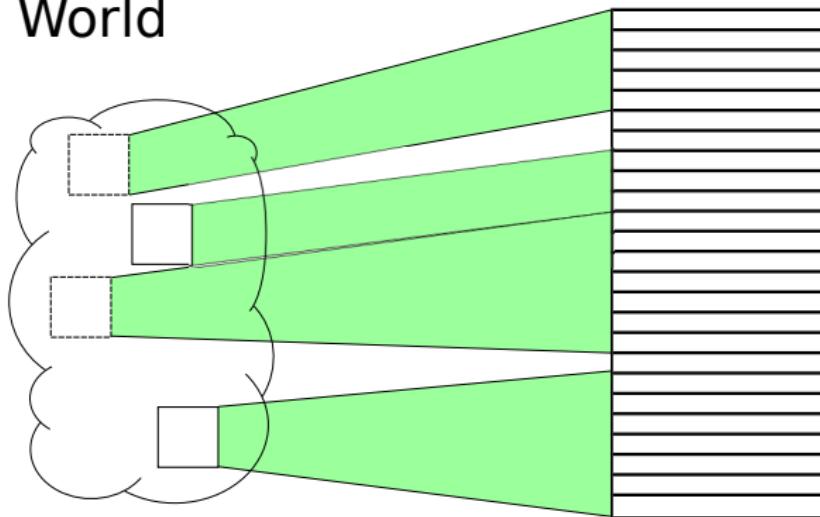
Memory



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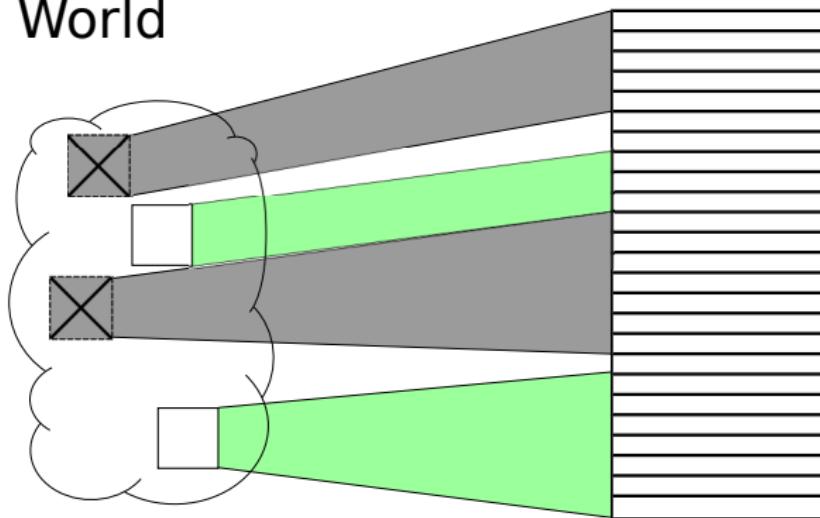
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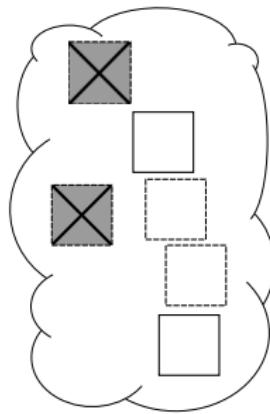
World

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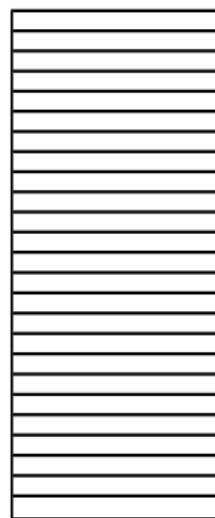


Worlds

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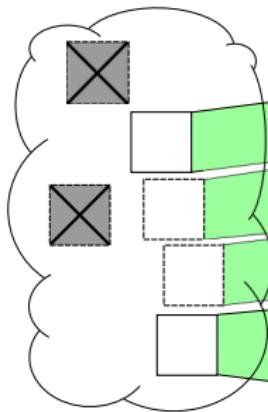


Memory



Worlds

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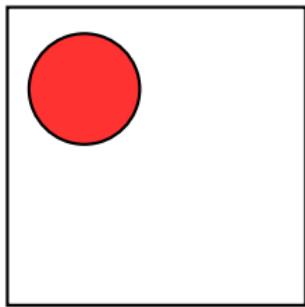
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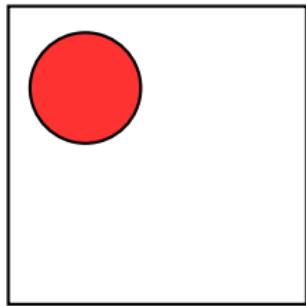
Regions

Region



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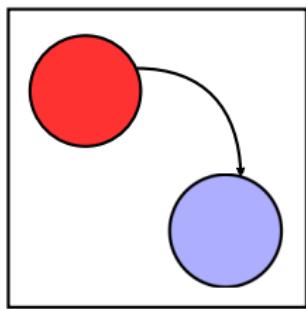


Memory cell



Regions

Region

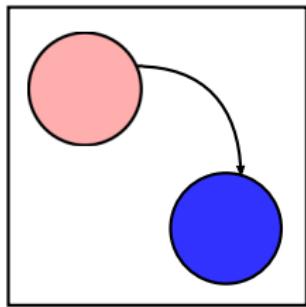


Memory cell



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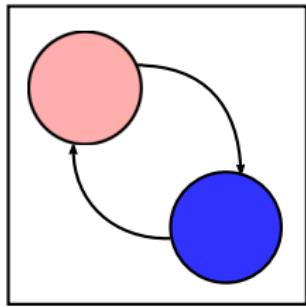


Memory cell



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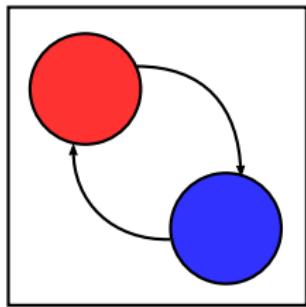


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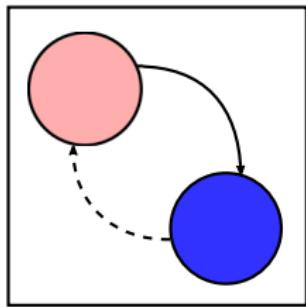


Memory cell



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Logical Relation

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- ▶ Executable configurations that produce desired results.

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Register-file relation

- ▶ Register-files with “well-behaved” words.
- ▶ On jump, the contents of the register-file can be seen as the arguments.

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 - ▶ Authority over memory segments governed by either permanent or temporary regions

Read condition

$$\begin{aligned} \text{readCondition}(g, W, \text{base}, \text{end}) = \\ \{(base, end) \mid \exists r \in \text{localityReg}(g, W). \\ \quad \exists [base', end'] \supseteq [base, end]. \\ \quad W(r) \subset \iota_{base', end'}^{\text{pwl}}\} \end{aligned}$$

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$$H^{\text{pwl}} : \text{Addr}^2 \rightarrow \text{State} \rightarrow (\text{Wor}_{\sqsubseteq^{\text{pub}}} \xrightarrow{\text{mon, ne}} \text{Pred}(\text{MemSegment}))$$

$$H_{base, end}^{\text{pwl}} \circ \hat{W} \stackrel{\text{def}}{=} \left\{ ms \middle| \begin{array}{l} \text{dom}(ms) = [base, end] \wedge \\ \forall a \in [base, end]. ms(a) \in \mathcal{V}(\hat{W}) \end{array} \right\}$$

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$$\iota_{base, end}^{nwl} \stackrel{\text{def}}{=} (\text{temp}, 1, =, =, H_{start, end}^{nwl})$$

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$$H^{nwl} : \text{Addr}^2 \rightarrow \text{State} \rightarrow (\text{Wor}_{\sqsupseteq^{\text{priv}}} \xrightarrow{\text{mon, ne}} \text{Pred}(\text{MemSegment}))$$

$$H_{base, end}^{nwl} \ s \ \hat{W} \stackrel{\text{def}}{=} \left\{ ms \middle| \begin{array}{l} \text{dom}(ms) = [base, end] \wedge \\ \forall a \in [base, end]. \\ ms(a) \in \mathcal{V}(\text{revokeTemp}(\hat{W})) \end{array} \right\}$$

Conditions on execution

$$\begin{aligned} \text{executeCondition}(g, W, perm, base, end) = \\ \{(perm, base, end) \mid & \forall W' \sqsupseteq W. \\ & \forall a \in [base, end]. \\ & ((perm, g), base, end, a) \in \mathcal{E}(W')\} \end{aligned}$$

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where $g = \text{local} \Rightarrow \sqsupseteq = \sqsupseteq^{\text{pub}}$

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Value relation

$$\mathcal{V} : \text{World} \xrightarrow[\sqsupseteq^{\textit{pub}}]{\textit{mon}} \text{Pred}(\text{Word})$$

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Fundamental Theorem of Logical Relations (FTLR)

Lemma (FTLR)

For all $W \in \text{World}$ and $c \in \text{Caps}$,

$$c \in \mathcal{E}(W).$$

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Lemma (FTLR)

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- ▶ The pc-register can be accessed like any other register
- ▶ Capability must behave when used for read/write

Fundamental Theorem of Logical Relations (FTLR)

Lemma (FTLR)

For all $W \in \text{World}$, $g \in \text{Global}$, $\text{perm} \in \text{Perm}$, and
 $\text{base}, \text{end}, a \in \text{Addr}$,

if

$\text{perm} = \text{rx}$ and $\text{readCondition}(g, W, \text{base}, \text{end})$,

or

$\text{perm} = \text{rwx}$ and $\text{readCondition}(W, \text{base}, \text{end})$

and $\text{writeCondition}(\iota^{nwl}, g, W, \text{base}, \text{end})$

or

...

then

$(\text{perm}, \text{base}, \text{end}, a) \in \mathcal{E}(W)$.

The awkward example

- ▶ Using the logical relation, we can prove well-bracketedness for the awkward example.

```
g = fun _ =>
  let x = 0 in
  fun adv =>
    x := 0;
    adv();
    x := 1;
    adv();
    assert(x == 1)
```

The awkward example

- ▶ Using the logical relation, we can prove well-bracketedness for the awkward example.
- ▶ The proof will have to wait for another time.

```
g = fun _ =>
  let x = 0 in
  fun adv =>
    x := 0;
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    assert(x == 1)
```

Namur



Road map

Capability Machine

Formalisation

Example, Macros, and Stack Discipline

Logical Relation

Conclusion

Conclusion

- ▶ With a simple capability system and reasonable conventions, we can enforce well-bracketedness.
- ▶ Using known logical relation techniques, we can reason about programs for a simple capability machine.

Questions?

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- ▶ Chocolates in the kitchen.

References

- [1] Jonathan Woodruff, Robert N.M. Watson, David Chisnall, Simon W. Moore, Jonathan Anderson, Brooks Davis, Ben Laurie, Peter G. Neumann, Robert Norton, and Michael Roe. The cheri capability model: Revisiting risc in an age of risk. In *International Symposium on Computer Architecture*, pages 457–468, Piscataway, NJ, USA, 2014. IEEE Press.