

# Systemnahe Informatik

## Übungsgruppe Xeon Phi

Dominik Walter

Sommersemester 2018

## Intel Skylake

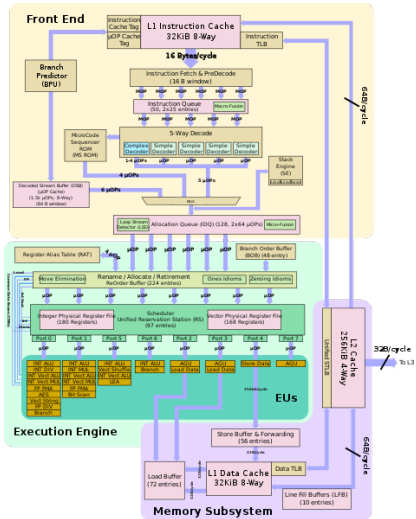
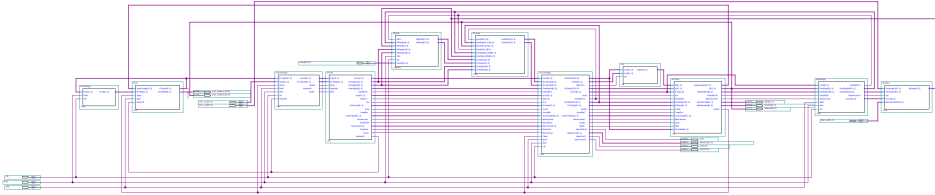


Figure: [https://en.wikichip.org/wiki/File:skylake\\_block\\_diagram.svg](https://en.wikichip.org/wiki/File:skylake_block_diagram.svg)

# RISCV Pipeline



# RISCV Pipeline



# Instruction Fetch



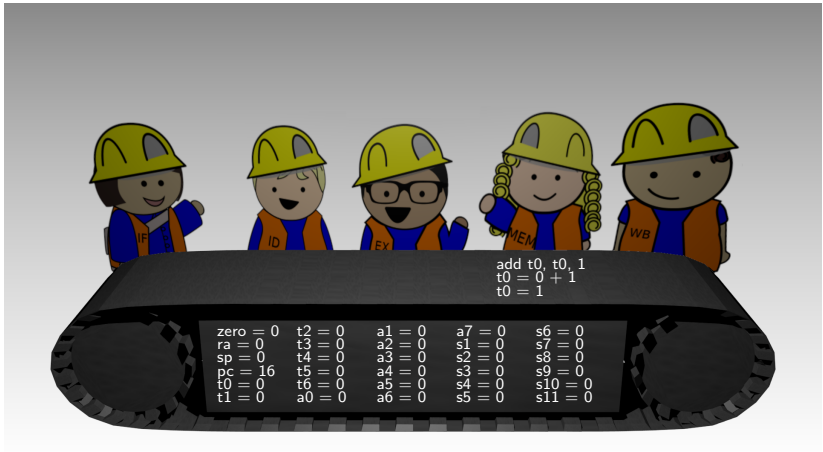
# Instruction Decode



# Execute

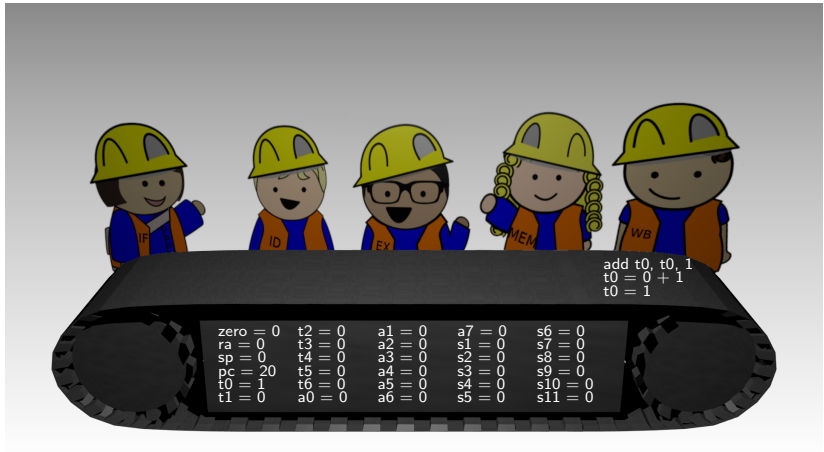


# Memory





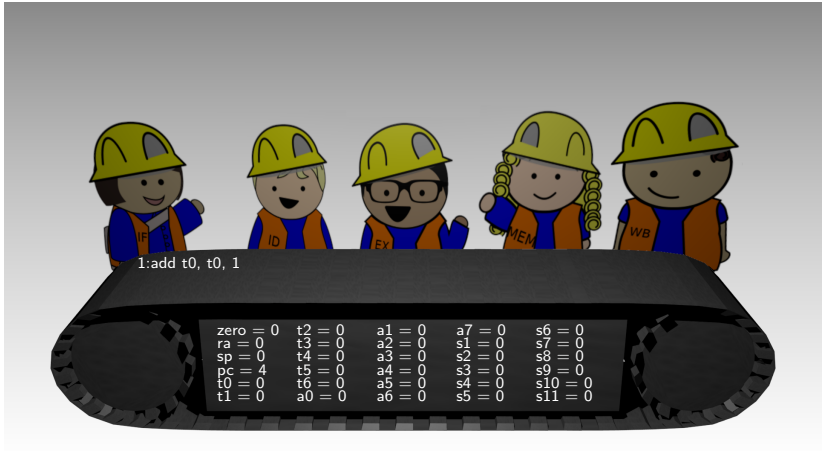
# Writeback



# Pipeline Konflikt: Takt 0



# Pipeline Konflikt: Takt 1



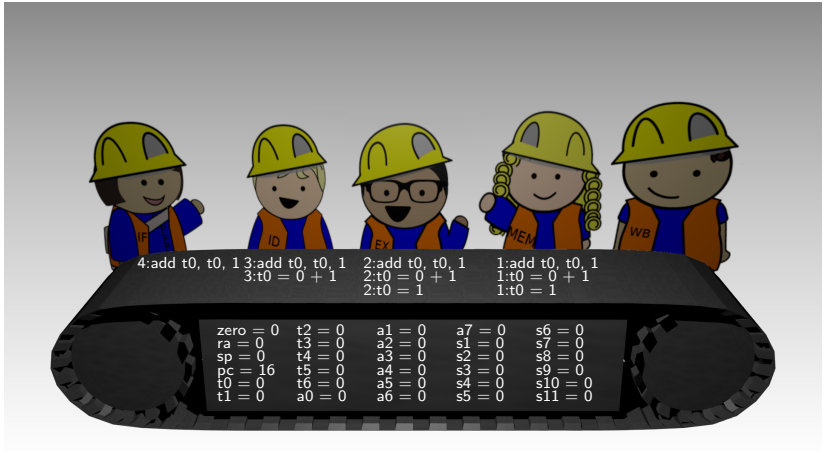
## Pipeline Konflikt: Takt 2



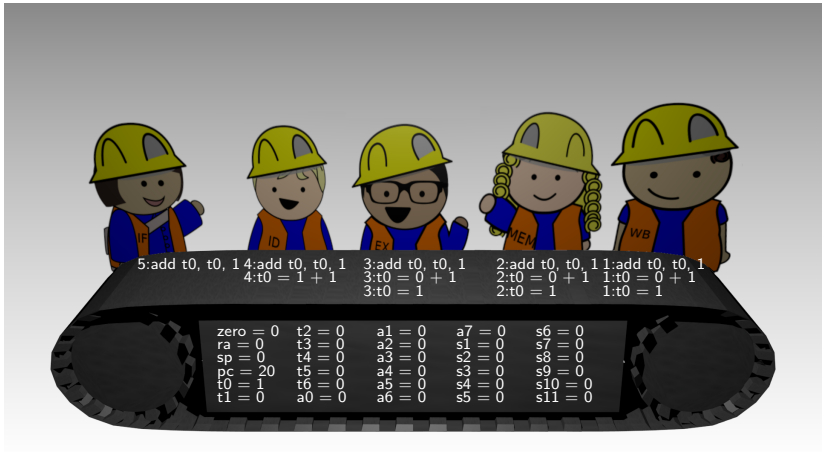
# Pipeline Konflikt: Takt 3



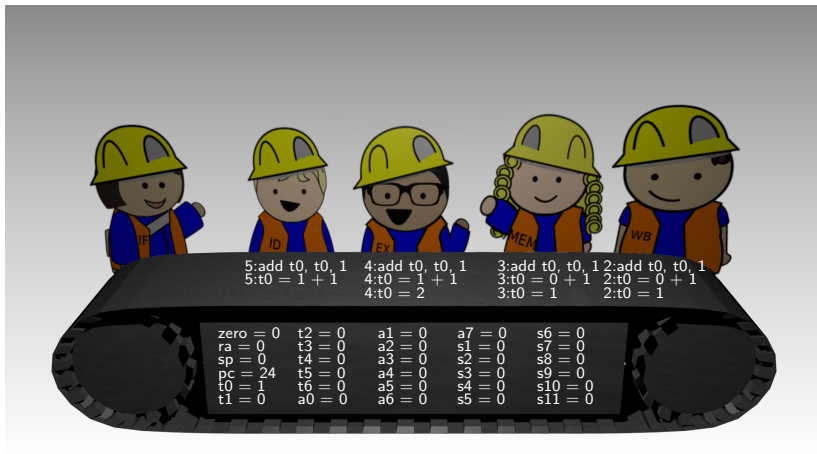
# Pipeline Konflikt: Takt 4



# Pipeline Konflikt: Takt 5

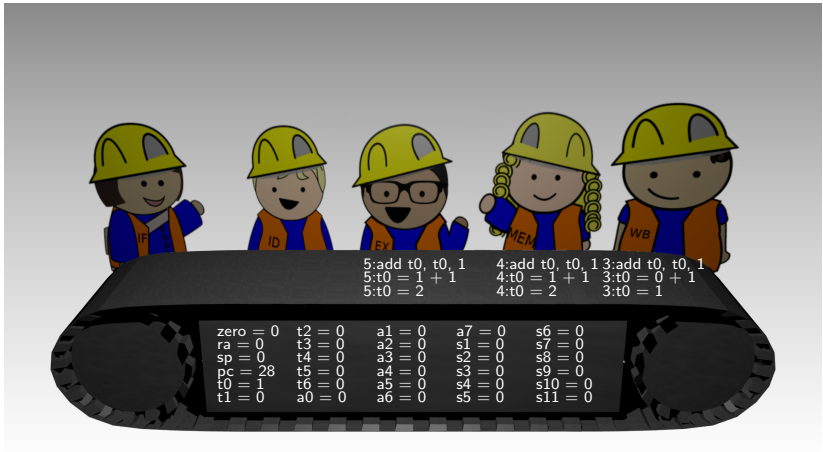


# Pipeline Konflikt: Takt 6

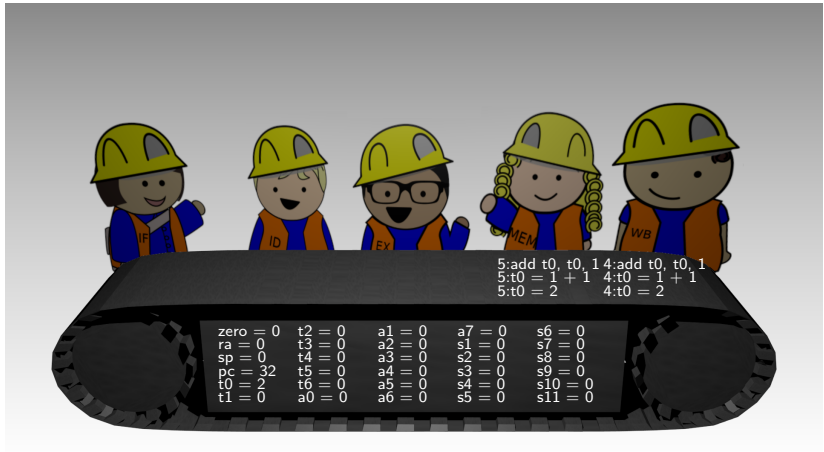




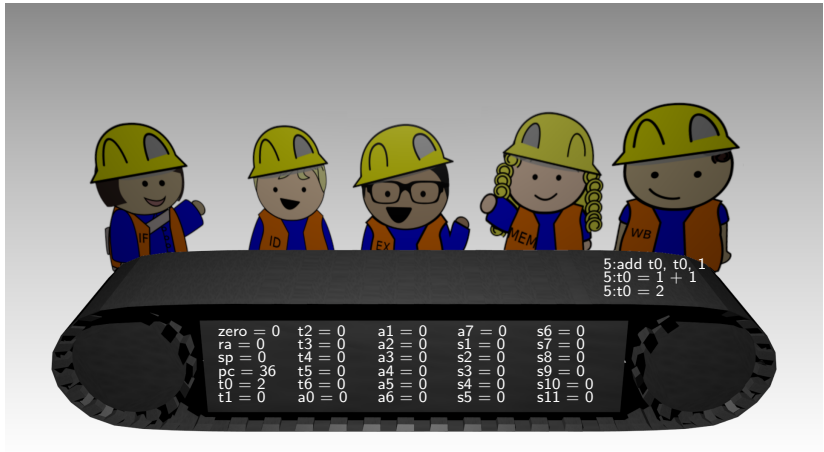
# Pipeline Konflikt: Takt 7



# Pipeline Konflikt: Takt 8



# Pipeline Konflikt: Takt 9



# Pipeline Konflikt: Takt 10



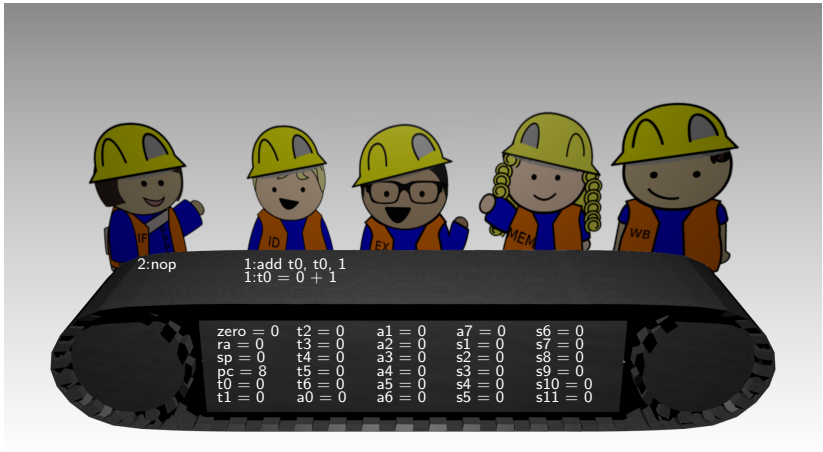
# Pipeline Konfliktlösung: Takt 0



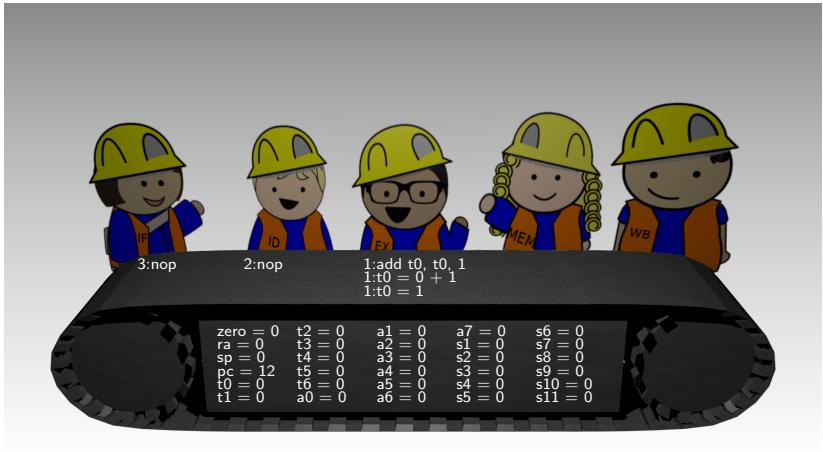
# Pipeline Konfliktlösung: Takt 1



# Pipeline Konfliktlösung: Takt 2

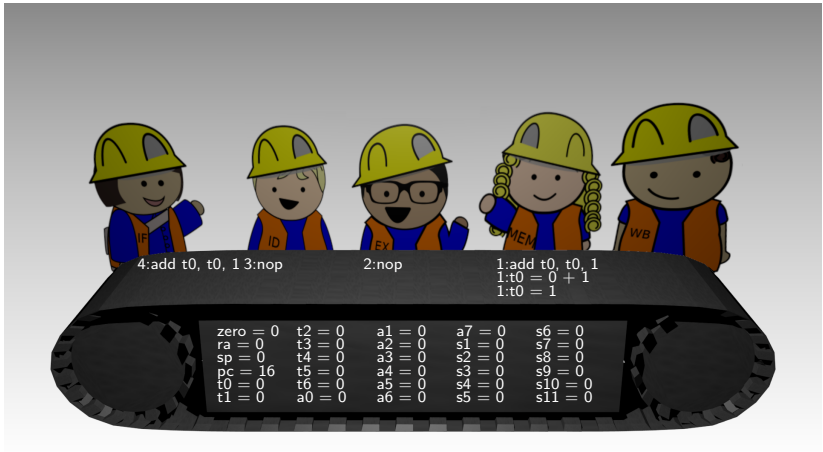


# Pipeline Konfliktlösung: Takt 3

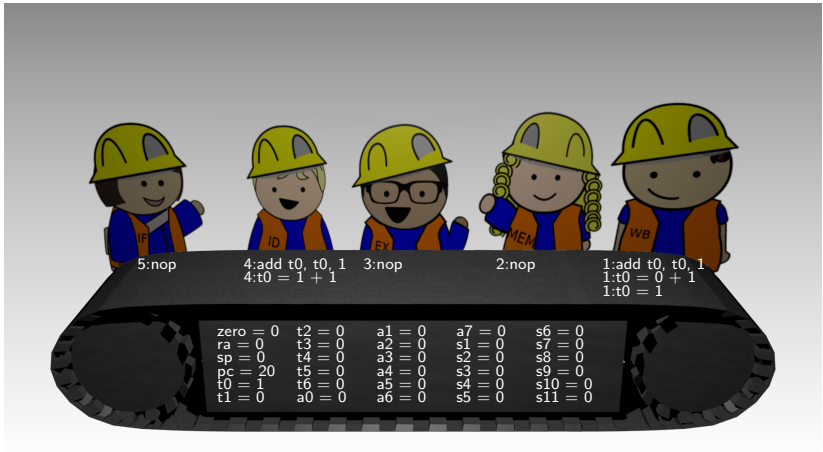




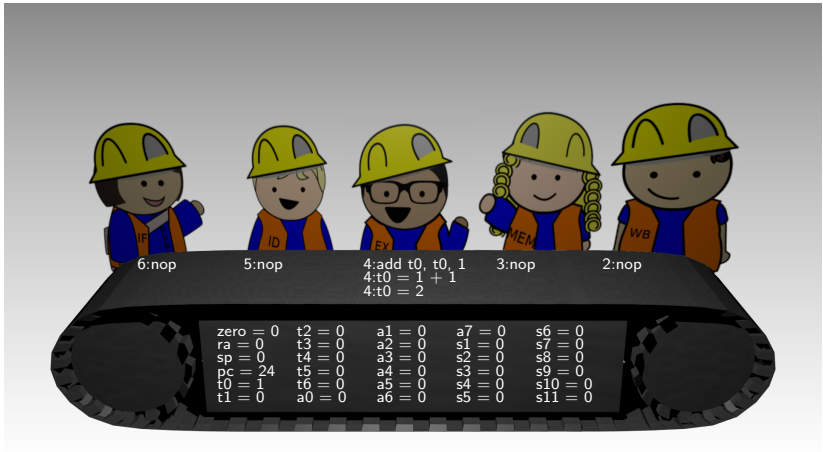
# Pipeline Konfliktlösung: Takt 4



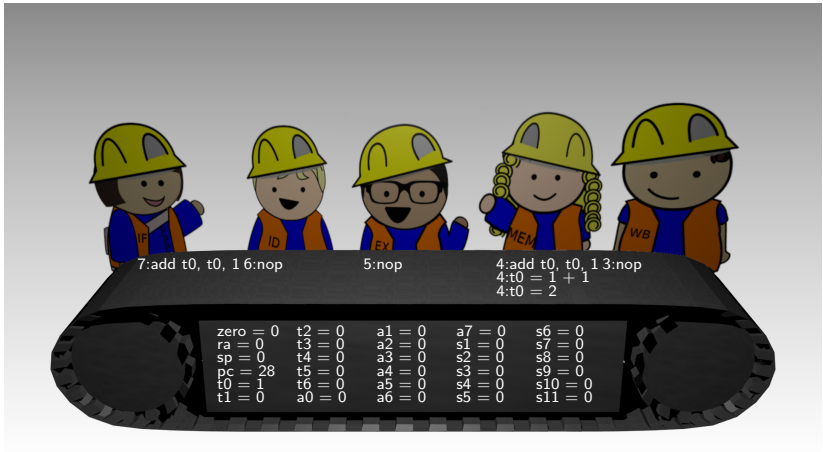
# Pipeline Konfliktlösung: Takt 5



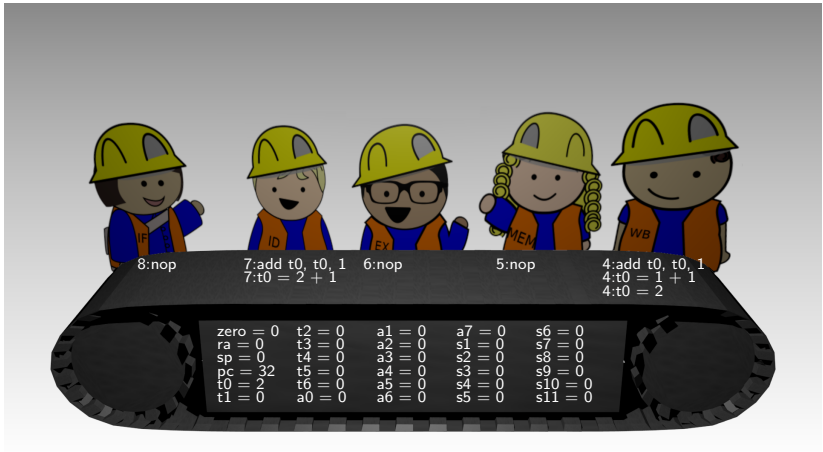
# Pipeline Konfliktlösung: Takt 6



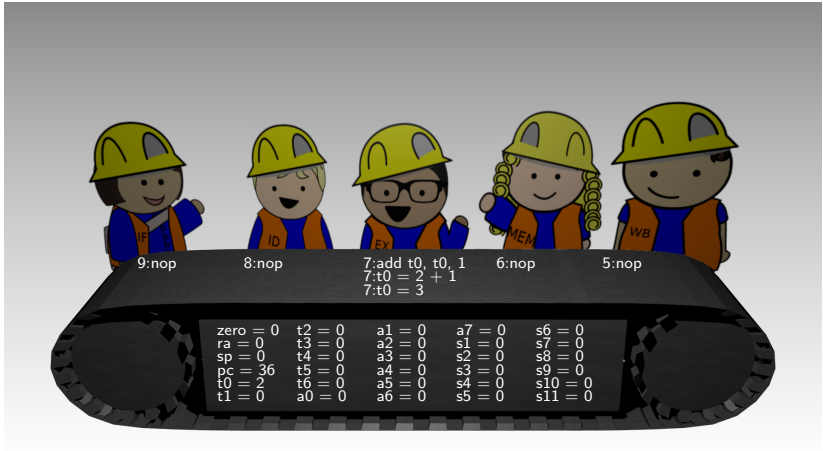
# Pipeline Konfliktlösung: Takt 7



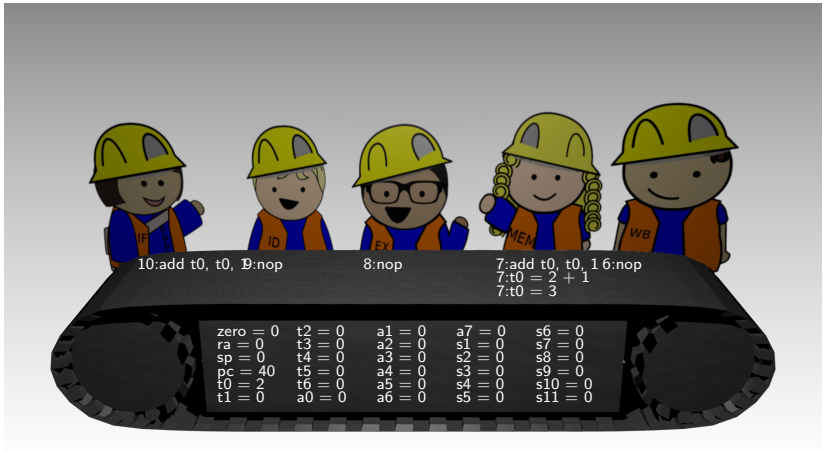
# Pipeline Konfliktlösung: Takt 8



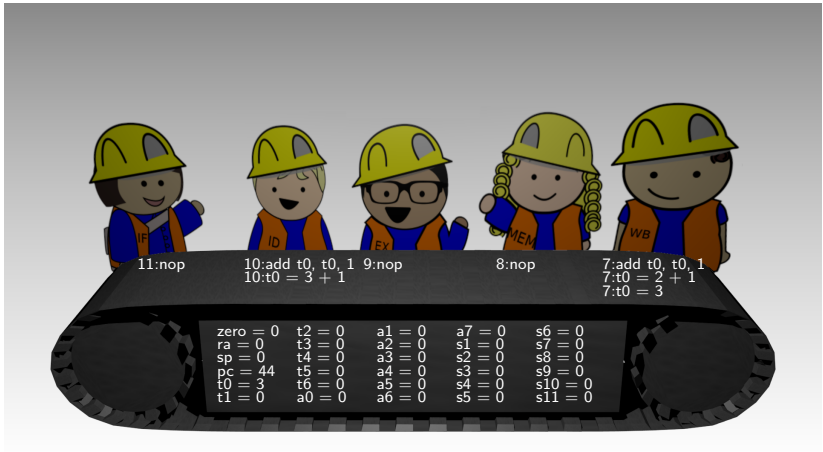
# Pipeline Konfliktlösung: Takt 9



# Pipeline Konfliktlösung: Takt 10

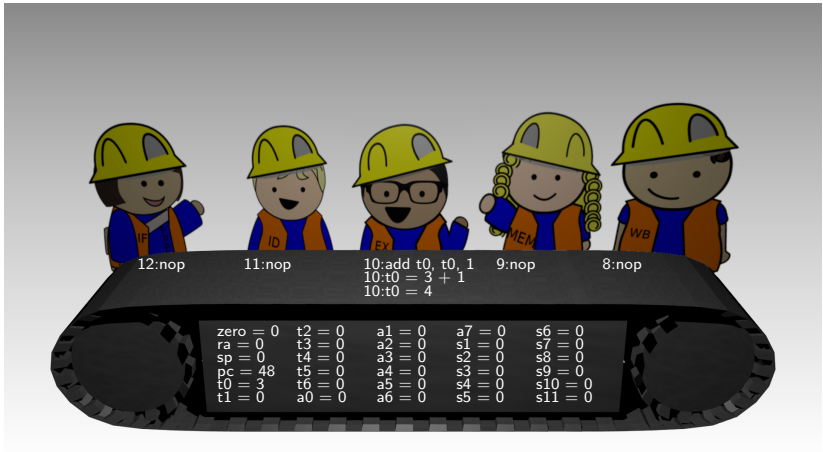


# Pipeline Konfliktlösung: Takt 11

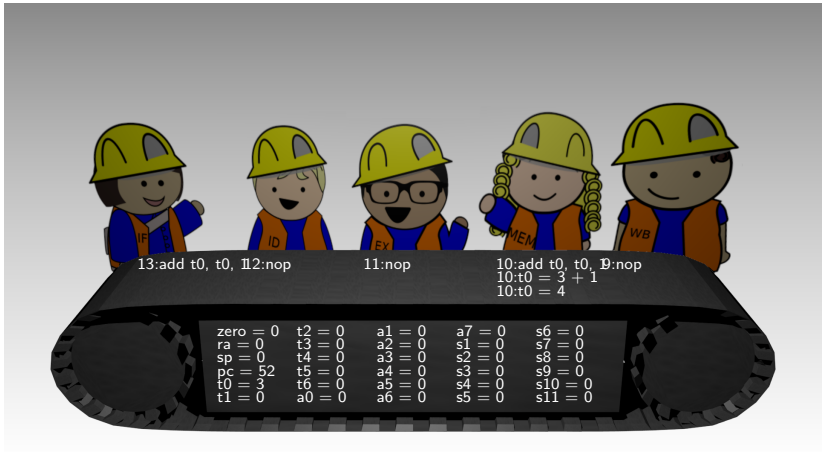




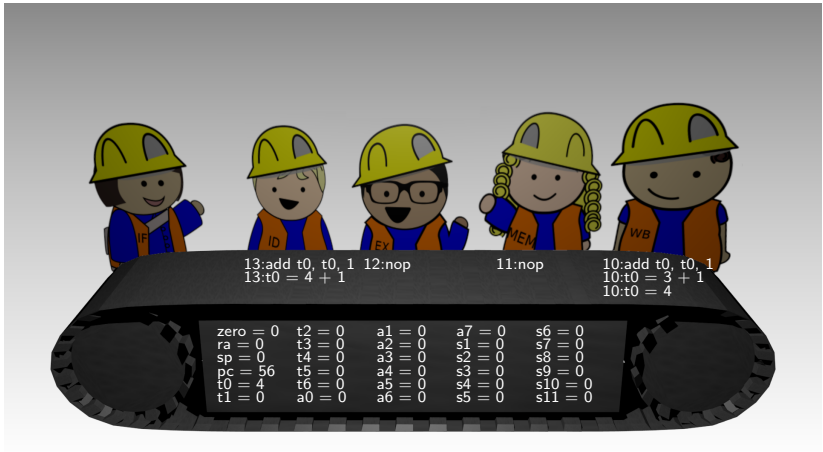
# Pipeline Konfliktlösung: Takt 12



# Pipeline Konfliktlösung: Takt 13



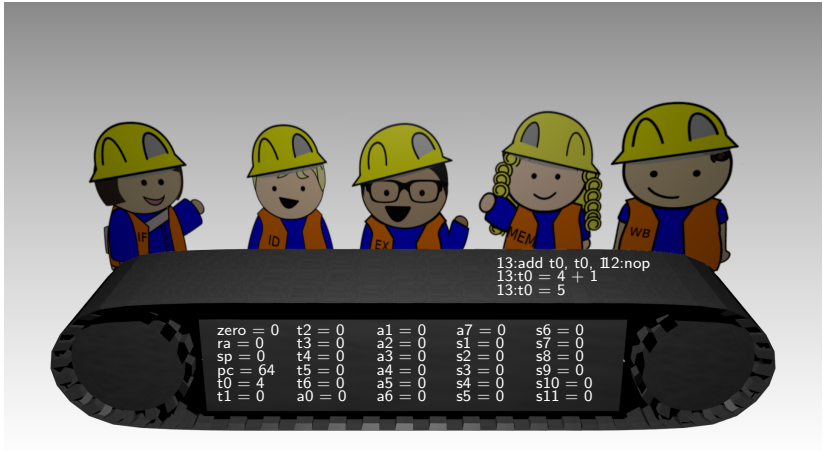
# Pipeline Konfliktlösung: Takt 14



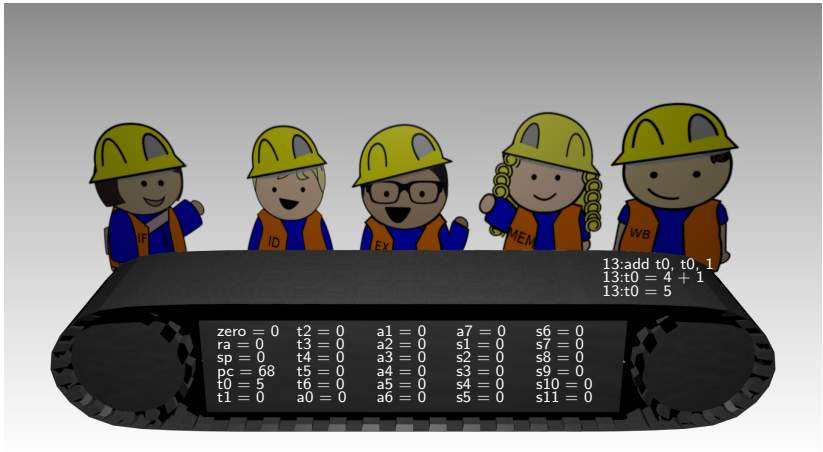
# Pipeline Konfliktlösung: Takt 15



# Pipeline Konfliktlösung: Takt 16



# Pipeline Konfliktlösung: Takt 17



# Pipeline Konfliktlösung: Takt 18

