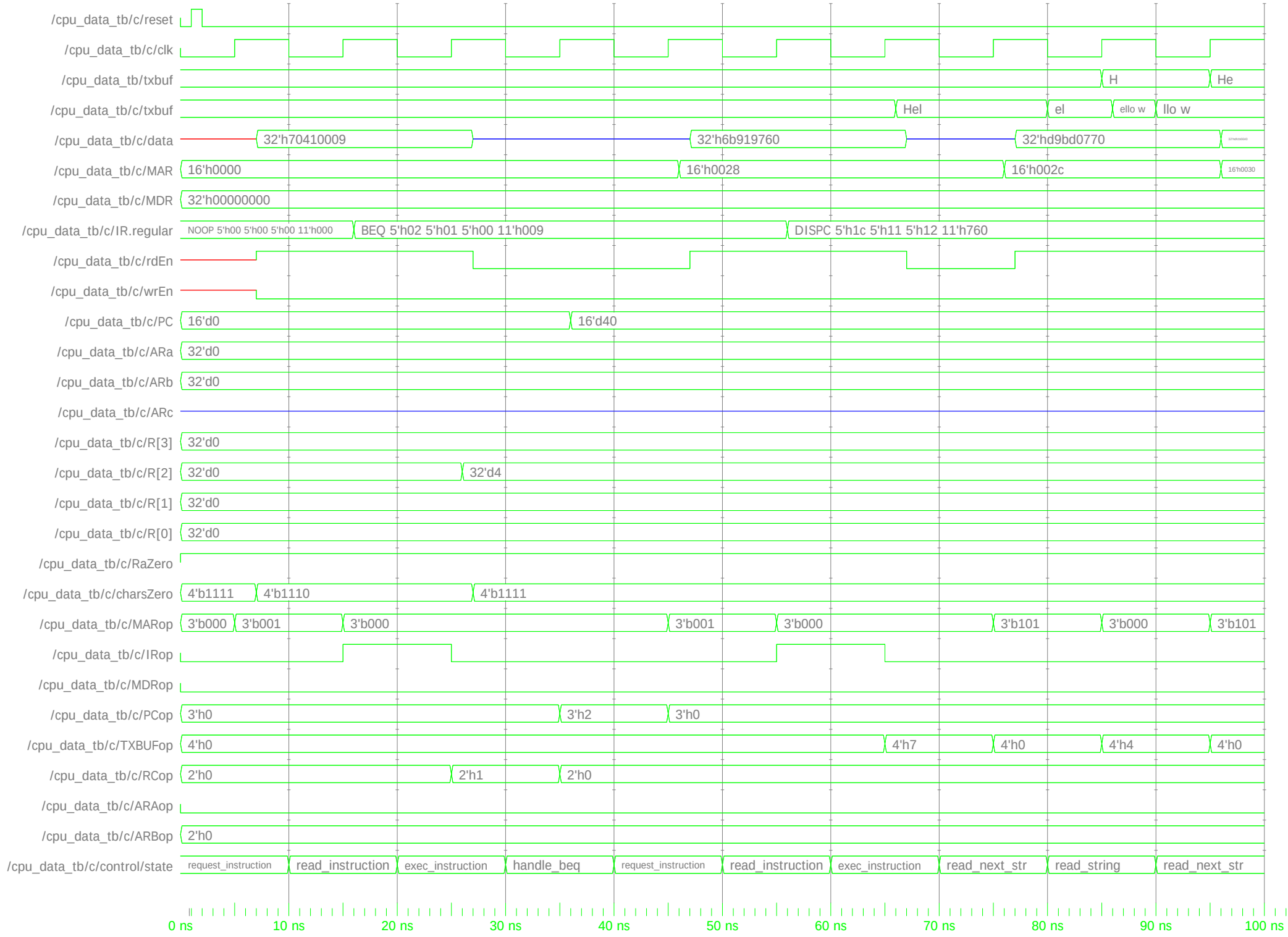
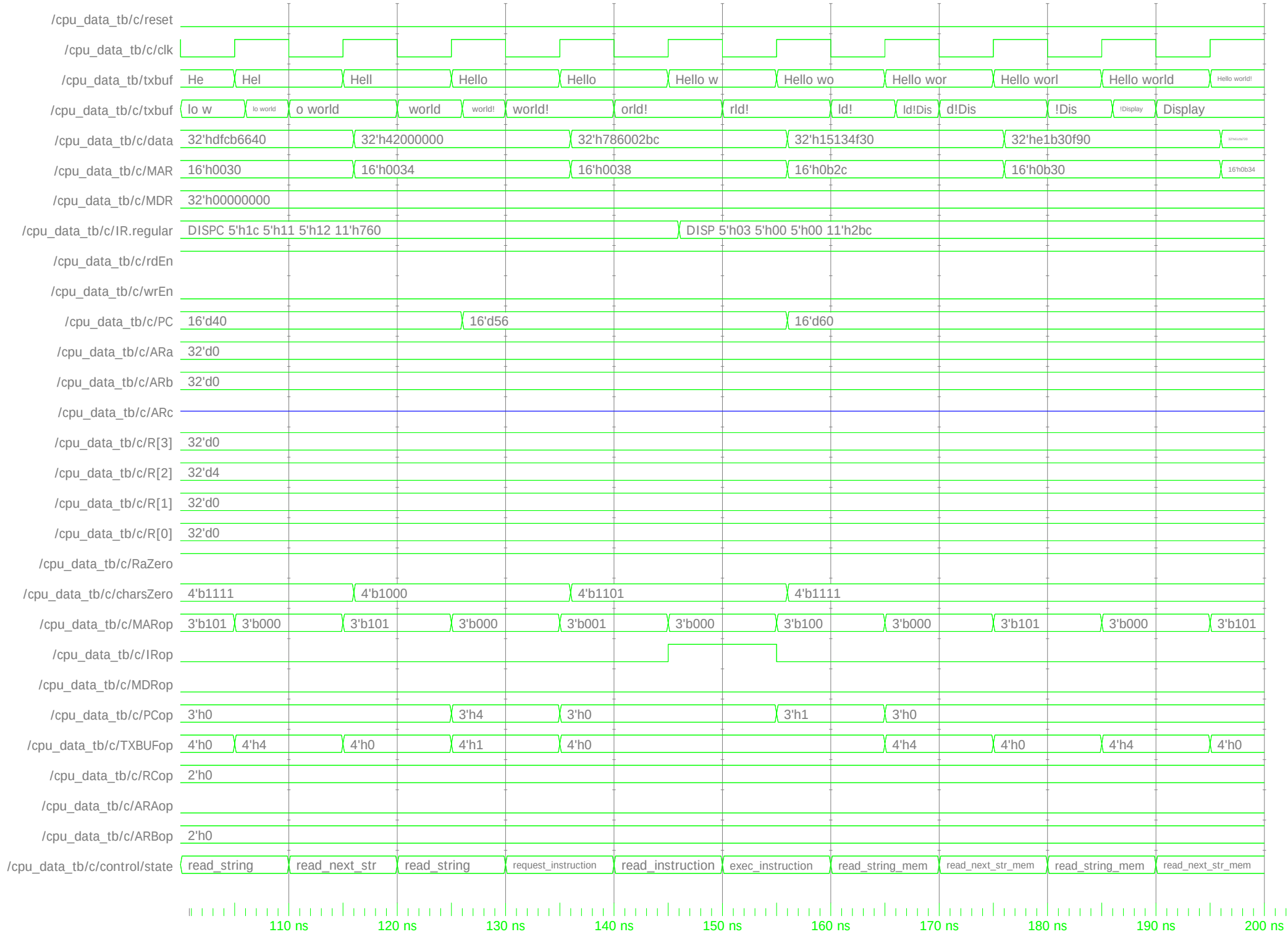
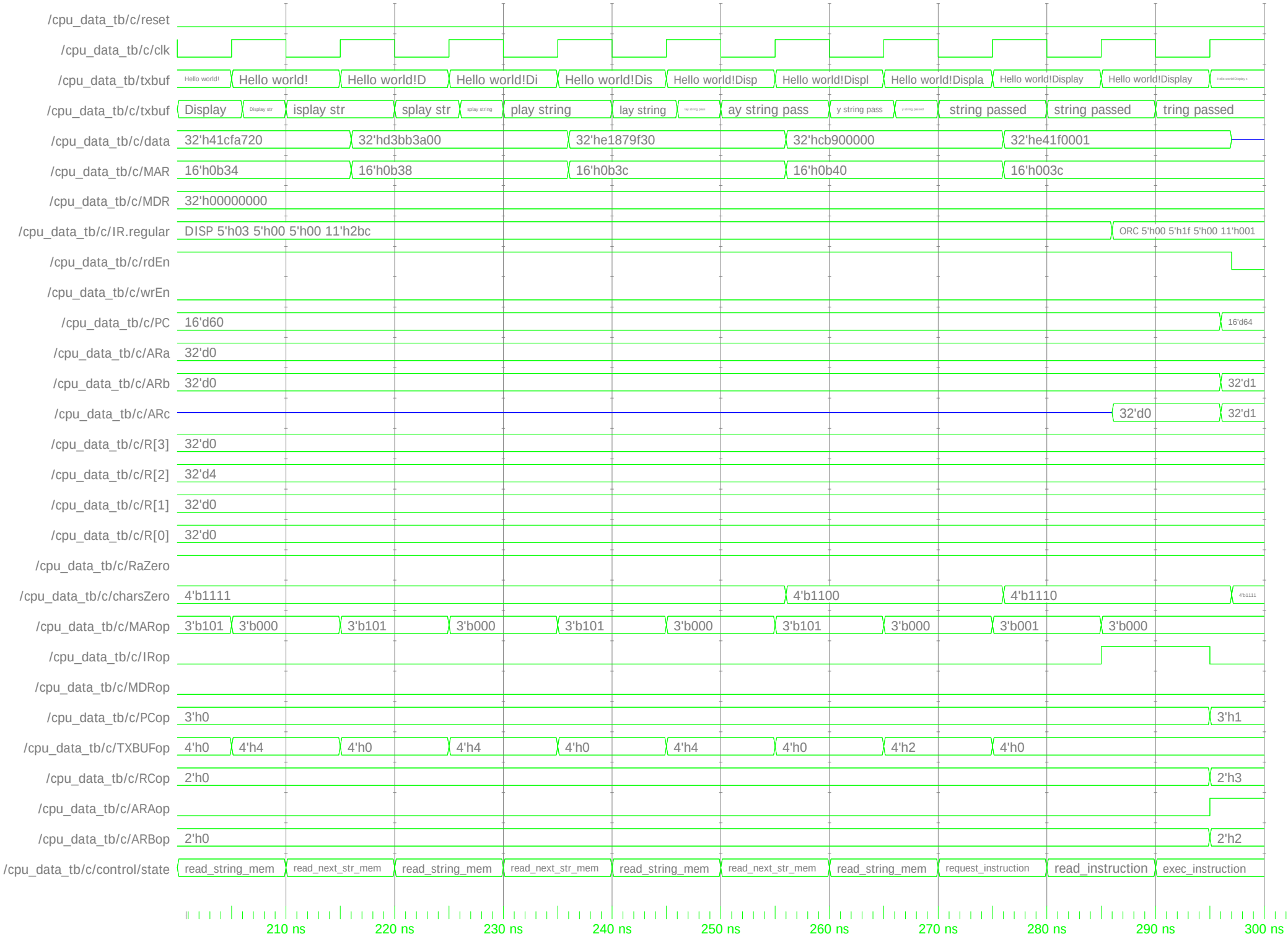


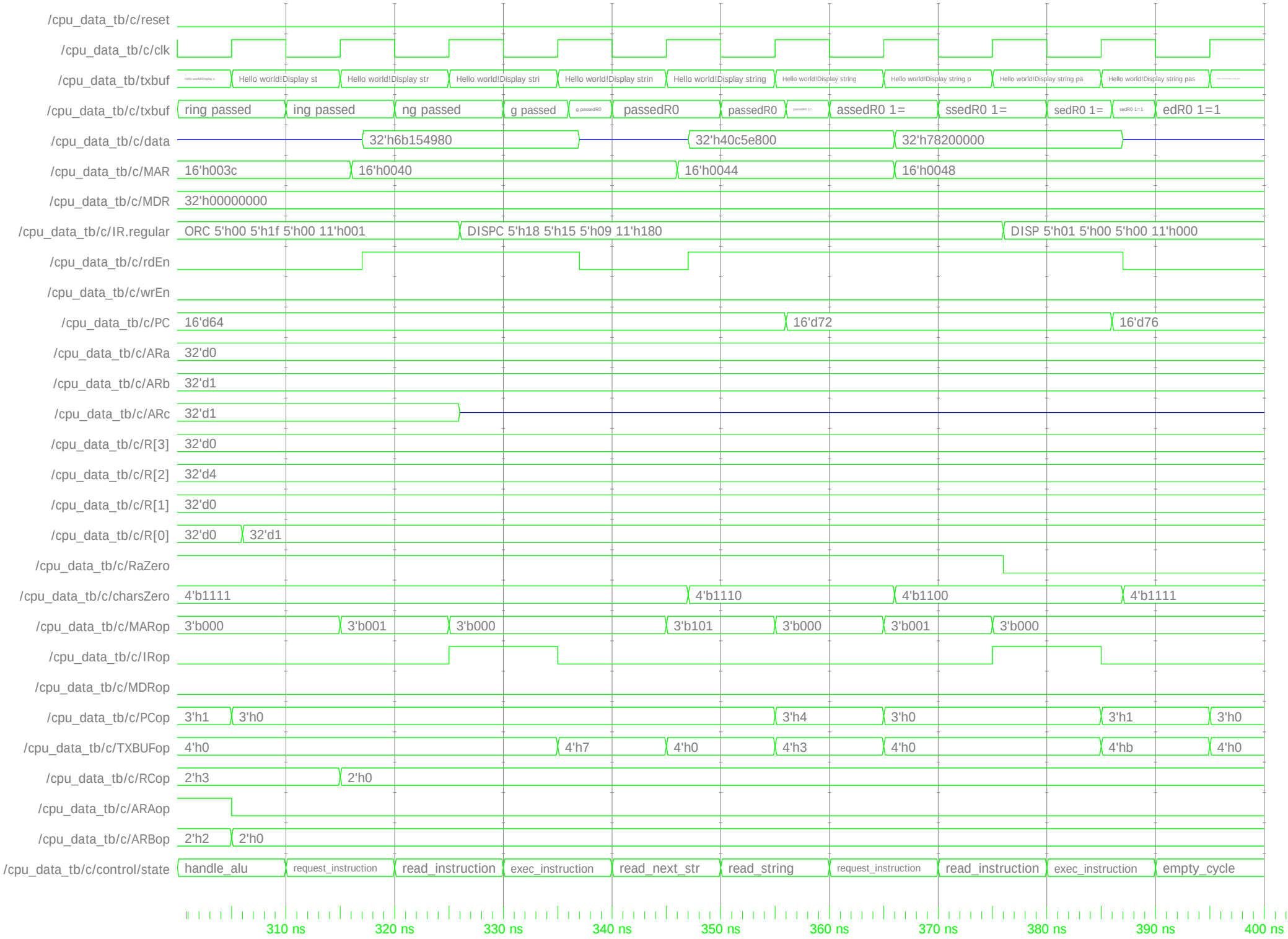
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 1 Page: 1



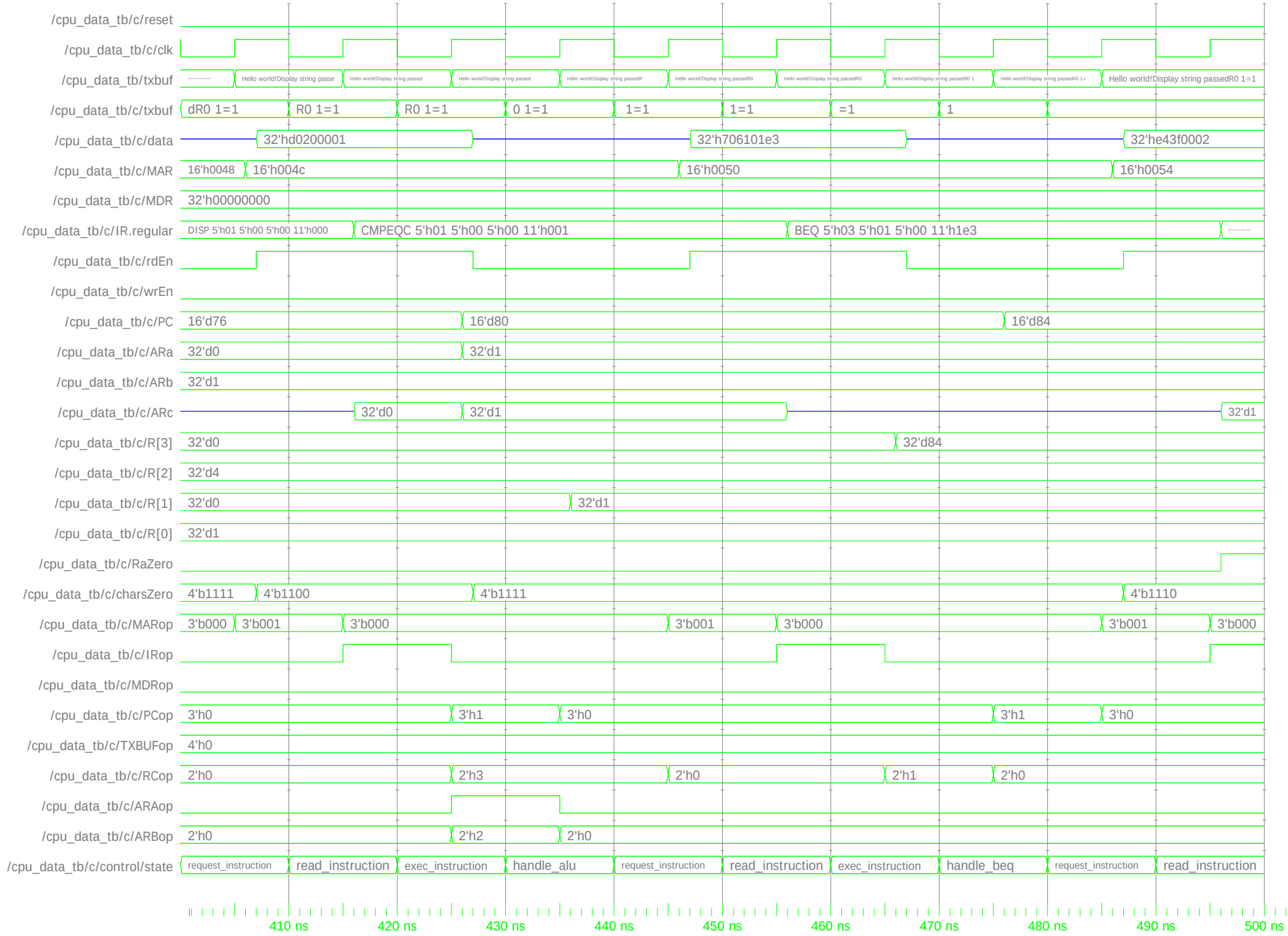
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 2 Page: 2



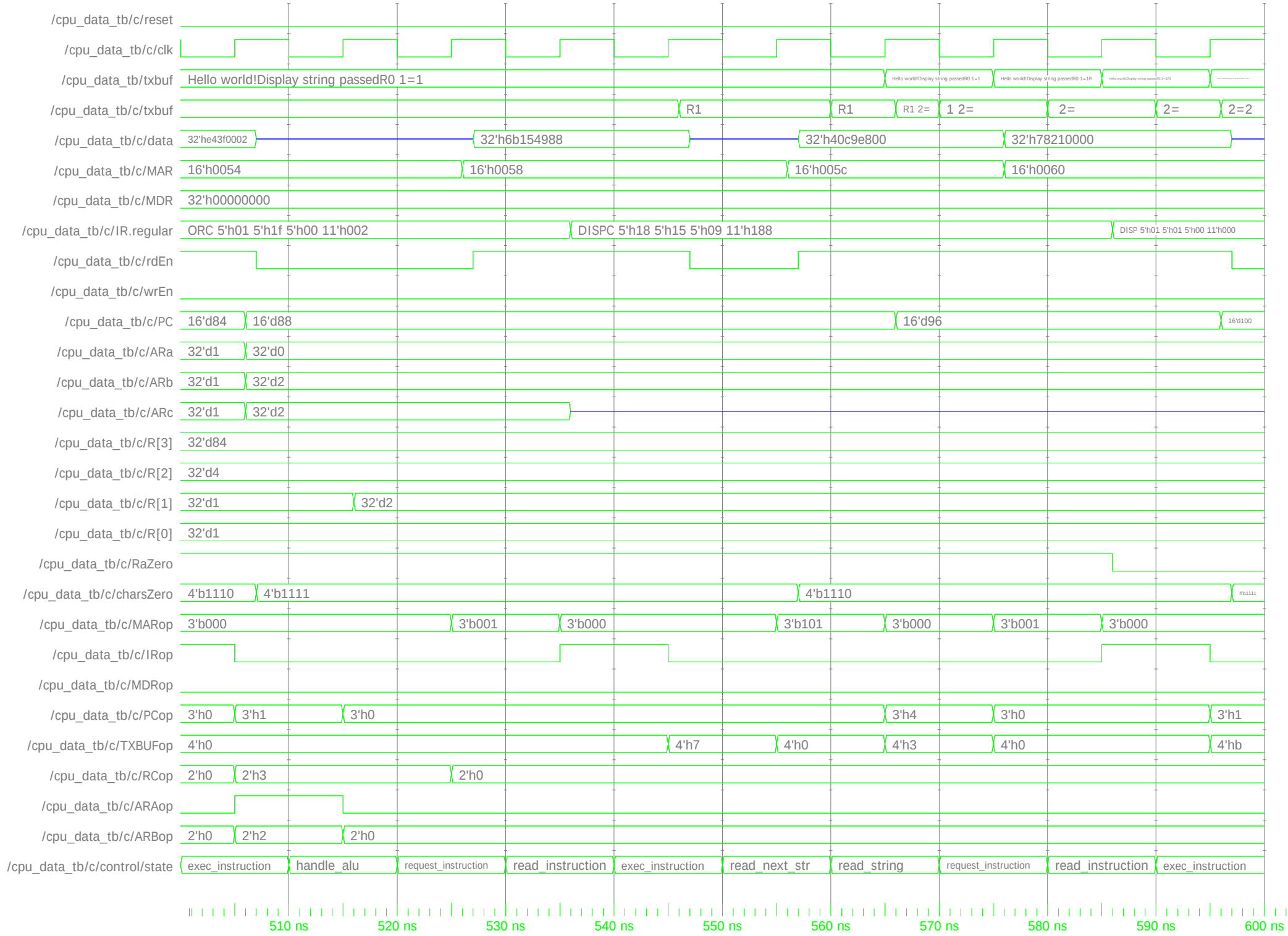
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 3 Page: 3

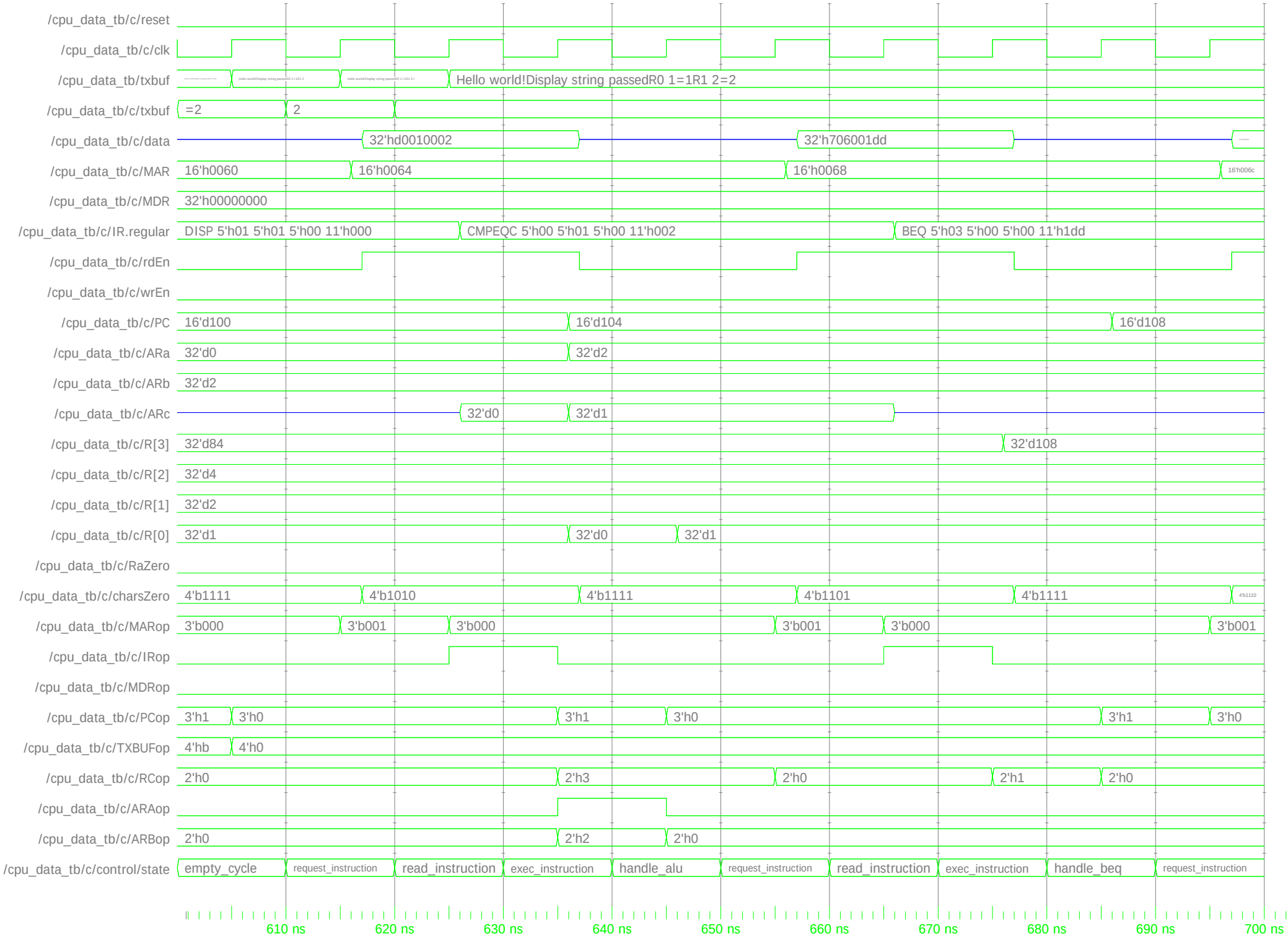


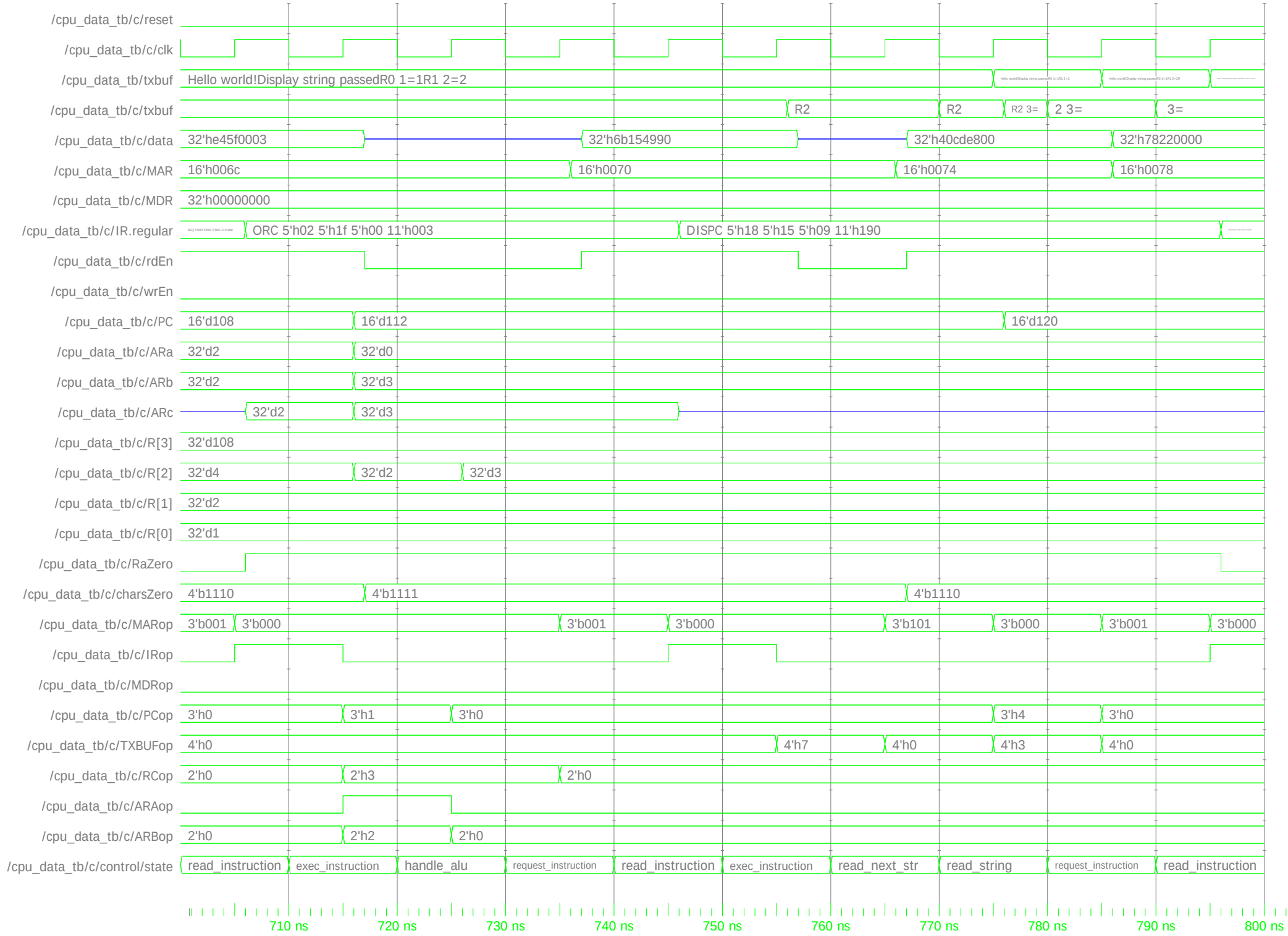
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 4 Page: 4



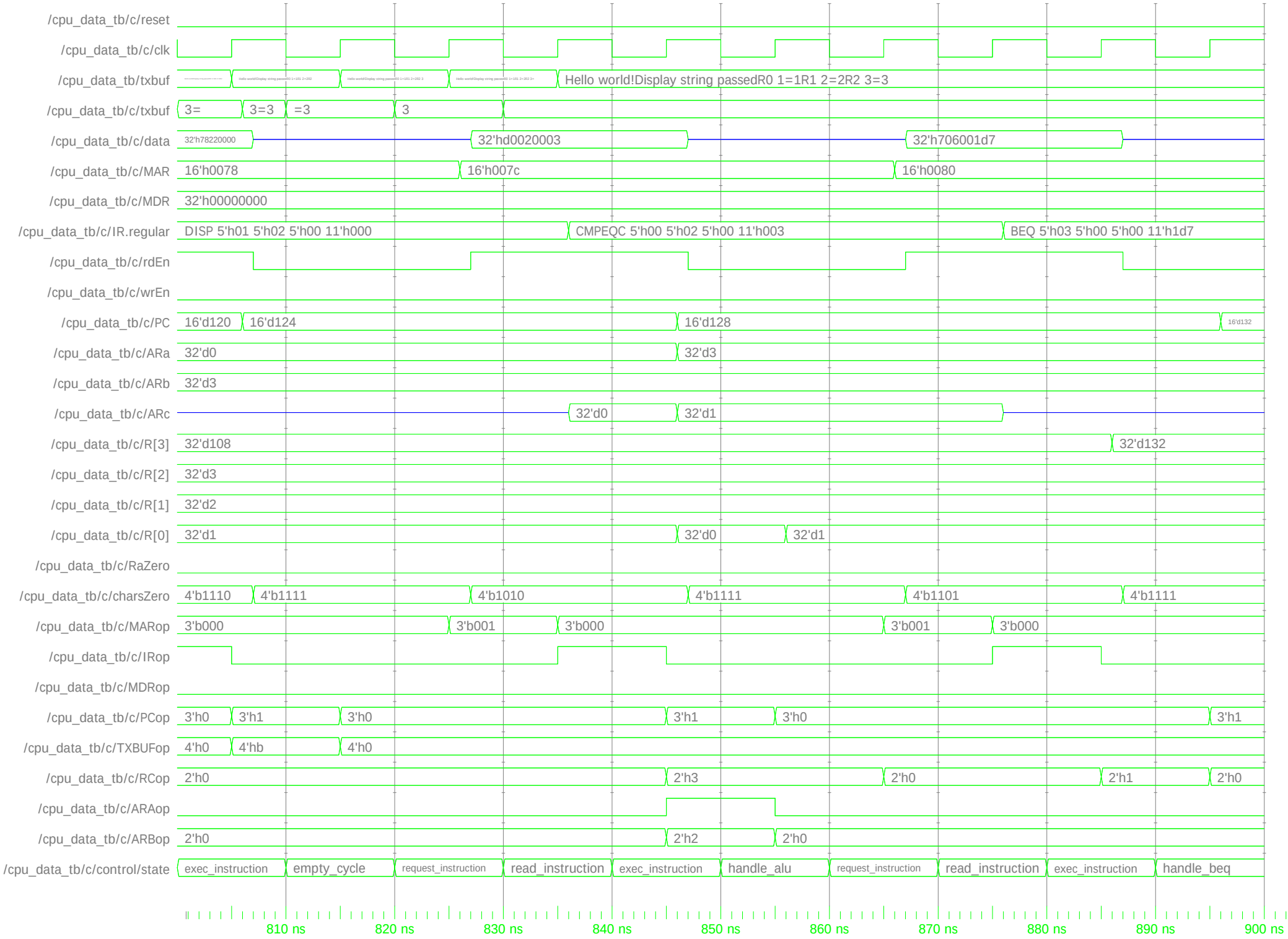
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 5 Page: 5

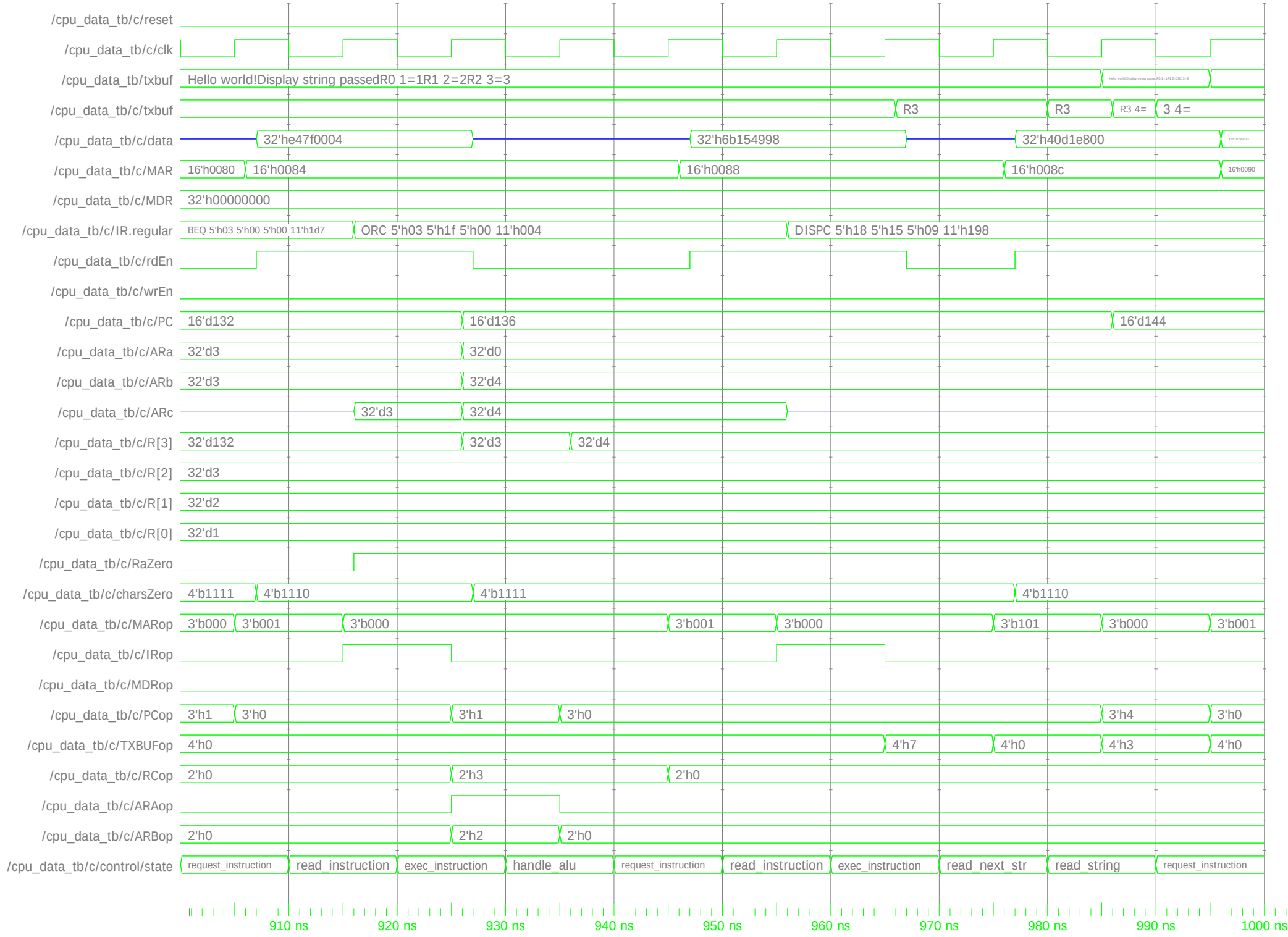

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1
/cpu_data_tb/c/txbuf
R1
R1
R1 2=
1 2=
2=
2=
2=2
/cpu_data_tb/c/data
32'he43f0002
32'h6b154988
32'h40c9e800
32'h78210000
/cpu_data_tb/c/MAR
16'h0054
16'h0058
16'h005c
16'h0060
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
ORC 5'h01 5'h1f 5'h00 11'h002
DISPC 5'h18 5'h15 5'h09 11'h188
DISP 5'h01 5'h01 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd84
16'd88
16'd96
16'd100
/cpu_data_tb/c/ARa
32'd1
32'd0
/cpu_data_tb/c/ARb
32'd1
32'd2
/cpu_data_tb/c/ARc
32'd1
32'd2
/cpu_data_tb/c/R[3]
32'd84
/cpu_data_tb/c/R[2]
32'd4
/cpu_data_tb/c/R[1]
32'd1
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b101
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h3
4'h0
4'hb
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
510 ns
520 ns
530 ns
540 ns
550 ns
560 ns
570 ns
580 ns
590 ns
600 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2
/cpu_data_tb/c/txbuf
=2
2
/cpu_data_tb/c/data
32'hd0010002
32'h706001dd
/cpu_data_tb/c/MAR
16'h0060
16'h0064
16'h0068
16'h006c
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h01 5'h00 11'h000
CMPEQC 5'h00 5'h01 5'h00 11'h002
BEQ 5'h03 5'h00 5'h00 11'h1dd
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd100
16'd104
16'd108
/cpu_data_tb/c/ARa
32'd0
32'd2
/cpu_data_tb/c/ARb
32'd2
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd84
32'd108
/cpu_data_tb/c/R[2]
32'd4
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1010
4'b1111
4'b1101
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
610 ns
620 ns
630 ns
640 ns
650 ns
660 ns
670 ns
680 ns
690 ns
700 ns

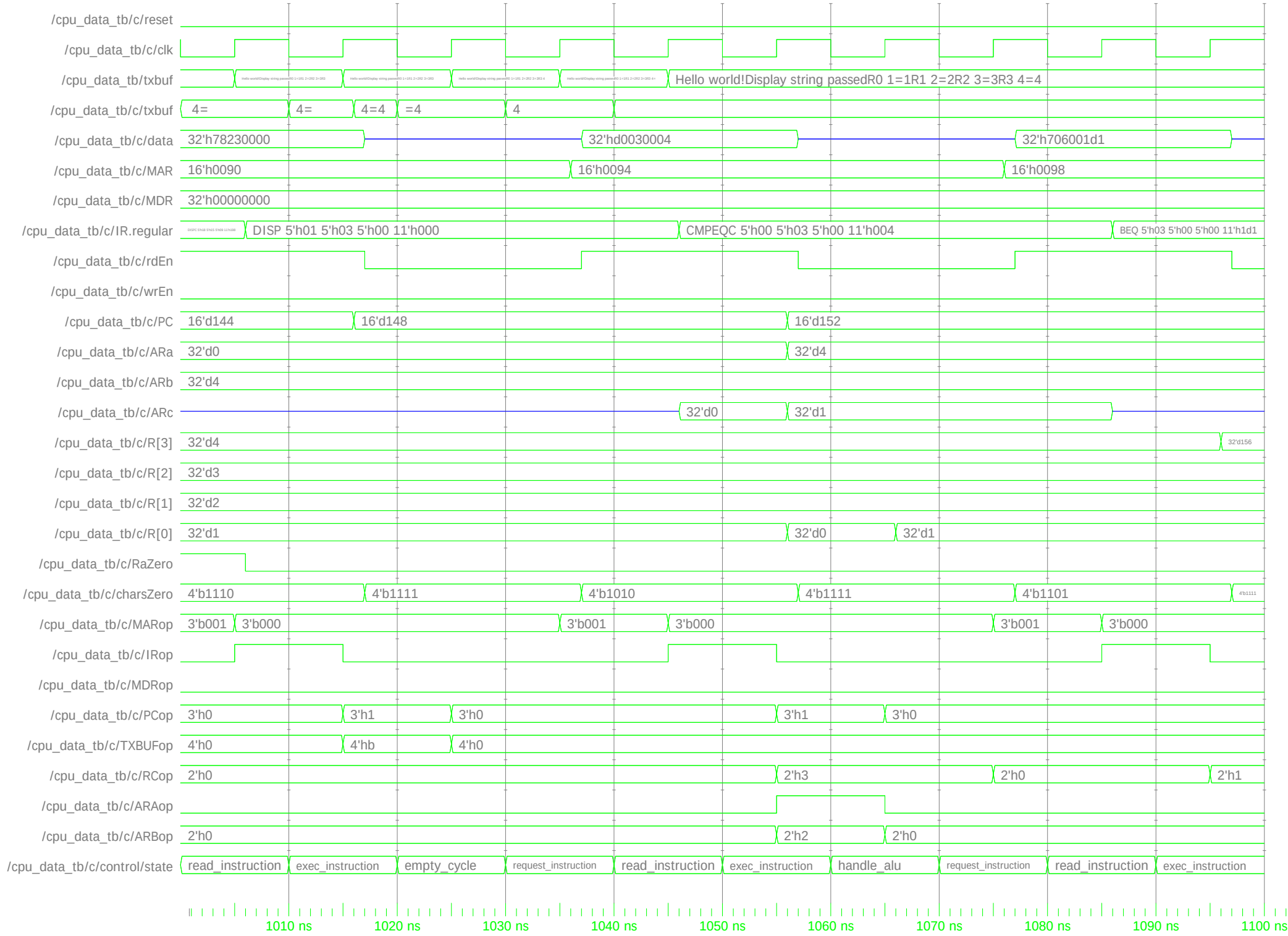


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 8 Page: 8

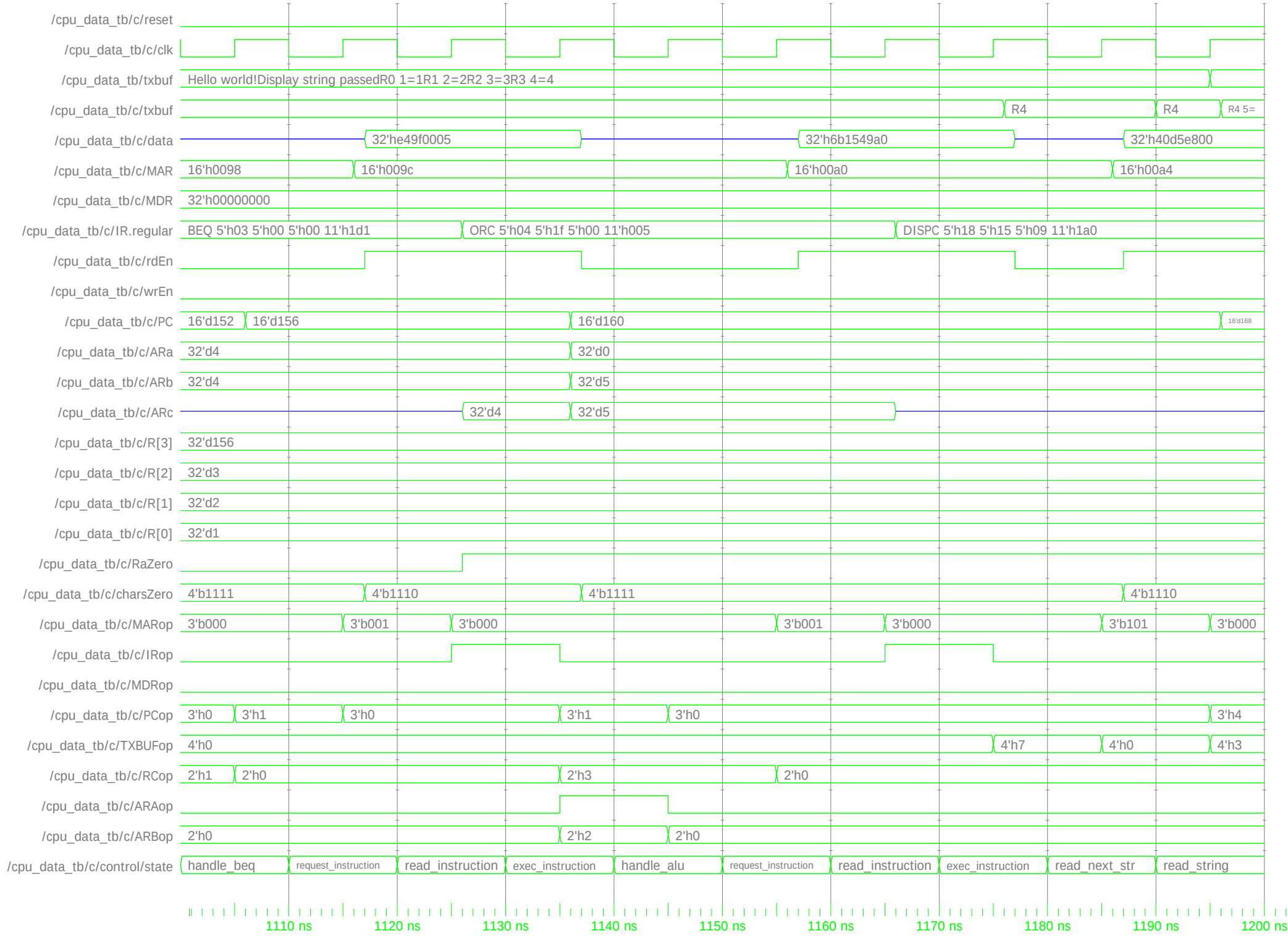

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
/cpu_data_tb/c/MAR
/cpu_data_tb/c/MDR
/cpu_data_tb/c/IR.regular
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
/cpu_data_tb/c/ARa
/cpu_data_tb/c/ARb
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
/cpu_data_tb/c/R[2]
/cpu_data_tb/c/R[1]
/cpu_data_tb/c/R[0]
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
/cpu_data_tb/c/MARop
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
/cpu_data_tb/c/TXBUFop
/cpu_data_tb/c/RCop
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
/cpu_data_tb/c/control/state
Hello world!Display string passedR0 1=1R1 2=2R2 3=3
3=
3=3
=3
3
32'h78220000
32'hd0020003
32'h706001d7
16'h0078
16'h007c
16'h0080
32'h00000000
DISP 5'h01 5'h02 5'h00 11'h000
CMPEQC 5'h00 5'h02 5'h00 11'h003
BEQ 5'h03 5'h00 5'h00 11'h1d7
16'd120
16'd124
16'd128
16'd132
32'd0
32'd3
32'd3
32'd0
32'd1
32'd108
32'd132
32'd3
32'd2
32'd1
32'd0
32'd1
4'b1110
4'b1111
4'b1010
4'b1111
4'b1101
4'b1111
3'b000
3'b001
3'b000
3'b001
3'b000
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
4'h0
4'hb
4'h0
2'h0
2'h3
2'h0
2'h1
2'h0
2'h0
2'h2
2'h0
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
810 ns
820 ns
830 ns
840 ns
850 ns
860 ns
870 ns
880 ns
890 ns
900 ns



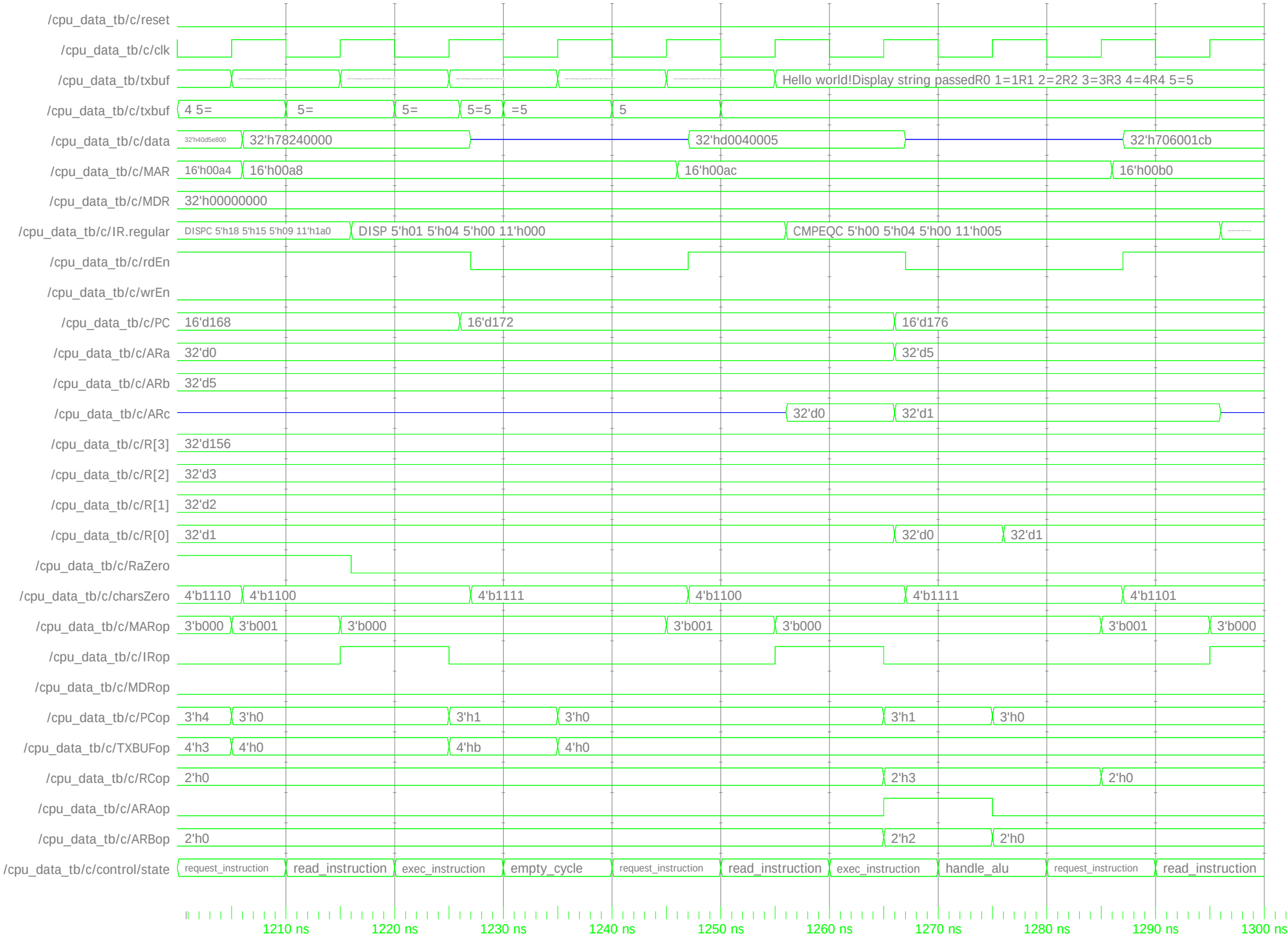
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 10 Page: 10

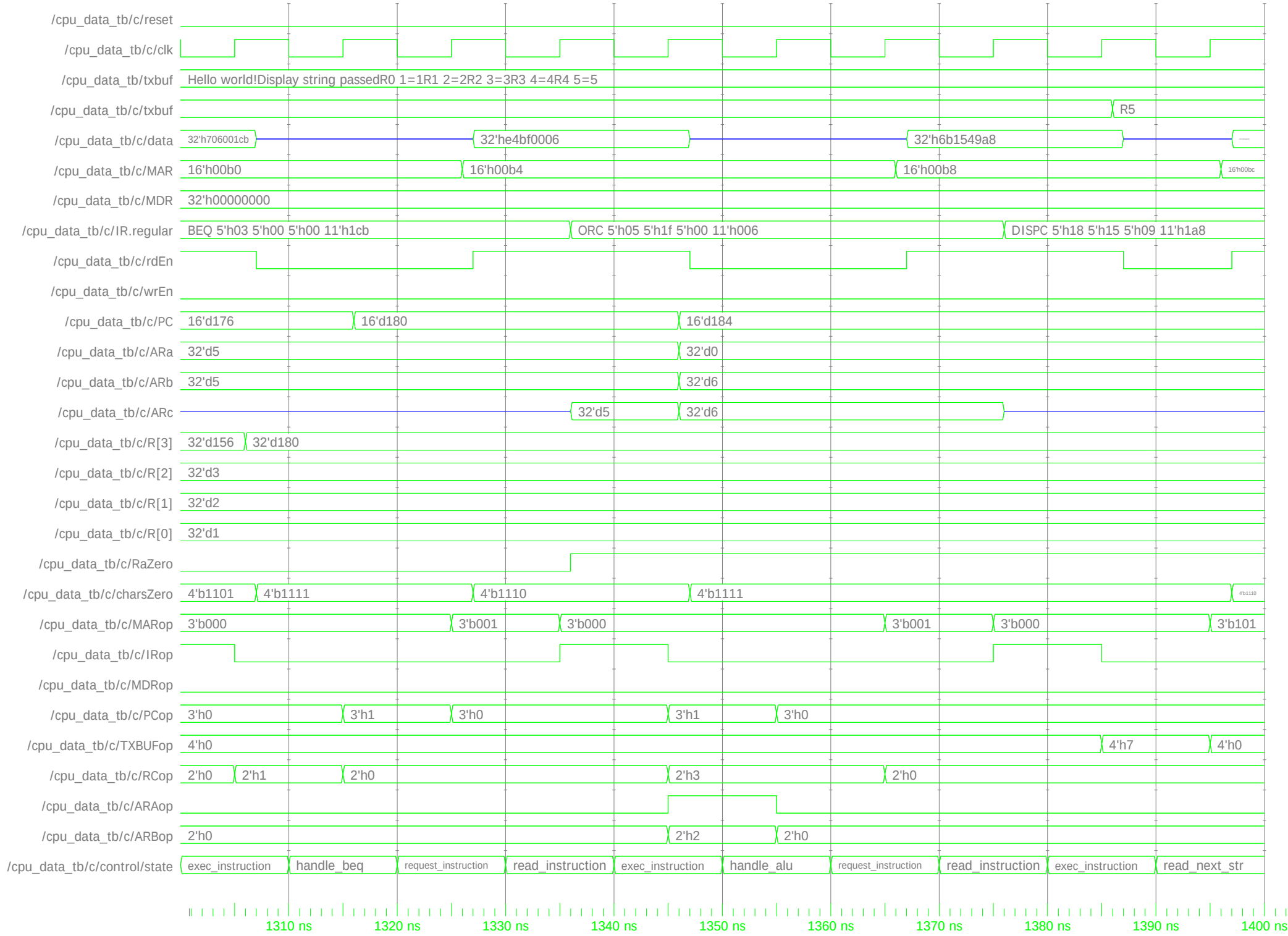


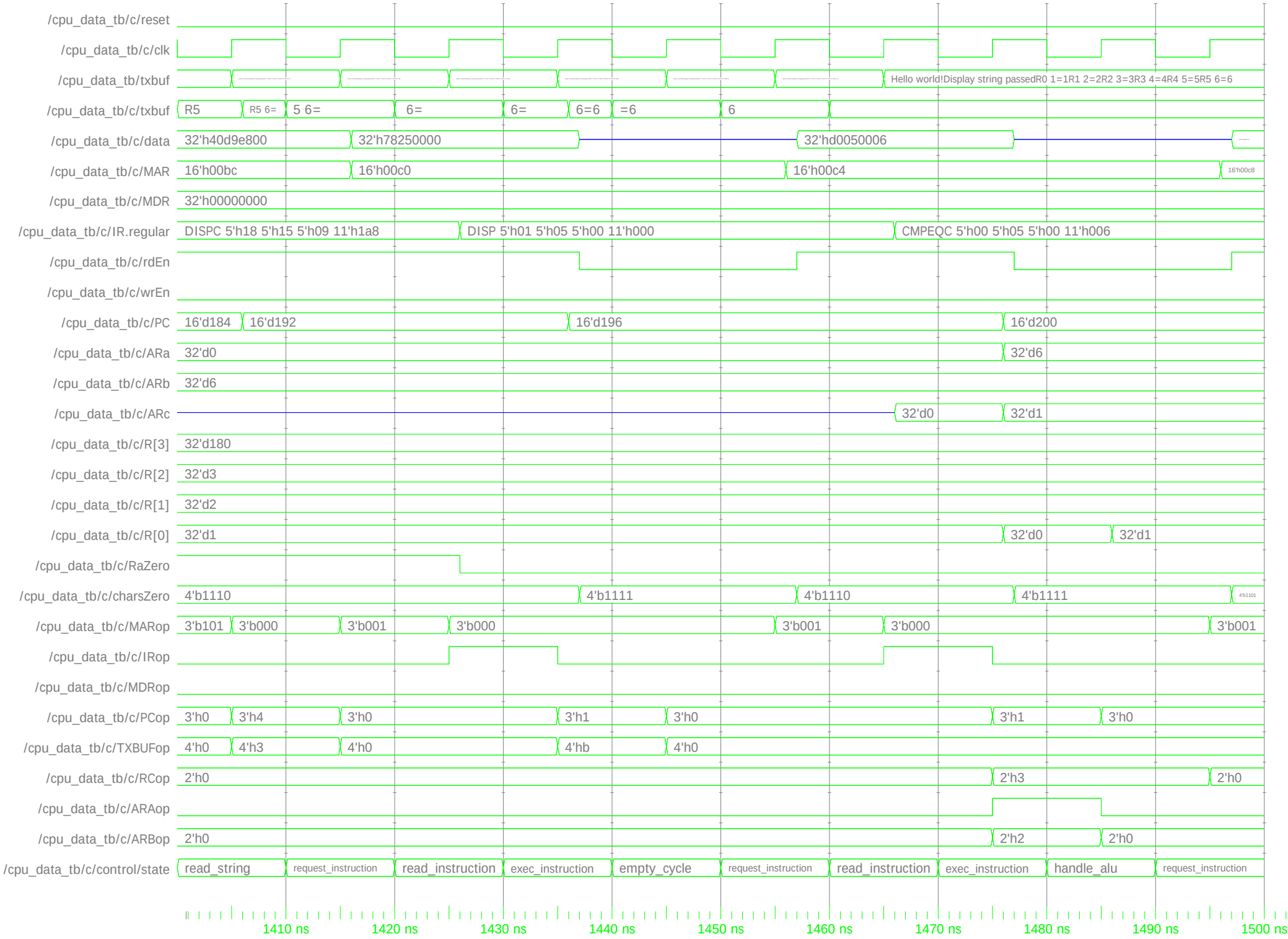
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 11 Page: 11

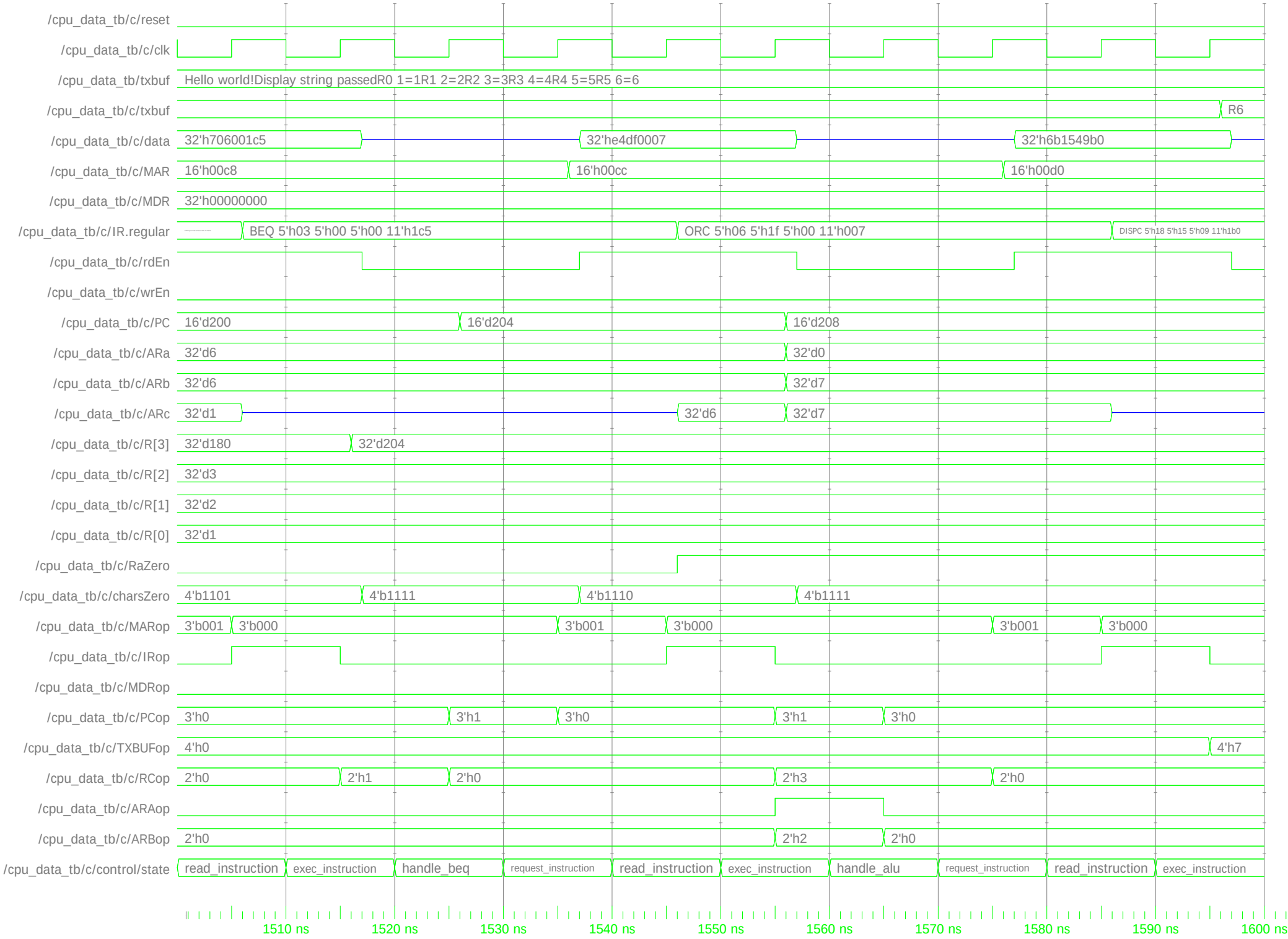


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 12 Page: 12

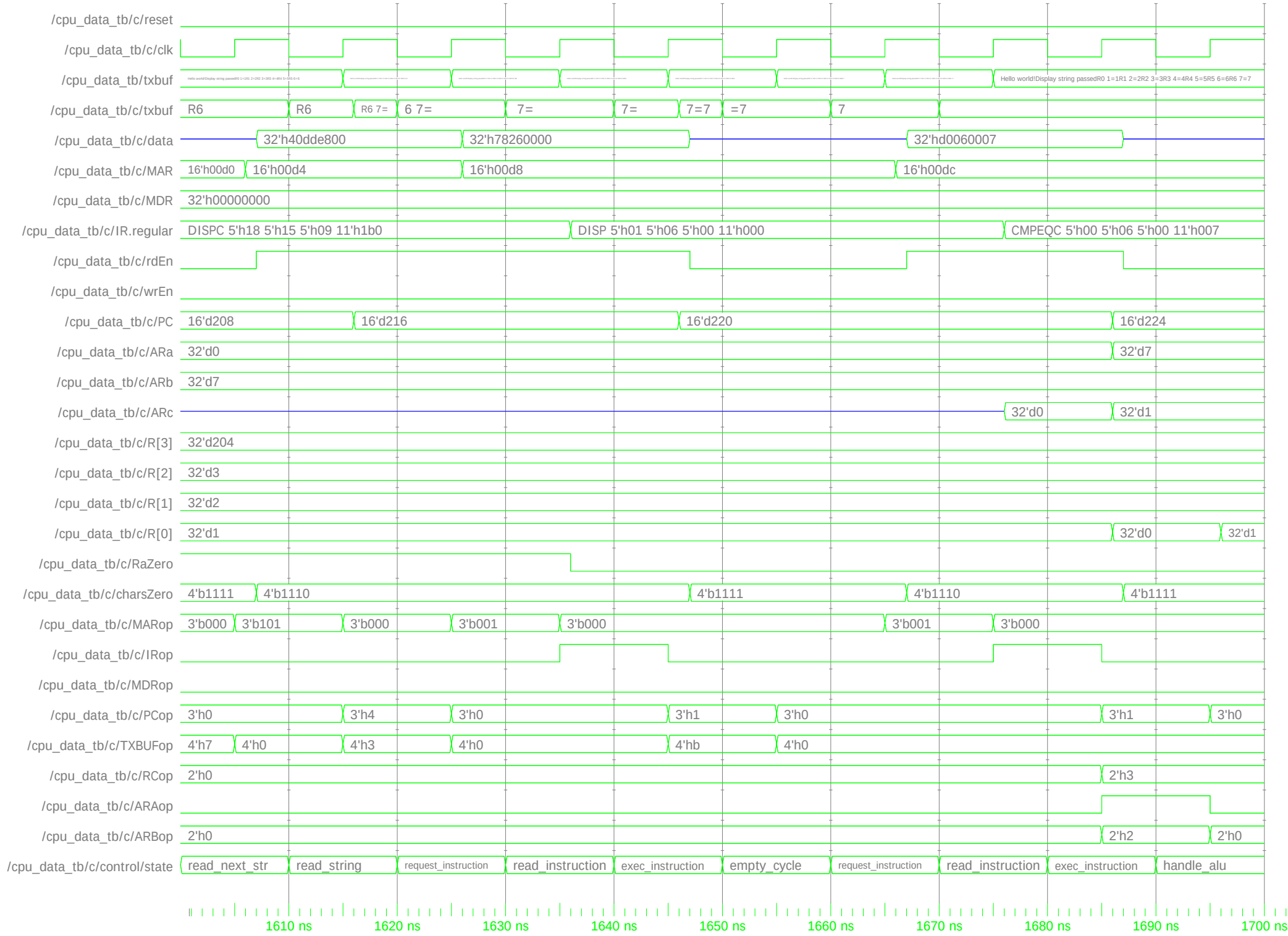

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5
/cpu_data_tb/c/txbuf
4 5= 5= 5= 5=5 =5 5
/cpu_data_tb/c/data
32'h40d5e800 32'h78240000 32'hd0040005 32'h706001cb
/cpu_data_tb/c/MAR
16'h00a4 16'h00a8 16'h00ac 16'h00b0
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h1a0 DISP 5'h01 5'h04 5'h00 11'h000 CMPEQC 5'h00 5'h04 5'h00 11'h005
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd168 16'd172 16'd176
/cpu_data_tb/c/ARa
32'd0 32'd5
/cpu_data_tb/c/ARb
32'd5
/cpu_data_tb/c/ARc
32'd0 32'd1
/cpu_data_tb/c/R[3]
32'd156
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1 32'd0 32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110 4'b1100 4'b1111 4'b1100 4'b1111 4'b1101
/cpu_data_tb/c/MARop
3'b000 3'b001 3'b000 3'b001 3'b000 3'b001 3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h4 3'h0 3'h1 3'h0 3'h1 3'h0
/cpu_data_tb/c/TXBUFop
4'h3 4'h0 4'hb 4'h0
/cpu_data_tb/c/RCop
2'h0 2'h3 2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0 2'h2 2'h0
/cpu_data_tb/c/control/state
request_instruction read_instruction exec_instruction empty_cycle request_instruction read_instruction exec_instruction handle_alu request_instruction read_instruction
1210 ns 1220 ns 1230 ns 1240 ns 1250 ns 1260 ns 1270 ns 1280 ns 1290 ns 1300 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5
/cpu_data_tb/c/txbuf
R5
/cpu_data_tb/c/data
32'h706001cb
32'he4bf0006
32'h6b1549a8
/cpu_data_tb/c/MAR
16'h00b0
16'h00b4
16'h00b8
16'h00bc
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h00 5'h00 11'h1cb
ORC 5'h05 5'h1f 5'h00 11'h006
DISPC 5'h18 5'h15 5'h09 11'h1a8
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd176
16'd180
16'd184
/cpu_data_tb/c/ARa
32'd5
32'd0
/cpu_data_tb/c/ARb
32'd5
32'd6
/cpu_data_tb/c/ARc
32'd5
32'd6
/cpu_data_tb/c/R[3]
32'd156
32'd180
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
4'b1110
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b101
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h1
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
read_next_str
1310 ns
1320 ns
1330 ns
1340 ns
1350 ns
1360 ns
1370 ns
1380 ns
1390 ns
1400 ns

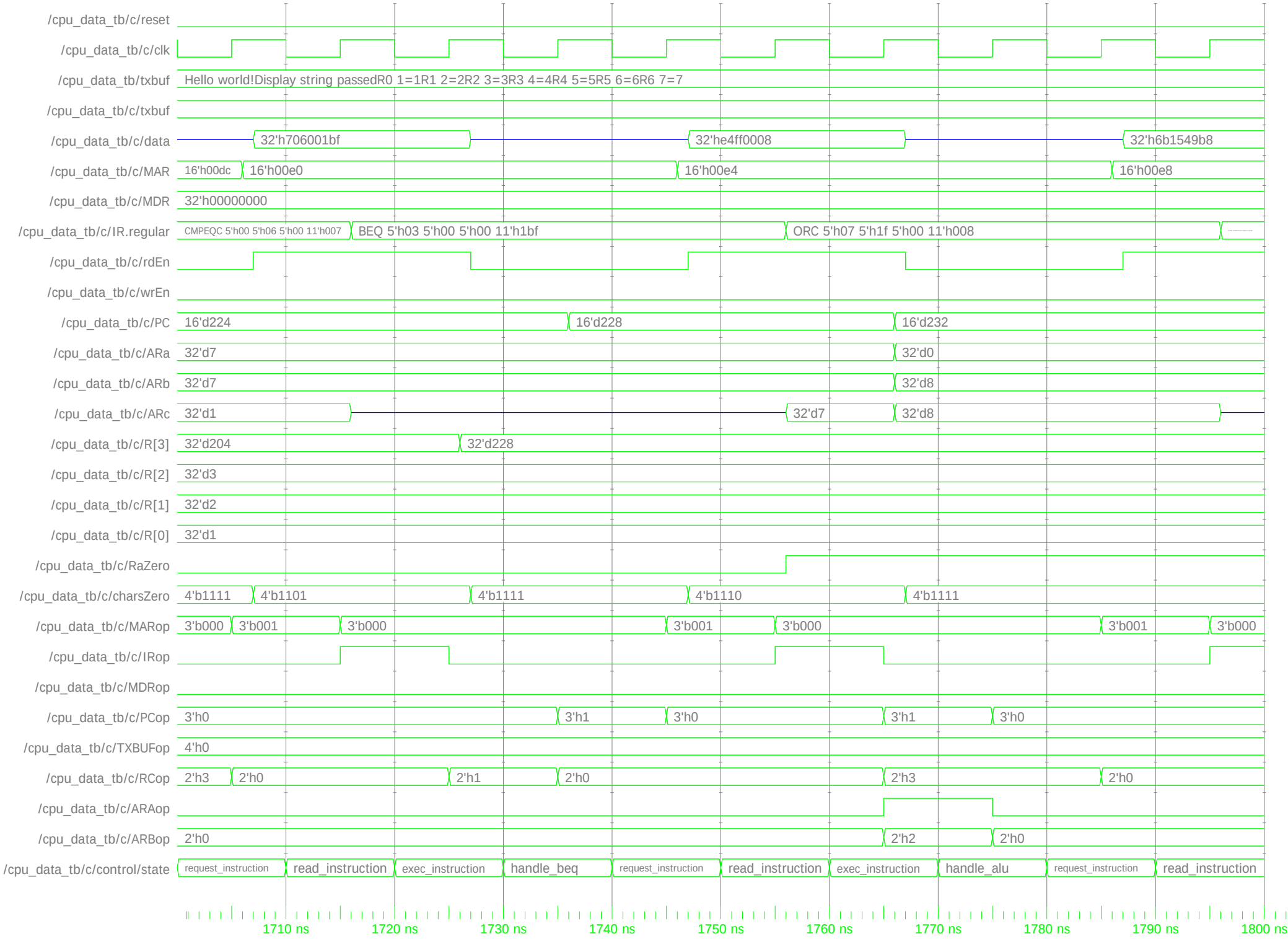

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6
/cpu_data_tb/c/txbuf
R5
R5 6=
5 6=
6=
6=
6=6
=6
6
/cpu_data_tb/c/data
32'h40d9e800
32'h78250000
32'hd0050006
/cpu_data_tb/c/MAR
16'h00bc
16'h00c0
16'h00c4
16'h00c8
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h1a8
DISP 5'h01 5'h05 5'h00 11'h000
CMPEQC 5'h00 5'h05 5'h00 11'h006
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd184
16'd192
16'd196
16'd200
/cpu_data_tb/c/ARa
32'd0
32'd6
/cpu_data_tb/c/ARb
32'd6
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd180
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1110
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h3
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
1410 ns
1420 ns
1430 ns
1440 ns
1450 ns
1460 ns
1470 ns
1480 ns
1490 ns
1500 ns



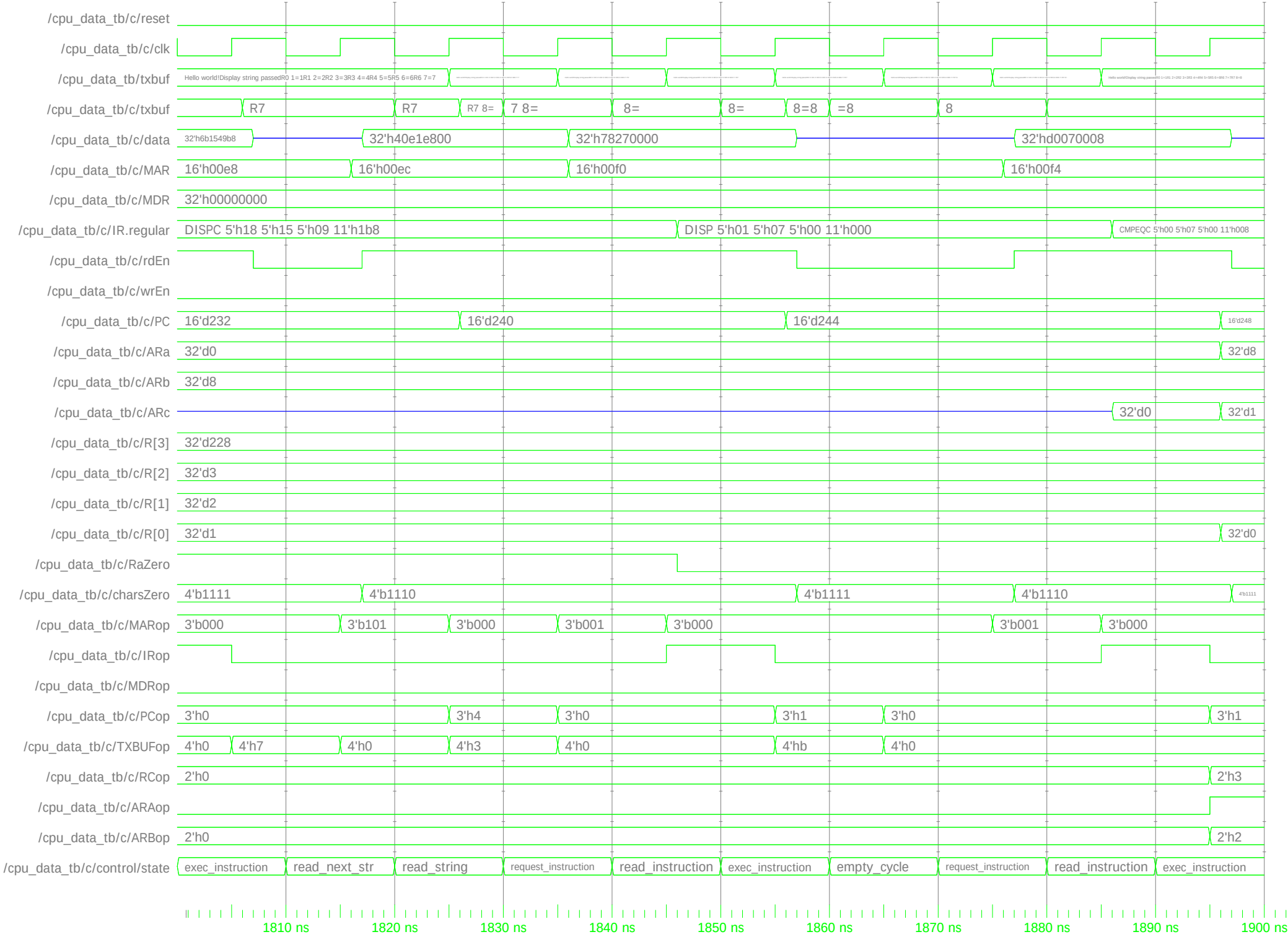
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 16 Page: 16

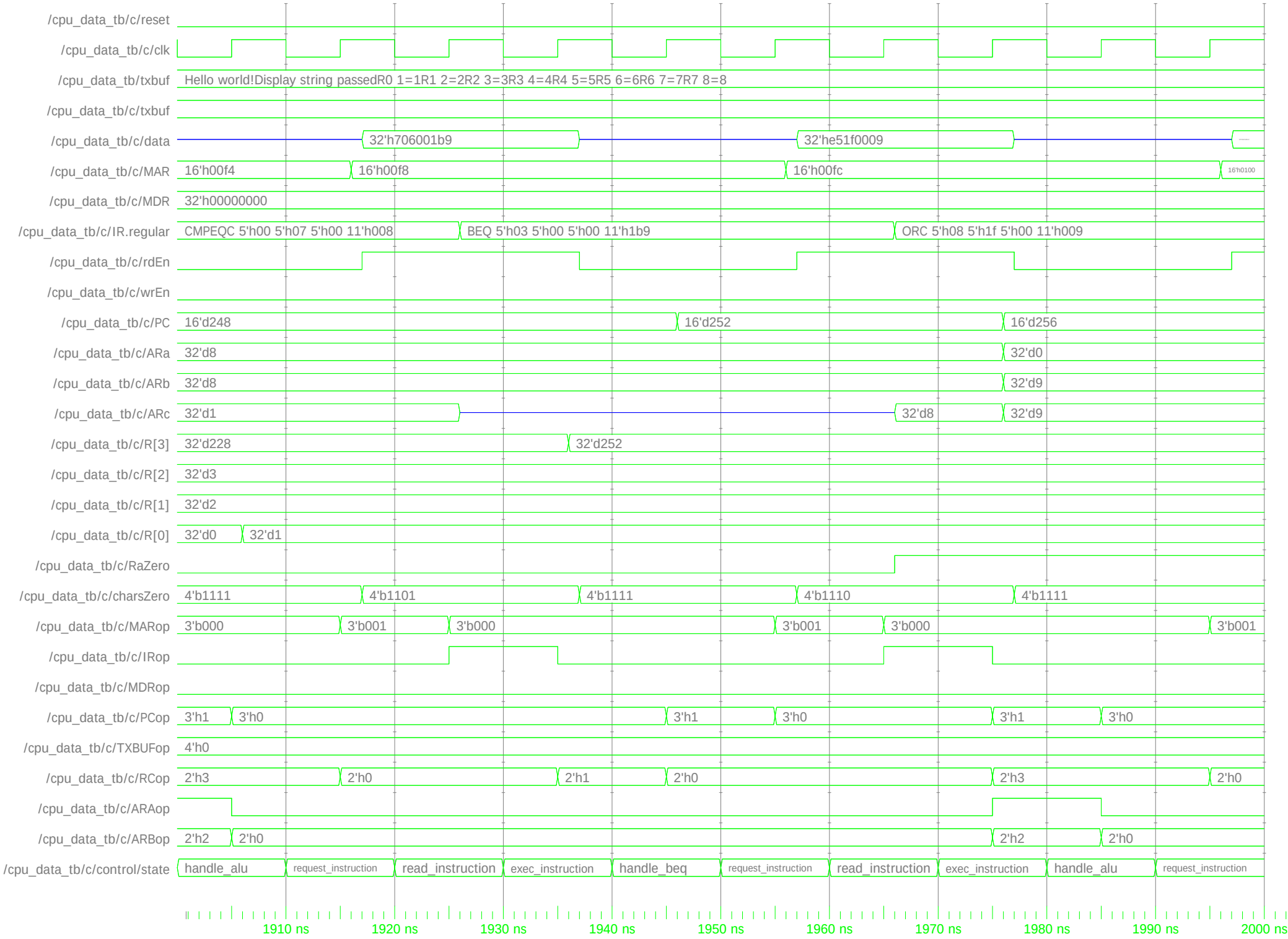


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 17 Page: 17

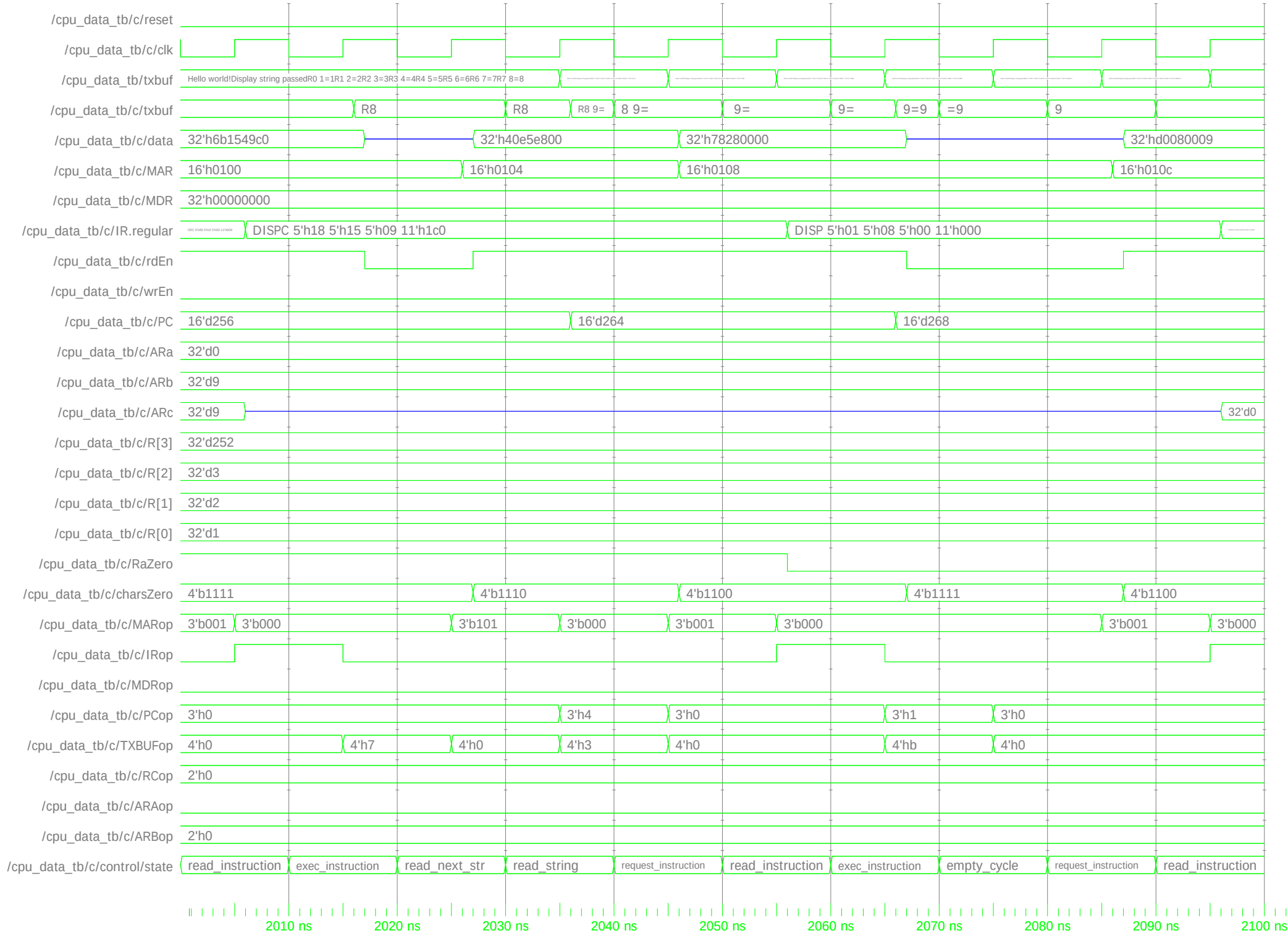


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 18 Page: 18

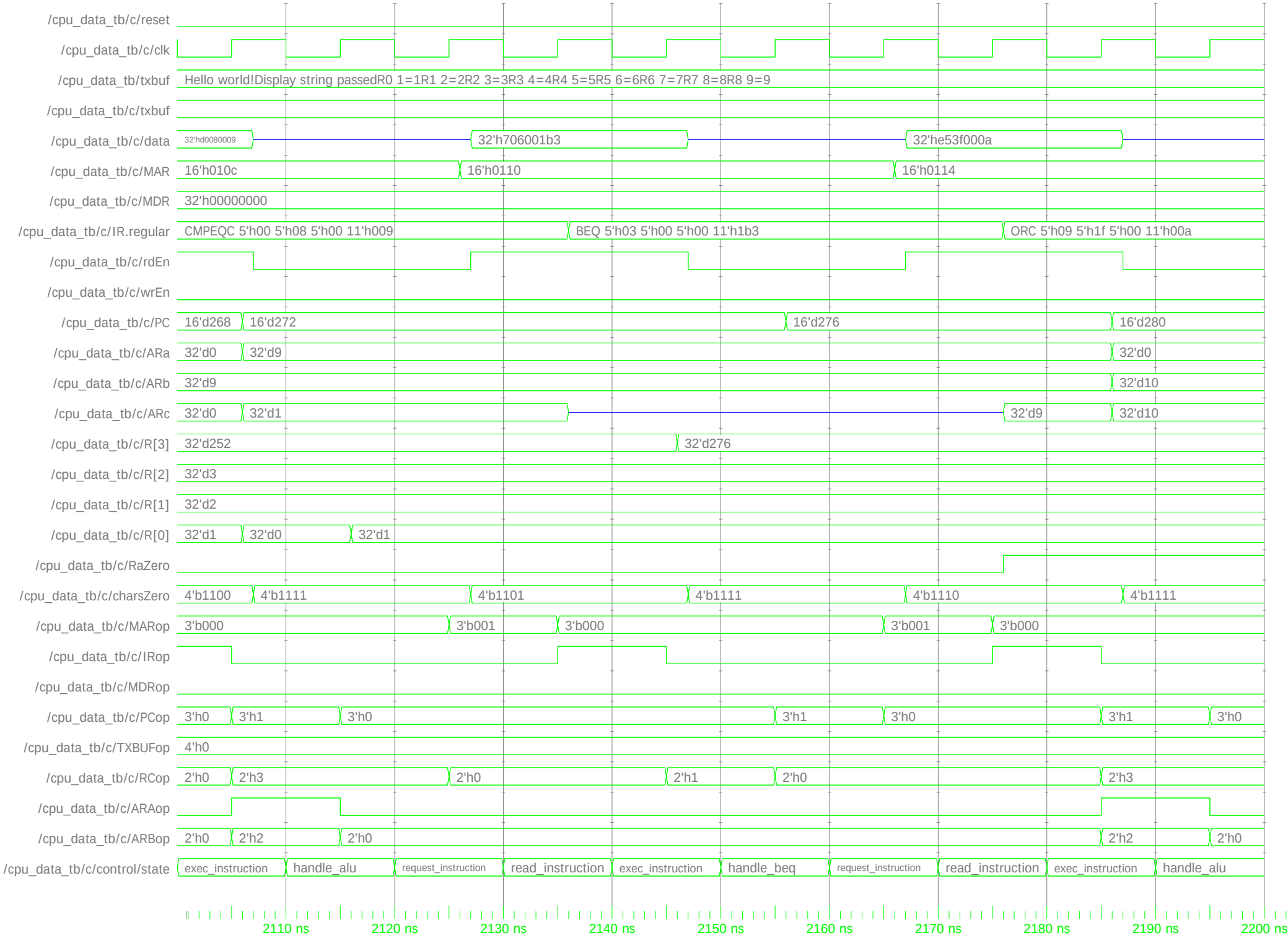

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7
/cpu_data_tb/c/txbuf
R7
R7
R7 8=
7 8=
8=
8=
8=8
=8
8
/cpu_data_tb/c/data
32'h6b1549b8
32'h40e1e800
32'h78270000
32'hd0070008
/cpu_data_tb/c/MAR
16'h00e8
16'h00ec
16'h00f0
16'h00f4
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h1b8
DISP 5'h01 5'h07 5'h00 11'h000
CMPEQC 5'h00 5'h07 5'h00 11'h008
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd232
16'd240
16'd244
16'd248
/cpu_data_tb/c/ARa
32'd0
32'd8
/cpu_data_tb/c/ARb
32'd8
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd228
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1110
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h3
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
/cpu_data_tb/c/control/state
exec_instruction
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
1810 ns
1820 ns
1830 ns
1840 ns
1850 ns
1860 ns
1870 ns
1880 ns
1890 ns
1900 ns



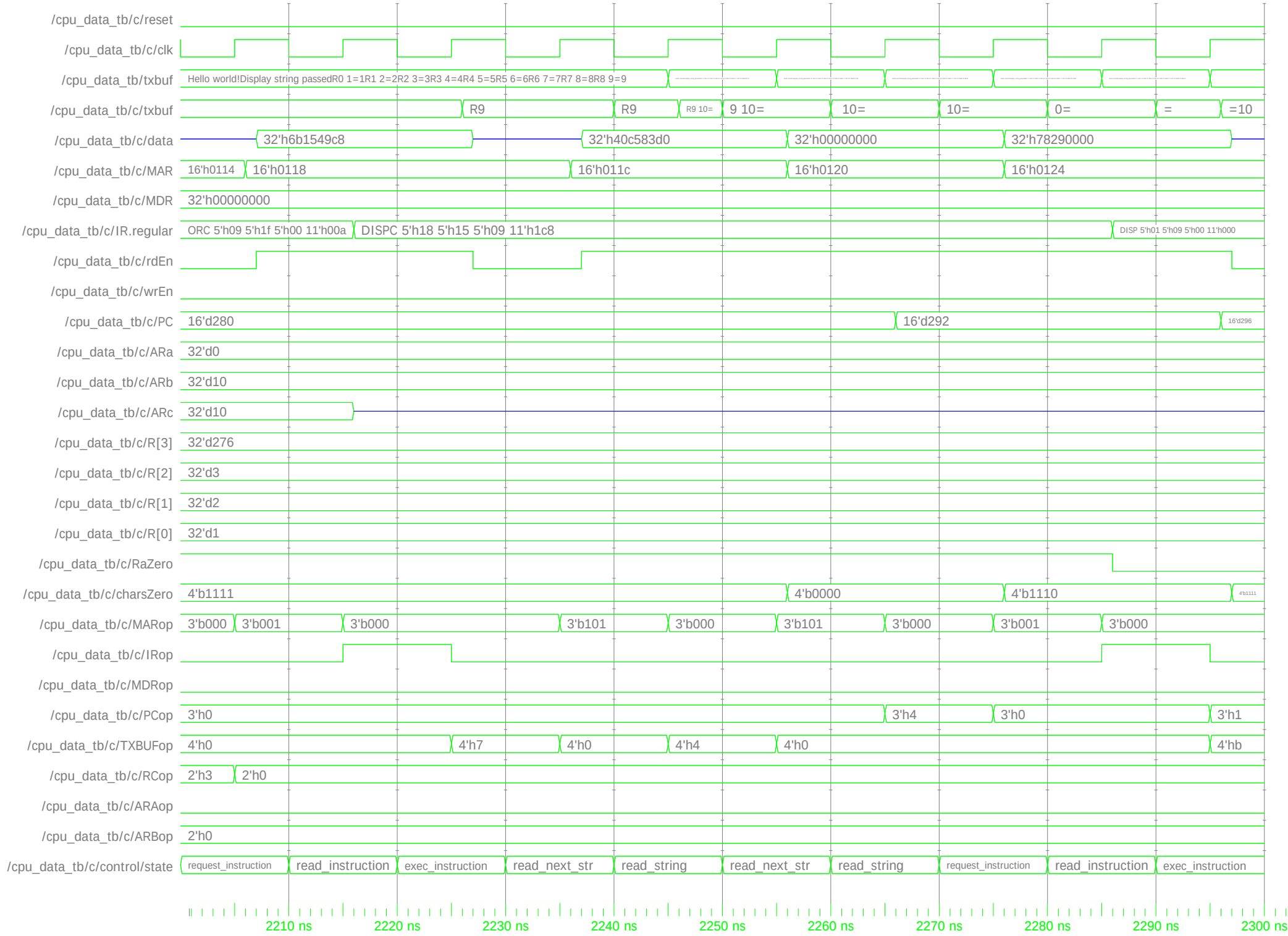
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 20 Page: 20



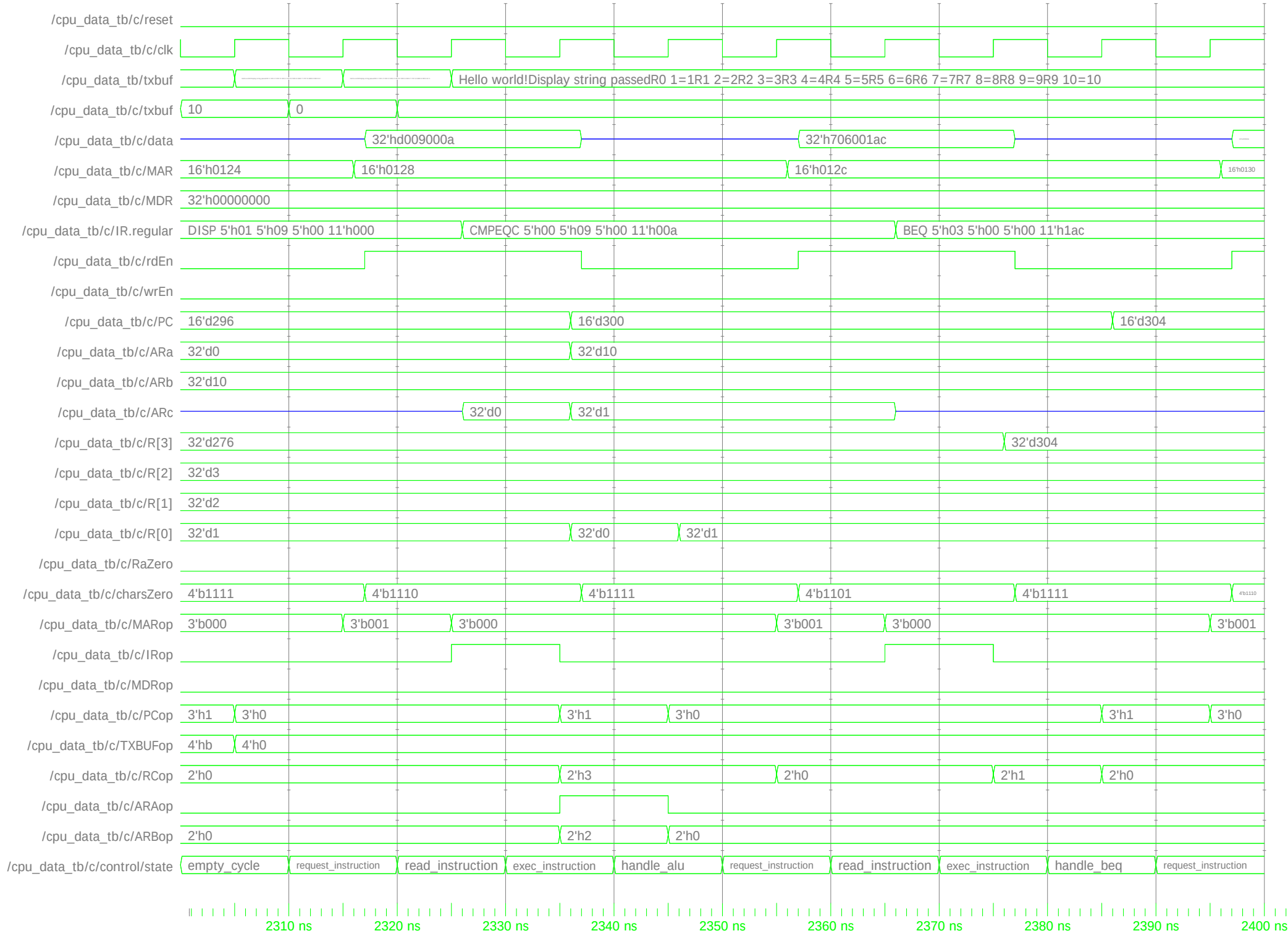
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 21 Page: 21

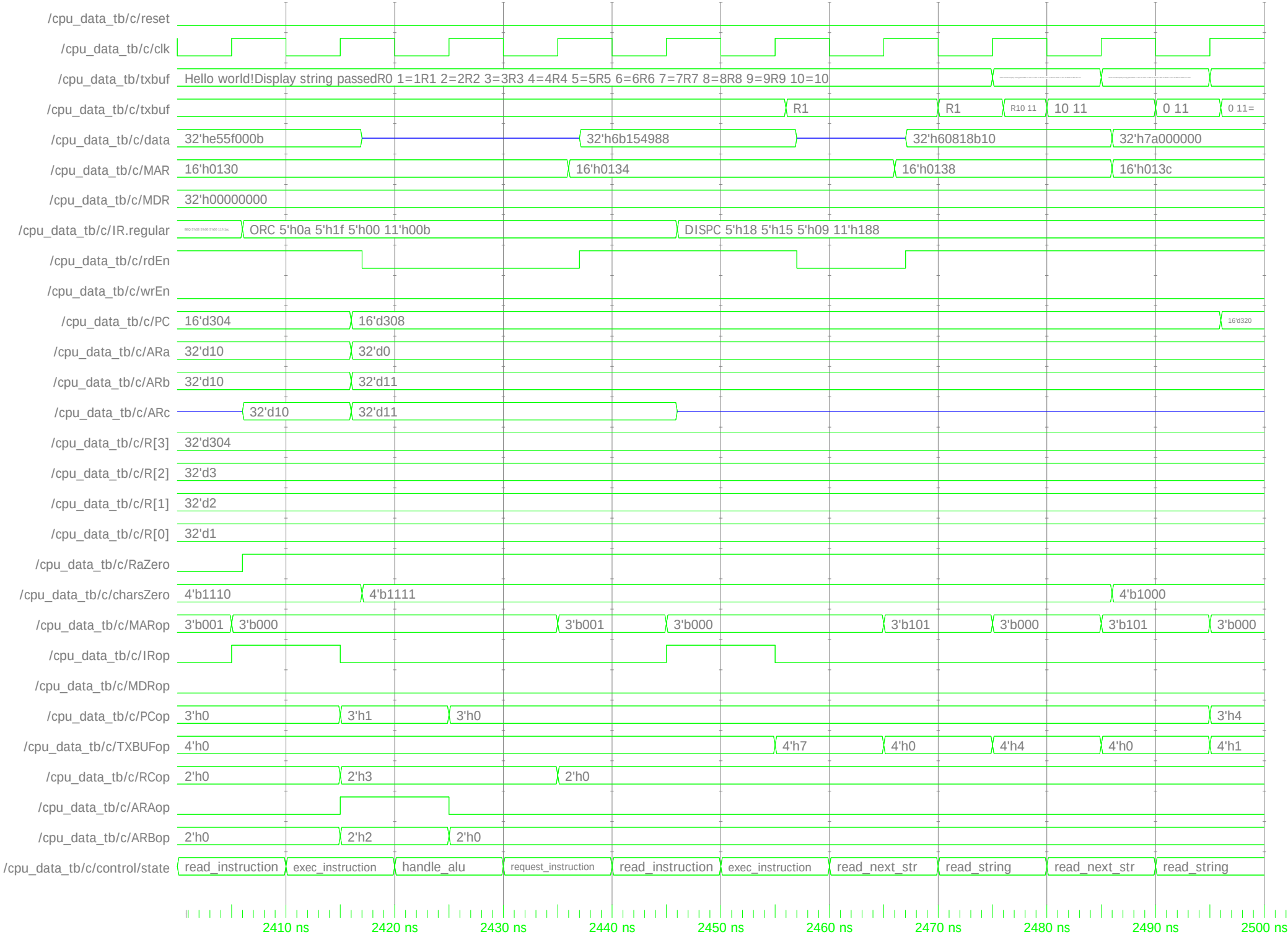


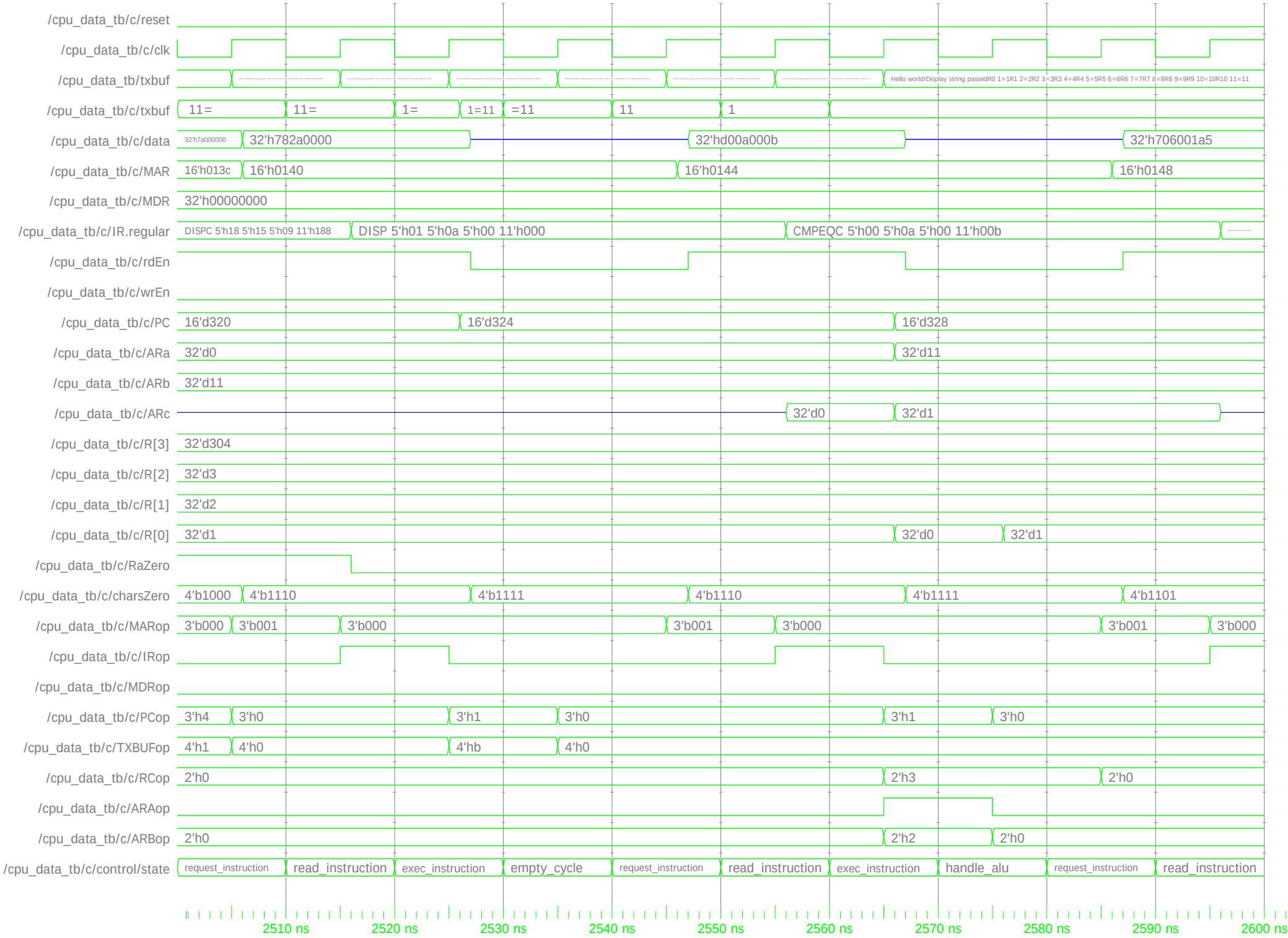
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 22 Page: 22



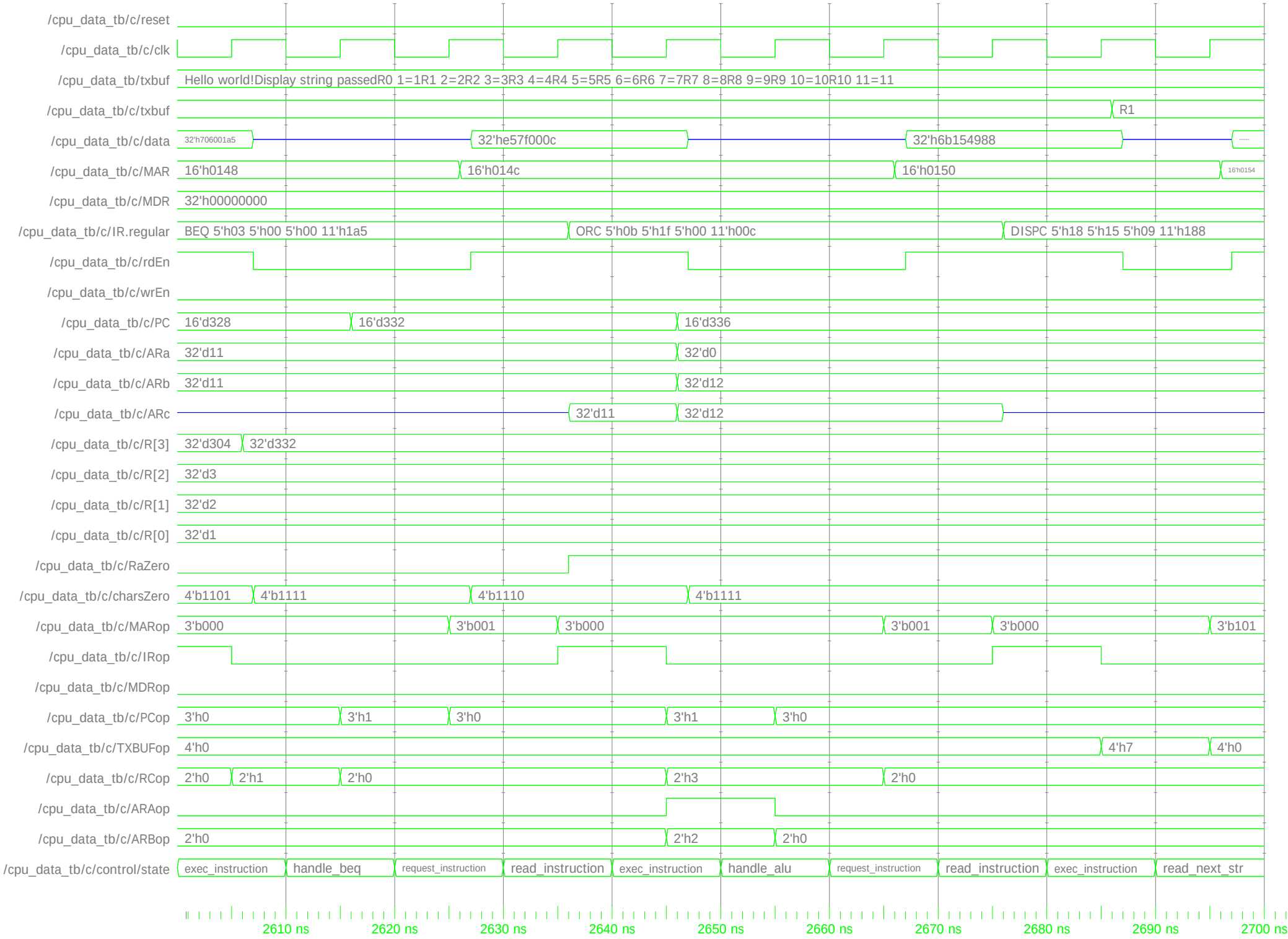
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 23 Page: 23

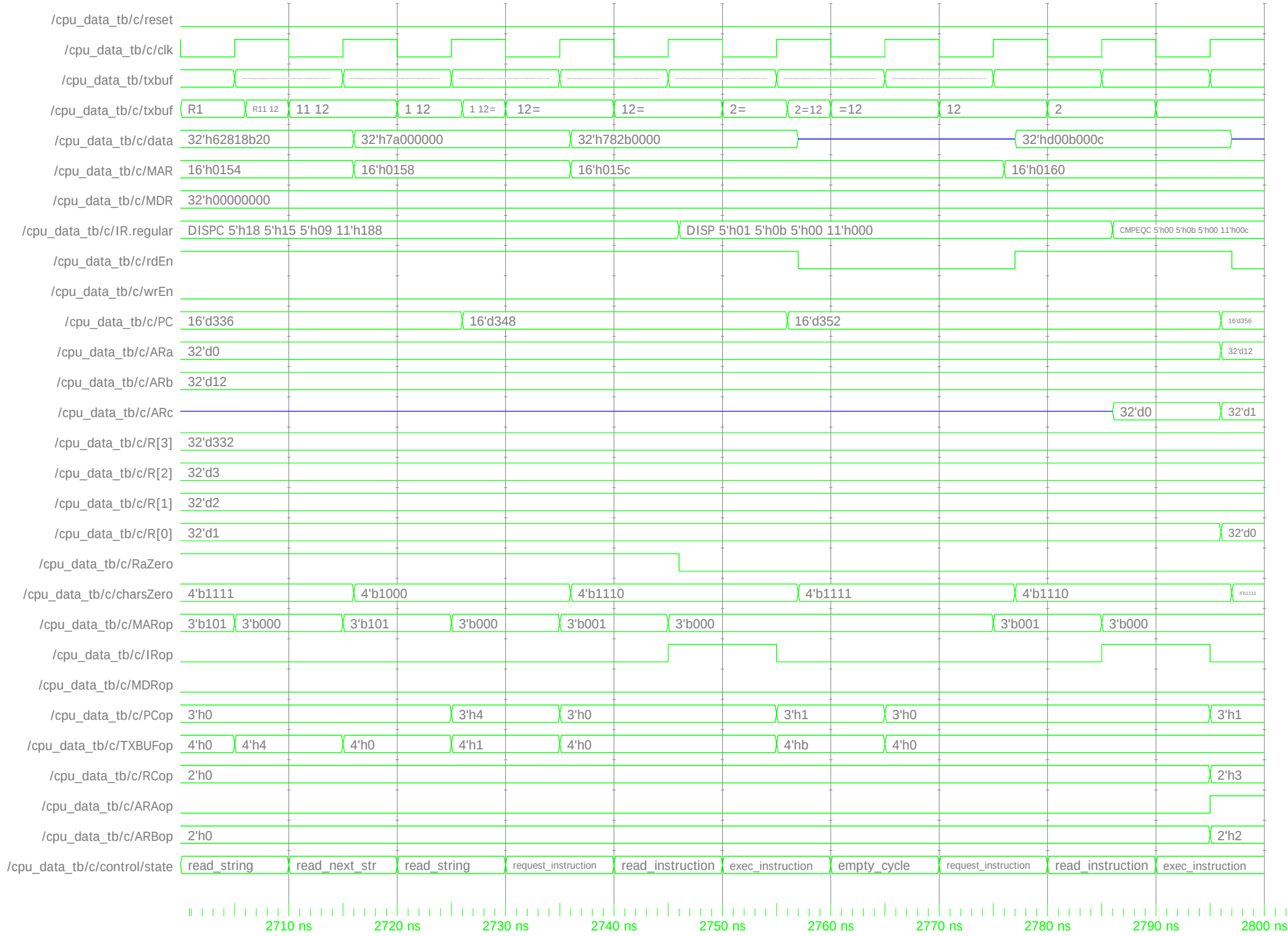

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10
/cpu_data_tb/c/txbuf
10
0
/cpu_data_tb/c/data
32'hd009000a
32'h706001ac
/cpu_data_tb/c/MAR
16'h0124
16'h0128
16'h012c
16'h0130
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h09 5'h00 11'h000
CMPEQC 5'h00 5'h09 5'h00 11'h00a
BEQ 5'h03 5'h00 5'h00 11'h1ac
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd296
16'd300
16'd304
/cpu_data_tb/c/ARa
32'd0
32'd10
/cpu_data_tb/c/ARb
32'd10
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd276
32'd304
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
2310 ns
2320 ns
2330 ns
2340 ns
2350 ns
2360 ns
2370 ns
2380 ns
2390 ns
2400 ns

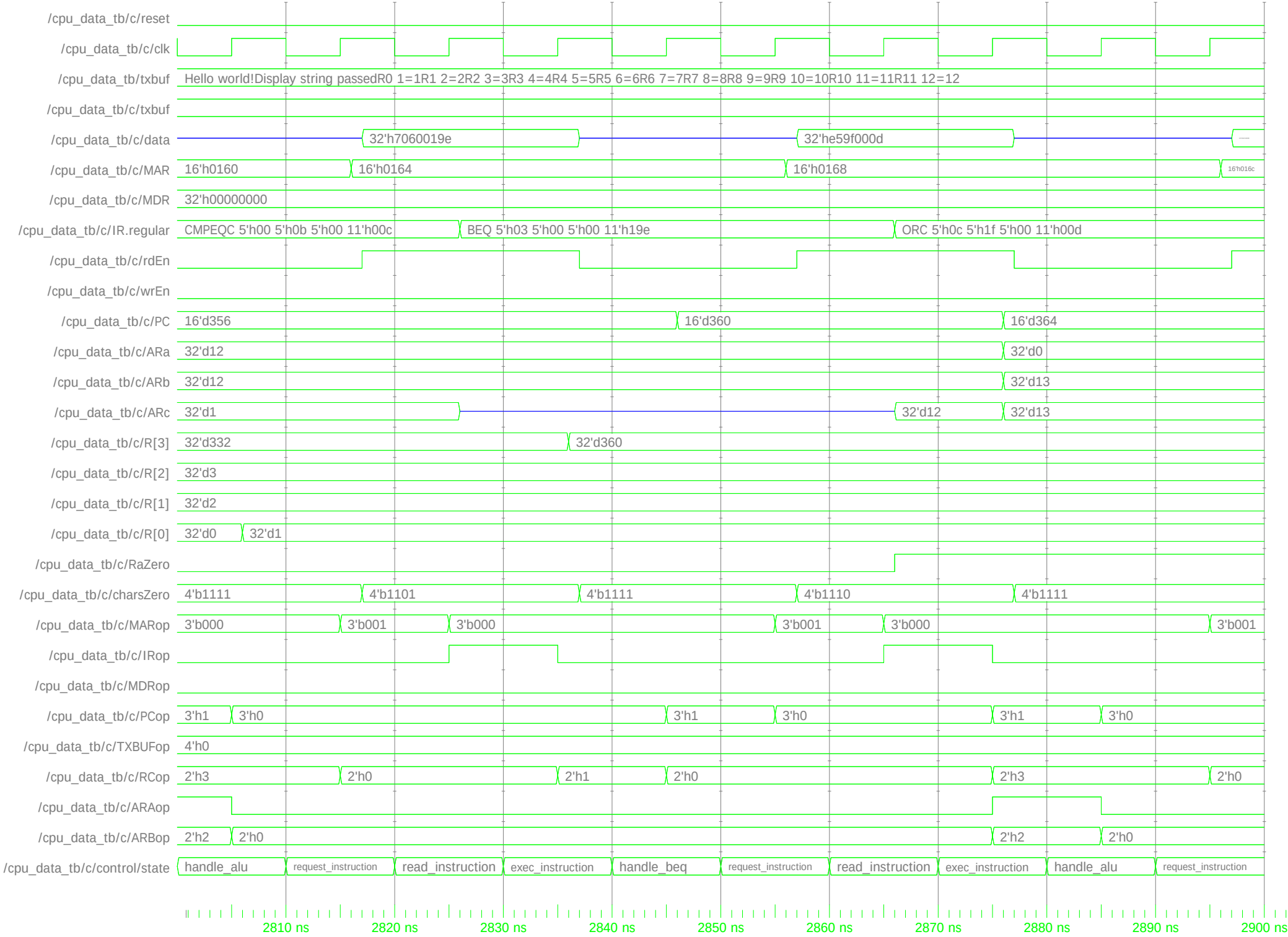

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10
/cpu_data_tb/c/txbuf
R1
R1
R10 11
10 11
0 11
0 11=
/cpu_data_tb/c/data
32'he55f000b
32'h6b154988
32'h60818b10
32'h7a000000
/cpu_data_tb/c/MAR
16'h0130
16'h0134
16'h0138
16'h013c
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
ORC 5'h0a 5'h1f 5'h00 11'h00b
DISPC 5'h18 5'h15 5'h09 11'h188
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd304
16'd308
16'd320
/cpu_data_tb/c/ARa
32'd10
32'd0
/cpu_data_tb/c/ARb
32'd10
32'd11
/cpu_data_tb/c/ARc
32'd10
32'd11
/cpu_data_tb/c/R[3]
32'd304
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1000
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
2410 ns
2420 ns
2430 ns
2440 ns
2450 ns
2460 ns
2470 ns
2480 ns
2490 ns
2500 ns

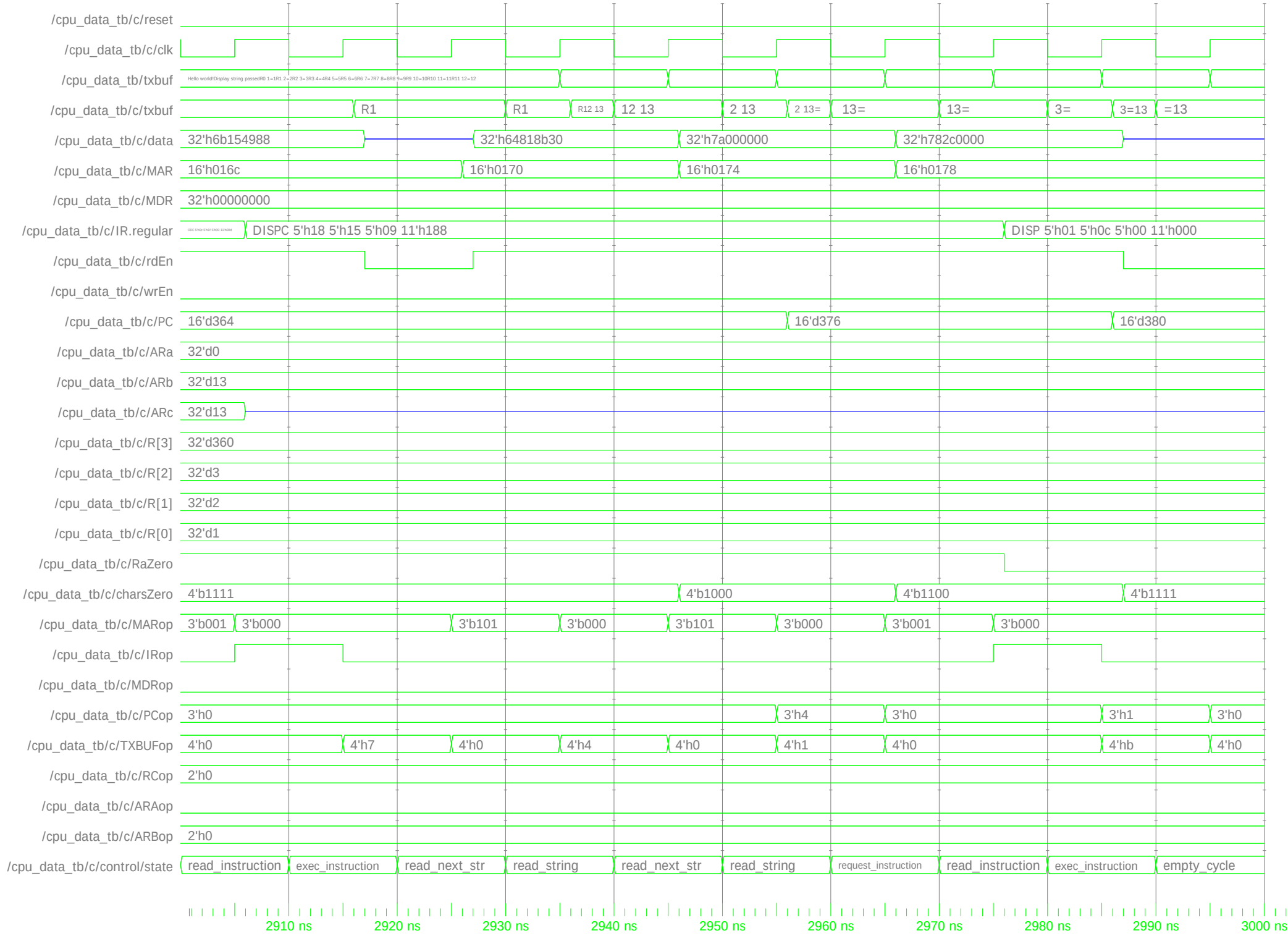


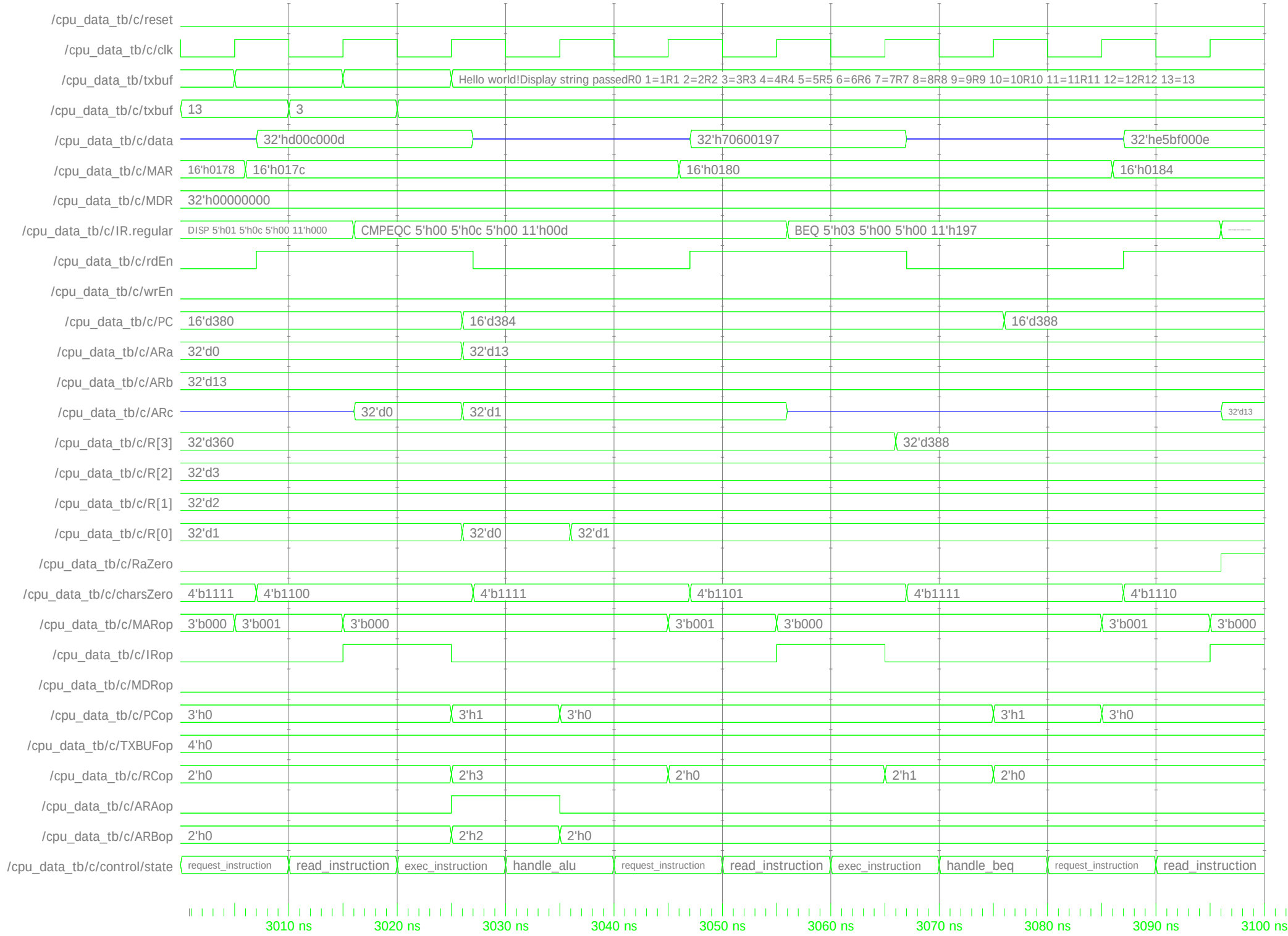
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 26 Page: 26


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11
/cpu_data_tb/c/txbuf
R1
/cpu_data_tb/c/data
32'h706001a5
32'he57f000c
32'h6b154988
/cpu_data_tb/c/MAR
16'h0148
16'h014c
16'h0150
16'h0154
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h00 5'h00 11'h1a5
ORC 5'h0b 5'h1f 5'h00 11'h00c
DISPC 5'h18 5'h15 5'h09 11'h188
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd328
16'd332
16'd336
/cpu_data_tb/c/ARa
32'd11
32'd0
/cpu_data_tb/c/ARb
32'd11
32'd12
/cpu_data_tb/c/ARc
32'd11
32'd12
/cpu_data_tb/c/R[3]
32'd304
32'd332
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b101
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h1
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
read_next_str
2610 ns
2620 ns
2630 ns
2640 ns
2650 ns
2660 ns
2670 ns
2680 ns
2690 ns
2700 ns

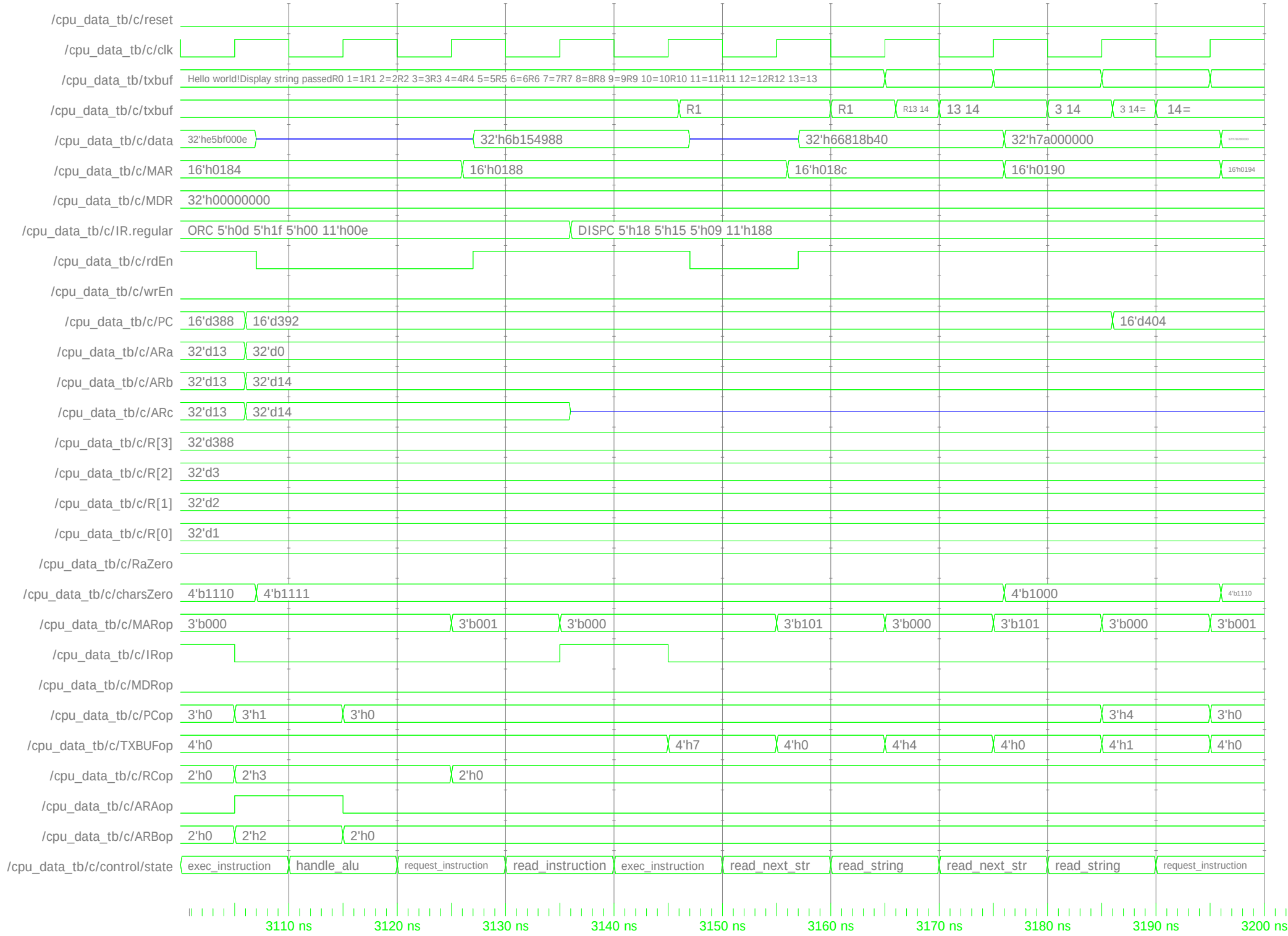

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
R1
R11 12
11 12
1 12
1 12=
12=
12=
2=
2=12
=12
12
2
/cpu_data_tb/c/data
32'h62818b20
32'h7a000000
32'h782b0000
32'hd00b000c
/cpu_data_tb/c/MAR
16'h0154
16'h0158
16'h015c
16'h0160
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h188
DISP 5'h01 5'h0b 5'h00 11'h000
CMPEQC 5'h00 5'h0b 5'h00 11'h00c
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd336
16'd348
16'd352
16'd356
/cpu_data_tb/c/ARa
32'd0
32'd12
/cpu_data_tb/c/ARb
32'd12
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd332
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1110
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'h4
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
/cpu_data_tb/c/control/state
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
2710 ns
2720 ns
2730 ns
2740 ns
2750 ns
2760 ns
2770 ns
2780 ns
2790 ns
2800 ns

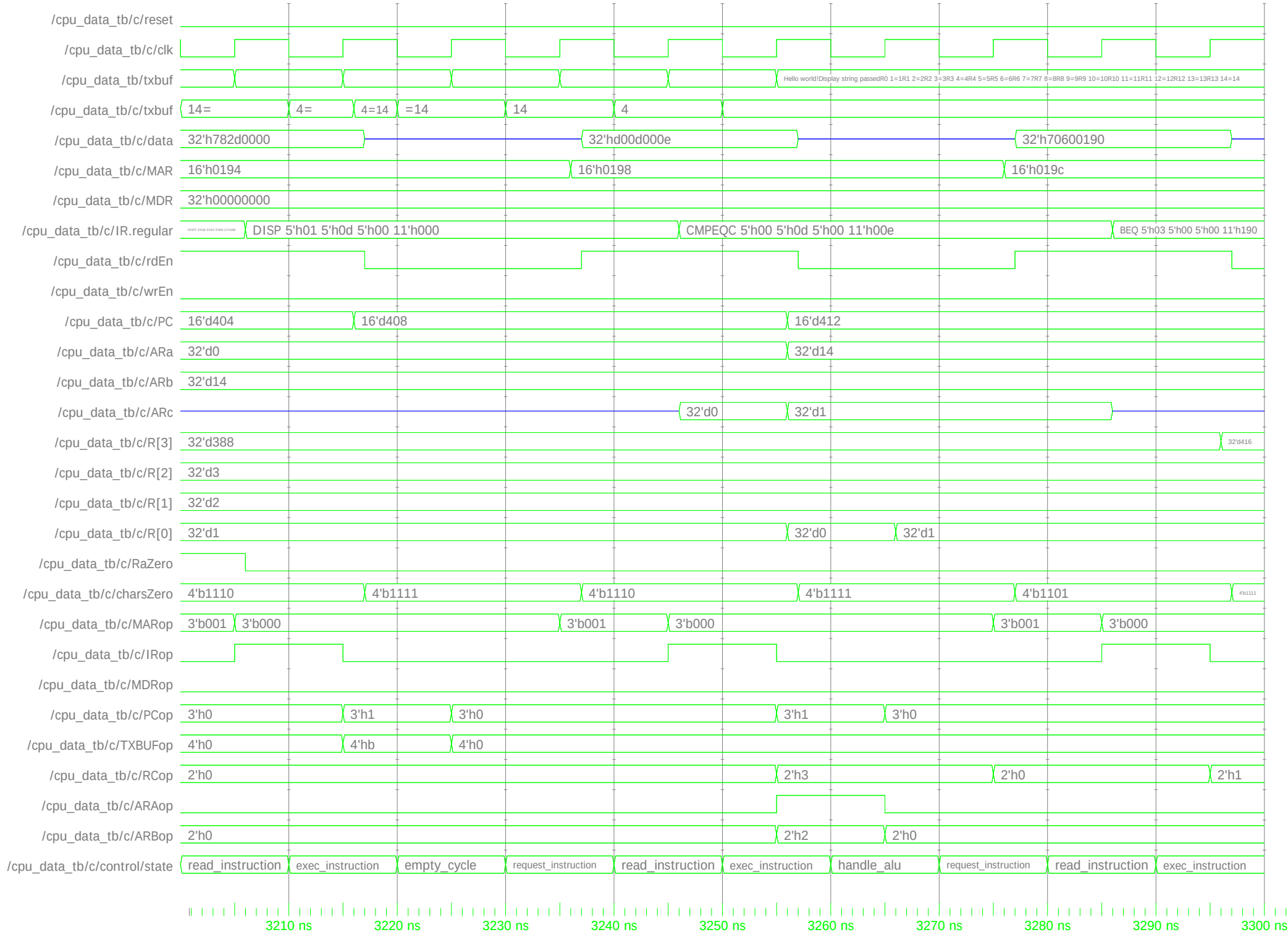

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h7060019e
32'he59f000d
/cpu_data_tb/c/MAR
16'h0160
16'h0164
16'h0168
16'h016c
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
CMPEQC 5'h00 5'h0b 5'h00 11'h00c
BEQ 5'h03 5'h00 5'h00 11'h19e
ORC 5'h0c 5'h1f 5'h00 11'h00d
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd356
16'd360
16'd364
/cpu_data_tb/c/ARa
32'd12
32'd0
/cpu_data_tb/c/ARb
32'd12
32'd13
/cpu_data_tb/c/ARc
32'd1
32'd12
32'd13
/cpu_data_tb/c/R[3]
32'd332
32'd360
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h3
2'h0
2'h1
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h2
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
2810 ns
2820 ns
2830 ns
2840 ns
2850 ns
2860 ns
2870 ns
2880 ns
2890 ns
2900 ns

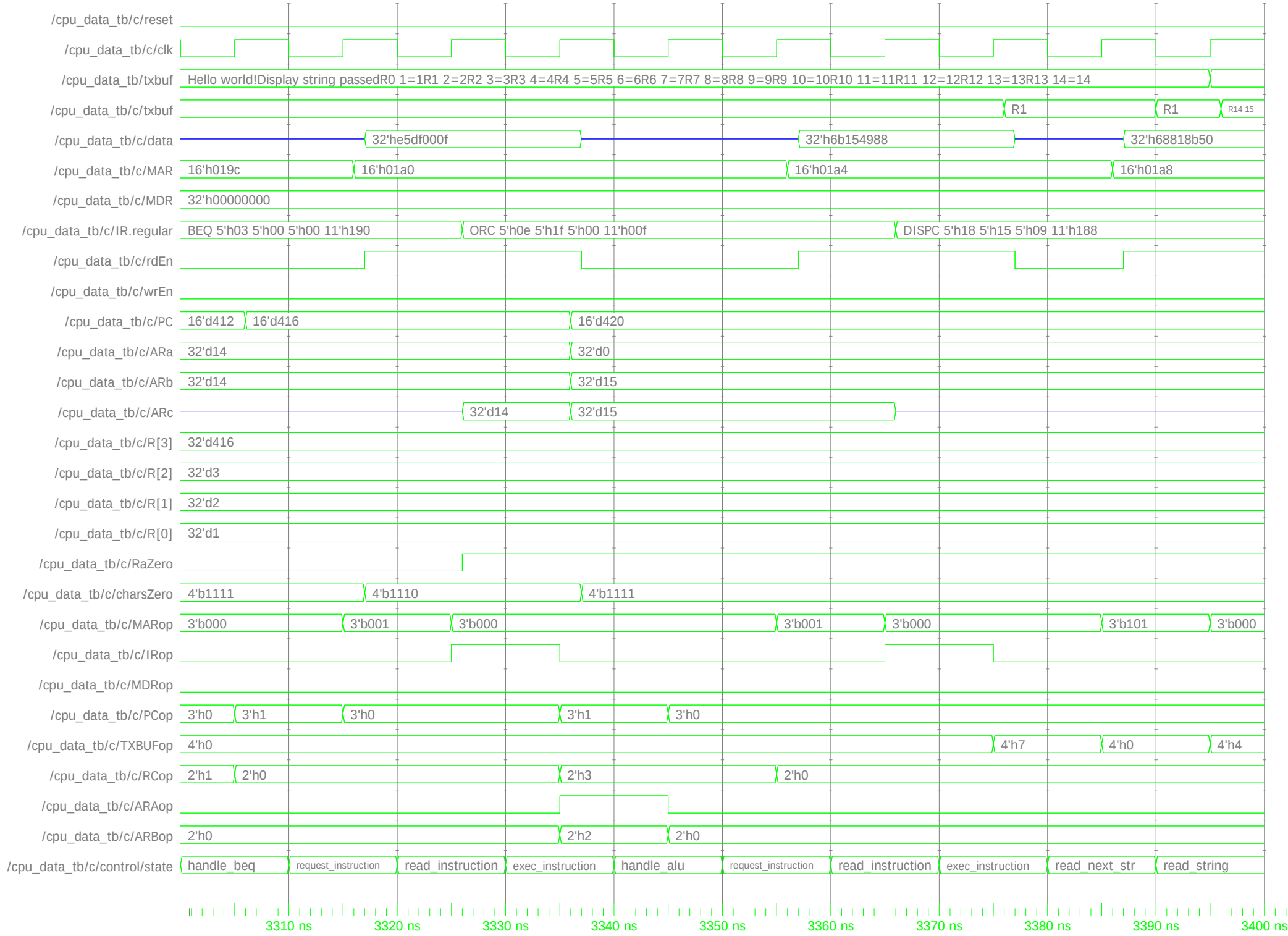

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12
/cpu_data_tb/c/txbuf
R1
R1
R12 13
12 13
2 13
2 13=
13=
13=
3=
3=13
=13
/cpu_data_tb/c/data
32'h6b154988
32'h64818b30
32'h7a000000
32'h782c0000
/cpu_data_tb/c/MAR
16'h016c
16'h0170
16'h0174
16'h0178
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h188
DISP 5'h01 5'h0c 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd364
16'd376
16'd380
/cpu_data_tb/c/ARa
32'd0
/cpu_data_tb/c/ARb
32'd13
/cpu_data_tb/c/ARc
32'd13
/cpu_data_tb/c/R[3]
32'd360
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1100
4'b1111
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
2910 ns
2920 ns
2930 ns
2940 ns
2950 ns
2960 ns
2970 ns
2980 ns
2990 ns
3000 ns



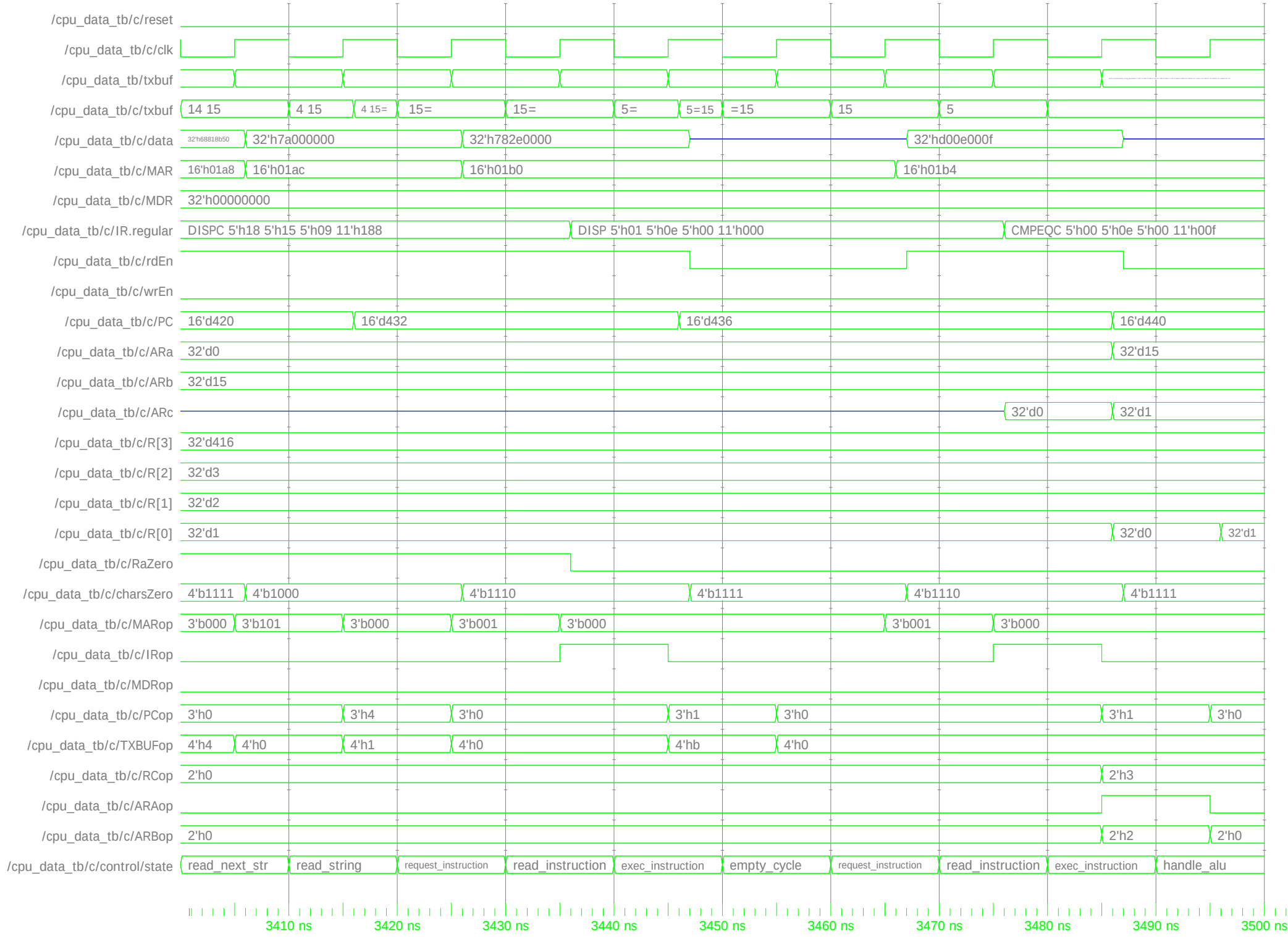
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 31 Page: 31


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13
/cpu_data_tb/c/txbuf
R1
R1
R13 14
13 14
3 14
3 14=
14=
/cpu_data_tb/c/data
32'he5bf000e
32'h6b154988
32'h66818b40
32'h7a000000
/cpu_data_tb/c/MAR
16'h0184
16'h0188
16'h018c
16'h0190
16'h0194
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
ORC 5'h0d 5'h1f 5'h00 11'h00e
DISPC 5'h18 5'h15 5'h09 11'h188
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd388
16'd392
16'd404
/cpu_data_tb/c/ARa
32'd13
32'd0
/cpu_data_tb/c/ARb
32'd13
32'd14
/cpu_data_tb/c/ARc
32'd13
32'd14
/cpu_data_tb/c/R[3]
32'd388
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1000
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
3110 ns
3120 ns
3130 ns
3140 ns
3150 ns
3160 ns
3170 ns
3180 ns
3190 ns
3200 ns

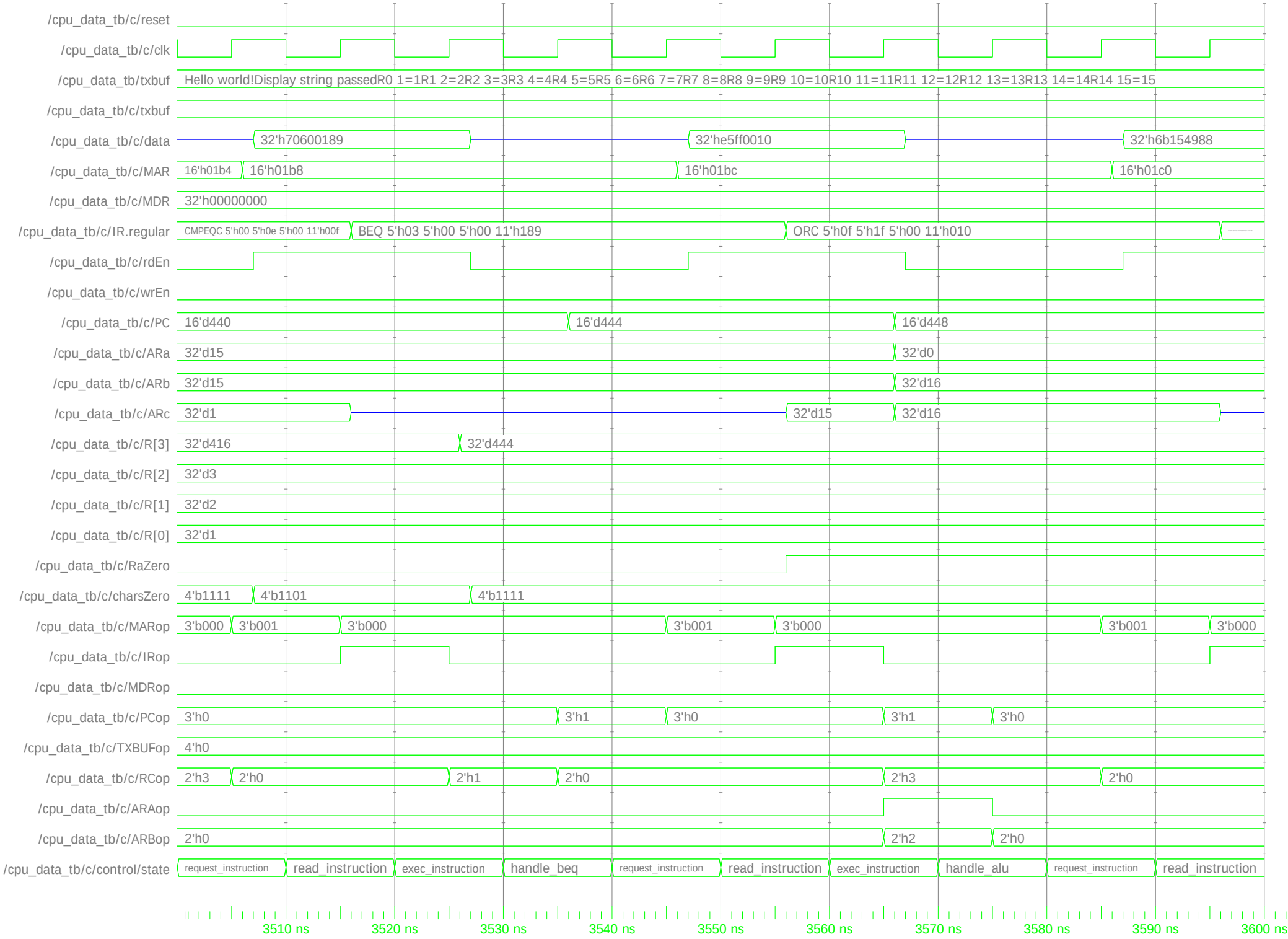

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14
/cpu_data_tb/c/txbuf
14= 4= 4=14 =14 14 4
/cpu_data_tb/c/data
32'h782d0000 32'hd00d000e 32'h70600190
/cpu_data_tb/c/MAR
16'h0194 16'h0198 16'h019c
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h0d 5'h00 11'h000 CMPEQC 5'h00 5'h0d 5'h00 11'h00e BEQ 5'h03 5'h00 5'h00 11'h190
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd404 16'd408 16'd412
/cpu_data_tb/c/ARa
32'd0 32'd14
/cpu_data_tb/c/ARb
32'd14
/cpu_data_tb/c/ARc
32'd0 32'd1
/cpu_data_tb/c/R[3]
32'd388 32'd416
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1 32'd0 32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110 4'b1111 4'b1110 4'b1111 4'b1101 4'b1111
/cpu_data_tb/c/MARop
3'b001 3'b000 3'b001 3'b000 3'b001 3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0 3'h1 3'h0 3'h1 3'h0
/cpu_data_tb/c/TXBUFop
4'h0 4'hb 4'h0
/cpu_data_tb/c/RCop
2'h0 2'h3 2'h0 2'h1
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0 2'h2 2'h0
/cpu_data_tb/c/control/state
read_instruction exec_instruction empty_cycle request_instruction read_instruction exec_instruction handle_alu request_instruction read_instruction exec_instruction
3210 ns 3220 ns 3230 ns 3240 ns 3250 ns 3260 ns 3270 ns 3280 ns 3290 ns 3300 ns



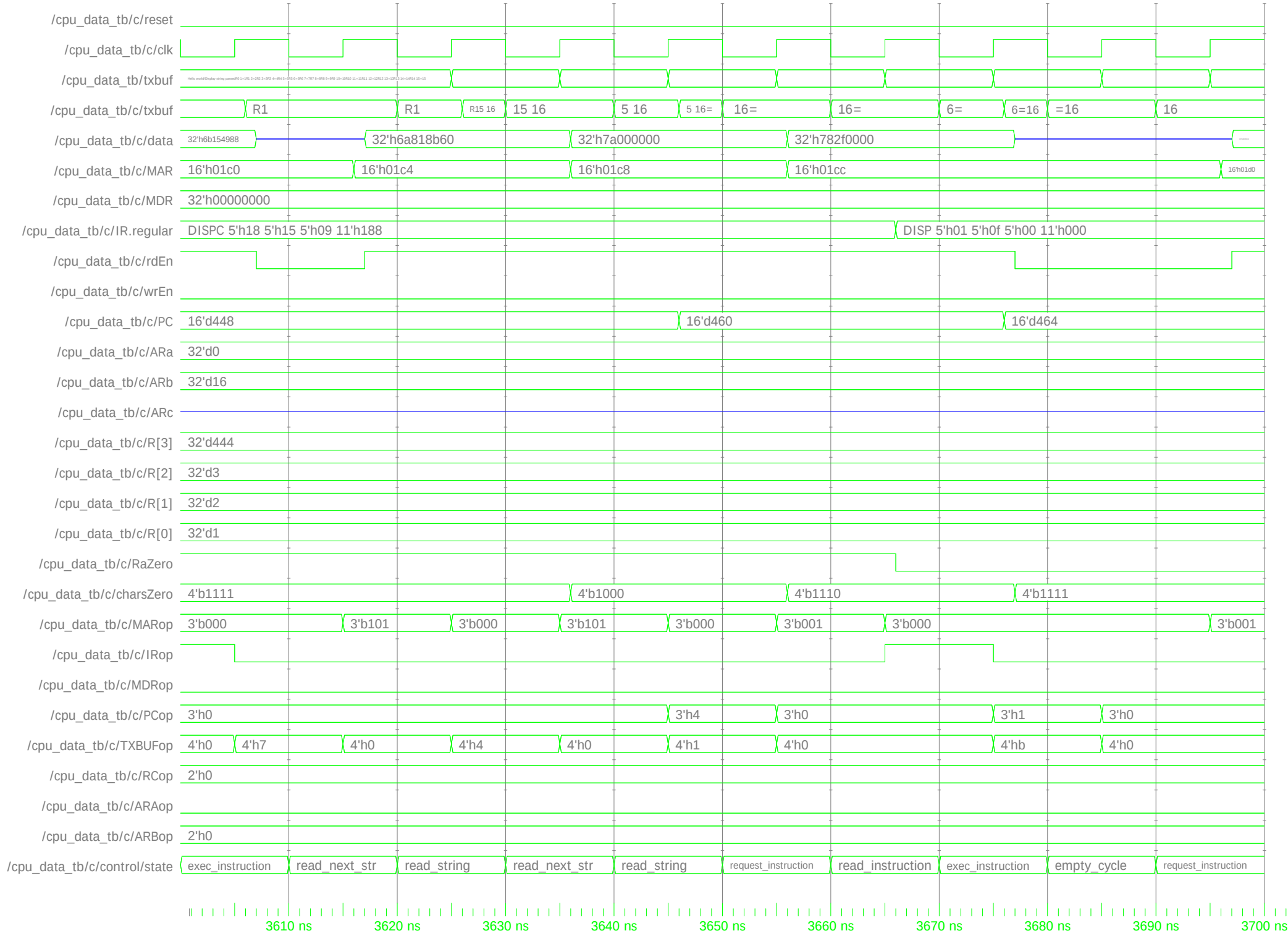
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 34 Page: 34

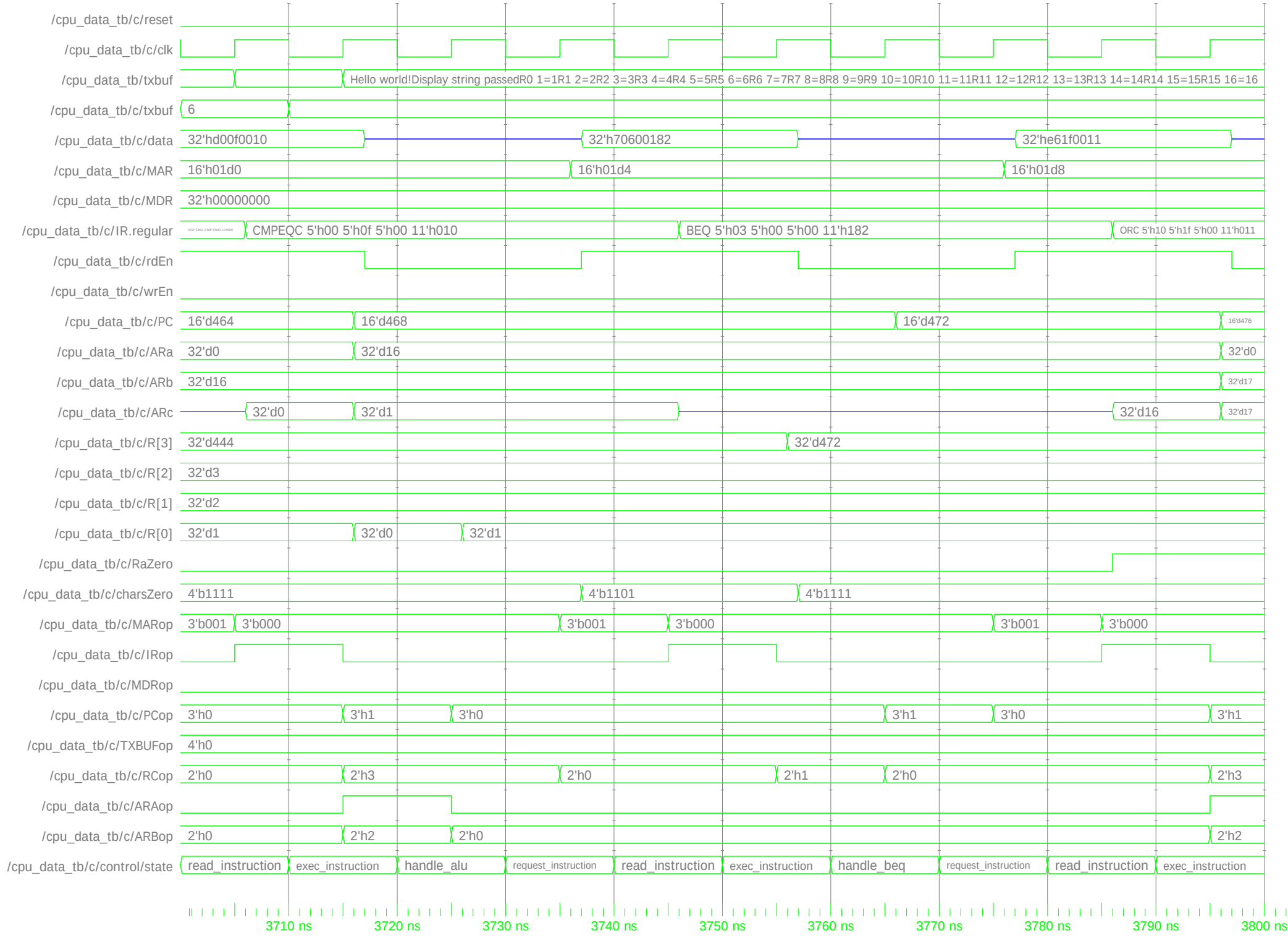


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 35 Page: 35

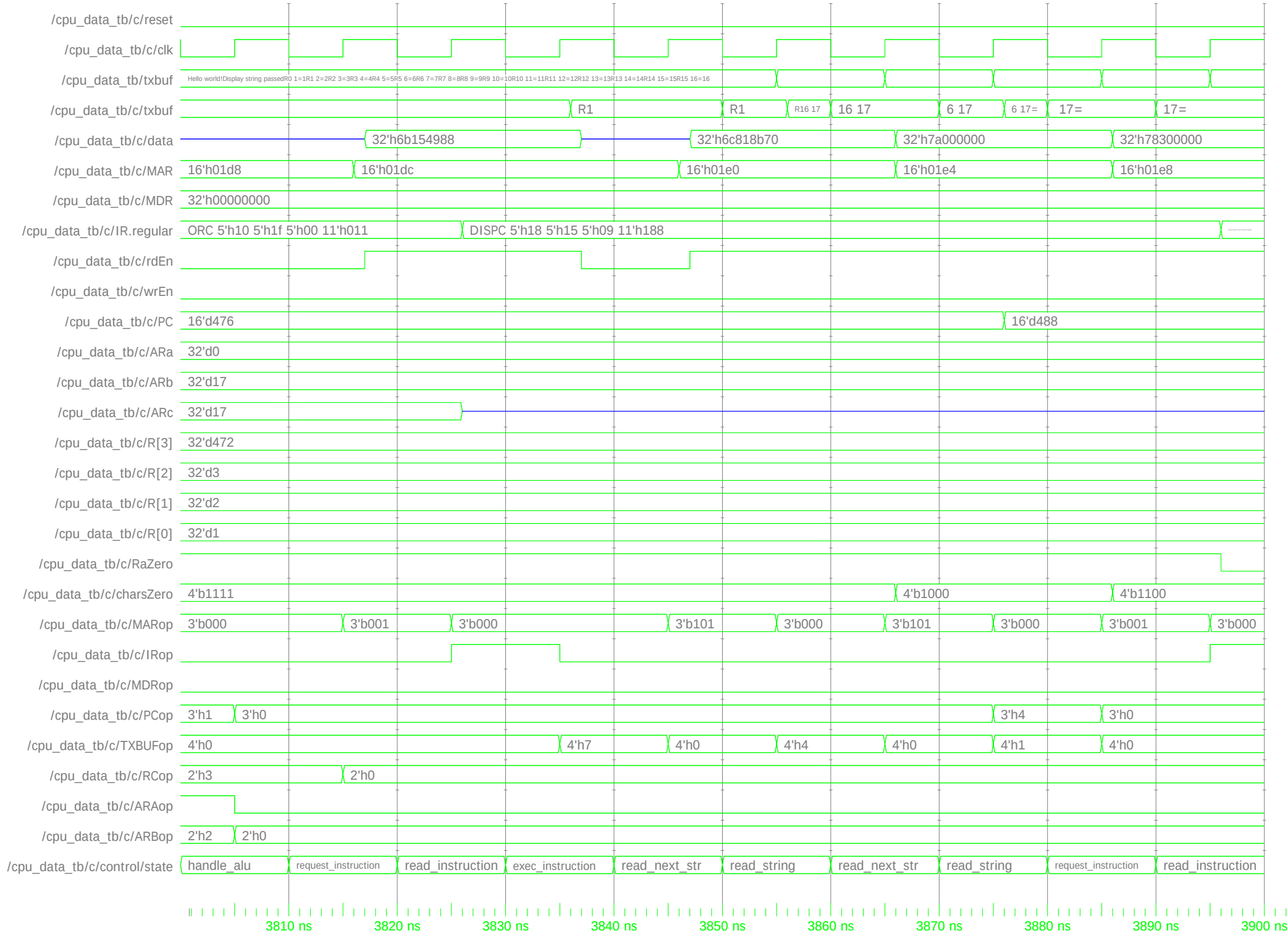


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 36 Page: 36

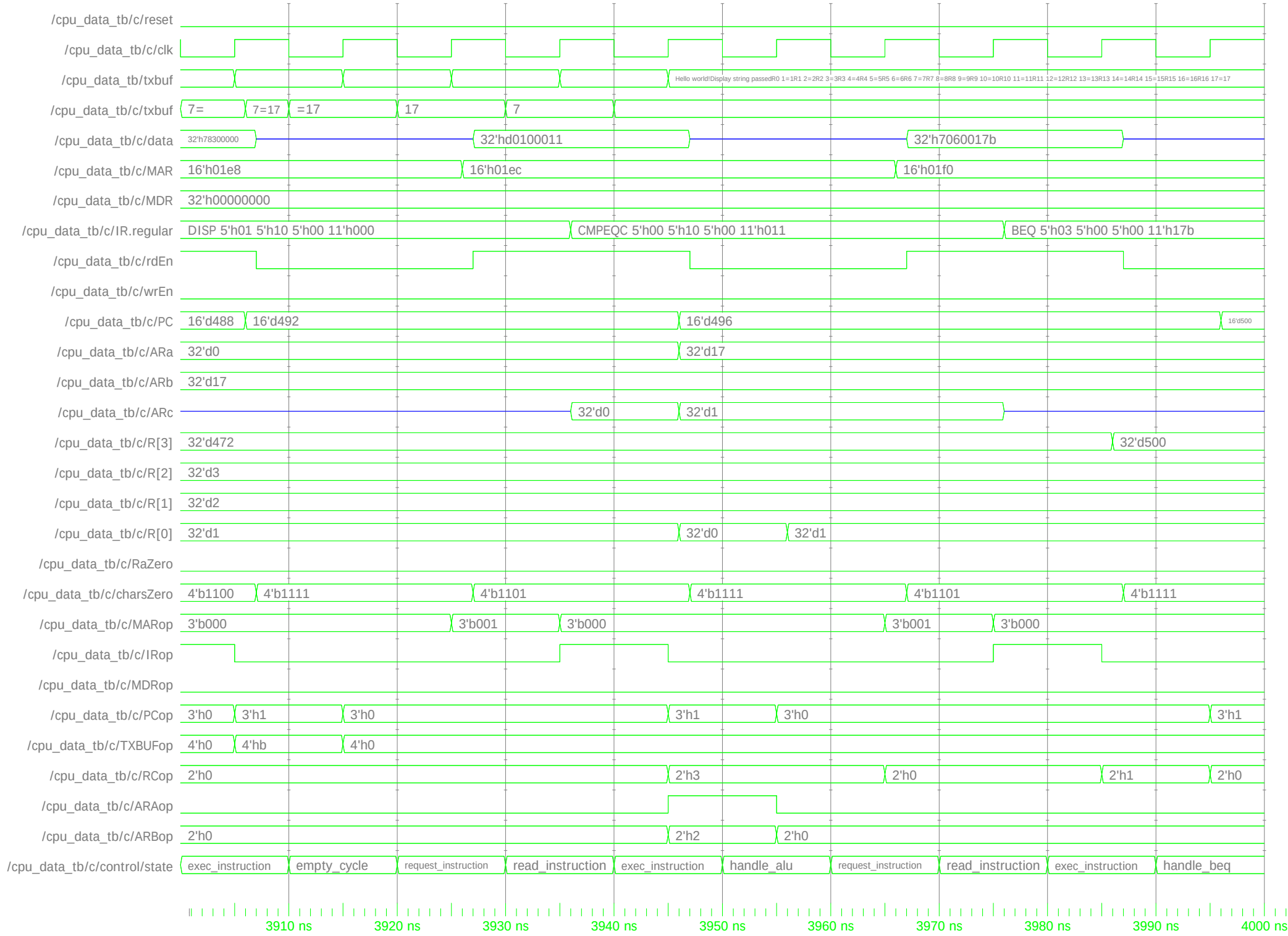

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
R1
R1
R15 16
15 16
5 16
5 16=
16=
16=
6=
6=16
=16
16
/cpu_data_tb/c/data
32'h6b154988
32'h6a818b60
32'h7a000000
32'h782f0000
/cpu_data_tb/c/MAR
16'h01c0
16'h01c4
16'h01c8
16'h01cc
16'h01d0
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h188
DISP 5'h01 5'h0f 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd448
16'd460
16'd464
/cpu_data_tb/c/ARa
32'd0
/cpu_data_tb/c/ARb
32'd16
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd444
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
3610 ns
3620 ns
3630 ns
3640 ns
3650 ns
3660 ns
3670 ns
3680 ns
3690 ns
3700 ns

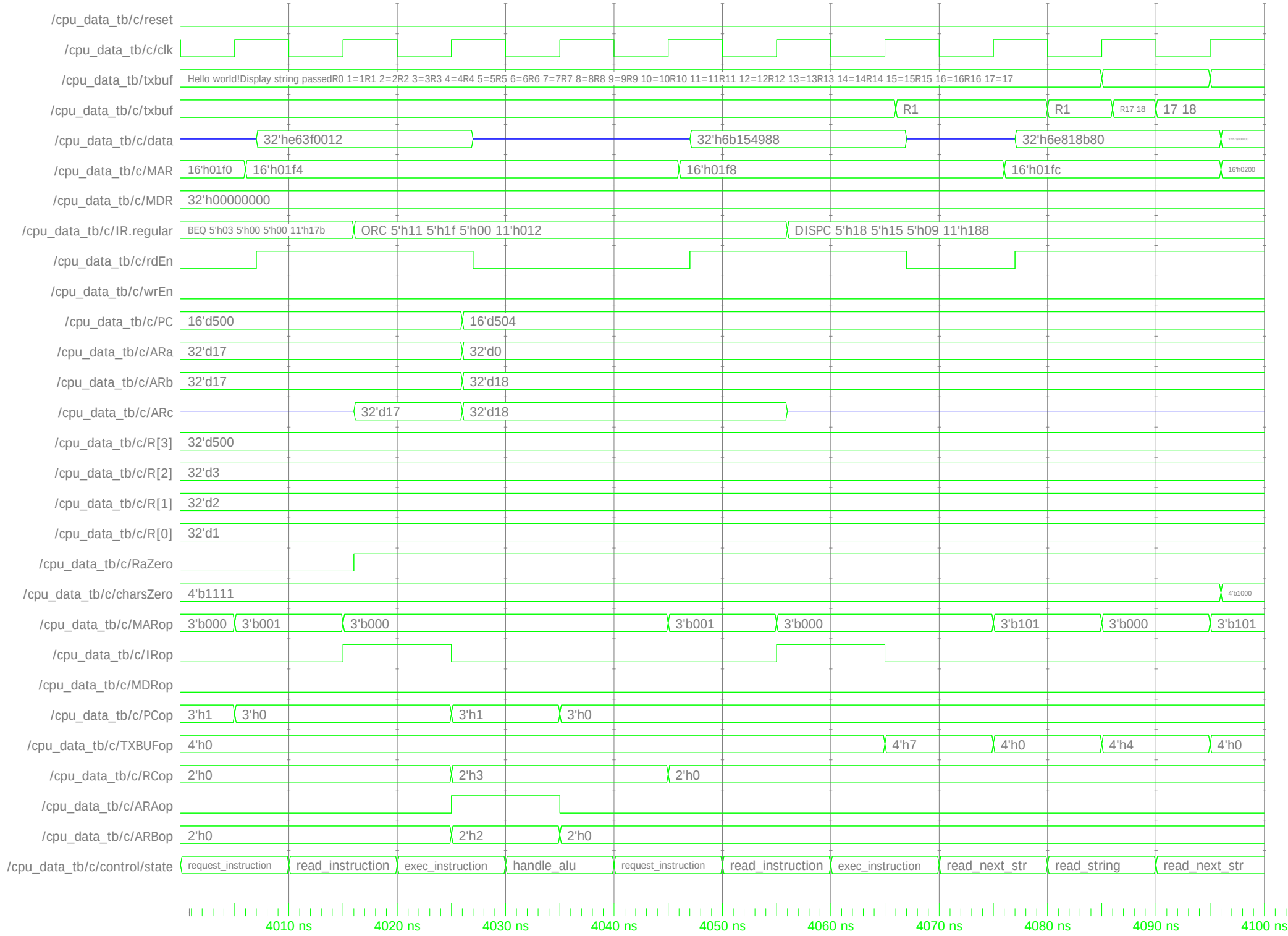


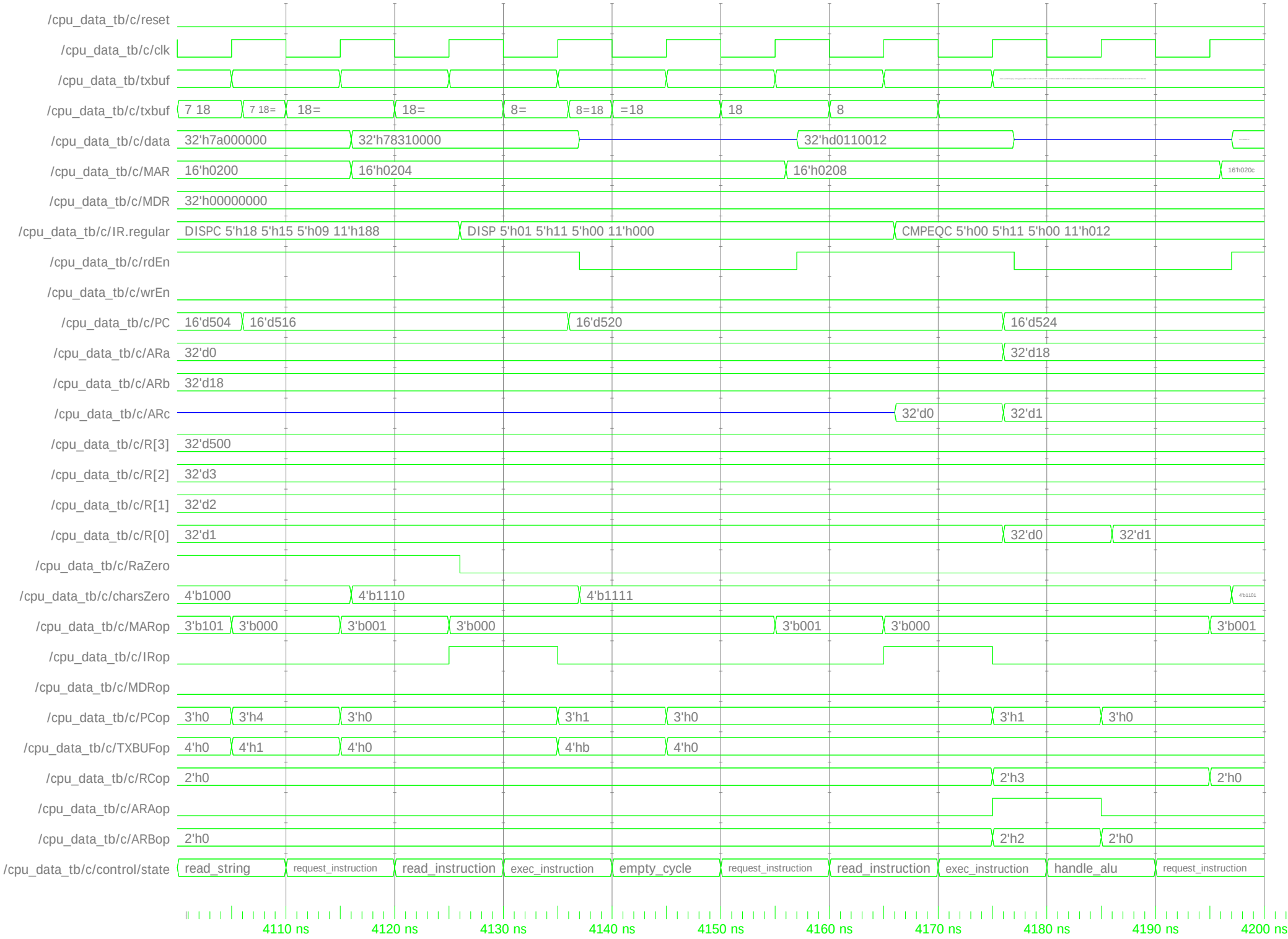
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 38 Page: 38

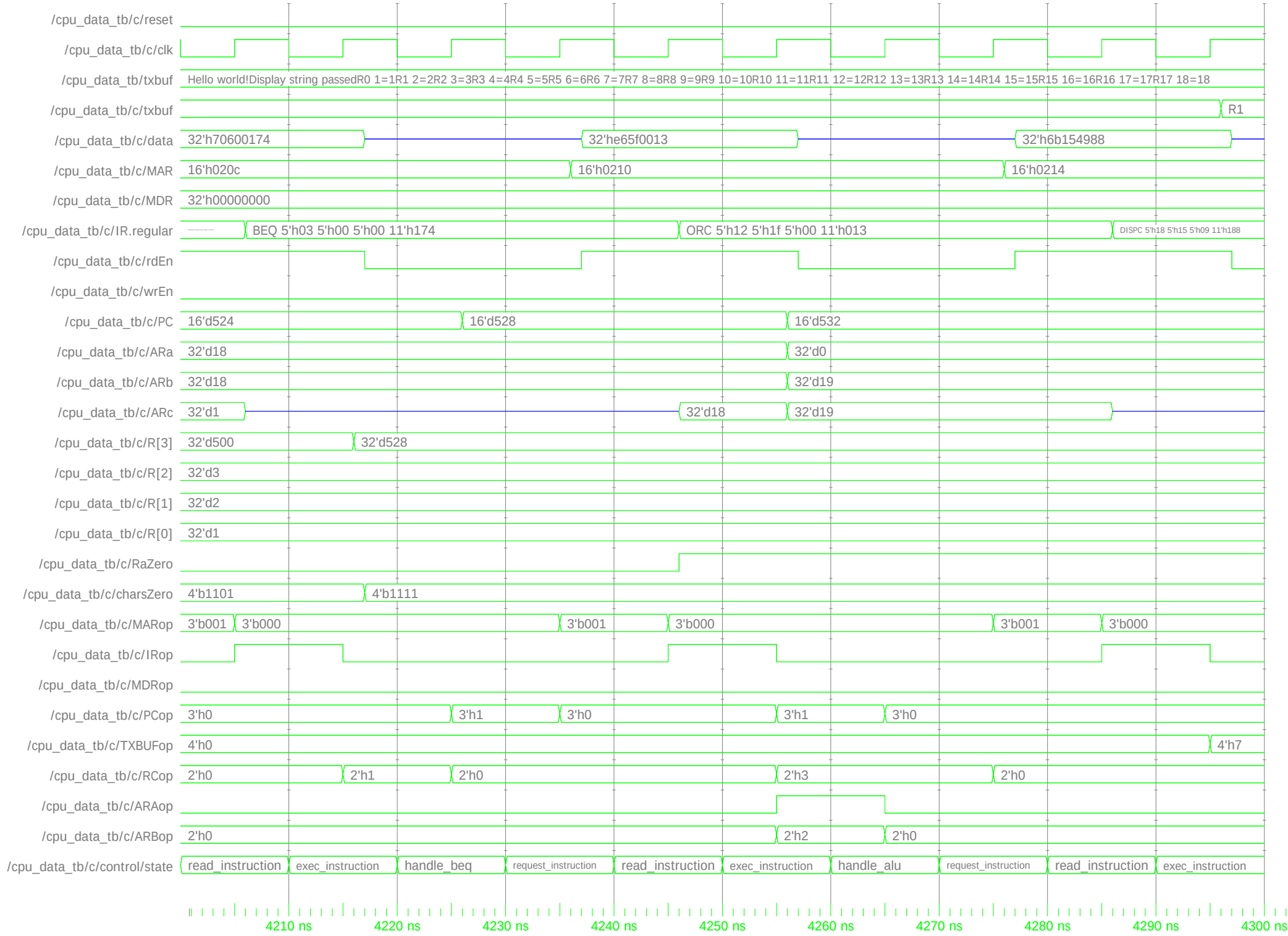


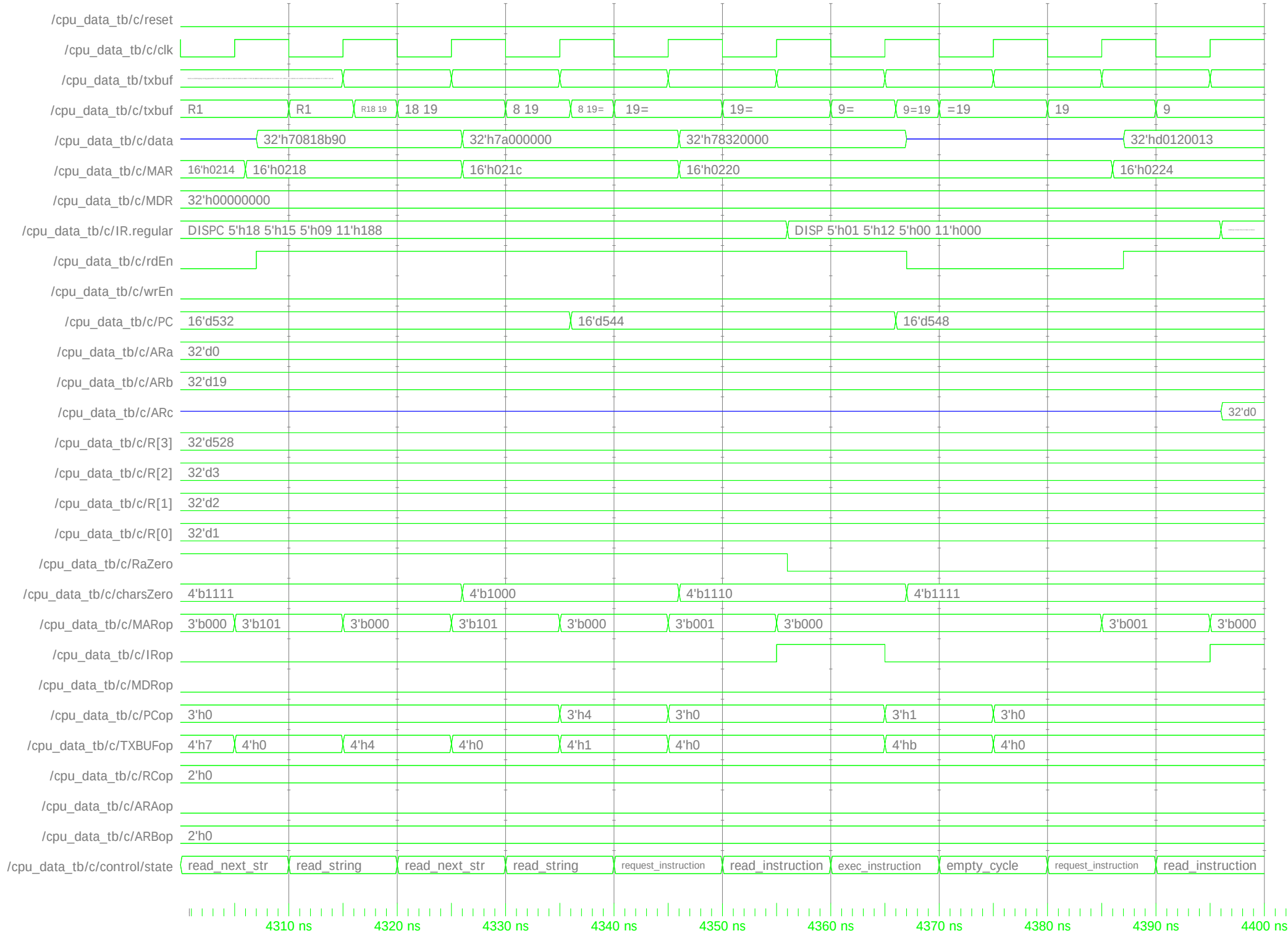
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 39 Page: 39


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17
/cpu_data_tb/c/txbuf
7=
7=17
=17
17
7
/cpu_data_tb/c/data
32'h78300000
32'hd0100011
32'h7060017b
/cpu_data_tb/c/MAR
16'h01e8
16'h01ec
16'h01f0
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h10 5'h00 11'h000
CMPEQC 5'h00 5'h10 5'h00 11'h011
BEQ 5'h03 5'h00 5'h00 11'h17b
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd488
16'd492
16'd496
16'd500
/cpu_data_tb/c/ARa
32'd0
32'd17
/cpu_data_tb/c/ARb
32'd17
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd472
32'd500
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1100
4'b1111
4'b1101
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
3910 ns
3920 ns
3930 ns
3940 ns
3950 ns
3960 ns
3970 ns
3980 ns
3990 ns
4000 ns

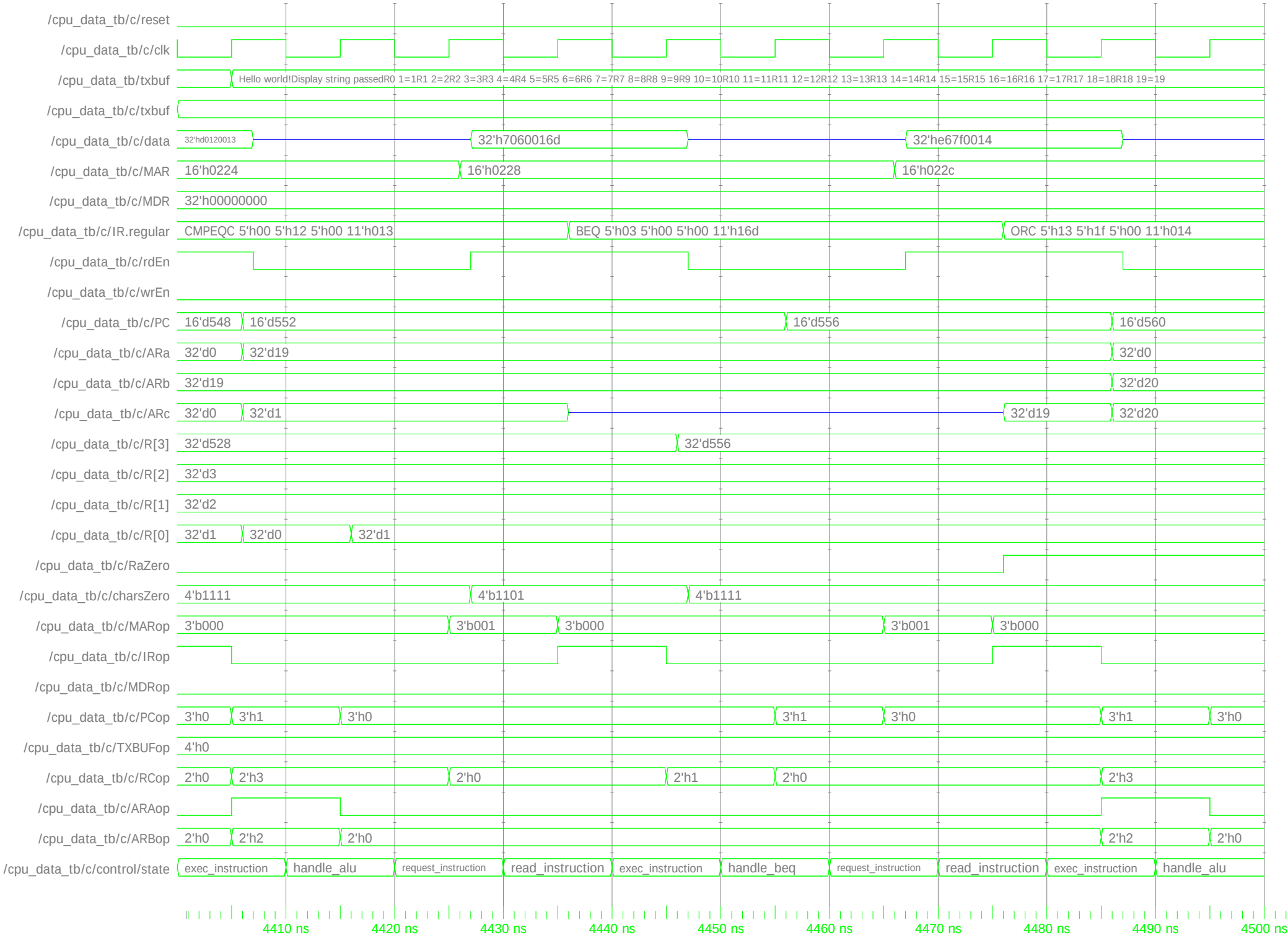

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17
/cpu_data_tb/c/txbuf
R1
R1
R17 18
17 18
/cpu_data_tb/c/data
32'he63f0012
32'h6b154988
32'h6e818b80
/cpu_data_tb/c/MAR
16'h01f0
16'h01f4
16'h01f8
16'h01fc
16'h0200
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h00 5'h00 11'h17b
ORC 5'h11 5'h1f 5'h00 11'h012
DISPC 5'h18 5'h15 5'h09 11'h188
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd500
16'd504
/cpu_data_tb/c/ARa
32'd17
32'd0
/cpu_data_tb/c/ARb
32'd17
32'd18
/cpu_data_tb/c/ARc
32'd17
32'd18
/cpu_data_tb/c/R[3]
32'd500
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
4010 ns
4020 ns
4030 ns
4040 ns
4050 ns
4060 ns
4070 ns
4080 ns
4090 ns
4100 ns

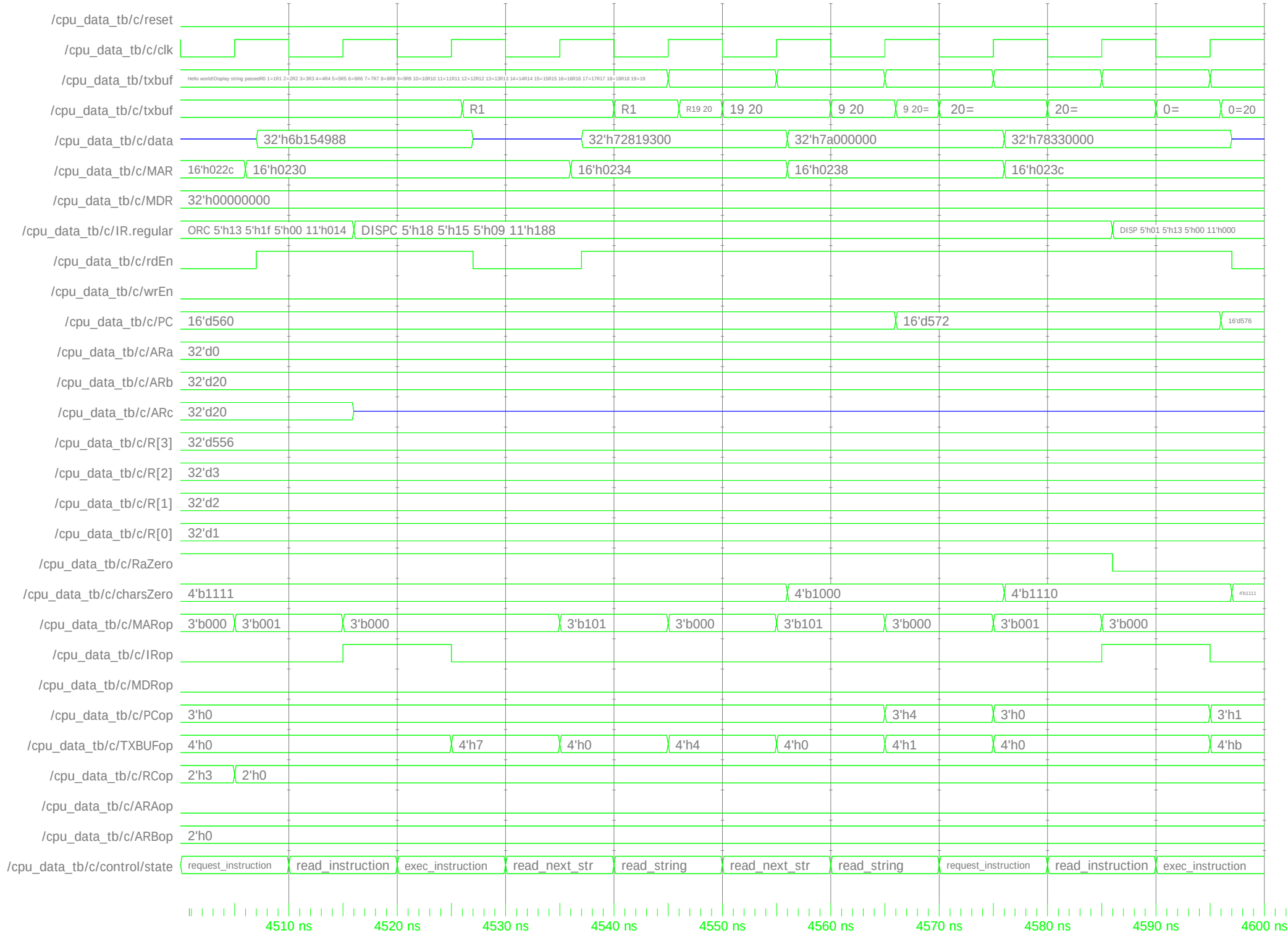

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
7 18
7 18=
18=
18=
8=
8=18
=18
18
8
/cpu_data_tb/c/data
32'h7a000000
32'h78310000
32'hd0110012
/cpu_data_tb/c/MAR
16'h0200
16'h0204
16'h0208
16'h020c
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h188
DISP 5'h01 5'h11 5'h00 11'h000
CMPEQC 5'h00 5'h11 5'h00 11'h012
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd504
16'd516
16'd520
16'd524
/cpu_data_tb/c/ARa
32'd0
32'd18
/cpu_data_tb/c/ARb
32'd18
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd500
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1000
4'b1110
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
4110 ns
4120 ns
4130 ns
4140 ns
4150 ns
4160 ns
4170 ns
4180 ns
4190 ns
4200 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17R17 18=18
/cpu_data_tb/c/txbuf
R1
/cpu_data_tb/c/data
32'h70600174
32'he65f0013
32'h6b154988
/cpu_data_tb/c/MAR
16'h020c
16'h0210
16'h0214
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h00 5'h00 11'h174
ORC 5'h12 5'h1f 5'h00 11'h013
DISPC 5'h18 5'h15 5'h09 11'h188
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd524
16'd528
16'd532
/cpu_data_tb/c/ARa
32'd18
32'd0
/cpu_data_tb/c/ARb
32'd18
32'd19
/cpu_data_tb/c/ARc
32'd1
32'd18
32'd19
/cpu_data_tb/c/R[3]
32'd500
32'd528
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
/cpu_data_tb/c/RCop
2'h0
2'h1
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
4210 ns
4220 ns
4230 ns
4240 ns
4250 ns
4260 ns
4270 ns
4280 ns
4290 ns
4300 ns

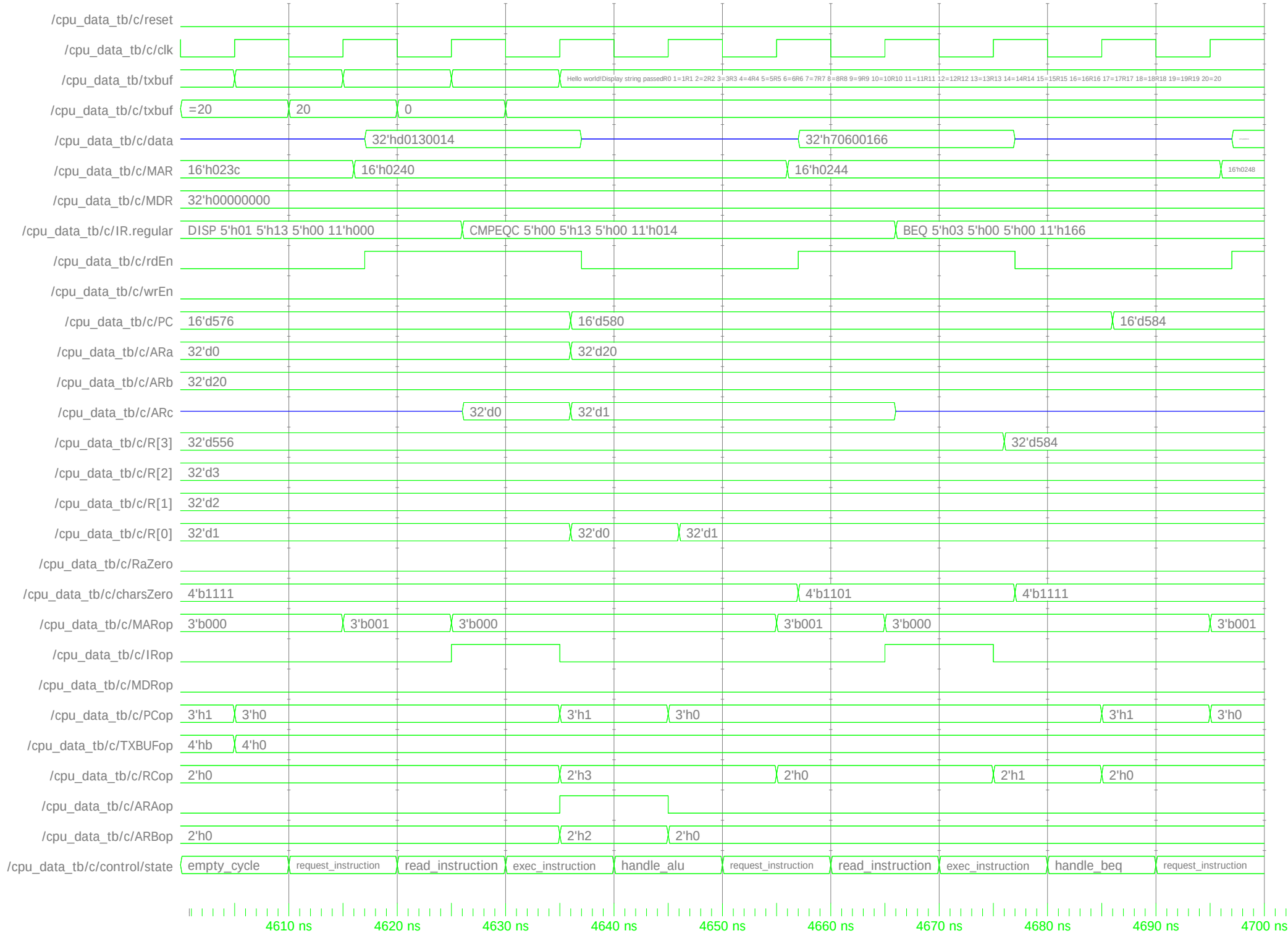


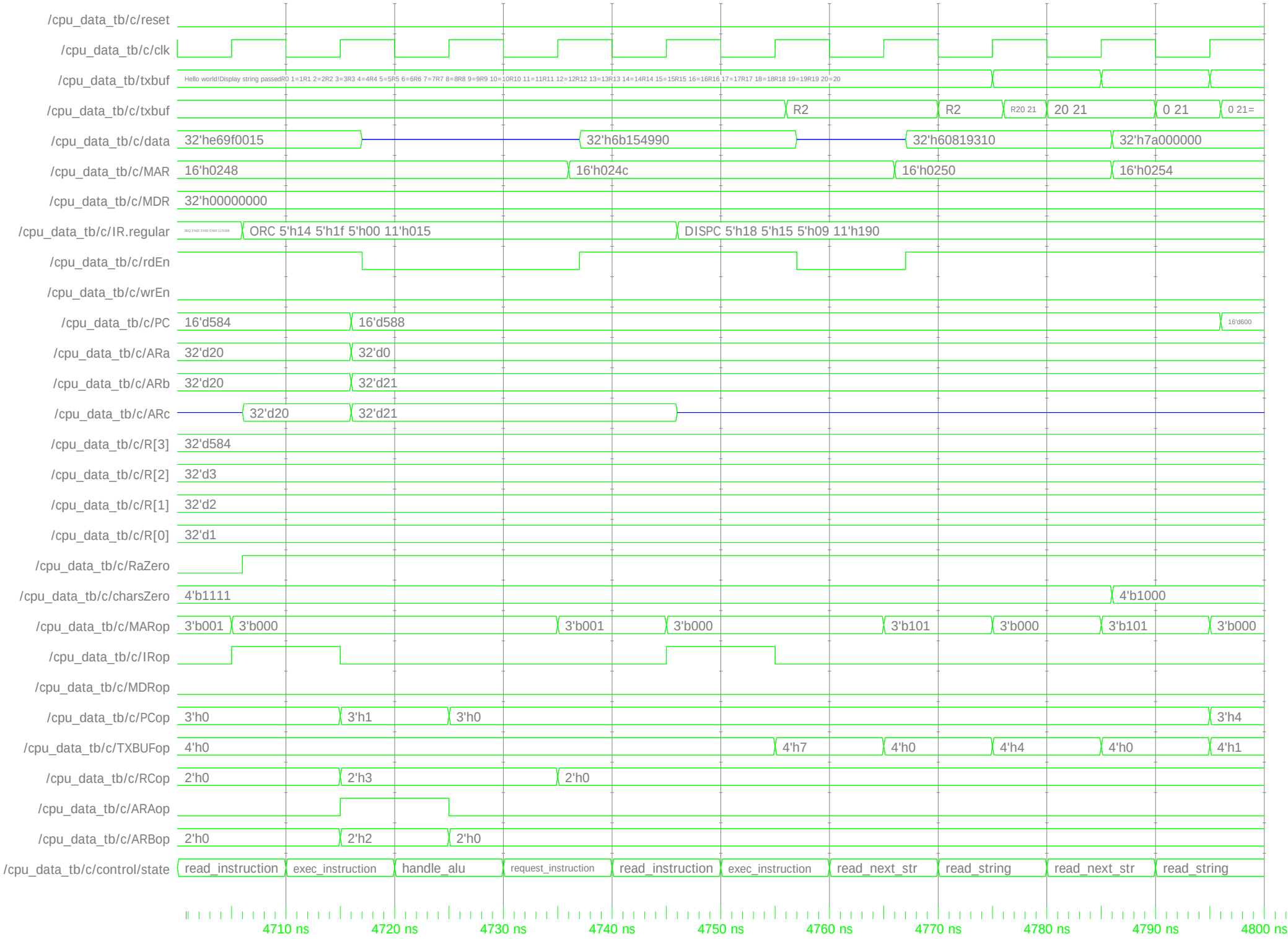
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 44 Page: 44


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17R17 18=18R18 19=19
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'hd0120013
32'h7060016d
32'he67f0014
/cpu_data_tb/c/MAR
16'h0224
16'h0228
16'h022c
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
CMPEQC 5'h00 5'h12 5'h00 11'h013
BEQ 5'h03 5'h00 5'h00 11'h16d
ORC 5'h13 5'h1f 5'h00 11'h014
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd548
16'd552
16'd556
16'd560
/cpu_data_tb/c/ARa
32'd0
32'd19
32'd0
/cpu_data_tb/c/ARb
32'd19
32'd20
/cpu_data_tb/c/ARc
32'd0
32'd1
32'd19
32'd20
/cpu_data_tb/c/R[3]
32'd528
32'd556
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
handle_alu
4410 ns
4420 ns
4430 ns
4440 ns
4450 ns
4460 ns
4470 ns
4480 ns
4490 ns
4500 ns

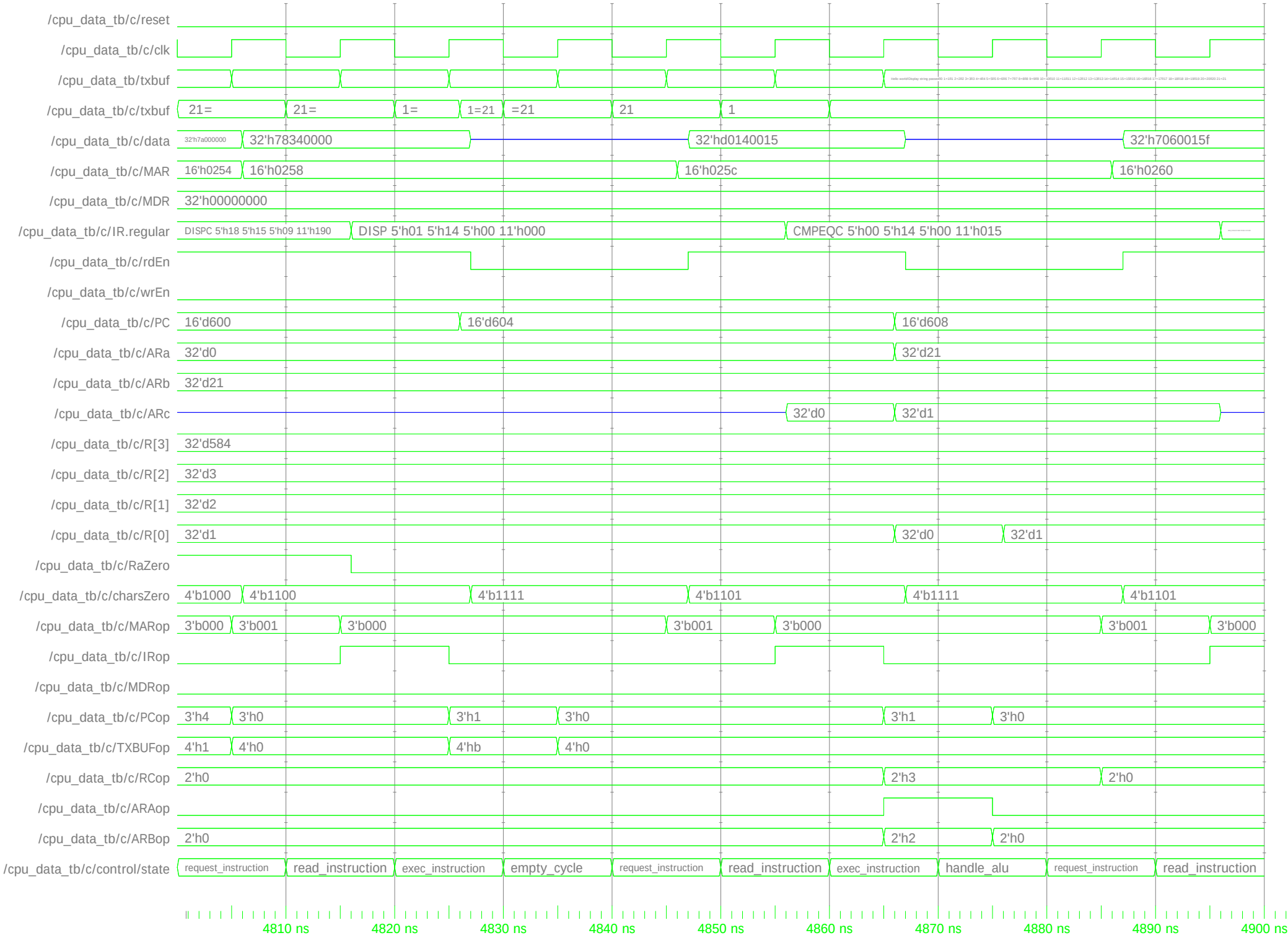


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 46 Page: 46

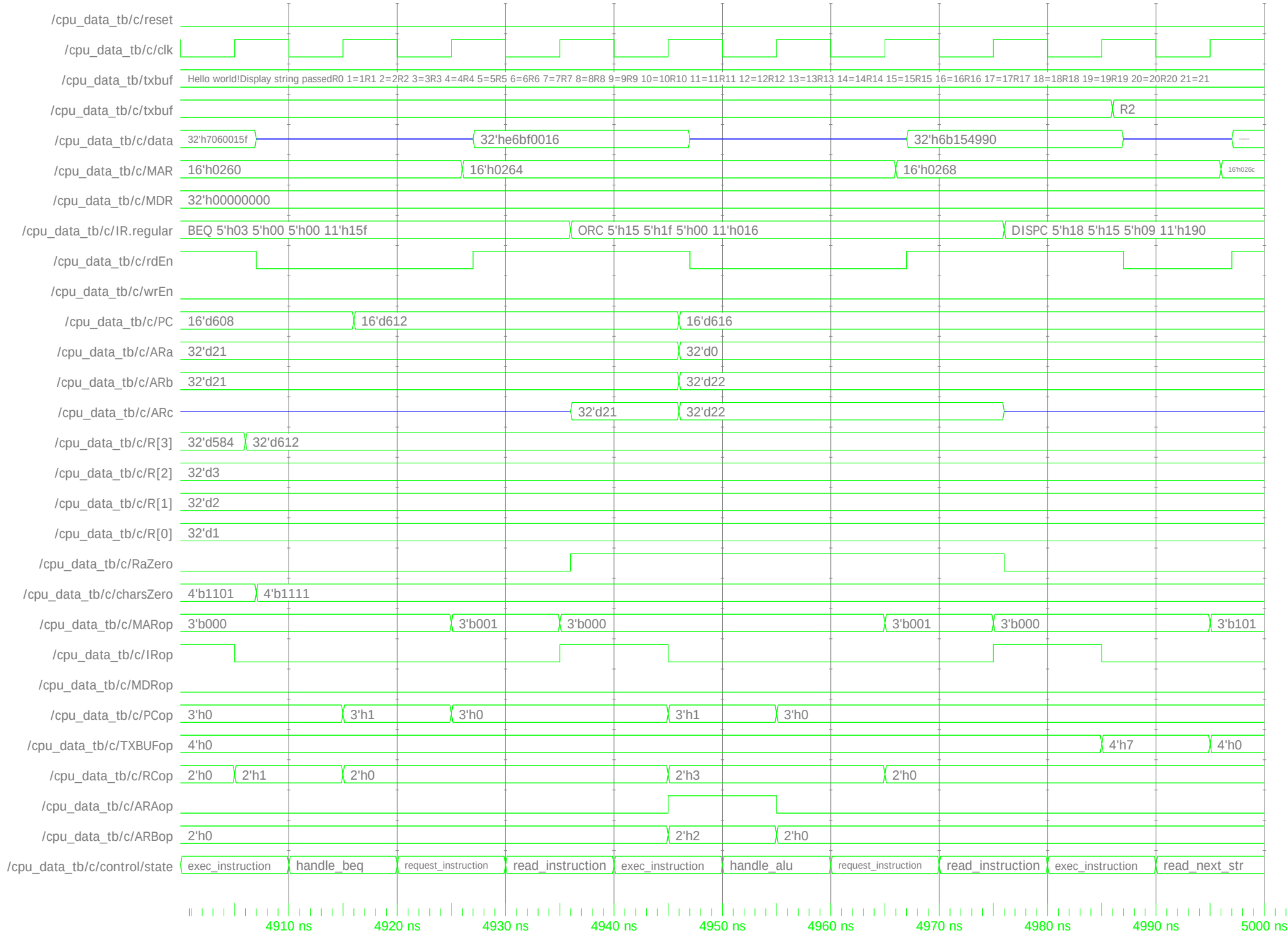

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17R17 18=18R18 19=19R19 20=20
/cpu_data_tb/c/txbuf
=20
20
0
/cpu_data_tb/c/data
32'hd0130014
32'h70600166
/cpu_data_tb/c/MAR
16'h023c
16'h0240
16'h0244
16'h0248
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h13 5'h00 11'h000
CMPEQC 5'h00 5'h13 5'h00 11'h014
BEQ 5'h03 5'h00 5'h00 11'h166
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd576
16'd580
16'd584
/cpu_data_tb/c/ARa
32'd0
32'd20
/cpu_data_tb/c/ARb
32'd20
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd556
32'd584
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
4610 ns
4620 ns
4630 ns
4640 ns
4650 ns
4660 ns
4670 ns
4680 ns
4690 ns
4700 ns



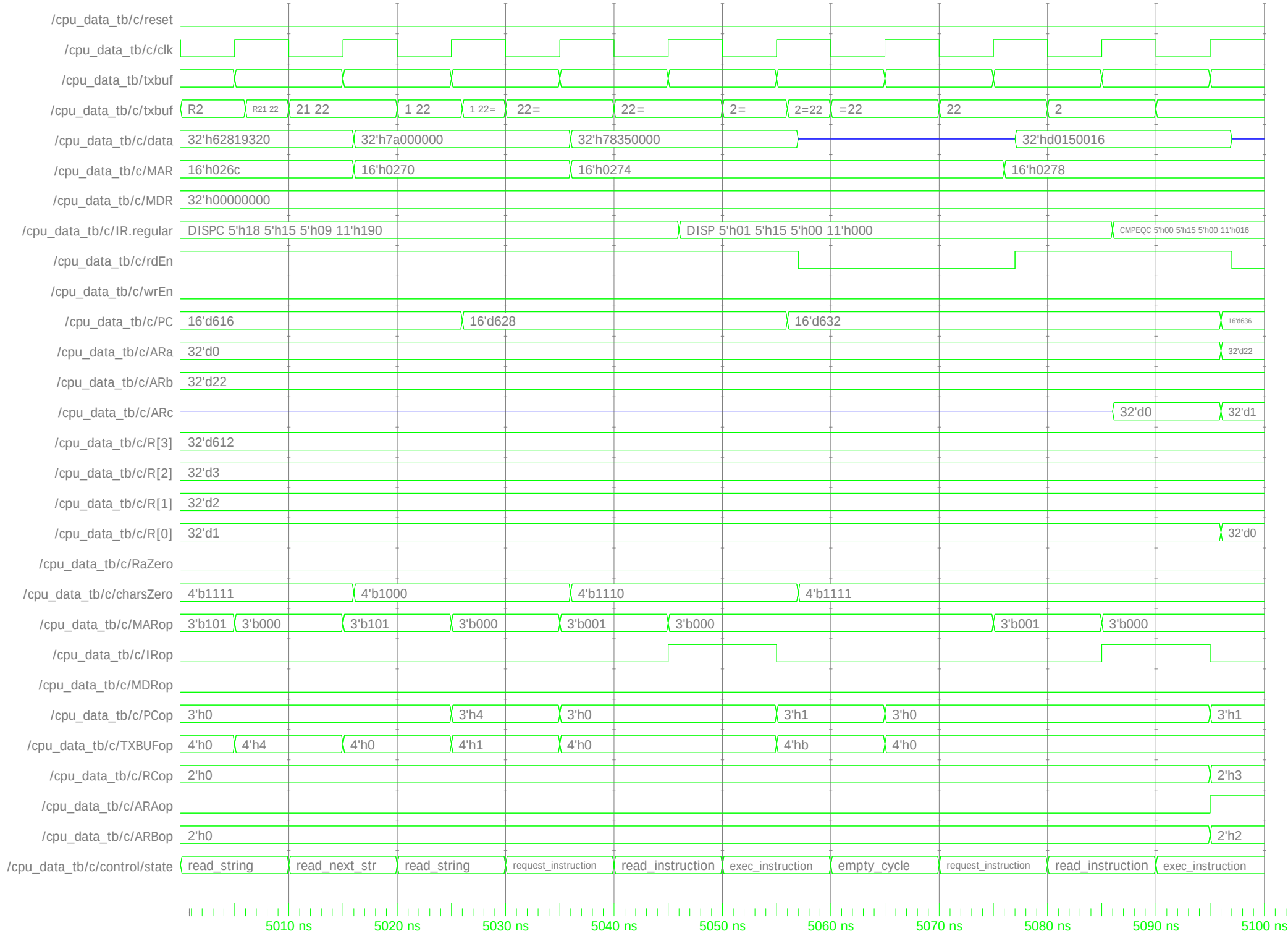
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 48 Page: 48

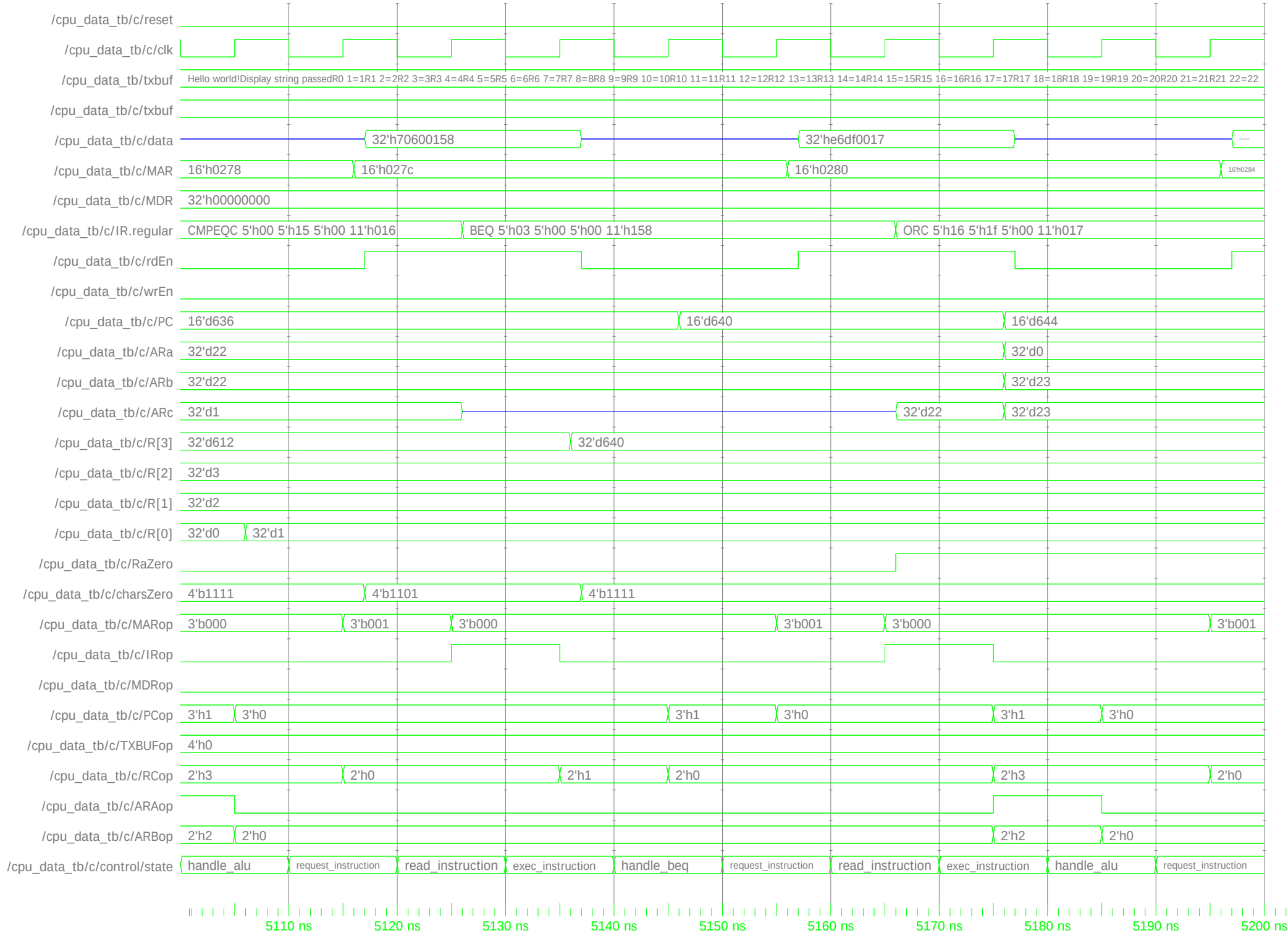


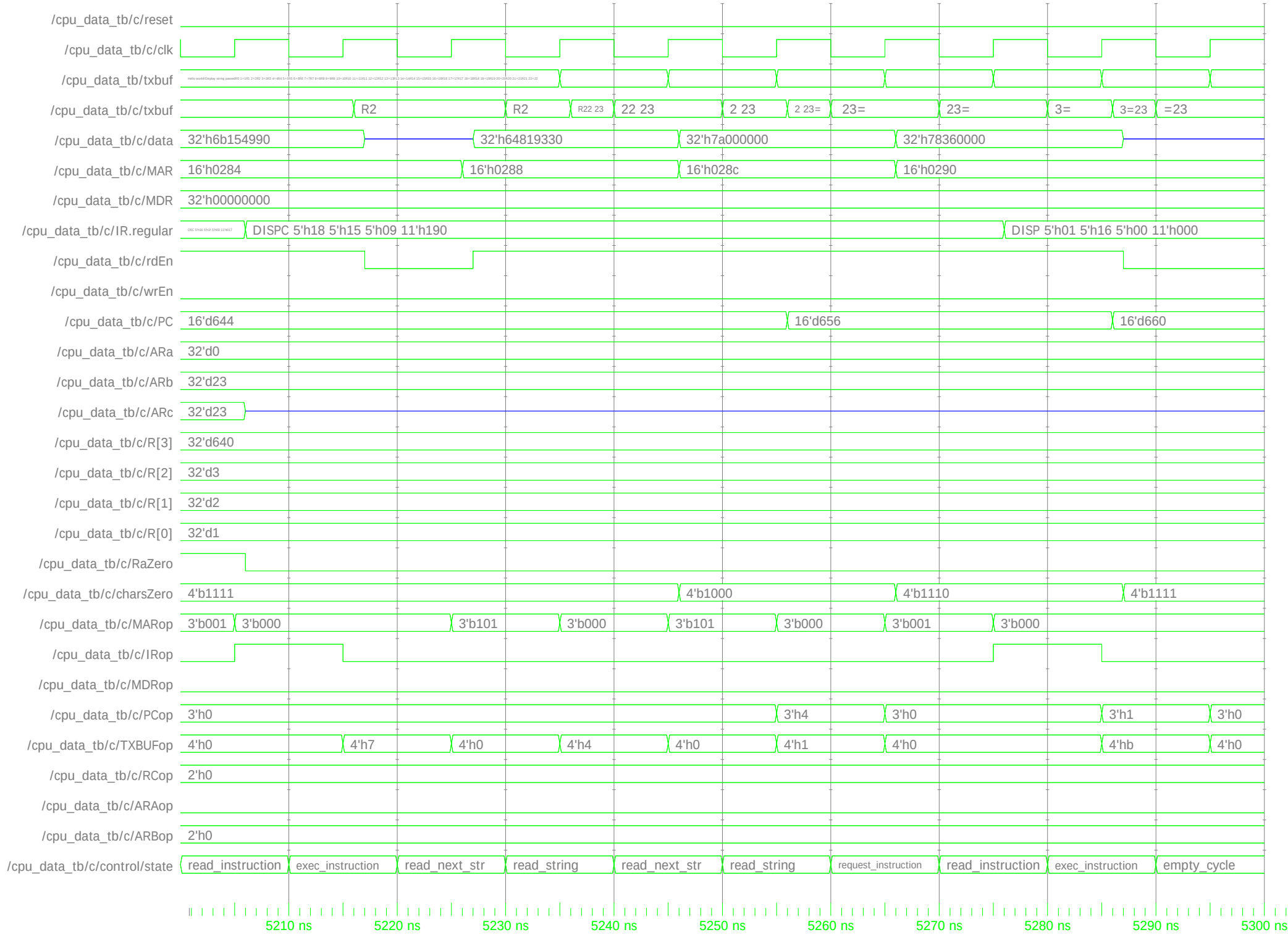
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 49 Page: 49

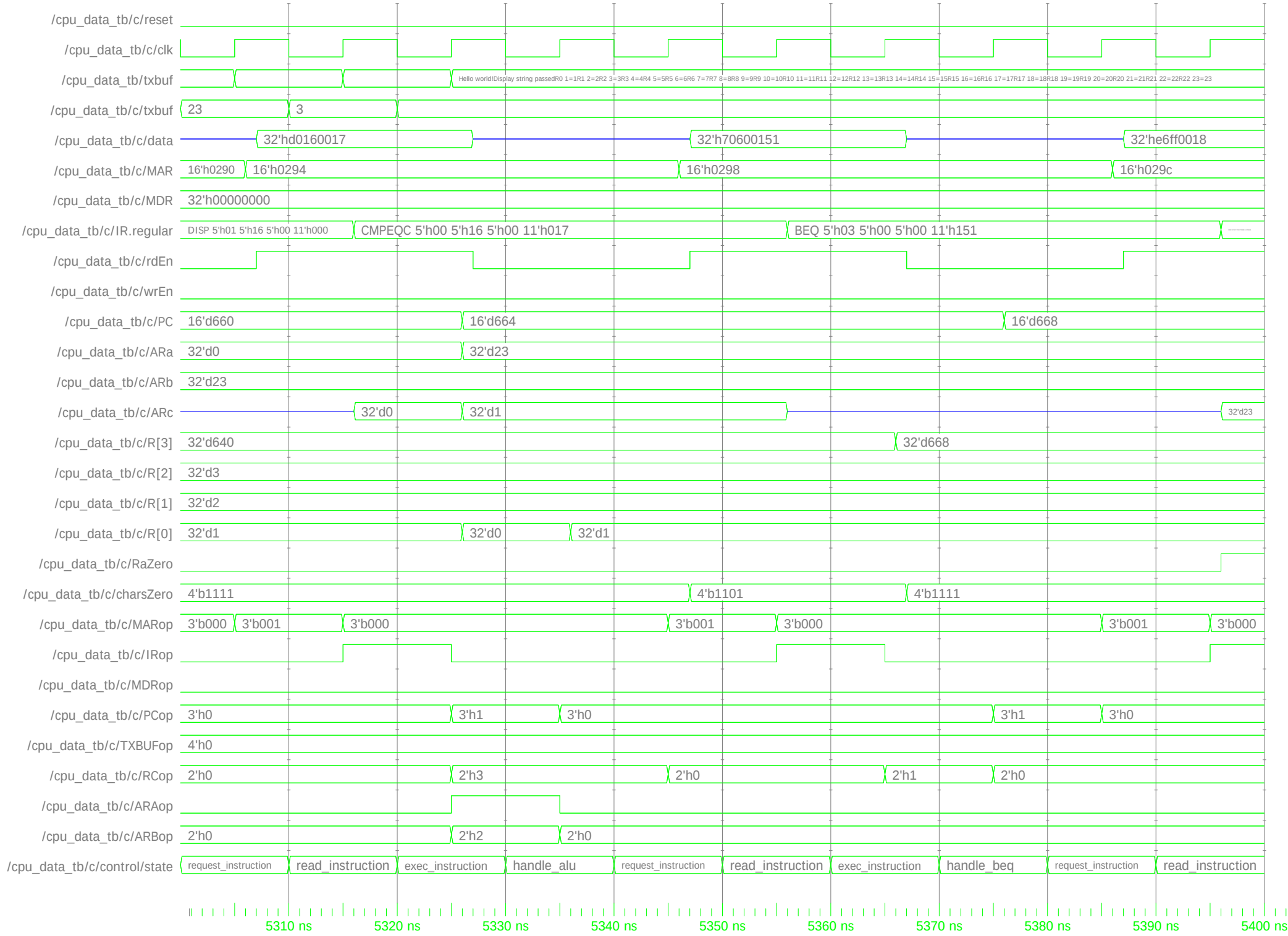


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 50 Page: 50

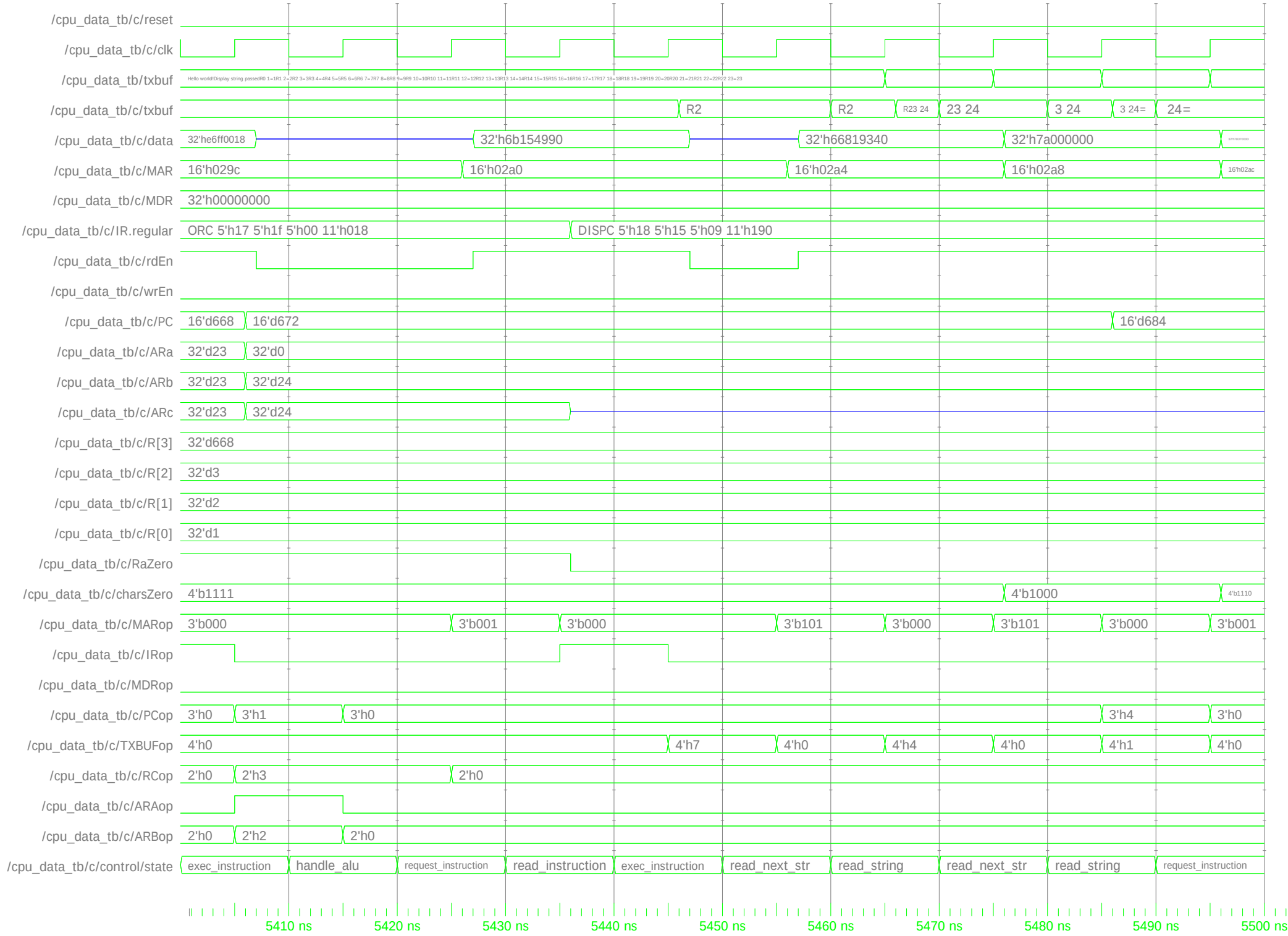

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
R2
R21 22
21 22
1 22
1 22=
22=
22=
2=
2=22
=22
22
2
/cpu_data_tb/c/data
32'h62819320
32'h7a000000
32'h78350000
32'hd0150016
/cpu_data_tb/c/MAR
16'h026c
16'h0270
16'h0274
16'h0278
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h190
DISP 5'h01 5'h15 5'h00 11'h000
CMPEQC 5'h00 5'h15 5'h00 11'h016
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd616
16'd628
16'd632
16'd636
/cpu_data_tb/c/ARa
32'd0
32'd22
/cpu_data_tb/c/ARb
32'd22
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd612
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'h4
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
/cpu_data_tb/c/control/state
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
5010 ns
5020 ns
5030 ns
5040 ns
5050 ns
5060 ns
5070 ns
5080 ns
5090 ns
5100 ns

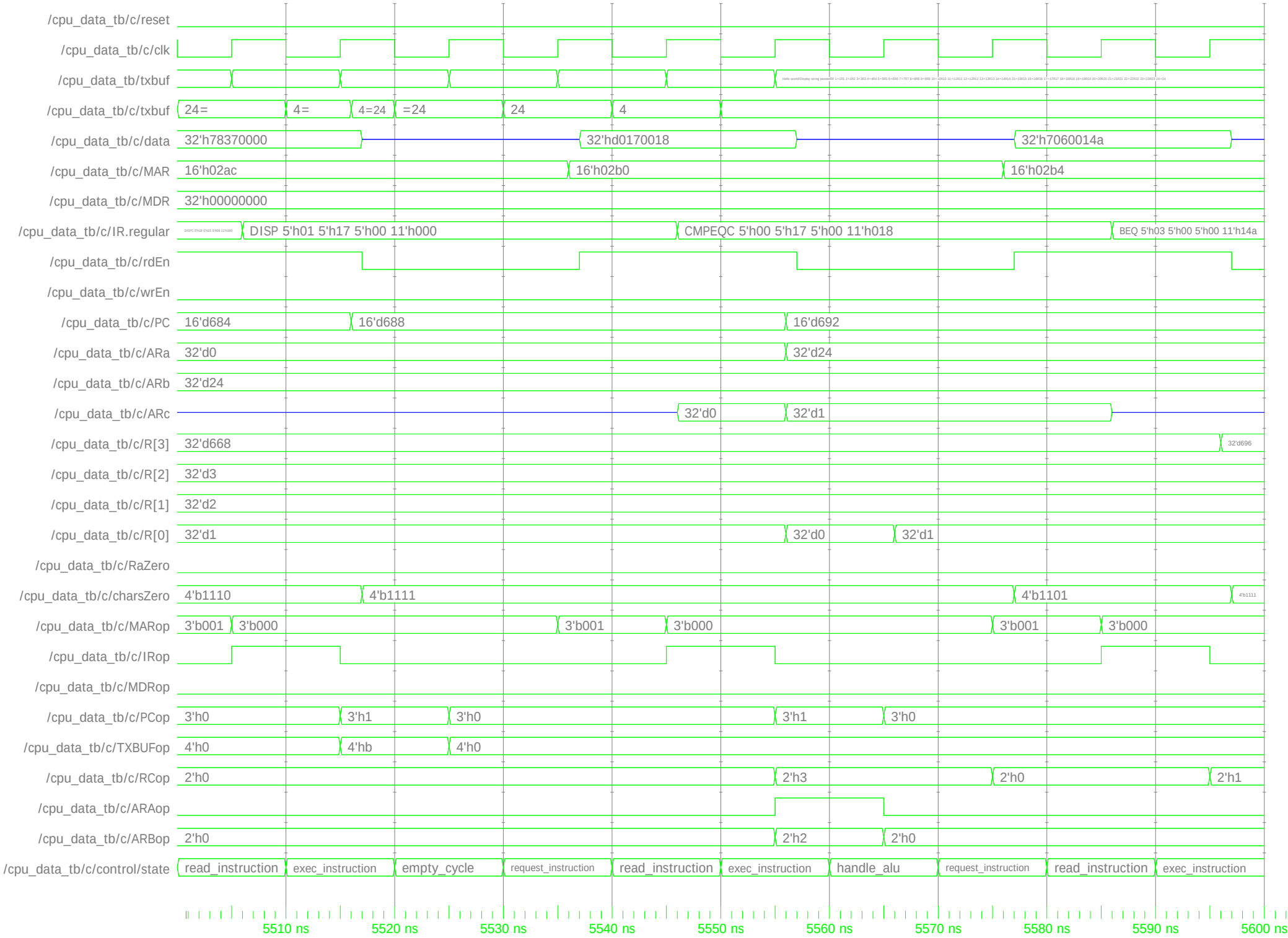

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17R17 18=18R18 19=19R19 20=20R20 21=21R21 22=22
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h70600158
32'he6df0017
/cpu_data_tb/c/MAR
16'h0278
16'h027c
16'h0280
16'h0284
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
CMPEQC 5'h00 5'h15 5'h00 11'h016
BEQ 5'h03 5'h00 5'h00 11'h158
ORC 5'h16 5'h1f 5'h00 11'h017
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd636
16'd640
16'd644
/cpu_data_tb/c/ARa
32'd22
32'd0
/cpu_data_tb/c/ARb
32'd22
32'd23
/cpu_data_tb/c/ARc
32'd1
32'd22
32'd23
/cpu_data_tb/c/R[3]
32'd612
32'd640
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h3
2'h0
2'h1
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h2
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
5110 ns
5120 ns
5130 ns
5140 ns
5150 ns
5160 ns
5170 ns
5180 ns
5190 ns
5200 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
R2
R2
R22 23
22 23
2 23
2 23=
23=
23=
3=
3=23
=23
/cpu_data_tb/c/data
32'h6b154990
32'h64819330
32'h7a000000
32'h78360000
/cpu_data_tb/c/MAR
16'h0284
16'h0288
16'h028c
16'h0290
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h190
DISP 5'h01 5'h16 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd644
16'd656
16'd660
/cpu_data_tb/c/ARa
32'd0
/cpu_data_tb/c/ARb
32'd23
/cpu_data_tb/c/ARc
32'd23
/cpu_data_tb/c/R[3]
32'd640
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
5210 ns
5220 ns
5230 ns
5240 ns
5250 ns
5260 ns
5270 ns
5280 ns
5290 ns
5300 ns

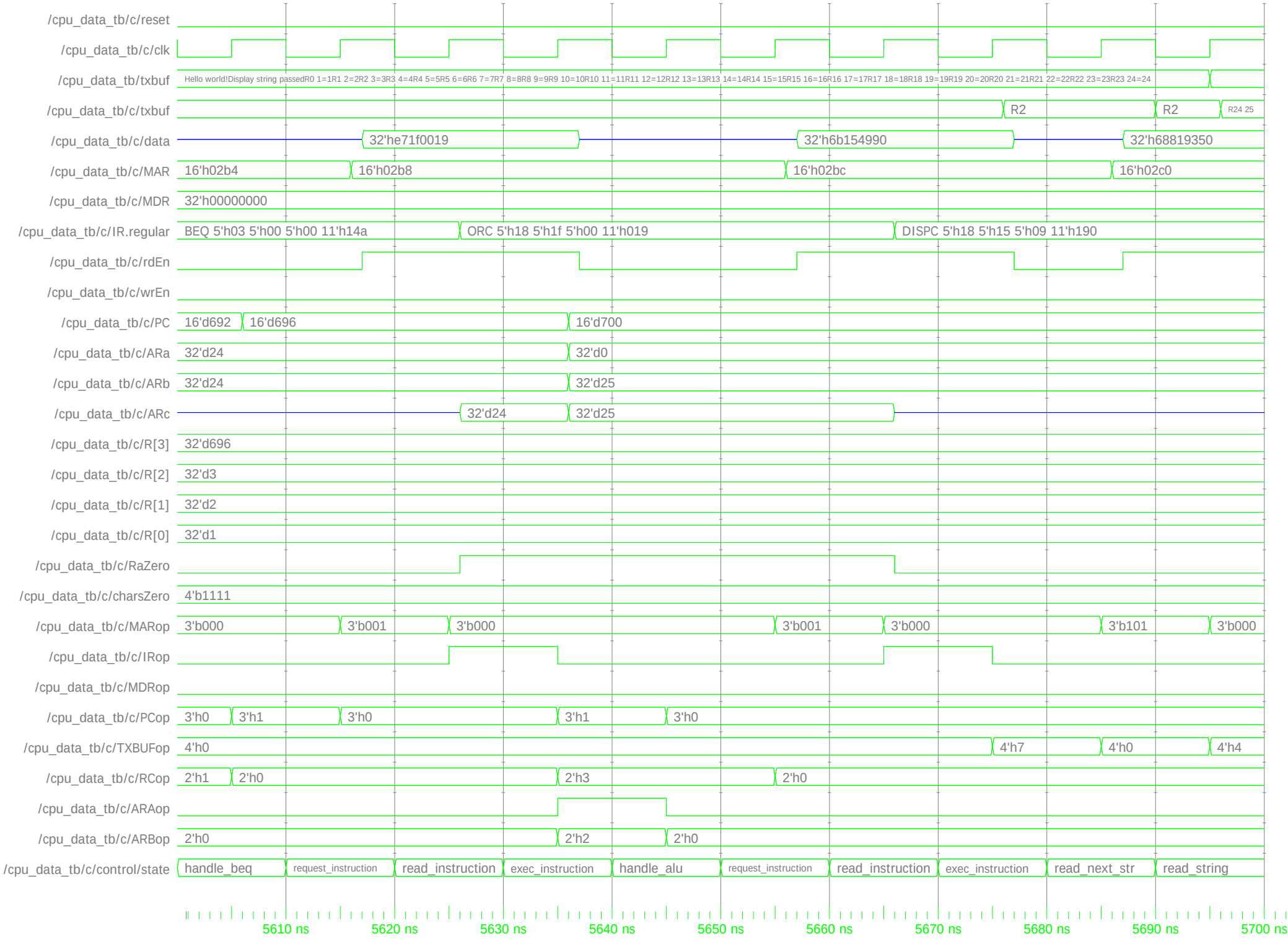


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 54 Page: 54

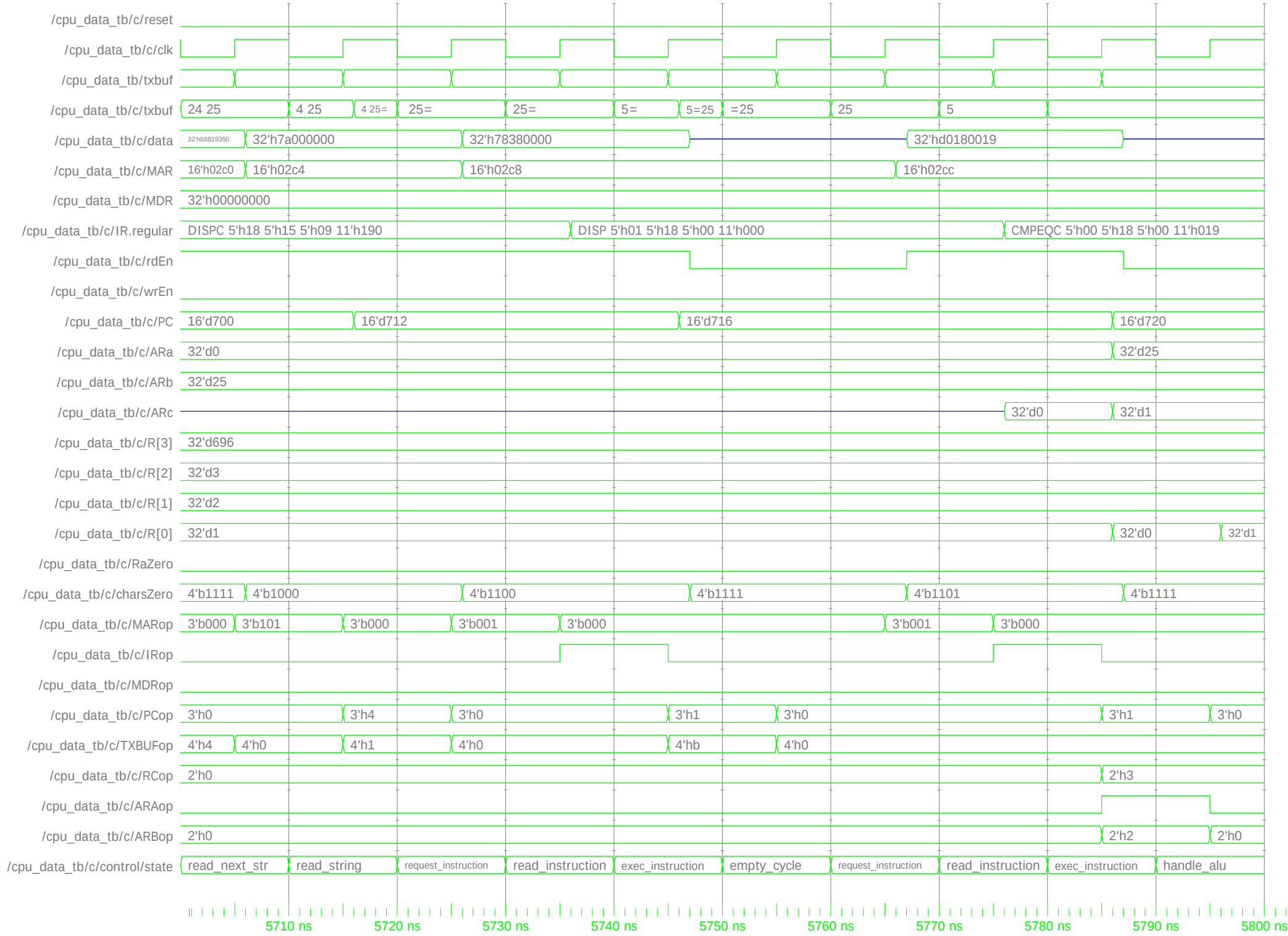

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17R17 18=18R18 19=19R19 20=20R20 21=21R21 22=22R22 23=23
/cpu_data_tb/c/txbuf
R2
R2
R23 24
23 24
3 24
3 24=
24=
/cpu_data_tb/c/data
32'he6ff0018
32'h6b154990
32'h66819340
32'h7a000000
/cpu_data_tb/c/MAR
16'h029c
16'h02a0
16'h02a4
16'h02a8
16'h02ac
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
ORC 5'h17 5'h1f 5'h00 11'h018
DISPC 5'h18 5'h15 5'h09 11'h190
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd668
16'd672
16'd684
/cpu_data_tb/c/ARa
32'd23
32'd0
/cpu_data_tb/c/ARb
32'd23
32'd24
/cpu_data_tb/c/ARc
32'd23
32'd24
/cpu_data_tb/c/R[3]
32'd668
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
5410 ns
5420 ns
5430 ns
5440 ns
5450 ns
5460 ns
5470 ns
5480 ns
5490 ns
5500 ns



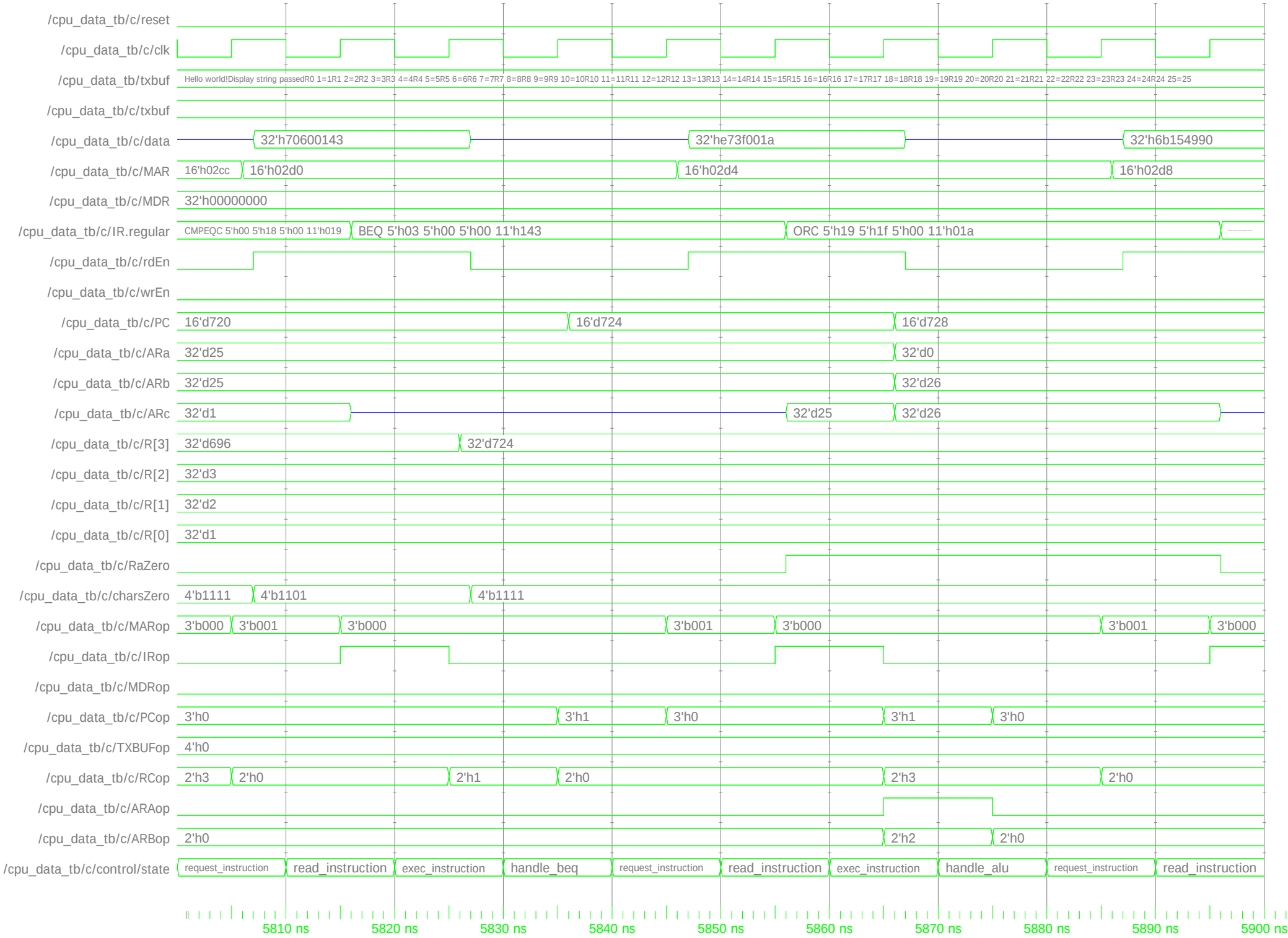
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 56 Page: 56



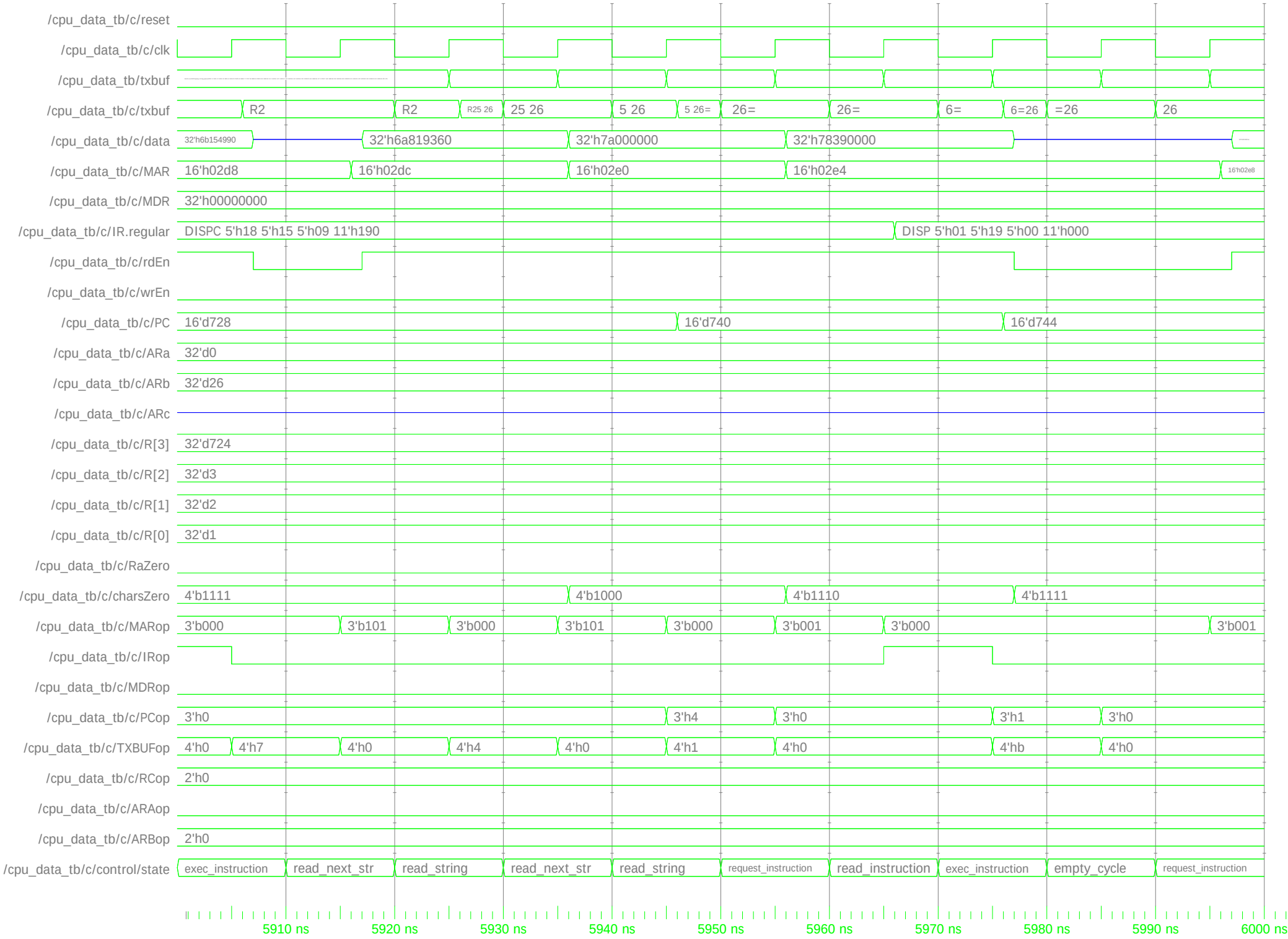
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 57 Page: 57



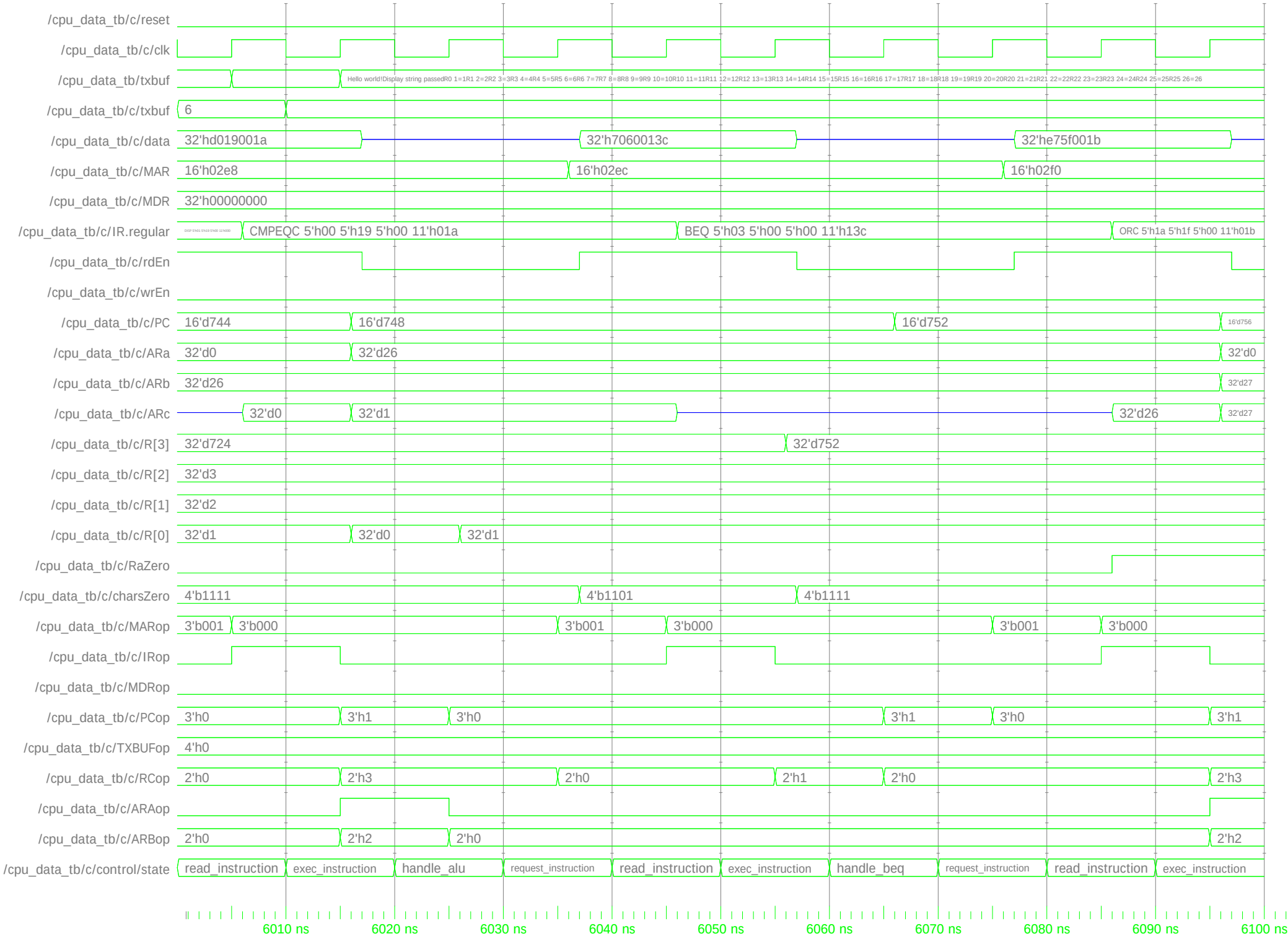
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 58 Page: 58

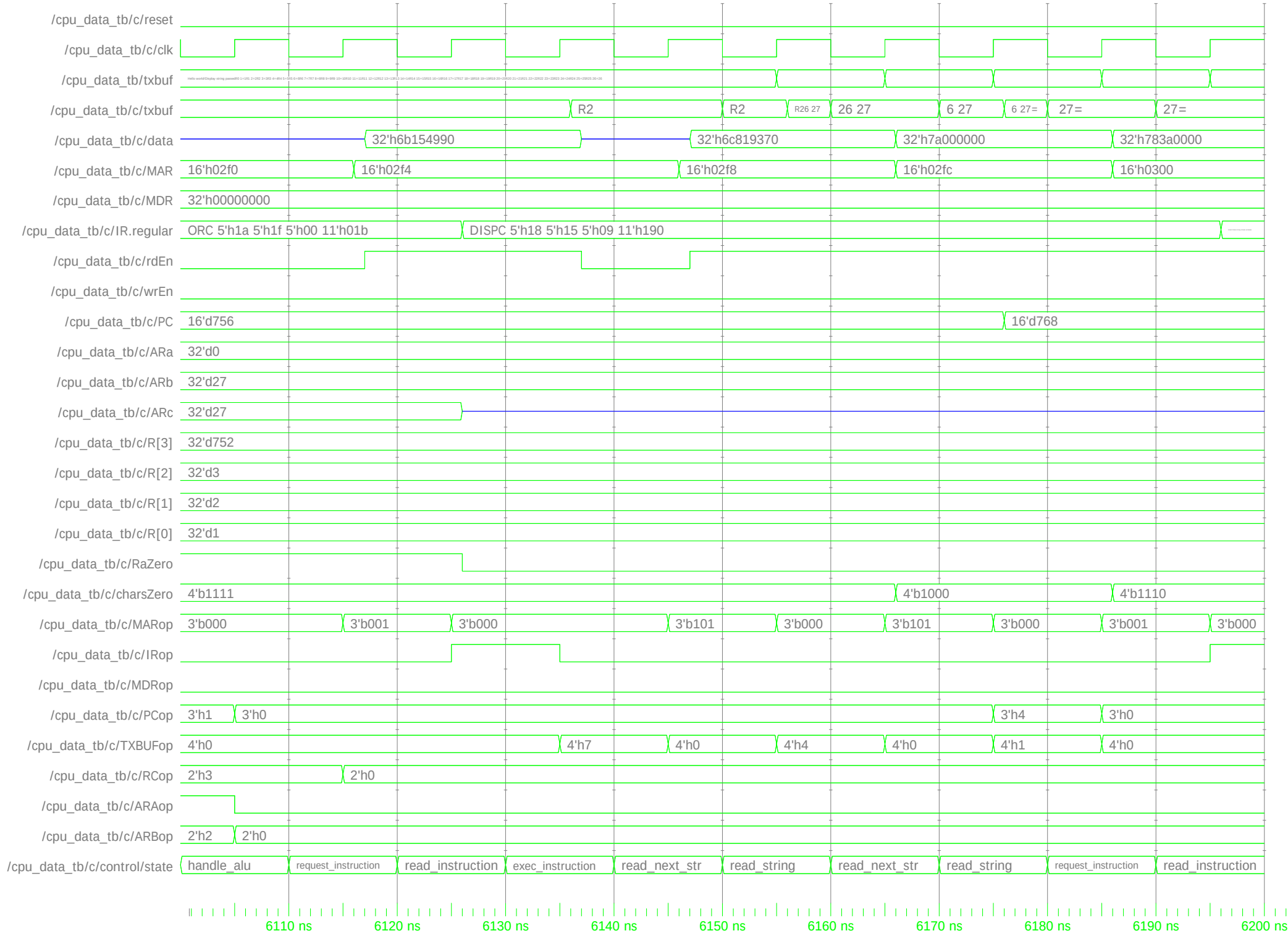


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 59 Page: 59

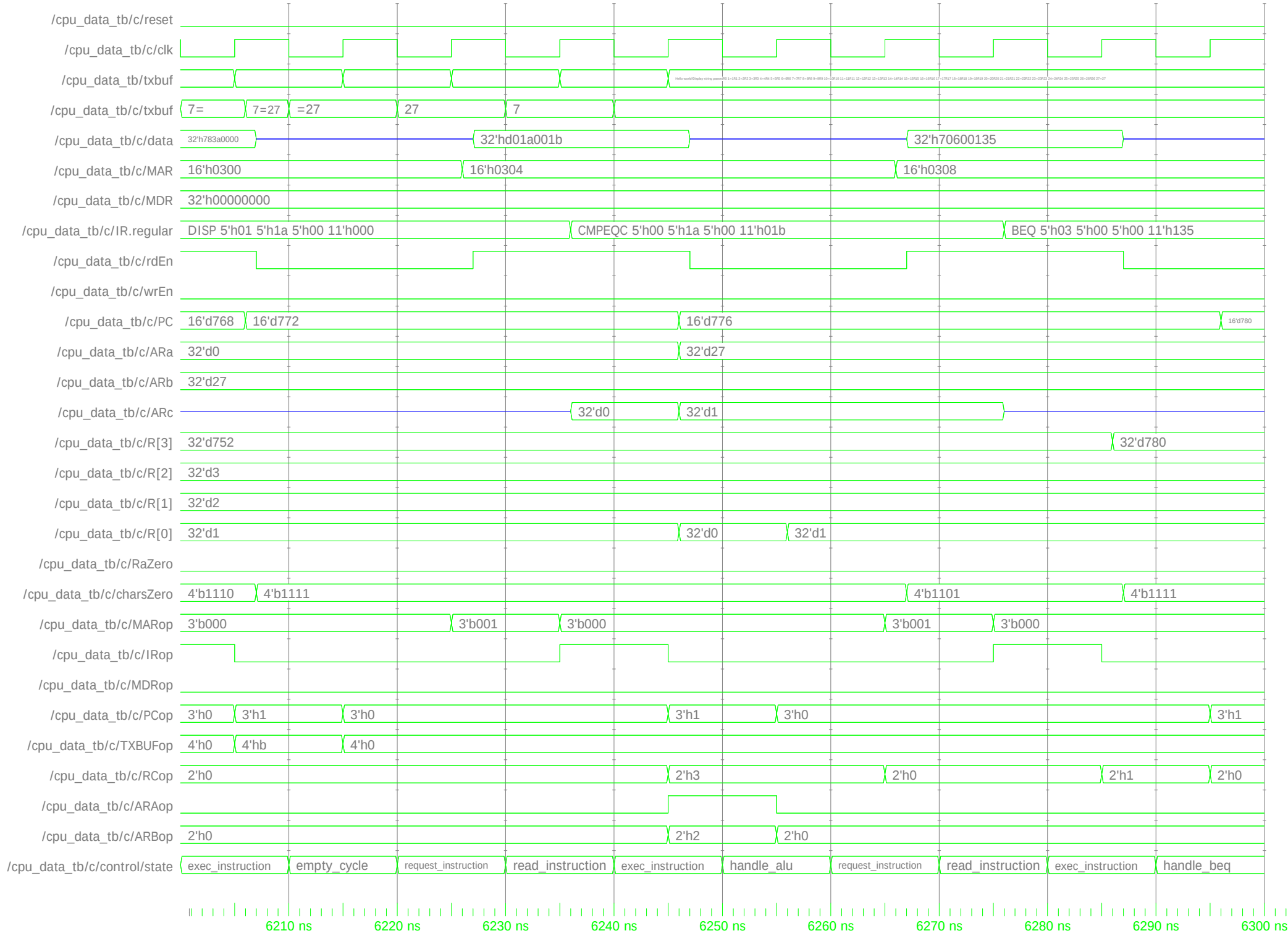


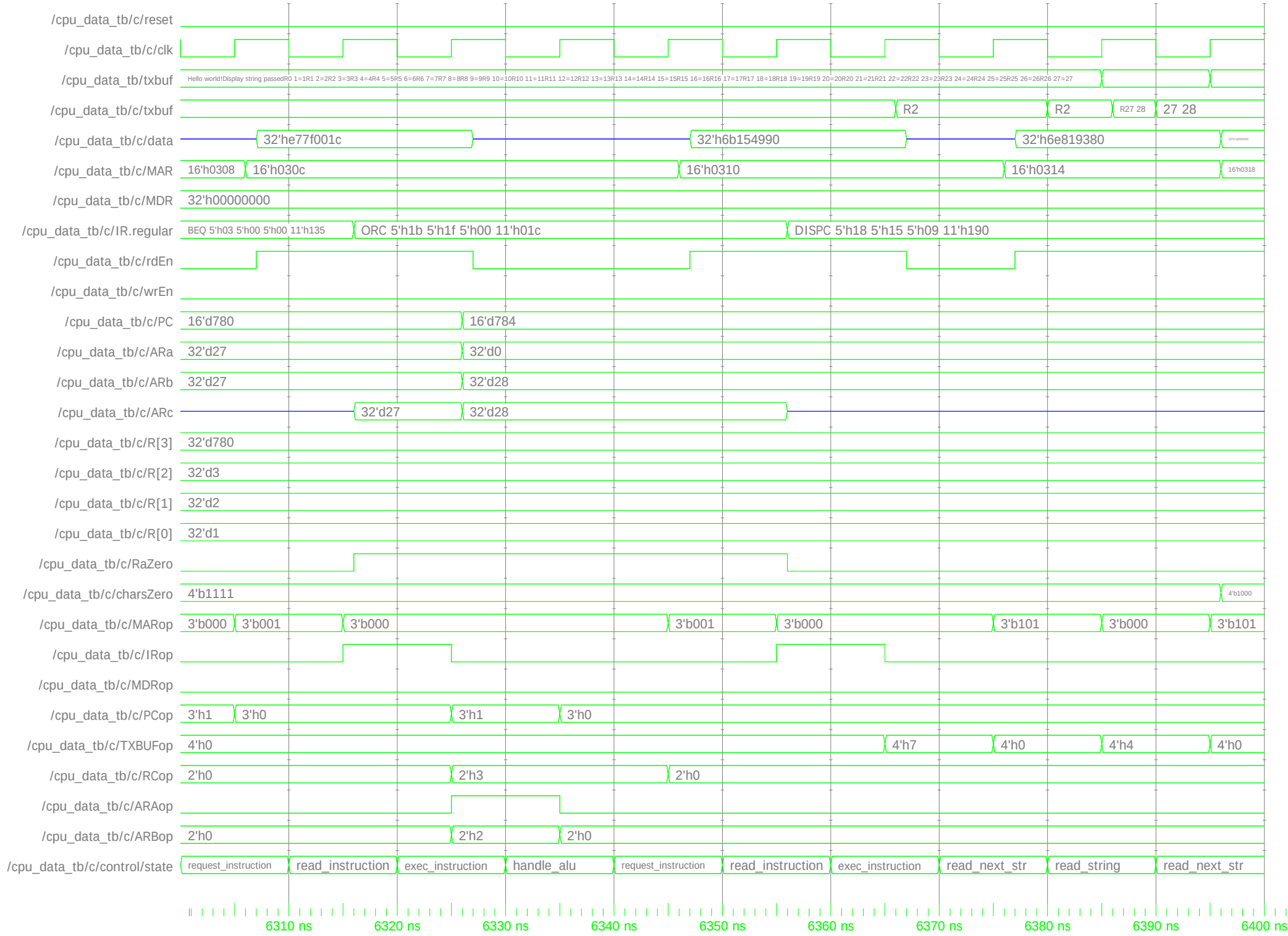
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 60 Page: 60


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
Hello world!Display string passedR0 1=1R1 2=2R2 3=3R3 4=4R4 5=5R5 6=6R6 7=7R7 8=8R8 9=9R9 10=10R10 11=11R11 12=12R12 13=13R13 14=14R14 15=15R15 16=16R16 17=17R17 18=18R18 19=19R19 20=20R20 21=21R21 22=22R22 23=23R23 24=24R24 25=25R25 26=26
/cpu_data_tb/c/txbuf
6
/cpu_data_tb/c/data
32'hd019001a
32'h7060013c
32'he75f001b
/cpu_data_tb/c/MAR
16'h02e8
16'h02ec
16'h02f0
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
CMPEQC 5'h00 5'h19 5'h00 11'h01a
BEQ 5'h03 5'h00 5'h00 11'h13c
ORC 5'h1a 5'h1f 5'h00 11'h01b
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd744
16'd748
16'd752
16'd756
/cpu_data_tb/c/ARa
32'd0
32'd26
32'd0
/cpu_data_tb/c/ARb
32'd26
32'd27
/cpu_data_tb/c/ARc
32'd0
32'd1
32'd26
32'd27
/cpu_data_tb/c/R[3]
32'd724
32'd752
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
2'h2
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
6010 ns
6020 ns
6030 ns
6040 ns
6050 ns
6060 ns
6070 ns
6080 ns
6090 ns
6100 ns

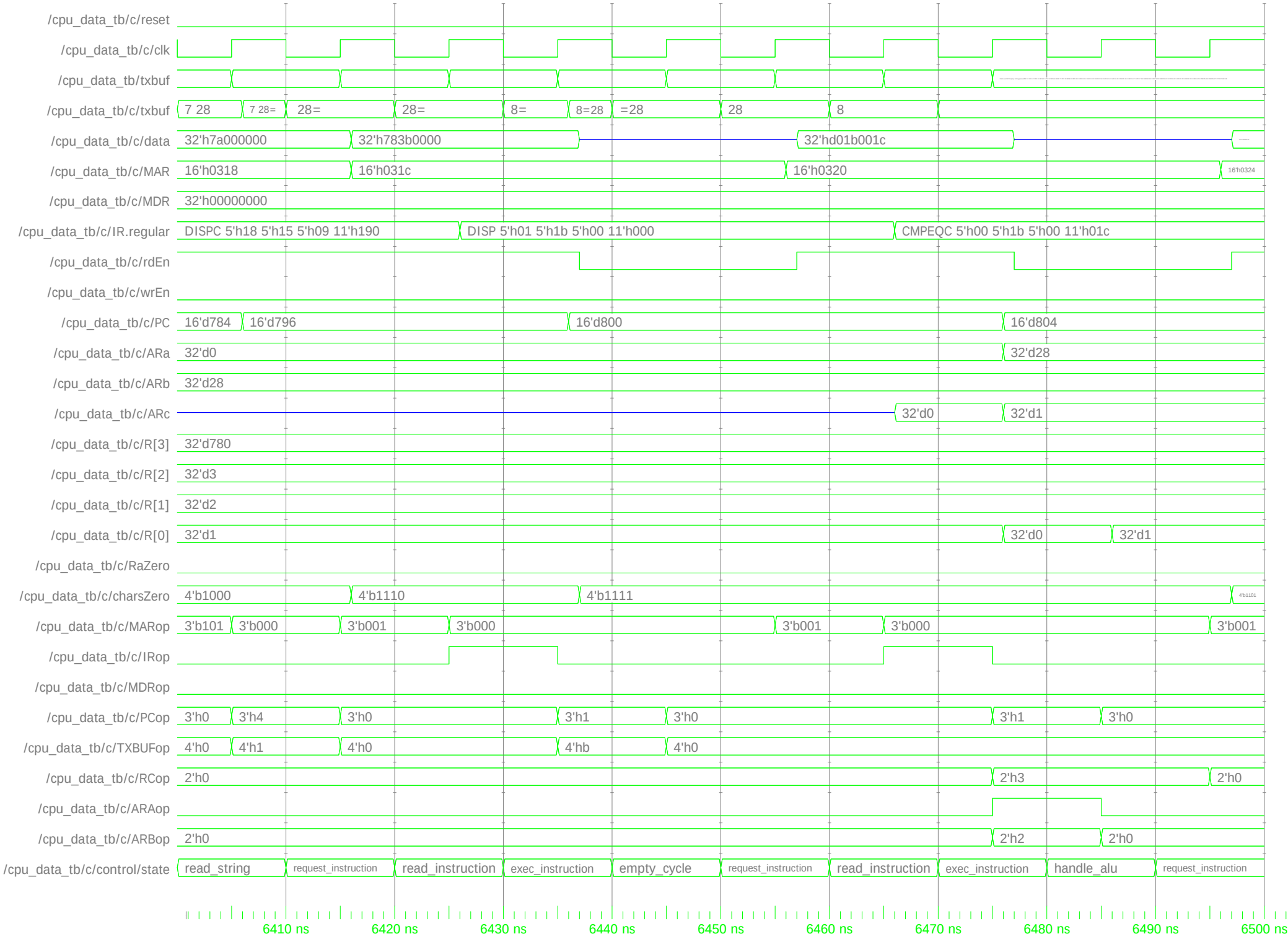


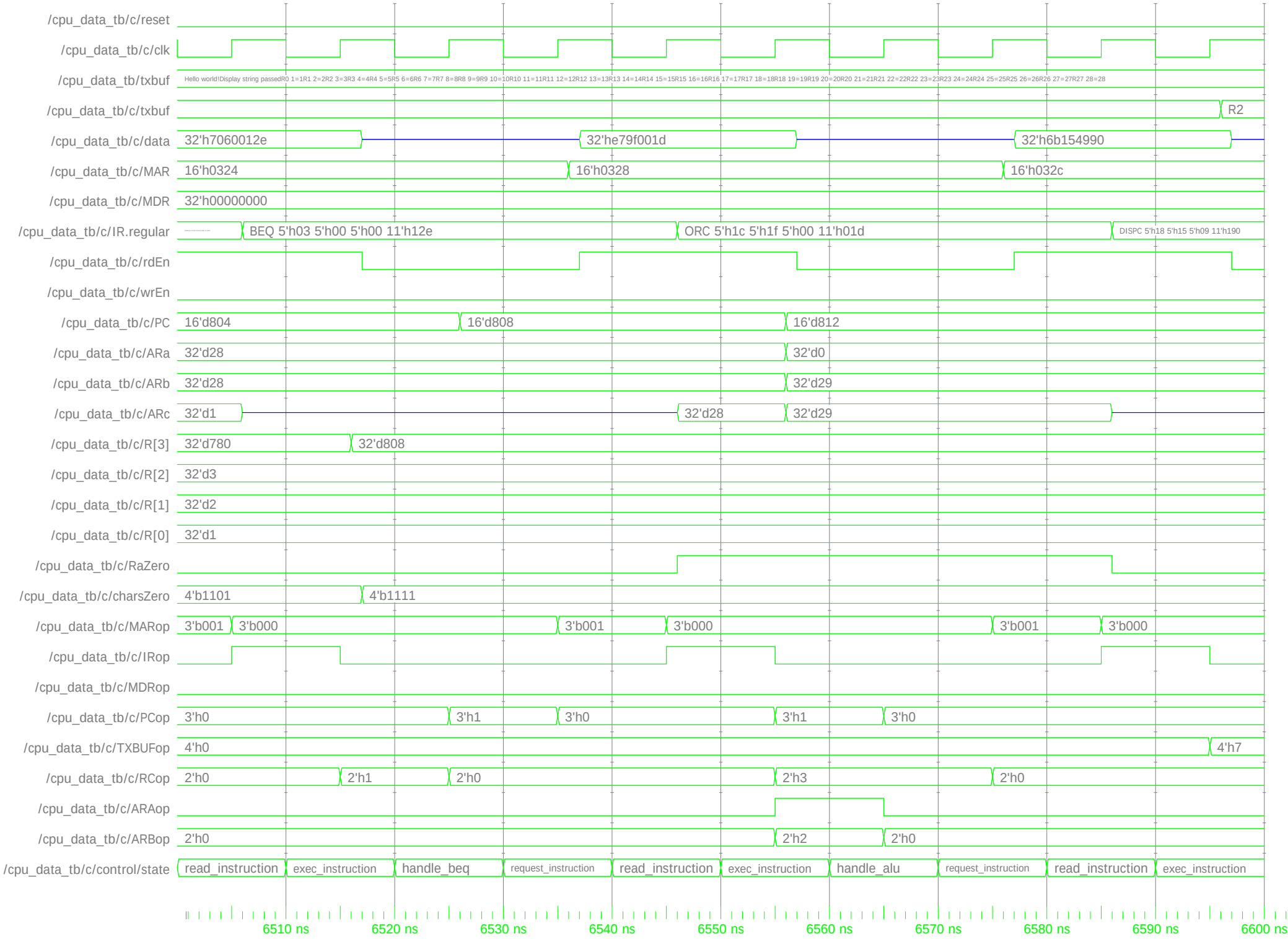
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 62 Page: 62


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
7=
7=27
=27
27
7
/cpu_data_tb/c/data
32'h783a0000
32'hd01a001b
32'h70600135
/cpu_data_tb/c/MAR
16'h0300
16'h0304
16'h0308
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h1a 5'h00 11'h000
CMPEQC 5'h00 5'h1a 5'h00 11'h01b
BEQ 5'h03 5'h00 5'h00 11'h135
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd768
16'd772
16'd776
16'd780
/cpu_data_tb/c/ARa
32'd0
32'd27
/cpu_data_tb/c/ARb
32'd27
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd752
32'd780
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
6210 ns
6220 ns
6230 ns
6240 ns
6250 ns
6260 ns
6270 ns
6280 ns
6290 ns
6300 ns

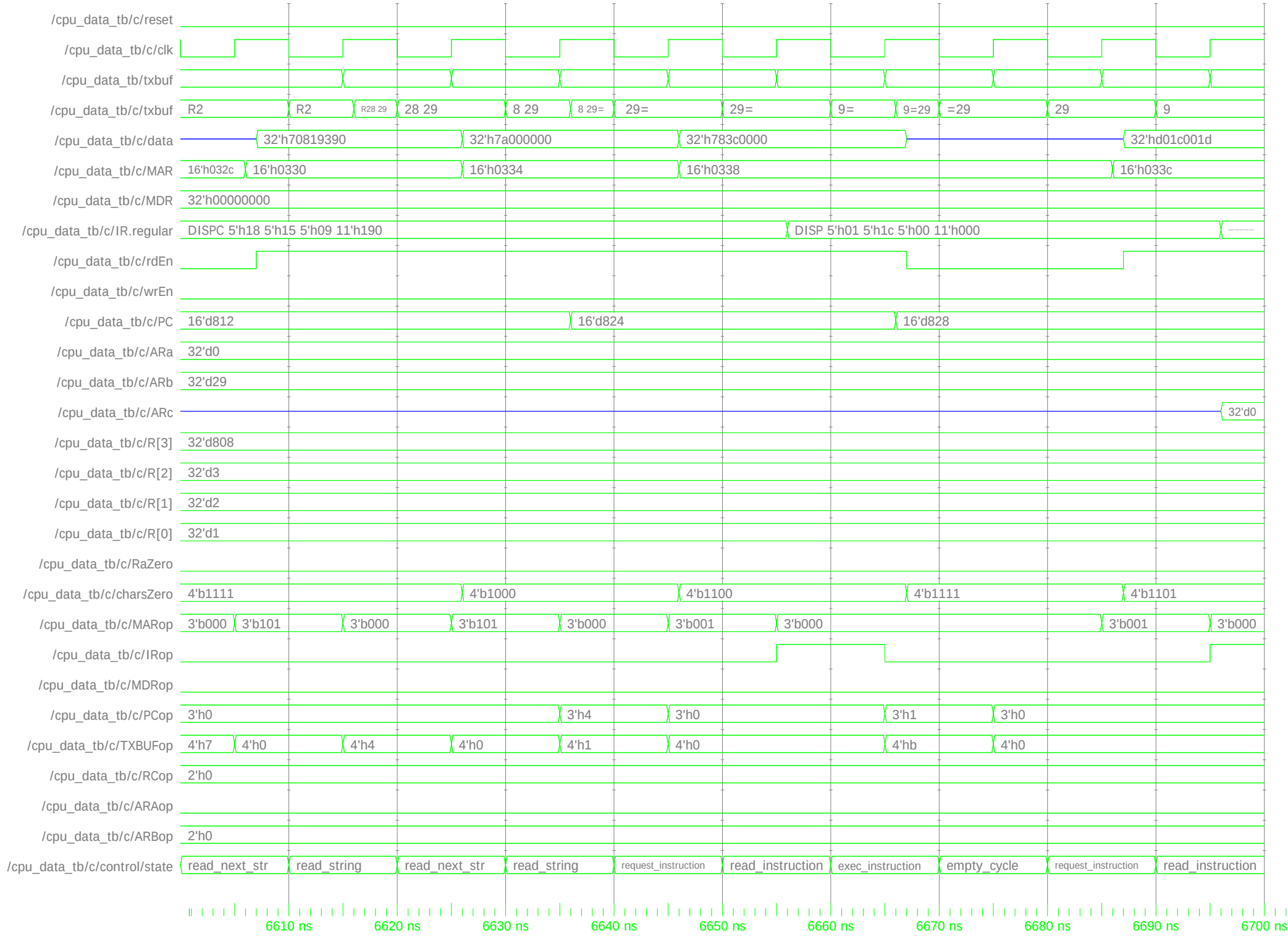


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 64 Page: 64

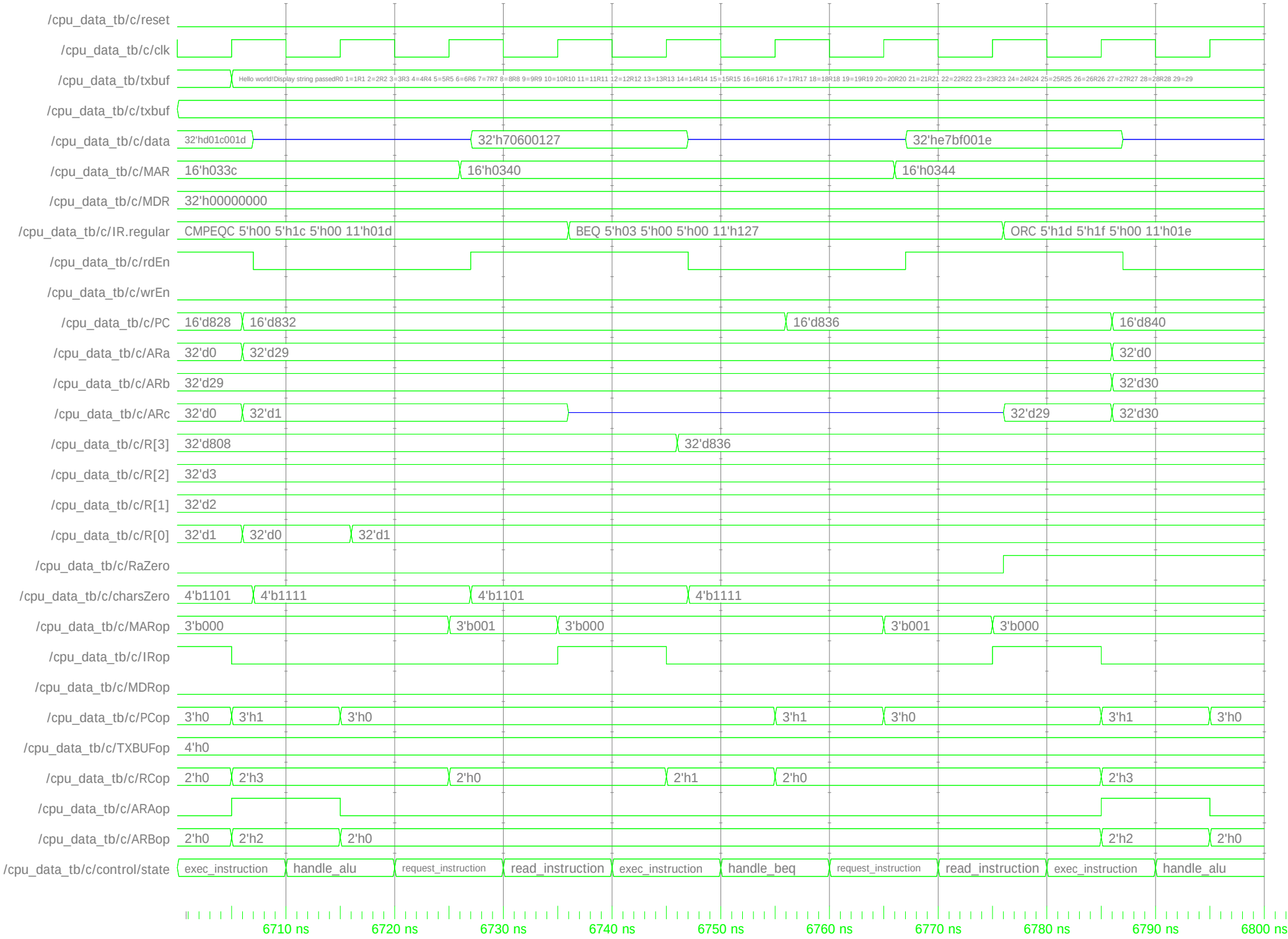

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
7 28
7 28=
28=
28=
8=
8=28
=28
28
8
/cpu_data_tb/c/data
32'h7a000000
32'h783b0000
32'hd01b001c
/cpu_data_tb/c/MAR
16'h0318
16'h031c
16'h0320
16'h0324
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h190
DISP 5'h01 5'h1b 5'h00 11'h000
CMPEQC 5'h00 5'h1b 5'h00 11'h01c
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd784
16'd796
16'd800
16'd804
/cpu_data_tb/c/ARa
32'd0
32'd28
/cpu_data_tb/c/ARb
32'd28
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd780
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1000
4'b1110
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
6410 ns
6420 ns
6430 ns
6440 ns
6450 ns
6460 ns
6470 ns
6480 ns
6490 ns
6500 ns



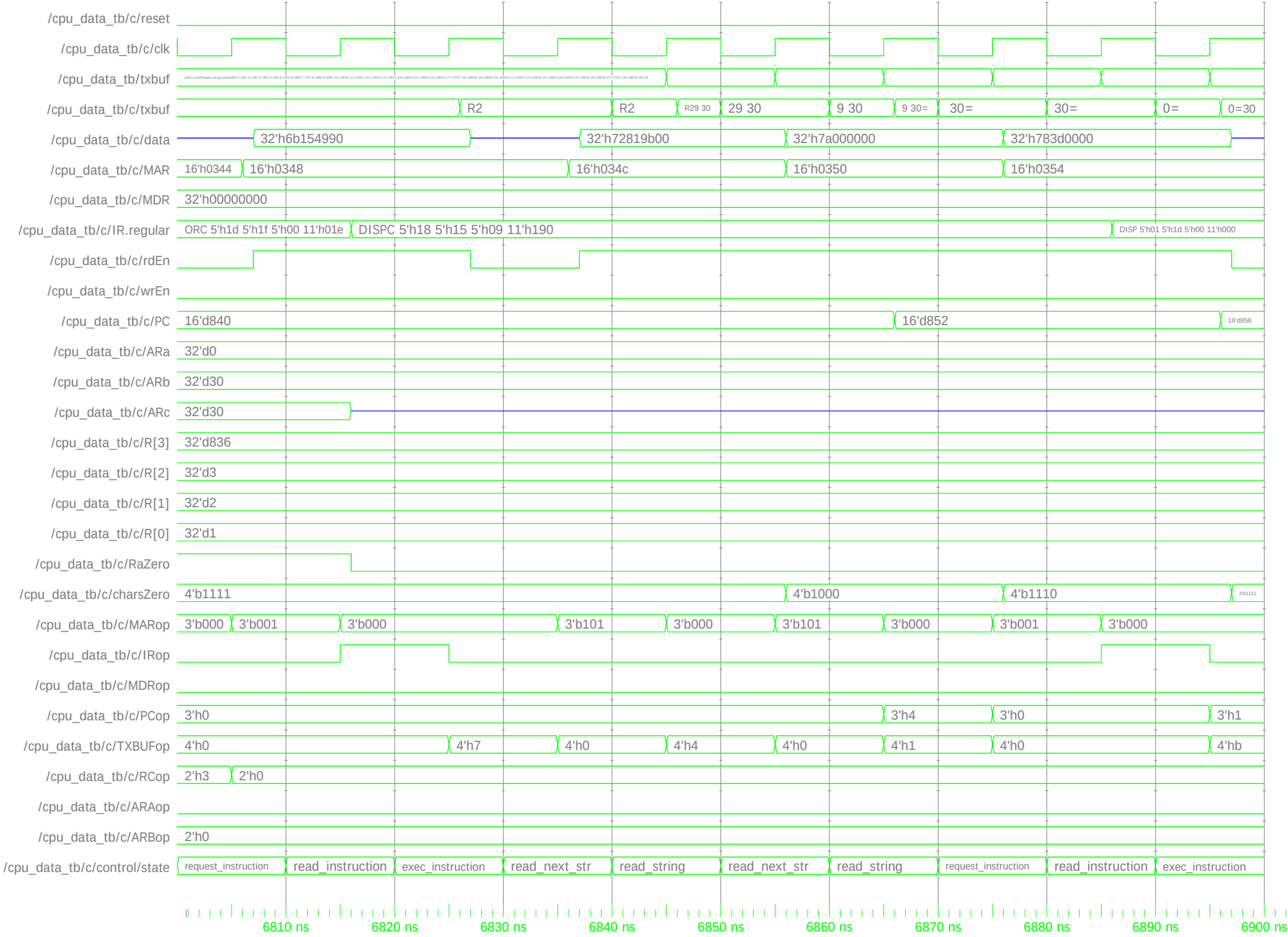
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 66 Page: 66



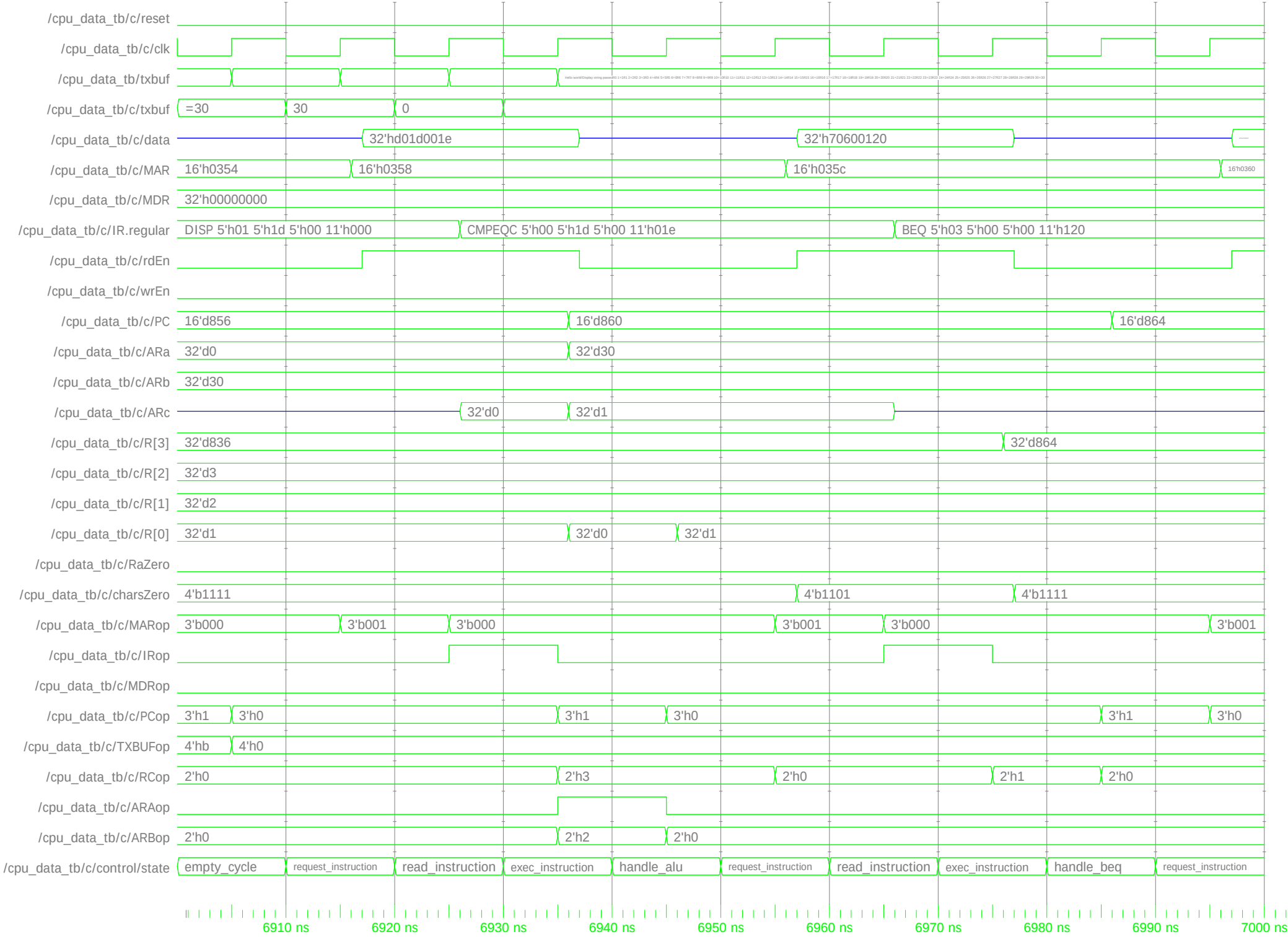
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 67 Page: 67

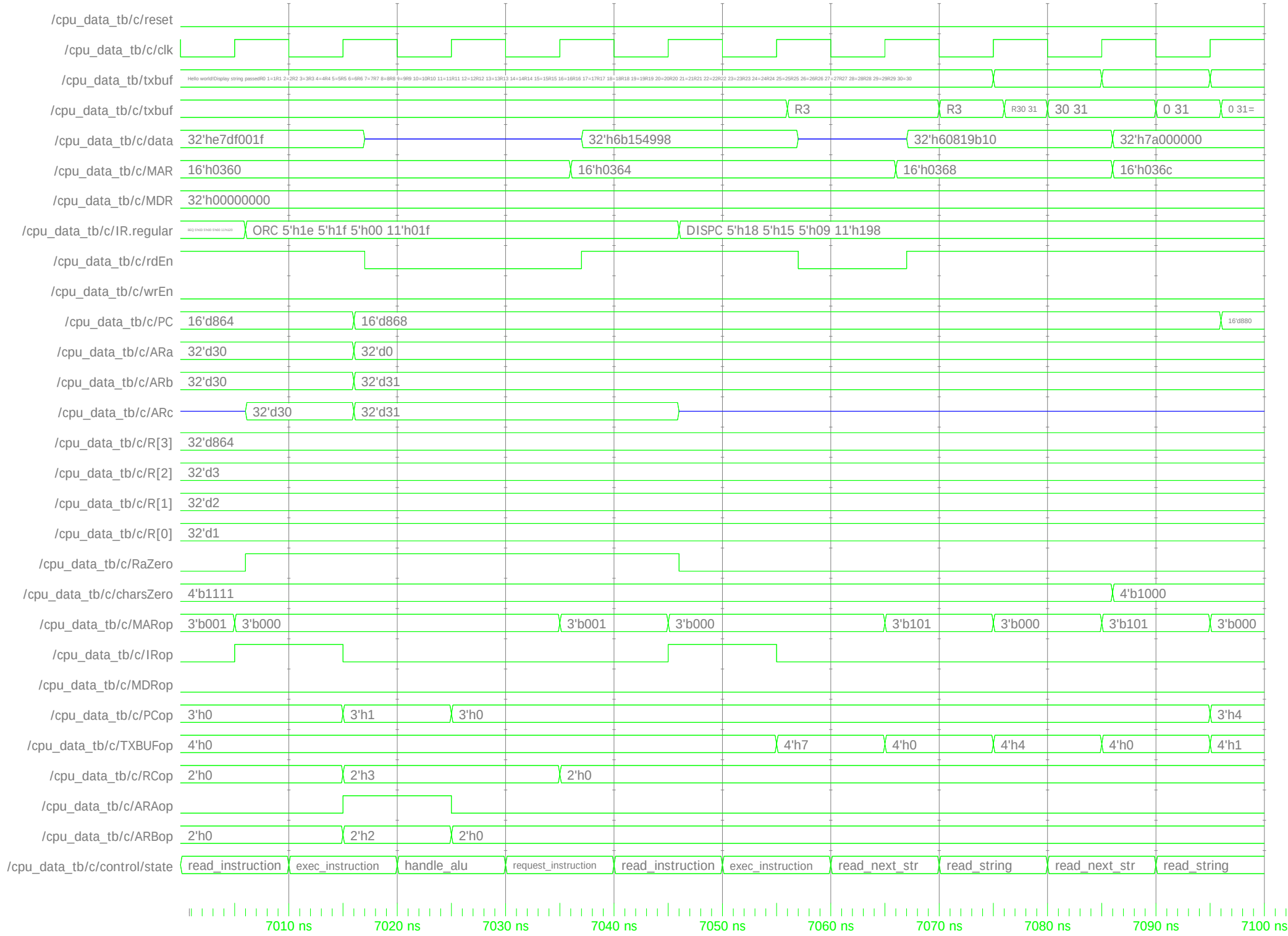


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 68 Page: 68

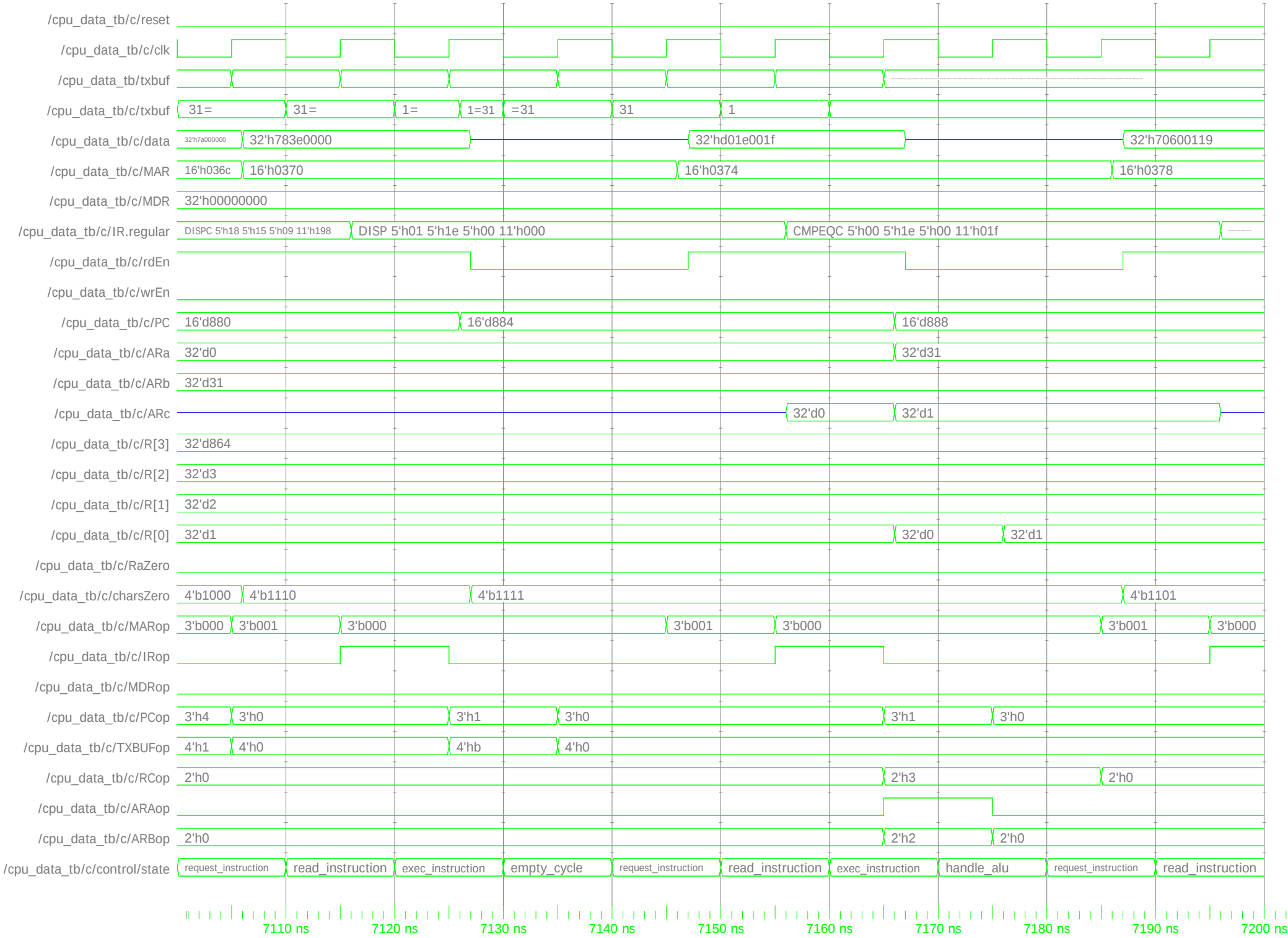


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 69 Page: 69

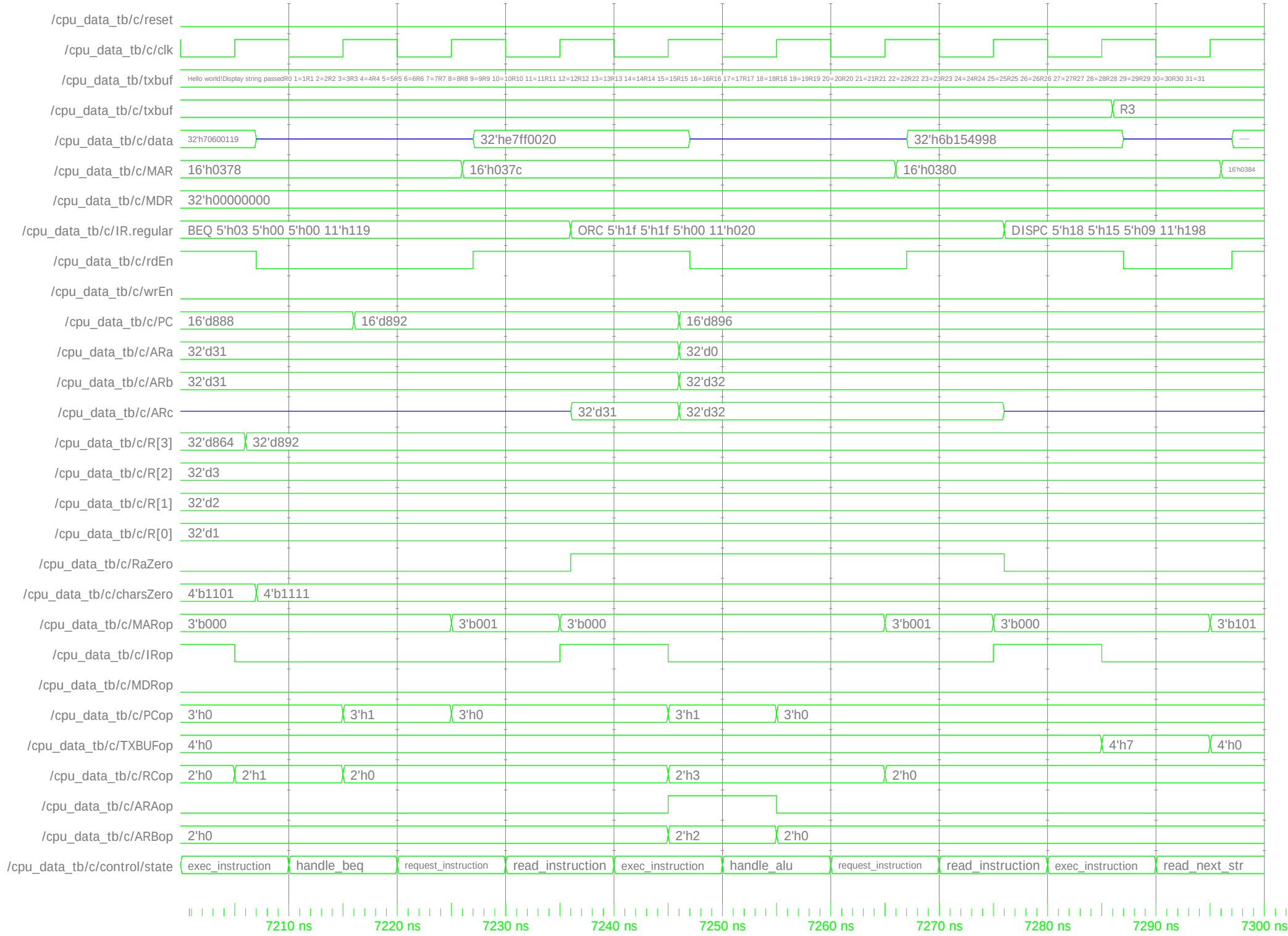

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
=30
30
0
/cpu_data_tb/c/data
32'hd01d001e
32'h70600120
/cpu_data_tb/c/MAR
16'h0354
16'h0358
16'h035c
16'h0360
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h1d 5'h00 11'h000
CMPEQC 5'h00 5'h1d 5'h00 11'h01e
BEQ 5'h03 5'h00 5'h00 11'h120
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd856
16'd860
16'd864
/cpu_data_tb/c/ARa
32'd0
32'd30
/cpu_data_tb/c/ARb
32'd30
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd836
32'd864
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
32'd0
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
6910 ns
6920 ns
6930 ns
6940 ns
6950 ns
6960 ns
6970 ns
6980 ns
6990 ns
7000 ns



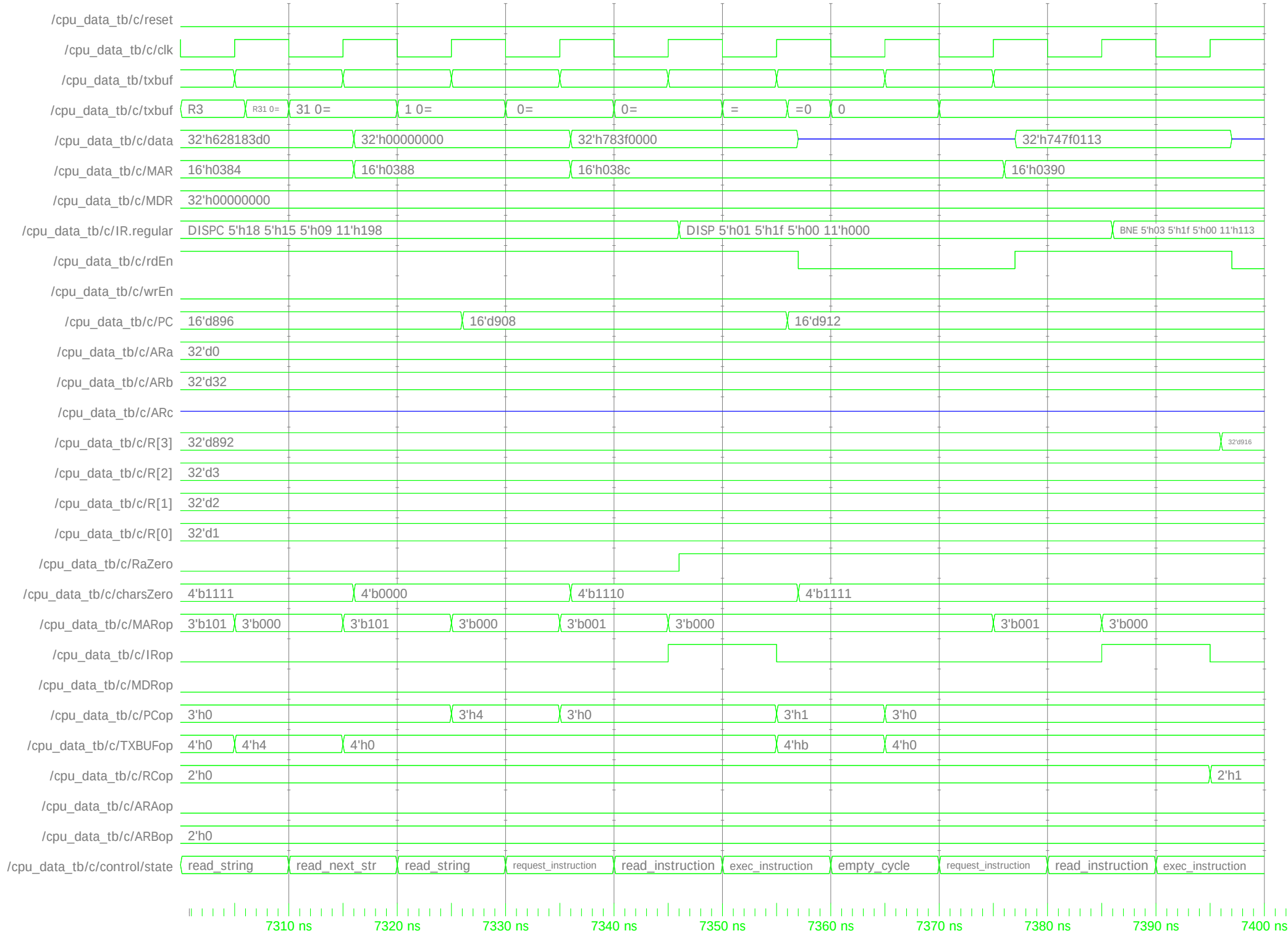
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 71 Page: 71

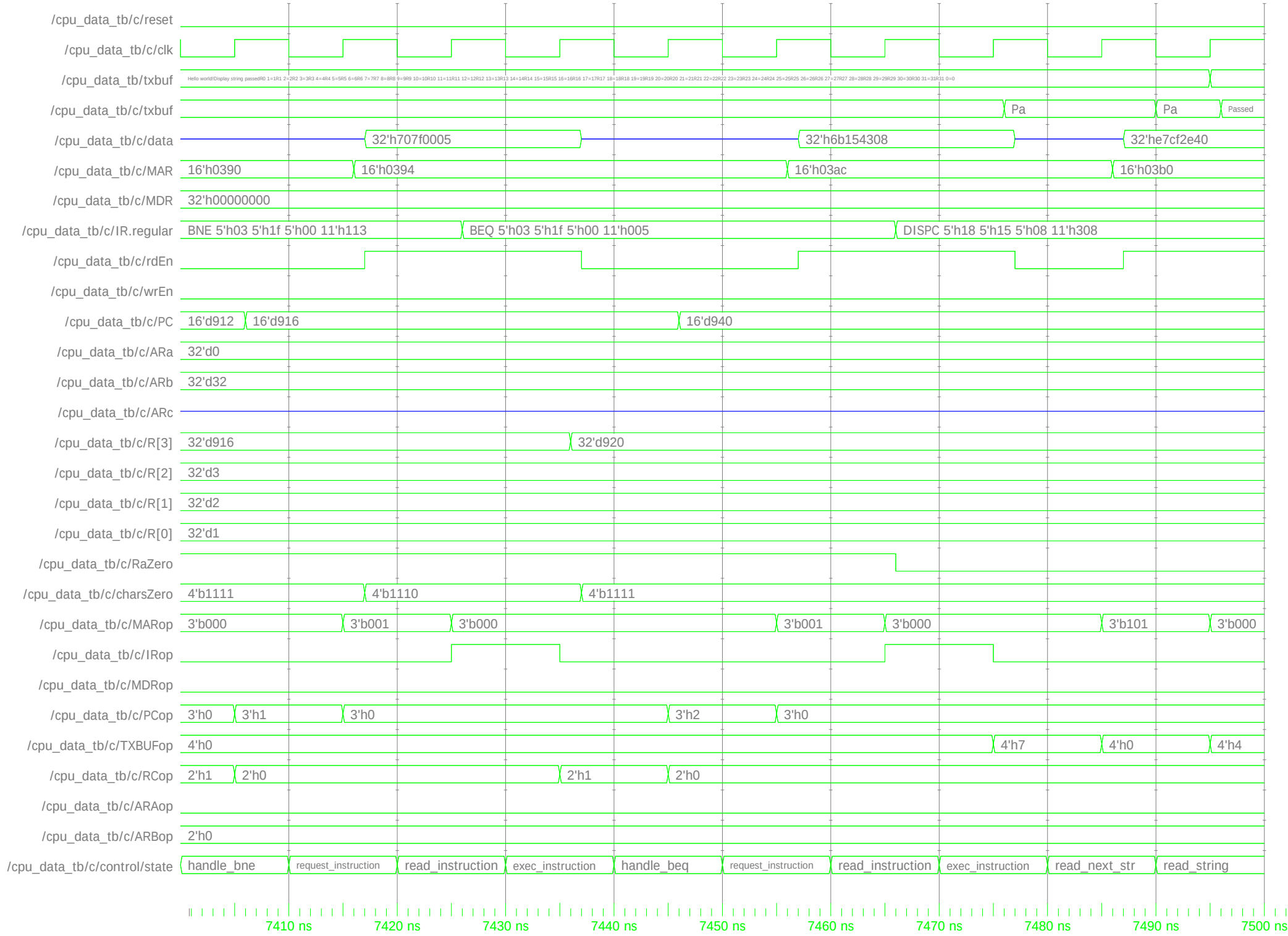


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 72 Page: 72

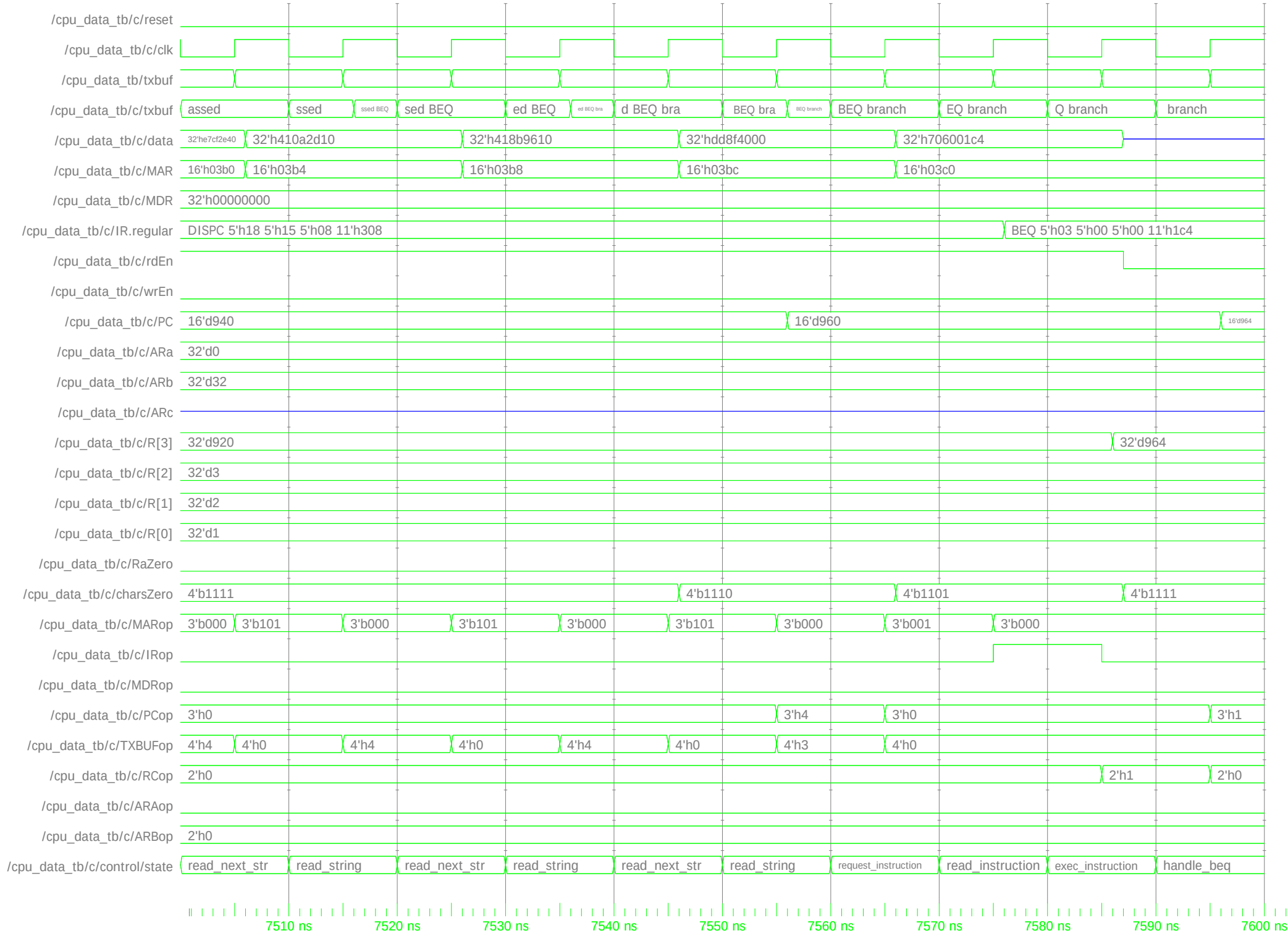


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 73 Page: 73

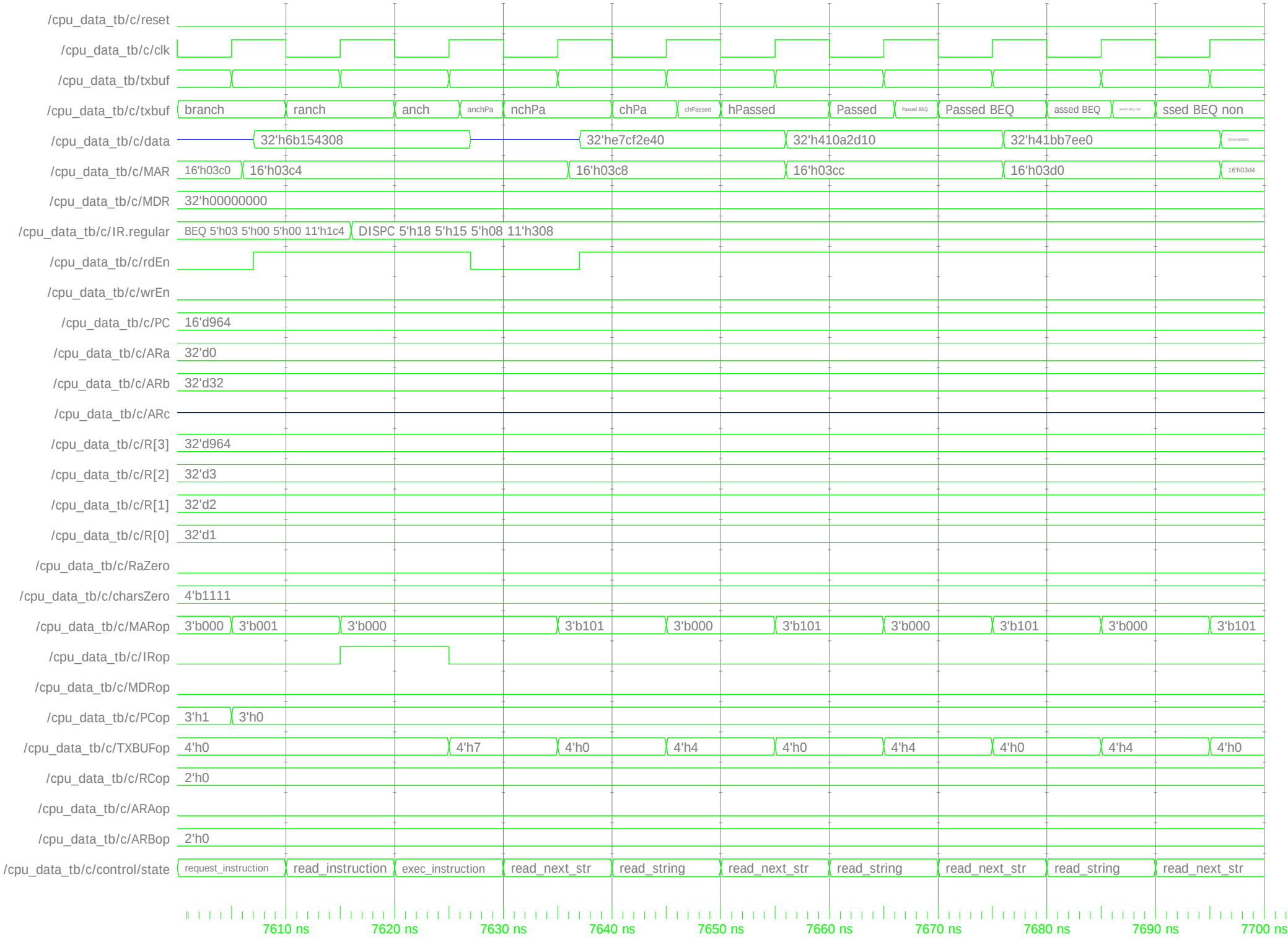

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/txbuf
R3
R31 0=
31 0=
1 0=
0=
0=
=
=0
0
/cpu_data_tb/c/data
32'h628183d0
32'h00000000
32'h783f0000
32'h747f0113
/cpu_data_tb/c/MAR
16'h0384
16'h0388
16'h038c
16'h0390
/cpu_data_tb/c/MDR
32'h00000000
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h198
DISP 5'h01 5'h1f 5'h00 11'h000
BNE 5'h03 5'h1f 5'h00 11'h113
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd896
16'd908
16'd912
/cpu_data_tb/c/ARa
32'd0
/cpu_data_tb/c/ARb
32'd32
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd892
32'd916
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd1
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b0000
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h4
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h1
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
7310 ns
7320 ns
7330 ns
7340 ns
7350 ns
7360 ns
7370 ns
7380 ns
7390 ns
7400 ns



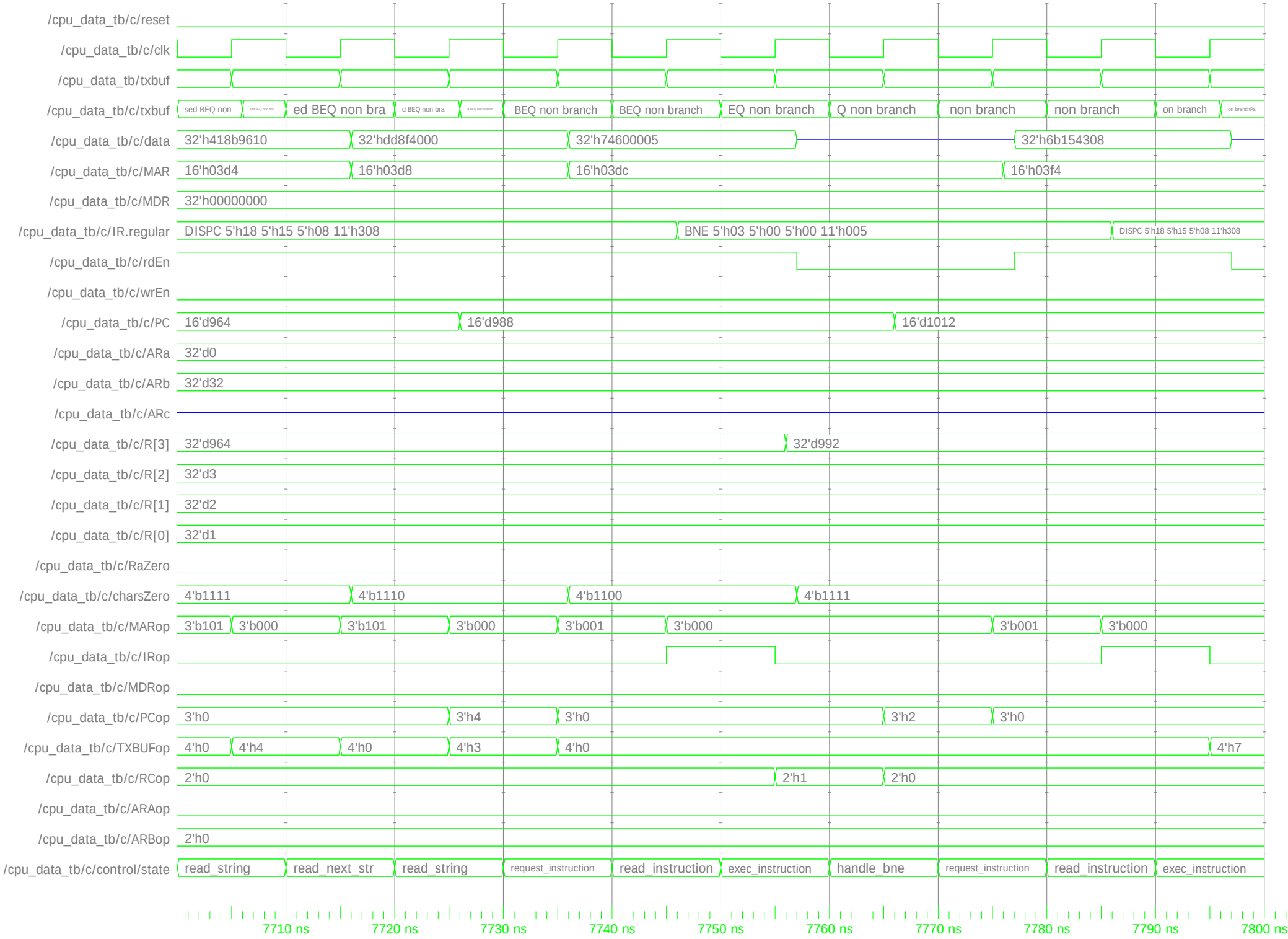
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 75 Page: 75



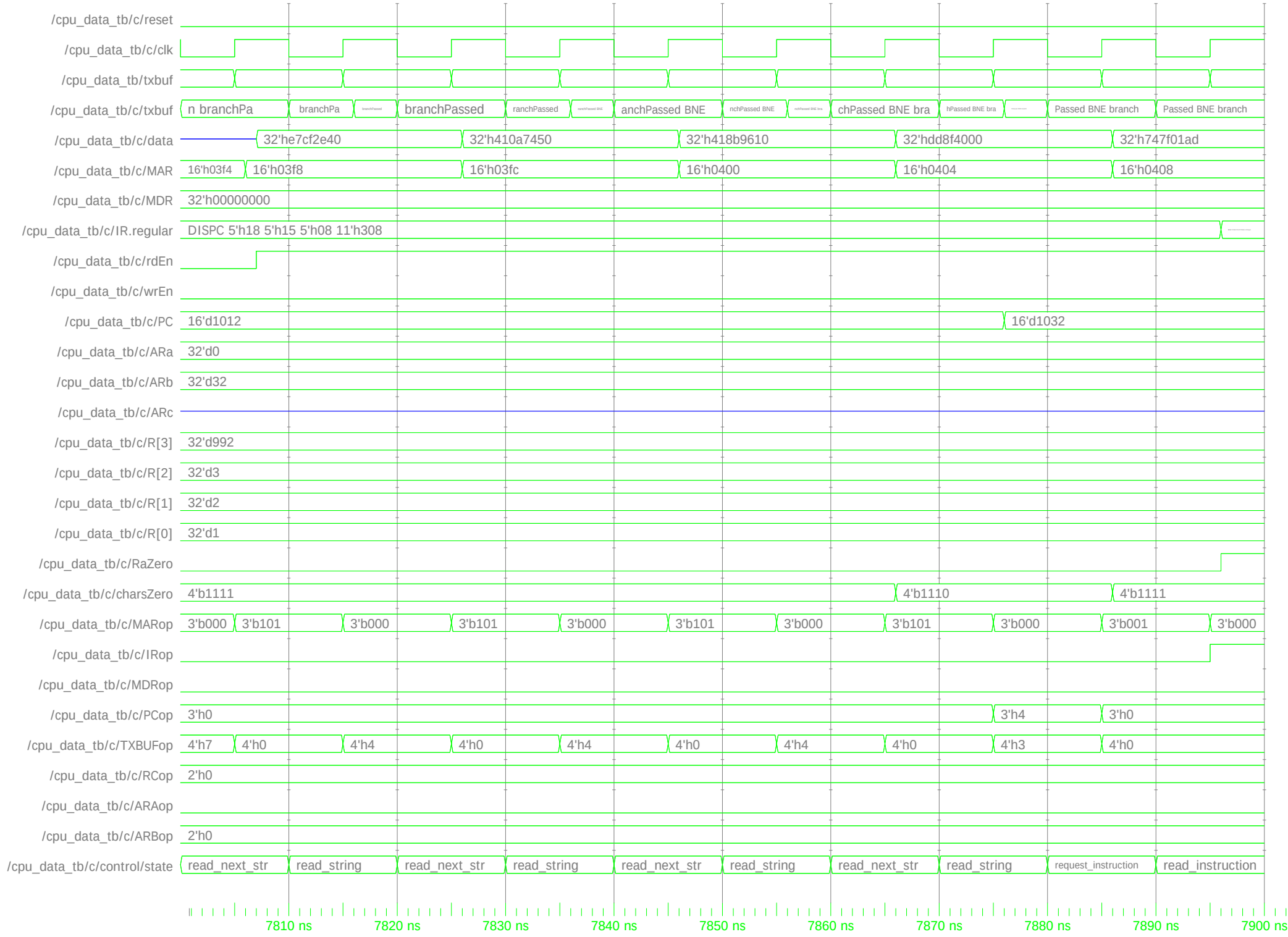
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 76 Page: 76



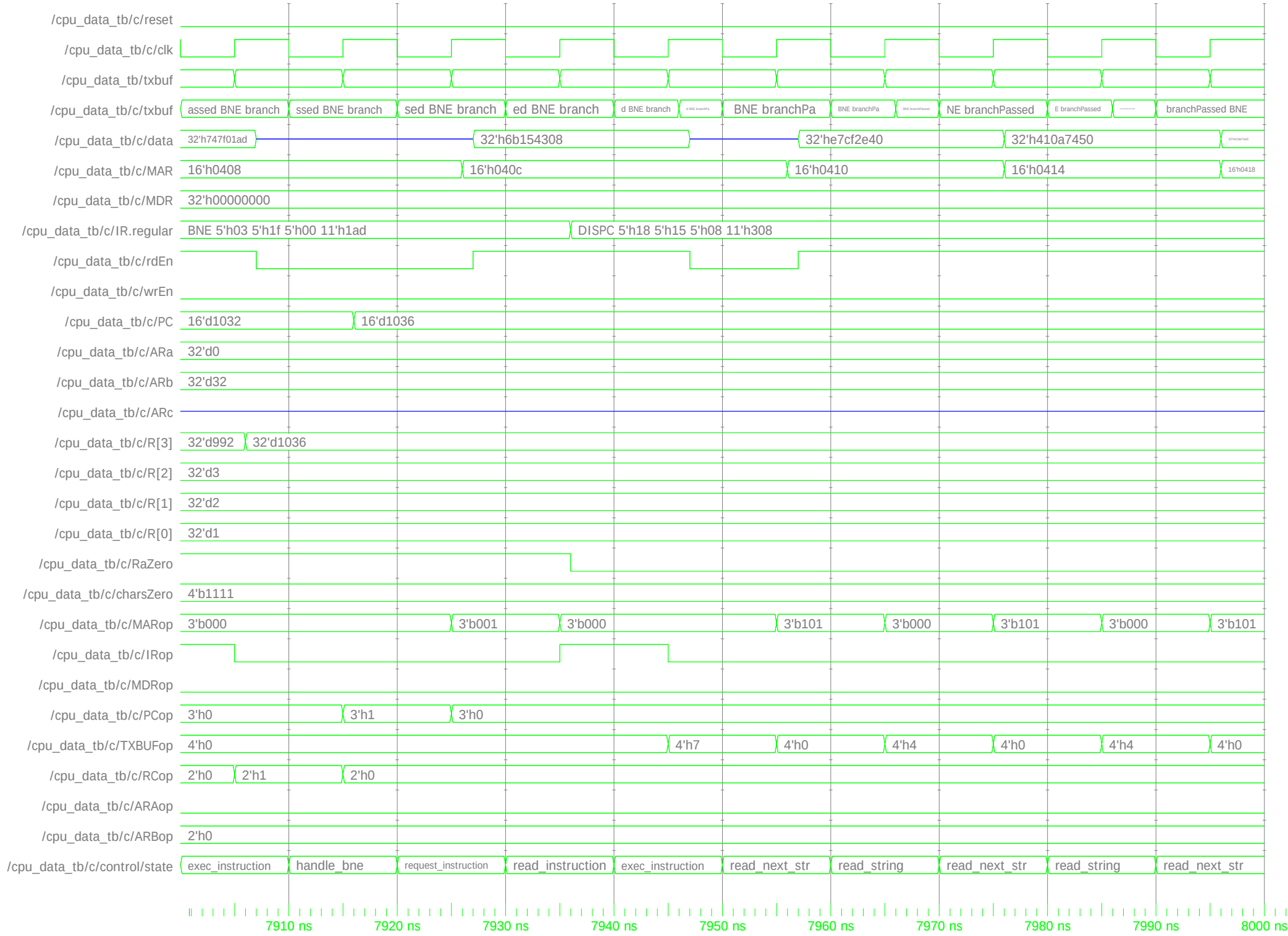
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 77 Page: 77



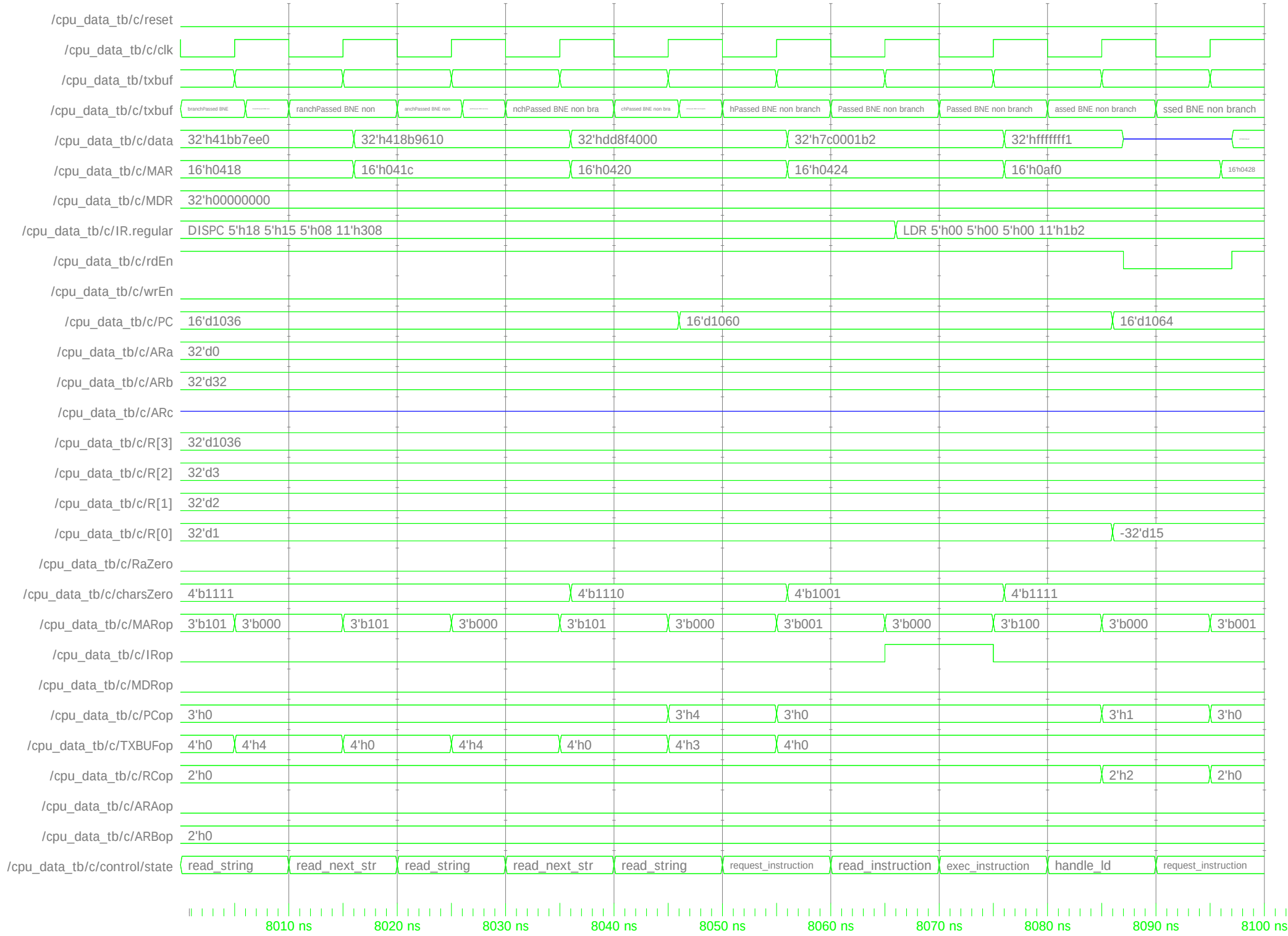
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 78 Page: 78



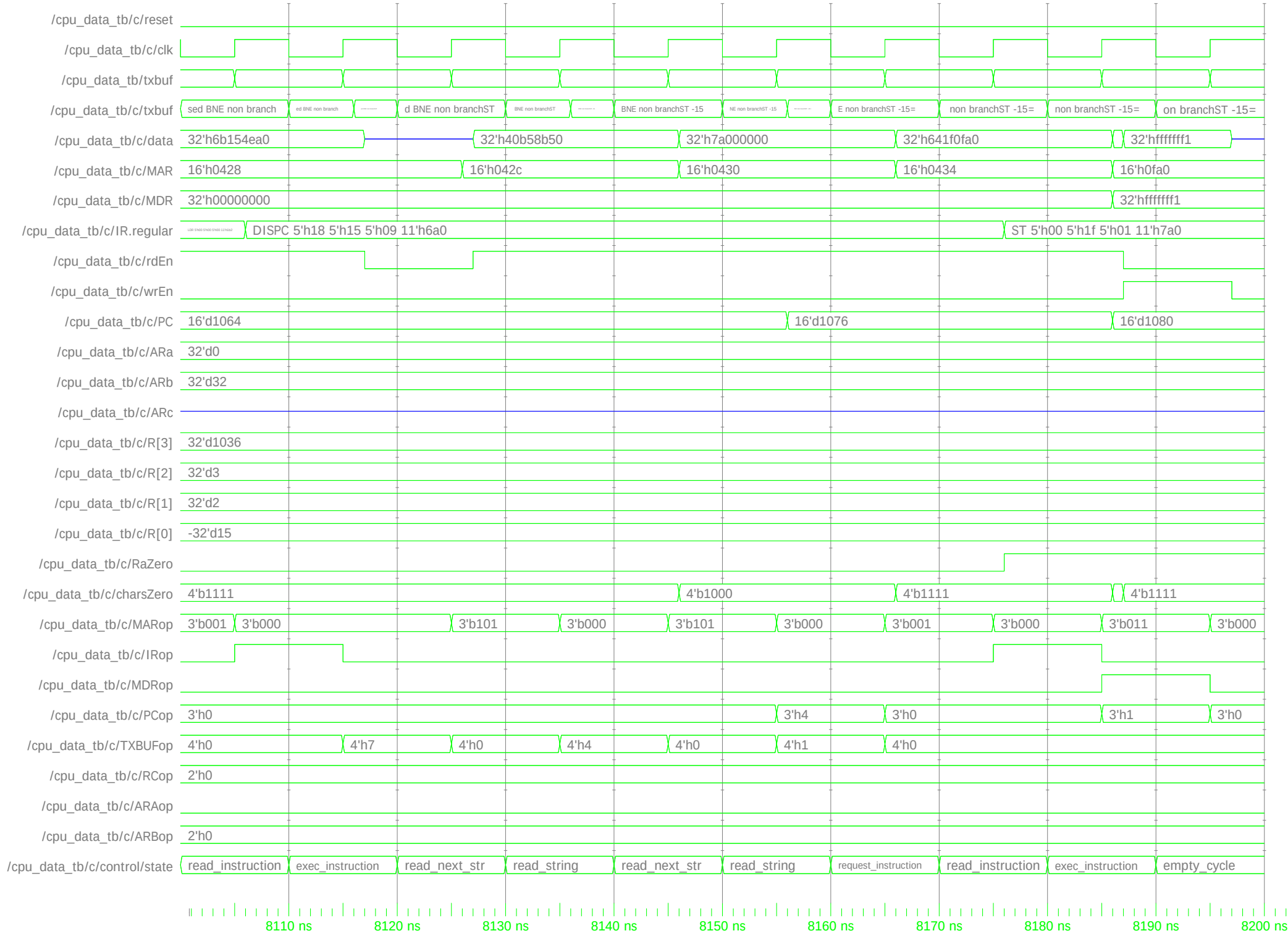
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 79 Page: 79



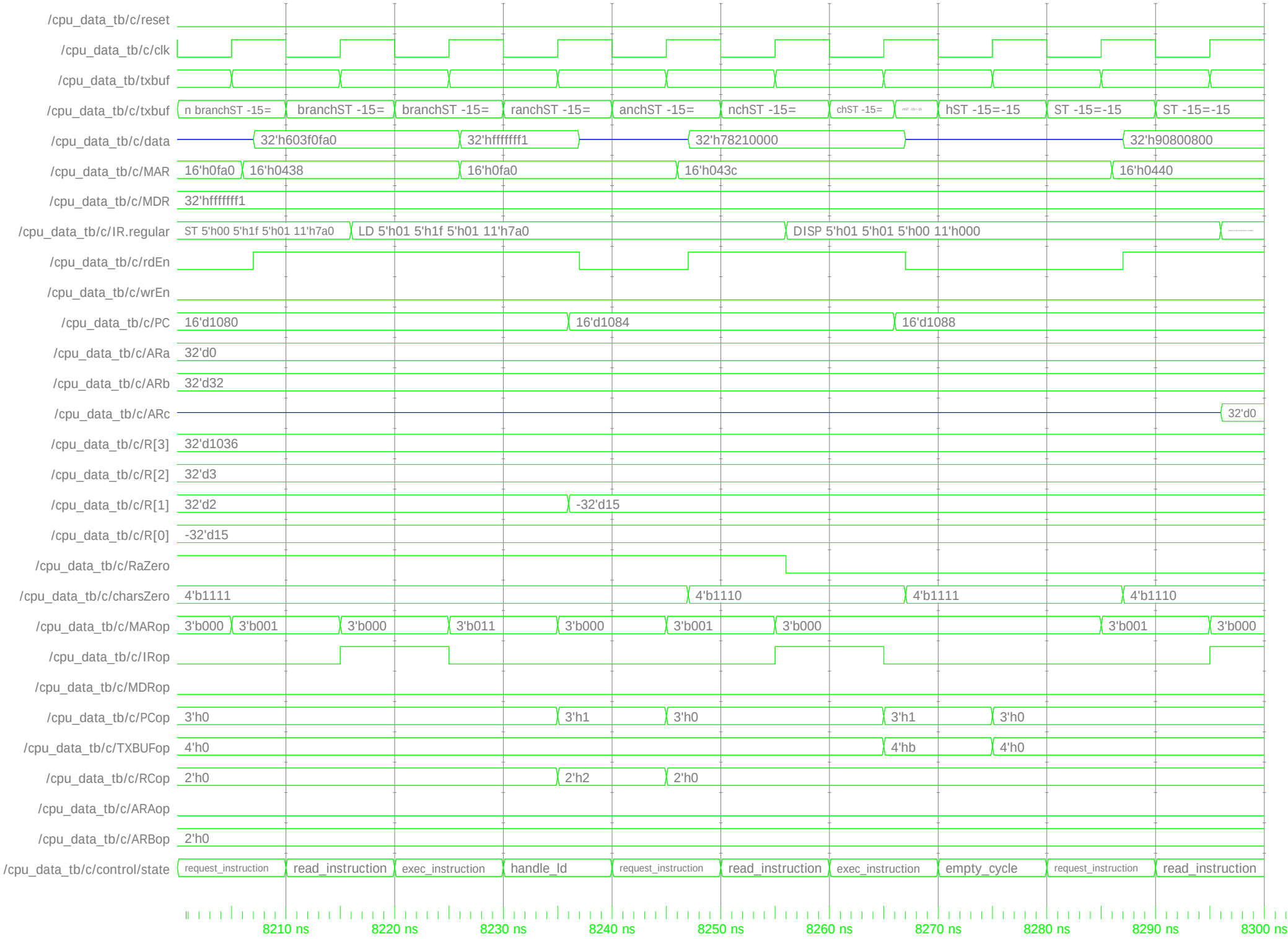
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 80 Page: 80

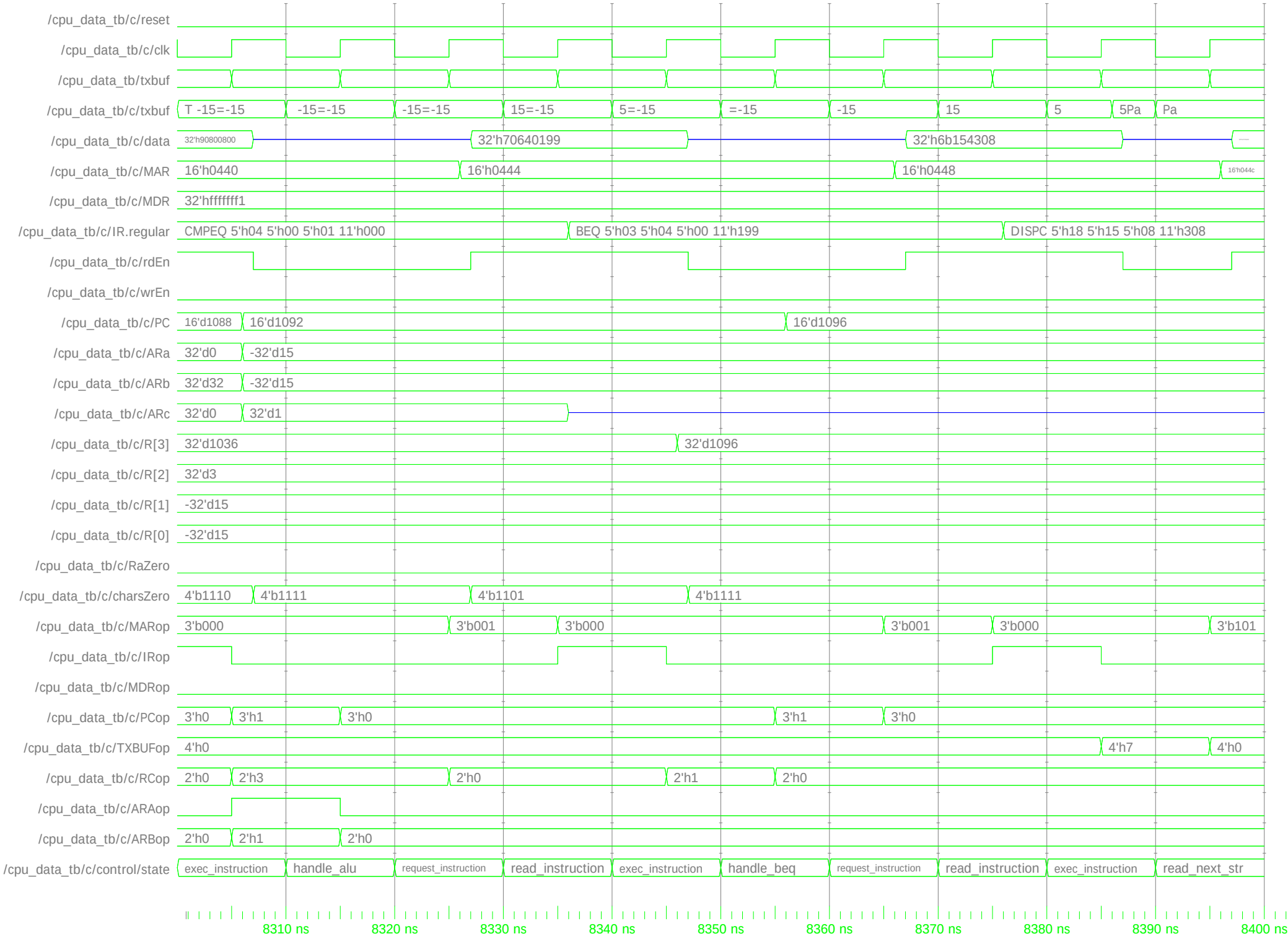


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 81 Page: 81

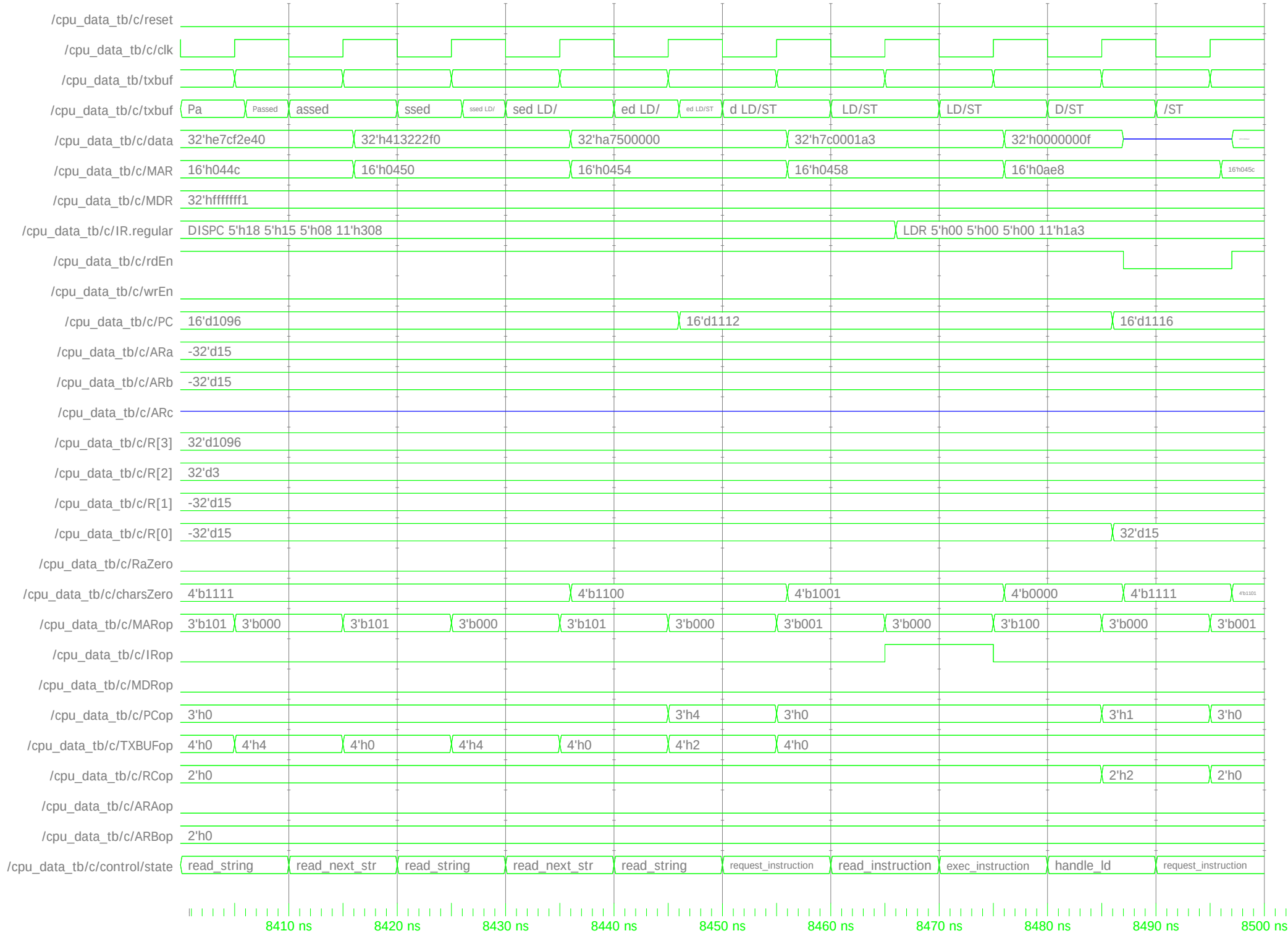


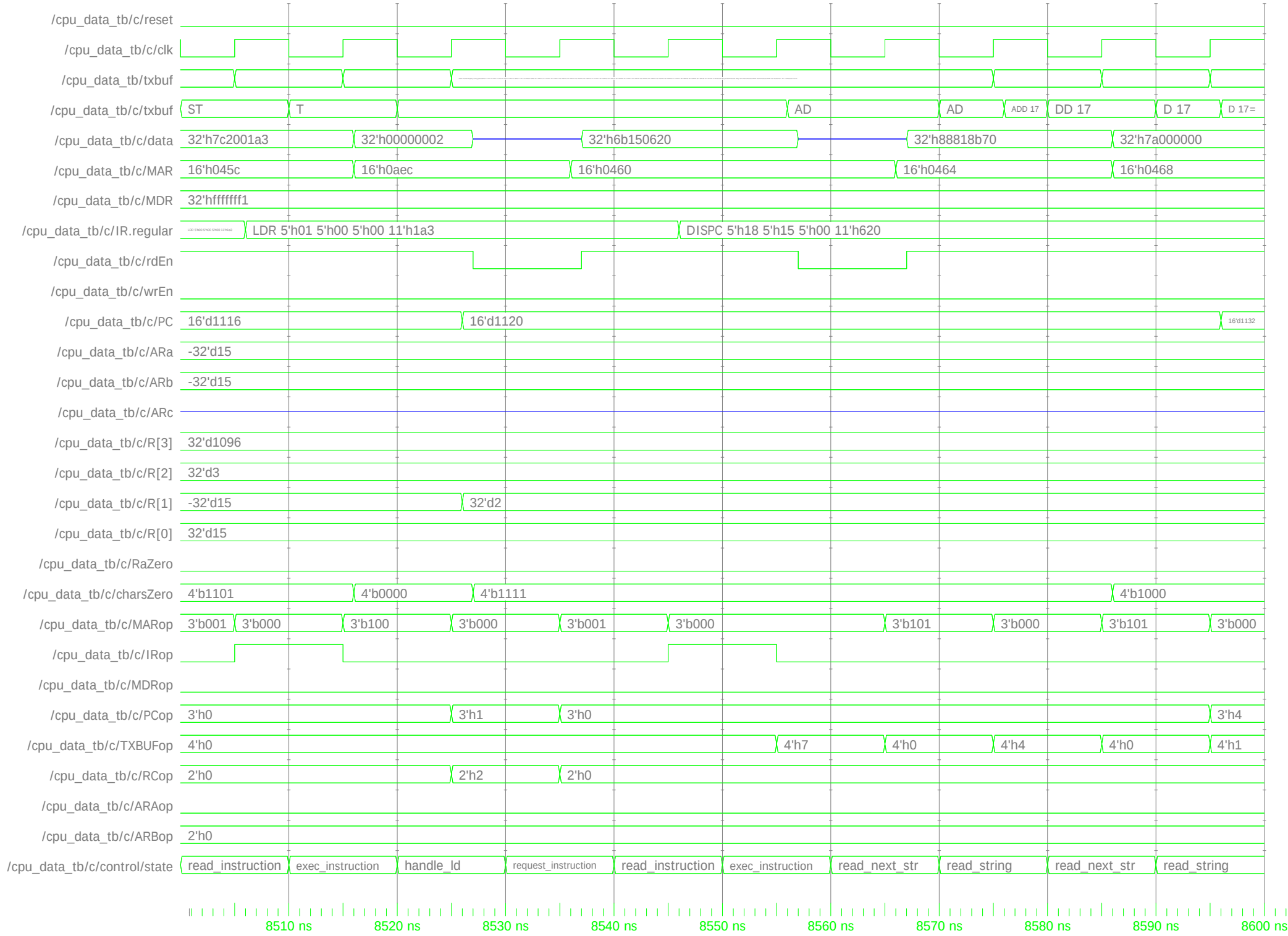
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 82 Page: 82

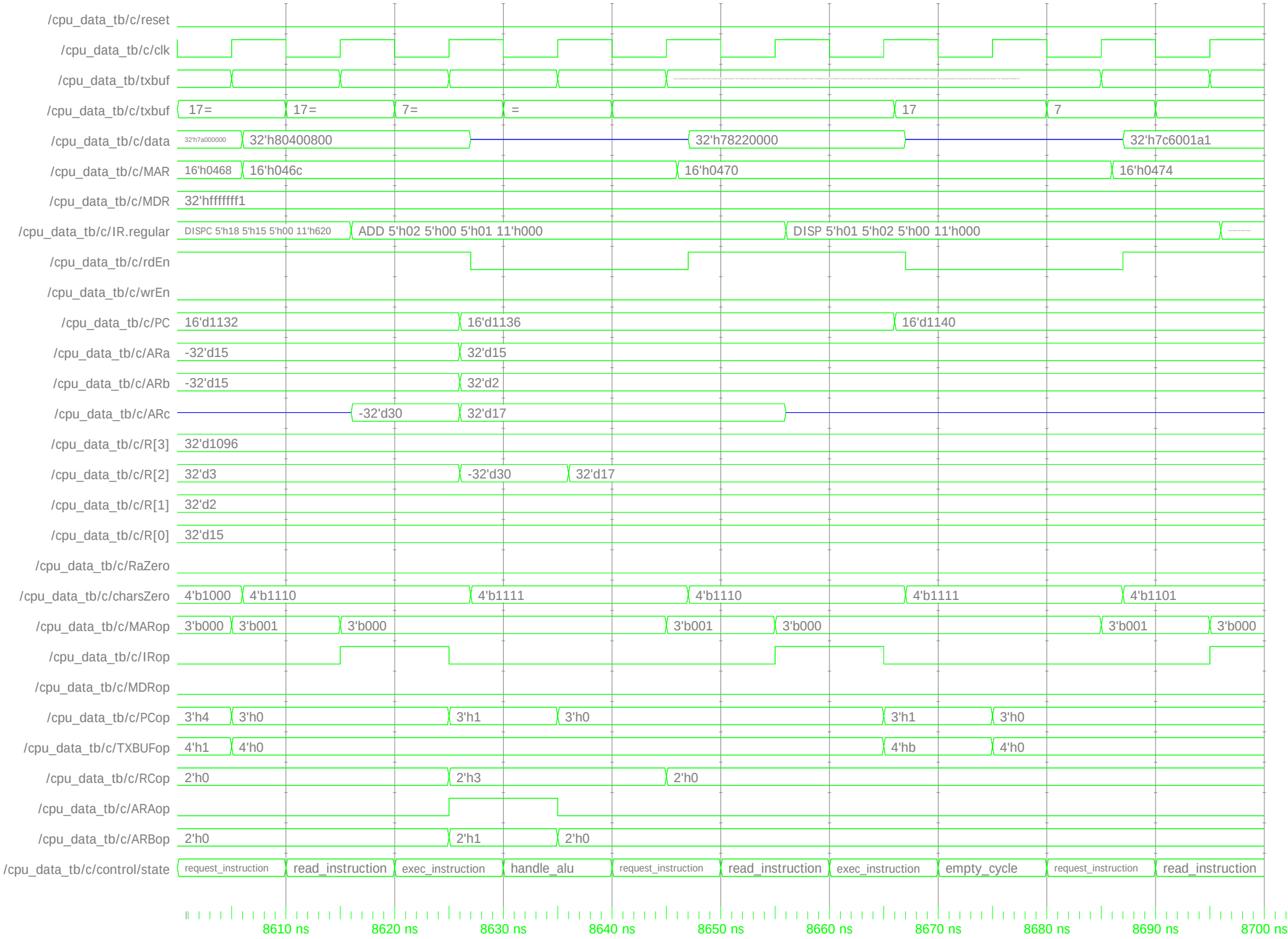

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
n branchST -15=
branchST -15=
branchST -15=
ranchST -15=
anchST -15=
nchST -15=
chST -15=
hST -15=-15
ST -15=-15
ST -15=-15
/cpu_data_tb/c/data
32'h603f0fa0
32'hffffffff1
32'h78210000
32'h90800800
/cpu_data_tb/c/MAR
16'h0fa0
16'h0438
16'h0fa0
16'h043c
16'h0440
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
ST 5'h00 5'h1f 5'h01 11'h7a0
LD 5'h01 5'h1f 5'h01 11'h7a0
DISP 5'h01 5'h01 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1080
16'd1084
16'd1088
/cpu_data_tb/c/ARa
32'd0
/cpu_data_tb/c/ARb
32'd32
/cpu_data_tb/c/ARc
32'd0
/cpu_data_tb/c/R[3]
32'd1036
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
-32'd15
/cpu_data_tb/c/R[0]
-32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1110
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b011
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
8210 ns
8220 ns
8230 ns
8240 ns
8250 ns
8260 ns
8270 ns
8280 ns
8290 ns
8300 ns



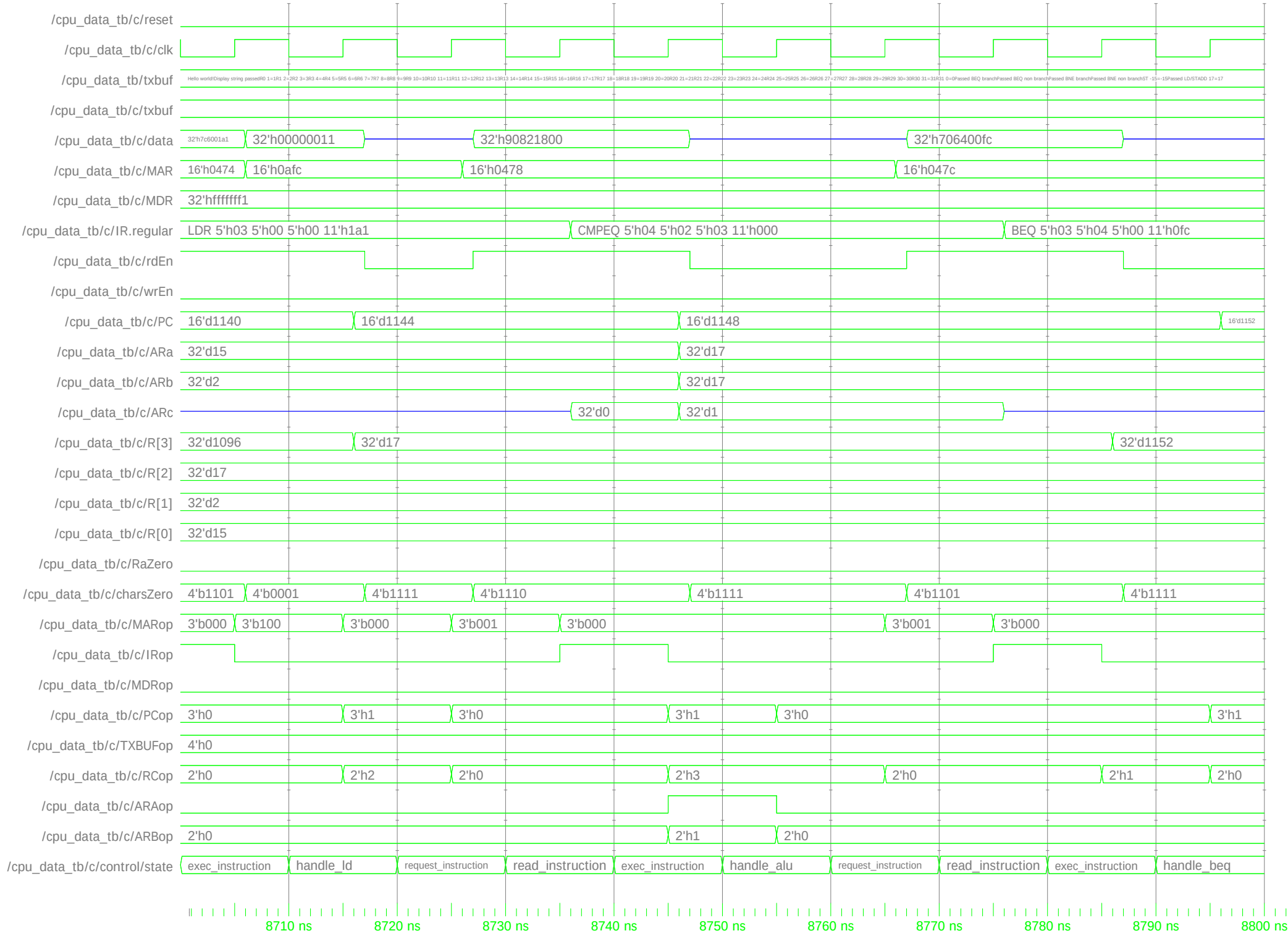
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 84 Page: 84


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
Pa
Passed
assed
ssed
ssed LD/
sed LD/
ed LD/
ed LD/ST
d LD/ST
LD/ST
LD/ST
D/ST
/ST
/cpu_data_tb/c/data
32'he7cf2e40
32'h413222f0
32'ha7500000
32'h7c0001a3
32'h0000000f
/cpu_data_tb/c/MAR
16'h044c
16'h0450
16'h0454
16'h0458
16'h0ae8
16'h045c
/cpu_data_tb/c/MDR
32'hffffffff
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h08 11'h308
LDR 5'h00 5'h00 5'h00 11'h1a3
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1096
16'd1112
16'd1116
/cpu_data_tb/c/ARa
-32'd15
/cpu_data_tb/c/ARb
-32'd15
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd1096
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
-32'd15
/cpu_data_tb/c/R[0]
-32'd15
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1100
4'b1001
4'b0000
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b100
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h4
4'h0
4'h4
4'h0
4'h2
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_string
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
handle_ld
request_instruction
8410 ns
8420 ns
8430 ns
8440 ns
8450 ns
8460 ns
8470 ns
8480 ns
8490 ns
8500 ns

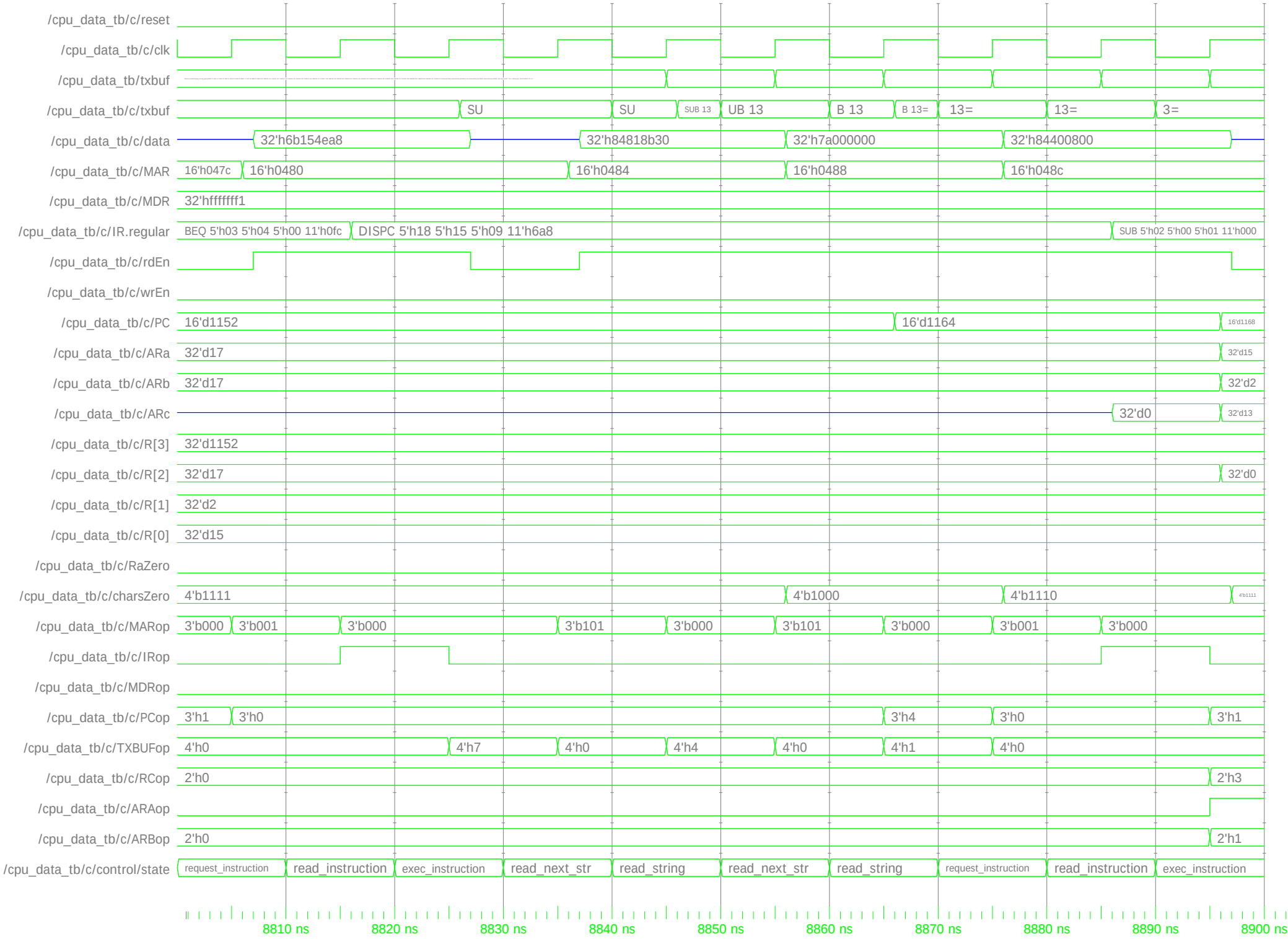

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
ST
T
AD
AD
ADD 17
DD 17
D 17
D 17=
/cpu_data_tb/c/data
32'h7c2001a3
32'h00000002
32'h6b150620
32'h88818b70
32'h7a000000
/cpu_data_tb/c/MAR
16'h045c
16'h0aec
16'h0460
16'h0464
16'h0468
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h01 5'h00 5'h00 11'h1a3
DISPC 5'h18 5'h15 5'h00 11'h620
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1116
16'd1120
16'd1132
/cpu_data_tb/c/ARa
-32'd15
/cpu_data_tb/c/ARb
-32'd15
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd1096
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
-32'd15
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b0000
4'b1111
4'b1000
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
8510 ns
8520 ns
8530 ns
8540 ns
8550 ns
8560 ns
8570 ns
8580 ns
8590 ns
8600 ns



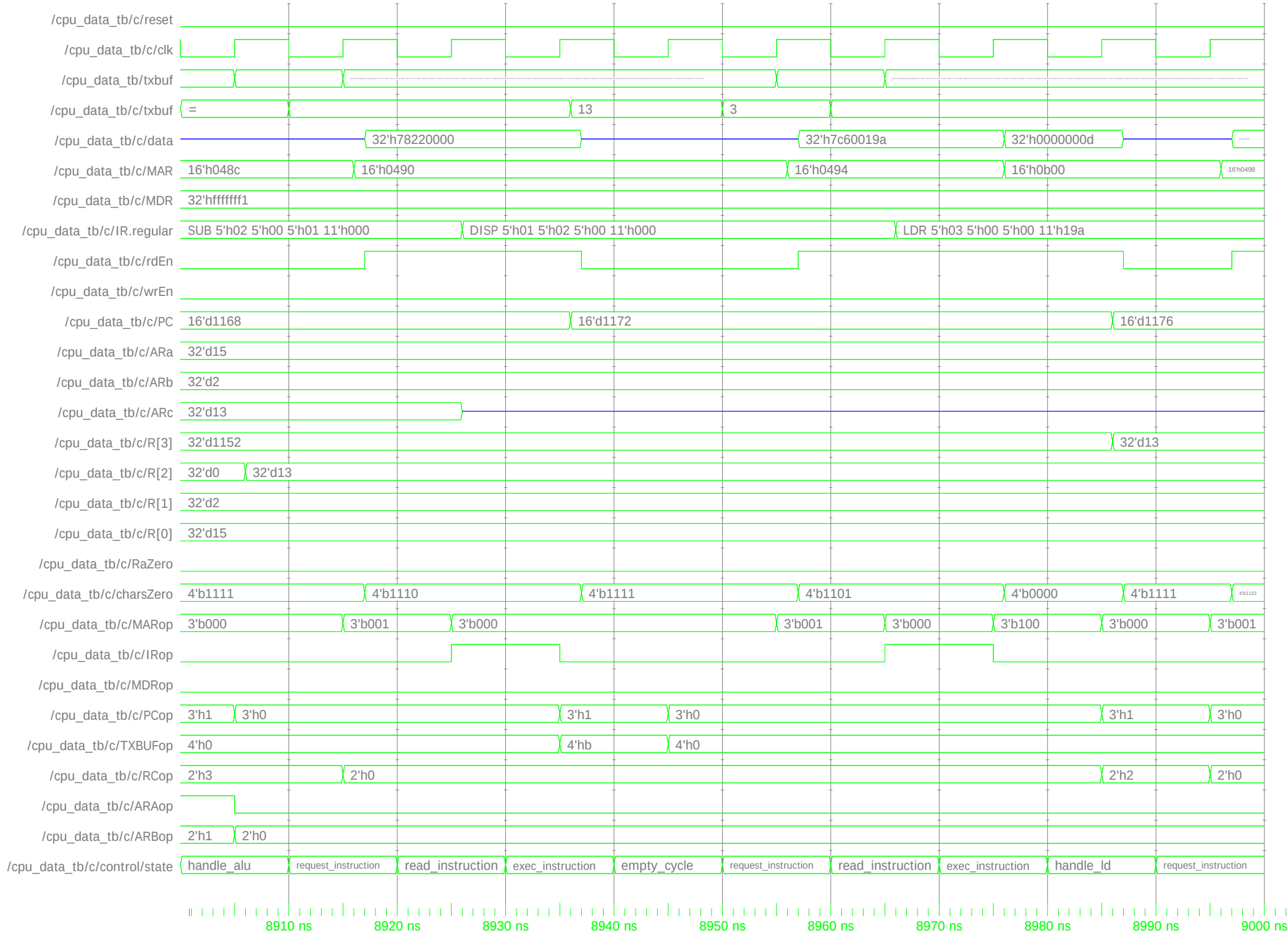
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 87 Page: 87



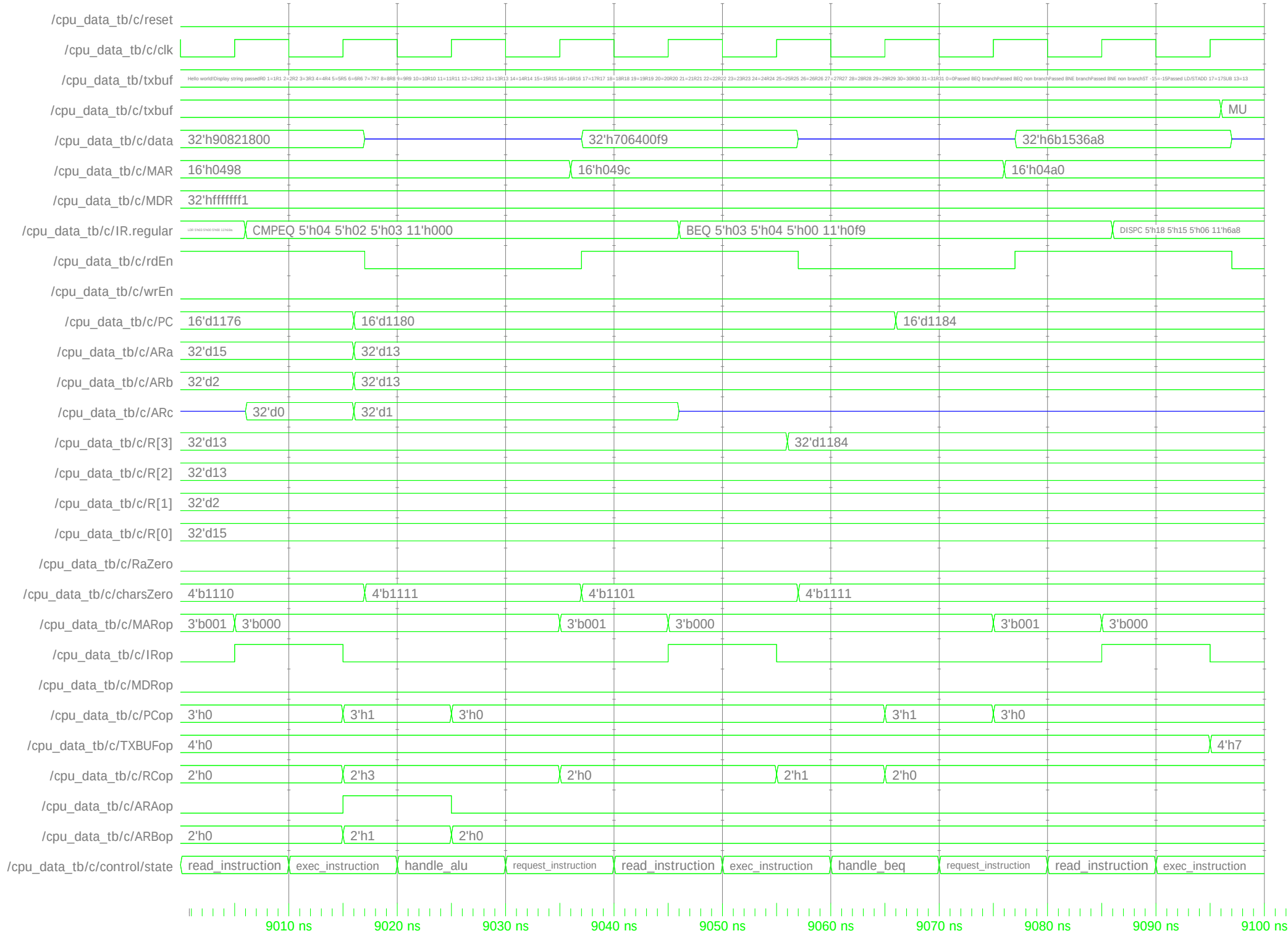
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 88 Page: 88



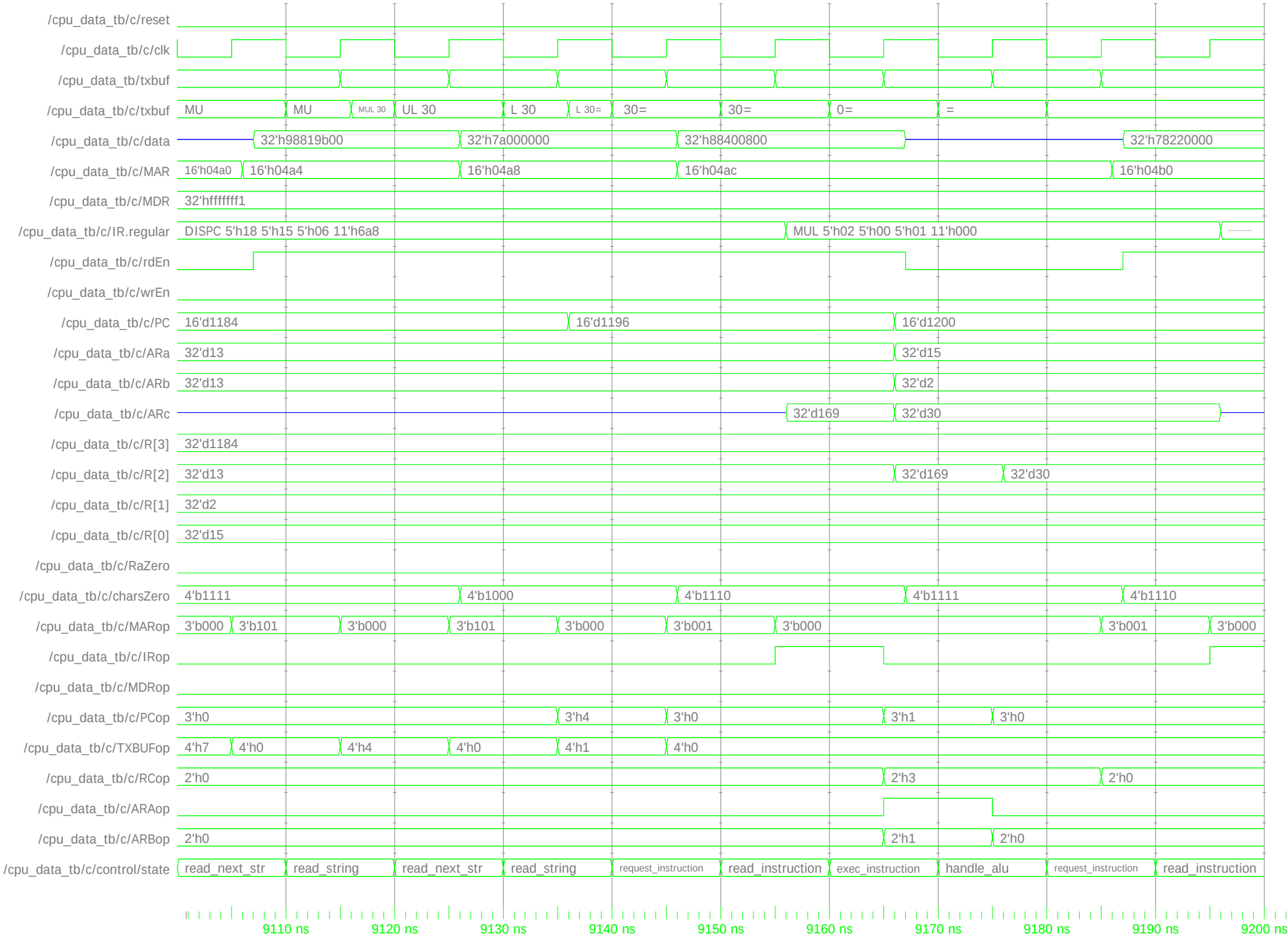
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 89 Page: 89

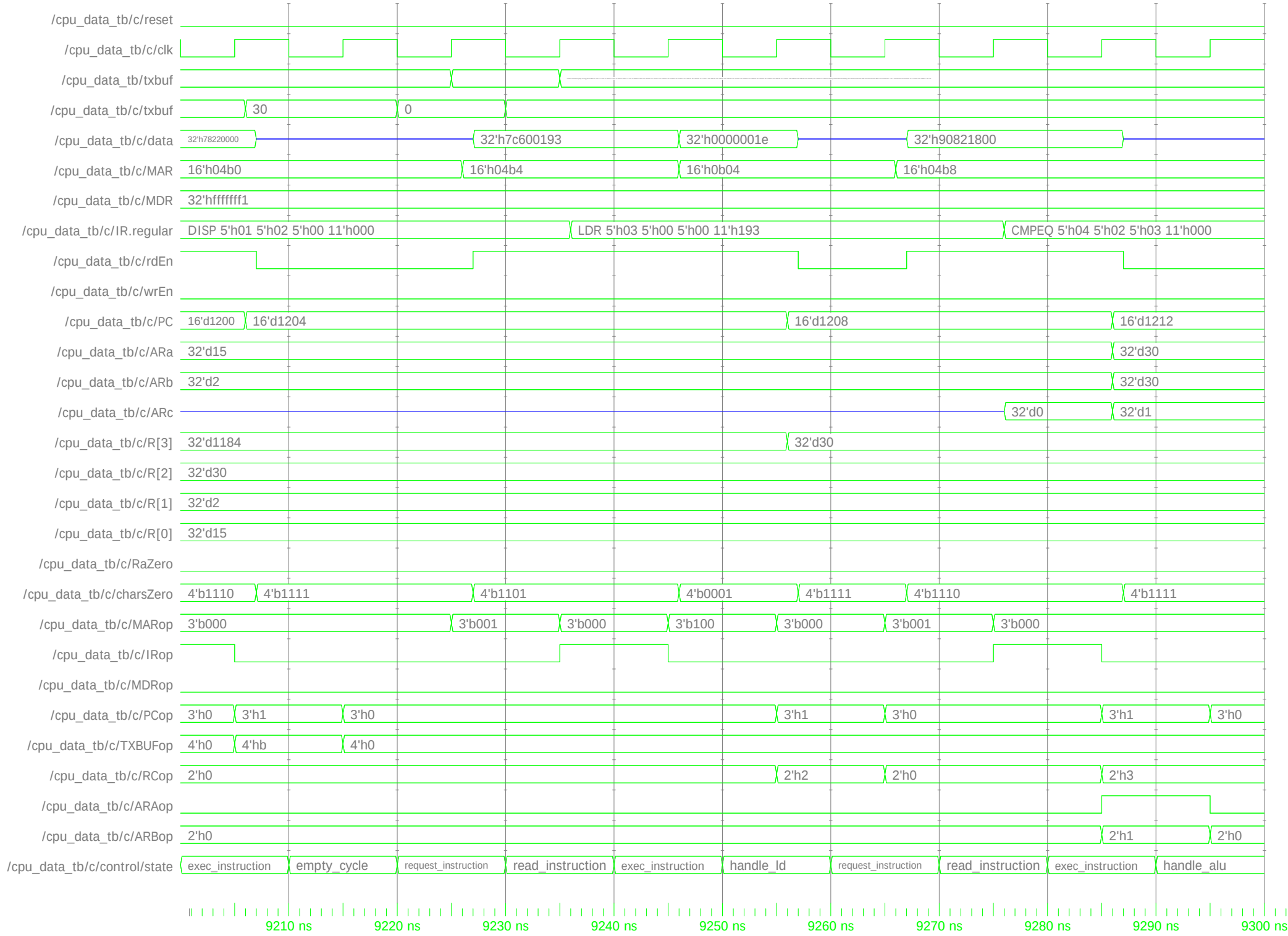


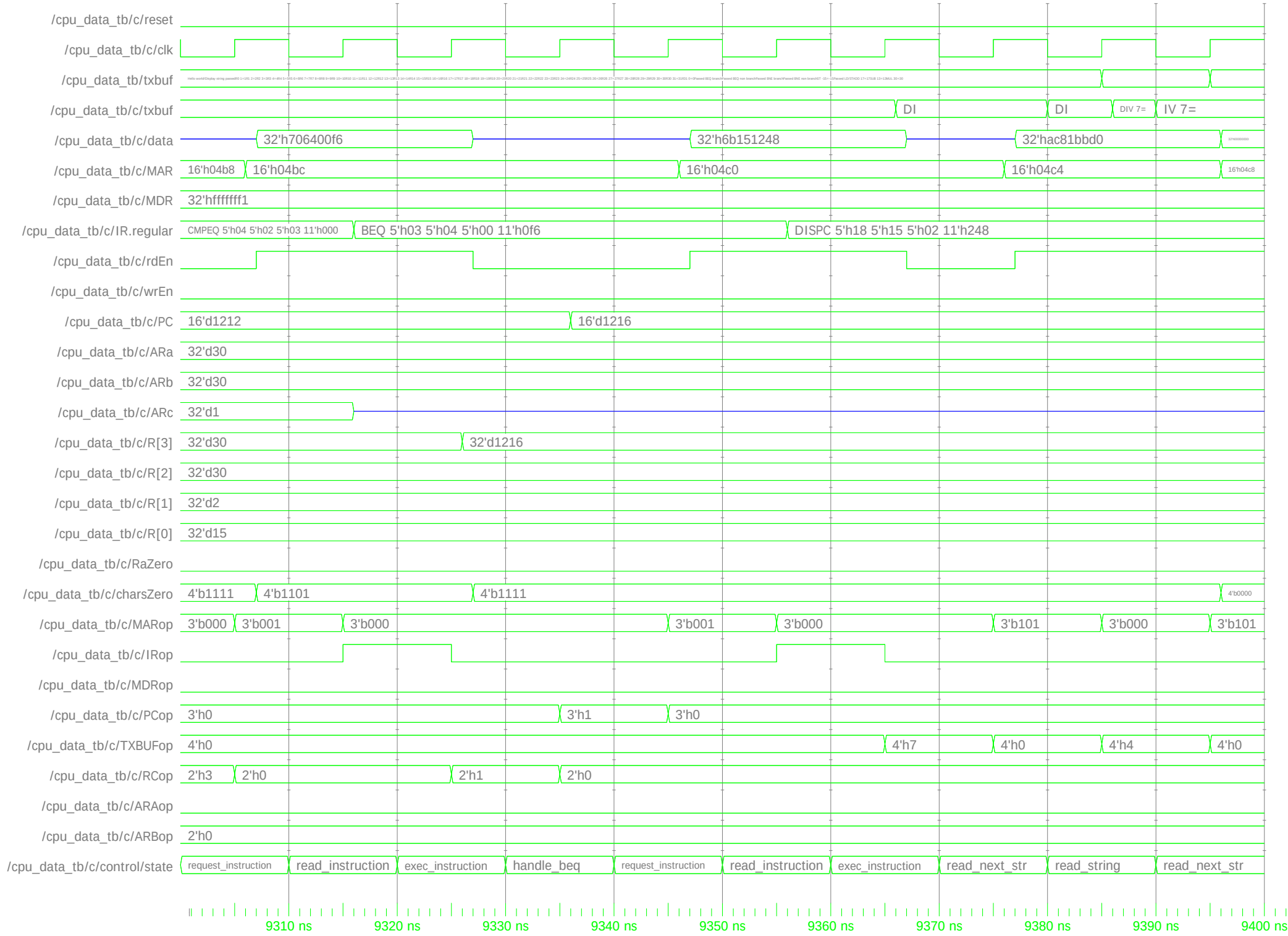
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 90 Page: 90



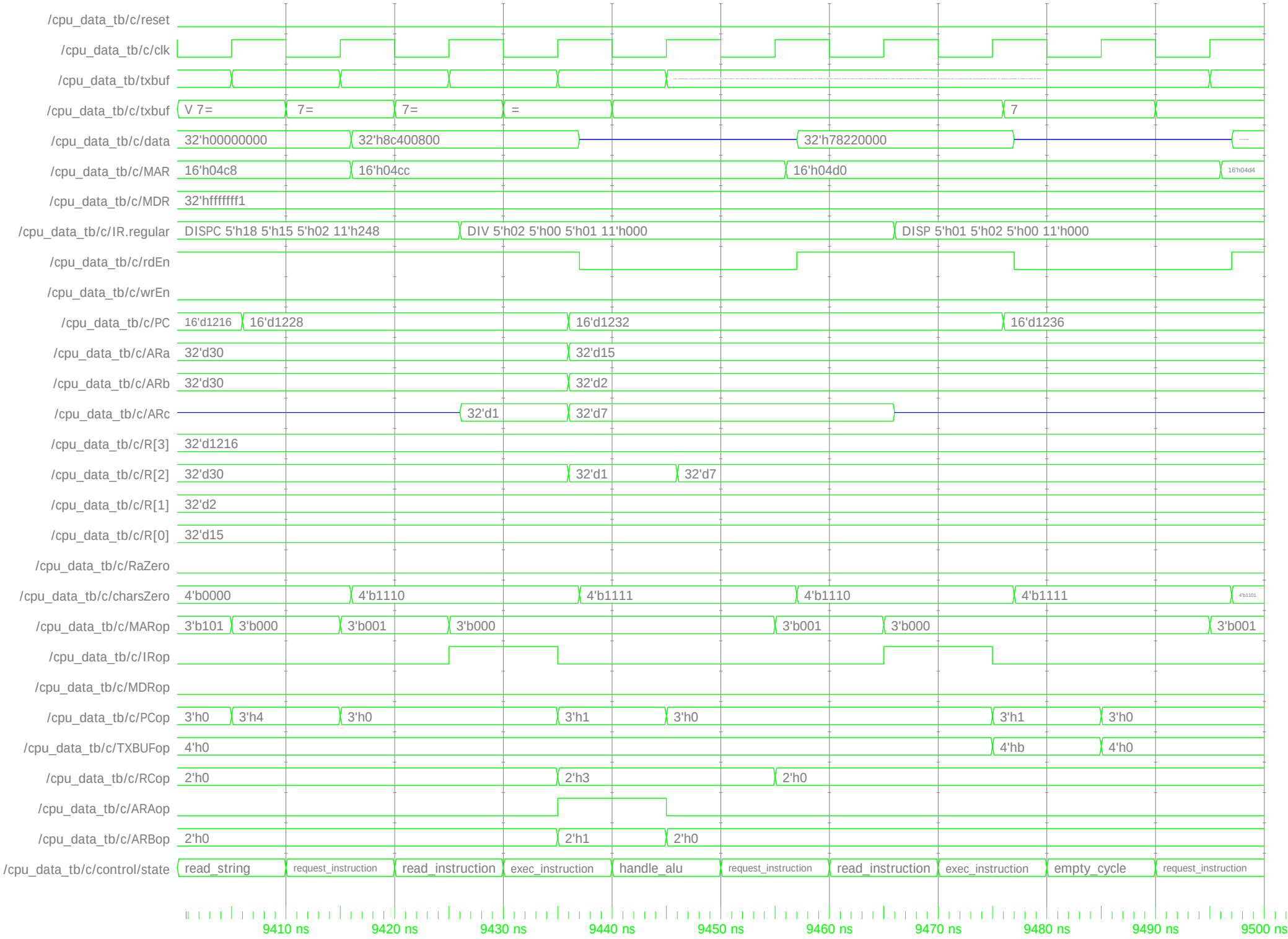
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 91 Page: 91

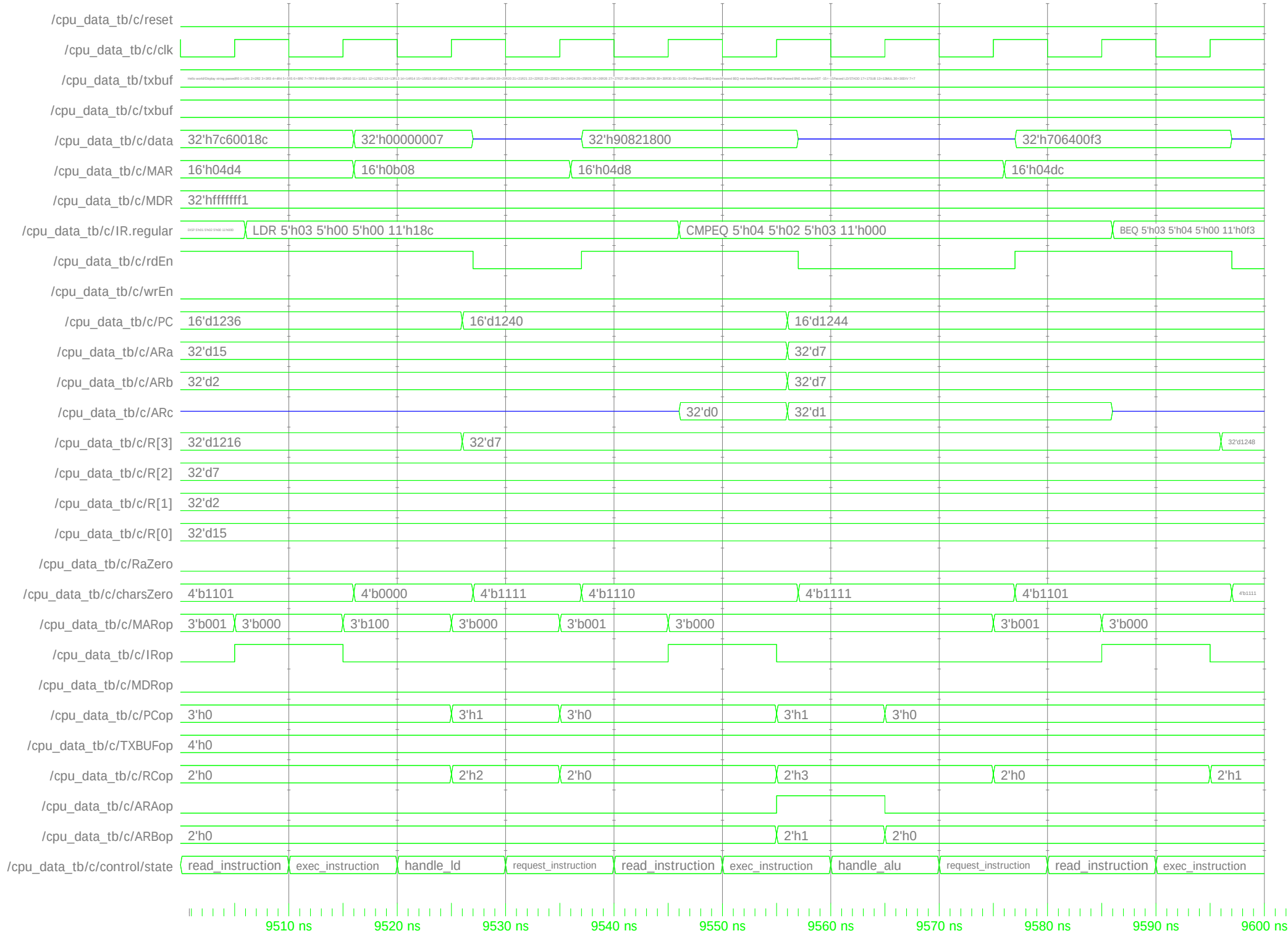

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
MU
MU
MUL 30
UL 30
L 30
L 30=
30=
30=
0=
=
/cpu_data_tb/c/data
32'h98819b00
32'h7a000000
32'h88400800
32'h78220000
/cpu_data_tb/c/MAR
16'h04a0
16'h04a4
16'h04a8
16'h04ac
16'h04b0
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h06 11'h6a8
MUL 5'h02 5'h00 5'h01 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1184
16'd1196
16'd1200
/cpu_data_tb/c/ARa
32'd13
32'd15
/cpu_data_tb/c/ARb
32'd13
32'd2
/cpu_data_tb/c/ARc
32'd169
32'd30
/cpu_data_tb/c/R[3]
32'd1184
/cpu_data_tb/c/R[2]
32'd13
32'd169
32'd30
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1110
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
9110 ns
9120 ns
9130 ns
9140 ns
9150 ns
9160 ns
9170 ns
9180 ns
9190 ns
9200 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
30
0
/cpu_data_tb/c/data
32'h78220000
32'h7c600193
32'h0000001e
32'h90821800
/cpu_data_tb/c/MAR
16'h04b0
16'h04b4
16'h0b04
16'h04b8
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h02 5'h00 11'h000
LDR 5'h03 5'h00 5'h00 11'h193
CMPEQ 5'h04 5'h02 5'h03 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1200
16'd1204
16'd1208
16'd1212
/cpu_data_tb/c/ARa
32'd15
32'd30
/cpu_data_tb/c/ARb
32'd2
32'd30
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1184
32'd30
/cpu_data_tb/c/R[2]
32'd30
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1101
4'b0001
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
9210 ns
9220 ns
9230 ns
9240 ns
9250 ns
9260 ns
9270 ns
9280 ns
9290 ns
9300 ns

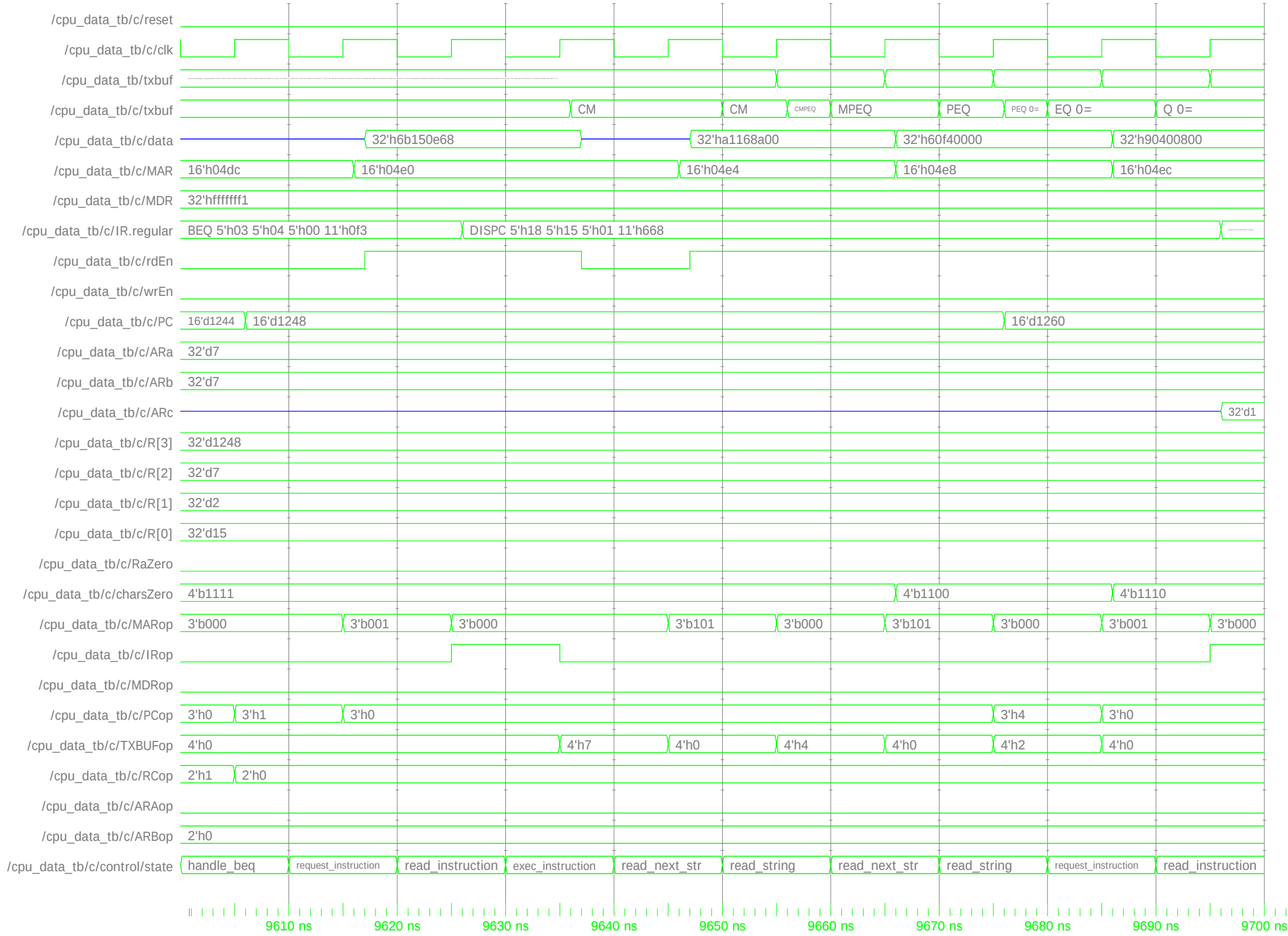


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 94 Page: 94

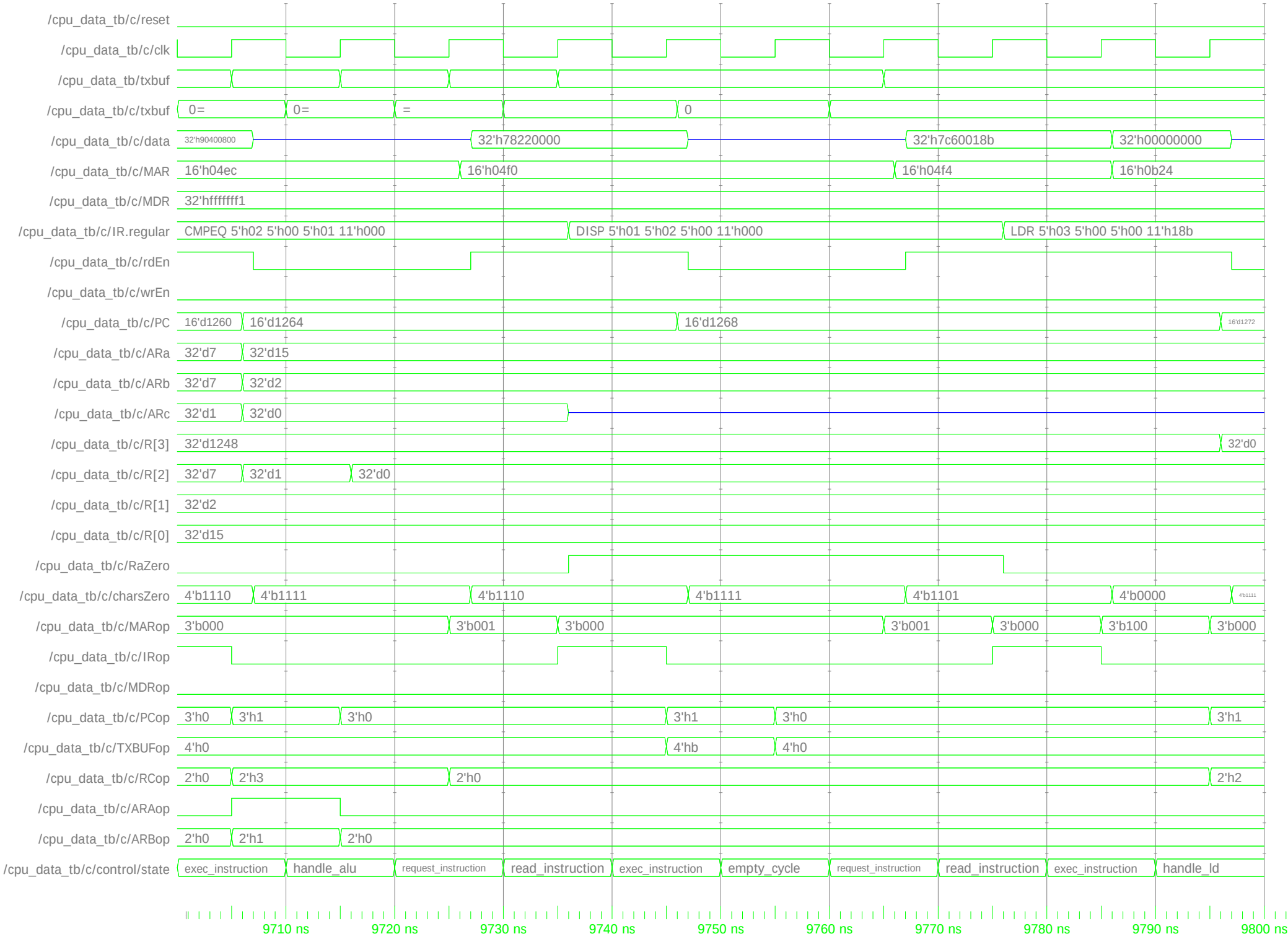

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
V 7= 7= 7= = 7
/cpu_data_tb/c/data
32'h00000000 32'h8c400800 32'h78220000
/cpu_data_tb/c/MAR
16'h04c8 16'h04cc 16'h04d0 16'h04d4
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h02 11'h248
DIV 5'h02 5'h00 5'h01 11'h000
DISP 5'h01 5'h02 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1216 16'd1228 16'd1232 16'd1236
/cpu_data_tb/c/ARa
32'd30 32'd15
/cpu_data_tb/c/ARb
32'd30 32'd2
/cpu_data_tb/c/ARc
32'd1 32'd7
/cpu_data_tb/c/R[3]
32'd1216
/cpu_data_tb/c/R[2]
32'd30 32'd1 32'd7
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b0000 4'b1110 4'b1111 4'b1110 4'b1111 4'b1101
/cpu_data_tb/c/MARop
3'b101 3'b000 3'b001 3'b000 3'b001 3'b000 3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0 3'h4 3'h0 3'h1 3'h0 3'h1 3'h0
/cpu_data_tb/c/TXBUFop
4'h0 4'hb 4'h0
/cpu_data_tb/c/RCop
2'h0 2'h3 2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0 2'h1 2'h0
/cpu_data_tb/c/control/state
read_string request_instruction read_instruction exec_instruction handle_alu request_instruction read_instruction exec_instruction empty_cycle request_instruction
9410 ns 9420 ns 9430 ns 9440 ns 9450 ns 9460 ns 9470 ns 9480 ns 9490 ns 9500 ns

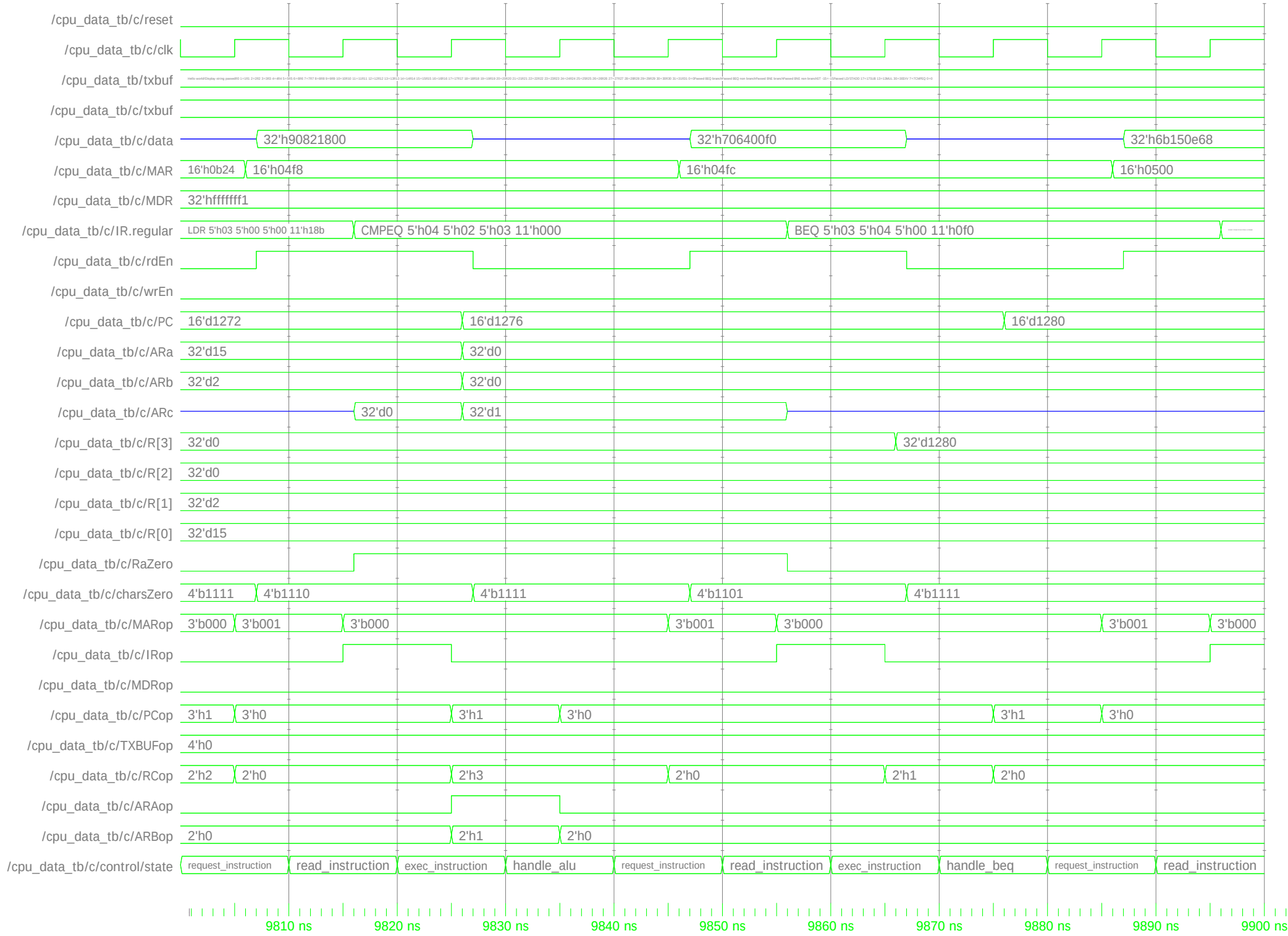


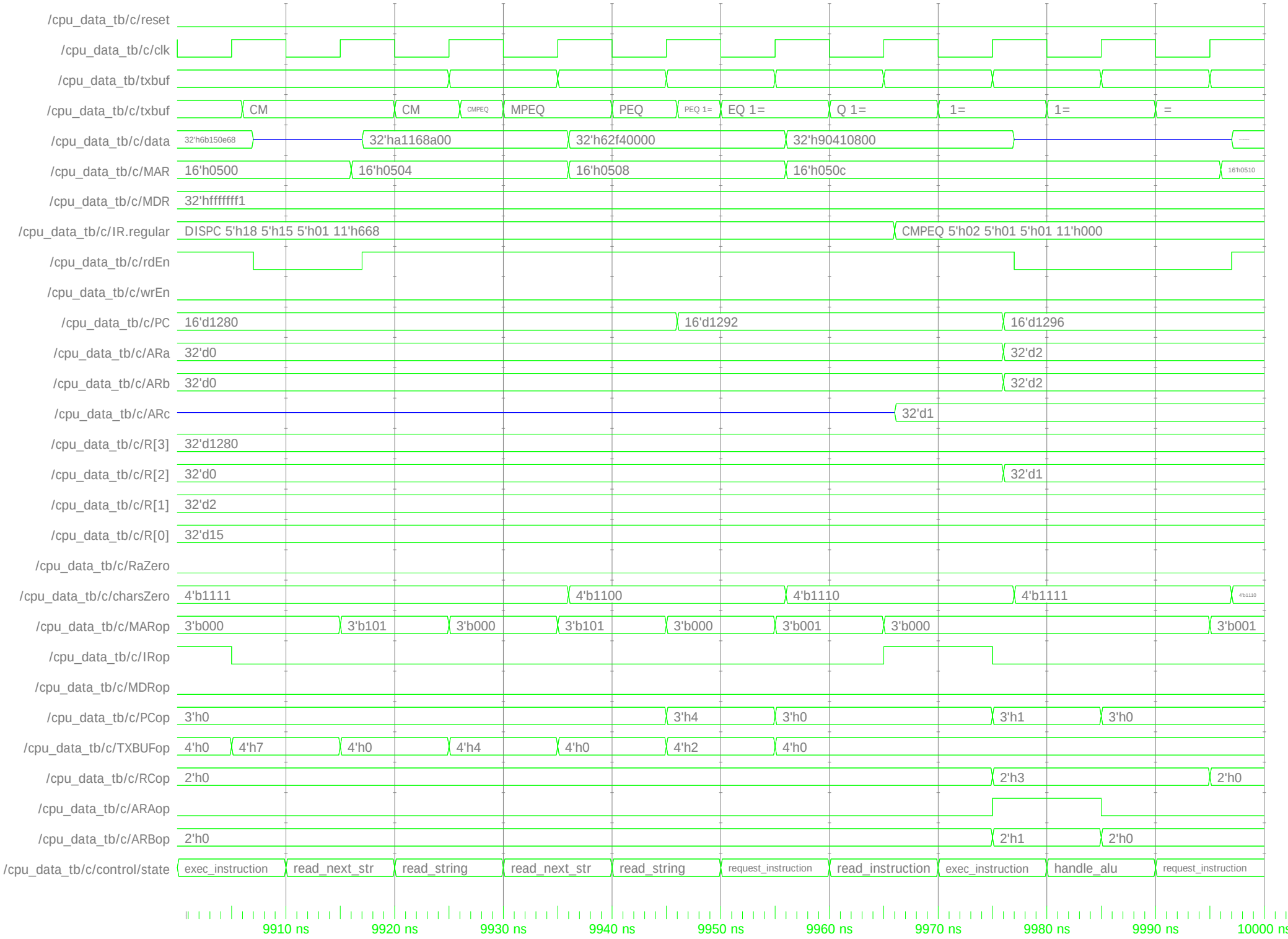
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 96 Page: 96



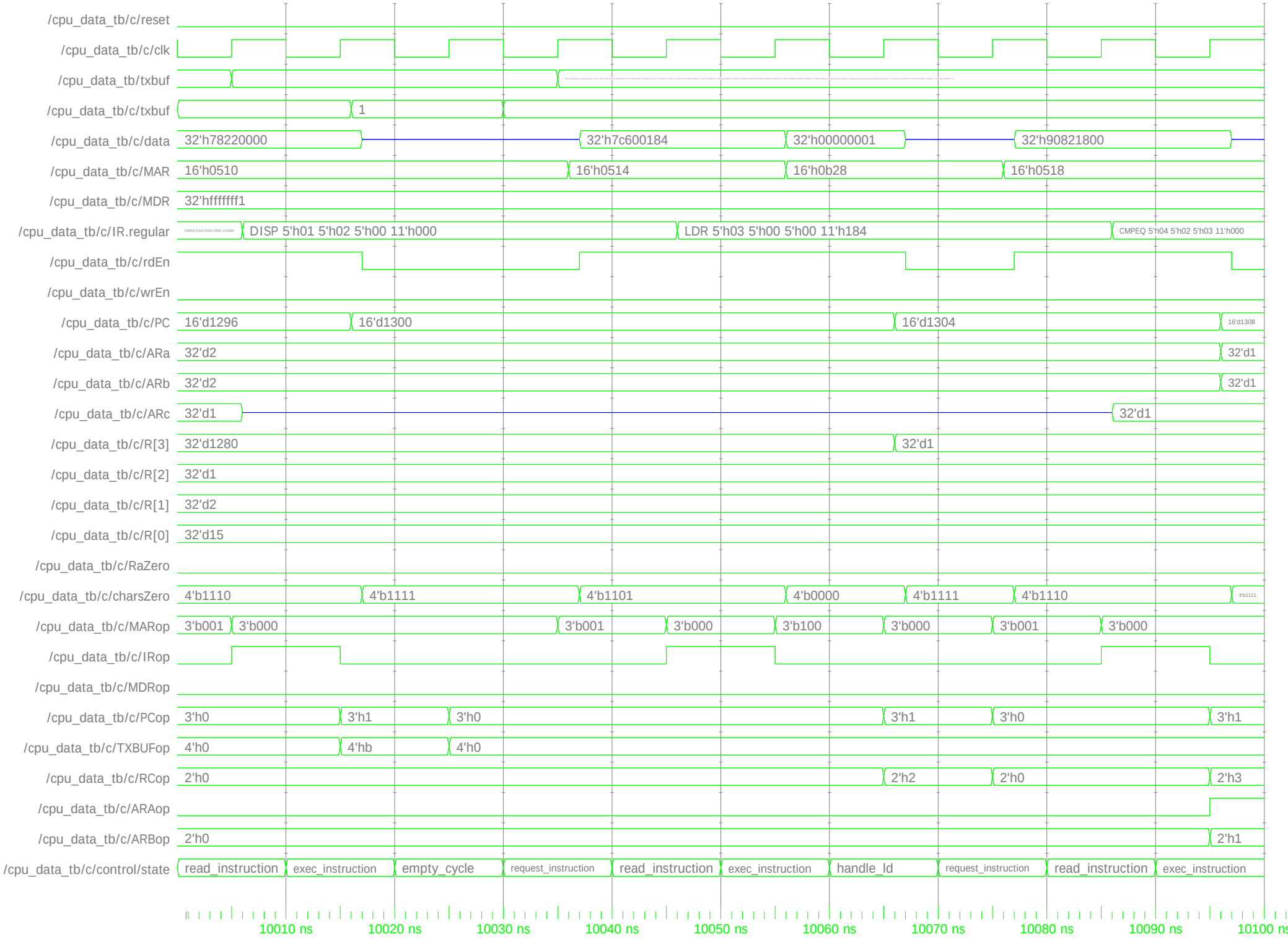
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 97 Page: 97


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/txbuf
0=
0=
=
0
/cpu_data_tb/c/data
32'h90400800
32'h78220000
32'h7c60018b
32'h00000000
/cpu_data_tb/c/MAR
16'h04ec
16'h04f0
16'h04f4
16'h0b24
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
CMPEQ 5'h02 5'h00 5'h01 11'h000
DISP 5'h01 5'h02 5'h00 11'h000
LDR 5'h03 5'h00 5'h00 11'h18b
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1260
16'd1264
16'd1268
16'd1272
/cpu_data_tb/c/ARa
32'd7
32'd15
/cpu_data_tb/c/ARb
32'd7
32'd2
/cpu_data_tb/c/ARc
32'd1
32'd0
/cpu_data_tb/c/R[3]
32'd1248
32'd0
/cpu_data_tb/c/R[2]
32'd7
32'd1
32'd0
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1110
4'b1111
4'b1101
4'b0000
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b100
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
2'h2
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_ld
9710 ns
9720 ns
9730 ns
9740 ns
9750 ns
9760 ns
9770 ns
9780 ns
9790 ns
9800 ns

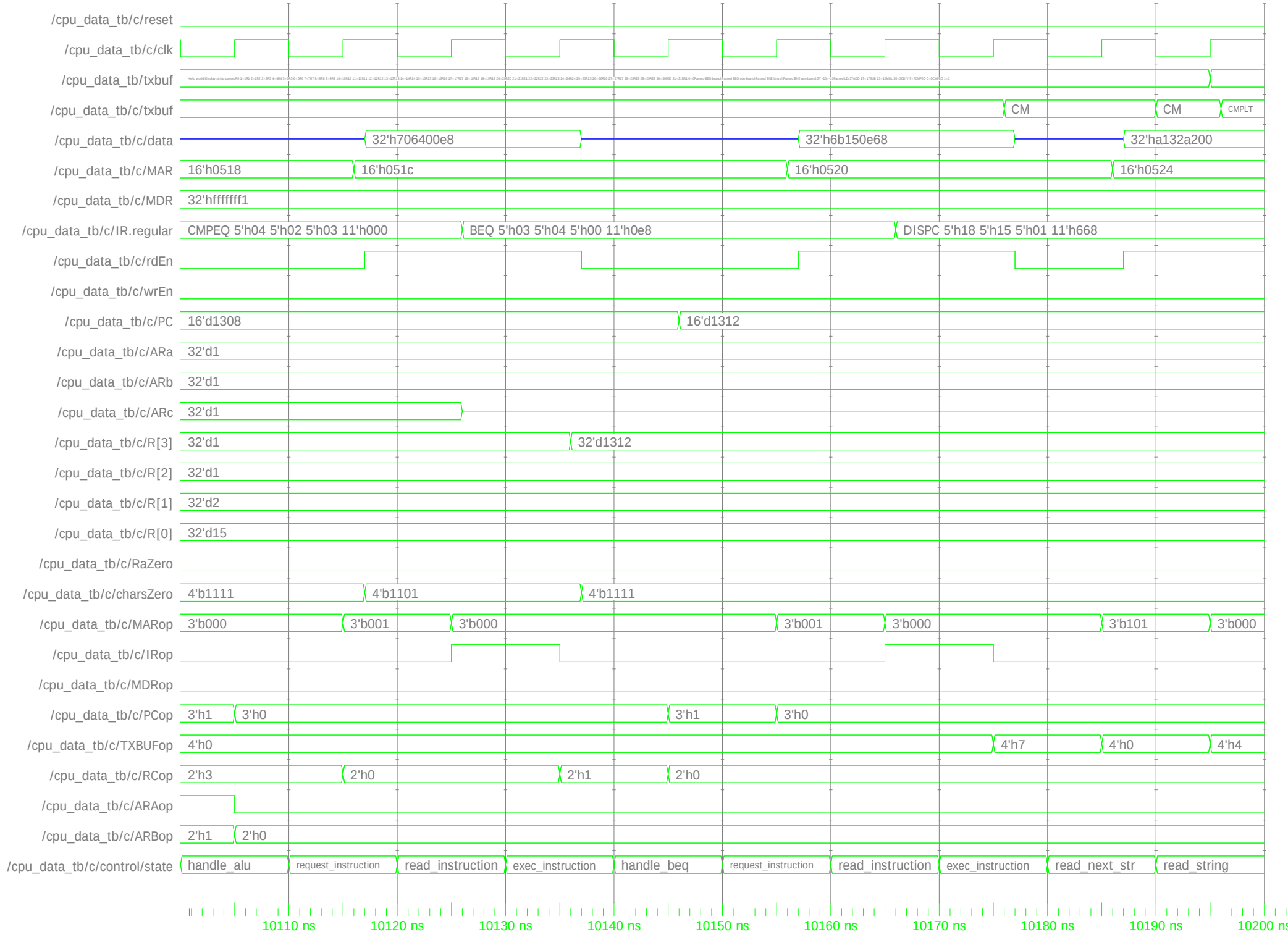

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h90821800
32'h706400f0
32'h6b150e68
/cpu_data_tb/c/MAR
16'h0b24
16'h04f8
16'h04fc
16'h0500
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h18b
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0f0
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1272
16'd1276
16'd1280
/cpu_data_tb/c/ARa
32'd15
32'd0
/cpu_data_tb/c/ARb
32'd2
32'd0
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd0
32'd1280
/cpu_data_tb/c/R[2]
32'd0
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
9810 ns
9820 ns
9830 ns
9840 ns
9850 ns
9860 ns
9870 ns
9880 ns
9890 ns
9900 ns



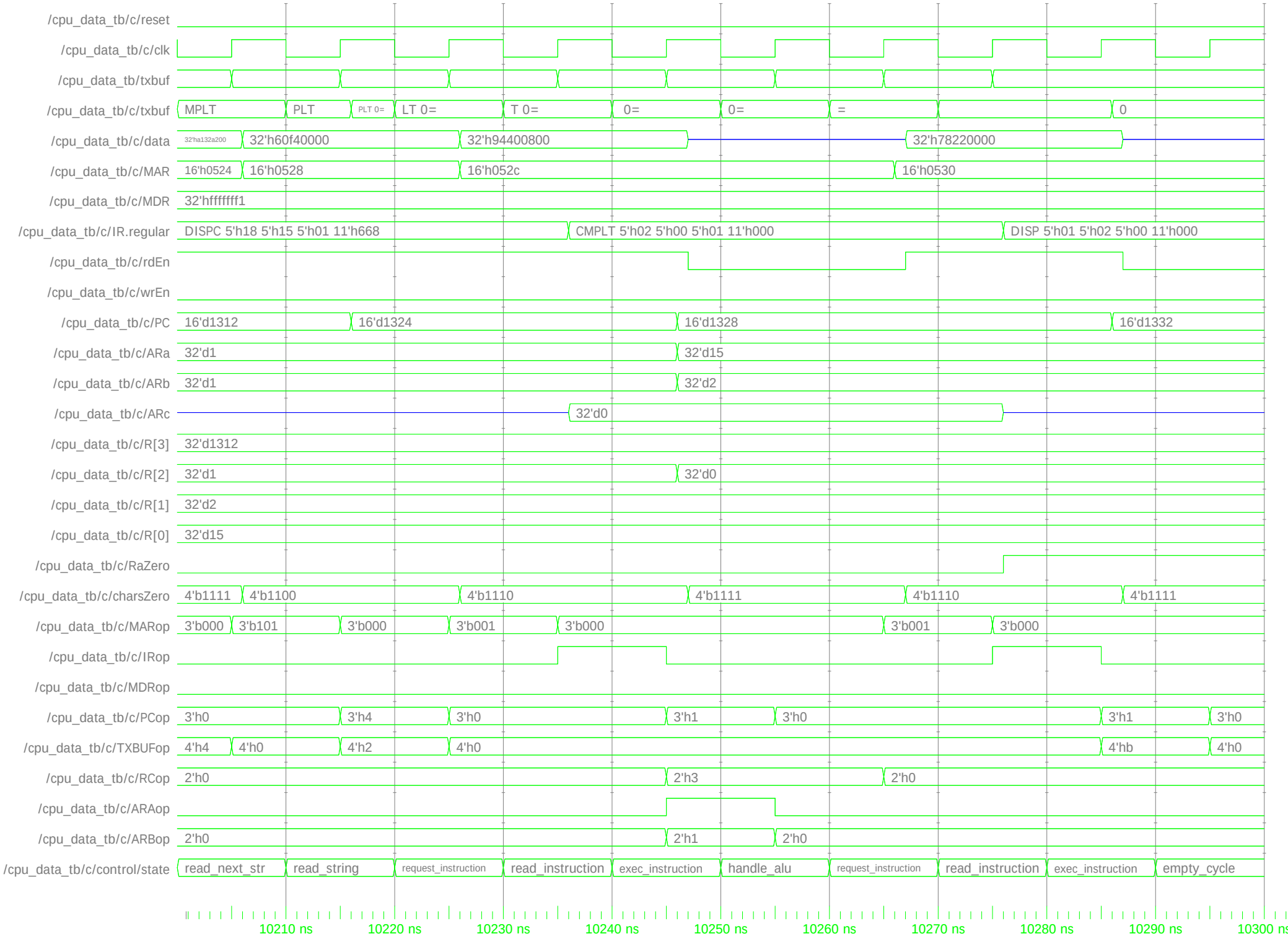
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 100 Page: 100



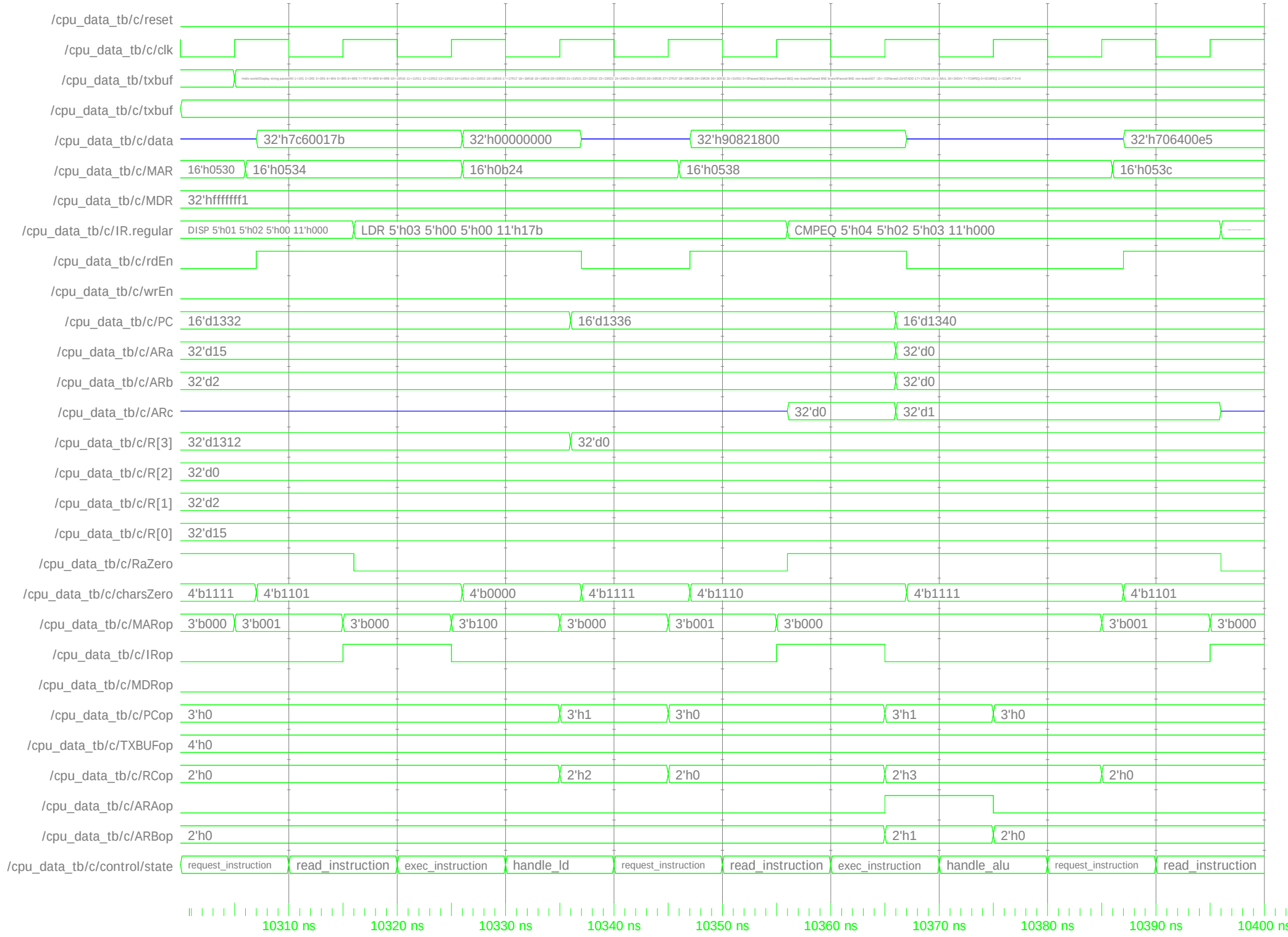
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 101 Page: 101



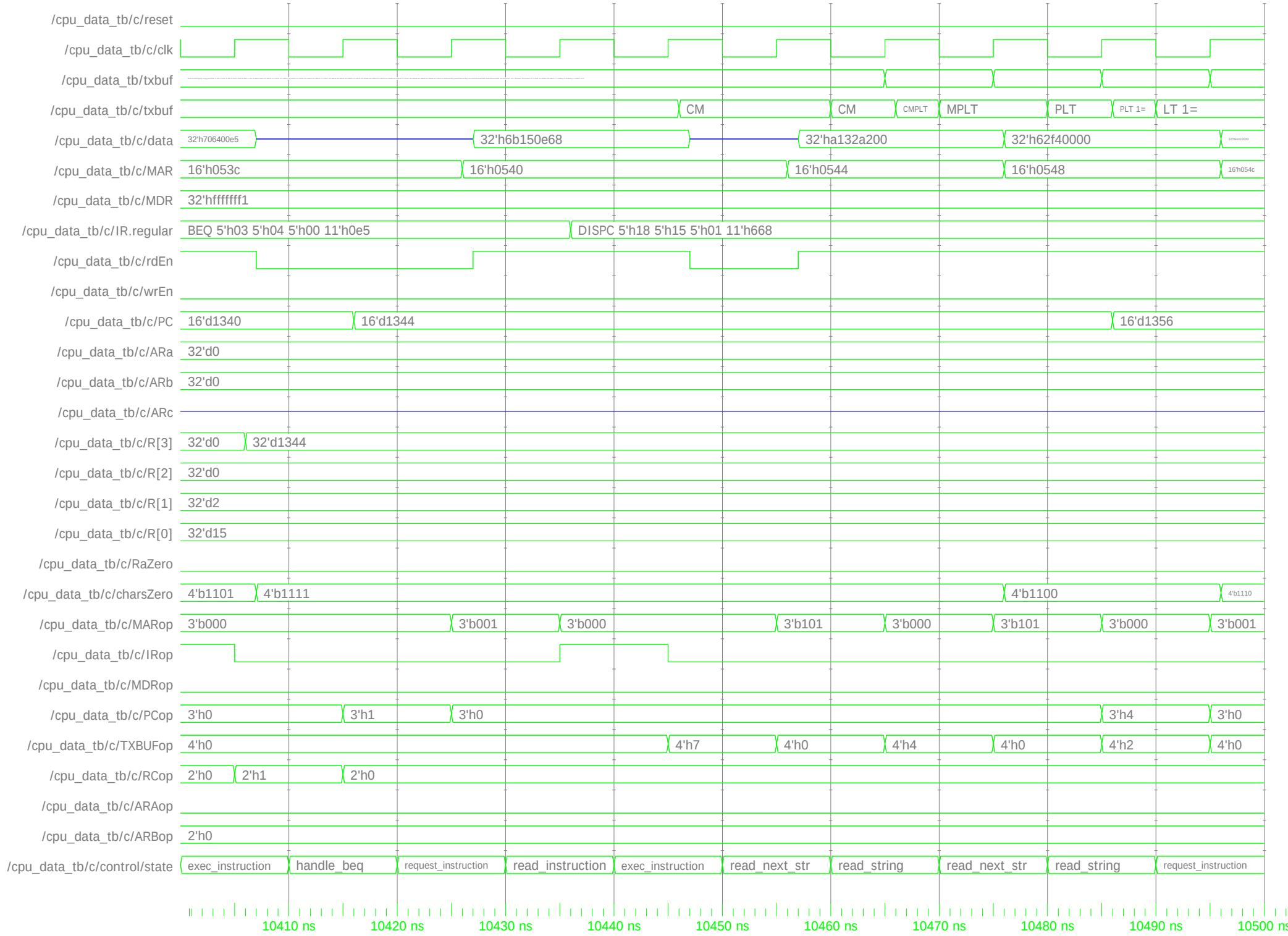
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 102 Page: 102

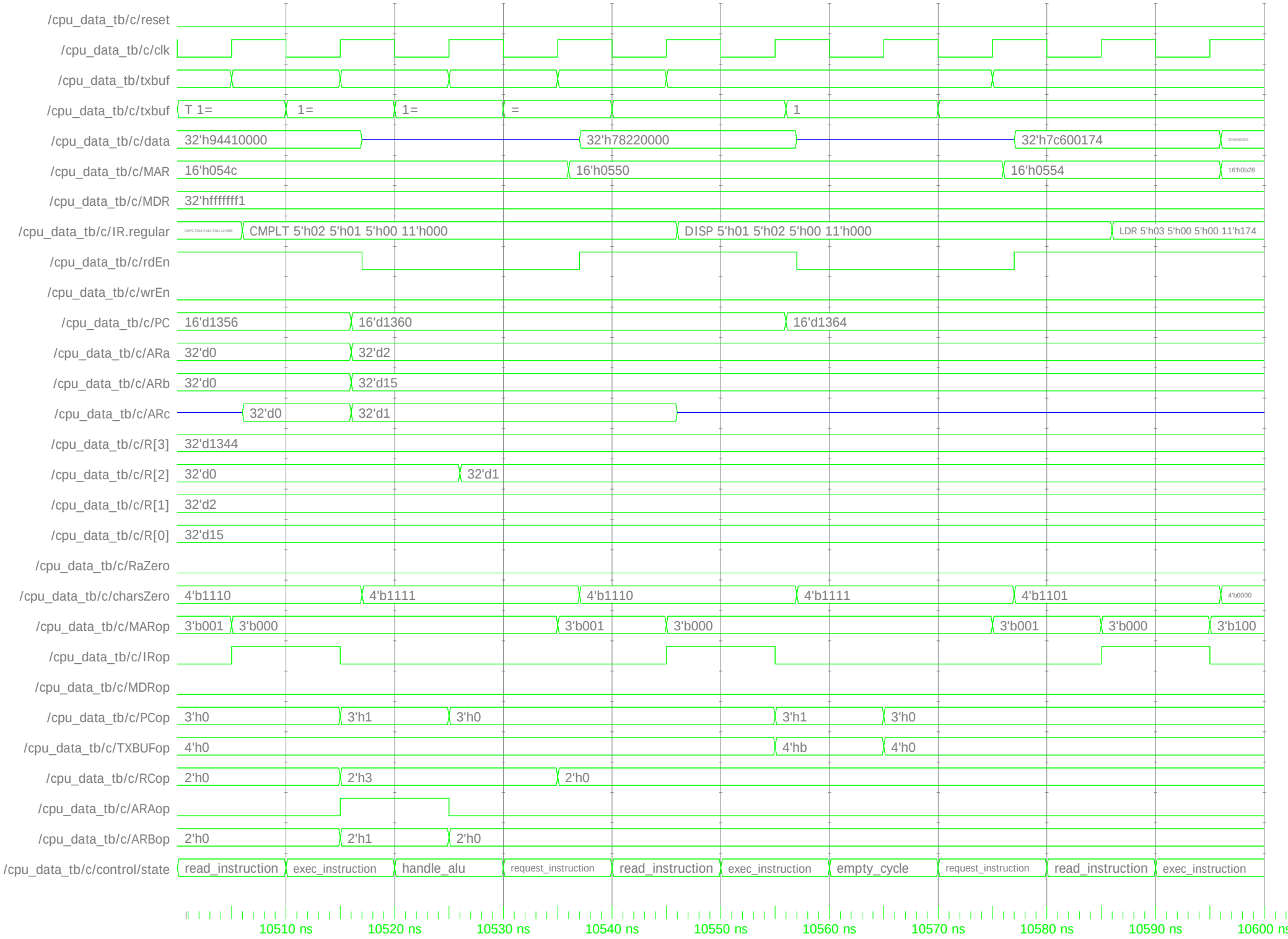


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 103 Page: 103

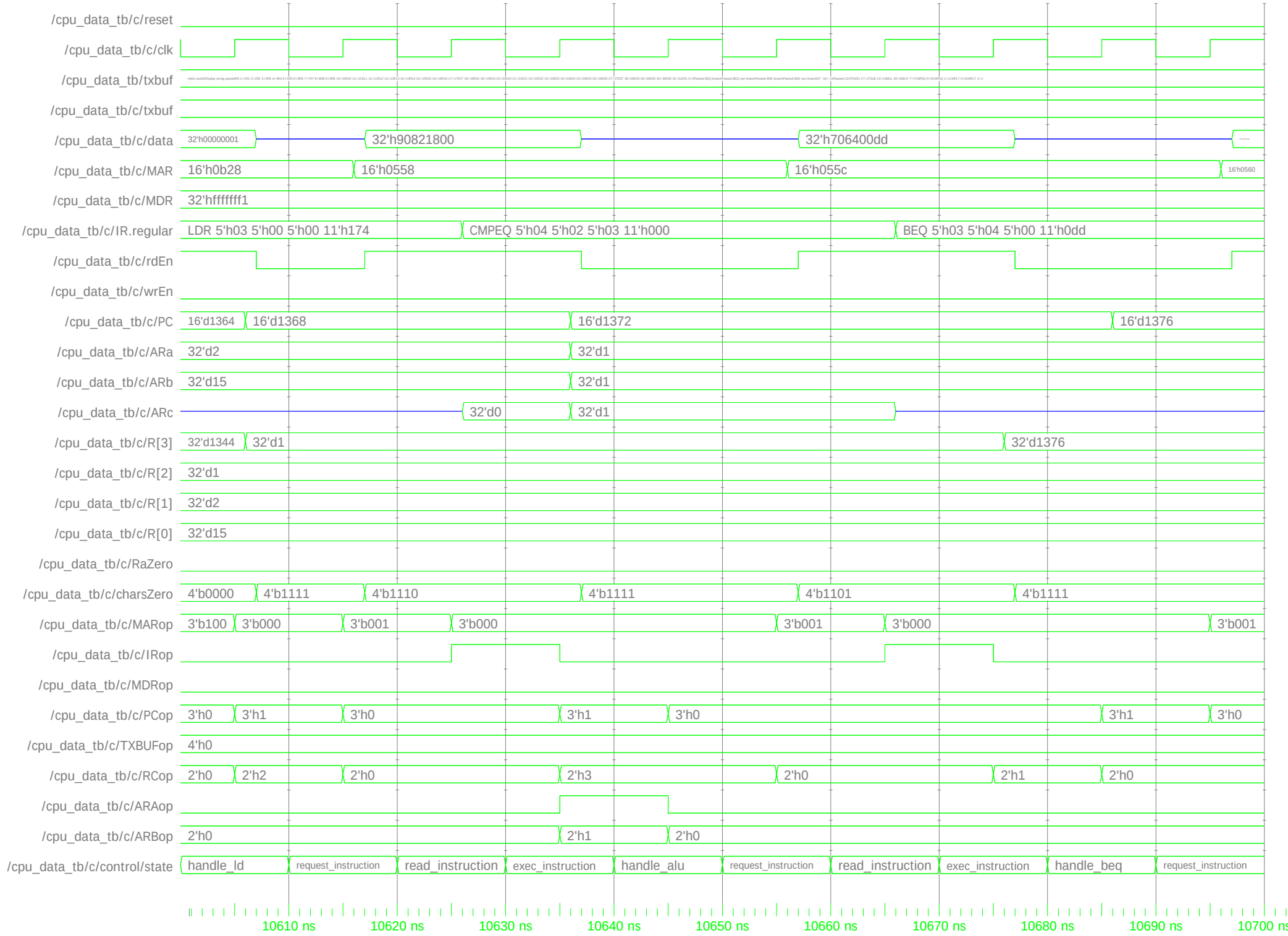


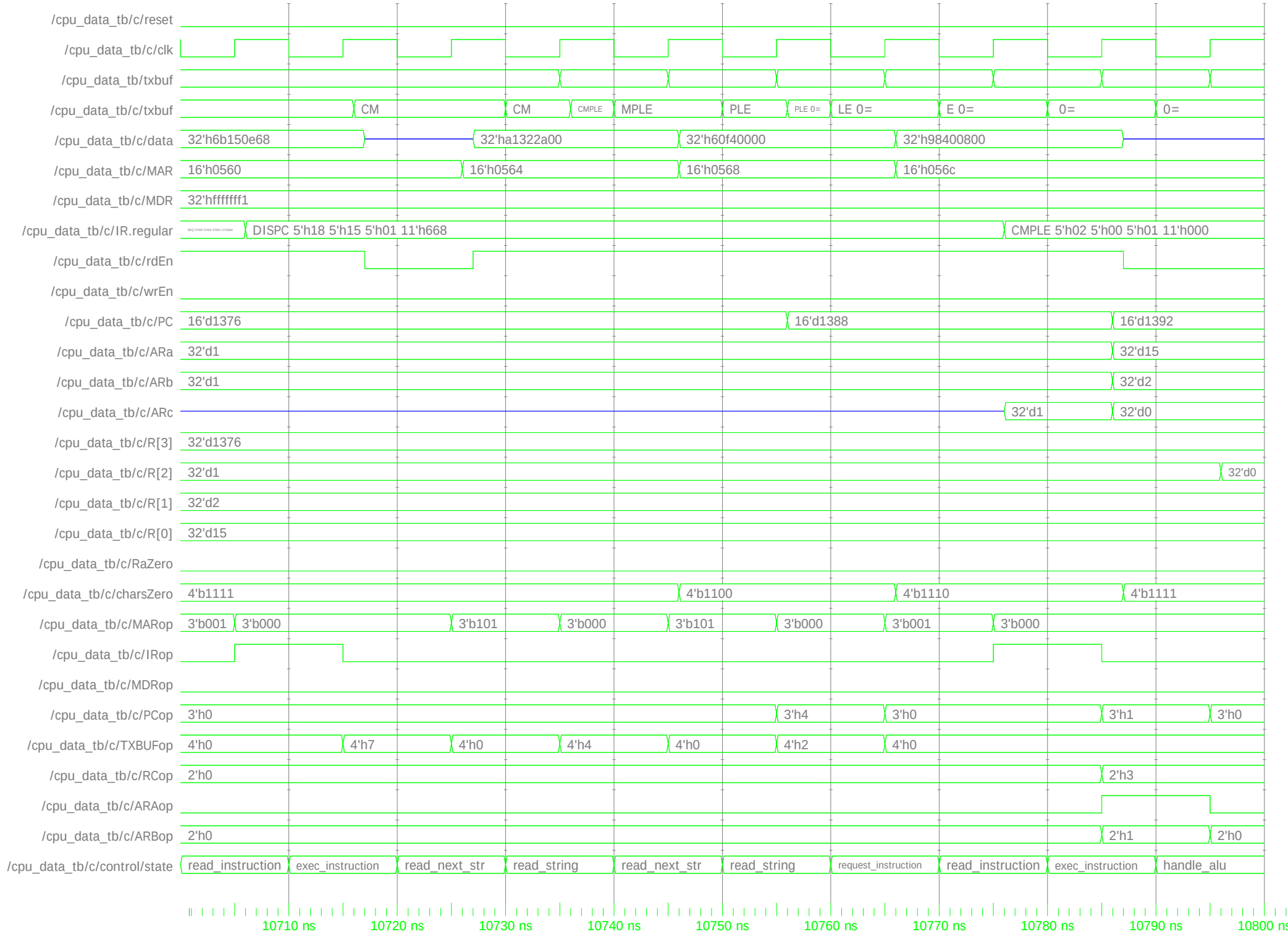
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 104 Page: 104


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
CM
CM
CMPLT
MPLT
PLT
PLT 1=
LT 1=
/cpu_data_tb/c/data
32'h706400e5
32'h6b150e68
32'ha132a200
32'h62f40000
/cpu_data_tb/c/MAR
16'h053c
16'h0540
16'h0544
16'h0548
16'h054c
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h04 5'h00 11'h0e5
DISPC 5'h18 5'h15 5'h01 11'h668
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1340
16'd1344
16'd1356
/cpu_data_tb/c/ARa
32'd0
/cpu_data_tb/c/ARb
32'd0
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd0
32'd1344
/cpu_data_tb/c/R[2]
32'd0
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
4'b1100
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h2
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
10410 ns
10420 ns
10430 ns
10440 ns
10450 ns
10460 ns
10470 ns
10480 ns
10490 ns
10500 ns

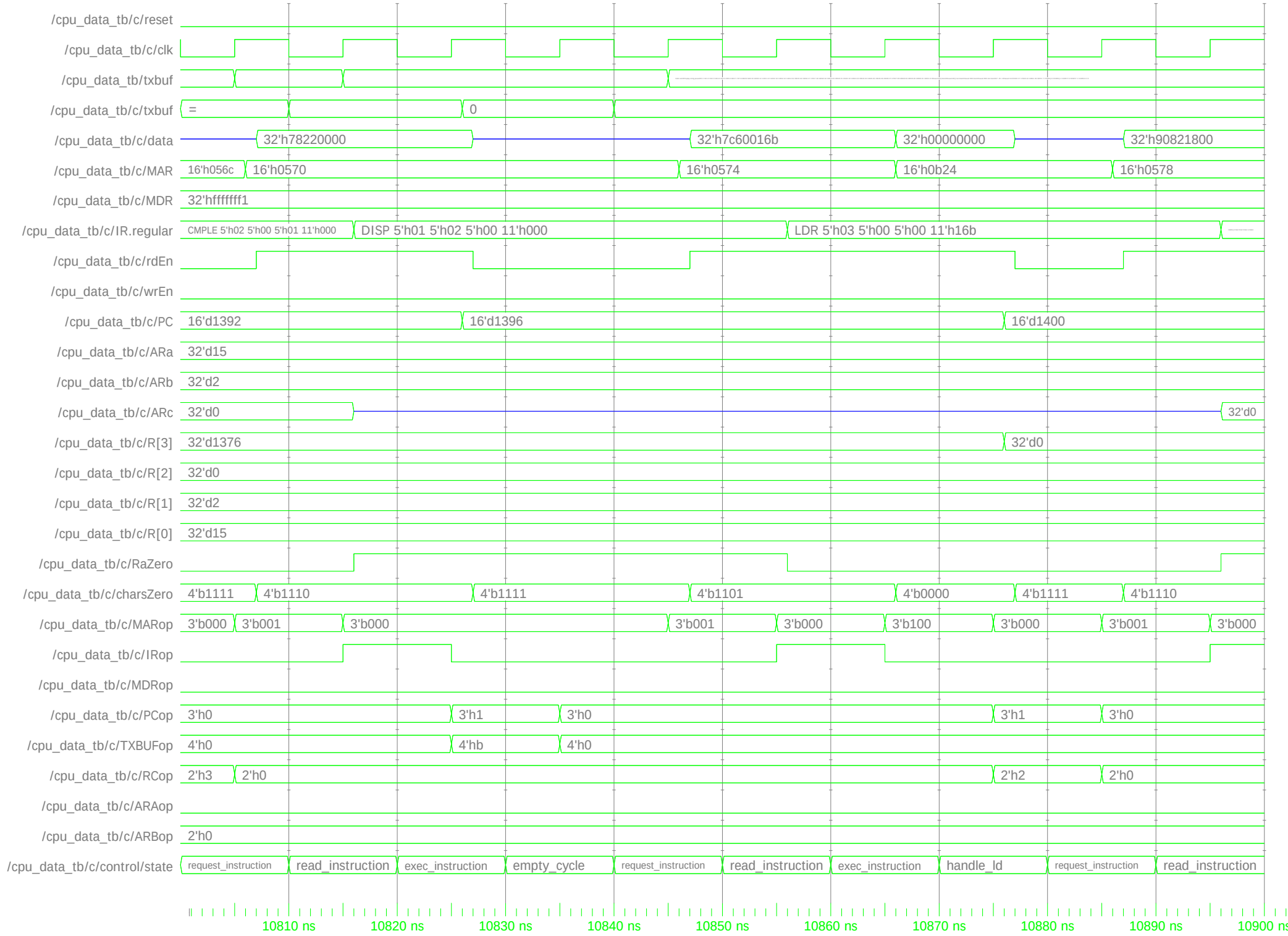


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 106 Page: 106

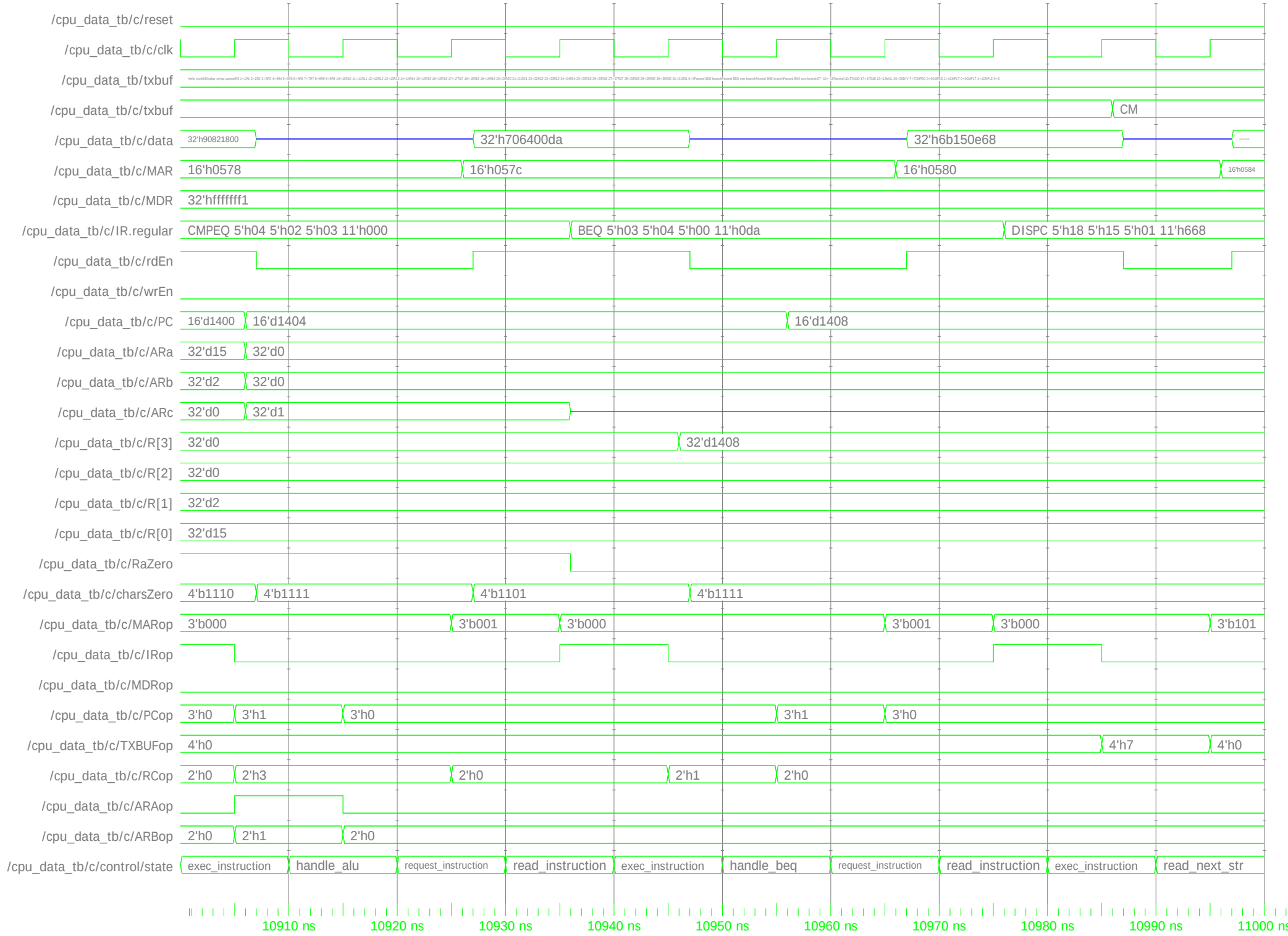

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h00000001
32'h90821800
32'h706400dd
/cpu_data_tb/c/MAR
16'h0b28
16'h0558
16'h055c
16'h0560
/cpu_data_tb/c/MDR
32'hffffffff
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h174
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0dd
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1364
16'd1368
16'd1372
16'd1376
/cpu_data_tb/c/ARa
32'd2
32'd1
/cpu_data_tb/c/ARb
32'd15
32'd1
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1344
32'd1
32'd1376
/cpu_data_tb/c/R[2]
32'd1
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b0000
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
10610 ns
10620 ns
10630 ns
10640 ns
10650 ns
10660 ns
10670 ns
10680 ns
10690 ns
10700 ns



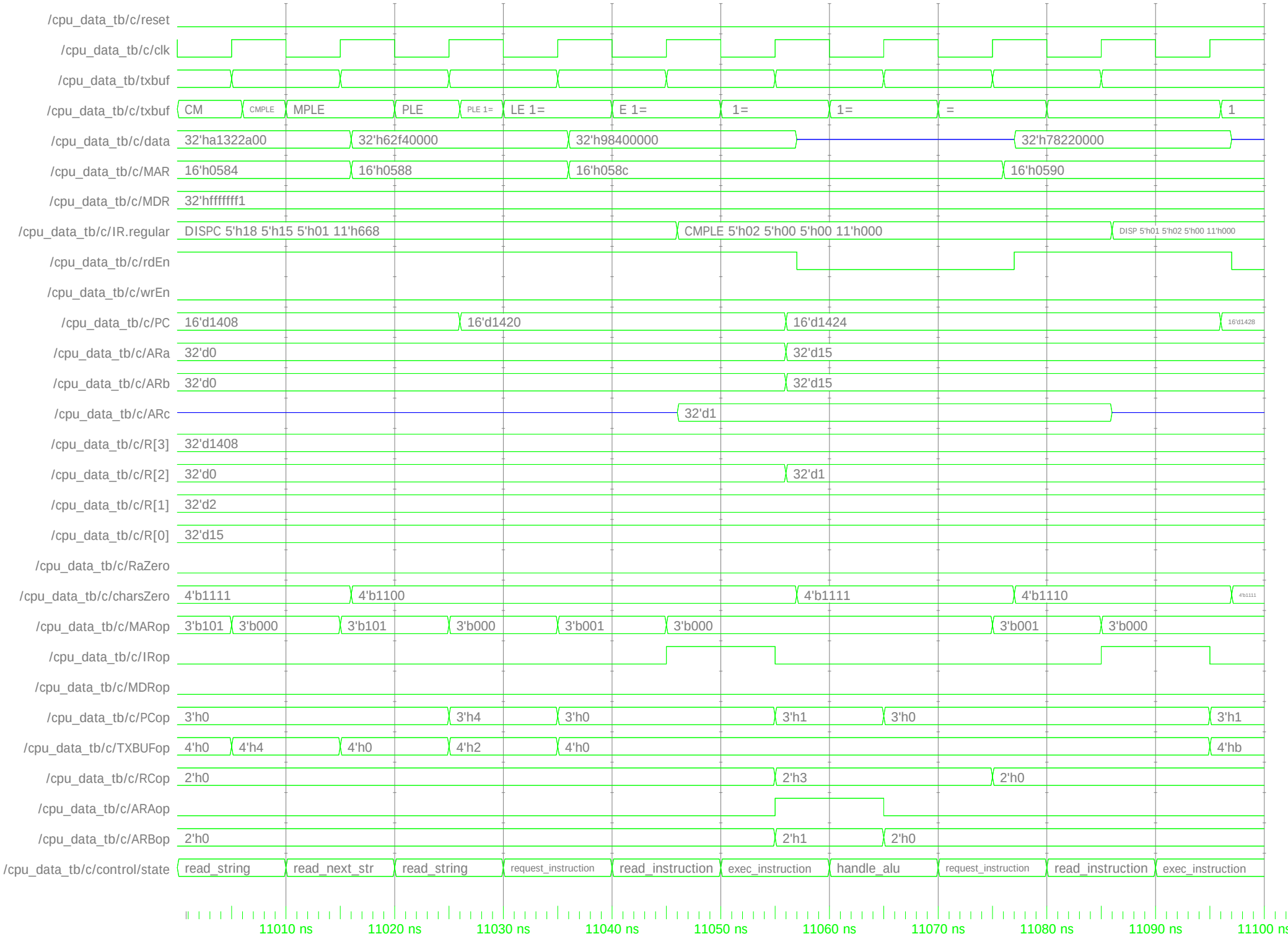
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 108 Page: 108

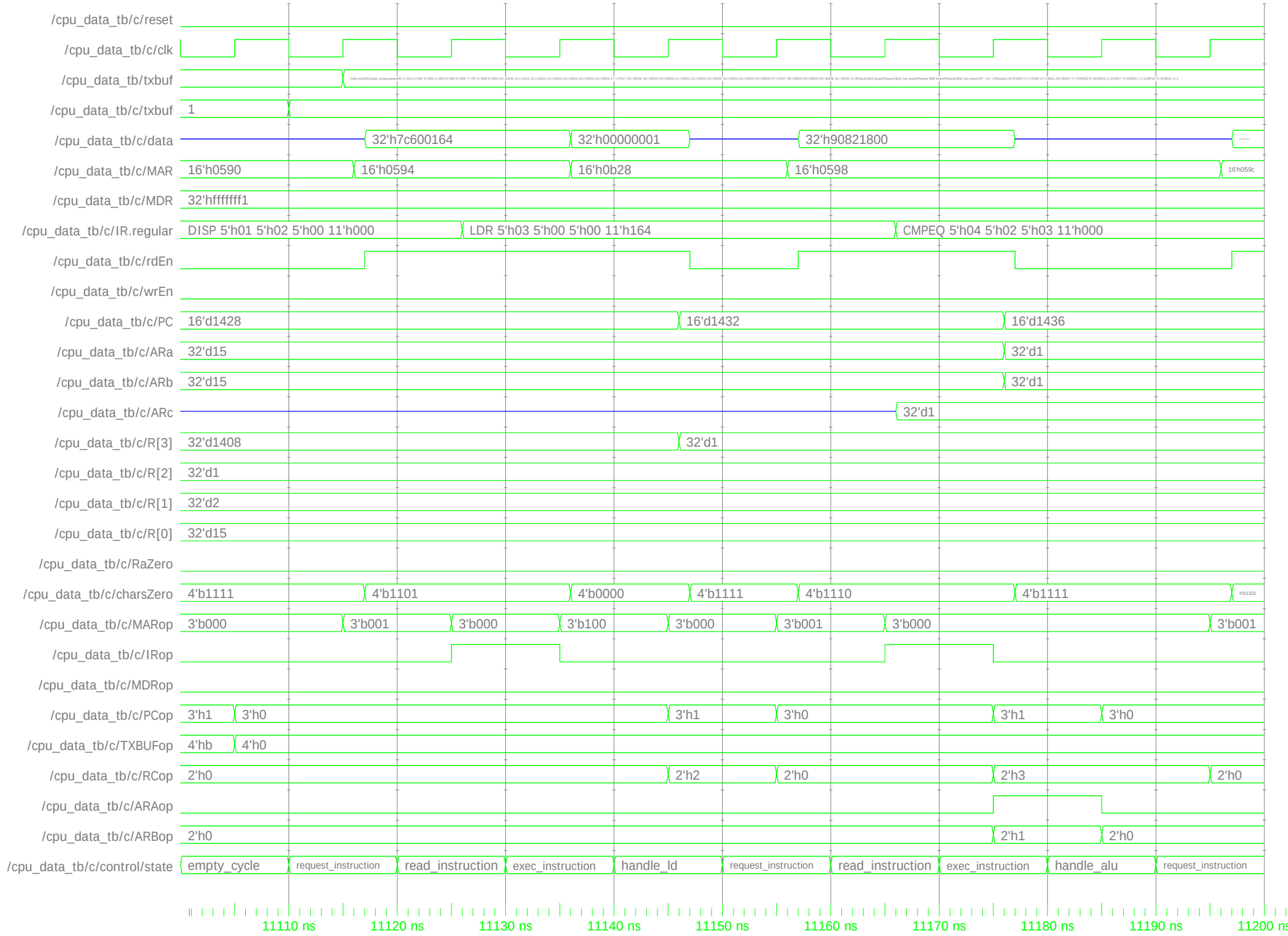


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 109 Page: 109

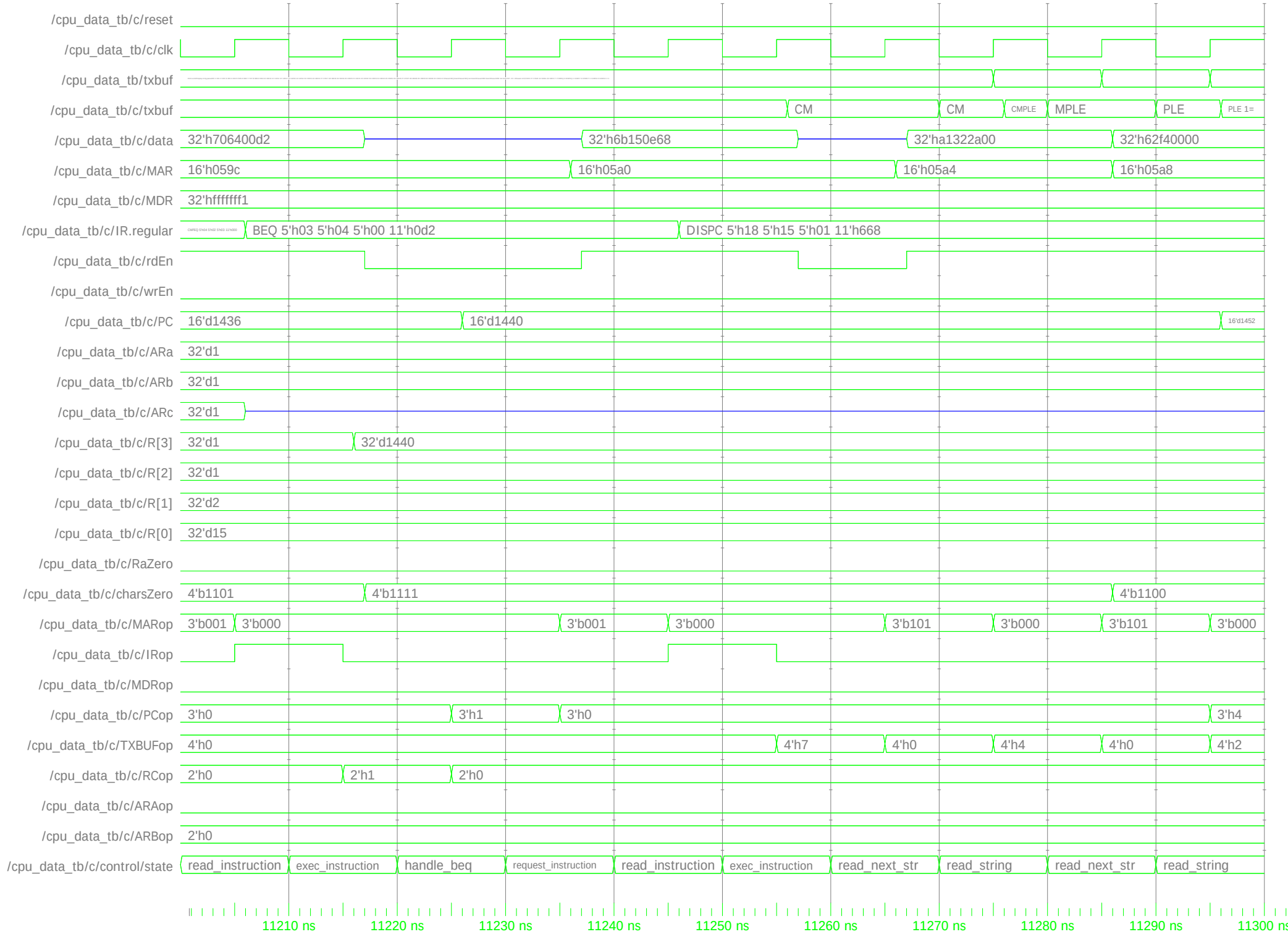


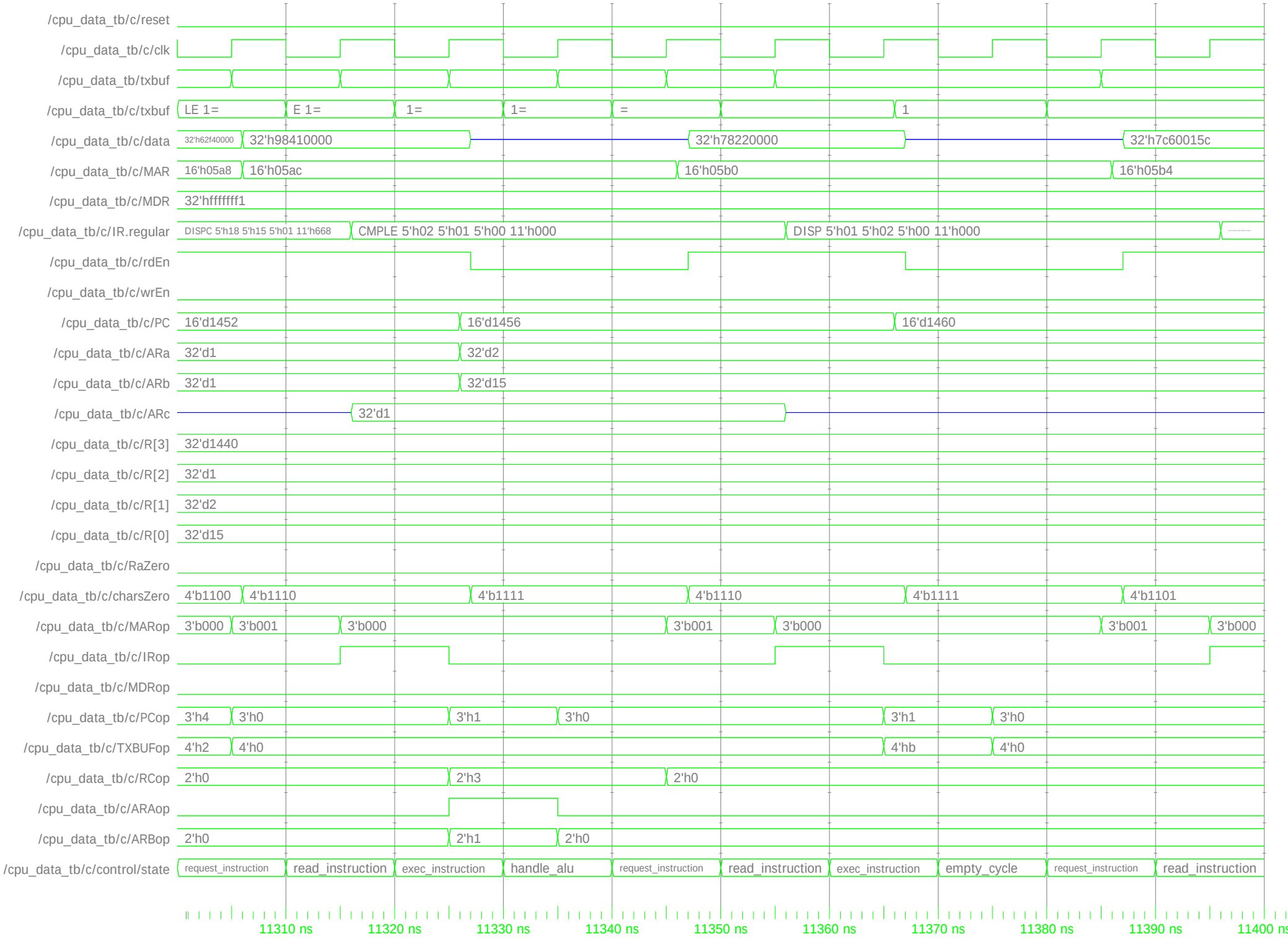
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 110 Page: 110

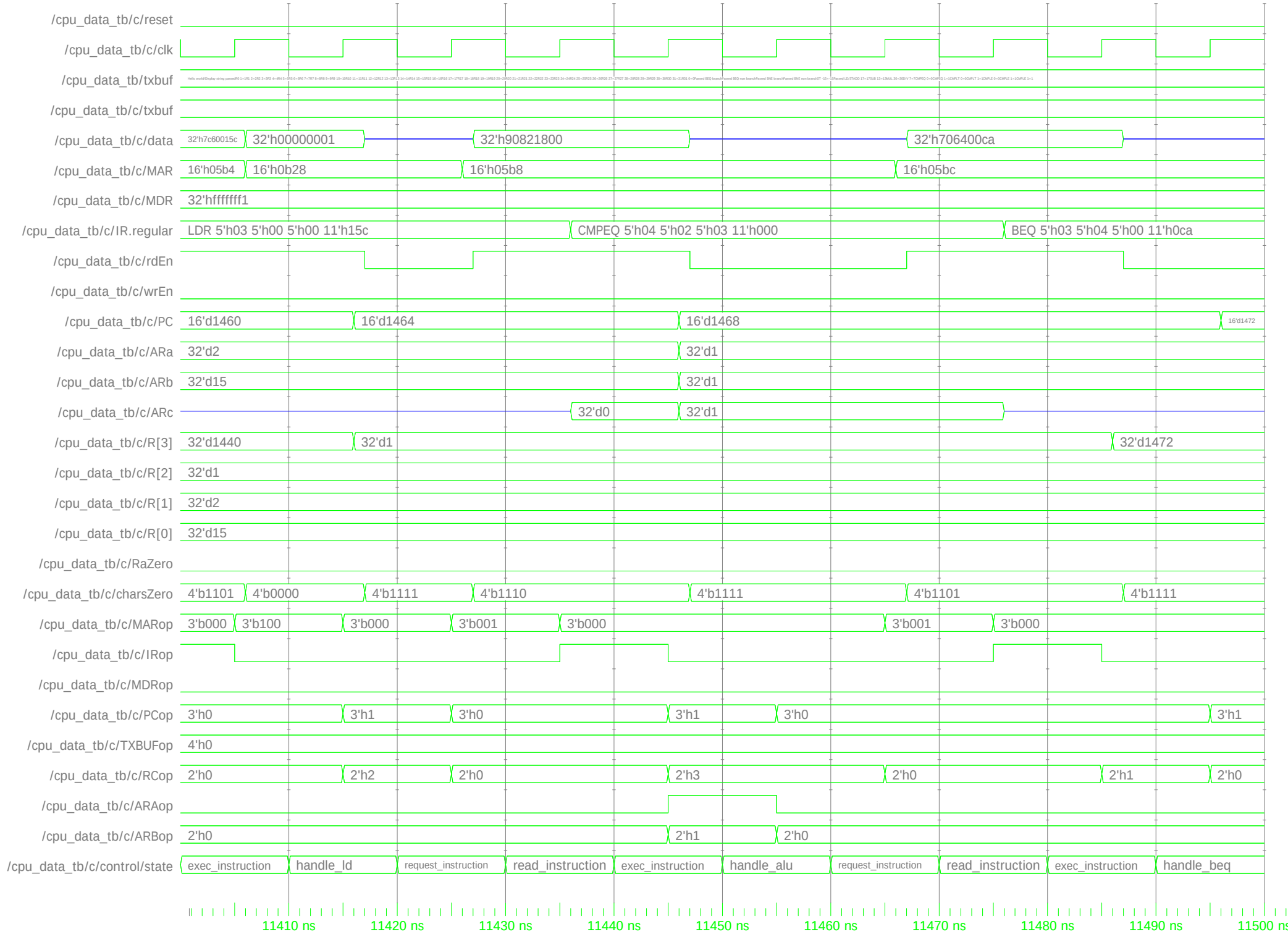

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
CM
CMPLE
MPLE
PLE
PLE 1=
LE 1=
E 1=
1=
1=
=
1
/cpu_data_tb/c/data
32'ha1322a00
32'h62f40000
32'h98400000
32'h78220000
/cpu_data_tb/c/MAR
16'h0584
16'h0588
16'h058c
16'h0590
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h01 11'h668
CMPLE 5'h02 5'h00 5'h00 11'h000
DISP 5'h01 5'h02 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1408
16'd1420
16'd1424
16'd1428
/cpu_data_tb/c/ARa
32'd0
32'd15
/cpu_data_tb/c/ARb
32'd0
32'd15
/cpu_data_tb/c/ARc
32'd1
/cpu_data_tb/c/R[3]
32'd1408
/cpu_data_tb/c/R[2]
32'd0
32'd1
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1100
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'h4
4'h0
4'h2
4'h0
4'hb
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
11010 ns
11020 ns
11030 ns
11040 ns
11050 ns
11060 ns
11070 ns
11080 ns
11090 ns
11100 ns

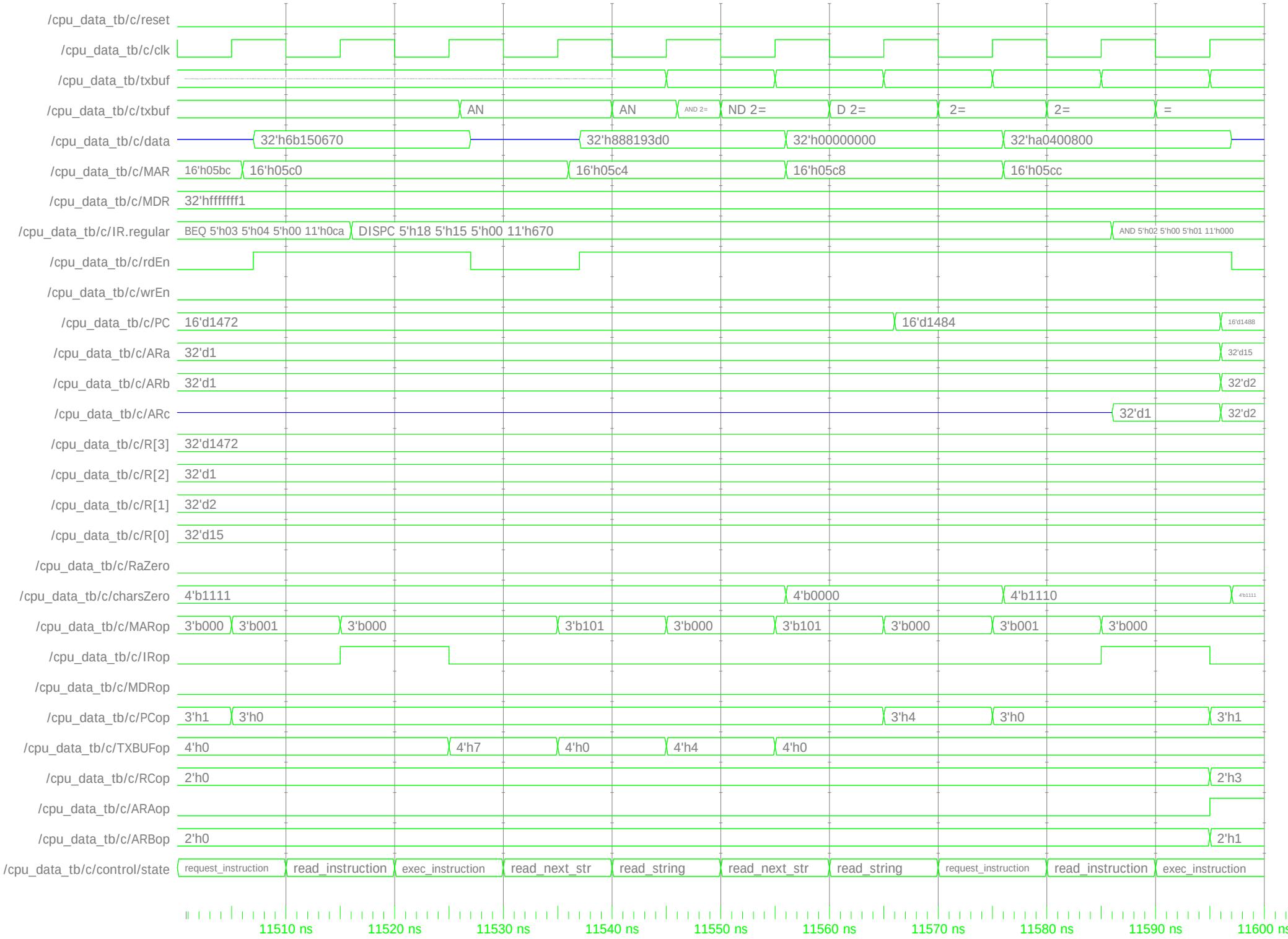


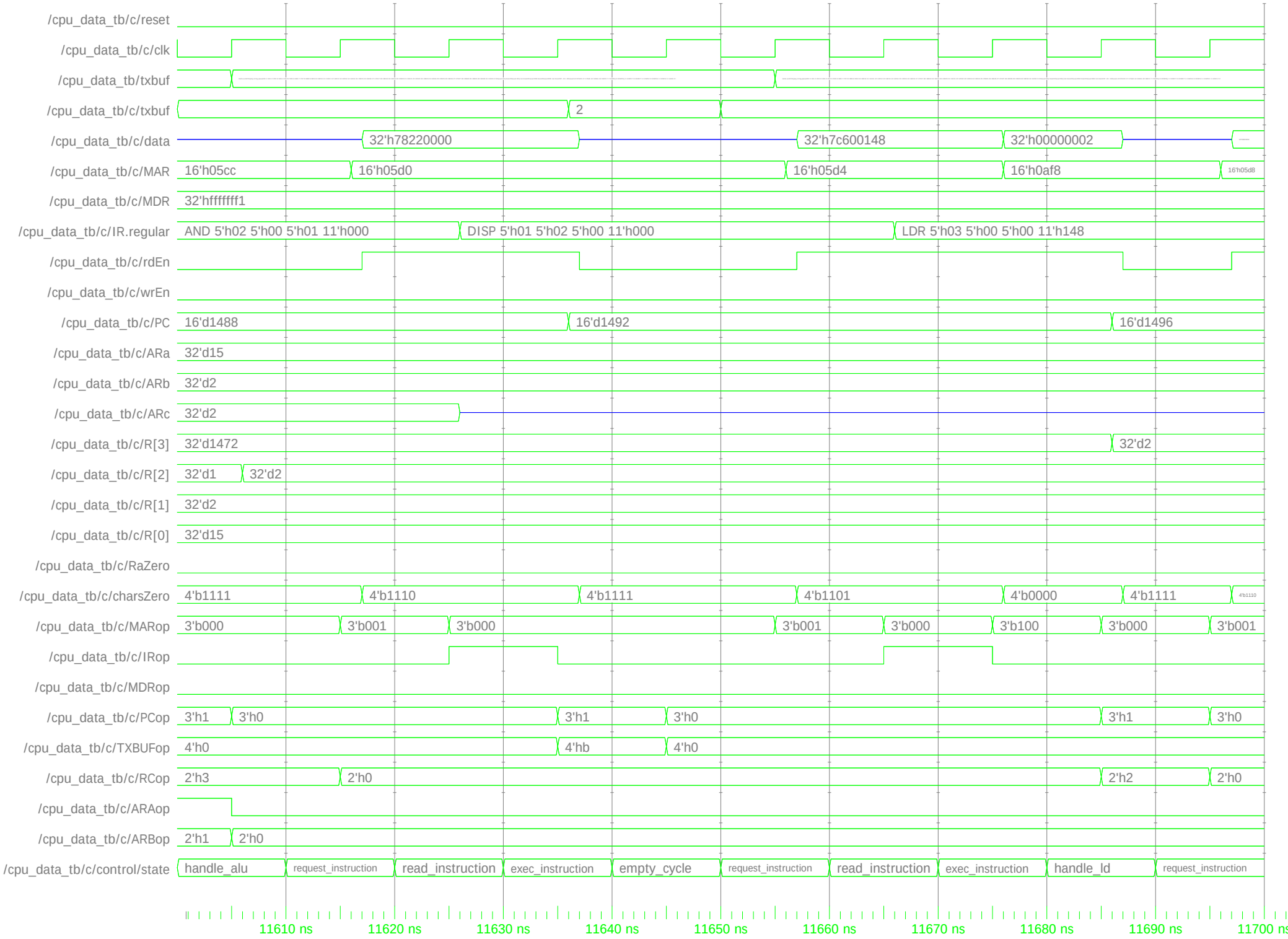
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 112 Page: 112

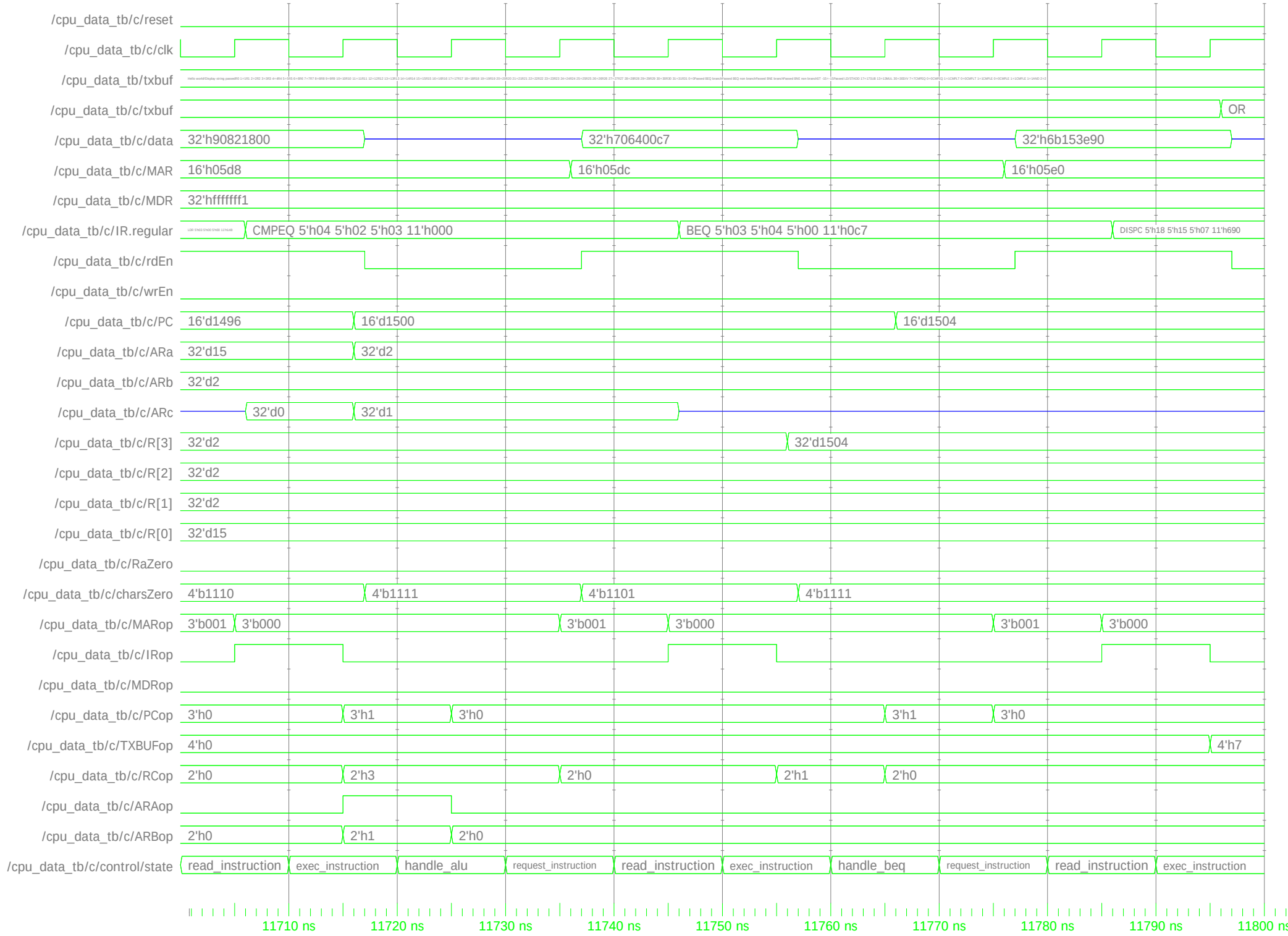

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
CM
CM
CMPLE
MPLE
PLE
PLE 1=
/cpu_data_tb/c/data
32'h706400d2
32'h6b150e68
32'ha1322a00
32'h62f40000
/cpu_data_tb/c/MAR
16'h059c
16'h05a0
16'h05a4
16'h05a8
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h04 5'h00 11'h0d2
DISPC 5'h18 5'h15 5'h01 11'h668
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1436
16'd1440
16'd1452
/cpu_data_tb/c/ARa
32'd1
/cpu_data_tb/c/ARb
32'd1
/cpu_data_tb/c/ARc
32'd1
/cpu_data_tb/c/R[3]
32'd1
32'd1440
/cpu_data_tb/c/R[2]
32'd1
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
4'b1100
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h2
/cpu_data_tb/c/RCop
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
11210 ns
11220 ns
11230 ns
11240 ns
11250 ns
11260 ns
11270 ns
11280 ns
11290 ns
11300 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
LE 1=
E 1=
1=
1=
=
1
/cpu_data_tb/c/data
32'h62f40000
32'h98410000
32'h78220000
32'h7c60015c
/cpu_data_tb/c/MAR
16'h05a8
16'h05ac
16'h05b0
16'h05b4
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h01 11'h668
CMPLE 5'h02 5'h01 5'h00 11'h000
DISP 5'h01 5'h02 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1452
16'd1456
16'd1460
/cpu_data_tb/c/ARa
32'd1
32'd2
/cpu_data_tb/c/ARb
32'd1
32'd15
/cpu_data_tb/c/ARc
32'd1
/cpu_data_tb/c/R[3]
32'd1440
/cpu_data_tb/c/R[2]
32'd1
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1100
4'b1110
4'b1111
4'b1110
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h4
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h2
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
11310 ns
11320 ns
11330 ns
11340 ns
11350 ns
11360 ns
11370 ns
11380 ns
11390 ns
11400 ns

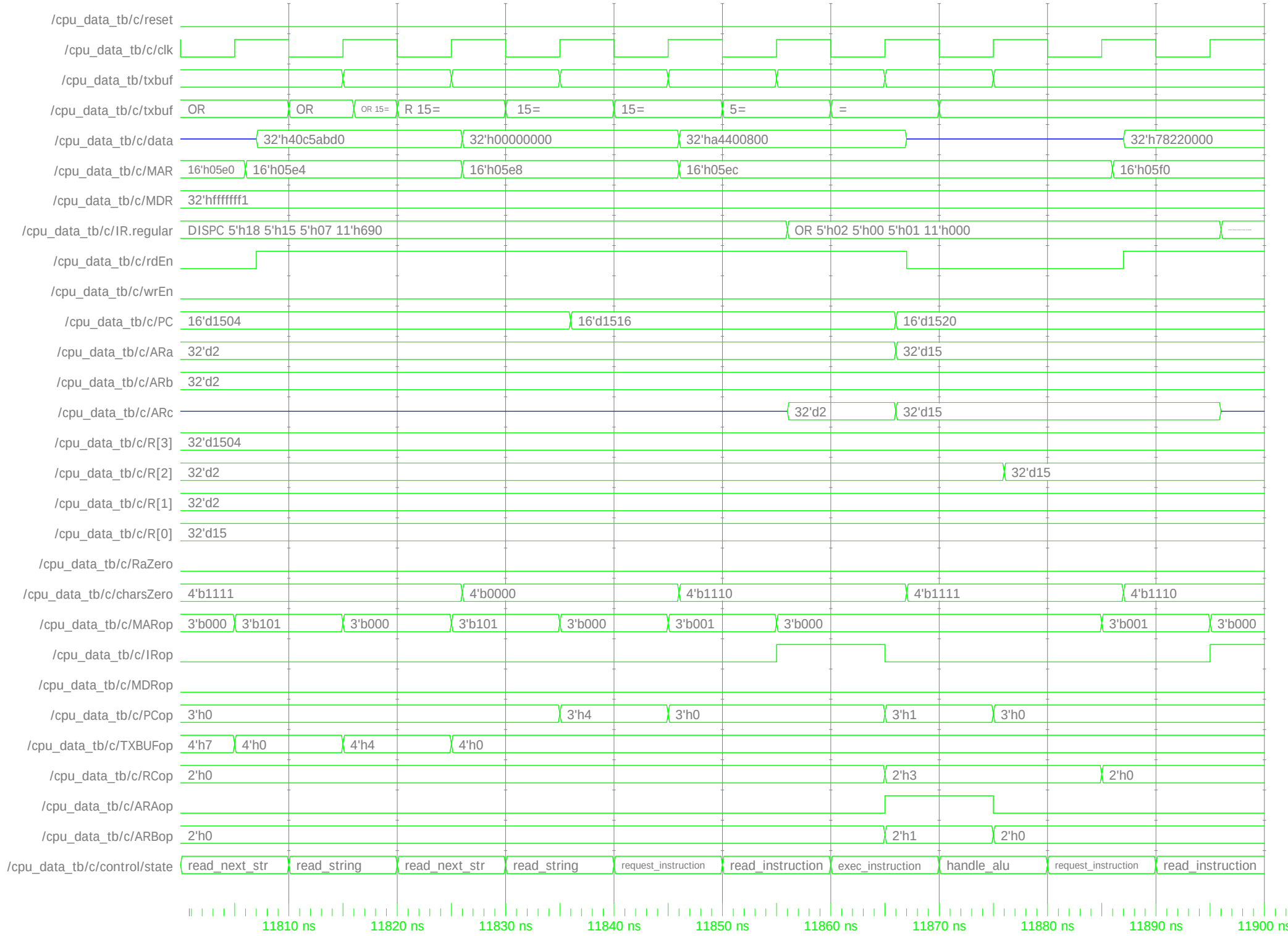

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h7c60015c
32'h00000001
32'h90821800
32'h706400ca
/cpu_data_tb/c/MAR
16'h05b4
16'h0b28
16'h05b8
16'h05bc
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h15c
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0ca
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1460
16'd1464
16'd1468
16'd1472
/cpu_data_tb/c/ARa
32'd2
32'd1
/cpu_data_tb/c/ARb
32'd15
32'd1
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1440
32'd1
32'd1472
/cpu_data_tb/c/R[2]
32'd1
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b0000
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
11410 ns
11420 ns
11430 ns
11440 ns
11450 ns
11460 ns
11470 ns
11480 ns
11490 ns
11500 ns

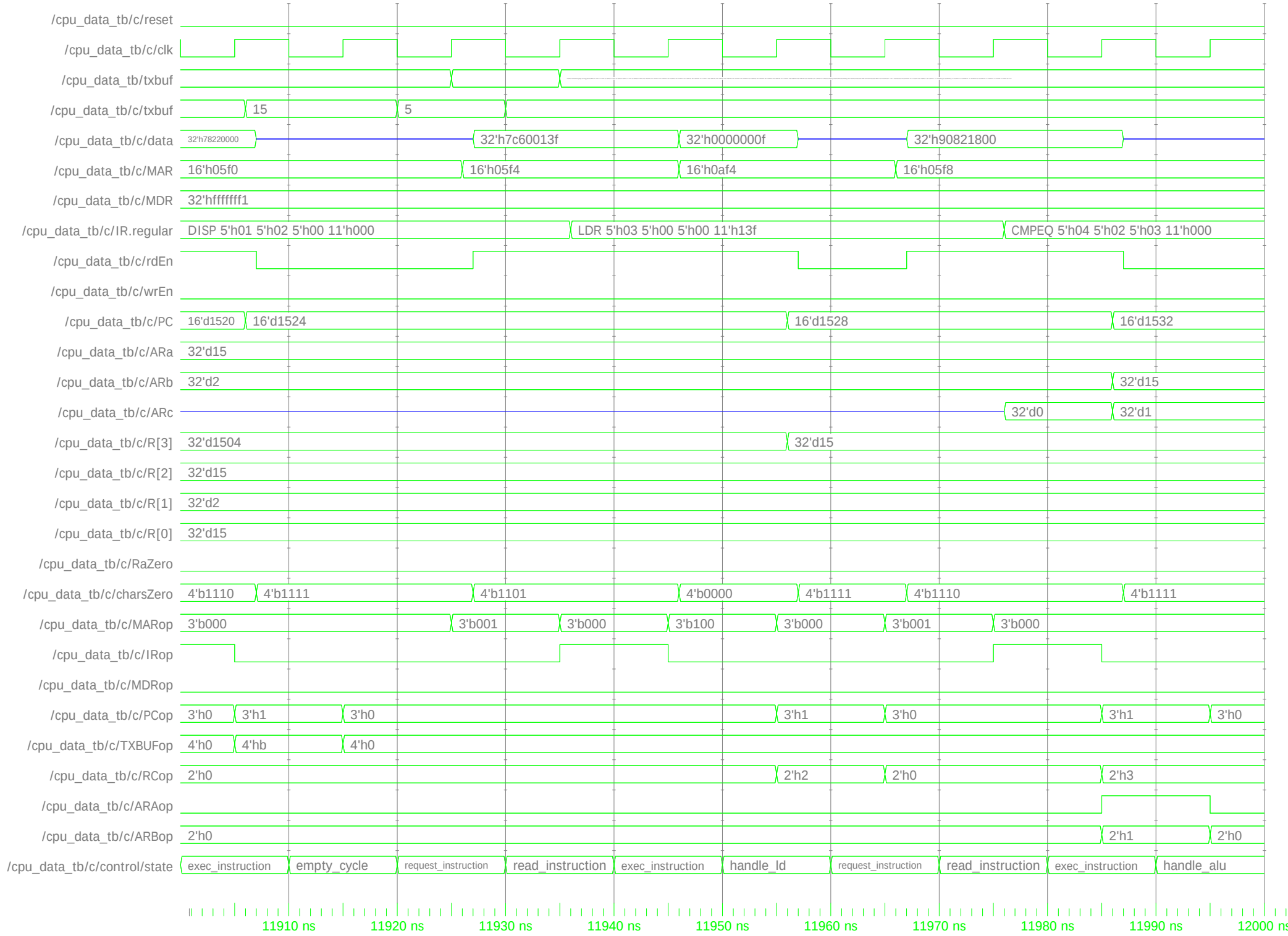

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
AN
AN
AND 2=
ND 2=
D 2=
2=
2=
=
/cpu_data_tb/c/data
32'h6b150670
32'h888193d0
32'h00000000
32'ha0400800
/cpu_data_tb/c/MAR
16'h05bc
16'h05c0
16'h05c4
16'h05c8
16'h05cc
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h04 5'h00 11'h0ca
DISPC 5'h18 5'h15 5'h00 11'h670
AND 5'h02 5'h00 5'h01 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1472
16'd1484
16'd1488
/cpu_data_tb/c/ARa
32'd1
32'd15
/cpu_data_tb/c/ARb
32'd1
32'd2
/cpu_data_tb/c/ARc
32'd1
32'd2
/cpu_data_tb/c/R[3]
32'd1472
/cpu_data_tb/c/R[2]
32'd1
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b0000
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h4
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
11510 ns
11520 ns
11530 ns
11540 ns
11550 ns
11560 ns
11570 ns
11580 ns
11590 ns
11600 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
2
/cpu_data_tb/c/data
32'h78220000
32'h7c600148
32'h00000002
/cpu_data_tb/c/MAR
16'h05cc
16'h05d0
16'h05d4
16'h0af8
16'h05d8
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
AND 5'h02 5'h00 5'h01 11'h000
DISP 5'h01 5'h02 5'h00 11'h000
LDR 5'h03 5'h00 5'h00 11'h148
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1488
16'd1492
16'd1496
/cpu_data_tb/c/ARa
32'd15
/cpu_data_tb/c/ARb
32'd2
/cpu_data_tb/c/ARc
32'd2
/cpu_data_tb/c/R[3]
32'd1472
32'd2
/cpu_data_tb/c/R[2]
32'd1
32'd2
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1110
4'b1111
4'b1101
4'b0000
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b100
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h3
2'h0
2'h2
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h1
2'h0
/cpu_data_tb/c/control/state
handle_alu
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_ld
request_instruction
11610 ns
11620 ns
11630 ns
11640 ns
11650 ns
11660 ns
11670 ns
11680 ns
11690 ns
11700 ns

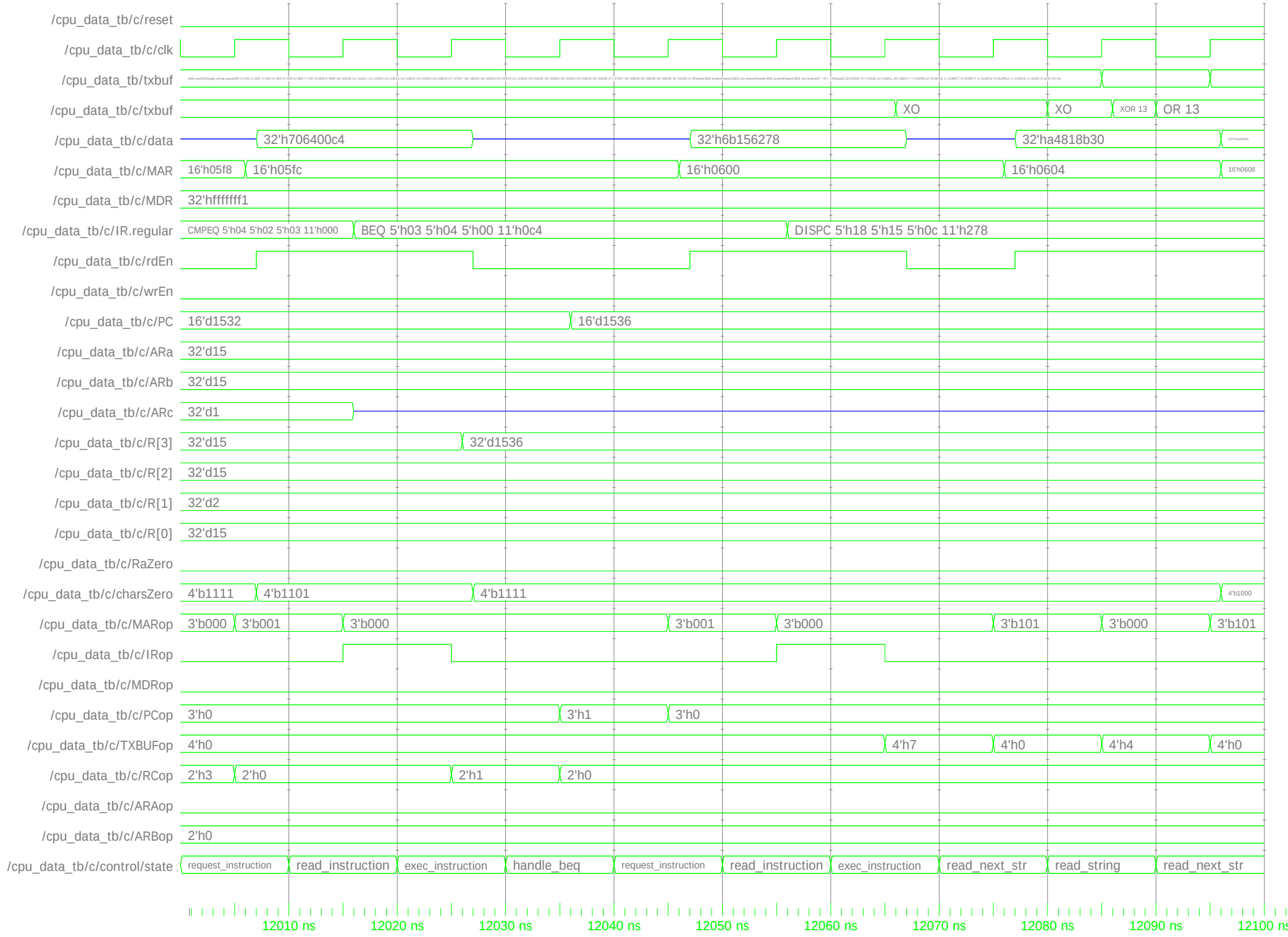


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 118 Page: 118

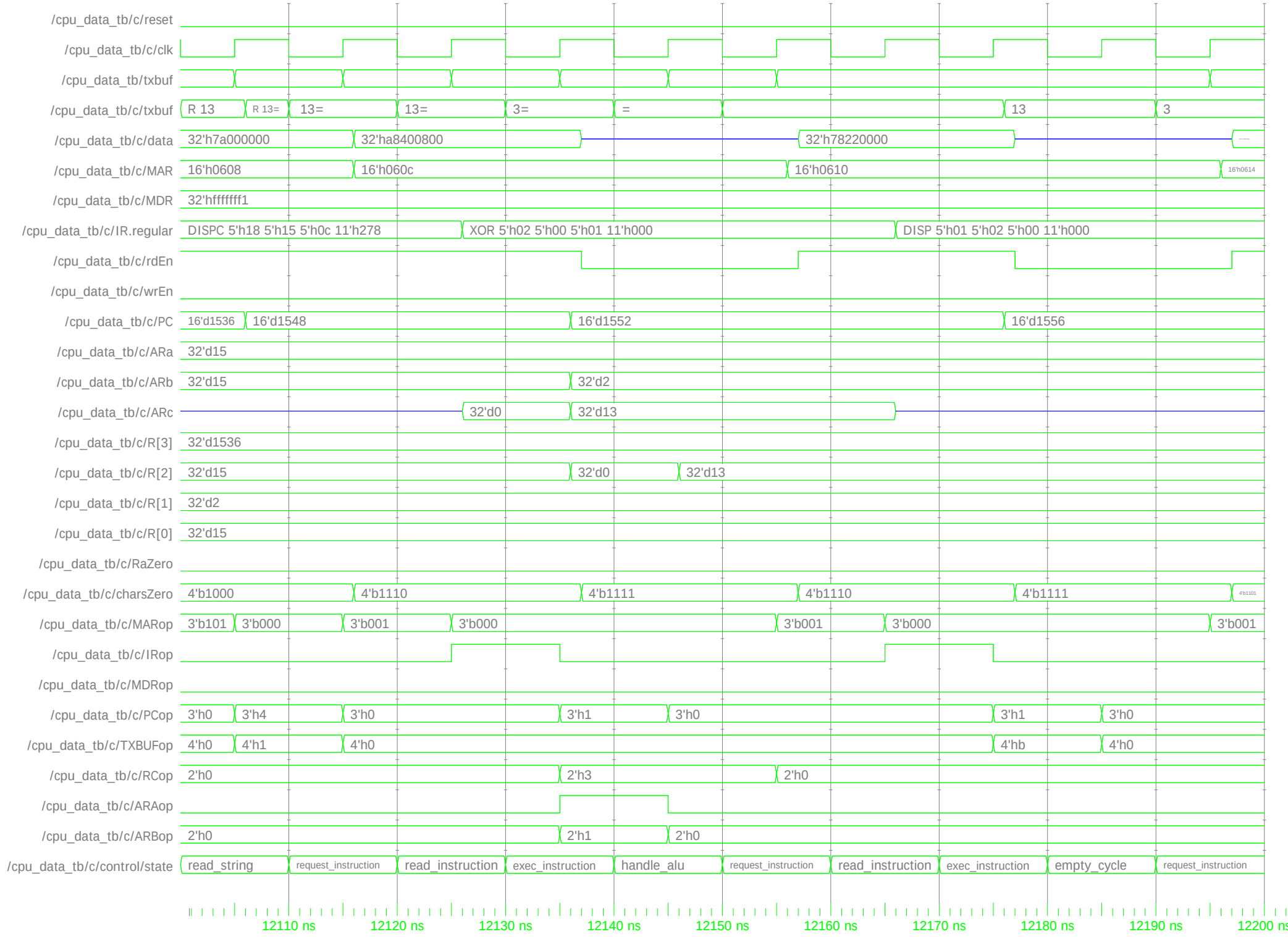

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
OR
OR
OR 15=
R 15=
15=
15=
5=
=
/cpu_data_tb/c/data
32'h40c5abd0
32'h00000000
32'ha4400800
32'h78220000
/cpu_data_tb/c/MAR
16'h05e0
16'h05e4
16'h05e8
16'h05ec
16'h05f0
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h07 11'h690
OR 5'h02 5'h00 5'h01 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1504
16'd1516
16'd1520
/cpu_data_tb/c/ARa
32'd2
32'd15
/cpu_data_tb/c/ARb
32'd2
/cpu_data_tb/c/ARc
32'd2
32'd15
/cpu_data_tb/c/R[3]
32'd1504
/cpu_data_tb/c/R[2]
32'd2
32'd15
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b0000
4'b1110
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h7
4'h0
4'h4
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
11810 ns
11820 ns
11830 ns
11840 ns
11850 ns
11860 ns
11870 ns
11880 ns
11890 ns
11900 ns

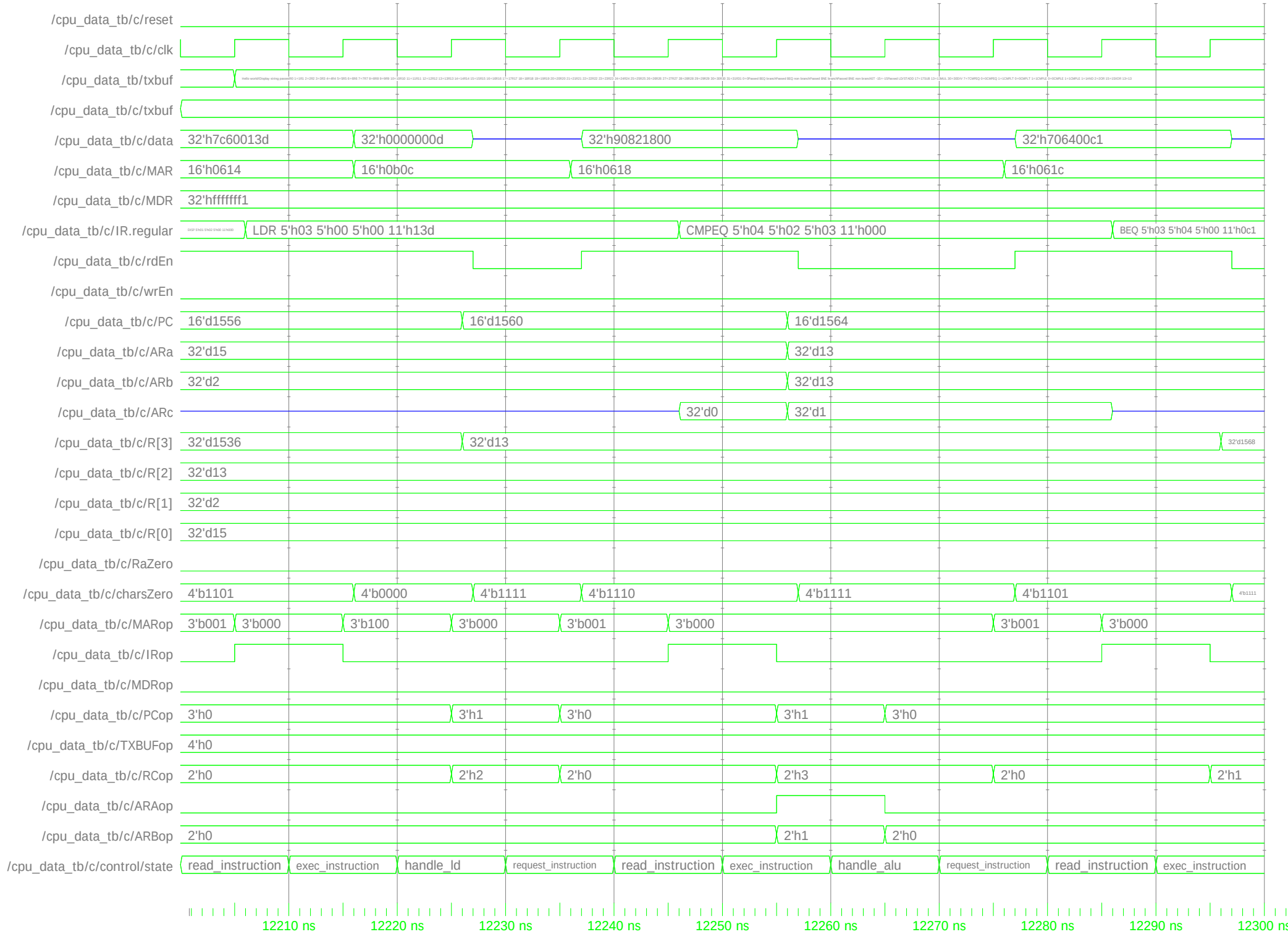


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 120 Page: 120

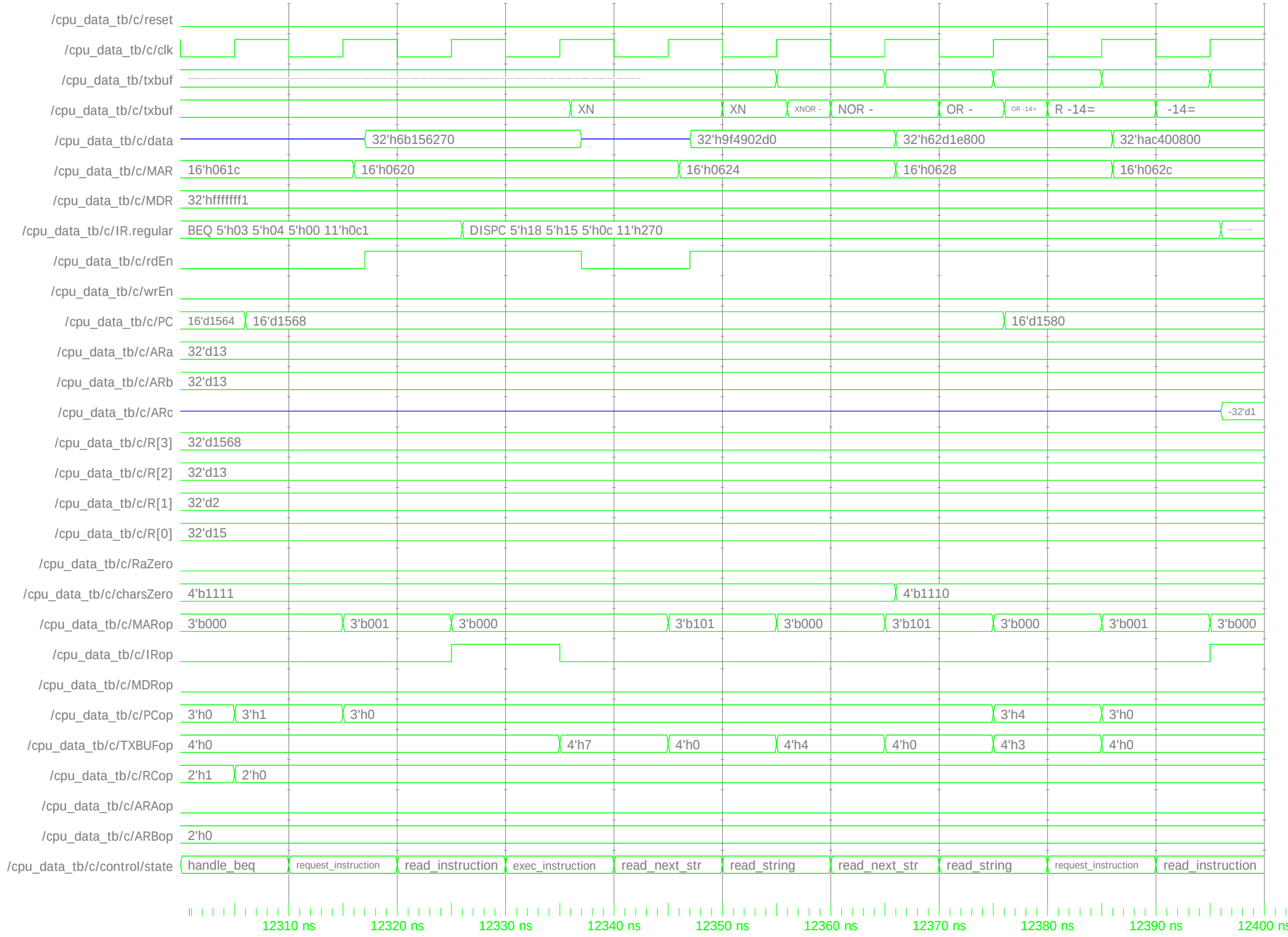


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 121 Page: 121

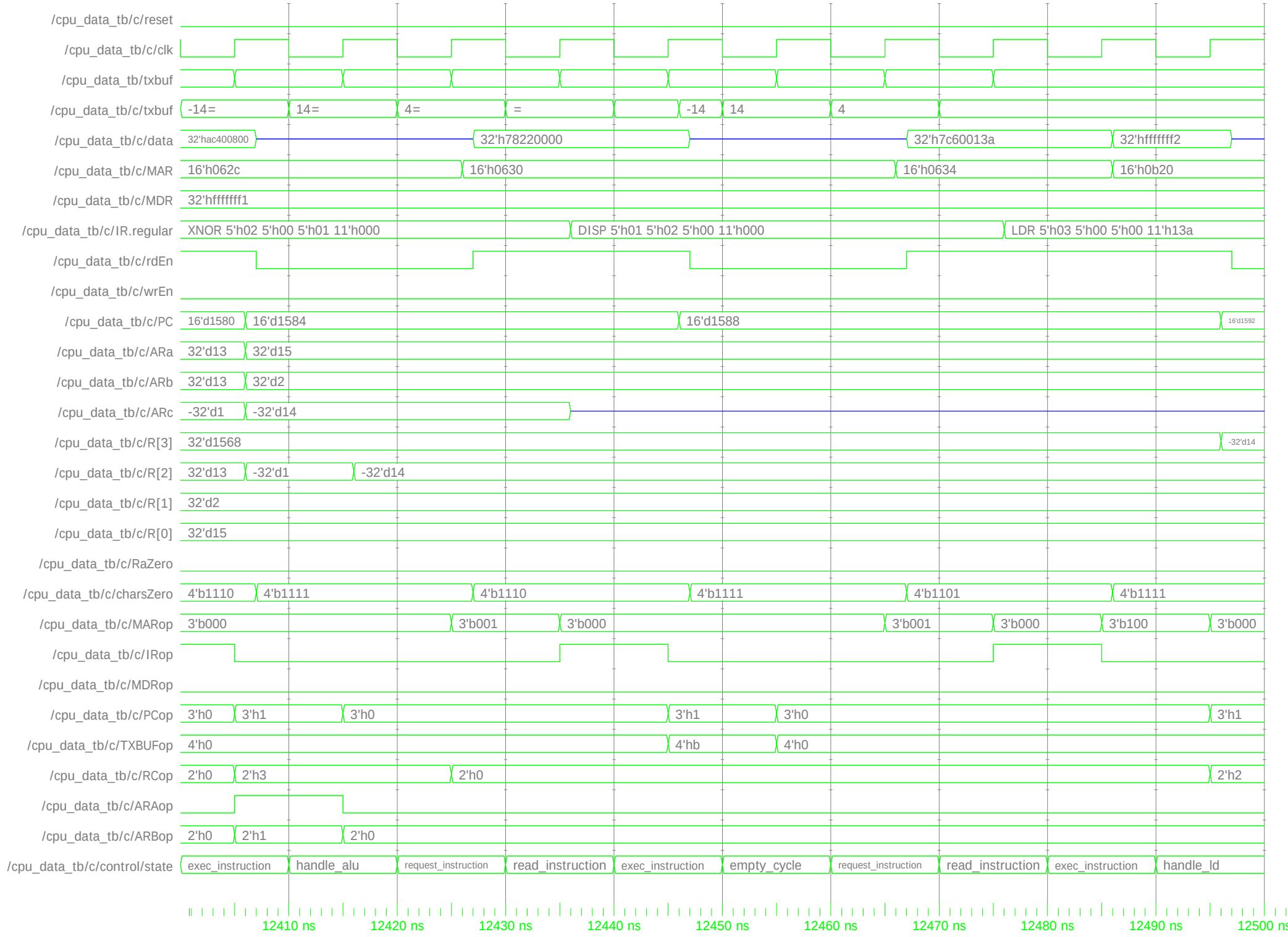

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
R 13
R 13=
13=
13=
3=
=
13
3
/cpu_data_tb/c/data
32'h7a000000
32'ha8400800
32'h78220000
/cpu_data_tb/c/MAR
16'h0608
16'h060c
16'h0610
16'h0614
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h0c 11'h278
XOR 5'h02 5'h00 5'h01 11'h000
DISP 5'h01 5'h02 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1536
16'd1548
16'd1552
16'd1556
/cpu_data_tb/c/ARa
32'd15
/cpu_data_tb/c/ARb
32'd15
32'd2
/cpu_data_tb/c/ARc
32'd0
32'd13
/cpu_data_tb/c/R[3]
32'd1536
/cpu_data_tb/c/R[2]
32'd15
32'd0
32'd13
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1000
4'b1110
4'b1111
4'b1110
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
12110 ns
12120 ns
12130 ns
12140 ns
12150 ns
12160 ns
12170 ns
12180 ns
12190 ns
12200 ns



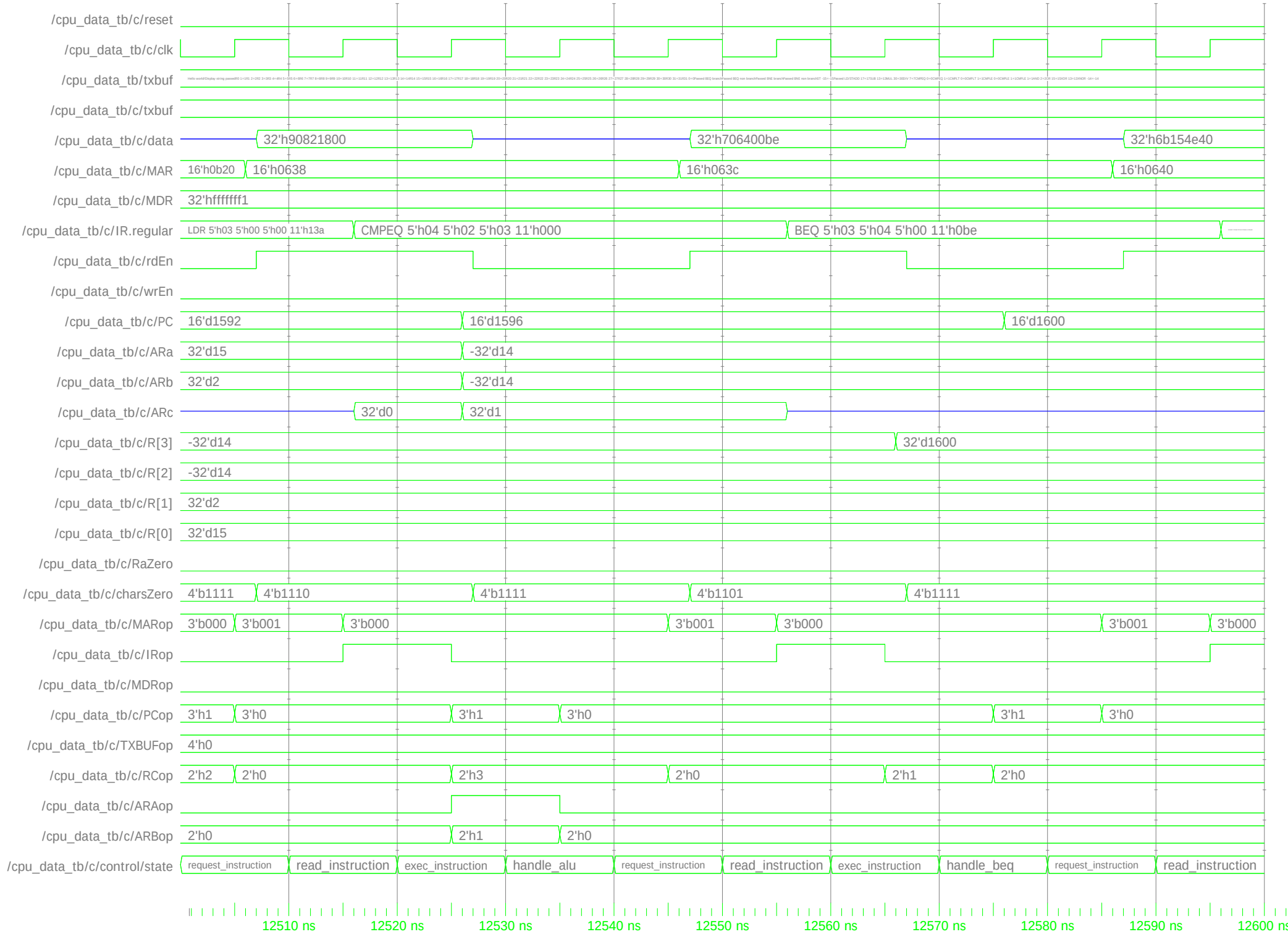
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 123 Page: 123

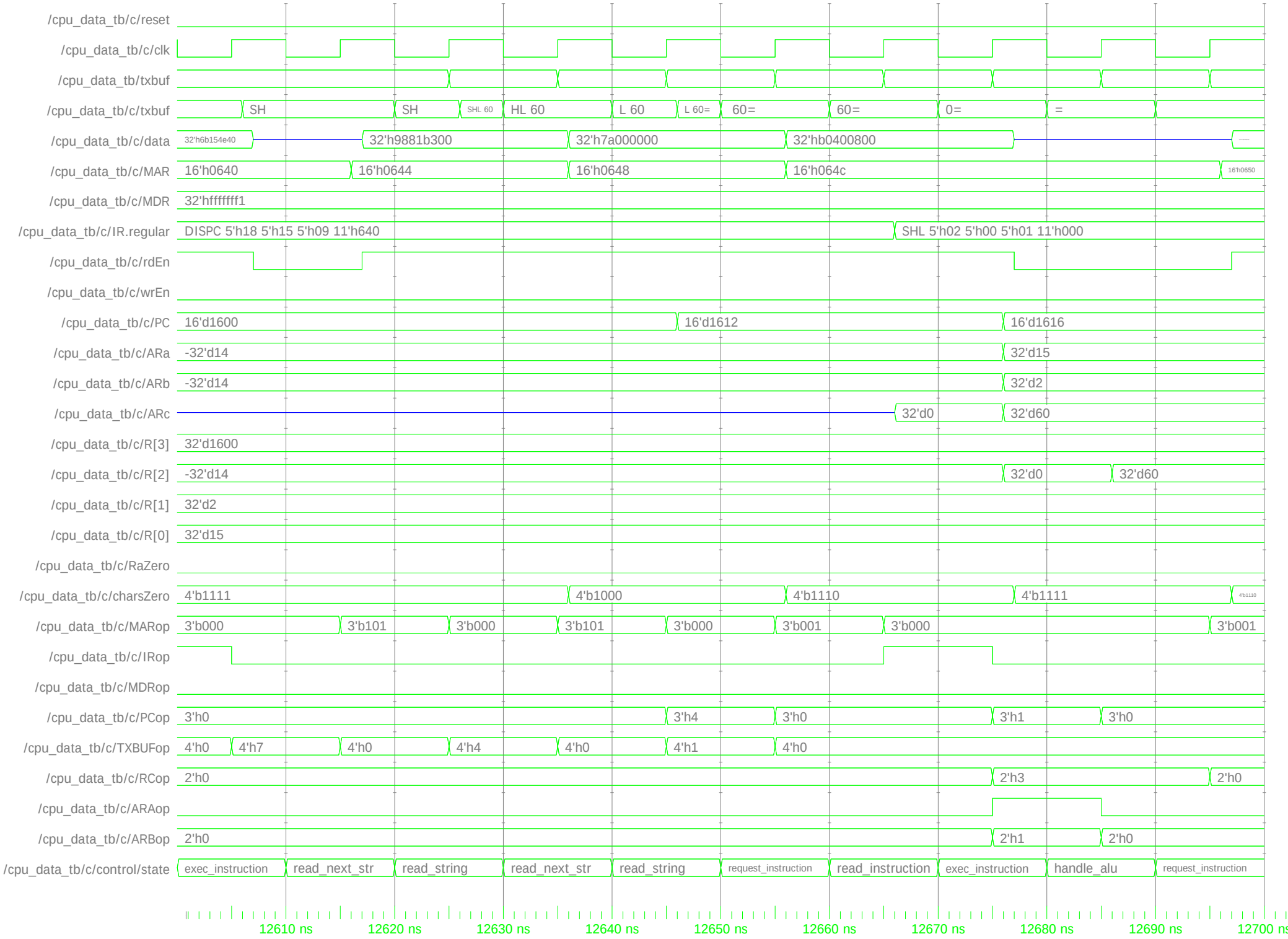


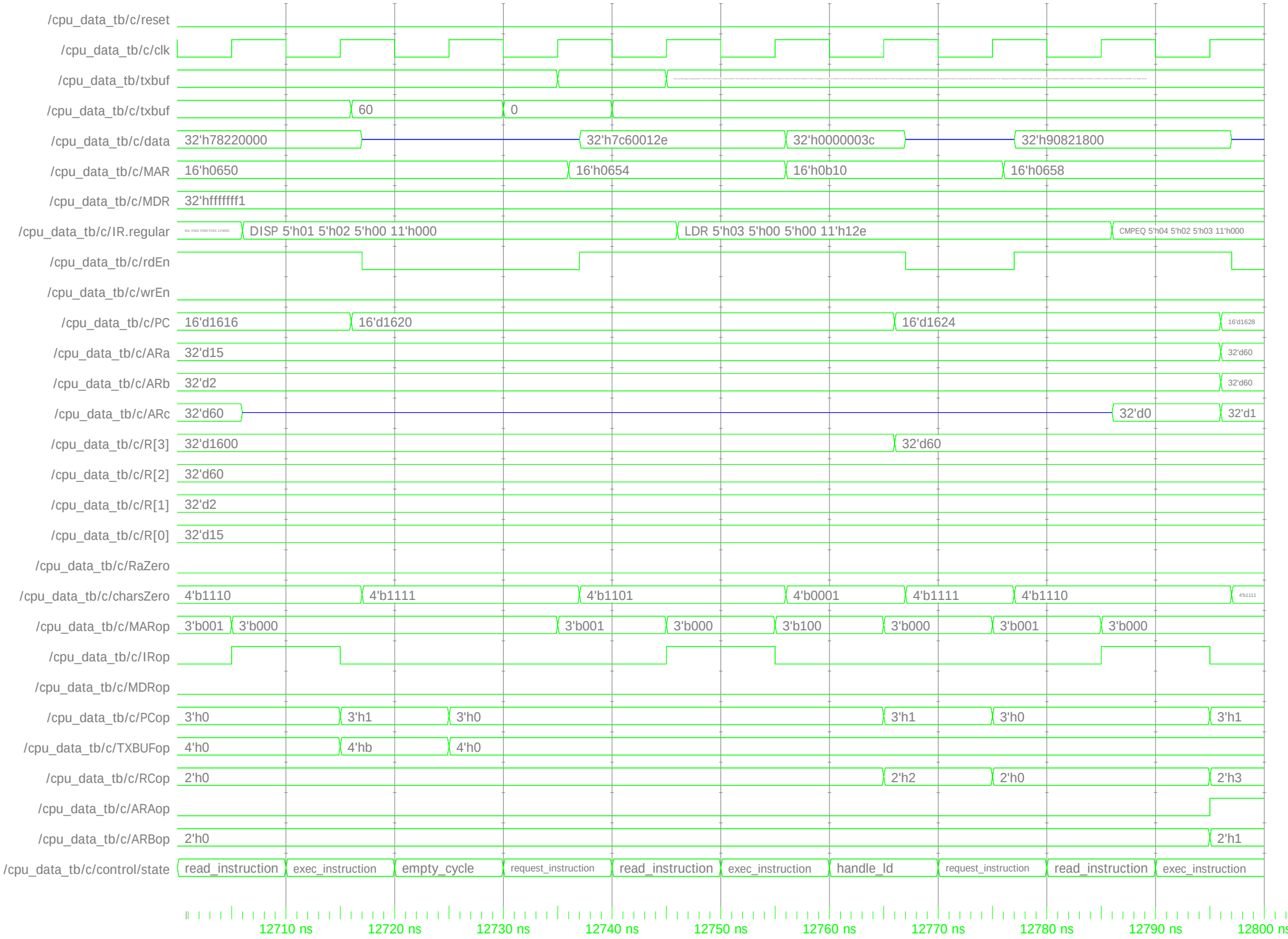
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 124 Page: 124



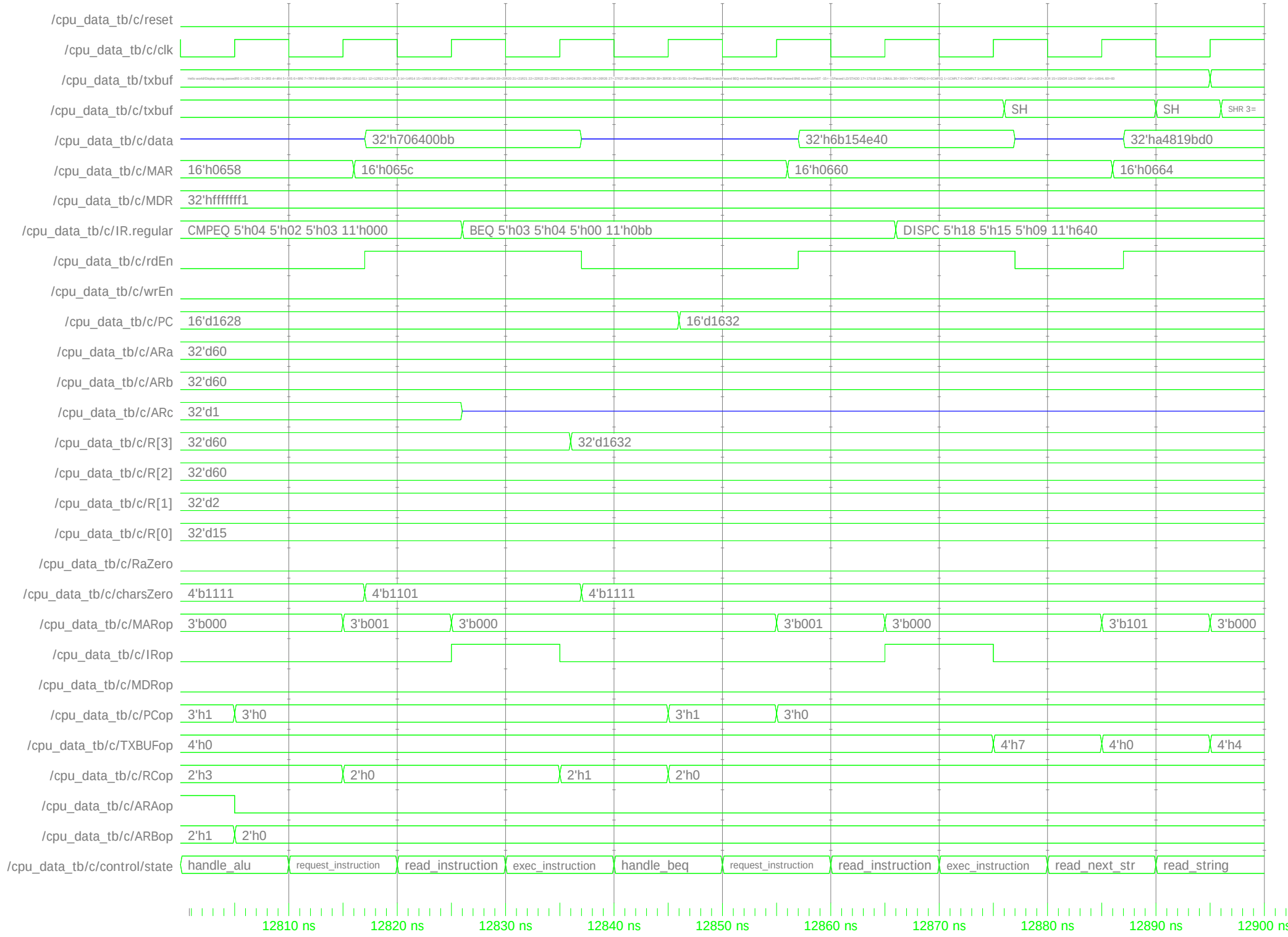
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 125 Page: 125


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h90821800
32'h706400be
32'h6b154e40
/cpu_data_tb/c/MAR
16'h0b20
16'h0638
16'h063c
16'h0640
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h13a
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0be
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1592
16'd1596
16'd1600
/cpu_data_tb/c/ARa
32'd15
-32'd14
/cpu_data_tb/c/ARb
32'd2
-32'd14
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
-32'd14
32'd1600
/cpu_data_tb/c/R[2]
-32'd14
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
12510 ns
12520 ns
12530 ns
12540 ns
12550 ns
12560 ns
12570 ns
12580 ns
12590 ns
12600 ns

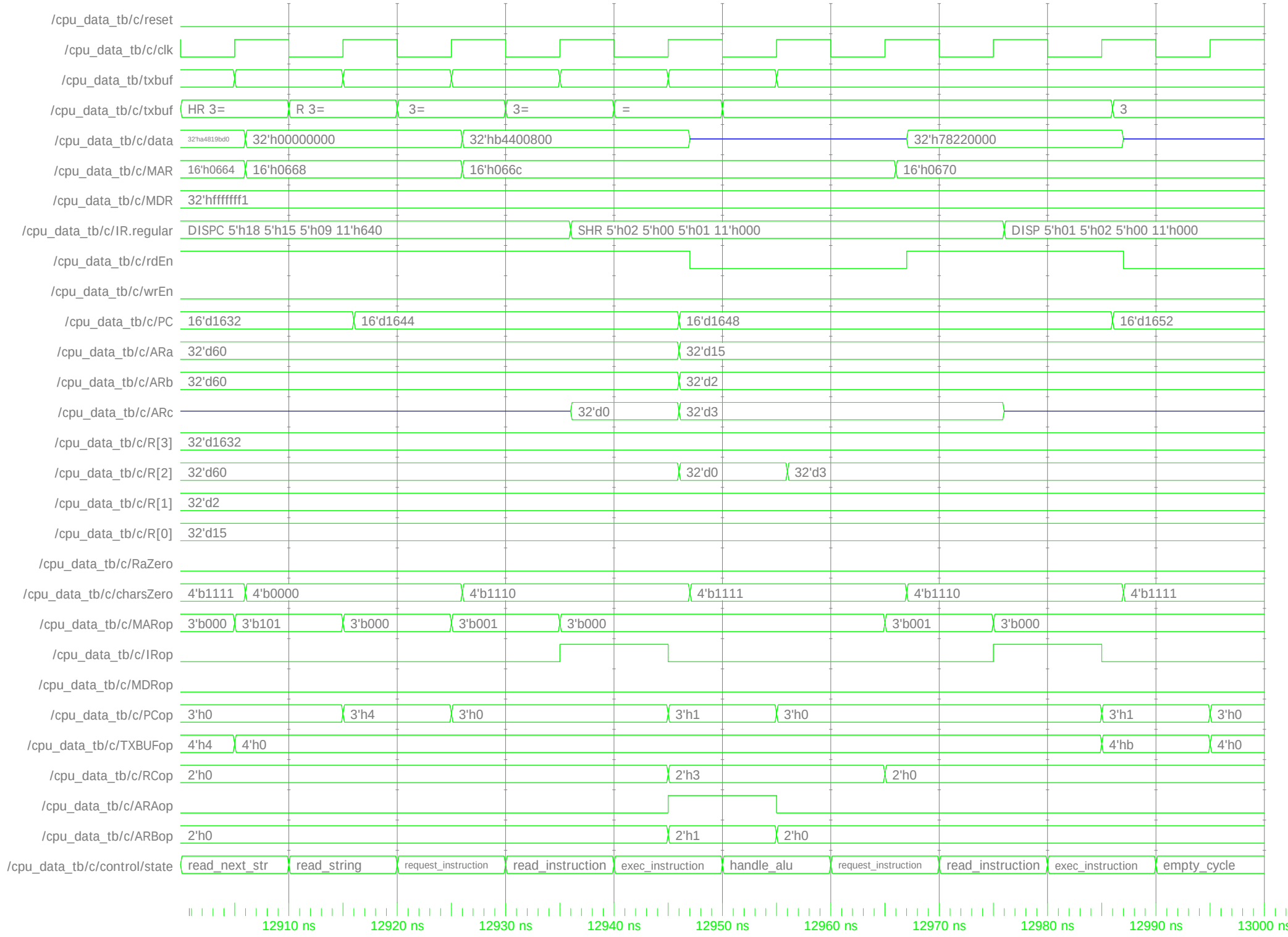

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
SH
SH
SHL 60
HL 60
L 60
L 60=
60=
60=
0=
=
/cpu_data_tb/c/data
32'h6b154e40
32'h9881b300
32'h7a000000
32'hb0400800
/cpu_data_tb/c/MAR
16'h0640
16'h0644
16'h0648
16'h064c
16'h0650
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h09 11'h640
SHL 5'h02 5'h00 5'h01 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1600
16'd1612
16'd1616
/cpu_data_tb/c/ARa
-32'd14
32'd15
/cpu_data_tb/c/ARb
-32'd14
32'd2
/cpu_data_tb/c/ARc
32'd0
32'd60
/cpu_data_tb/c/R[3]
32'd1600
/cpu_data_tb/c/R[2]
-32'd14
32'd0
32'd60
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1110
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
12610 ns
12620 ns
12630 ns
12640 ns
12650 ns
12660 ns
12670 ns
12680 ns
12690 ns
12700 ns



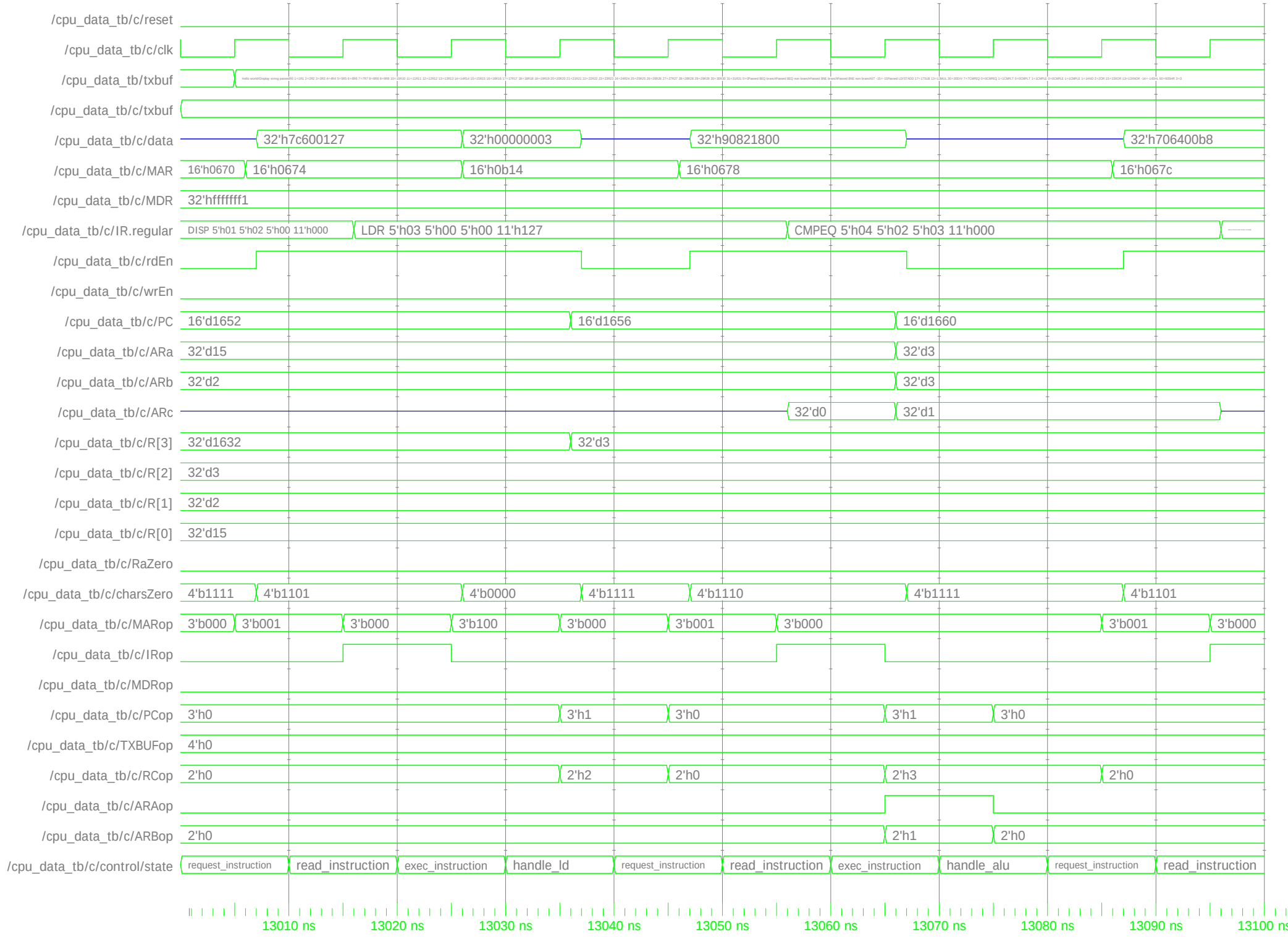
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 128 Page: 128

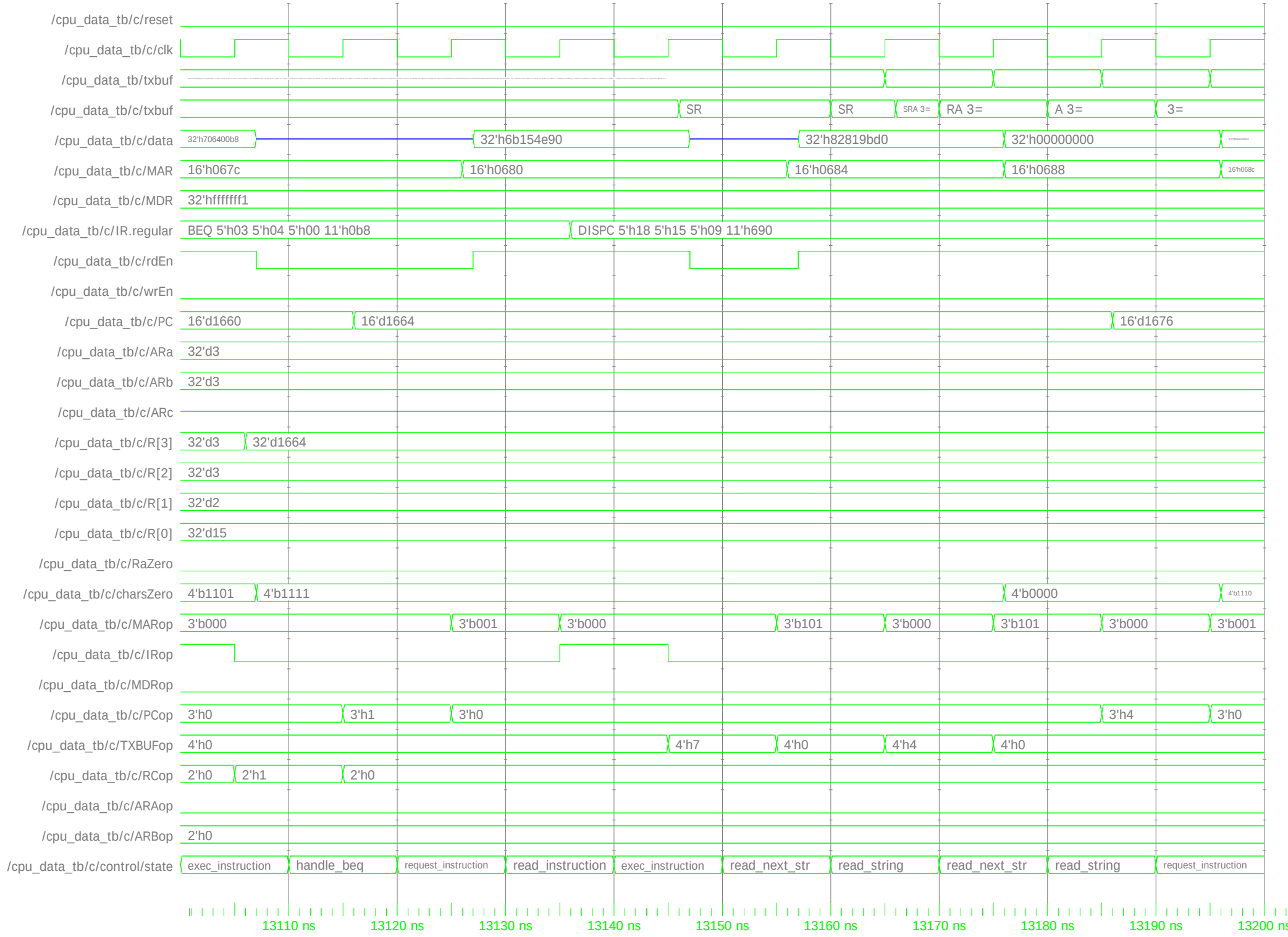


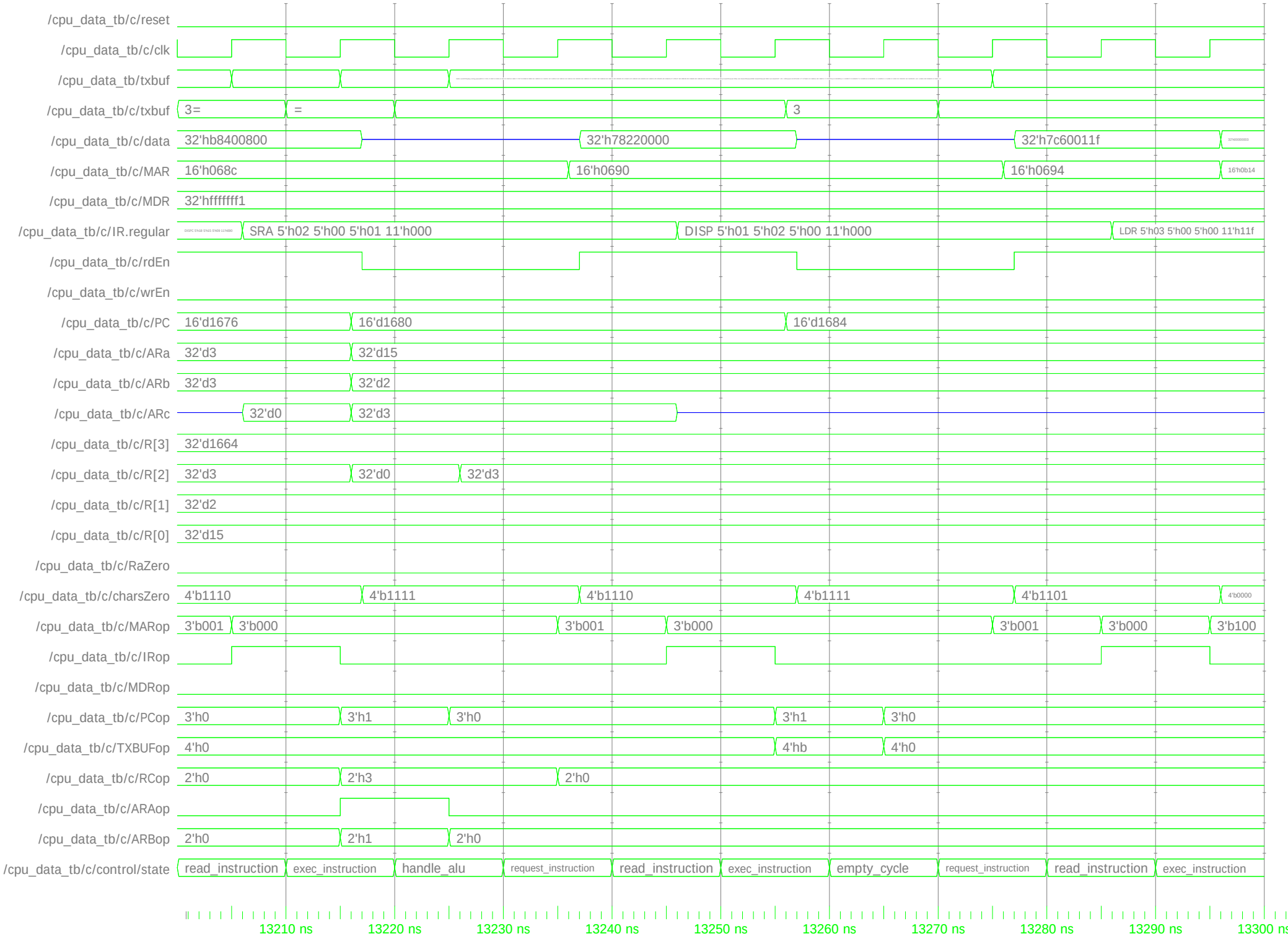
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 129 Page: 129



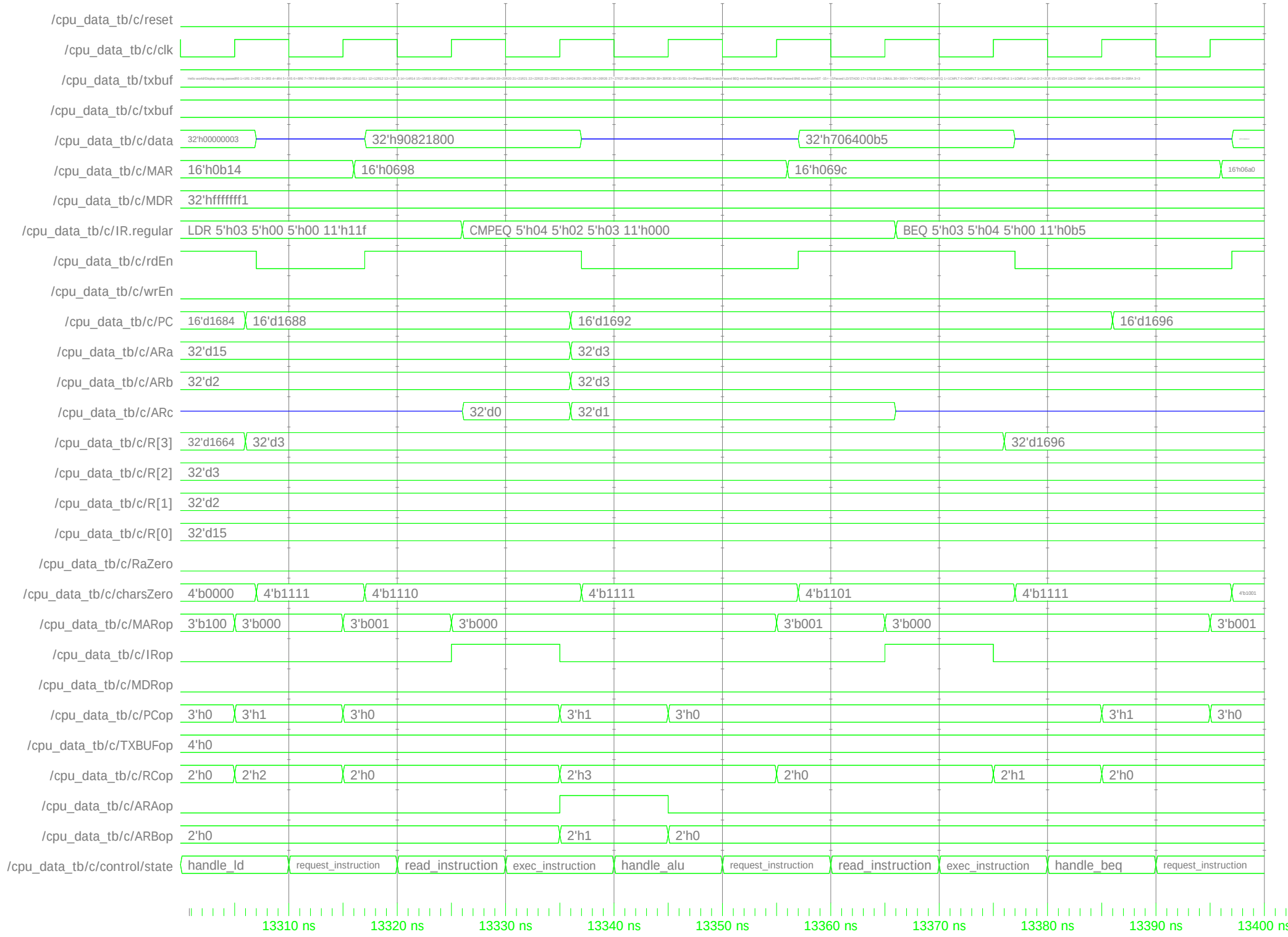
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 130 Page: 130

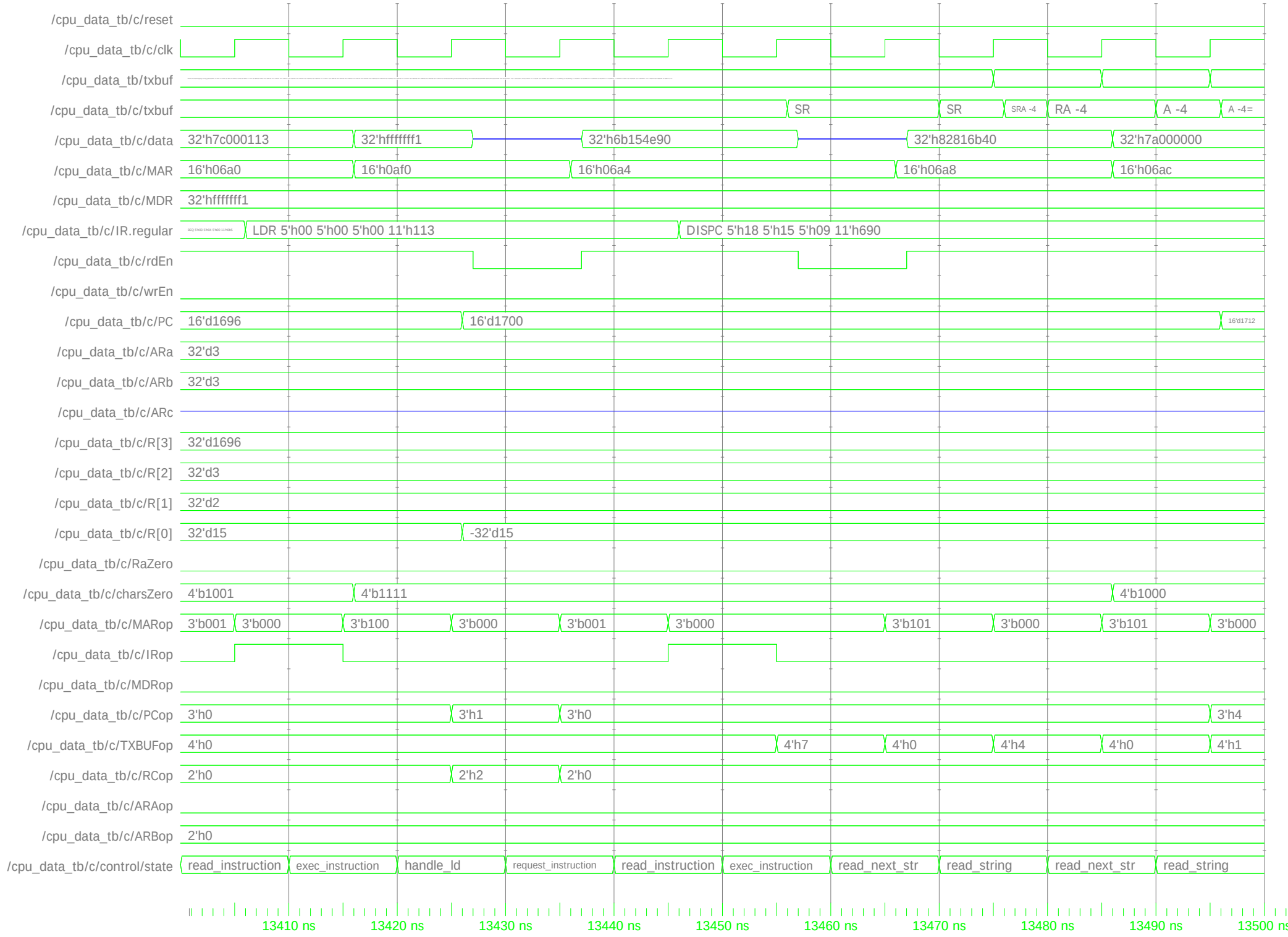

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h7c600127
32'h00000003
32'h90821800
32'h706400b8
/cpu_data_tb/c/MAR
16'h0670
16'h0674
16'h0b14
16'h0678
16'h067c
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h02 5'h00 11'h000
LDR 5'h03 5'h00 5'h00 11'h127
CMPEQ 5'h04 5'h02 5'h03 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1652
16'd1656
16'd1660
/cpu_data_tb/c/ARa
32'd15
32'd3
/cpu_data_tb/c/ARb
32'd2
32'd3
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1632
32'd3
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b0000
4'b1111
4'b1110
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
13010 ns
13020 ns
13030 ns
13040 ns
13050 ns
13060 ns
13070 ns
13080 ns
13090 ns
13100 ns

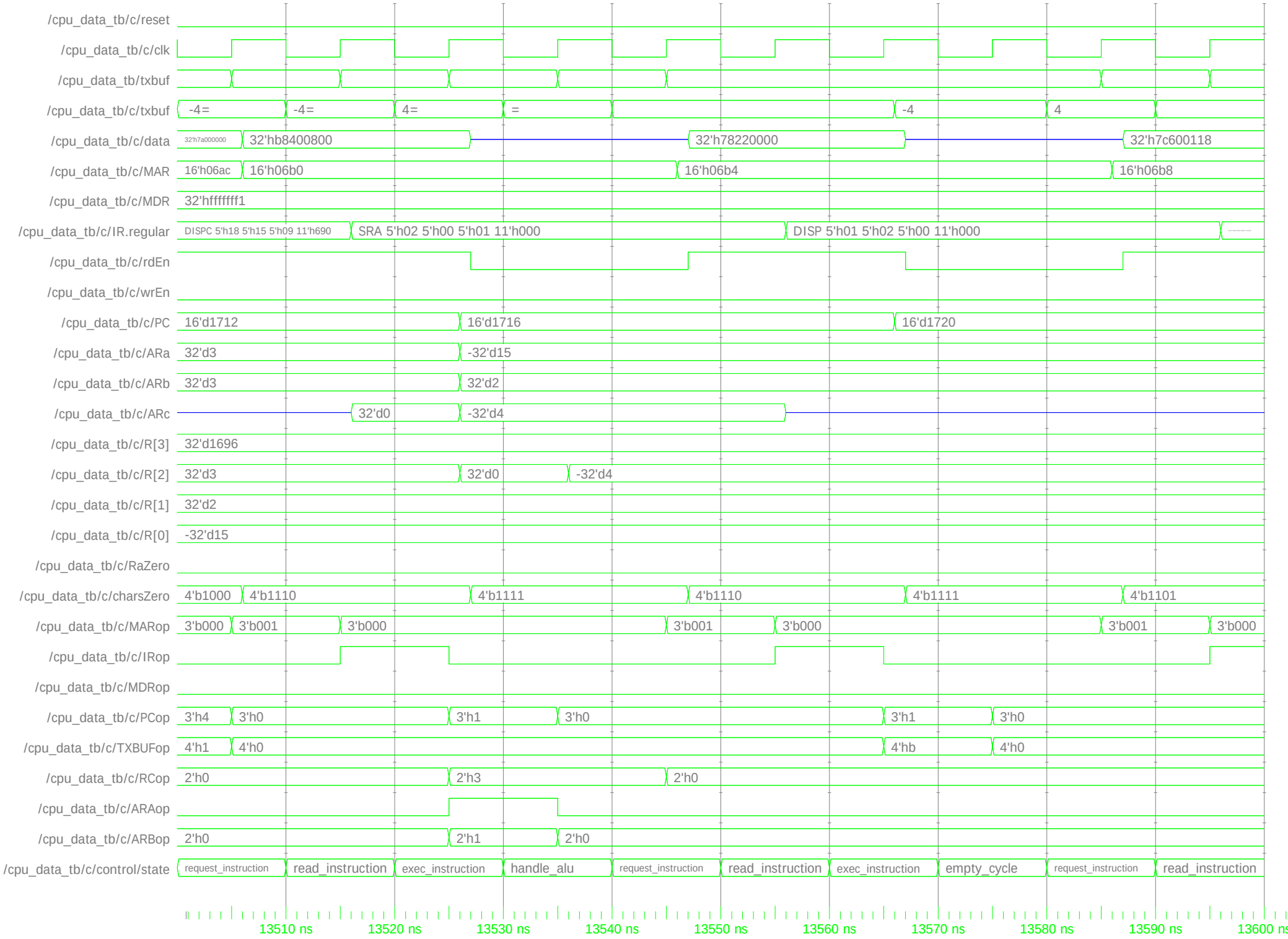

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
SR
SR
SRA 3=
RA 3=
A 3=
3=
/cpu_data_tb/c/data
32'h706400b8
32'h6b154e90
32'h82819bd0
32'h00000000
/cpu_data_tb/c/MAR
16'h067c
16'h0680
16'h0684
16'h0688
16'h068c
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h04 5'h00 11'h0b8
DISPC 5'h18 5'h15 5'h09 11'h690
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1660
16'd1664
16'd1676
/cpu_data_tb/c/ARa
32'd3
/cpu_data_tb/c/ARb
32'd3
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd3
32'd1664
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
4'b0000
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
13110 ns
13120 ns
13130 ns
13140 ns
13150 ns
13160 ns
13170 ns
13180 ns
13190 ns
13200 ns



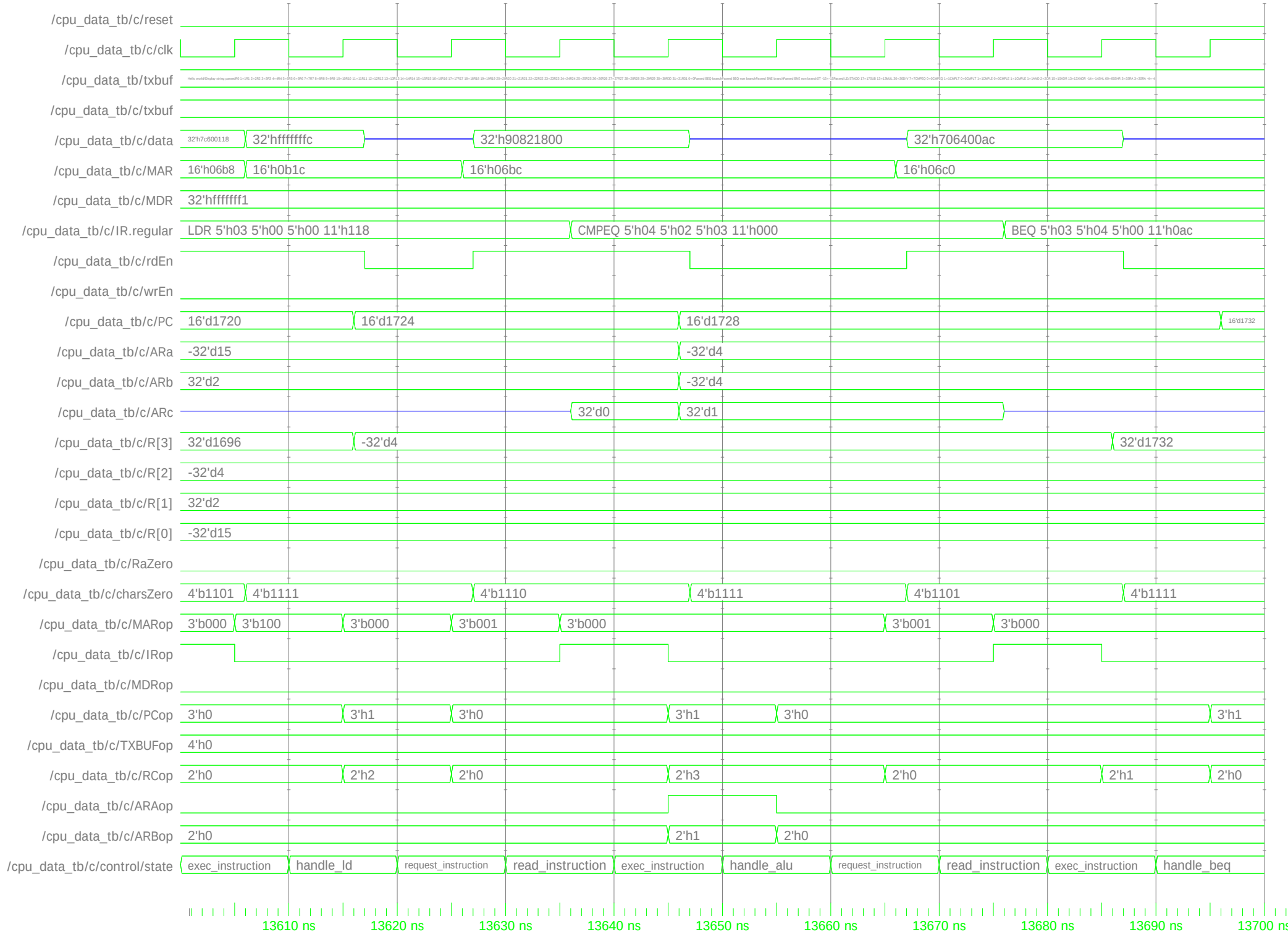
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 133 Page: 133

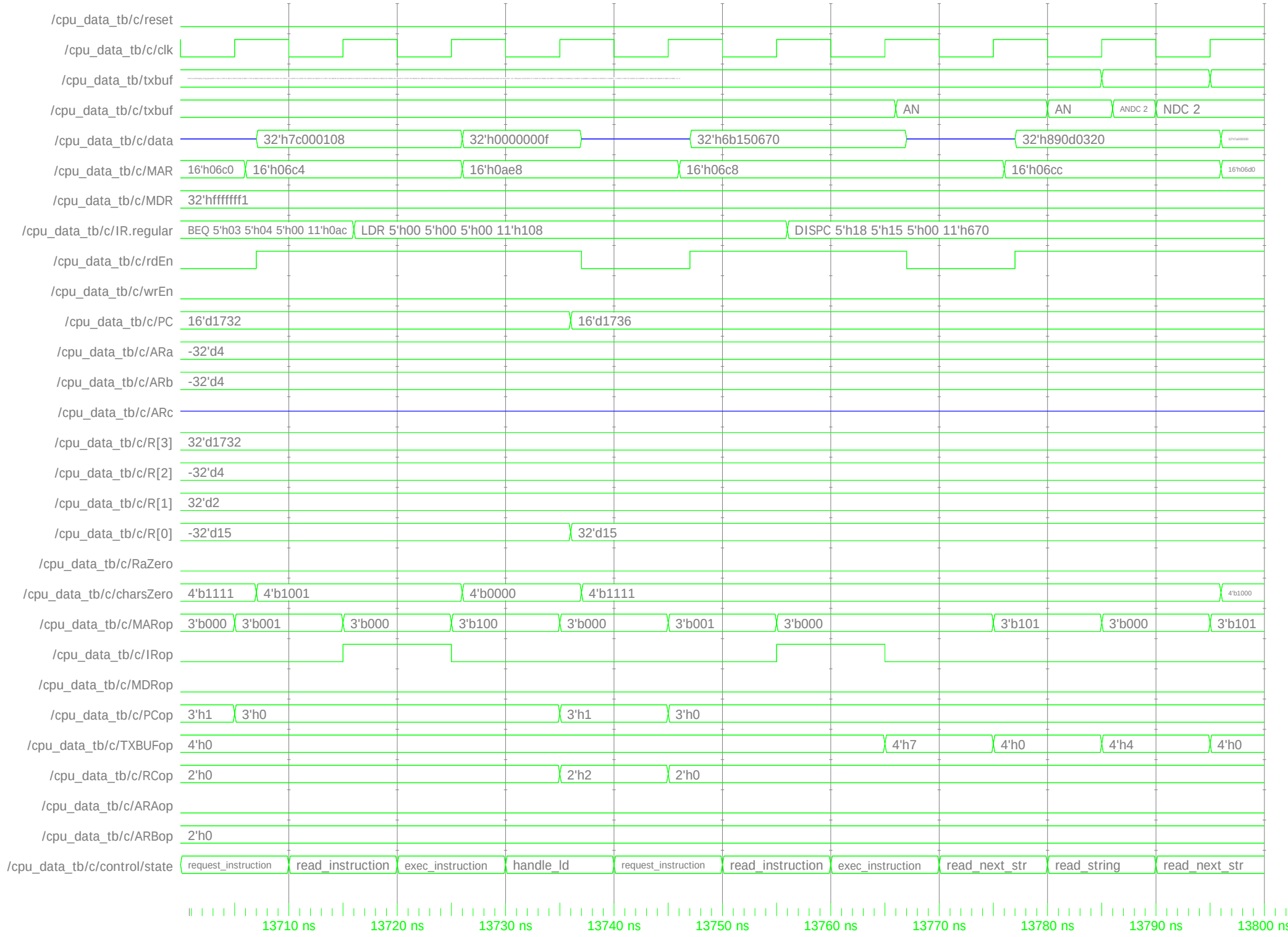

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h00000003
32'h90821800
32'h706400b5
/cpu_data_tb/c/MAR
16'h0b14
16'h0698
16'h069c
16'h06a0
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h11f
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0b5
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1684
16'd1688
16'd1692
16'd1696
/cpu_data_tb/c/ARa
32'd15
32'd3
/cpu_data_tb/c/ARb
32'd2
32'd3
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1664
32'd3
32'd1696
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b0000
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
4'b1001
/cpu_data_tb/c/MARop
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
13310 ns
13320 ns
13330 ns
13340 ns
13350 ns
13360 ns
13370 ns
13380 ns
13390 ns
13400 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
SR
SR
SRA -4
RA -4
A -4
A -4=
/cpu_data_tb/c/data
32'h7c000113
32'hffffffff1
32'h6b154e90
32'h82816b40
32'h7a000000
/cpu_data_tb/c/MAR
16'h06a0
16'h0af0
16'h06a4
16'h06a8
16'h06ac
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h00 5'h00 5'h00 11'h113
DISPC 5'h18 5'h15 5'h09 11'h690
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1696
16'd1700
16'd1712
/cpu_data_tb/c/ARa
32'd3
/cpu_data_tb/c/ARb
32'd3
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd1696
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
-32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1001
4'b1111
4'b1000
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
13410 ns
13420 ns
13430 ns
13440 ns
13450 ns
13460 ns
13470 ns
13480 ns
13490 ns
13500 ns

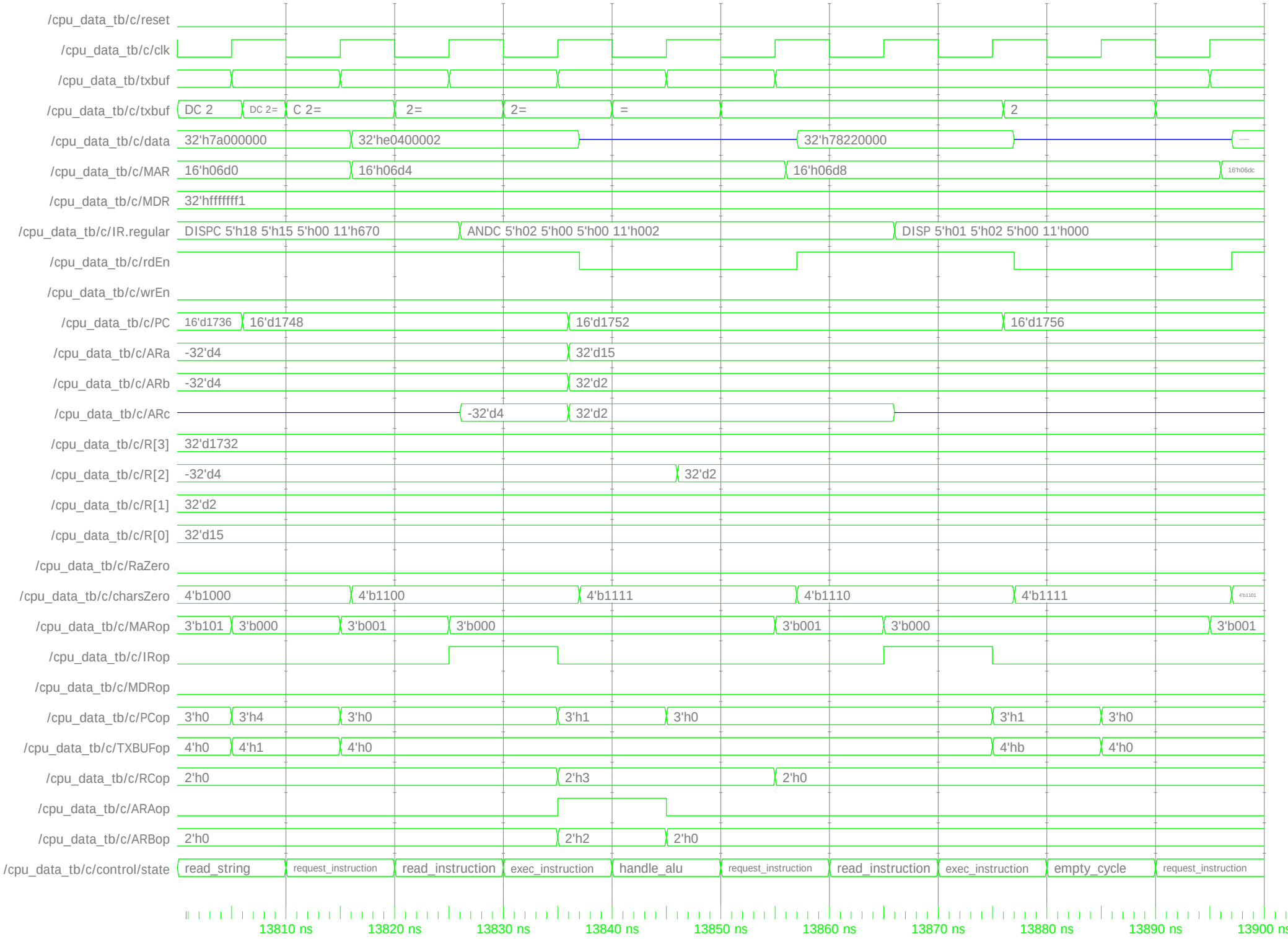


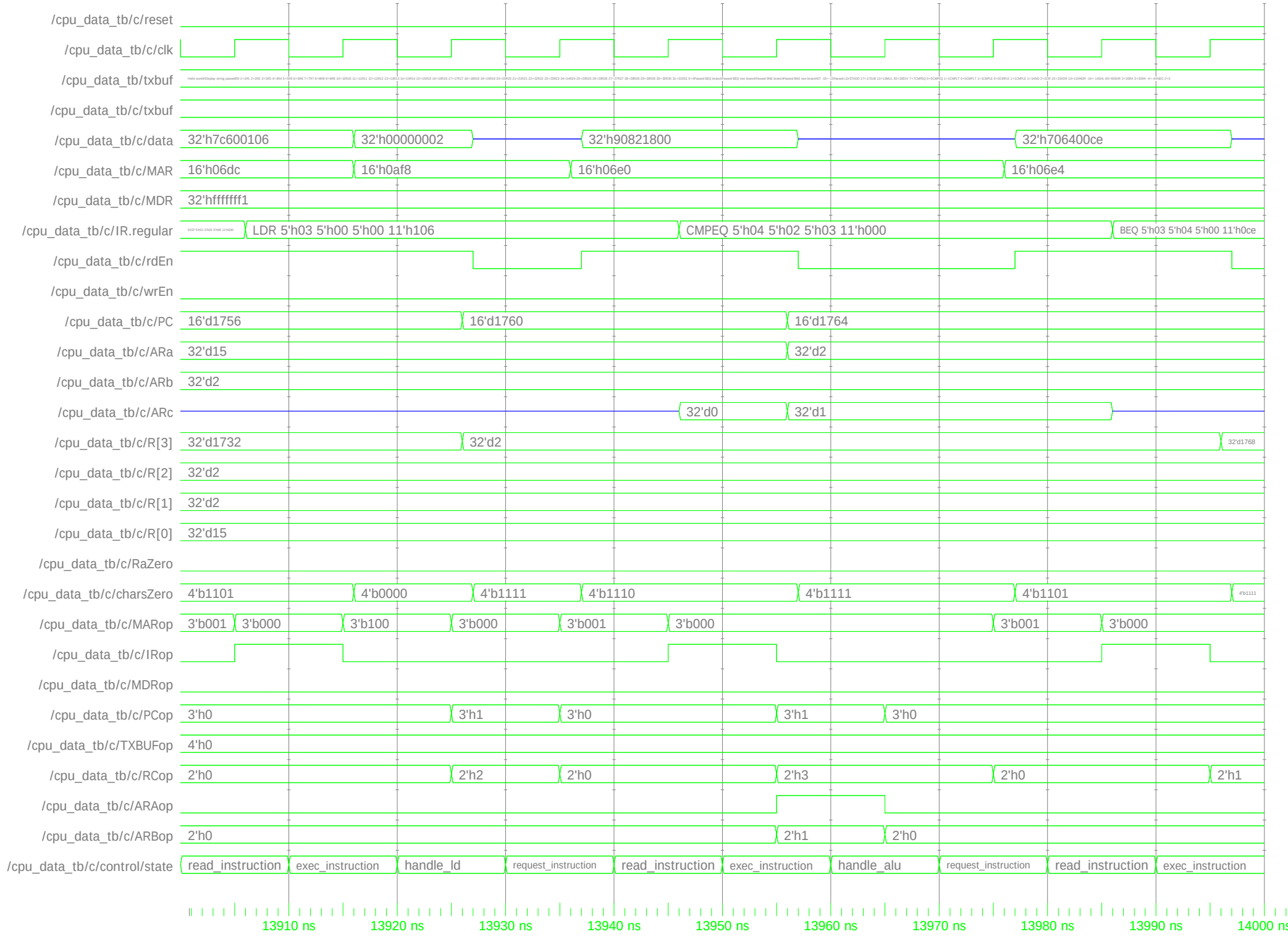
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 136 Page: 136

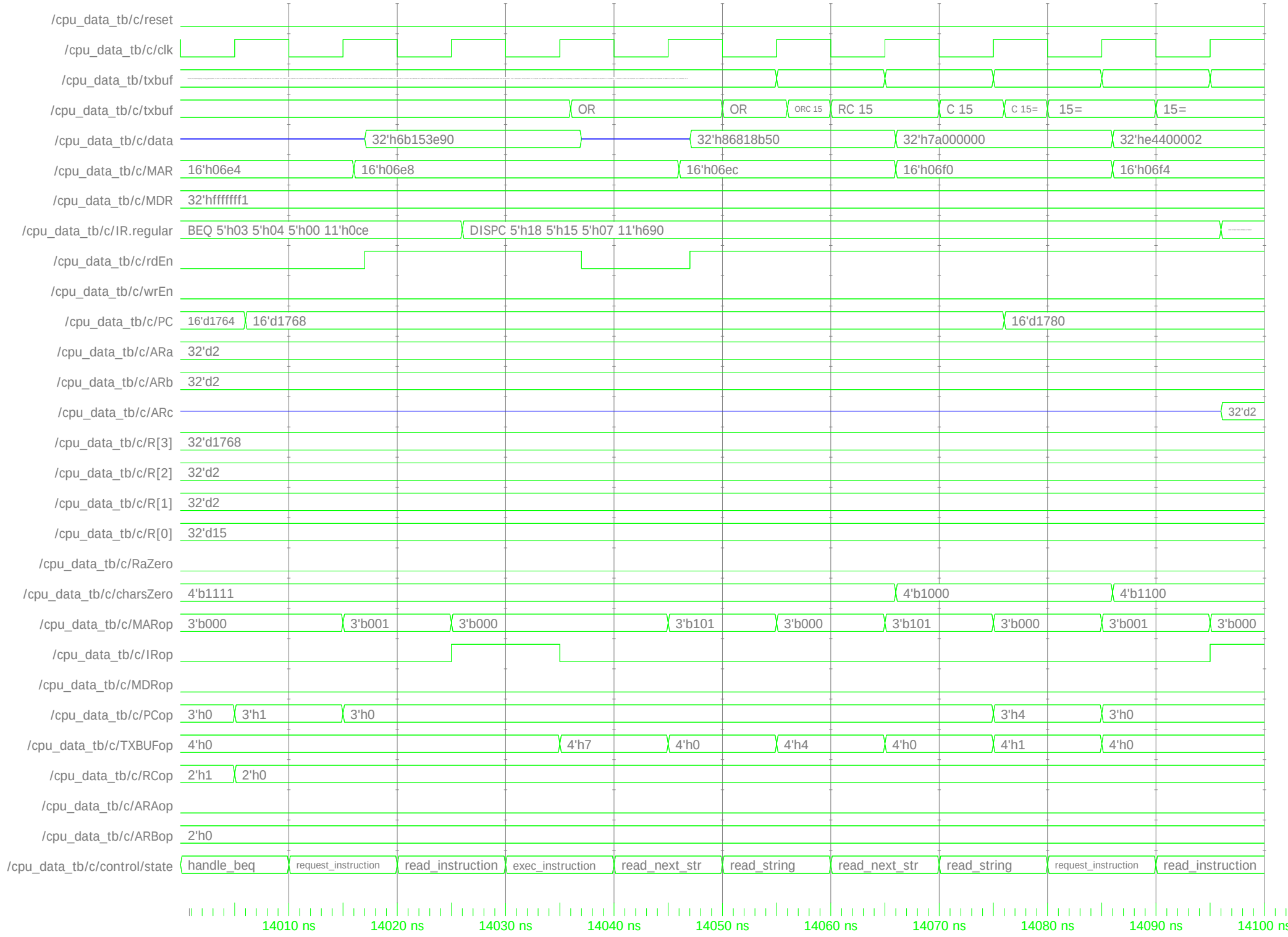

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h7c600118
32'hfffffffc
32'h90821800
32'h706400ac
/cpu_data_tb/c/MAR
16'h06b8
16'h0b1c
16'h06bc
16'h06c0
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h118
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0ac
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1720
16'd1724
16'd1728
16'd1732
/cpu_data_tb/c/ARa
-32'd15
-32'd4
/cpu_data_tb/c/ARb
32'd2
-32'd4
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1696
-32'd4
32'd1732
/cpu_data_tb/c/R[2]
-32'd4
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
-32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
13610 ns
13620 ns
13630 ns
13640 ns
13650 ns
13660 ns
13670 ns
13680 ns
13690 ns
13700 ns

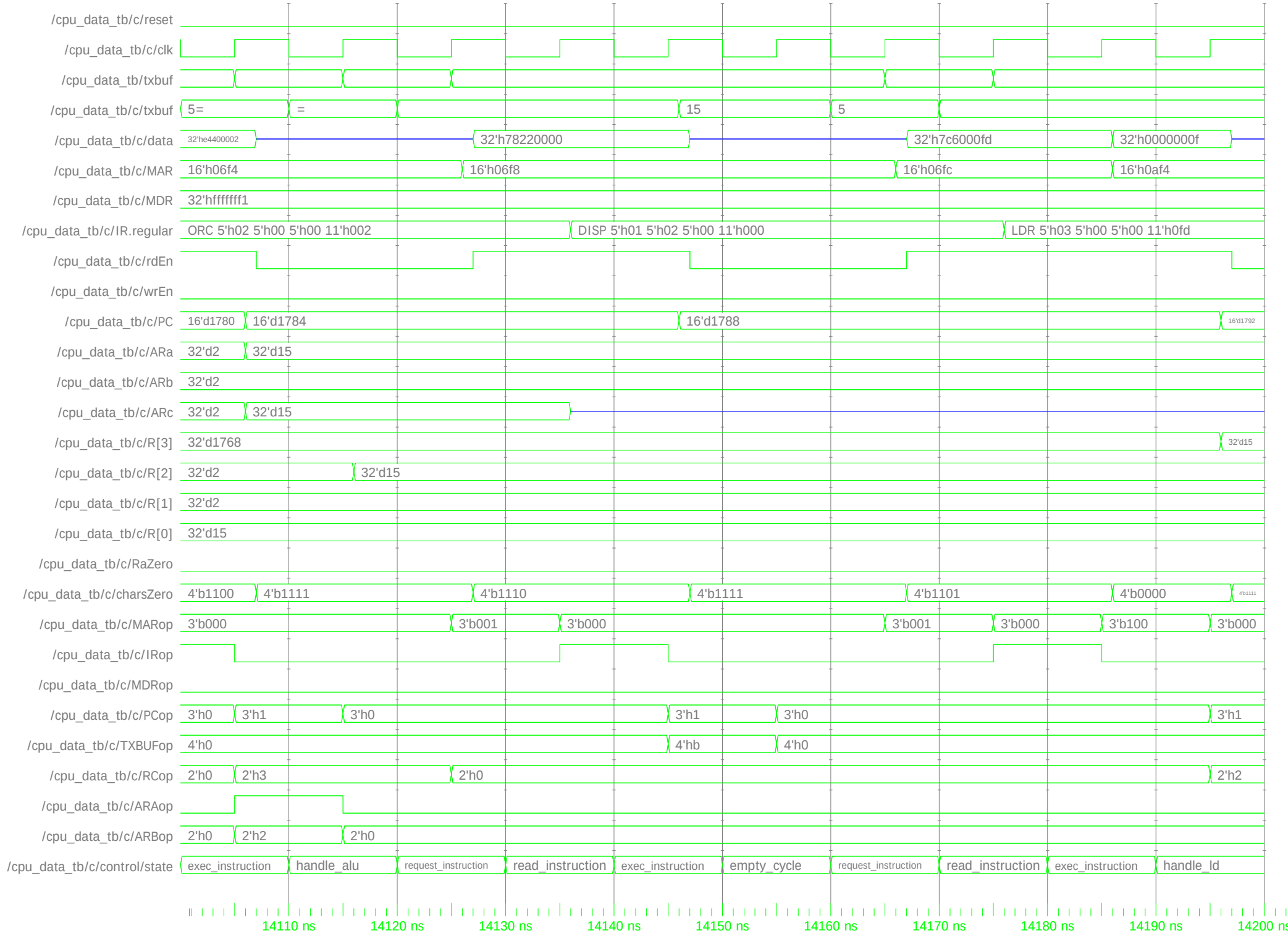


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 138 Page: 138

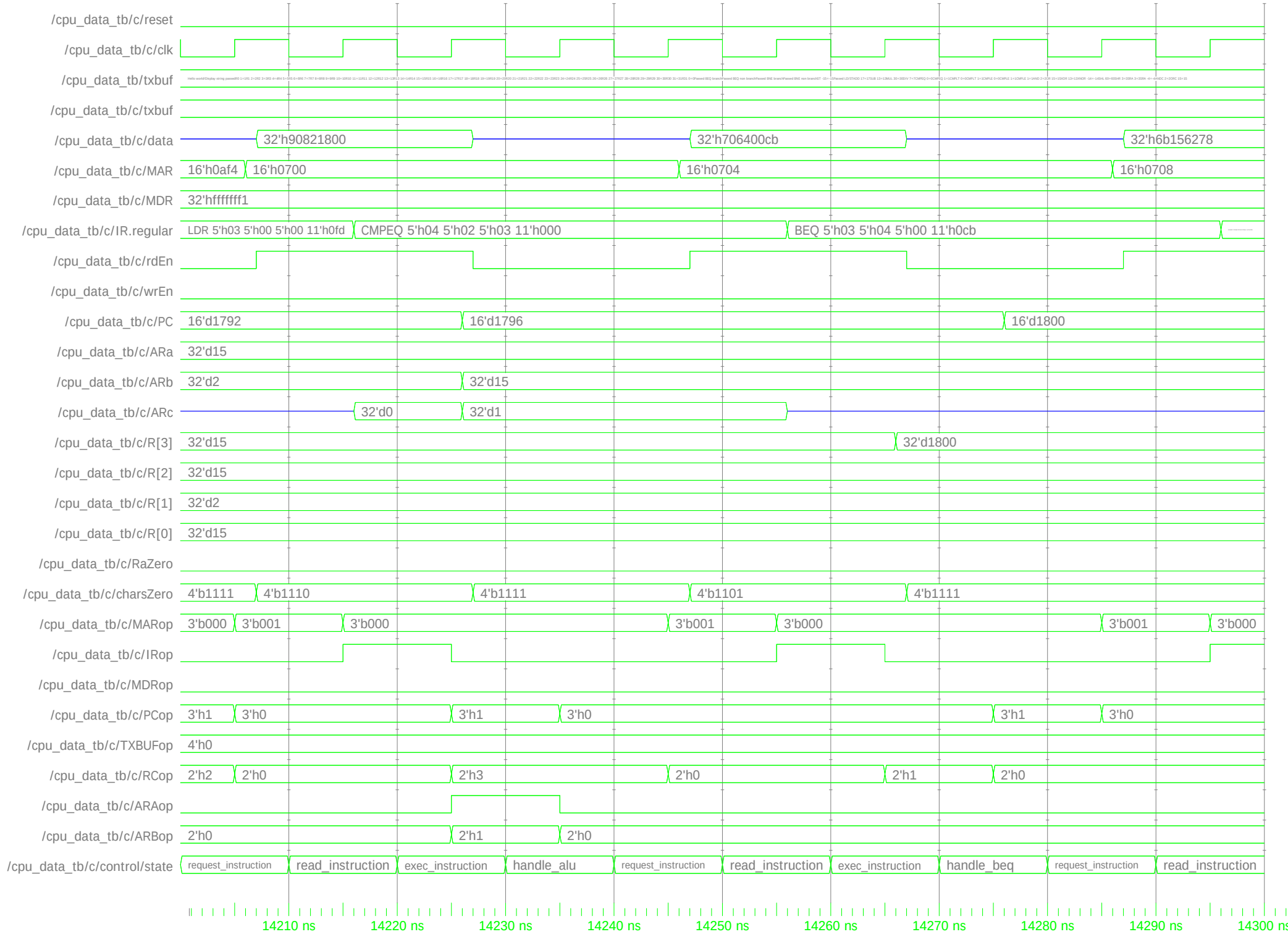

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
DC 2
DC 2=
C 2=
2=
2=
=
2
/cpu_data_tb/c/data
32'h7a000000
32'he0400002
32'h78220000
/cpu_data_tb/c/MAR
16'h06d0
16'h06d4
16'h06d8
16'h06dc
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h00 11'h670
ANDC 5'h02 5'h00 5'h00 11'h002
DISP 5'h01 5'h02 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1736
16'd1748
16'd1752
16'd1756
/cpu_data_tb/c/ARa
-32'd4
32'd15
/cpu_data_tb/c/ARb
-32'd4
32'd2
/cpu_data_tb/c/ARc
-32'd4
32'd2
/cpu_data_tb/c/R[3]
32'd1732
/cpu_data_tb/c/R[2]
-32'd4
32'd2
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1000
4'b1100
4'b1111
4'b1110
4'b1111
4'b1101
/cpu_data_tb/c/MARop
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h1
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
empty_cycle
request_instruction
13810 ns
13820 ns
13830 ns
13840 ns
13850 ns
13860 ns
13870 ns
13880 ns
13890 ns
13900 ns

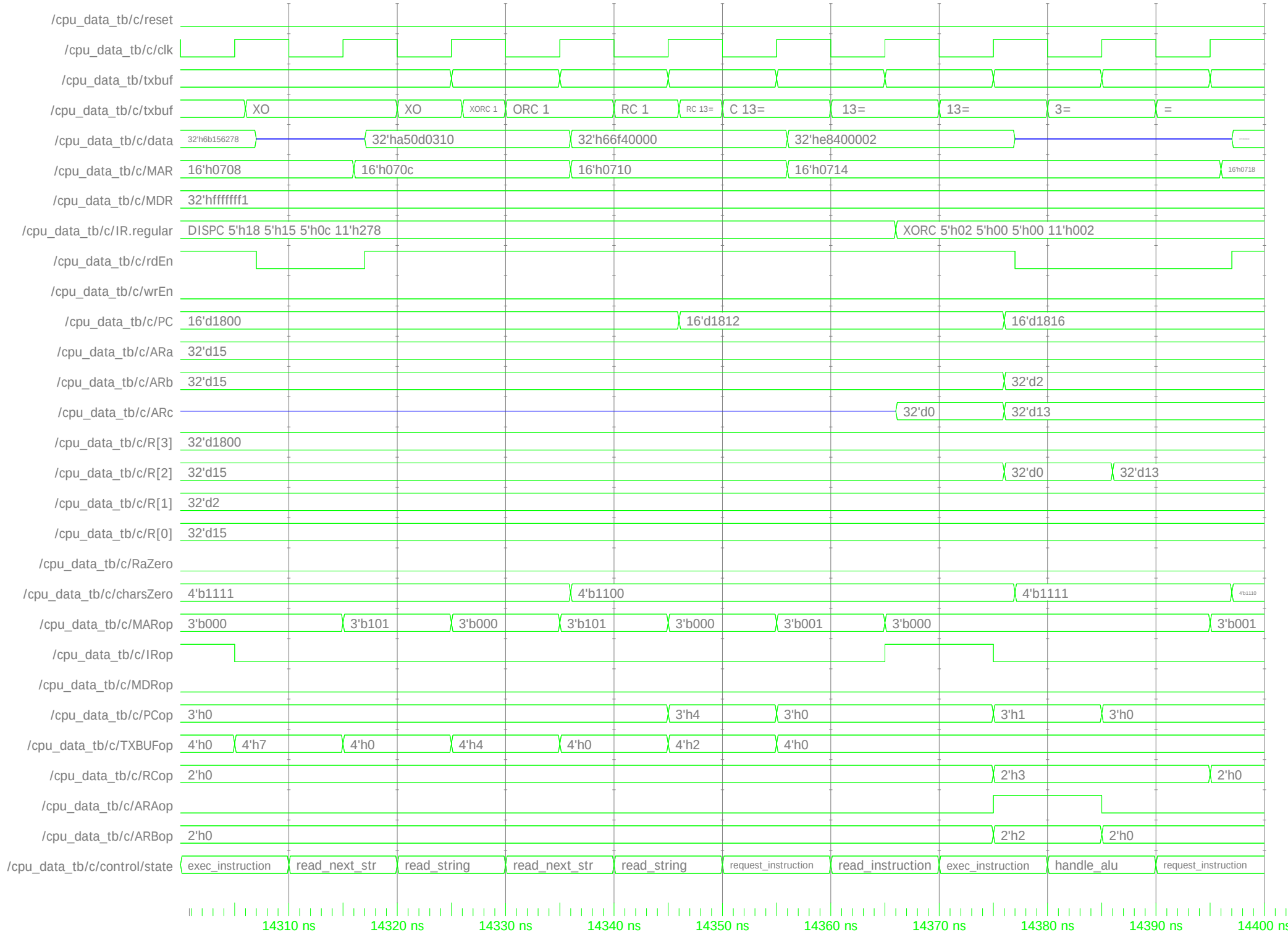

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h7c600106
32'h00000002
32'h90821800
32'h706400ce
/cpu_data_tb/c/MAR
16'h06dc
16'h0af8
16'h06e0
16'h06e4
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h106
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0ce
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1756
16'd1760
16'd1764
/cpu_data_tb/c/ARa
32'd15
32'd2
/cpu_data_tb/c/ARb
32'd2
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1732
32'd2
32'd1768
/cpu_data_tb/c/R[2]
32'd2
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b0000
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
2'h1
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
13910 ns
13920 ns
13930 ns
13940 ns
13950 ns
13960 ns
13970 ns
13980 ns
13990 ns
14000 ns

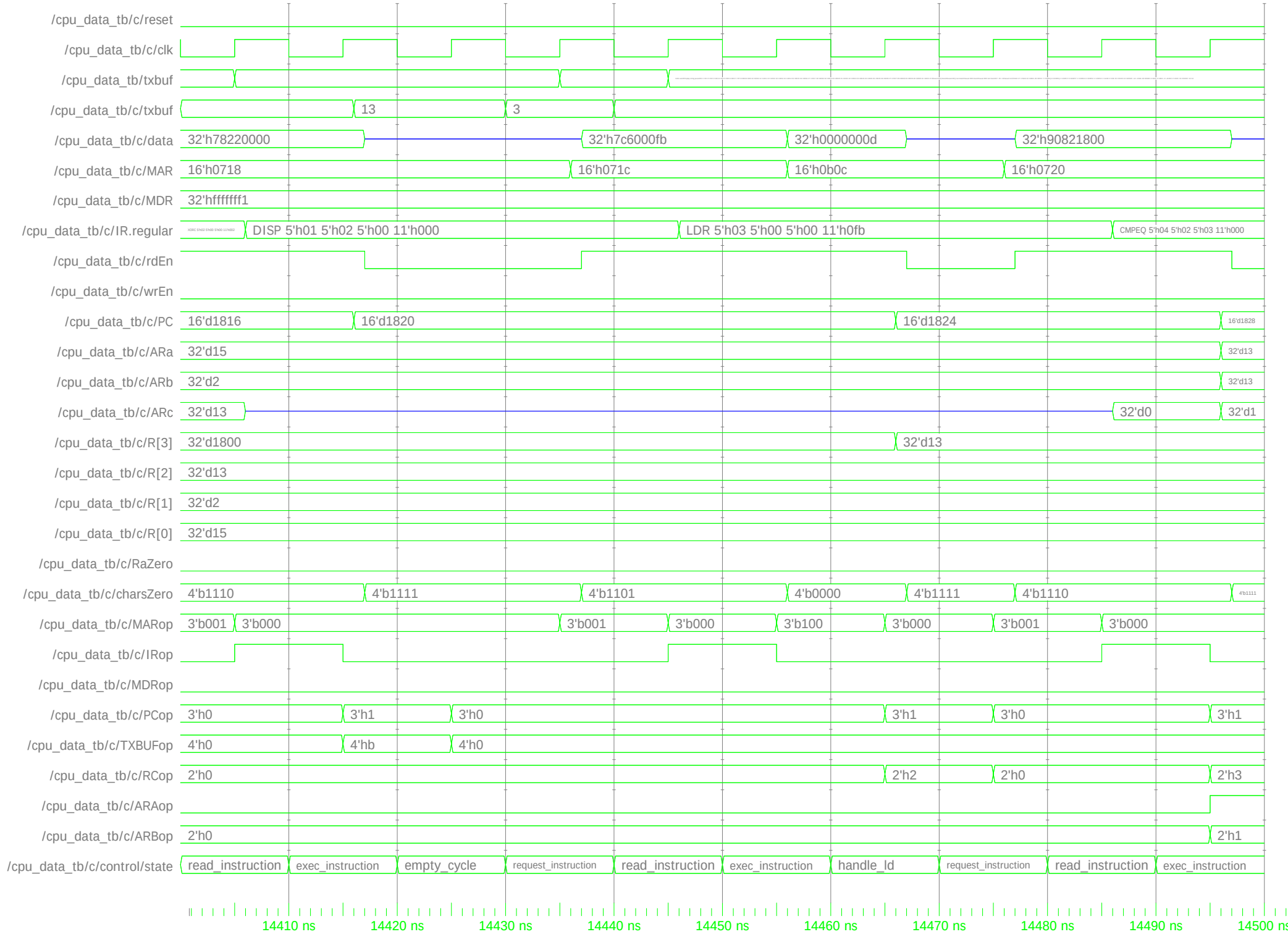

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
OR
OR
ORC 15
RC 15
C 15
C 15=
15=
15=
/cpu_data_tb/c/data
32'h6b153e90
32'h86818b50
32'h7a000000
32'he4400002
/cpu_data_tb/c/MAR
16'h06e4
16'h06e8
16'h06ec
16'h06f0
16'h06f4
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
BEQ 5'h03 5'h04 5'h00 11'h0ce
DISPC 5'h18 5'h15 5'h07 11'h690
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1764
16'd1768
16'd1780
/cpu_data_tb/c/ARa
32'd2
/cpu_data_tb/c/ARb
32'd2
/cpu_data_tb/c/ARc
32'd2
/cpu_data_tb/c/R[3]
32'd1768
/cpu_data_tb/c/R[2]
32'd2
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1000
4'b1100
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
/cpu_data_tb/c/RCop
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
handle_beq
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
14010 ns
14020 ns
14030 ns
14040 ns
14050 ns
14060 ns
14070 ns
14080 ns
14090 ns
14100 ns

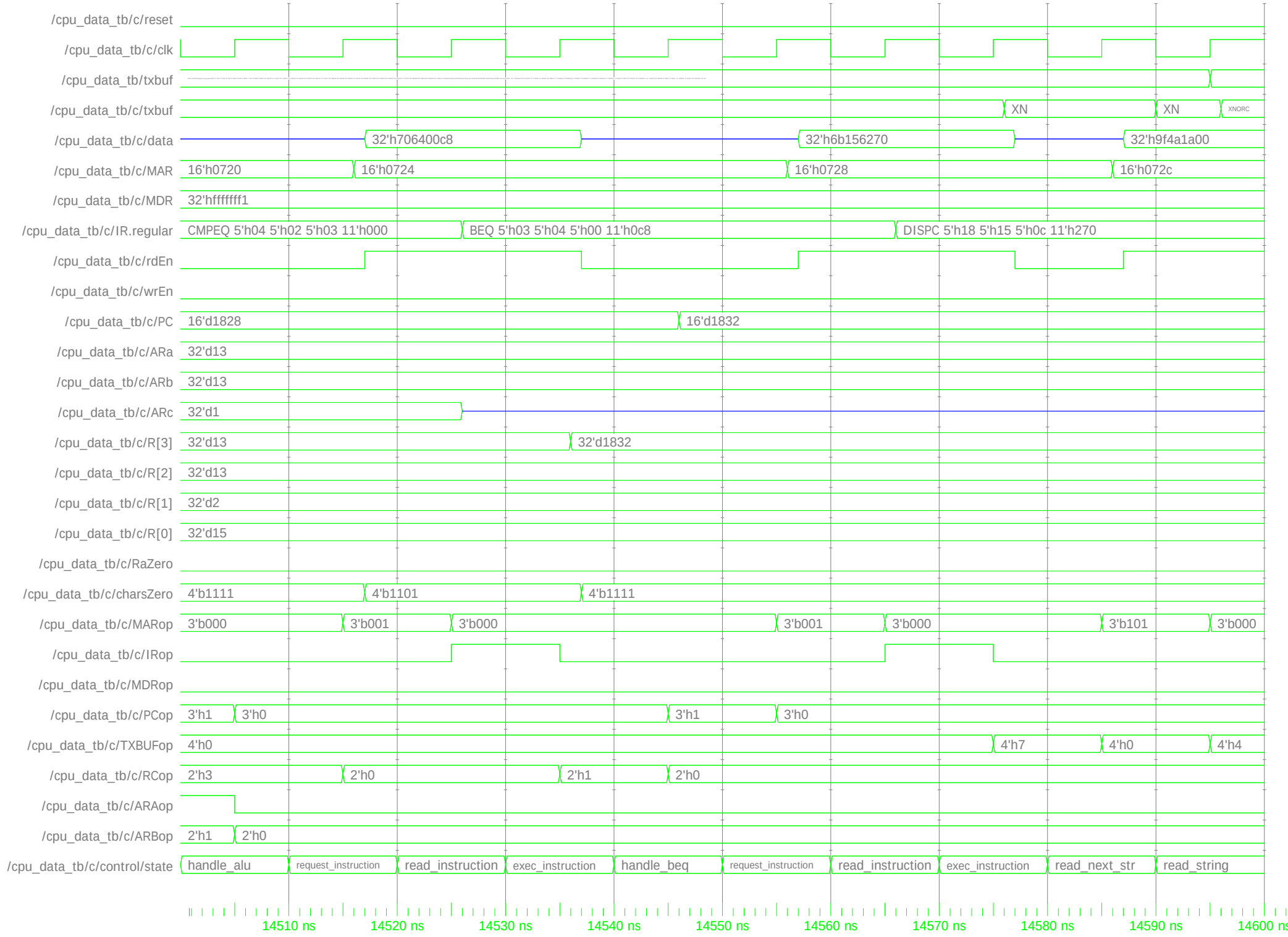


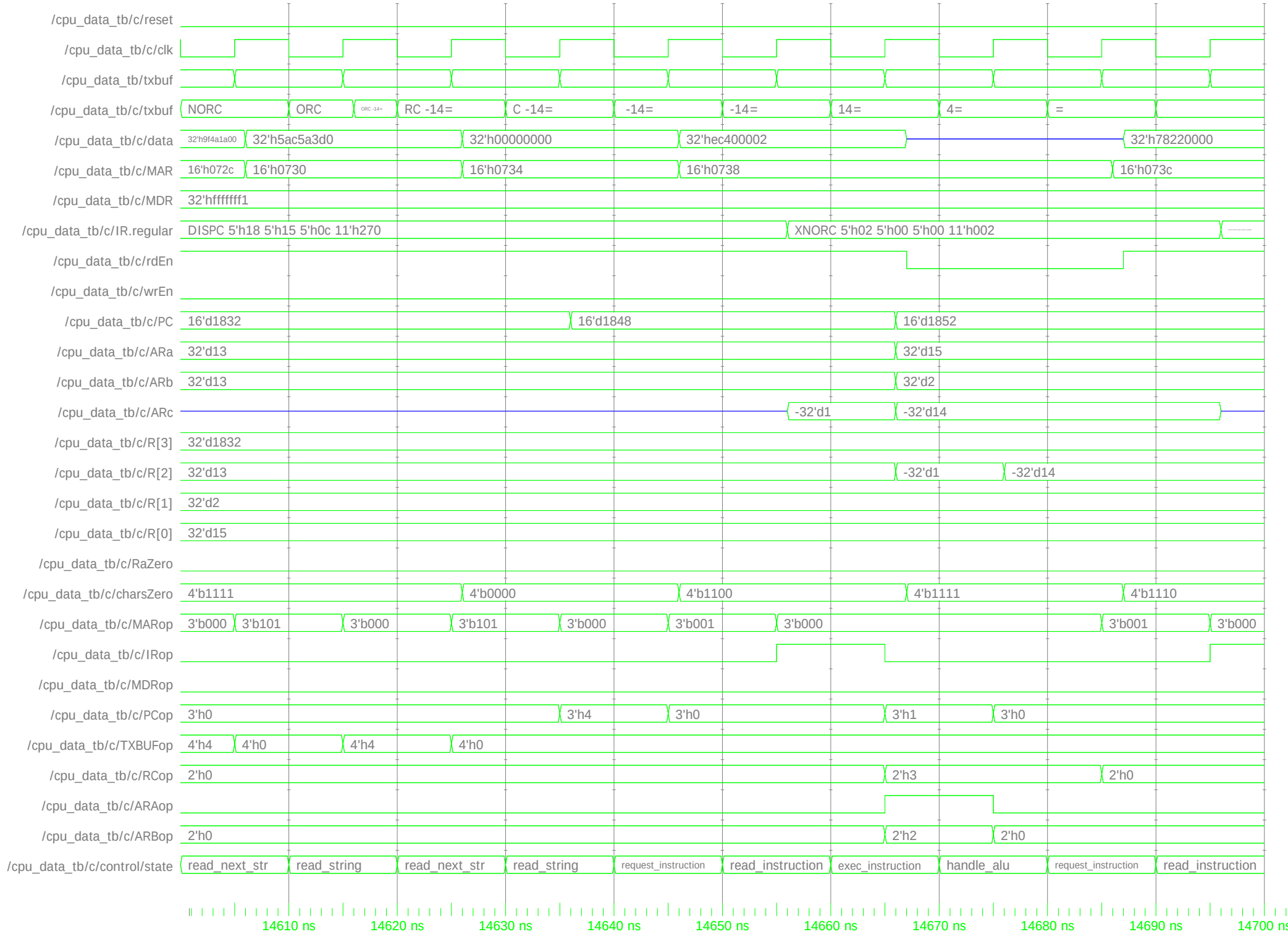
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 142 Page: 142

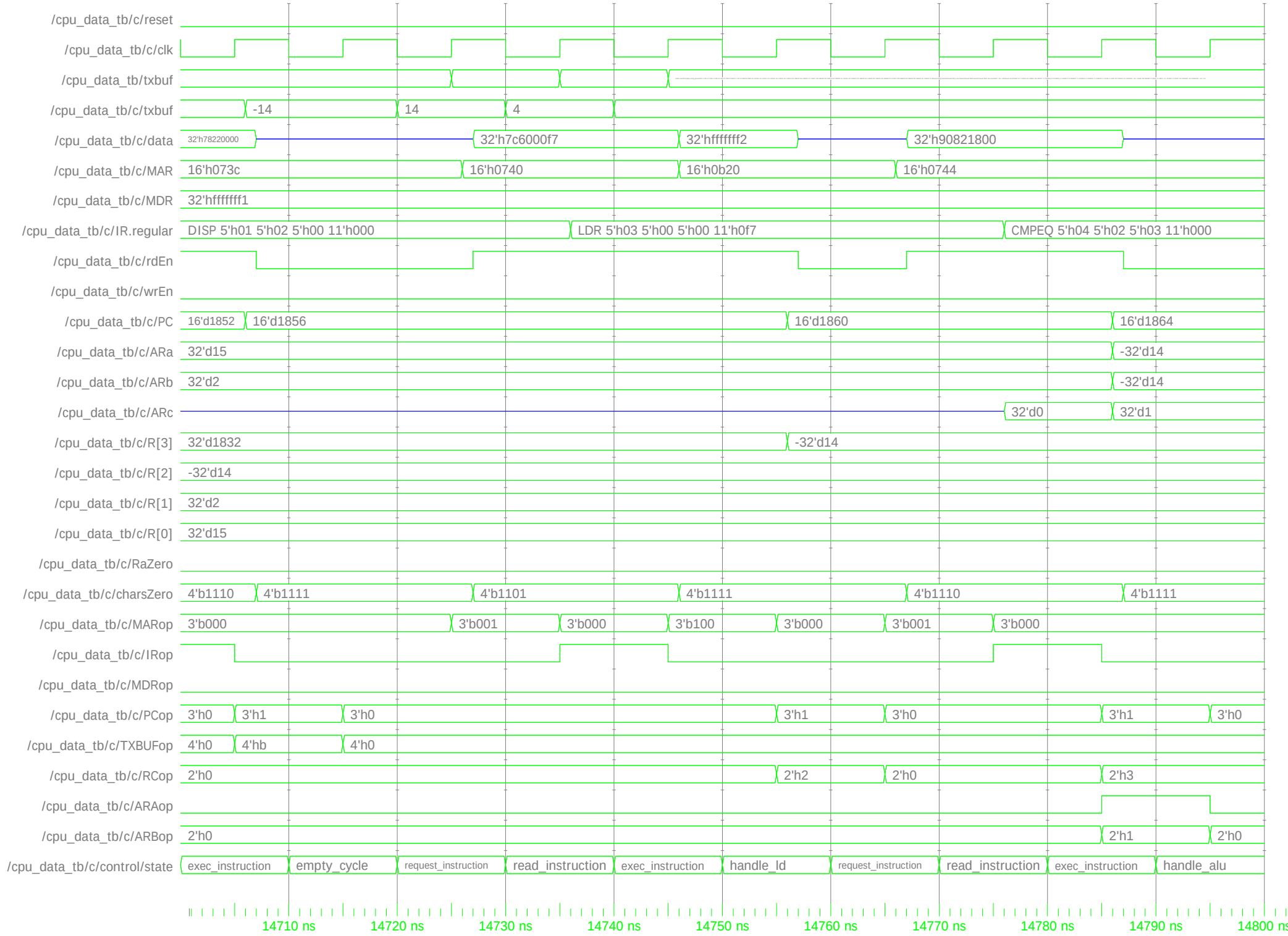

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h90821800
32'h706400cb
32'h6b156278
/cpu_data_tb/c/MAR
16'h0af4
16'h0700
16'h0704
16'h0708
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h0fd
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0cb
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1792
16'd1796
16'd1800
/cpu_data_tb/c/ARa
32'd15
/cpu_data_tb/c/ARb
32'd2
32'd15
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd15
32'd1800
/cpu_data_tb/c/R[2]
32'd15
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
14210 ns
14220 ns
14230 ns
14240 ns
14250 ns
14260 ns
14270 ns
14280 ns
14290 ns
14300 ns

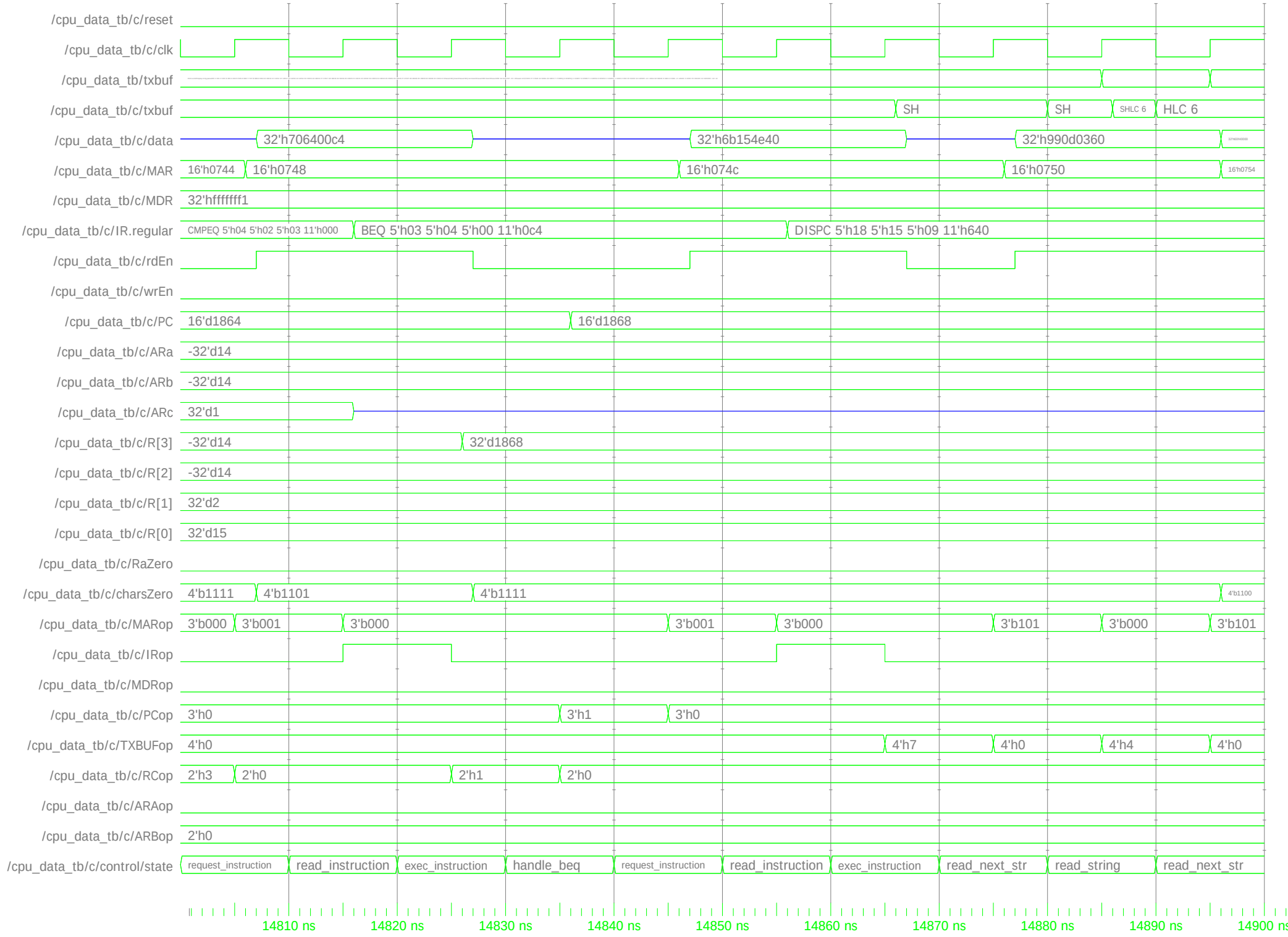

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
XO
XO
XORC 1
ORC 1
RC 1
RC 13=
C 13=
13=
13=
3=
=
/cpu_data_tb/c/data
32'h6b156278
32'ha50d0310
32'h66f40000
32'he8400002
/cpu_data_tb/c/MAR
16'h0708
16'h070c
16'h0710
16'h0714
16'h0718
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h0c 11'h278
XORC 5'h02 5'h00 5'h00 11'h002
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1800
16'd1812
16'd1816
/cpu_data_tb/c/ARa
32'd15
/cpu_data_tb/c/ARb
32'd15
32'd2
/cpu_data_tb/c/ARc
32'd0
32'd13
/cpu_data_tb/c/R[3]
32'd1800
/cpu_data_tb/c/R[2]
32'd15
32'd0
32'd13
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1100
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h2
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
14310 ns
14320 ns
14330 ns
14340 ns
14350 ns
14360 ns
14370 ns
14380 ns
14390 ns
14400 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
13
3
/cpu_data_tb/c/data
32'h78220000
32'h7c6000fb
32'h0000000d
32'h90821800
/cpu_data_tb/c/MAR
16'h0718
16'h071c
16'h0b0c
16'h0720
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h02 5'h00 11'h000
LDR 5'h03 5'h00 5'h00 11'h0fb
CMPEQ 5'h04 5'h02 5'h03 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1816
16'd1820
16'd1824
16'd1828
/cpu_data_tb/c/ARa
32'd15
32'd13
/cpu_data_tb/c/ARb
32'd2
32'd13
/cpu_data_tb/c/ARc
32'd13
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1800
32'd13
/cpu_data_tb/c/R[2]
32'd13
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1101
4'b0000
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
14410 ns
14420 ns
14430 ns
14440 ns
14450 ns
14460 ns
14470 ns
14480 ns
14490 ns
14500 ns

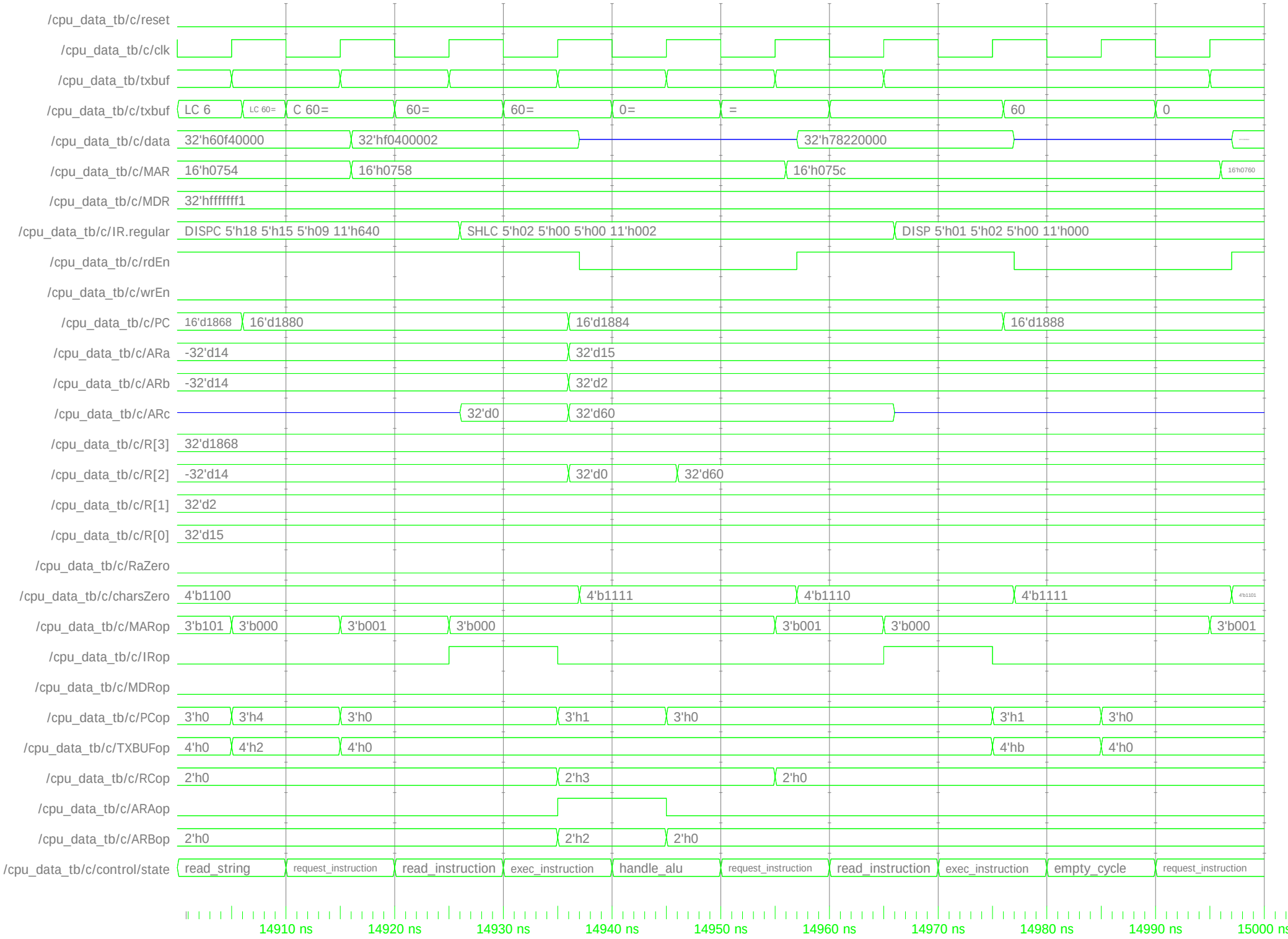

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
XN
XN
XNORC
/cpu_data_tb/c/data
32'h706400c8
32'h6b156270
32'h9f4a1a00
/cpu_data_tb/c/MAR
16'h0720
16'h0724
16'h0728
16'h072c
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0c8
DISPC 5'h18 5'h15 5'h0c 11'h270
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1828
16'd1832
/cpu_data_tb/c/ARa
32'd13
/cpu_data_tb/c/ARb
32'd13
/cpu_data_tb/c/ARc
32'd1
/cpu_data_tb/c/R[3]
32'd13
32'd1832
/cpu_data_tb/c/R[2]
32'd13
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b001
3'b000
3'b101
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
/cpu_data_tb/c/RCop
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h1
2'h0
/cpu_data_tb/c/control/state
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
14510 ns
14520 ns
14530 ns
14540 ns
14550 ns
14560 ns
14570 ns
14580 ns
14590 ns
14600 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
NORC
ORC
ORC -14=
RC -14=
C -14=
-14=
-14=
14=
4=
=
/cpu_data_tb/c/data
32'h9f4a1a00
32'h5ac5a3d0
32'h00000000
32'hec400002
32'h78220000
/cpu_data_tb/c/MAR
16'h072c
16'h0730
16'h0734
16'h0738
16'h073c
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISPC 5'h18 5'h15 5'h0c 11'h270
XNORC 5'h02 5'h00 5'h00 11'h002
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1832
16'd1848
16'd1852
/cpu_data_tb/c/ARa
32'd13
32'd15
/cpu_data_tb/c/ARb
32'd13
32'd2
/cpu_data_tb/c/ARc
-32'd1
-32'd14
/cpu_data_tb/c/R[3]
32'd1832
/cpu_data_tb/c/R[2]
32'd13
-32'd1
-32'd14
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1111
4'b0000
4'b1100
4'b1111
4'b1110
/cpu_data_tb/c/MARop
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h4
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h4
4'h0
4'h4
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h3
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h2
2'h0
/cpu_data_tb/c/control/state
read_next_str
read_string
read_next_str
read_string
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
14610 ns
14620 ns
14630 ns
14640 ns
14650 ns
14660 ns
14670 ns
14680 ns
14690 ns
14700 ns

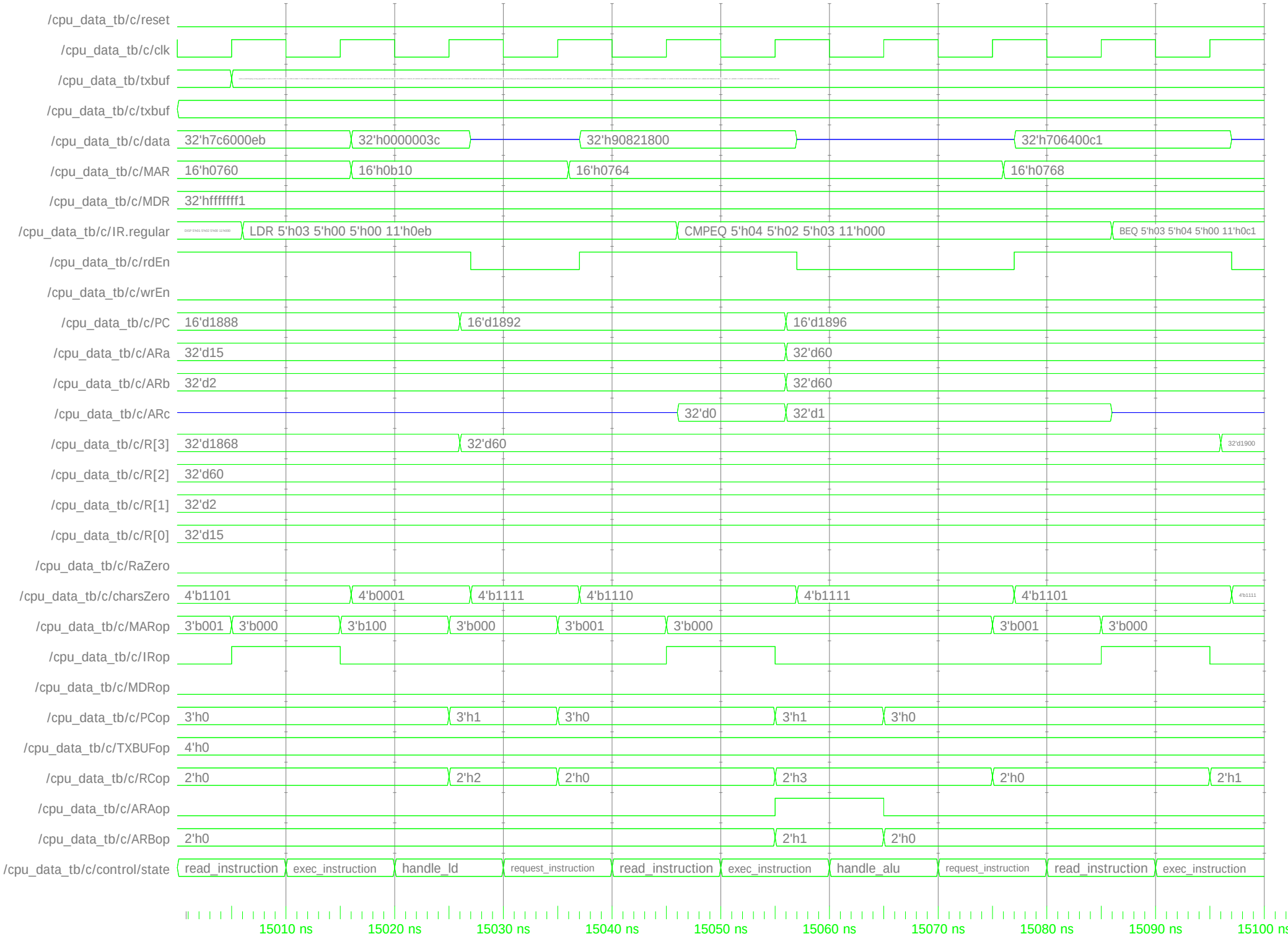

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
-14
14
4
/cpu_data_tb/c/data
32'h78220000
32'h7c6000f7
32'hffffffff2
32'h90821800
/cpu_data_tb/c/MAR
16'h073c
16'h0740
16'h0b20
16'h0744
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
DISP 5'h01 5'h02 5'h00 11'h000
LDR 5'h03 5'h00 5'h00 11'h0f7
CMPEQ 5'h04 5'h02 5'h03 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1852
16'd1856
16'd1860
16'd1864
/cpu_data_tb/c/ARa
32'd15
-32'd14
/cpu_data_tb/c/ARb
32'd2
-32'd14
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1832
-32'd14
/cpu_data_tb/c/R[2]
-32'd14
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1110
4'b1111
4'b1101
4'b1111
4'b1110
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'hb
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
exec_instruction
empty_cycle
request_instruction
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
14710 ns
14720 ns
14730 ns
14740 ns
14750 ns
14760 ns
14770 ns
14780 ns
14790 ns
14800 ns



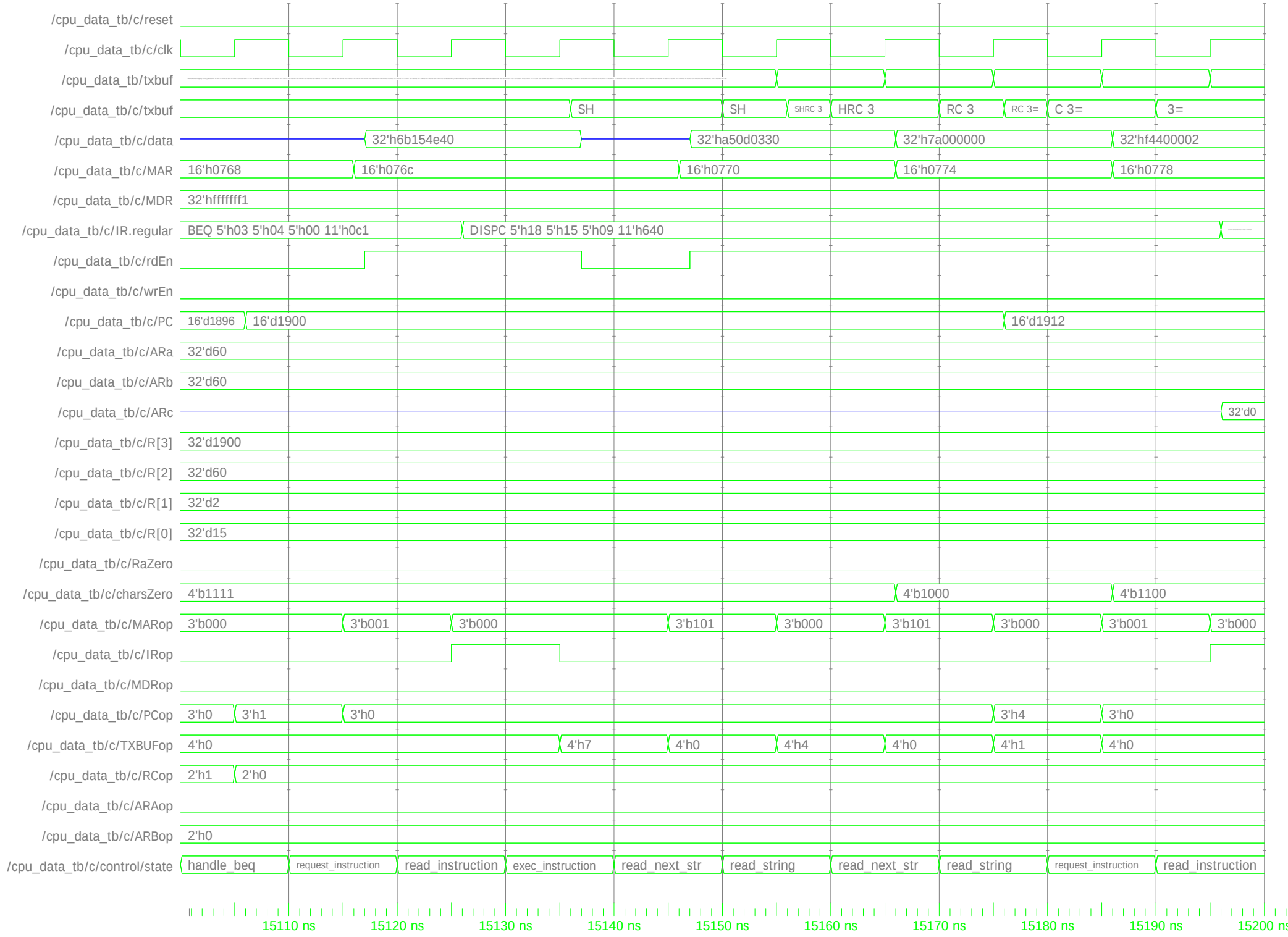
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 149 Page: 149



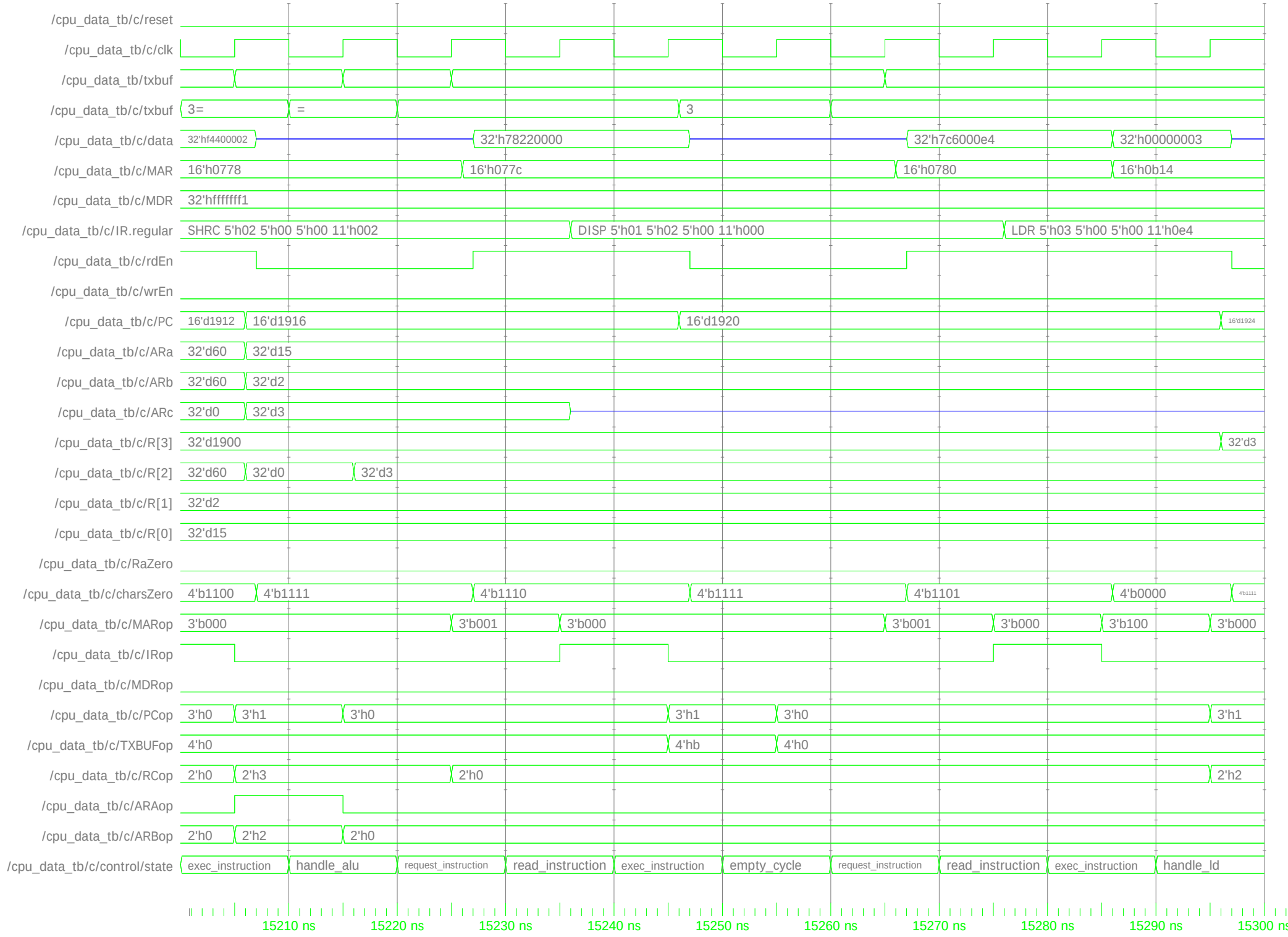
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 150 Page: 150

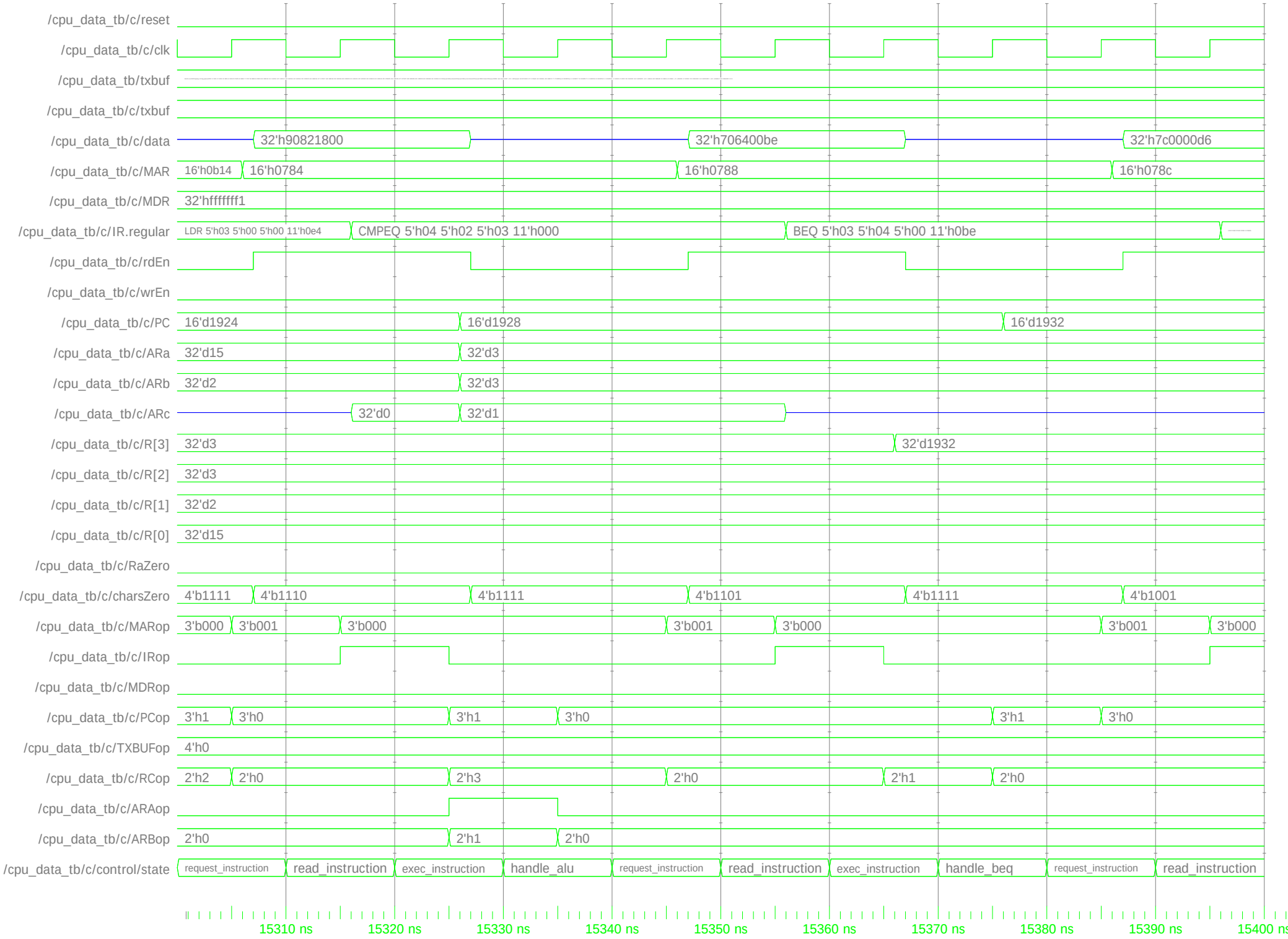


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 151 Page: 151

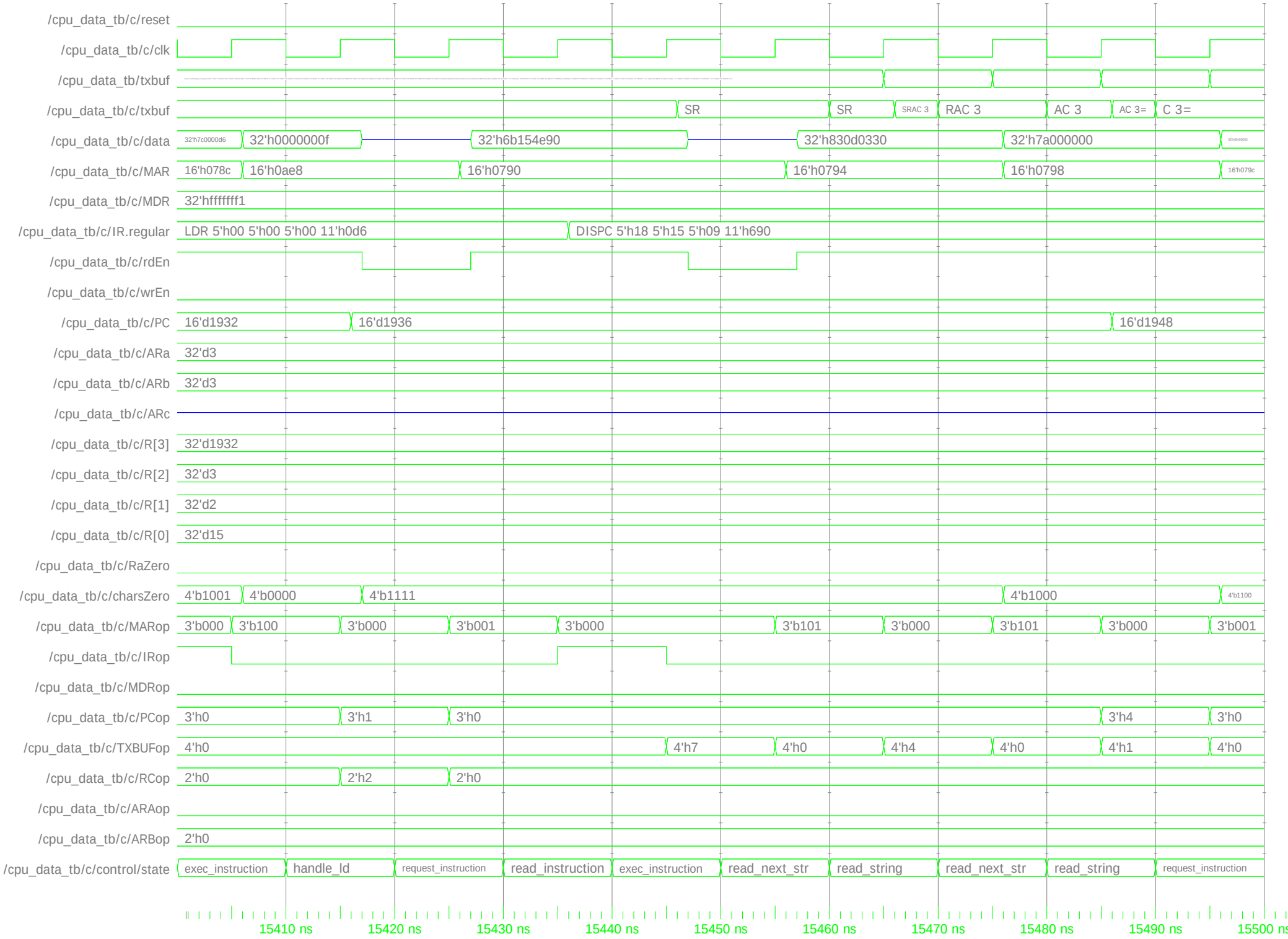


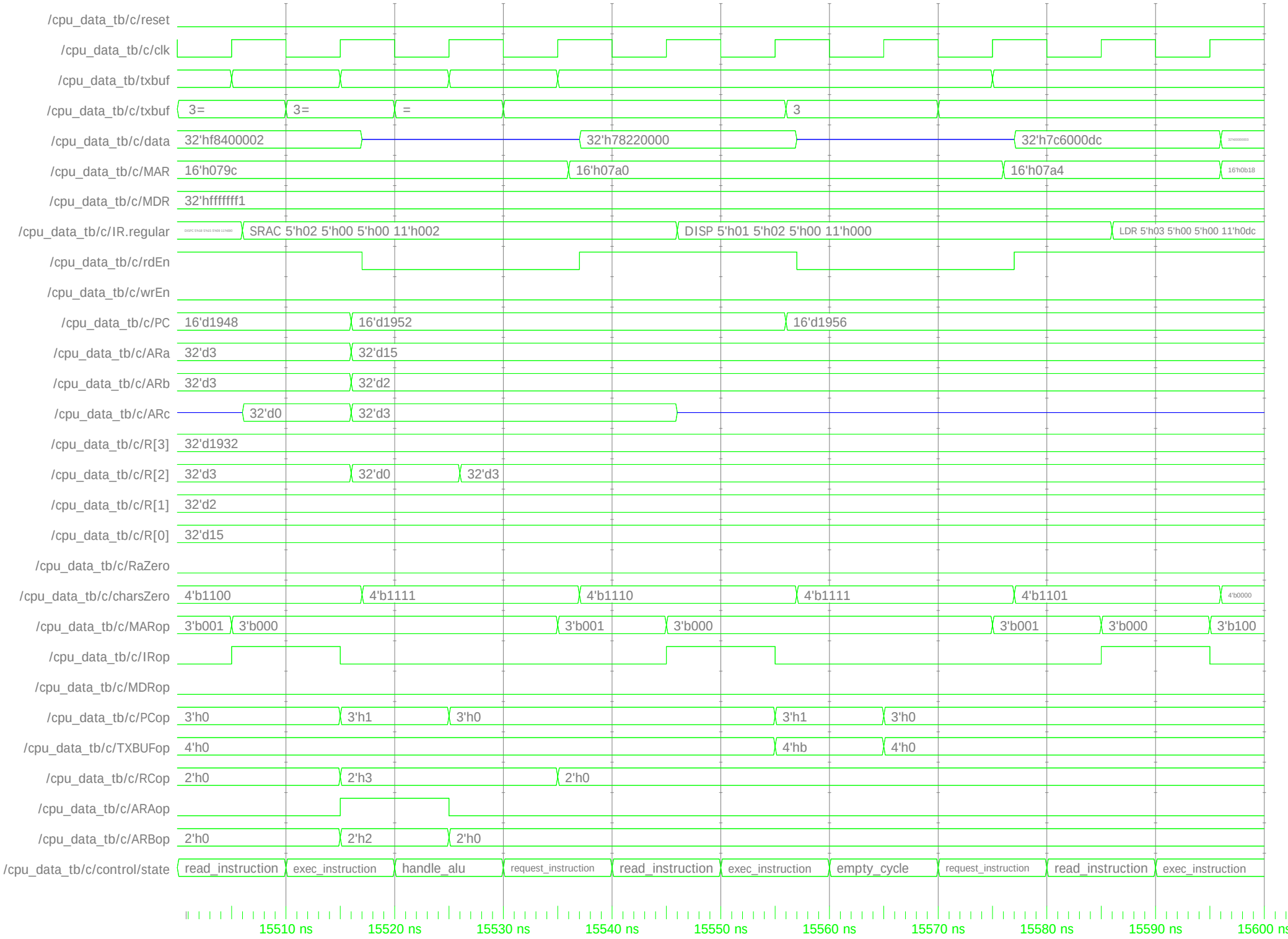
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 152 Page: 152


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/txbuf 3= = 3
/cpu_data_tb/c/data 32'hf4400002 32'h78220000 32'h7c6000e4 32'h00000003
/cpu_data_tb/c/MAR 16'h0778 16'h077c 16'h0780 16'h0b14
/cpu_data_tb/c/MDR 32'hffffffff1
/cpu_data_tb/c/IR.regular SHRC 5'h02 5'h00 5'h00 11'h002 DISP 5'h01 5'h02 5'h00 11'h000 LDR 5'h03 5'h00 5'h00 11'h0e4
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC 16'd1912 16'd1916 16'd1920 16'd1924
/cpu_data_tb/c/ARa 32'd60 32'd15
/cpu_data_tb/c/ARb 32'd60 32'd2
/cpu_data_tb/c/ARc 32'd0 32'd3
/cpu_data_tb/c/R[3] 32'd1900 32'd3
/cpu_data_tb/c/R[2] 32'd60 32'd0 32'd3
/cpu_data_tb/c/R[1] 32'd2
/cpu_data_tb/c/R[0] 32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero 4'b1100 4'b1111 4'b1110 4'b1111 4'b1101 4'b0000 4'b1111
/cpu_data_tb/c/MARop 3'b000 3'b001 3'b000 3'b001 3'b000 3'b100 3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop 3'h0 3'h1 3'h0 3'h1 3'h0 3'h1
/cpu_data_tb/c/TXBUFop 4'h0 4'hb 4'h0
/cpu_data_tb/c/RCop 2'h0 2'h3 2'h0 2'h2
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop 2'h0 2'h2 2'h0
/cpu_data_tb/c/control/state exec_instruction handle_alu request_instruction read_instruction exec_instruction empty_cycle request_instruction read_instruction exec_instruction handle_ld
15210 ns
15220 ns
15230 ns
15240 ns
15250 ns
15260 ns
15270 ns
15280 ns
15290 ns
15300 ns

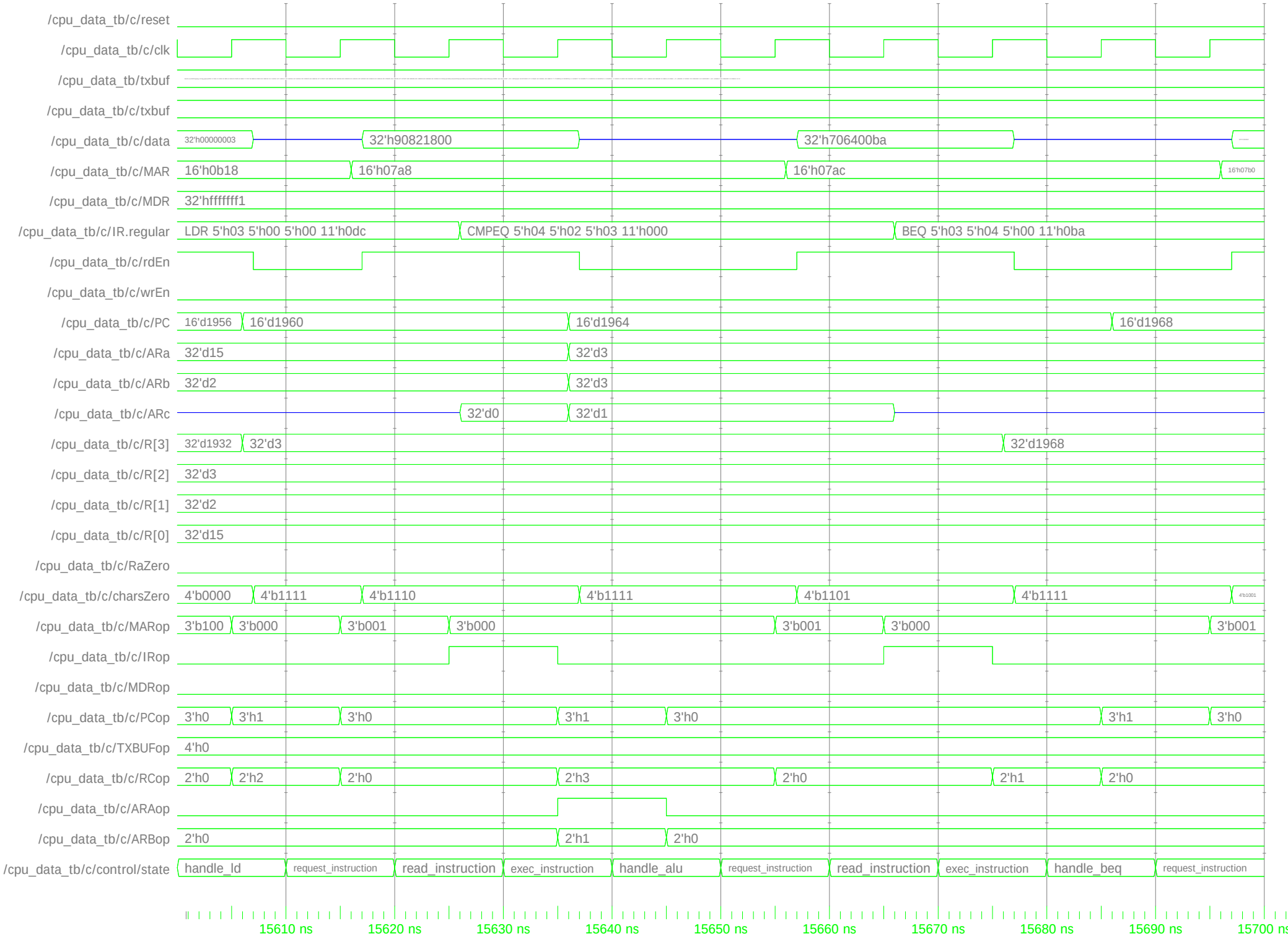


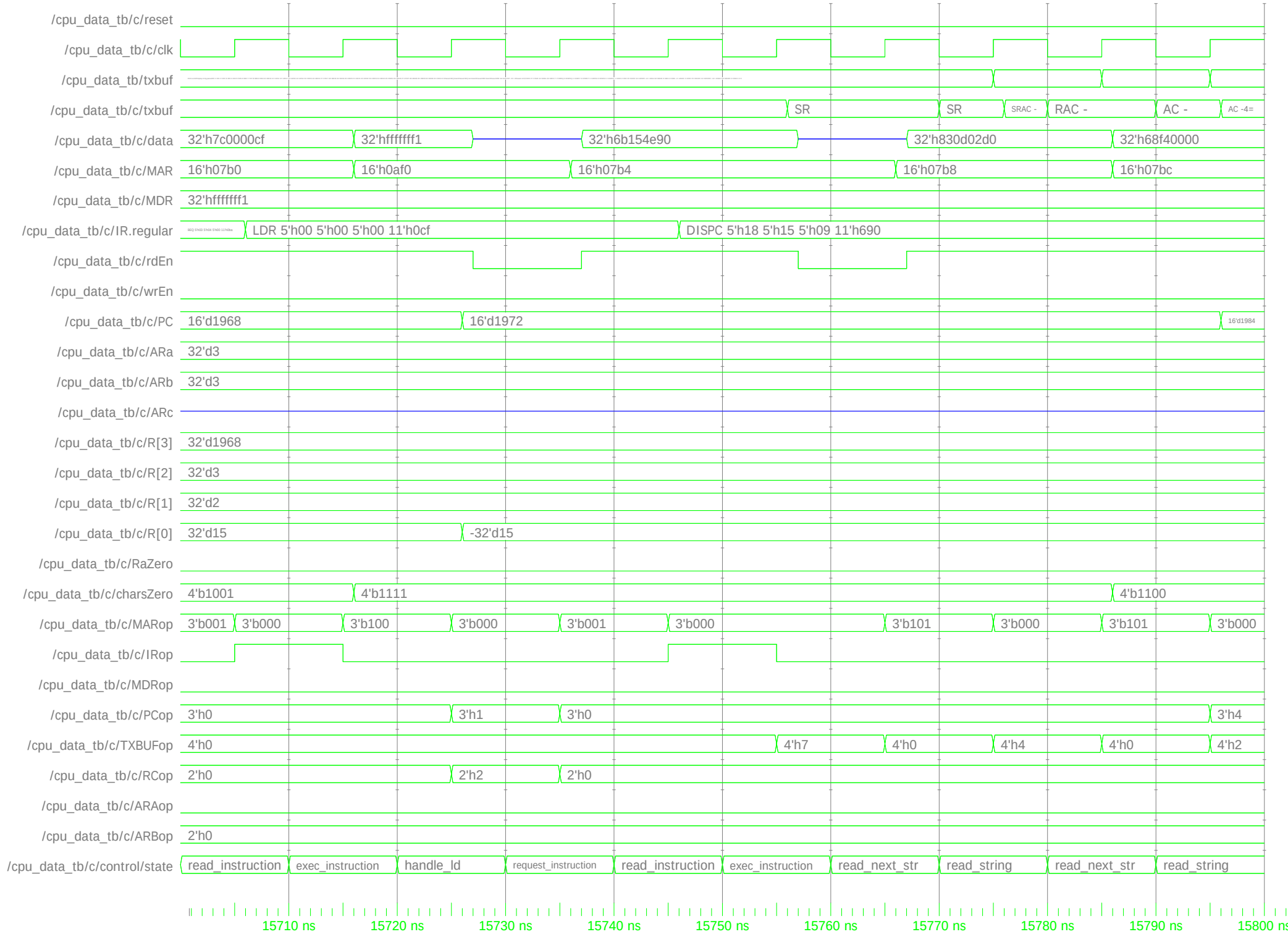
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 154 Page: 154

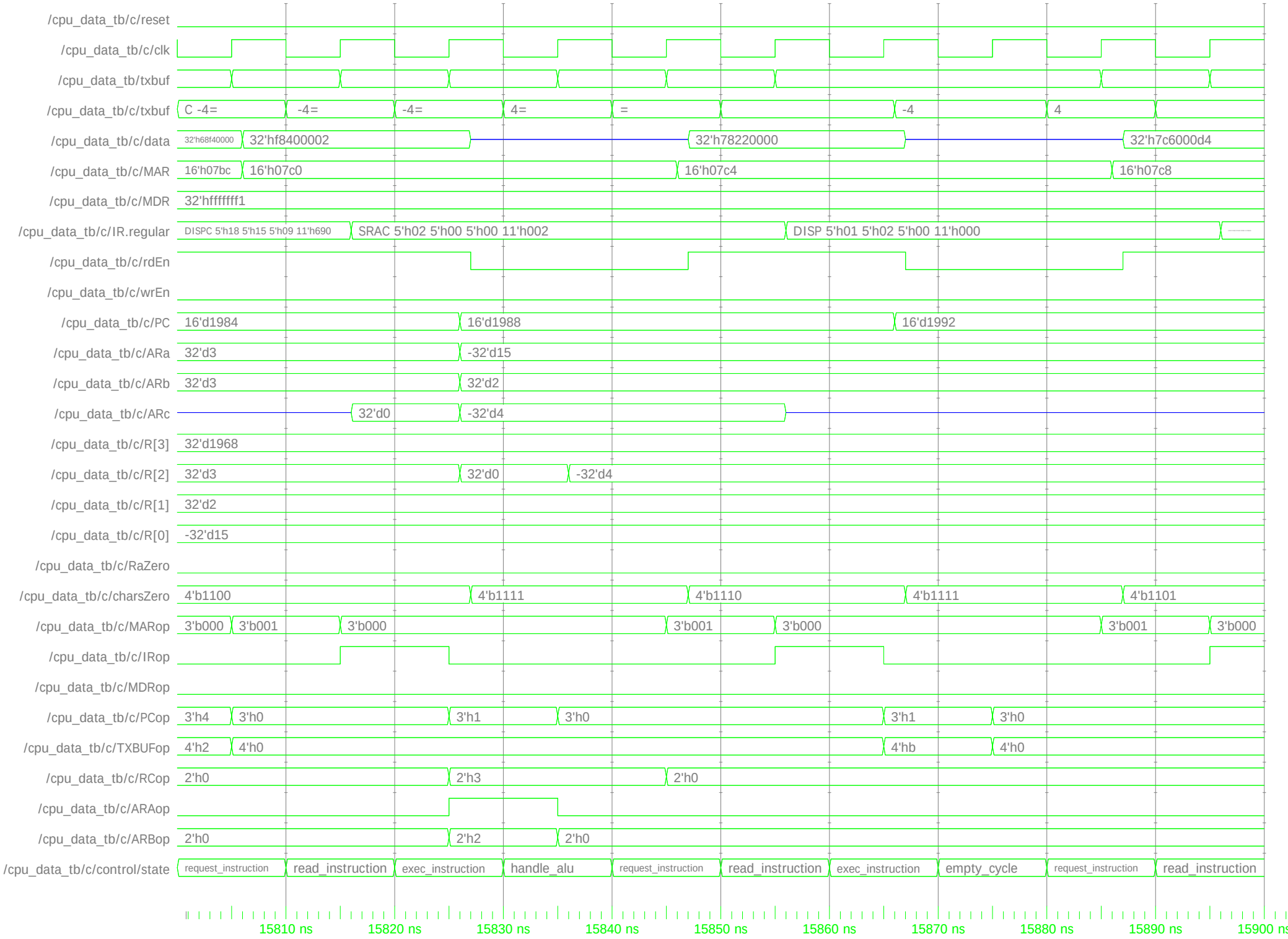

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
SR
SR
SRAC 3
RAC 3
AC 3
AC 3=
C 3=
/cpu_data_tb/c/data
32'h7c0000d6
32'h0000000f
32'h6b154e90
32'h830d0330
32'h7a000000
/cpu_data_tb/c/MAR
16'h078c
16'h0ae8
16'h0790
16'h0794
16'h0798
16'h079c
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h00 5'h00 5'h00 11'h0d6
DISPC 5'h18 5'h15 5'h09 11'h690
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1932
16'd1936
16'd1948
/cpu_data_tb/c/ARa
32'd3
/cpu_data_tb/c/ARb
32'd3
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd1932
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1001
4'b0000
4'b1111
4'b1000
4'b1100
/cpu_data_tb/c/MARop
3'b000
3'b100
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h1
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
request_instruction
15410 ns
15420 ns
15430 ns
15440 ns
15450 ns
15460 ns
15470 ns
15480 ns
15490 ns
15500 ns



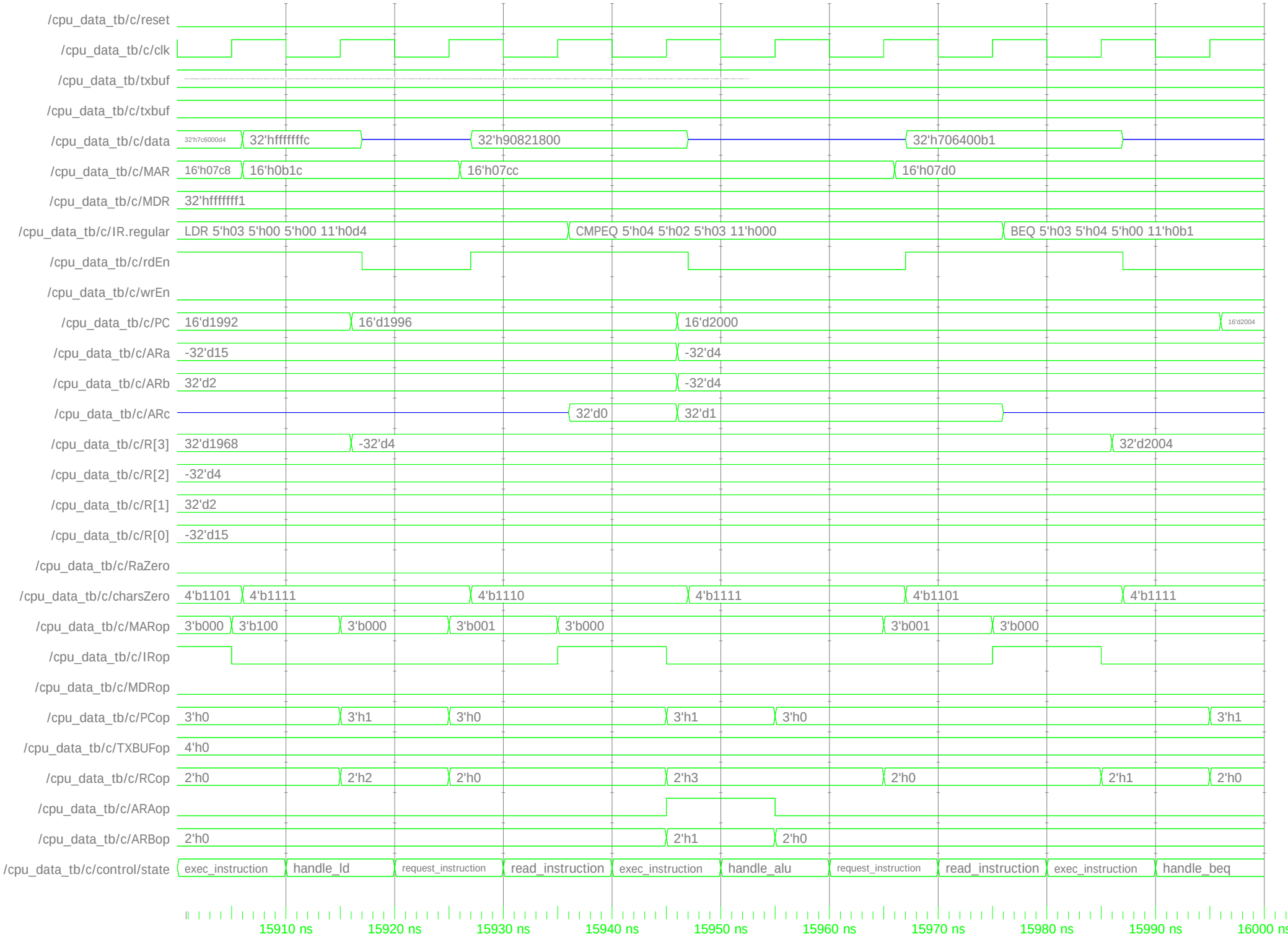
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 156 Page: 156

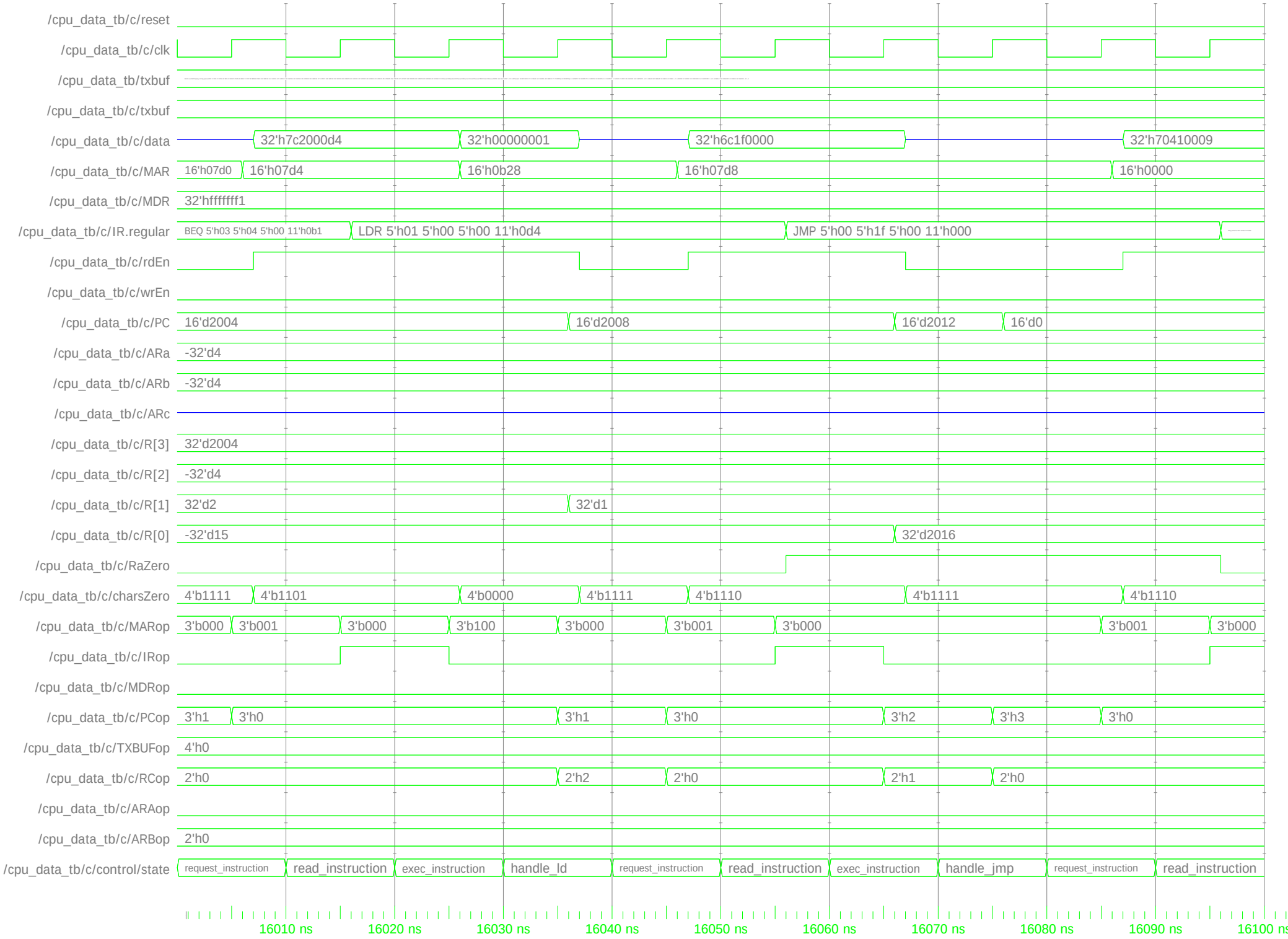

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h00000003
32'h90821800
32'h706400ba
/cpu_data_tb/c/MAR
16'h0b18
16'h07a8
16'h07ac
16'h07b0
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h0dc
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0ba
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1956
16'd1960
16'd1964
16'd1968
/cpu_data_tb/c/ARa
32'd15
32'd3
/cpu_data_tb/c/ARb
32'd2
32'd3
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1932
32'd3
32'd1968
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b0000
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
4'b1001
/cpu_data_tb/c/MARop
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
3'b001
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
request_instruction
15610 ns
15620 ns
15630 ns
15640 ns
15650 ns
15660 ns
15670 ns
15680 ns
15690 ns
15700 ns


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
SR
SR
SRAC -
RAC -
AC -
AC -4=
/cpu_data_tb/c/data
32'h7c0000cf
32'hffffffff
32'h6b154e90
32'h830d02d0
32'h68f40000
/cpu_data_tb/c/MAR
16'h07b0
16'h0af0
16'h07b4
16'h07b8
16'h07bc
/cpu_data_tb/c/MDR
32'hffffffff
/cpu_data_tb/c/IR.regular
LDR 5'h00 5'h00 5'h00 11'h0cf
DISPC 5'h18 5'h15 5'h09 11'h690
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1968
16'd1972
16'd1984
/cpu_data_tb/c/ARa
32'd3
/cpu_data_tb/c/ARb
32'd3
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd1968
/cpu_data_tb/c/R[2]
32'd3
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
32'd15
-32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1001
4'b1111
4'b1100
/cpu_data_tb/c/MARop
3'b001
3'b000
3'b100
3'b000
3'b001
3'b000
3'b101
3'b000
3'b101
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h4
/cpu_data_tb/c/TXBUFop
4'h0
4'h7
4'h0
4'h4
4'h0
4'h2
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
read_next_str
read_string
read_next_str
read_string
15710 ns
15720 ns
15730 ns
15740 ns
15750 ns
15760 ns
15770 ns
15780 ns
15790 ns
15800 ns

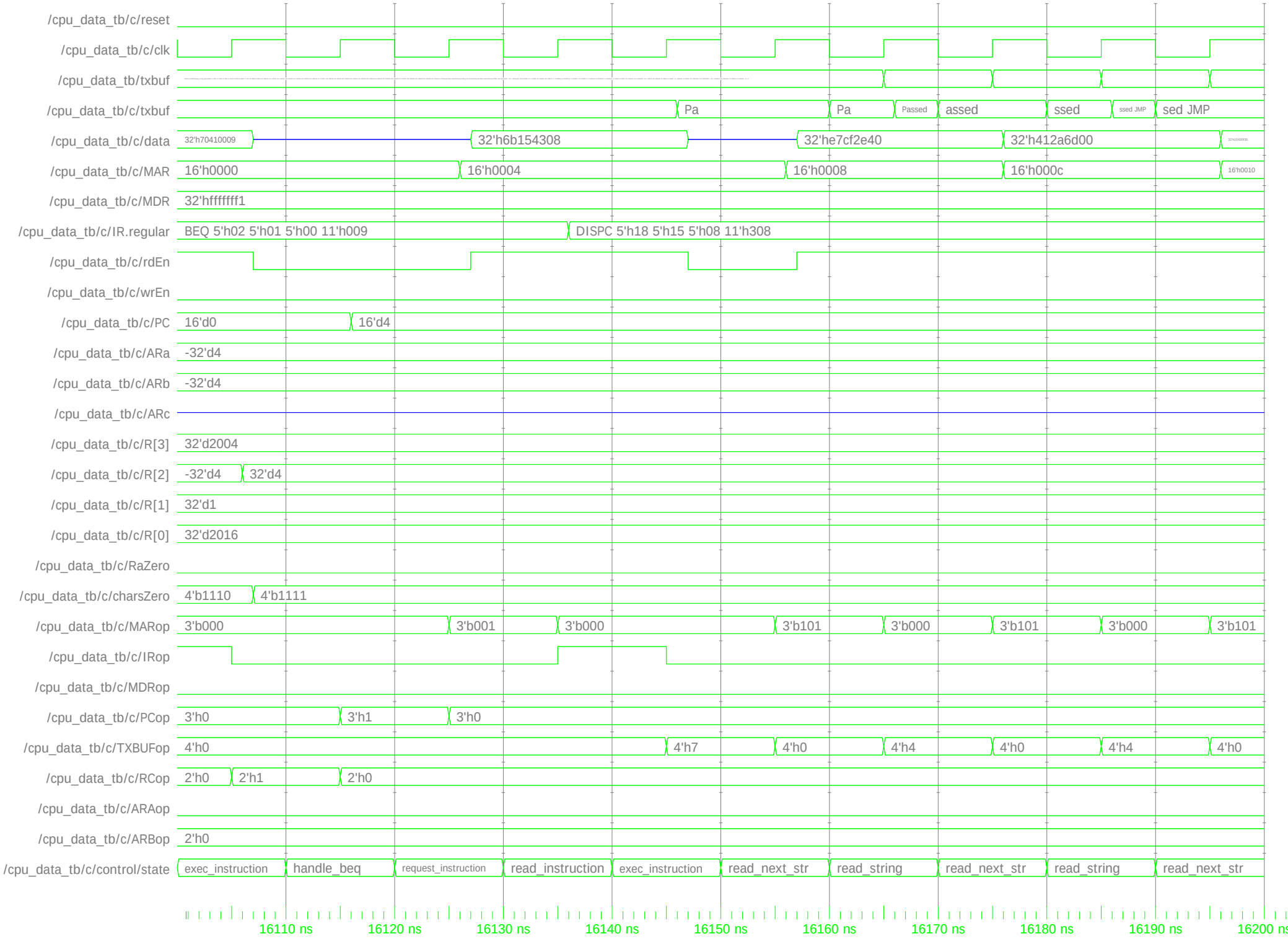


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 159 Page: 159

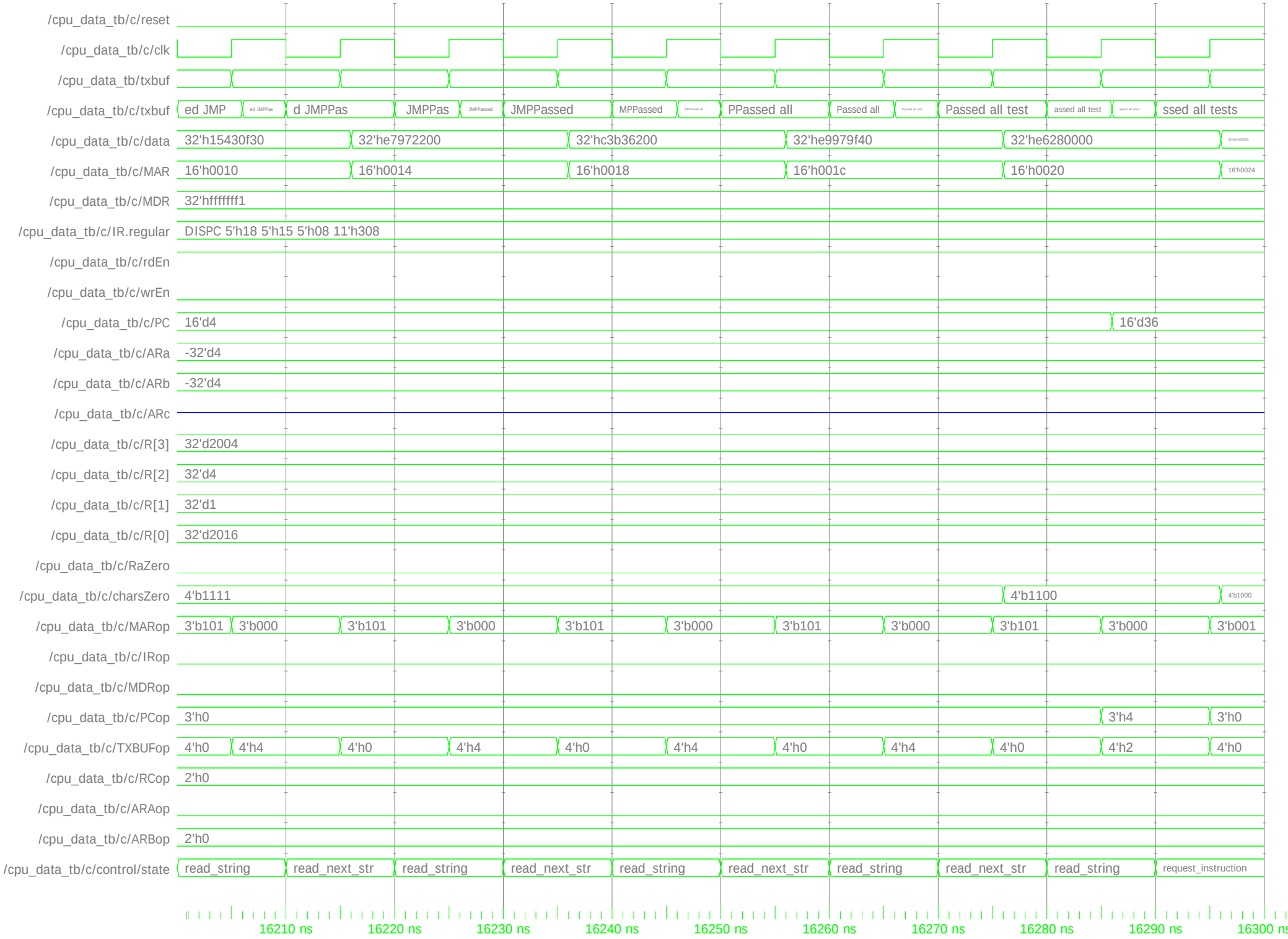

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
32'h7c6000d4
32'hfffffffc
32'h90821800
32'h706400b1
/cpu_data_tb/c/MAR
16'h07c8
16'h0b1c
16'h07cc
16'h07d0
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
LDR 5'h03 5'h00 5'h00 11'h0d4
CMPEQ 5'h04 5'h02 5'h03 11'h000
BEQ 5'h03 5'h04 5'h00 11'h0b1
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd1992
16'd1996
16'd2000
16'd2004
/cpu_data_tb/c/ARa
-32'd15
-32'd4
/cpu_data_tb/c/ARb
32'd2
-32'd4
/cpu_data_tb/c/ARc
32'd0
32'd1
/cpu_data_tb/c/R[3]
32'd1968
-32'd4
32'd2004
/cpu_data_tb/c/R[2]
-32'd4
/cpu_data_tb/c/R[1]
32'd2
/cpu_data_tb/c/R[0]
-32'd15
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1101
4'b1111
4'b1110
4'b1111
4'b1101
4'b1111
/cpu_data_tb/c/MARop
3'b000
3'b100
3'b000
3'b001
3'b000
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
3'h1
3'h0
3'h1
3'h0
3'h1
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
2'h2
2'h0
2'h3
2'h0
2'h1
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
2'h1
2'h0
/cpu_data_tb/c/control/state
exec_instruction
handle_ld
request_instruction
read_instruction
exec_instruction
handle_alu
request_instruction
read_instruction
exec_instruction
handle_beq
15910 ns
15920 ns
15930 ns
15940 ns
15950 ns
15960 ns
15970 ns
15980 ns
15990 ns
16000 ns



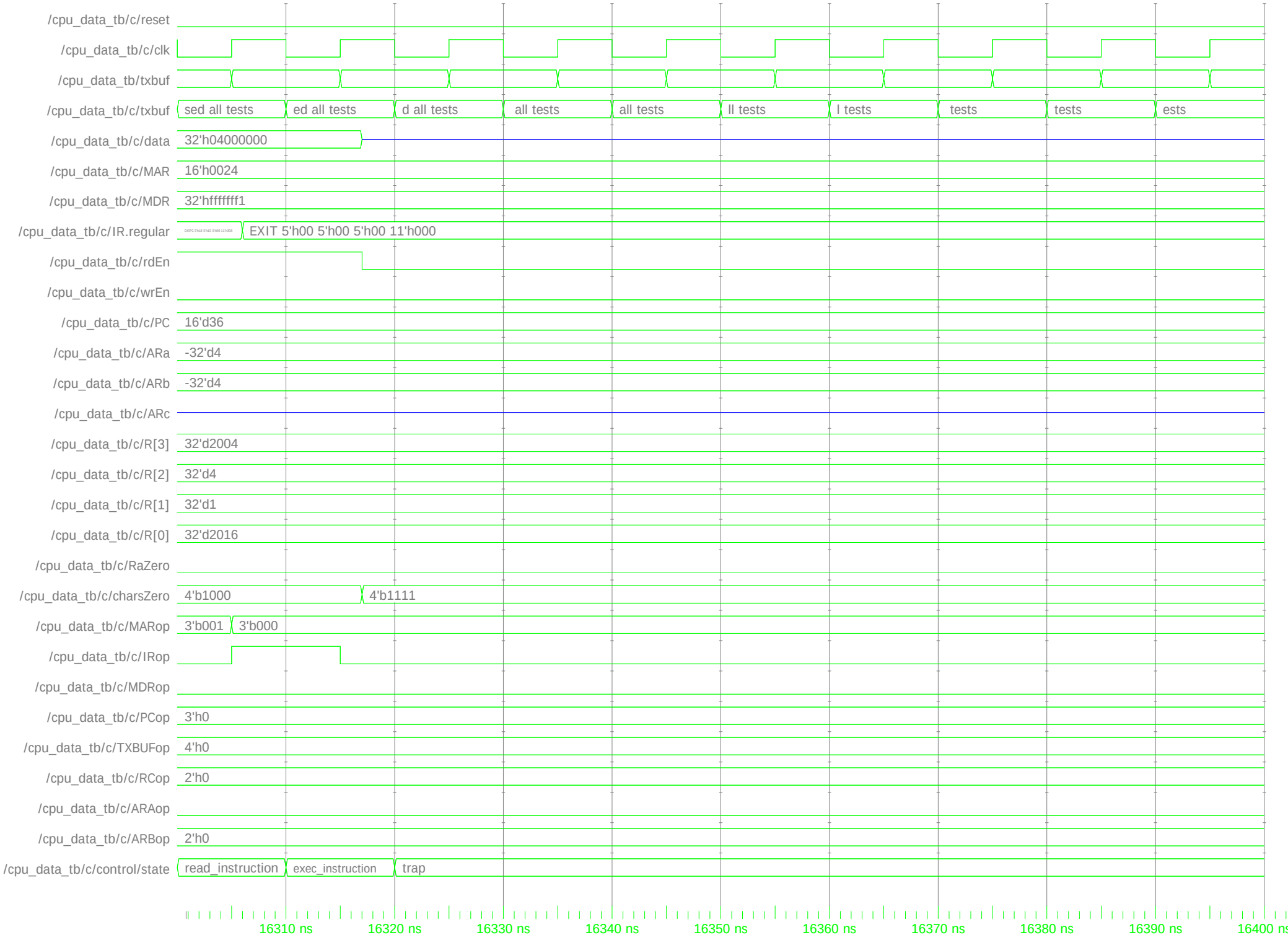
Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 161 Page: 161

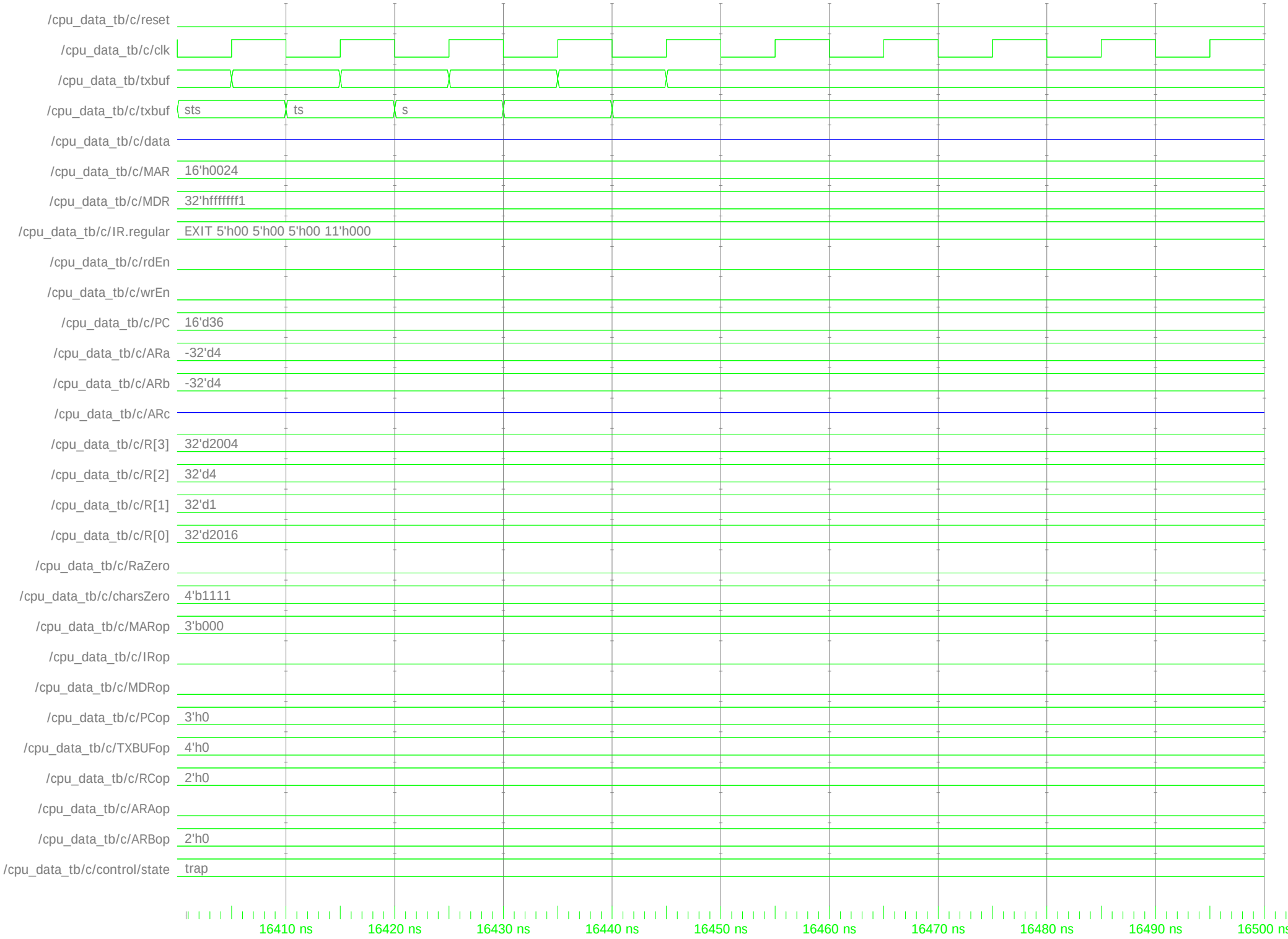


Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 162 Page: 162



Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 163 Page: 163


/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
sed all tests
ed all tests
d all tests
all tests
all tests
ll tests
l tests
tests
tests
ests
/cpu_data_tb/c/data
32'h04000000
/cpu_data_tb/c/MAR
16'h0024
/cpu_data_tb/c/MDR
32'hffffffff1
/cpu_data_tb/c/IR.regular
EXIT 5'h00 5'h00 5'h00 11'h000
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
16'd36
/cpu_data_tb/c/ARa
-32'd4
/cpu_data_tb/c/ARb
-32'd4
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
32'd2004
/cpu_data_tb/c/R[2]
32'd4
/cpu_data_tb/c/R[1]
32'd1
/cpu_data_tb/c/R[0]
32'd2016
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
4'b1000
4'b1111
/cpu_data_tb/c/MARop
3'b001
3'b000
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
3'h0
/cpu_data_tb/c/TXBUFop
4'h0
/cpu_data_tb/c/RCop
2'h0
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
2'h0
/cpu_data_tb/c/control/state
read_instruction
exec_instruction
trap
16310 ns
16320 ns
16330 ns
16340 ns
16350 ns
16360 ns
16370 ns
16380 ns
16390 ns
16400 ns



Entity:cpu_data_tb Architecture: Date: Wed May 02 13:03:20 PDT 2018 Row: 165 Page: 165

/cpu_data_tb/c/reset
/cpu_data_tb/c/clk
/cpu_data_tb/txbuf
/cpu_data_tb/c/txbuf
/cpu_data_tb/c/data
/cpu_data_tb/c/MAR
/cpu_data_tb/c/MDR
/cpu_data_tb/c/IR.regular
/cpu_data_tb/c/rdEn
/cpu_data_tb/c/wrEn
/cpu_data_tb/c/PC
/cpu_data_tb/c/ARa
/cpu_data_tb/c/ARb
/cpu_data_tb/c/ARc
/cpu_data_tb/c/R[3]
/cpu_data_tb/c/R[2]
/cpu_data_tb/c/R[1]
/cpu_data_tb/c/R[0]
/cpu_data_tb/c/RaZero
/cpu_data_tb/c/charsZero
/cpu_data_tb/c/MARop
/cpu_data_tb/c/IRop
/cpu_data_tb/c/MDRop
/cpu_data_tb/c/PCop
/cpu_data_tb/c/TXBUFop
/cpu_data_tb/c/RCop
/cpu_data_tb/c/ARAop
/cpu_data_tb/c/ARBop
/cpu_data_tb/c/control/state
16510 ns
16520 ns
16530 ns
16540 ns
16550 ns
16560 ns
16570 ns
16580 ns
16590 ns
16600 ns