This document will give a quick overview of the UART module and signals for users.

Note: The name *_byte_* is a bit of a misnomer. The default is 8 bits of data which is a byte, but the data size is configurable so it can be more or less than 8 bits. The name may be updated in the future, but at this point I am most likely going to leave it.

Parameters:

The UART top module is parameterizable for the following options:

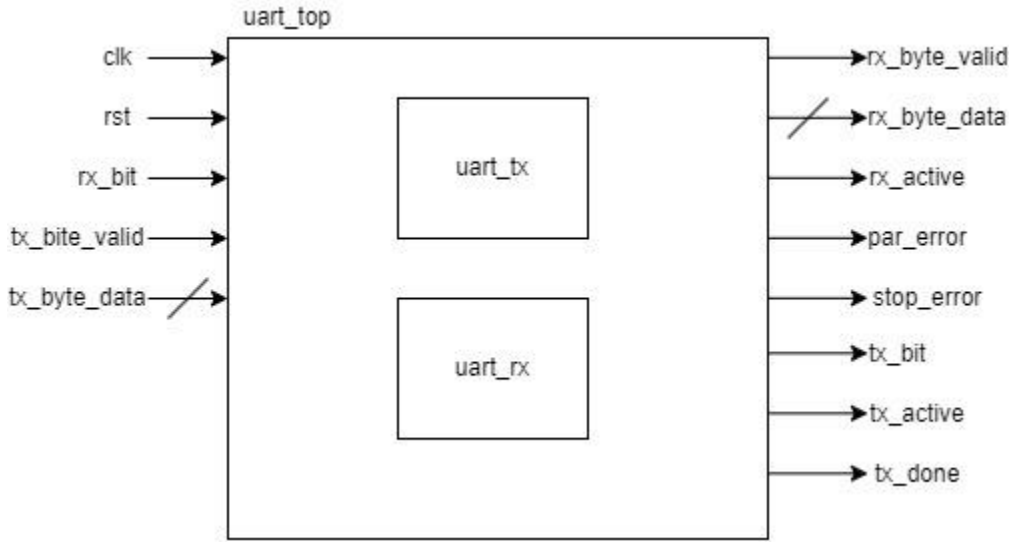
- **CLK_PER_BIT**: This lets you set the desired baud rate based on your clock. The equation to find out what the parameter should be is (clock rate Hz) / (desired baud rate). For the example that I have in my project, the parameter is (100 MHz clk) / (115200 baud) = 868.

- **PACK_SIZE**: This lets you choose the desired amount of data bits in each UART packet. For this project, 8 bits was chosen.

- **PARITY_EN**: This is a 1 bit on or off parameter. If the value is 1, then the parity bit is enabled. If the value is 0, then the parity bit is disabled.

- **EVEN_PAR**: This is a 1 bit on or off parameter. If the value is 1, then the module will use even parity. If the value is 0, then the module will use odd parity. If PARITY_EN is 0, then this parameter doesn't matter because parity will be disabled.

Top Level Diagram:



Signal Descriptions

Singal Name	**I/O**	**Size**	**Description**
rx_bit	I	1 bit	Main rx receiver for UART data
rx_byte_valid	O	1 bit	Goes high for one cycle after stop bit has been received
rx_byte_data	O	PACK_SIZE bits	Data received on the rx transmission assembled into an array of data
rx_active	O	1 bit	Goes high once start bit is received and remains high until packet is received or there has been an error
par_error	O	1 bit	Goes high for one cycle after stop bit is received to show that there was a parity error in packet
stop_error	O	1 bit	Goes high for one cycle after stop bit should have been received if there is an error on the stop bit
tx_byte_valid	I	1 bit	Bit sent to the module to show that the data in tx_byte_data is ready to be sent. If tx_active is high then the module will not accept a new packet.

tx_byte_data	I	PACK_SIZE bits	Data to be transmitted out of that module via UART protocol
tx_bit	O	1 bit	Main tx sender for UART data
tx_active	O	1 bit	Goes high once a packet has started sending. Will go low once stop bit has sent
tx_done	O	1 bit	Goes high for one cycle after packet has been sent. Offset from tx_active going low by one cycle