Note: The simulations run here are all using Modelsim and Windows. Feel free to use other simulators and operating systems, but they will not be covered in this guide.

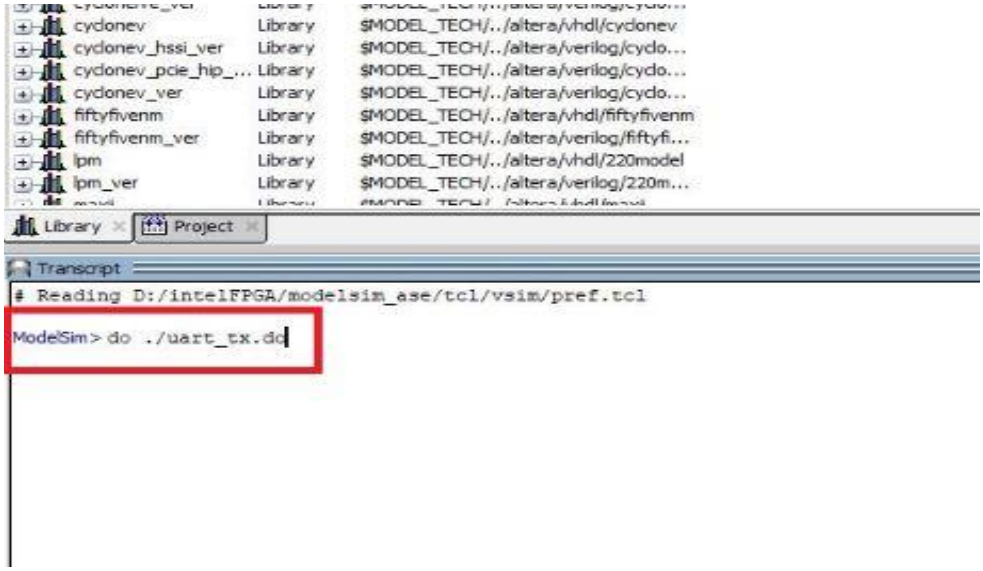
Quick Start

Step 1: Download Modelsim. There are free versions available online. The one I am using is Modelsim ME from Microsemi. (This could be out of date)

Step 2: Install Modelsim and note the folder that the install is located in.

Step 3: Setup your “modelsim.bat.placeholder” file located in tools/Modelsim. To do this, paste the address in the file where your modelsim.exe is located. Then delete the .placeholder from the end of the file and you should now be able to open modelsim by double clicking the modelsim.bat file.

Step 4: Once modelsim opens, you can now choose a test to run. All tests are contained in their own .do file. To run a simple, go to the transcript panel and run “do ./<test name here>.do”.



Step 5: Once the test has finished running you should be able to view the waveforms from the tests.

DO File Structure

This will go through the elements of a do file you will need to change to create your own tests.

1. You will need to include all source and testbench files that are needed to run the test. They can be added using “vlog /<location of file/<file name>”. You can also add multiple

files in one line using the * character, such as “../../src/*.sv” to include all files from your source folder.

2. Make sure that the item of this line is the name of the testbench module that you want to run.
3. Pick a location and name for your wave file. The wave file is another .do file that you can create and save to choose which pieces of logic will be displayed in your wave viewer. When you first run your <test>.do top level file, there will be an error that the wave file does not exist. To fix this, save a new .do wave file in the location you specified in the current .do file. I will add an explanation below on how to do that.

```
1   # Create work library
2   vlib work
3
4   # Compile Verilog
5   vlog ../../src/uart_rx.sv  1
6
7   # Call vsim to invoke simulator
8   #     Make sure the last item on the line is the name of the
9   #     testbench module you want to execute.
10  vsim -voptargs="+acc" -t 1ps -lib work uart_rx_tb    2
11
12
13
14  # Source the wave do file
15  #     This should be the file that sets up the signal window for
16  #     the module you are testing.
17  do wave/wave_uart_rx.do                    3
18
19
20  # Set the window types
21  view wave
22  view structure
23  view signals
24
25  # Run the simulation
26  run -all
27
28  # End
```

Saving a Waveform .do File

1. Run a test and go to the waveform viewer tab
2. Add signals to the waveform viewer that you would like to keep

3. Click on File->Save Format
4. Enter the location of the file that you specified in the test level .do file.
5. When you rerun the test, your waveform should automatically come up now.