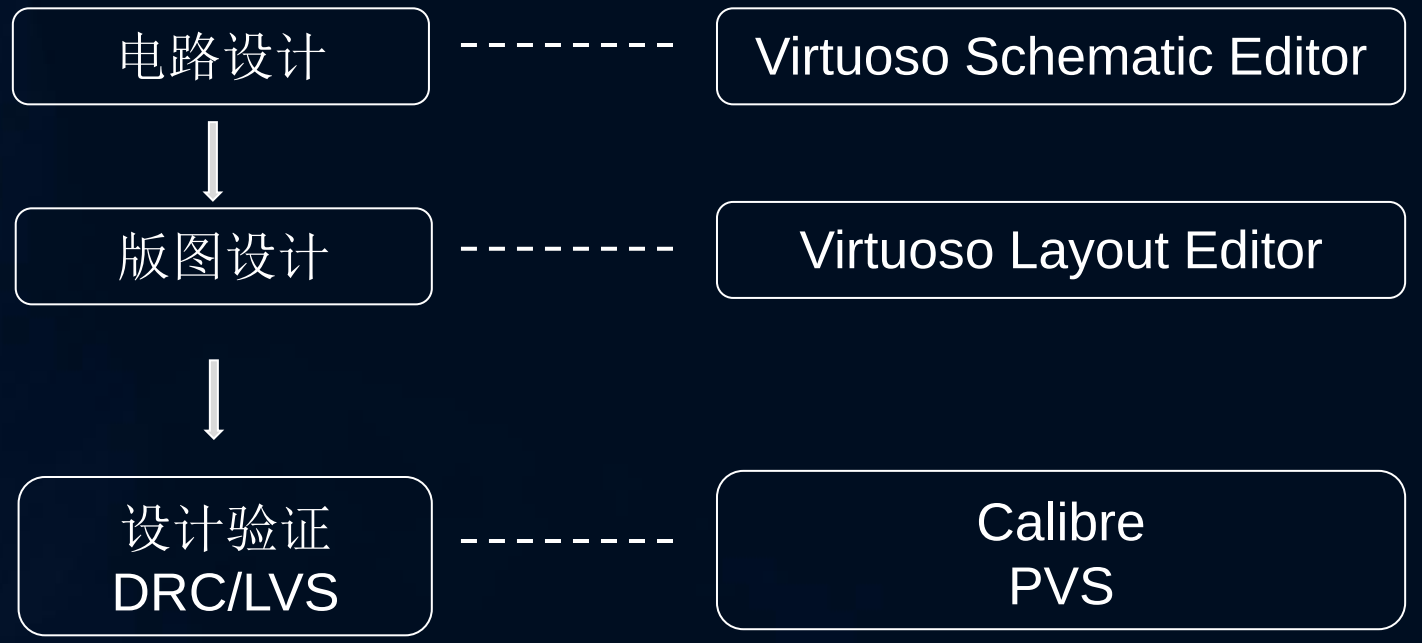
集成电路版图设计培训

Charlie

课程内容

1. DEA软件使用 — 版图编辑和物理验证工具
2. CMOS工艺中的层次
3. 基本器件和单元的版图结构
4. Stdcell 标准单元
5. 数字电路
6. 模拟电路
7. 模拟电路高级技能

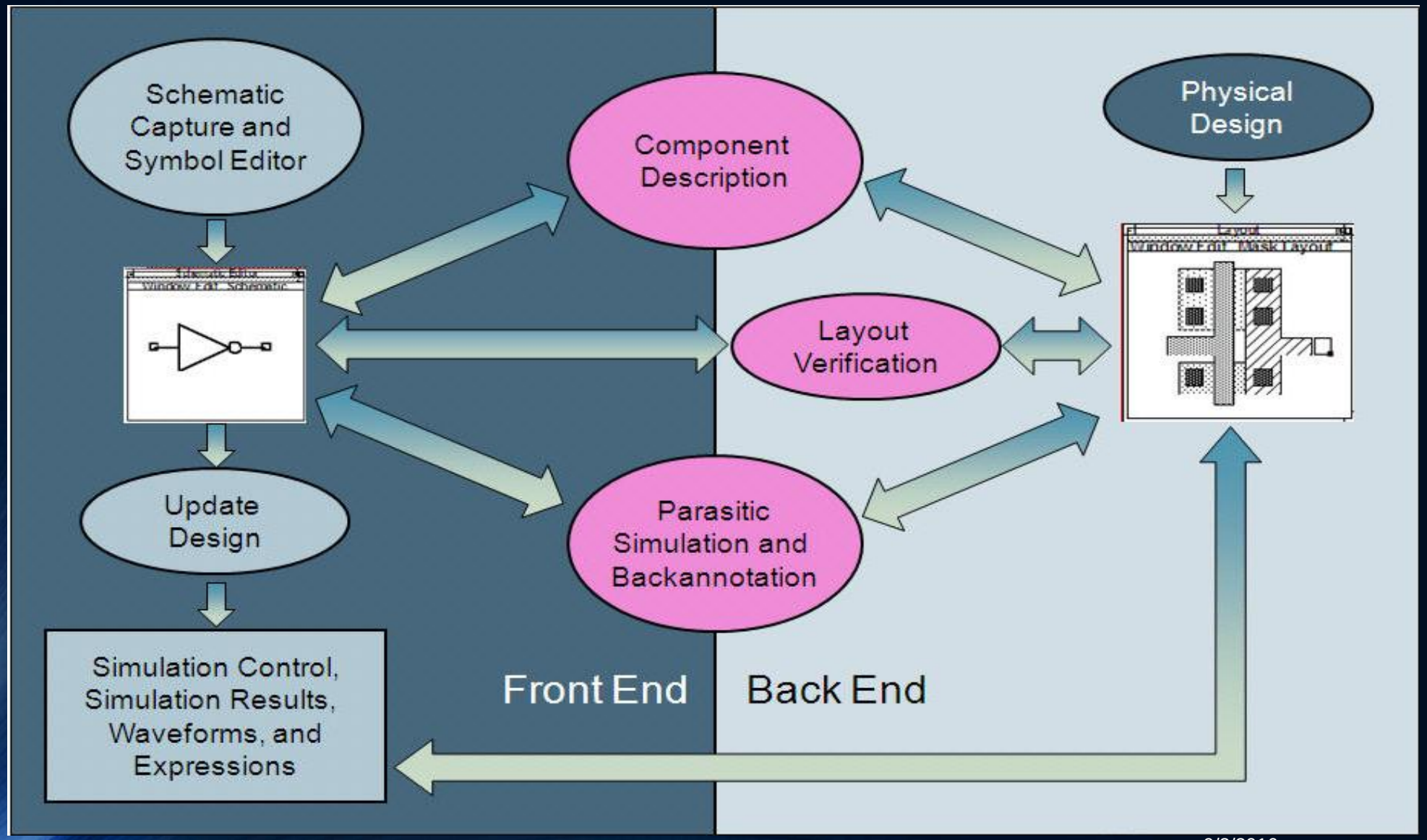
版图设计流程与对应EDA 软件



常用术语和定义

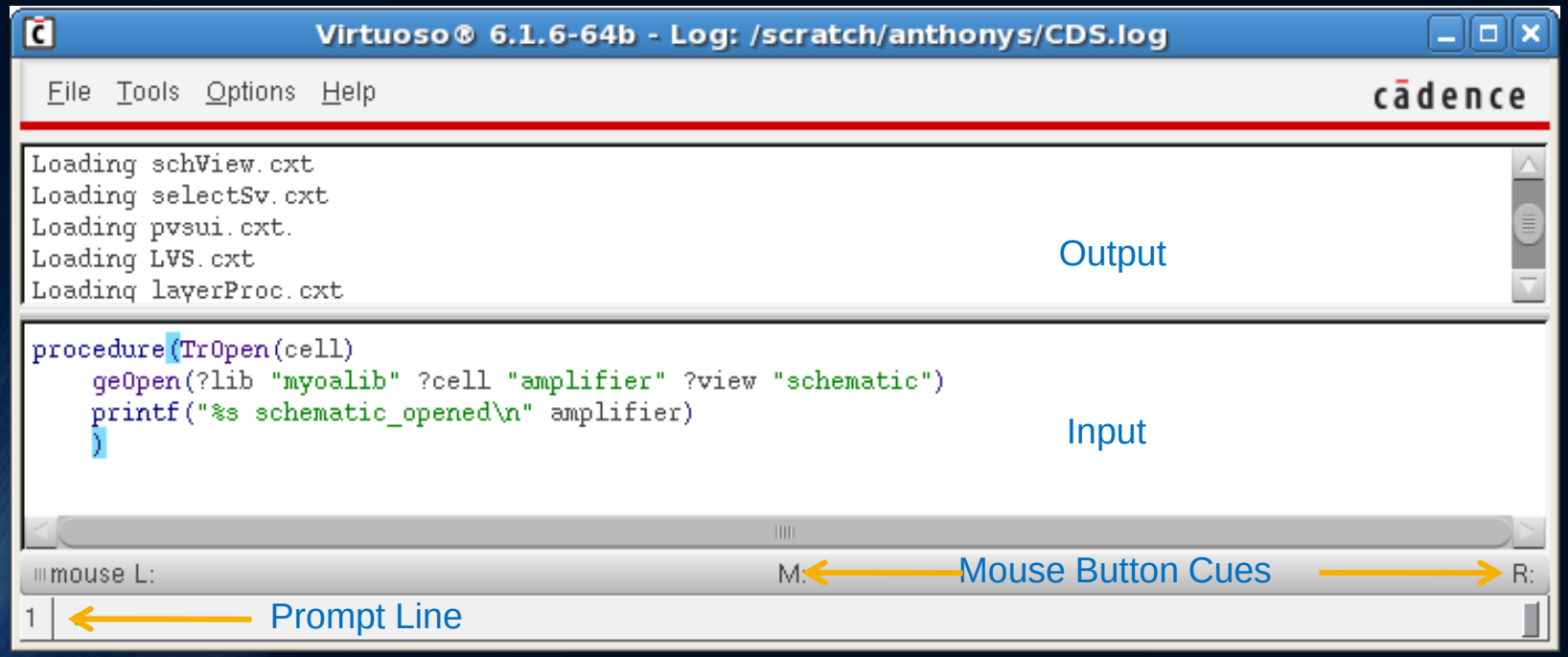
Virtuoso Design Environment	The framework that provides a common access and database for front- and back-end custom design tools
Command Interpreter Window (CIW)	The design environment interface used to access many Virtuoso applications
CWD	Current working directory (from which *virtuoso* is started)
Text entry field	A line buffer in the CIW that accepts commands written in the SKILL programming language
Cyclic field	Selectable options in an entry field, denoted by a small down arrow
Library	A collection of design cells represented by cellviews
Library Manager	A Cadence® tool to manage a design library
Cell	A basic unit of a design hierarchy described by cellviews
Cellview	A specific view of a cell (schematic, symbol, text, or layout)
Instance	A uniquely named placement of a cell symbol onto a schematic
Bindkey	A predefined key on the keyboard that applies a preselected command

Virtuoso Design Environment

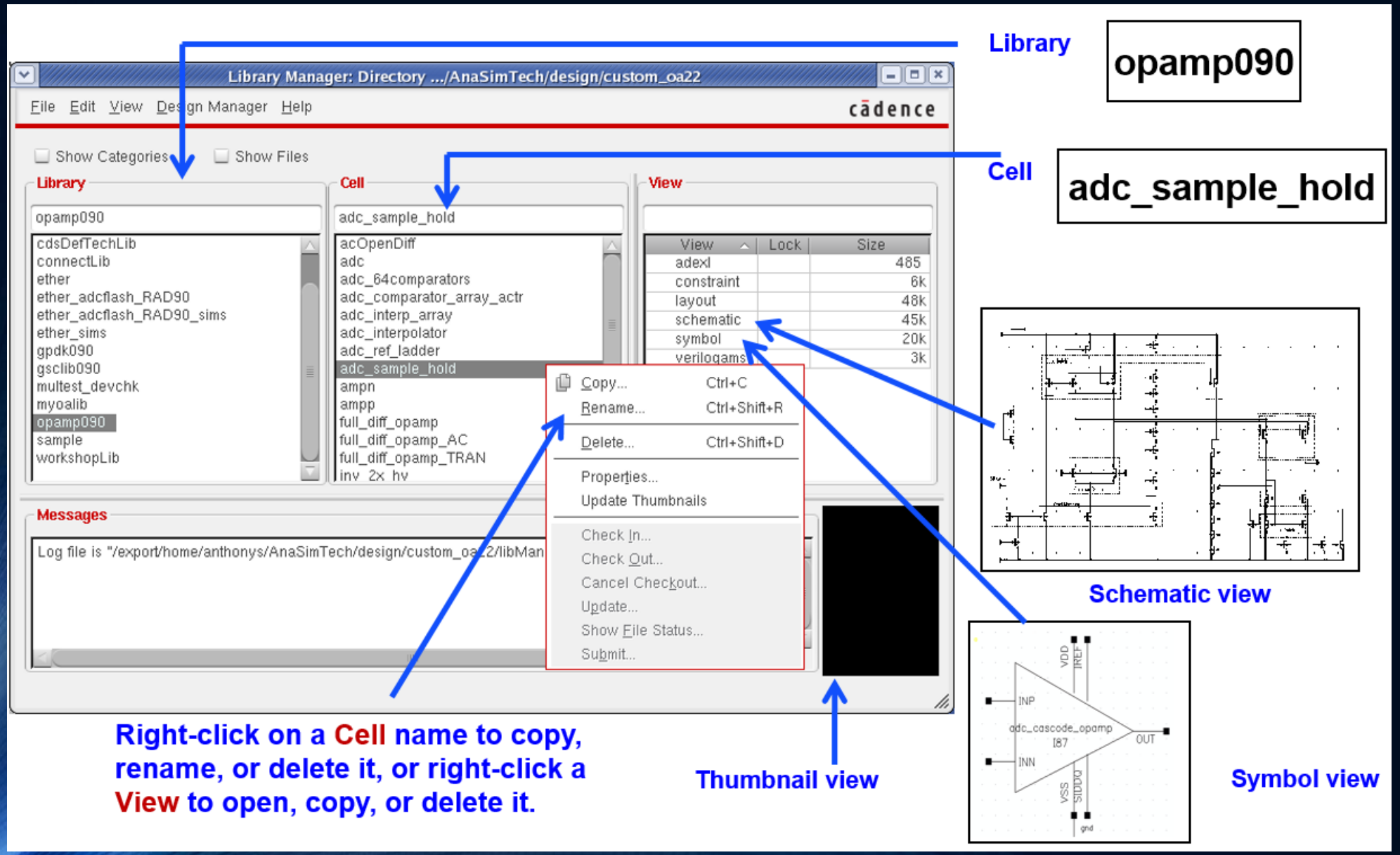


Virtuoso Command Interpreter Window

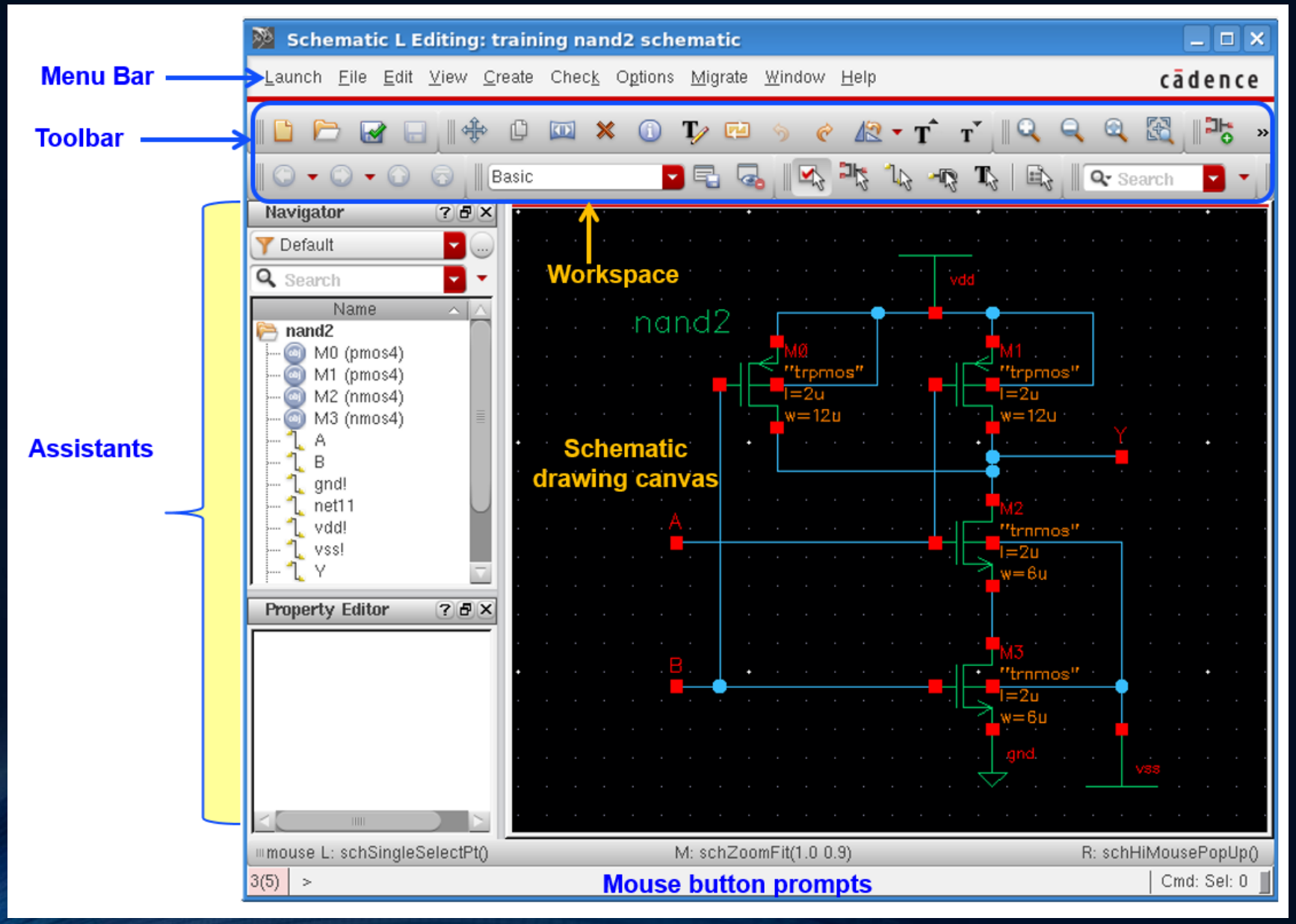
启动命令：virtuoso



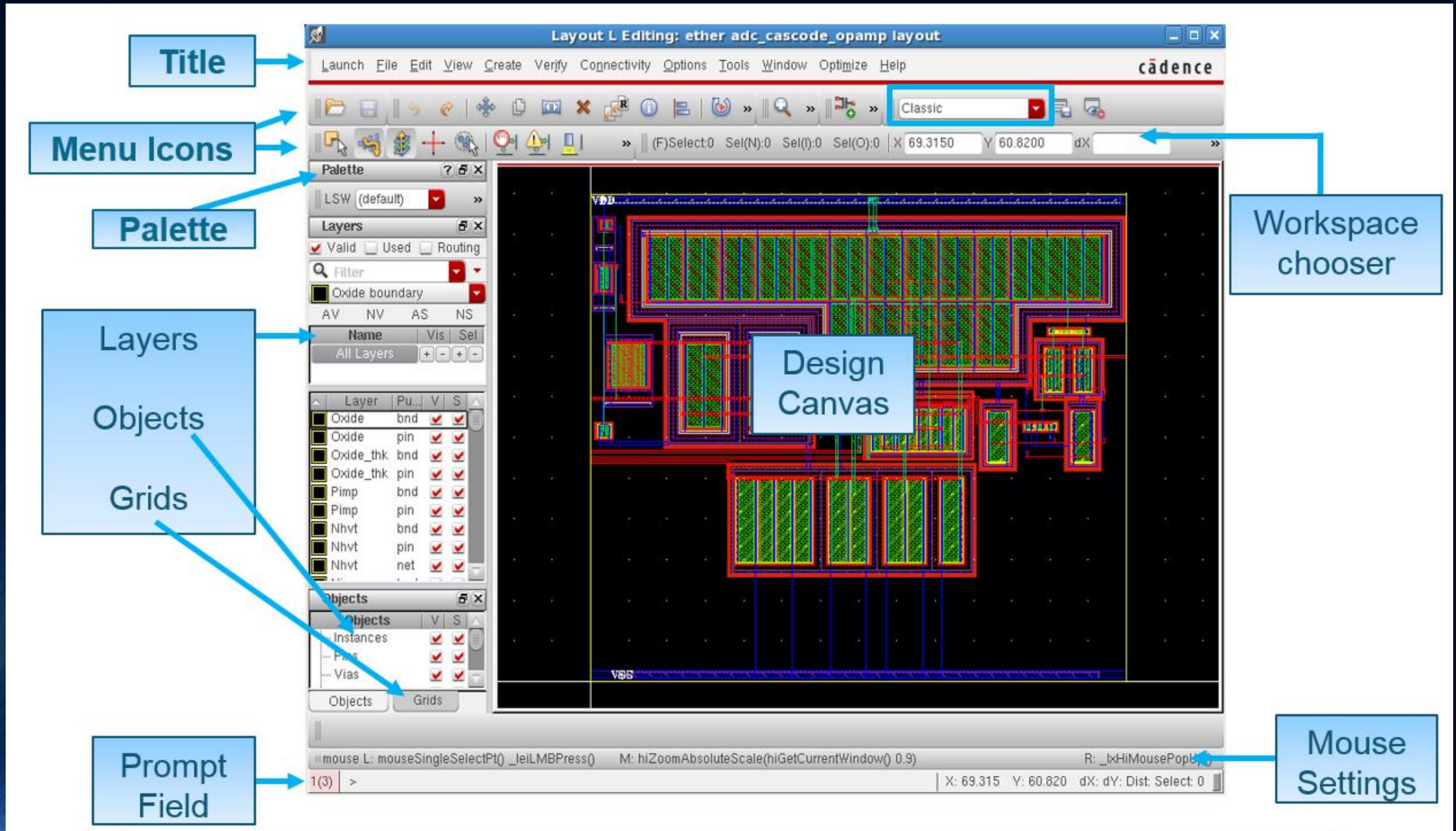
Virtuoso Library Manager



Virtuoso Schematic Editor

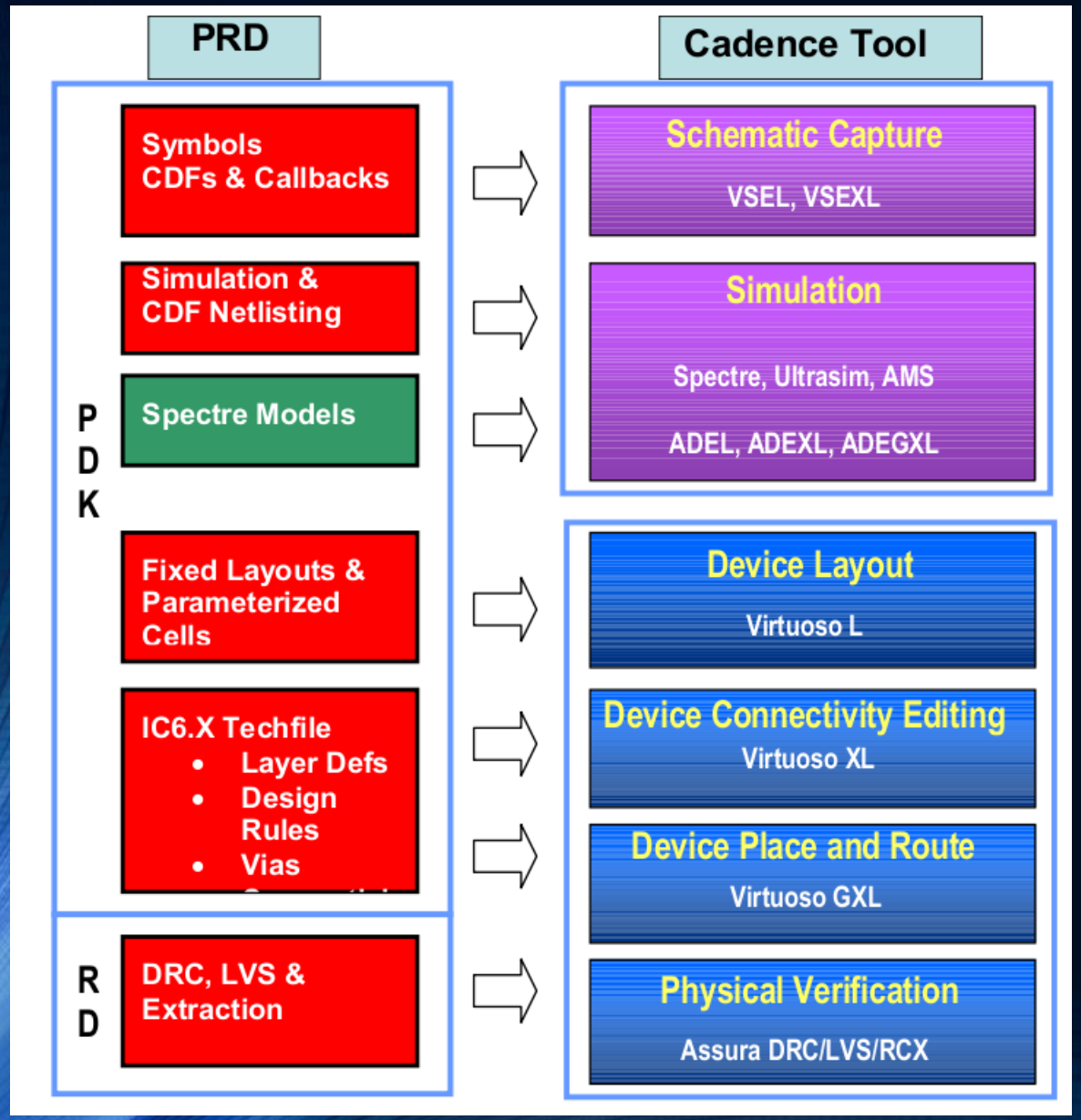


Virtuoso Layout Editor



The Palette assistant is activated by default in the Classic and Basic workspace.

Process Design Kits (PDK) and Rule Decks (RD)



Process Design Kits (PDK) contains the following:

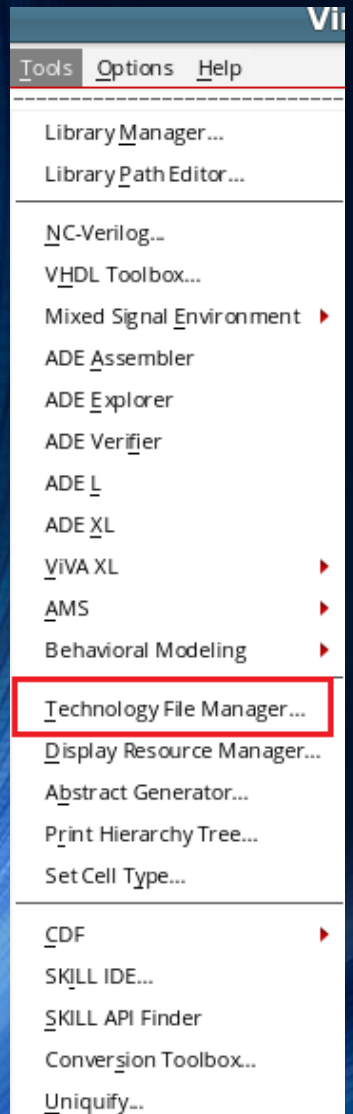
- Symbols & CDFs & Callbacks
- Simulation & CDFs
- Spectre Models
- Fixed Layouts & Parameterized Cells
- IC6.X Technology File

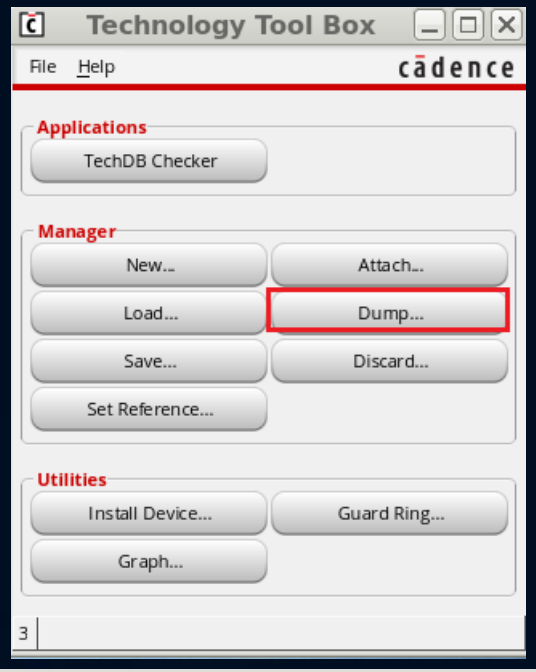
Rule Decks (RD) contain the following

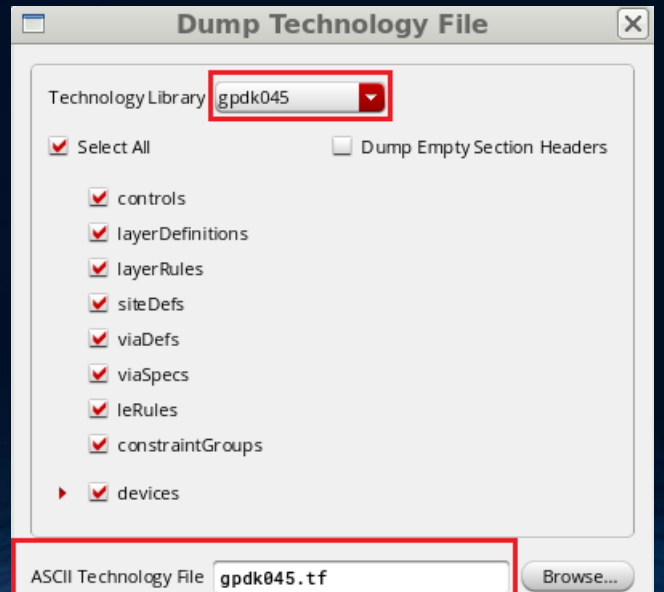
- DRC Rule Decks
- LVS Rule Decks
- Extraction Files

基本操作— 查看工艺文件(Technology File)

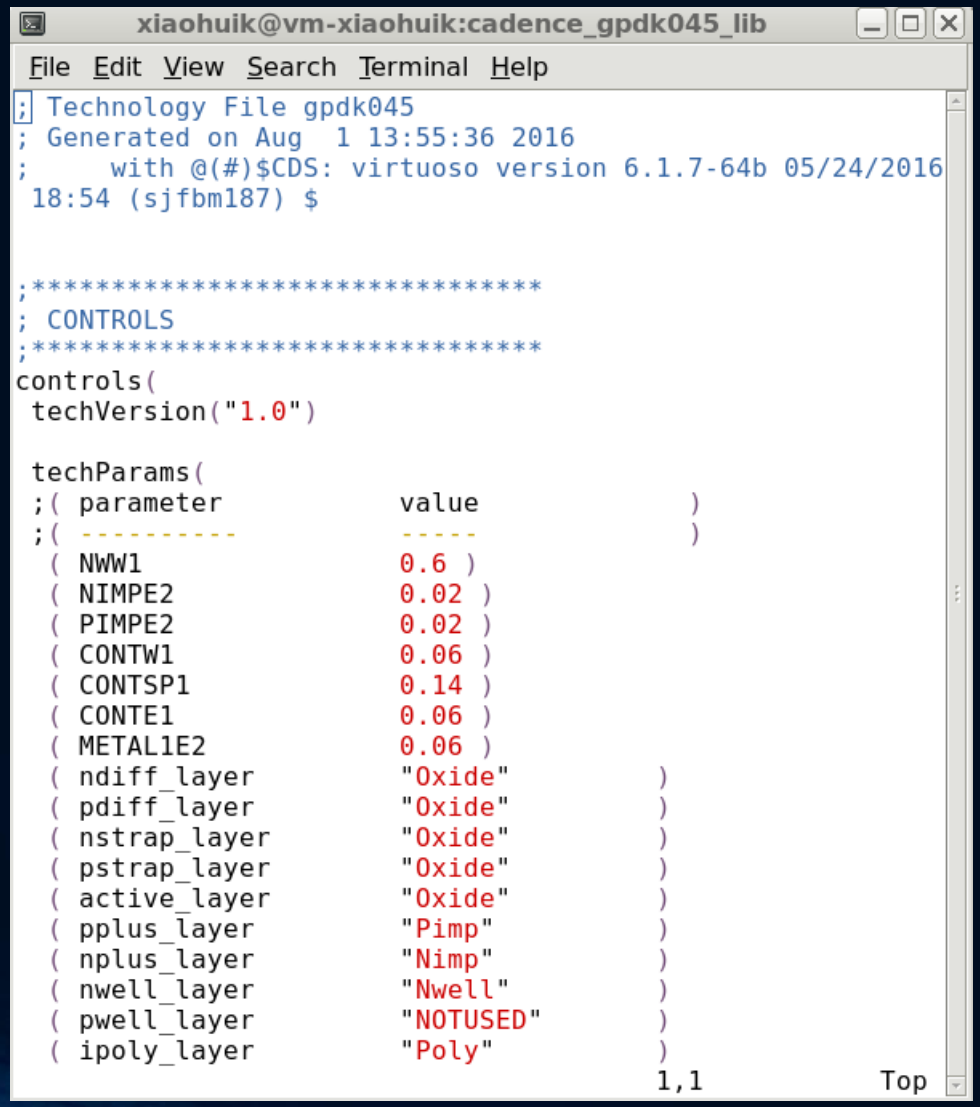
Tools → Technology File Manager





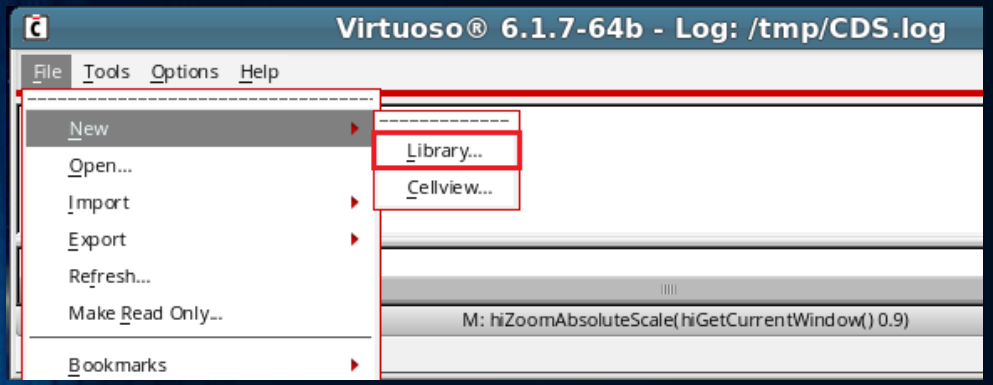


Technology File

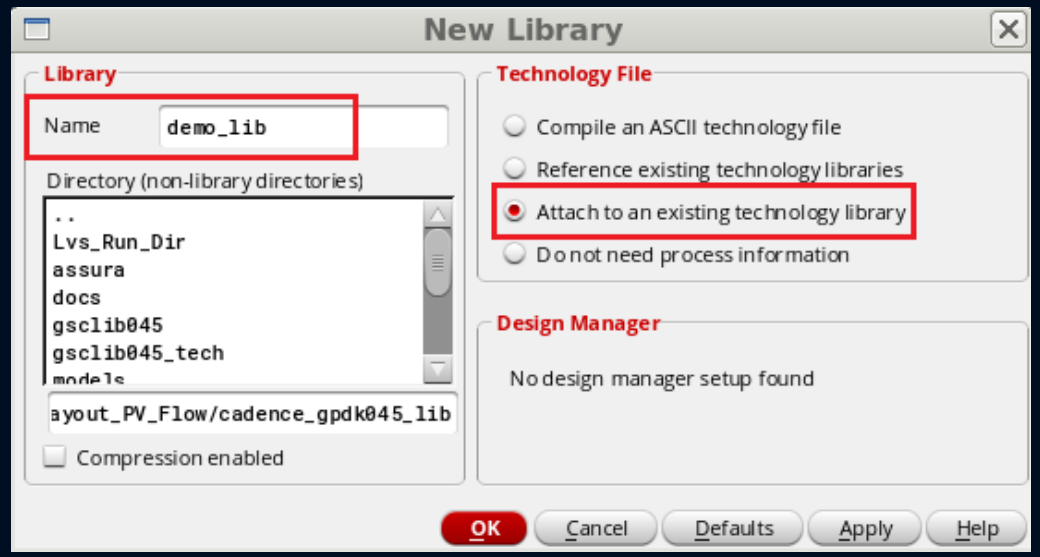


基本操作— 建立一个库

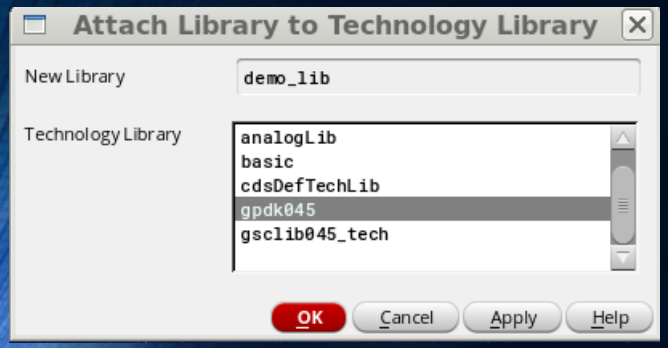
File→ New → Library



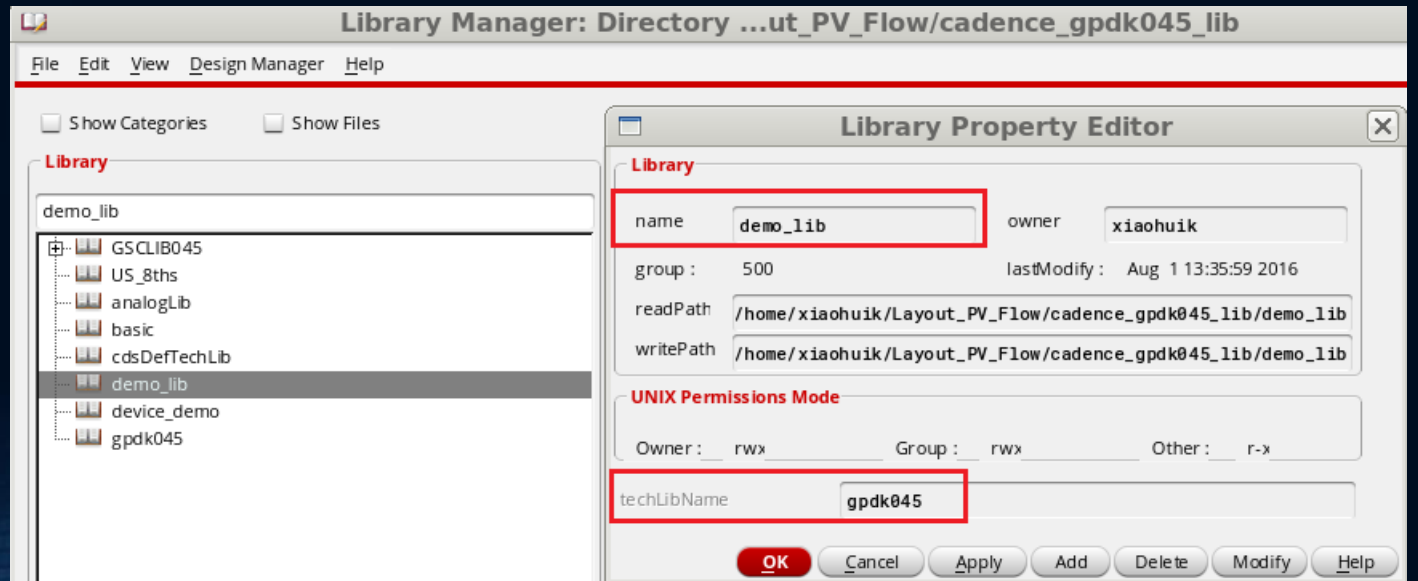
填写库名称和指定工艺文件



选择PDK工艺库

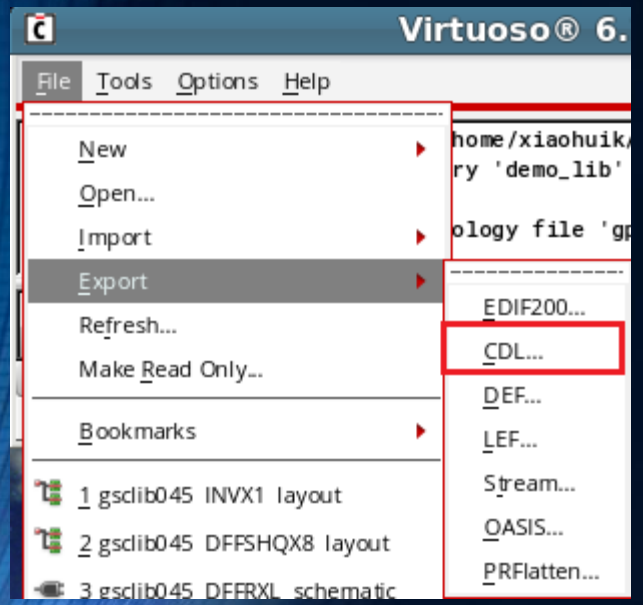


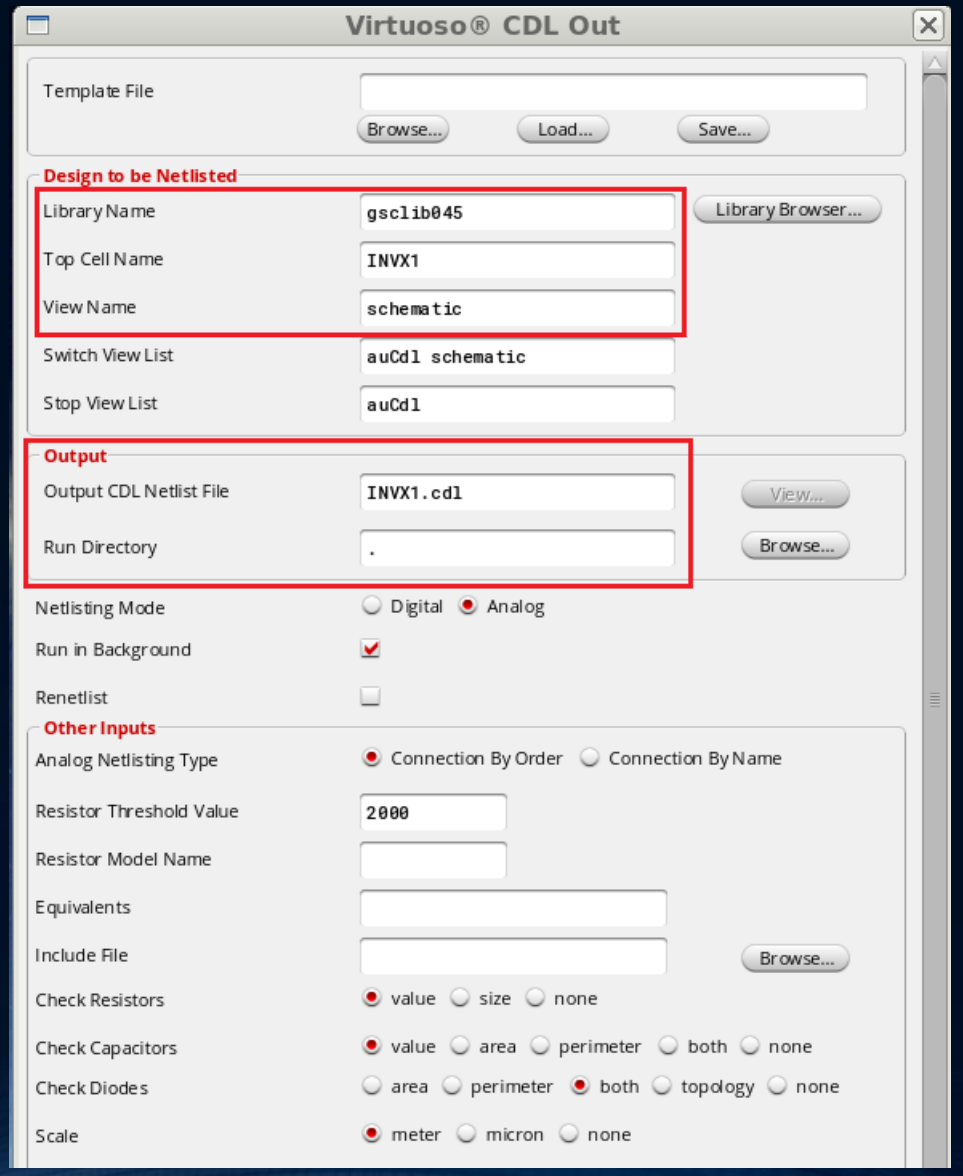
查看新建库的属性

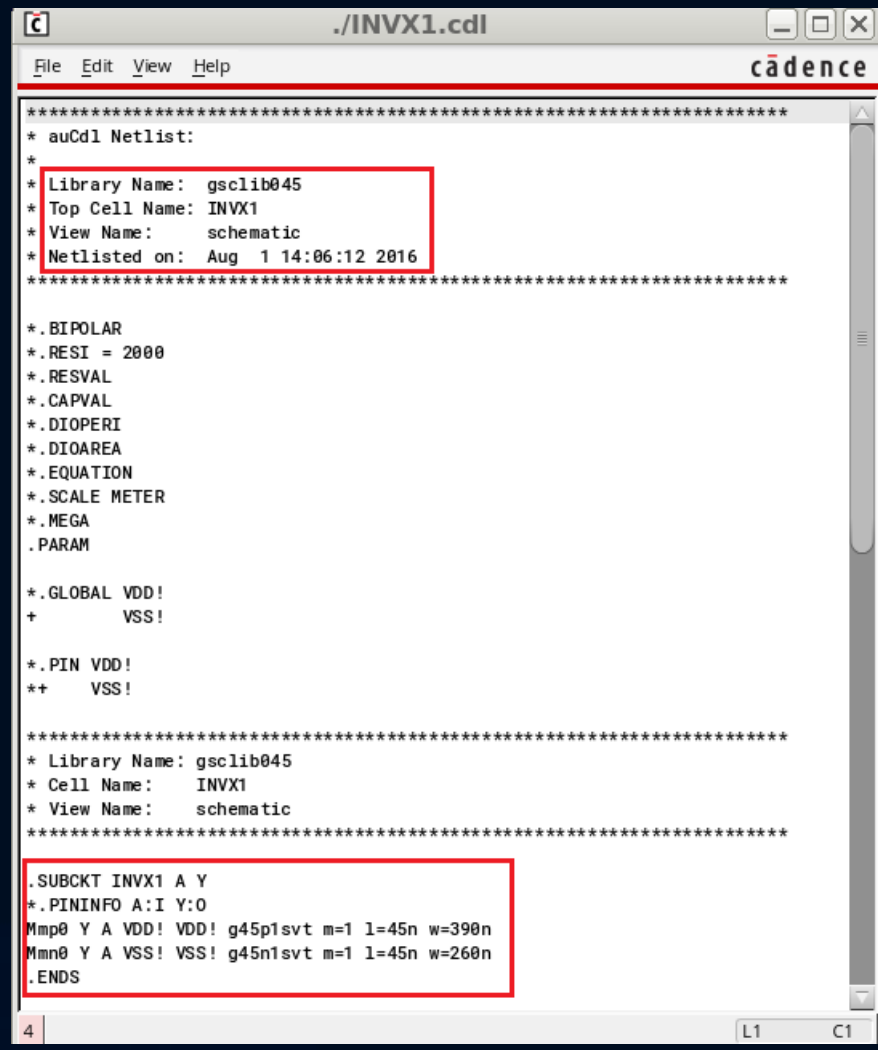


基本操作— 导出设计网表

File → Export → CDL

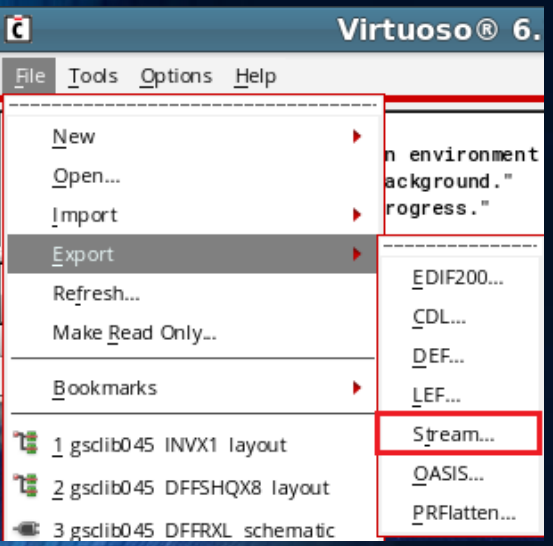


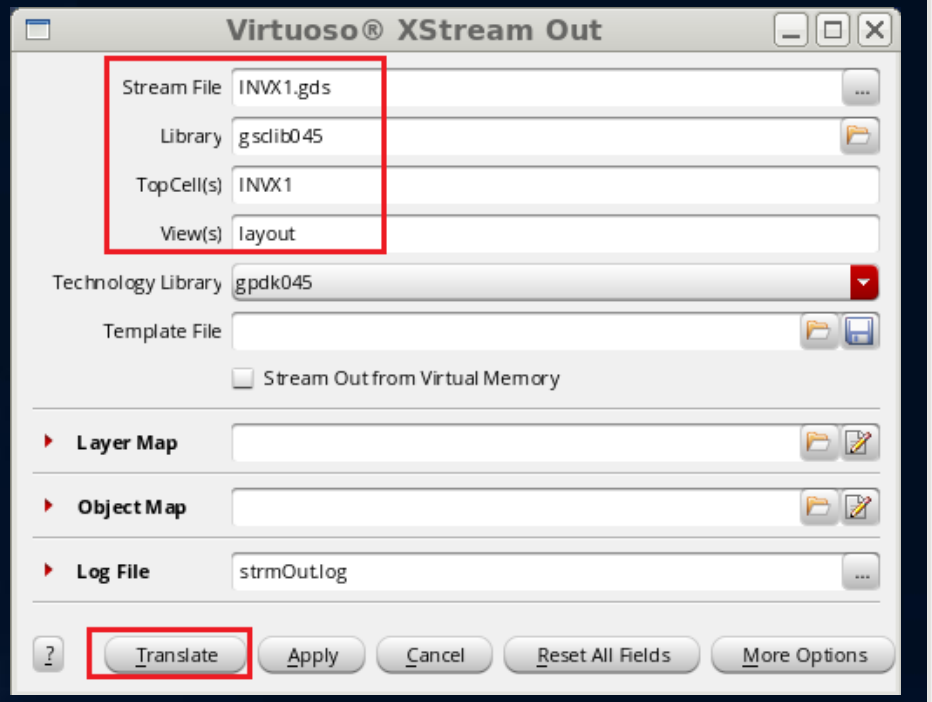




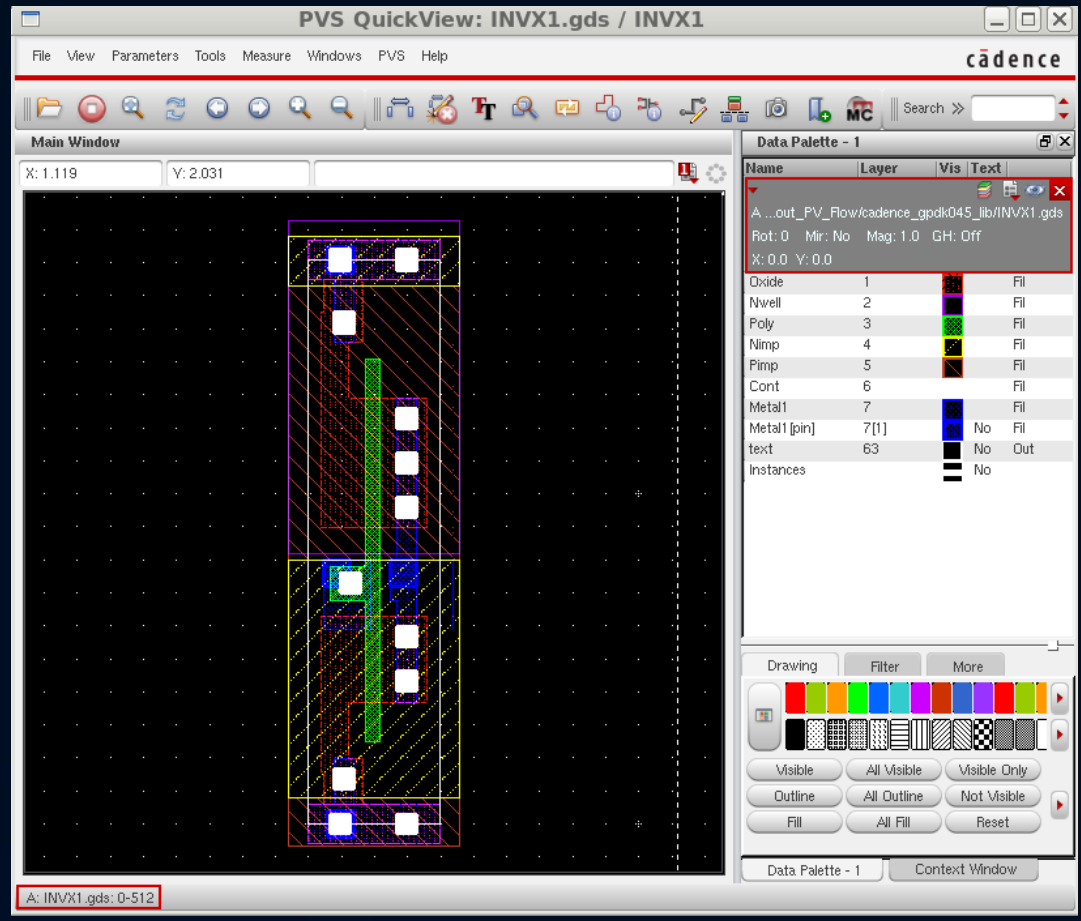
基本操作— 导出设计版图

File → Export → Stream

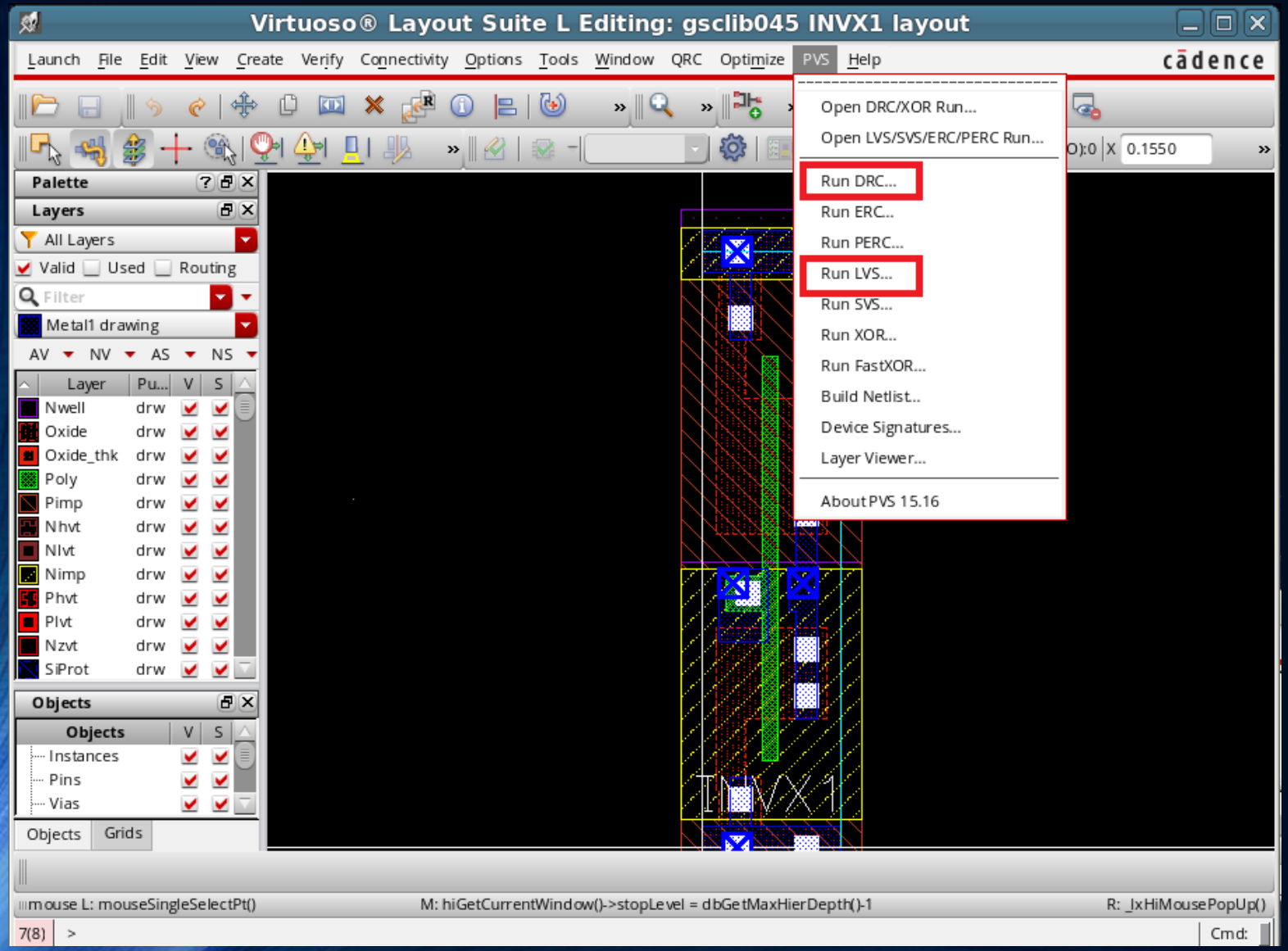




Gds Viewer

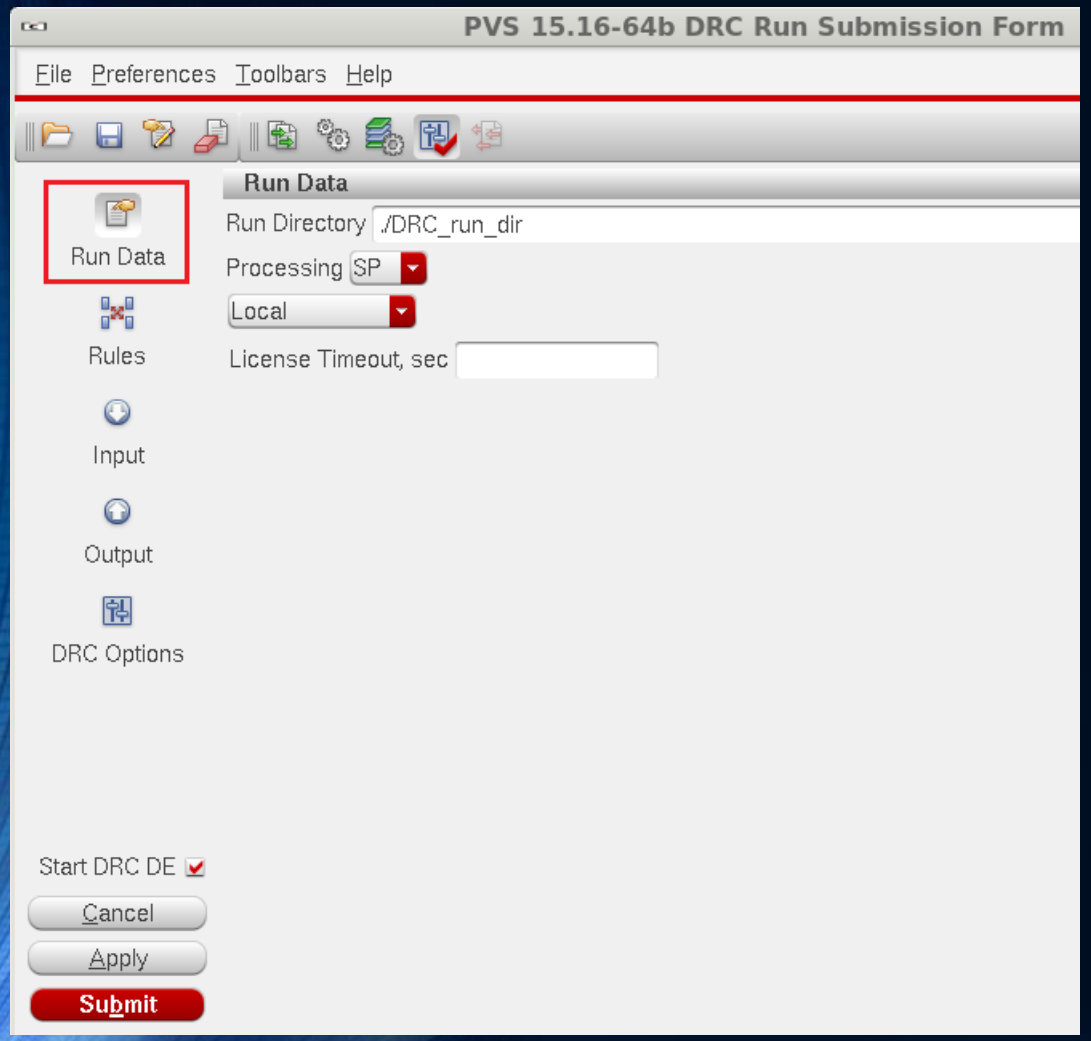


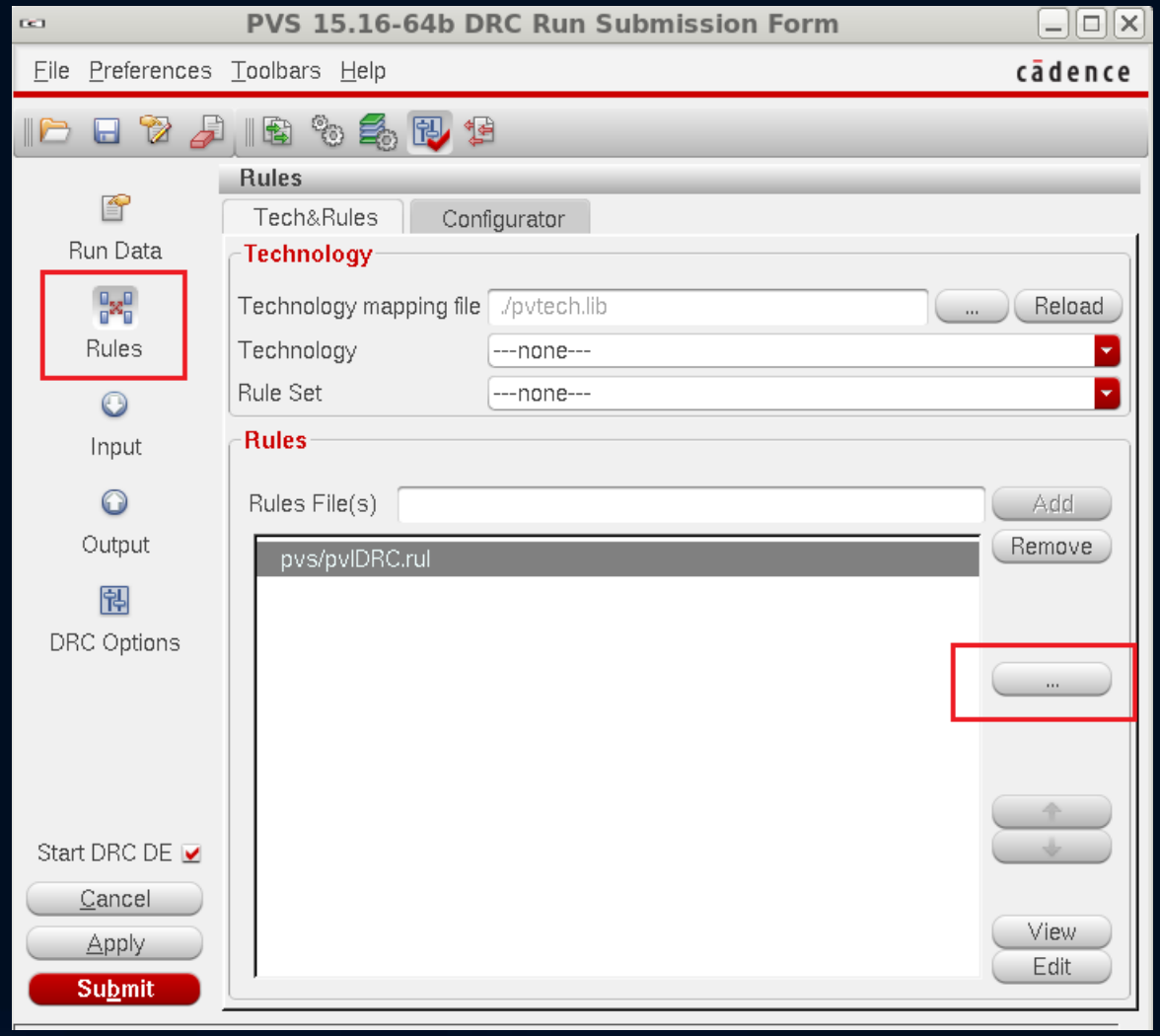
Physical Verification System (PVS)



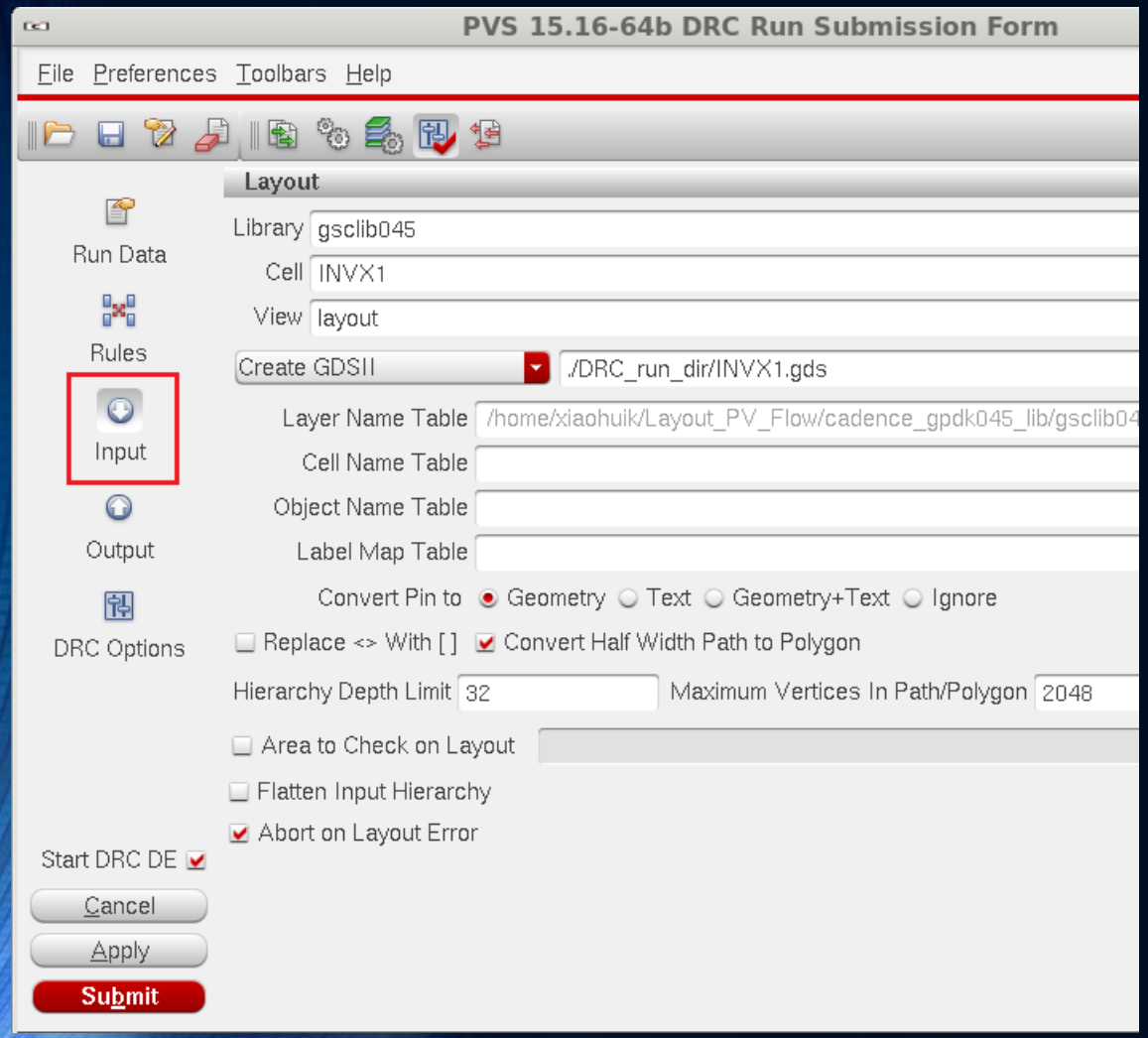
Design Rule Check (DRC)
Layout Vs. Schematic (LVS)

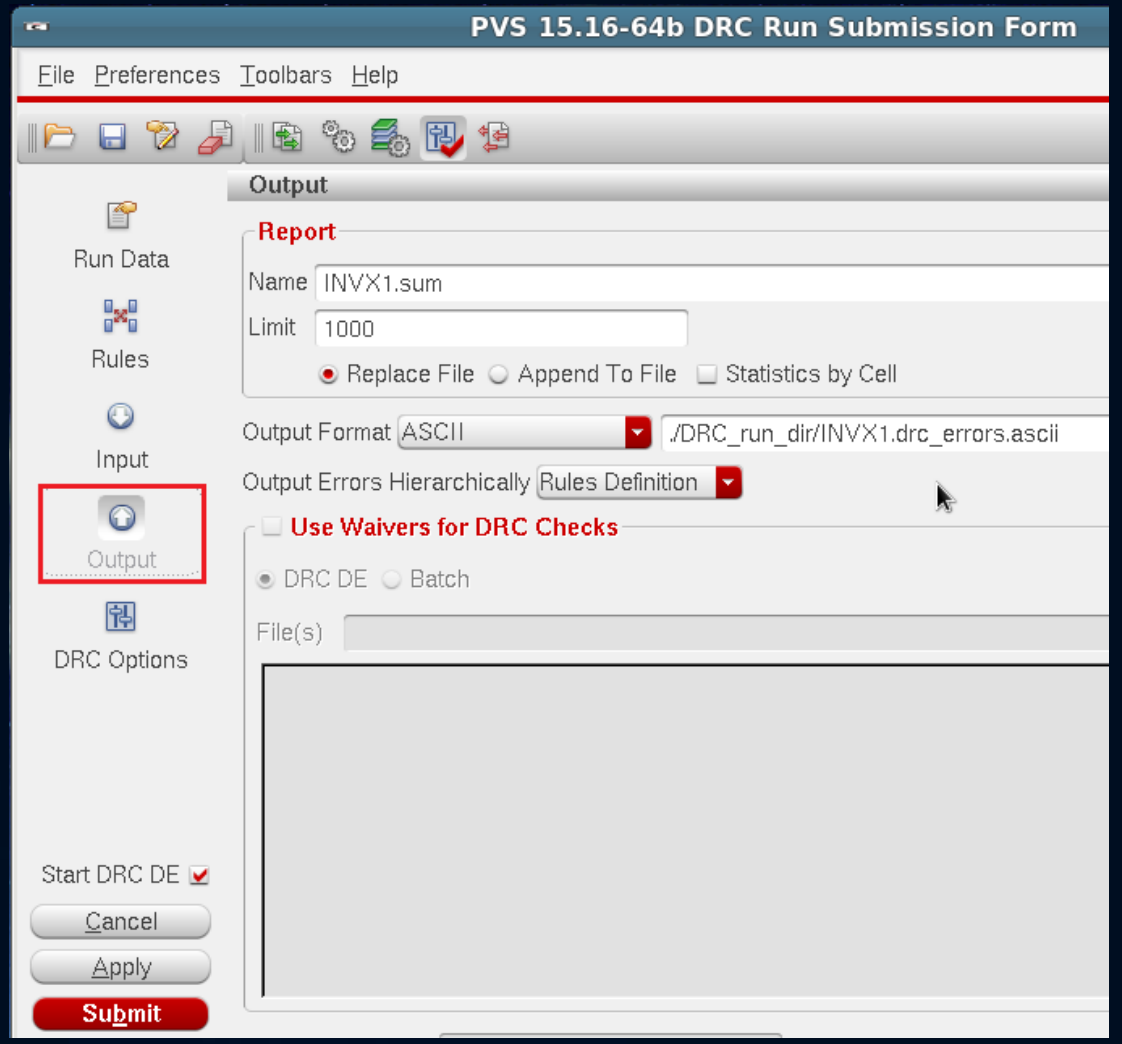
DRC检查选项 — Run Data and Rules



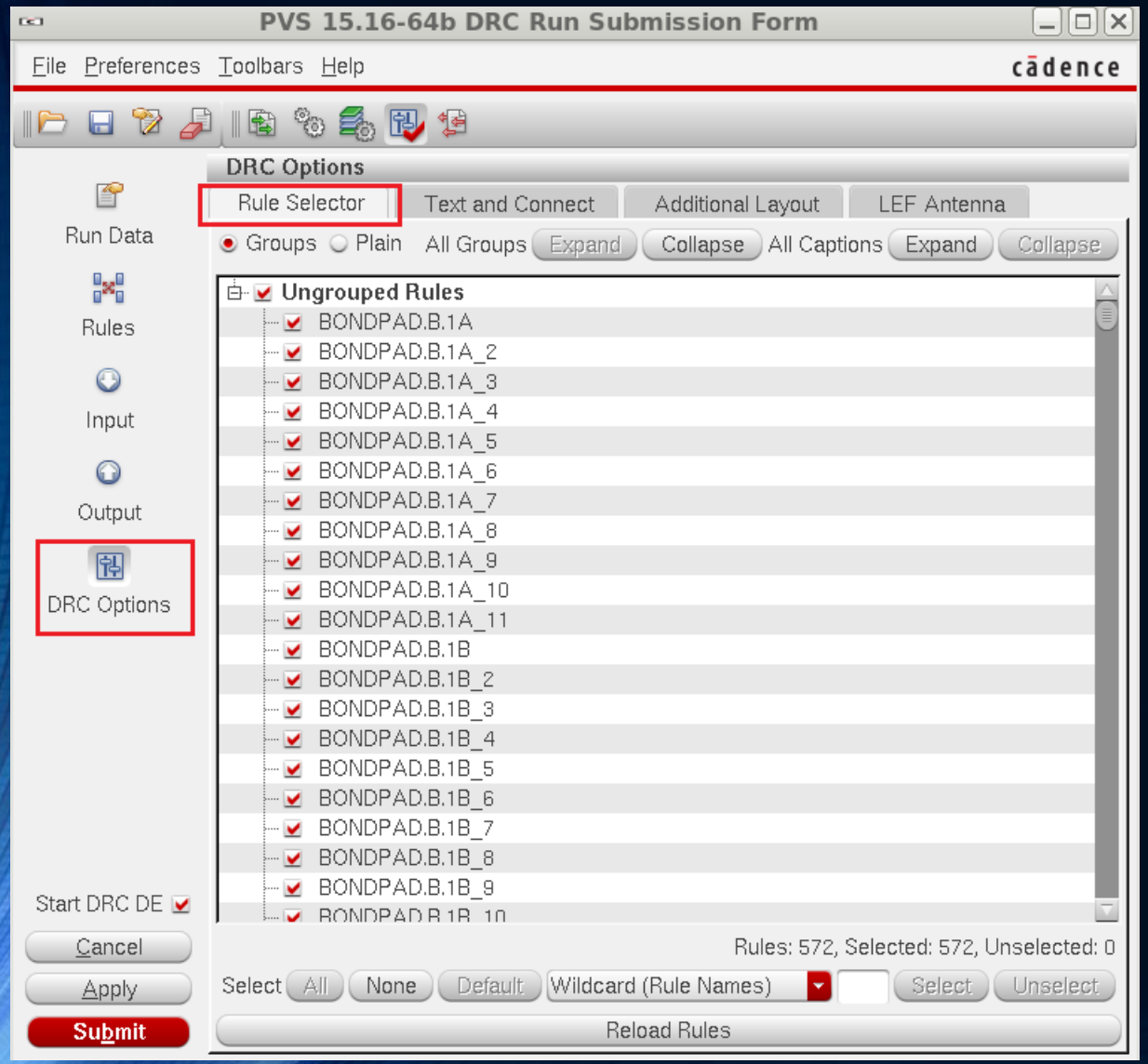


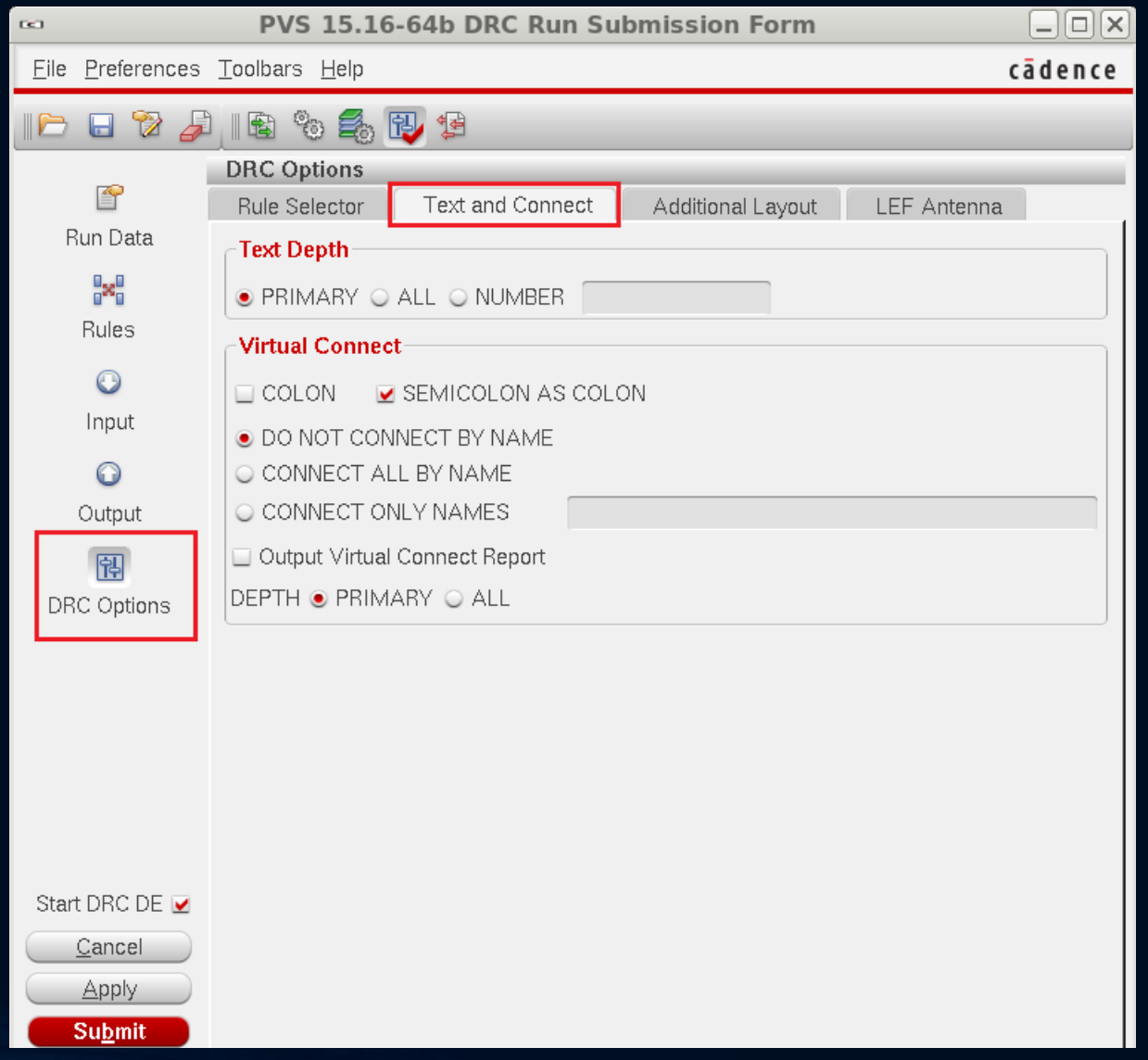
DRC检查选项 — Input and Output



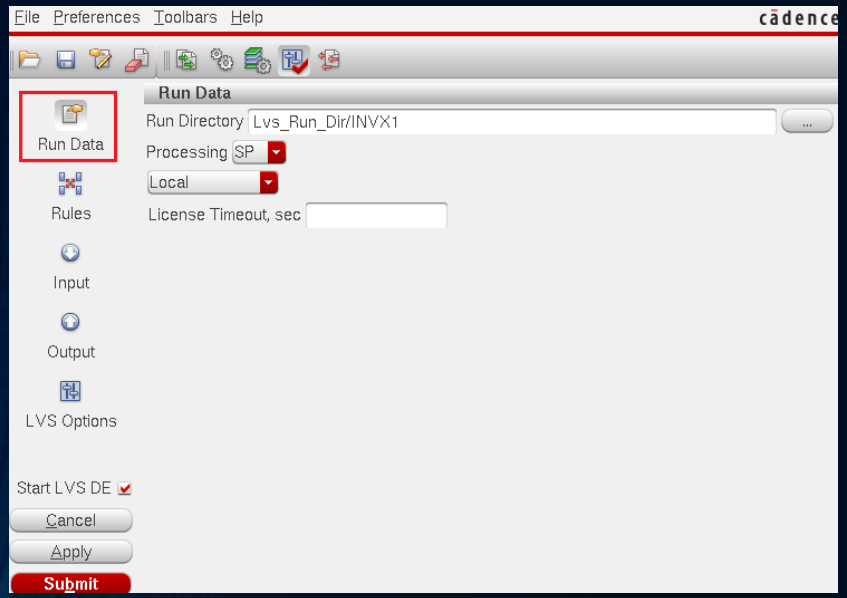


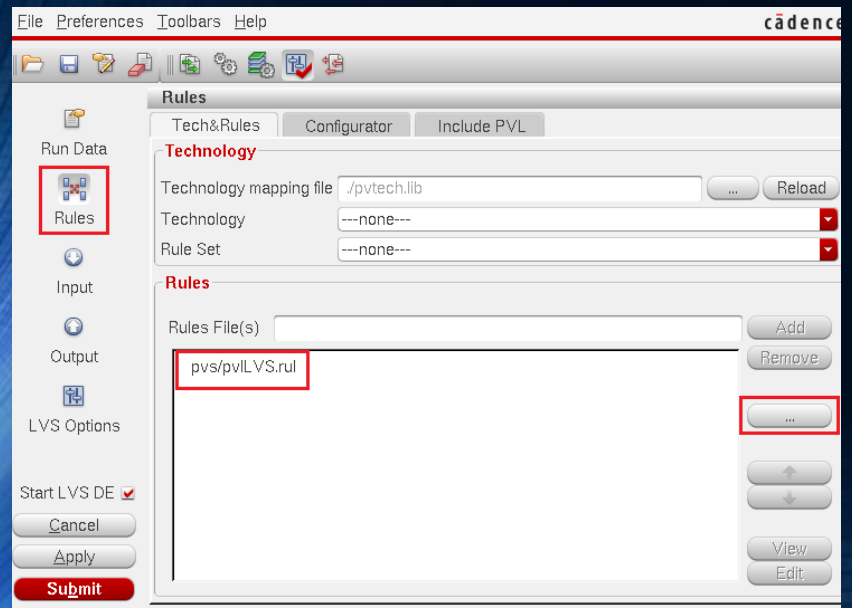
DRC检查选项 — Rule Selector and Text Options

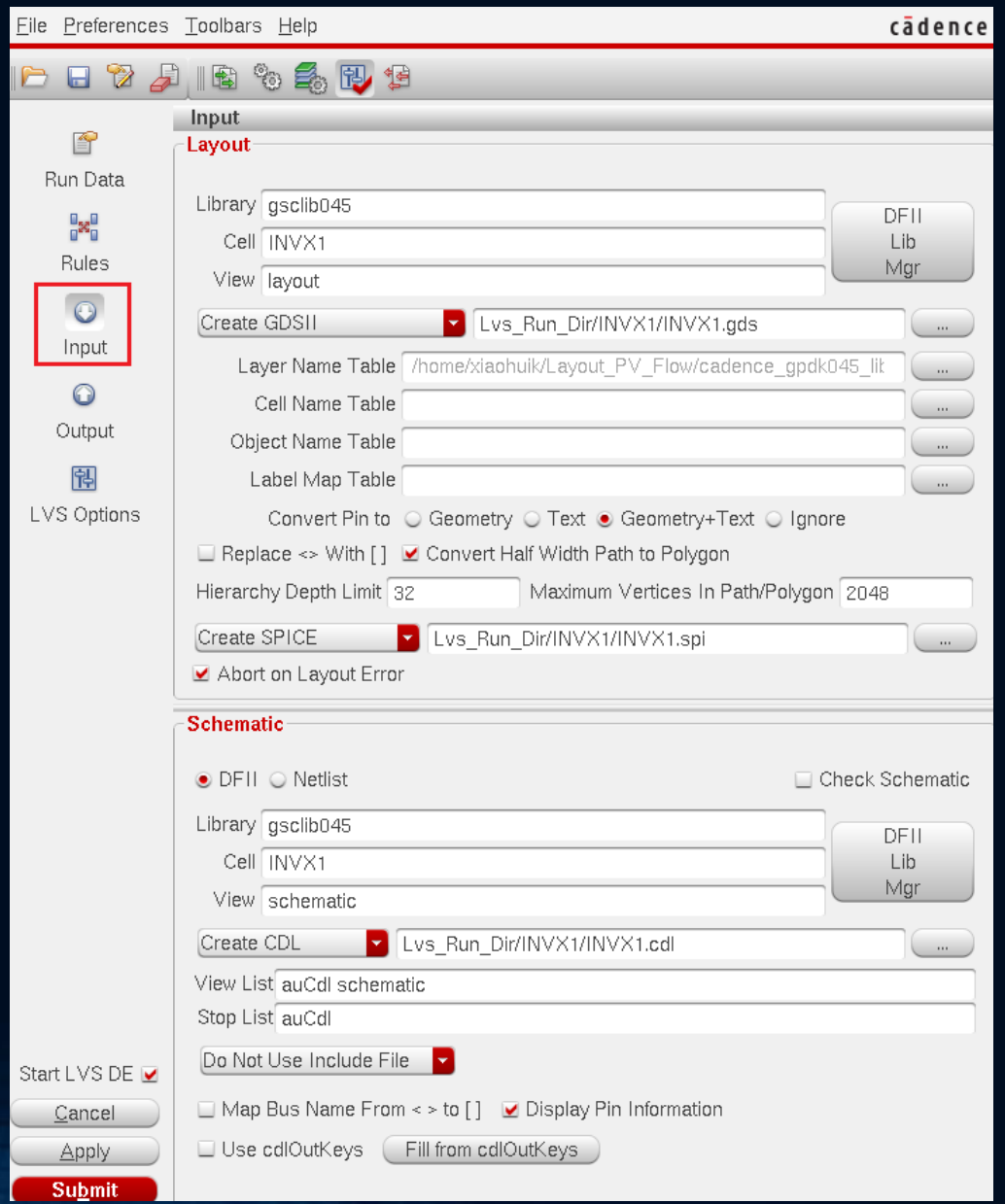




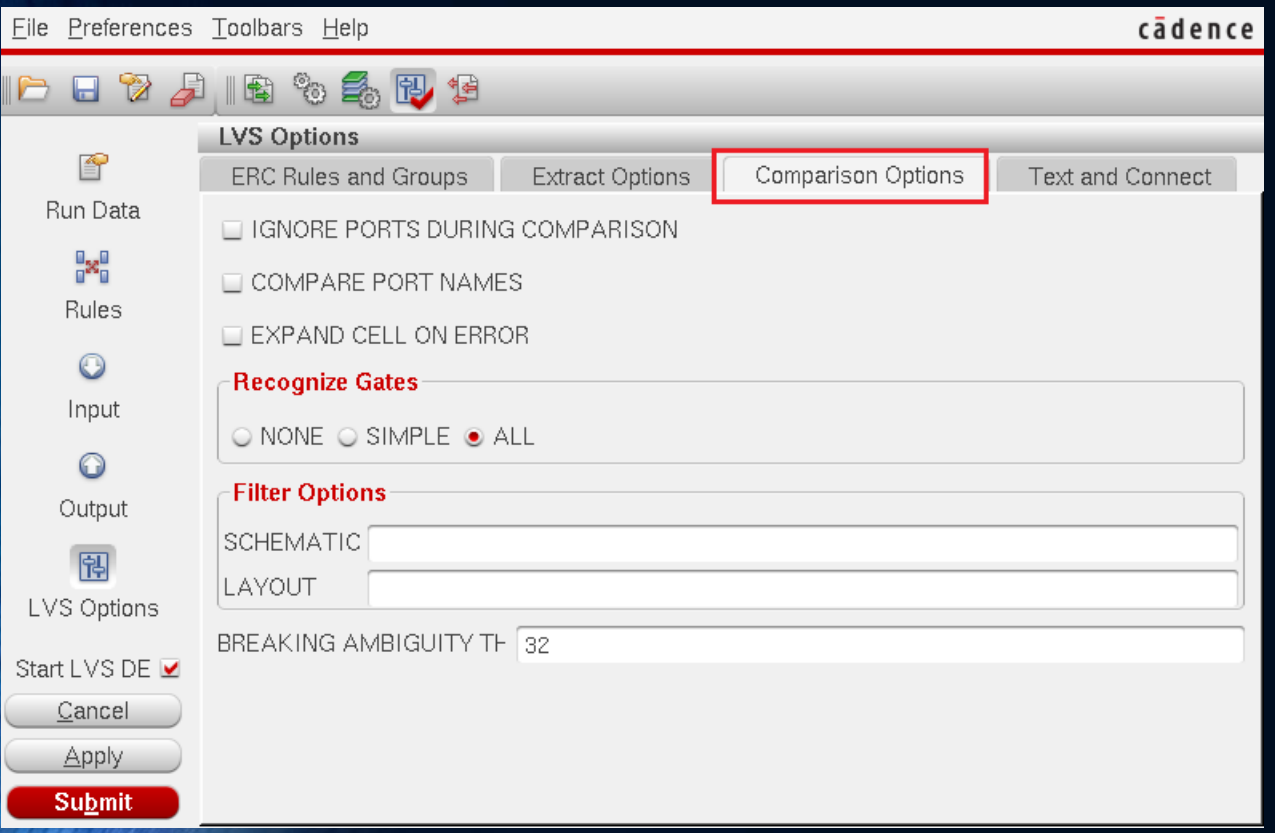
LVS检查选项 — Run Data, Rules and Input

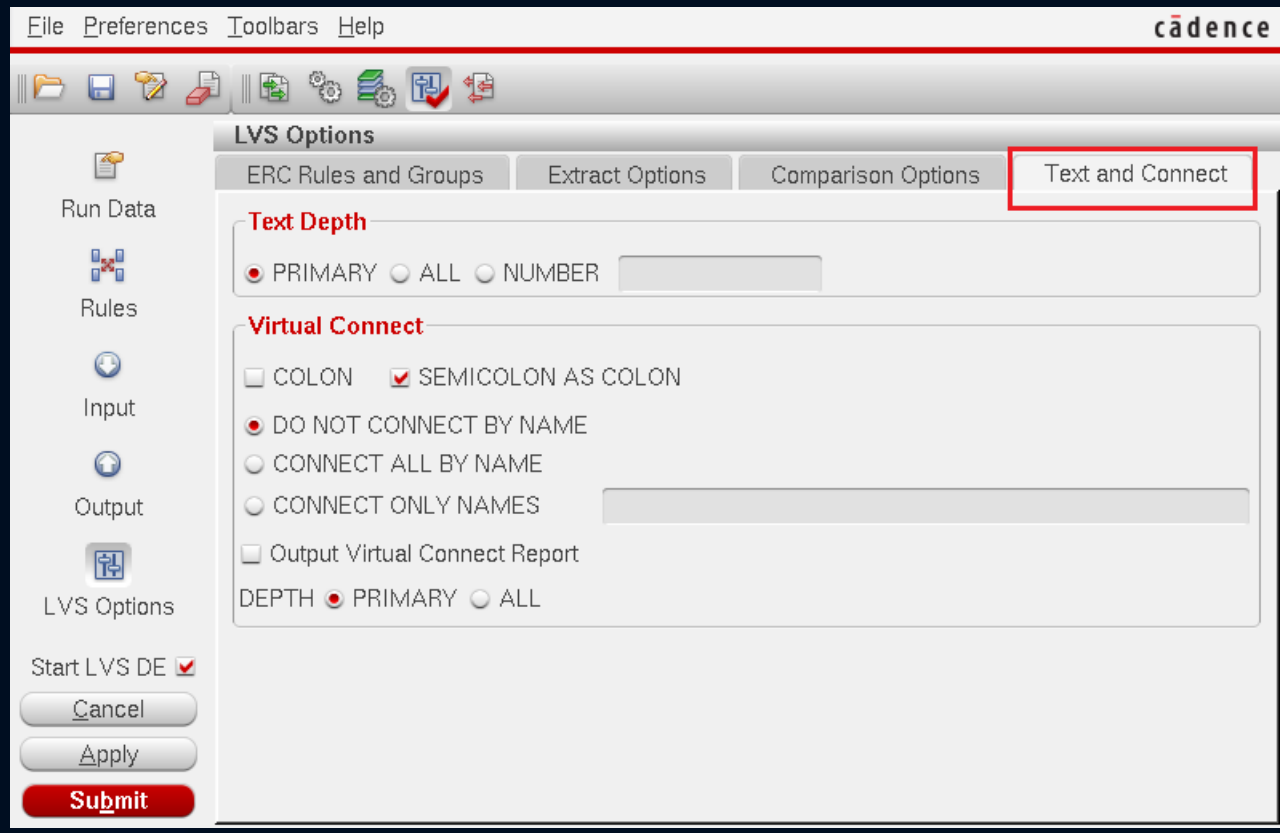




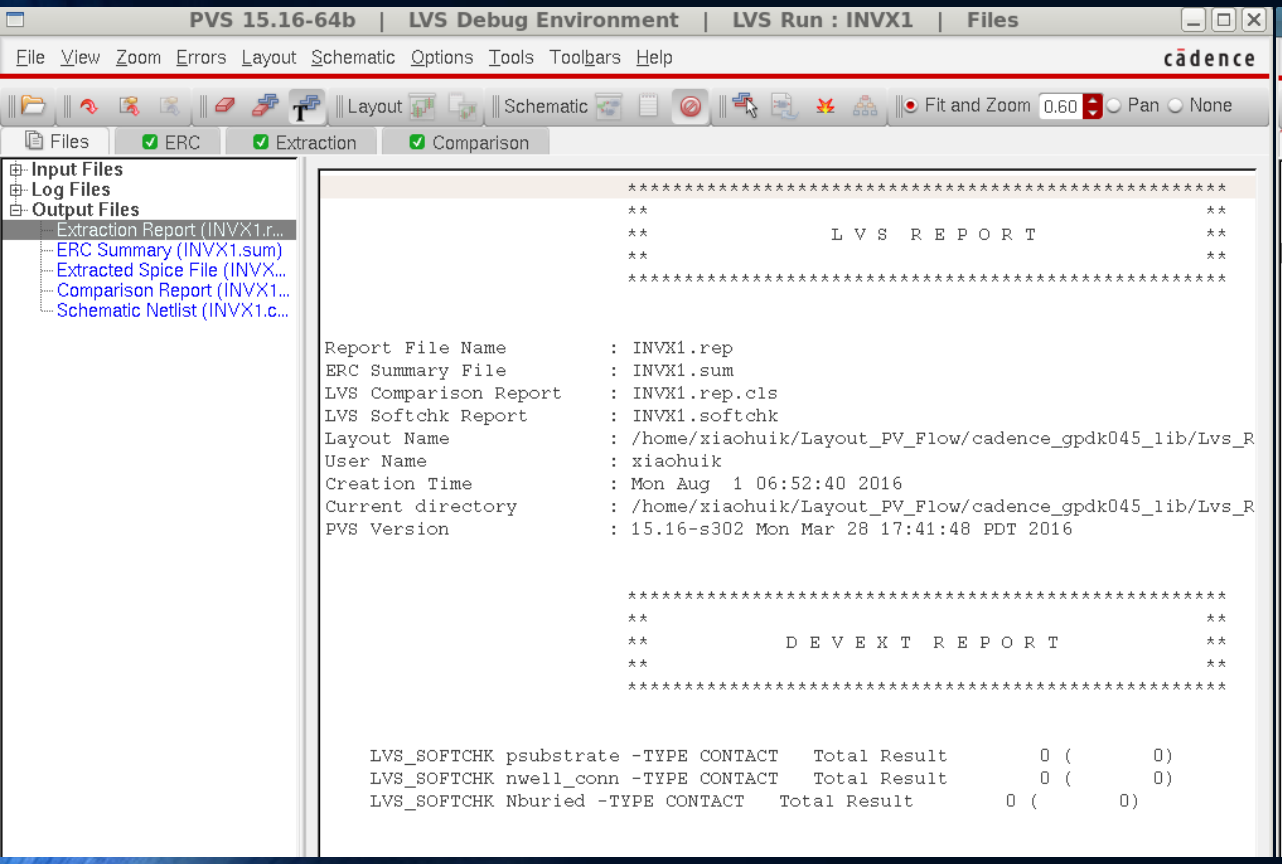


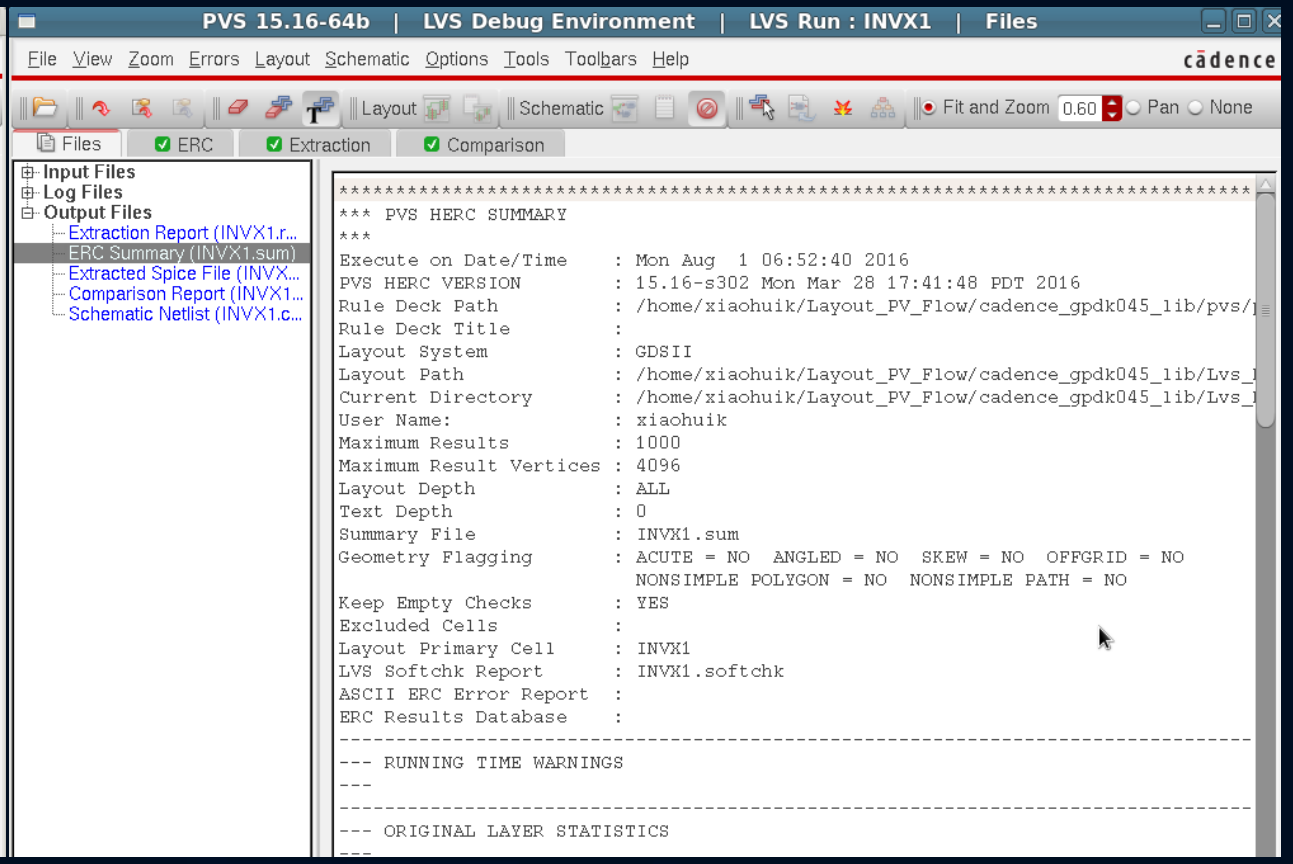
LVS检查选项 — Comparison Options and Text Options



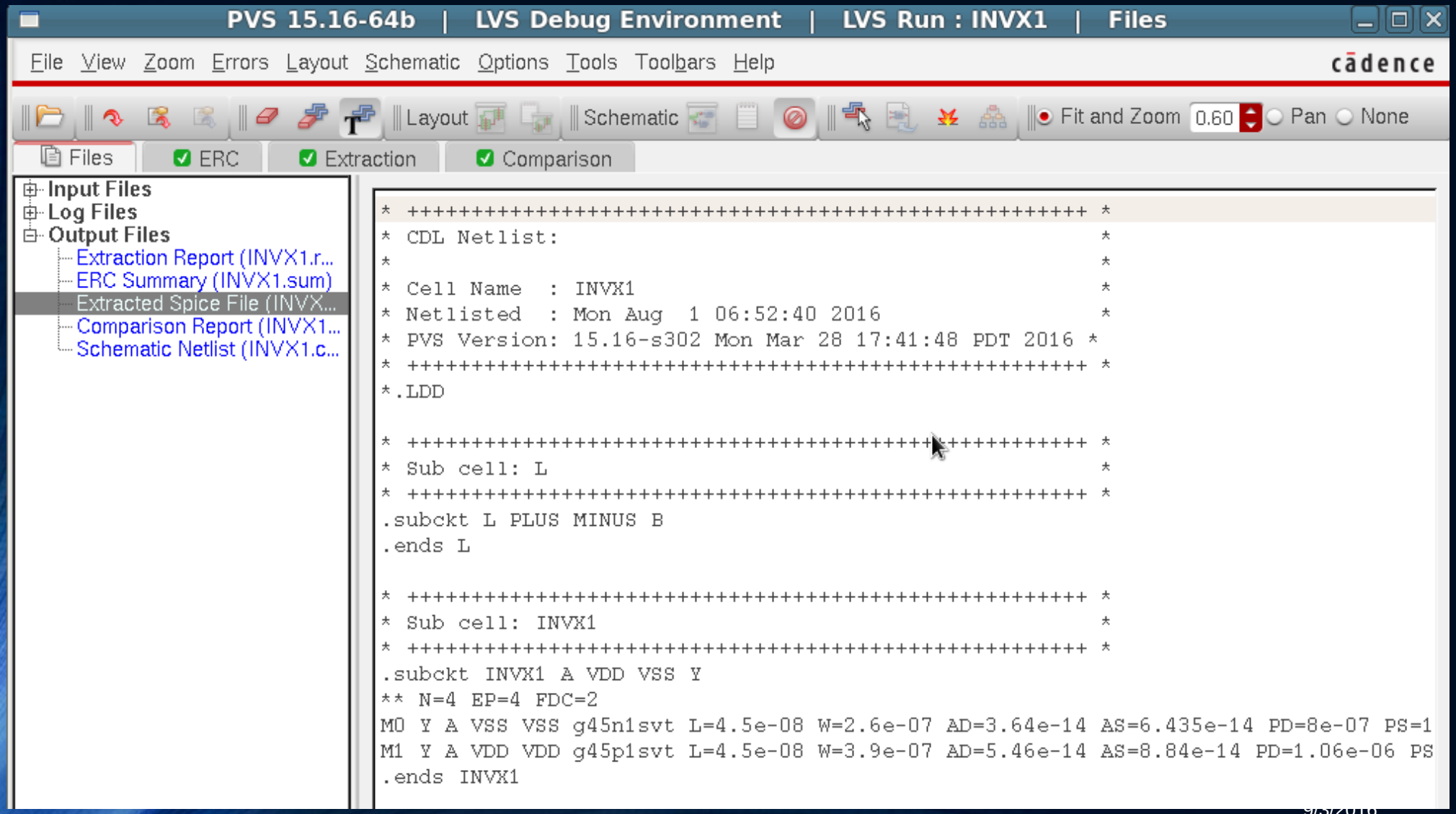


LVS检查结果 — Extraction Report and ERC Summary

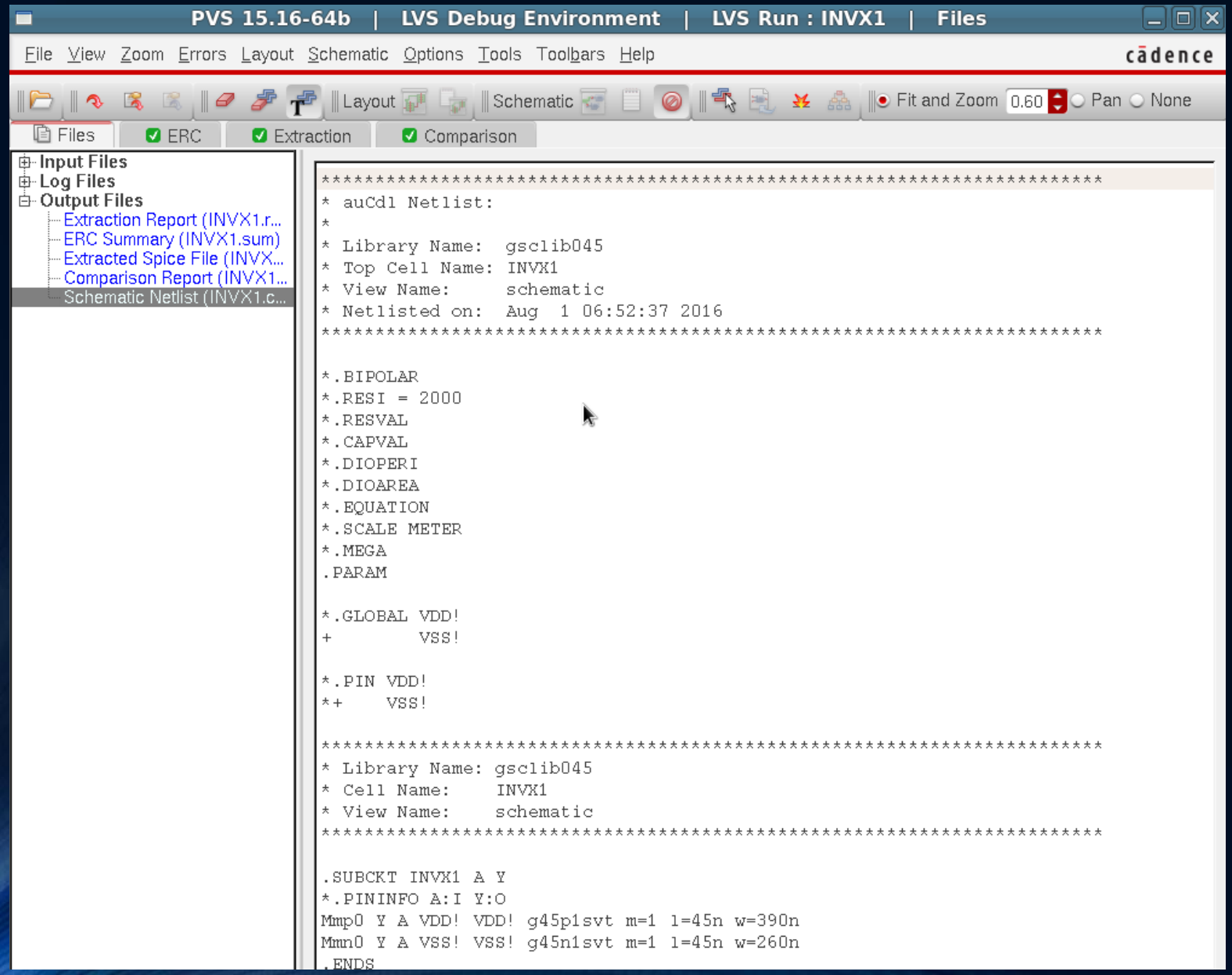




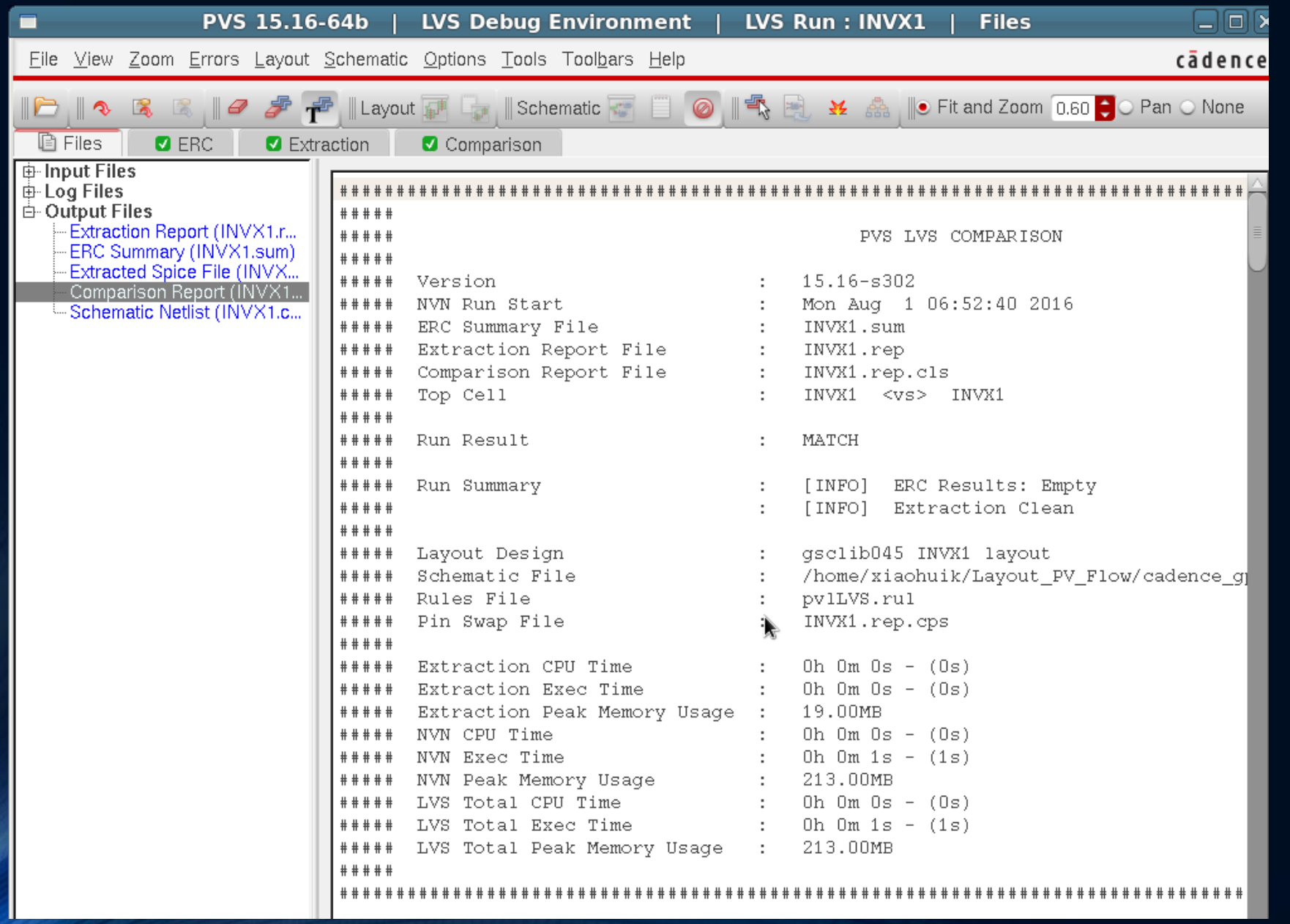
LVS检查结果 — Layout Spice File



LVS检查结果 — Schematic Netlist



LVS检查结果 — Comparison Report



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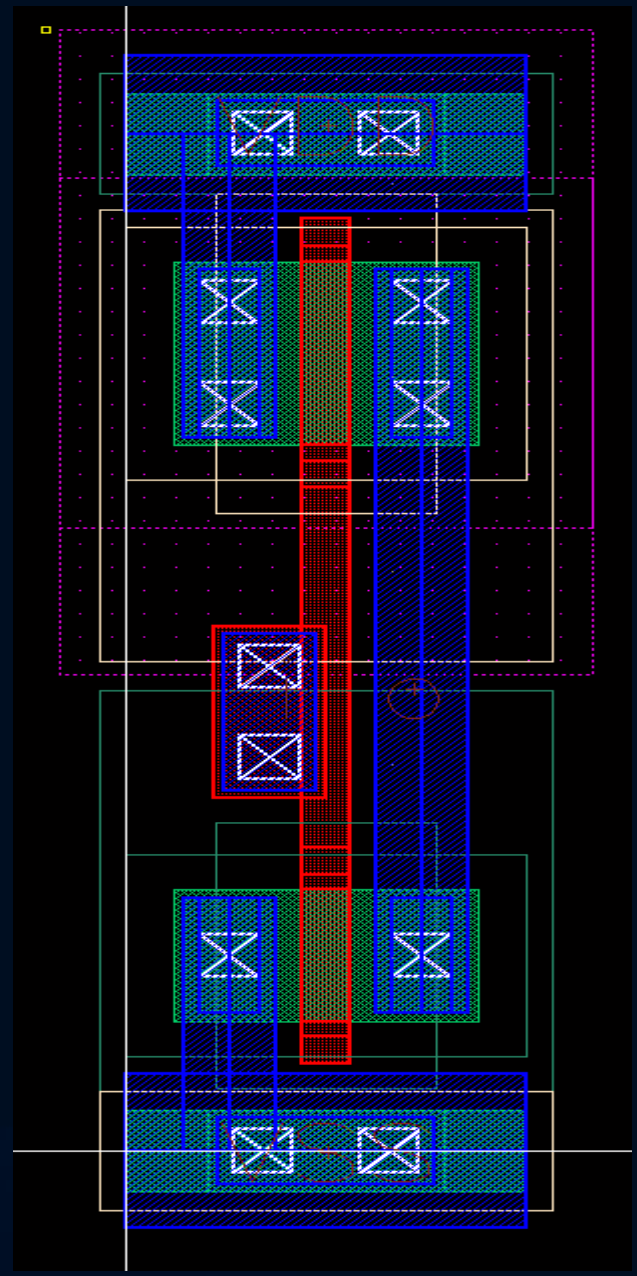
7. 模拟电路高级技能

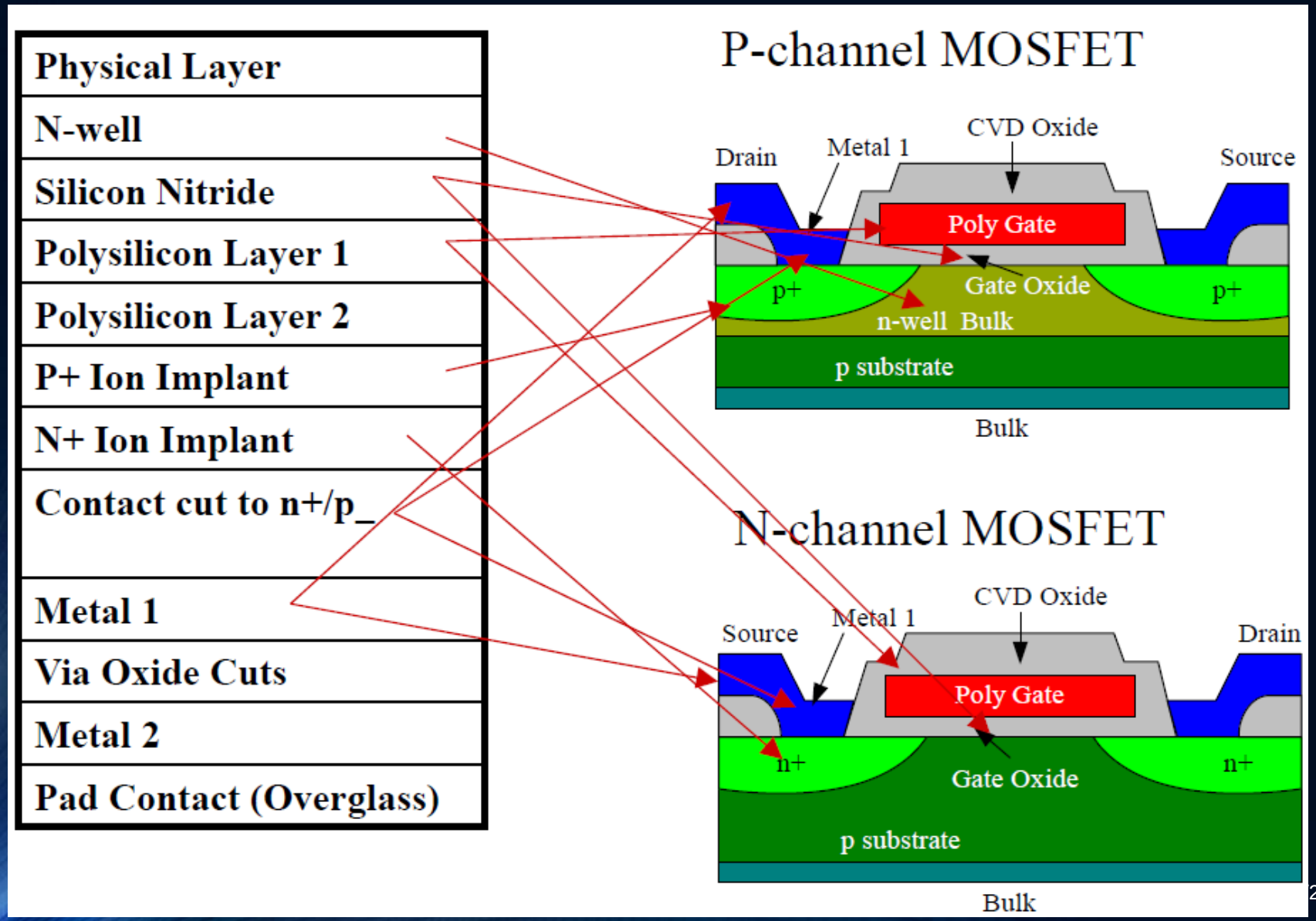
2，CMOS工艺中的层次

了解CMOS工艺中的层次，理解各个层次在版图应用中的图形，颜色，功能和规则。

Nwell/Pwell
Active/Diffusion
Nplus/Pplus
Poly/Gate
Contact
Metal
Via



CMOS 工艺层和版图对应关系



CMOS 工艺层和Techfile文件

```
techLayers(
;( LayerName                Layer#      Abbreviation )
;( ---------                ------      ------------ )
;User-Defined Layers:
 ( OVERLAP                  0           OVERLAP      )
 ( Oxide                    2           Oxide        )
 ( Oxide_thk                4           Oxide_thk    )
 ( Nwell                    6           Nwell        )
 ( Poly                     10          Poly         )
 ( Nhvt                     11          Nhvt         )
 ( Nimp                     12          Nimp         )
 ( Phvt                     13          Phvt         )
 ( Pimp                     14          Pimp         )
 ( Nzvt                     15          Nzvt         )
 ( SiProt                   16          SiProt       )
 ( Nburied                  18          Nburied      )
 ( Cont                     20          Cont         )
 ( SNA                      24          SNA          )
 ( Nlvt                     26          Nlvt         )
 ( Plvt                     27          Plvt         )
 ( Metal1                   30          Metal1       )
 ( Via1                     32          Via1         )
 ( Metal2                   34          Metal2       )
 ( Via2                     36          Via2         )
 ( Metal3                   38          Metal3       )
 ( Via3                     40          Via3         )
 ( Metal4                   42          Metal4       )
 ( Via4                     44          Via4         )
 ( Metal5                   46          Metal5       )
 ( Via5                     48          Via5         )
 ( Metal6                   50          Metal6       )
 ( Via6                     52          Via6         )
 ( Metal7                   54          Metal7       )
 ( Via7                     56          Via7         )
 ( Metal8                   58          Metal8       )
 ( Via8                     60          Via8         )
 ( Metal9                   62          Metal9       )
 ( Via9                     64          Via9         )
 ( Metal10                  66          Metal10      )
 ( Via10                    68          Via10        )
```

```
techLayerPurposePriorities(
;layers are ordered from lowest to highest priority
;( LayerName                Purpose     )
;( ---------                -------     )
 ( OVERLAP                  drawing     )
 ( OVERLAP                  label       )
 ( OVERLAP                  boundary    )
 ( Nwell                    drawing     )
 ( Nwell                    pin         )
 ( Nwell                    boundary    )
 ( Oxide                    drawing     )
 ( Oxide_thk                drawing     )
 ( Poly                     drawing     )
 ( Poly                     track       )
 ( Pimp                     drawing     )
 ( Nhvt                     drawing     )
 ( Nlvt                     drawing     )
 ( Nimp                     drawing     )
 ( Phvt                     drawing     )
 ( Plvt                     drawing     )
 ( Nzvt                     drawing     )
 ( SiProt                   drawing     )
 ( Cont                     drawing     )
 ( Cont                     grid        )
 ( Cont                     blockage    )
 ( Metal1                   drawing     )
 ( Metal1                   grid        )
 ( Metal1                   track       )
 ( Metal1                   blockage    )
 ( Via1                     drawing     )
 ( Via1                     grid        )
 ( Via1                     blockage    )
 ( Metal2                   drawing     )
 ( Metal2                   grid        )
 ( Metal2                   track       )
 ( Metal2                   blockage    )
 ( Via2                     drawing     )
 ( Via2                     grid        )
 ( Via2                     blockage    )
 ( Metal3                   drawing     )
 ( Metal3                   grid        )
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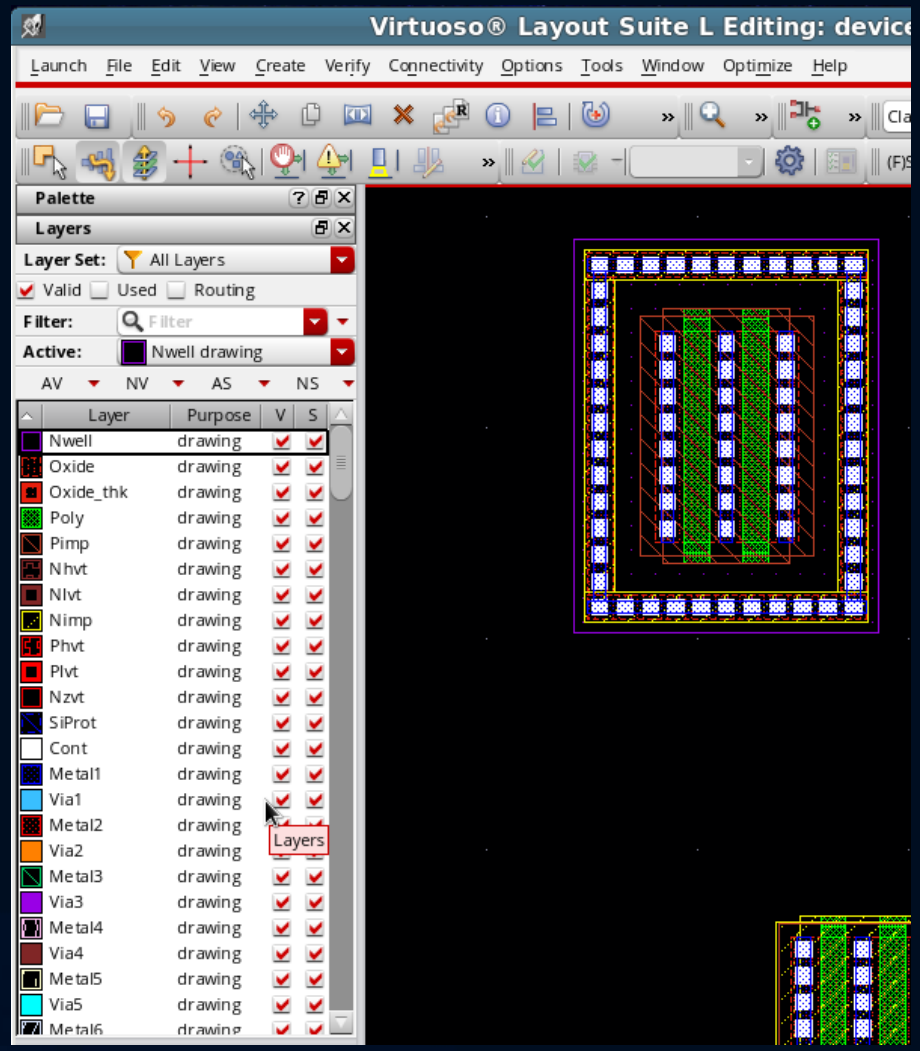
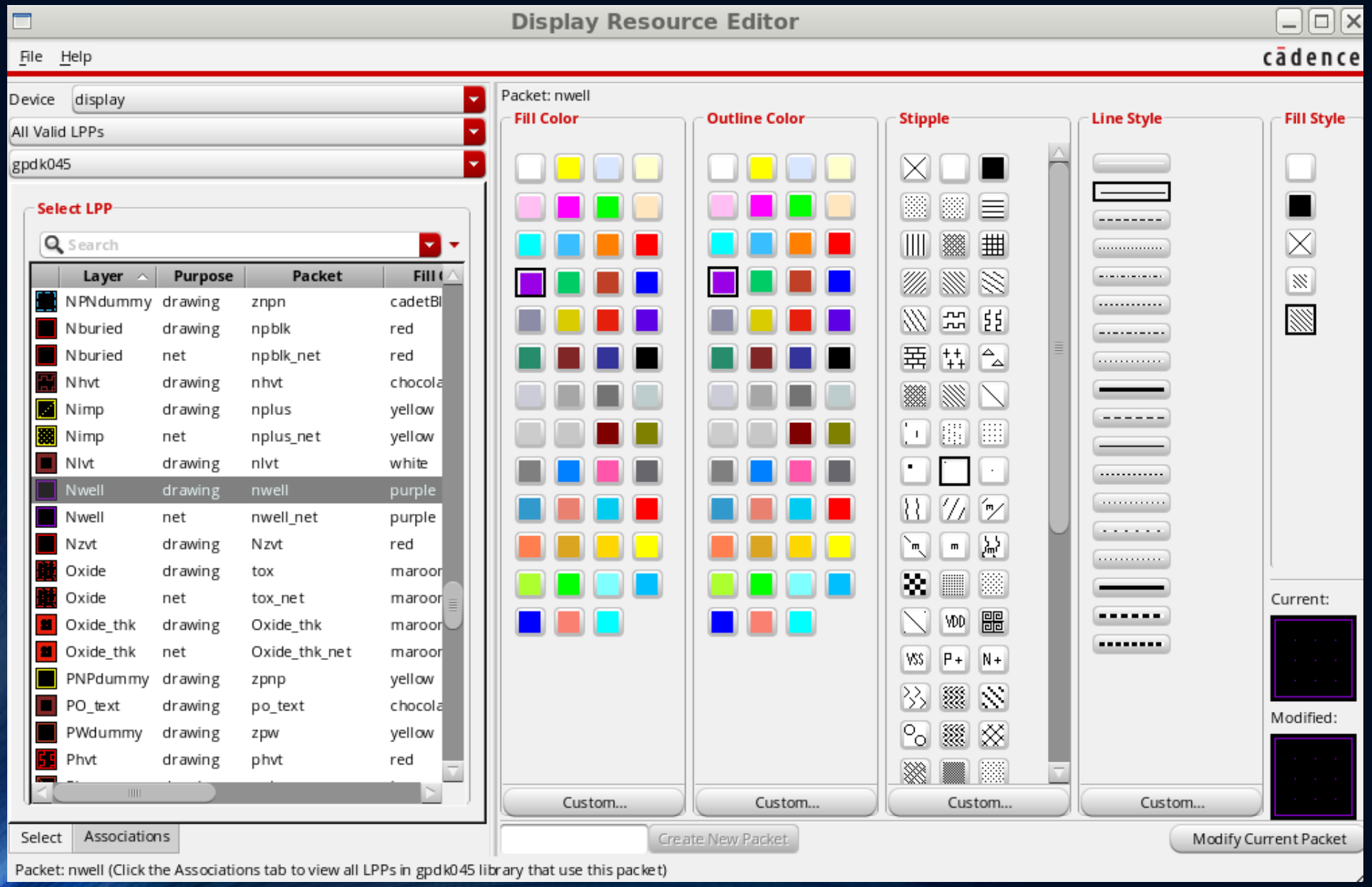


工艺层显示文件及设置


Display Resource Editor
File
Help
cadence
Device
display
All Valid LPPs
gpdk045
Select LPP
Search
Layer
Purpose
Packet
Fill
NPNdummy drawing znpn cadetBl
Nburied drawing npblk red
Nburied net npblk_net red
Nhvt drawing nhvt chocola
Nimp drawing nplus yellow
Nimp net nplus_net yellow
Nlvt drawing nlvt white
Nwell drawing nwell purple
Nwell net nwell_net purple
Nzvt drawing Nzvt red
Oxide drawing tox maroon
Oxide net tox_net maroon
Oxide_thk drawing Oxide_thk maroon
Oxide_thk net Oxide_thk_net maroon
PNPdummy drawing zpnp yellow
PO_text drawing po_text chocola
PWdummy drawing zpw yellow
Phvt drawing phvt red
Select
Associations
Packet: nwell
Fill Color
Outline Color
Stipple
Line Style
Fill Style
Custom...
Custom...
Custom...
Custom...
Current:
Modified:
Create New Packet
Modify Current Packet
Packet: nwell (Click the Associations tab to view all LPPs in gpdk045 library that use this packet)

课程内容

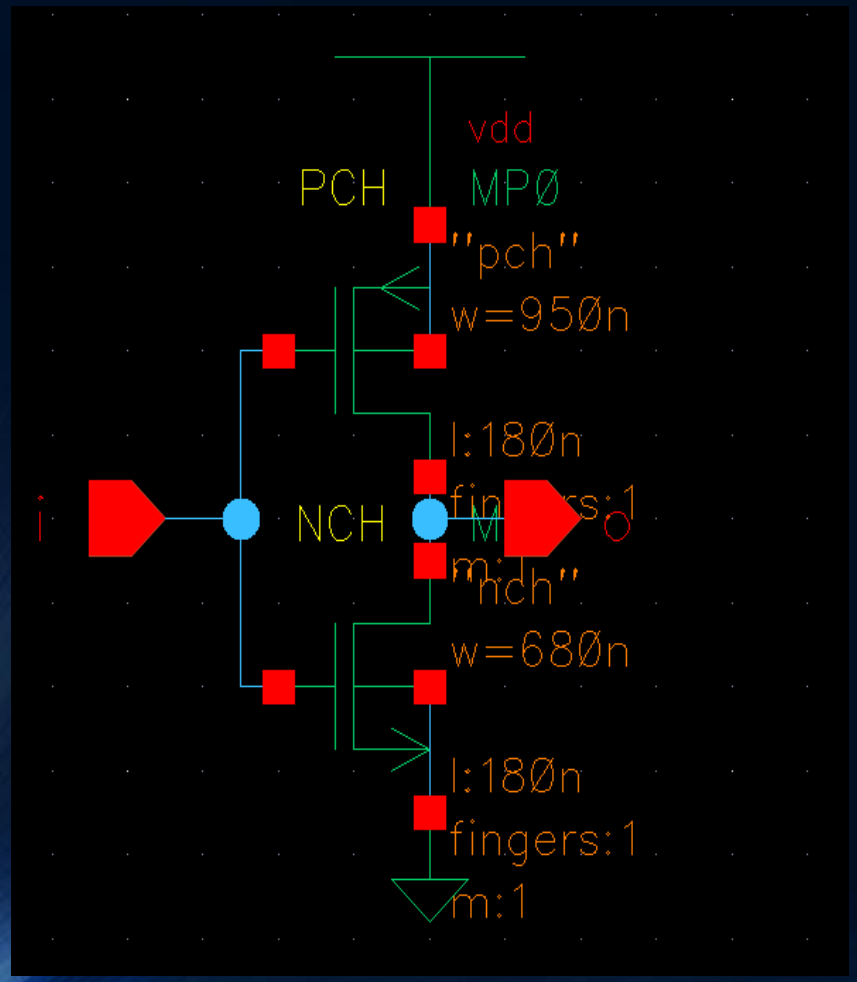
1. DEA软件使用 — 版图编辑和物理验证工具
2. CMOS工艺中的层次
3. 基本器件和单元的版图结构
4. Stdcell 标准单元
5. 数字电路
6. 模拟电路
7. 模拟电路高级技能

3，基本器件和单元的版图结构

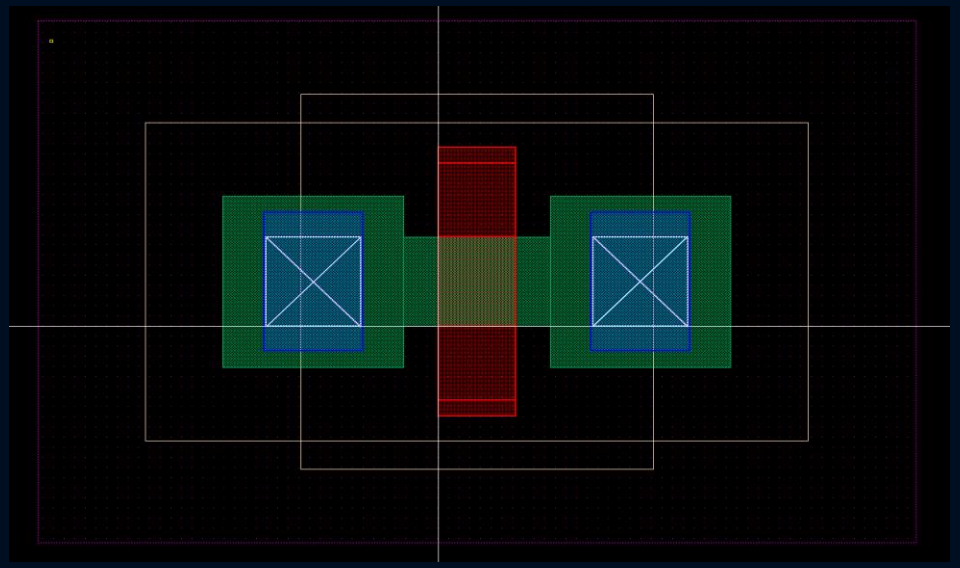
学习CMOS工艺中的器件和单元的版图结构，
在以后的版图编辑中熟练运用各个基本器件。

MOSFET
Diode
Bipolar
Resistor
Capacitor
Ind
PAD
Sub/Guardring

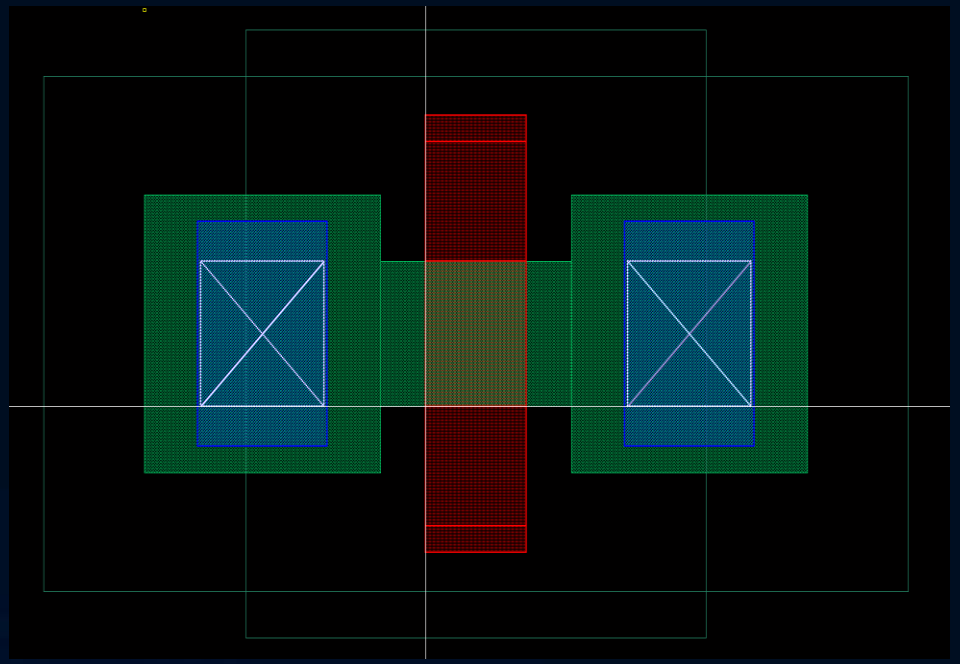
3.1 Mosfet



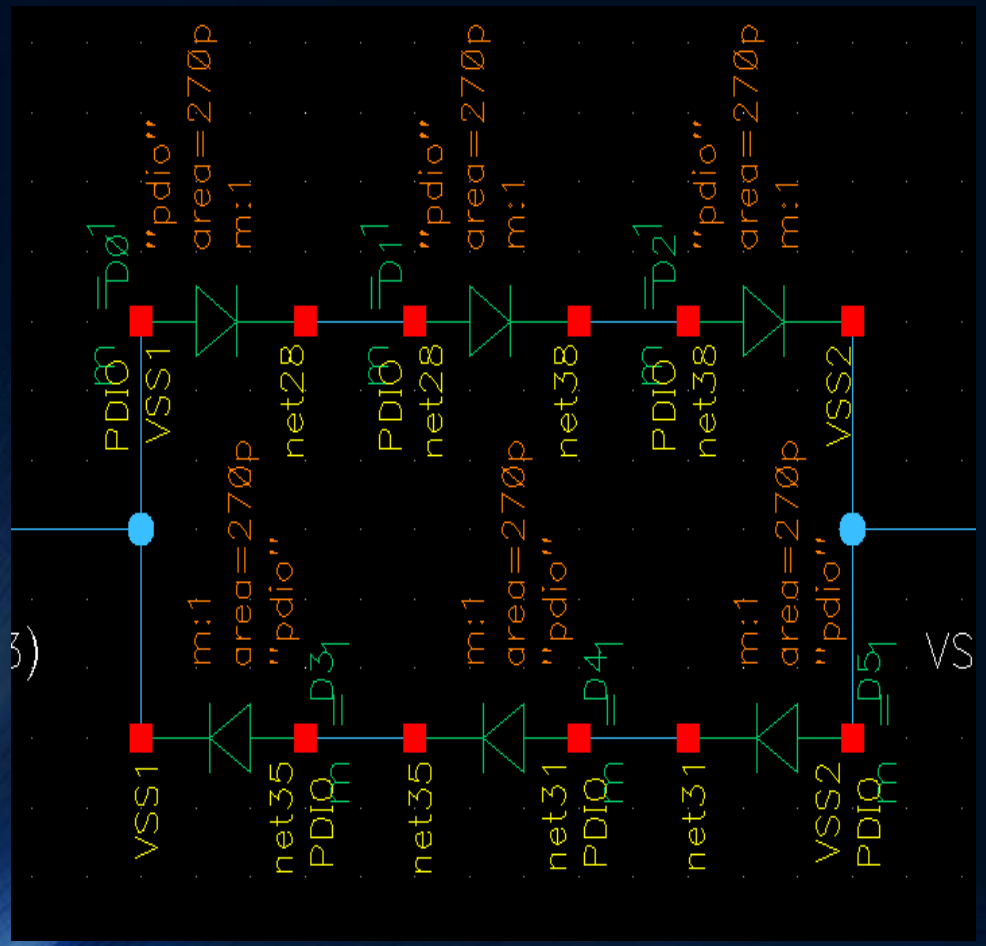
Pmosfet

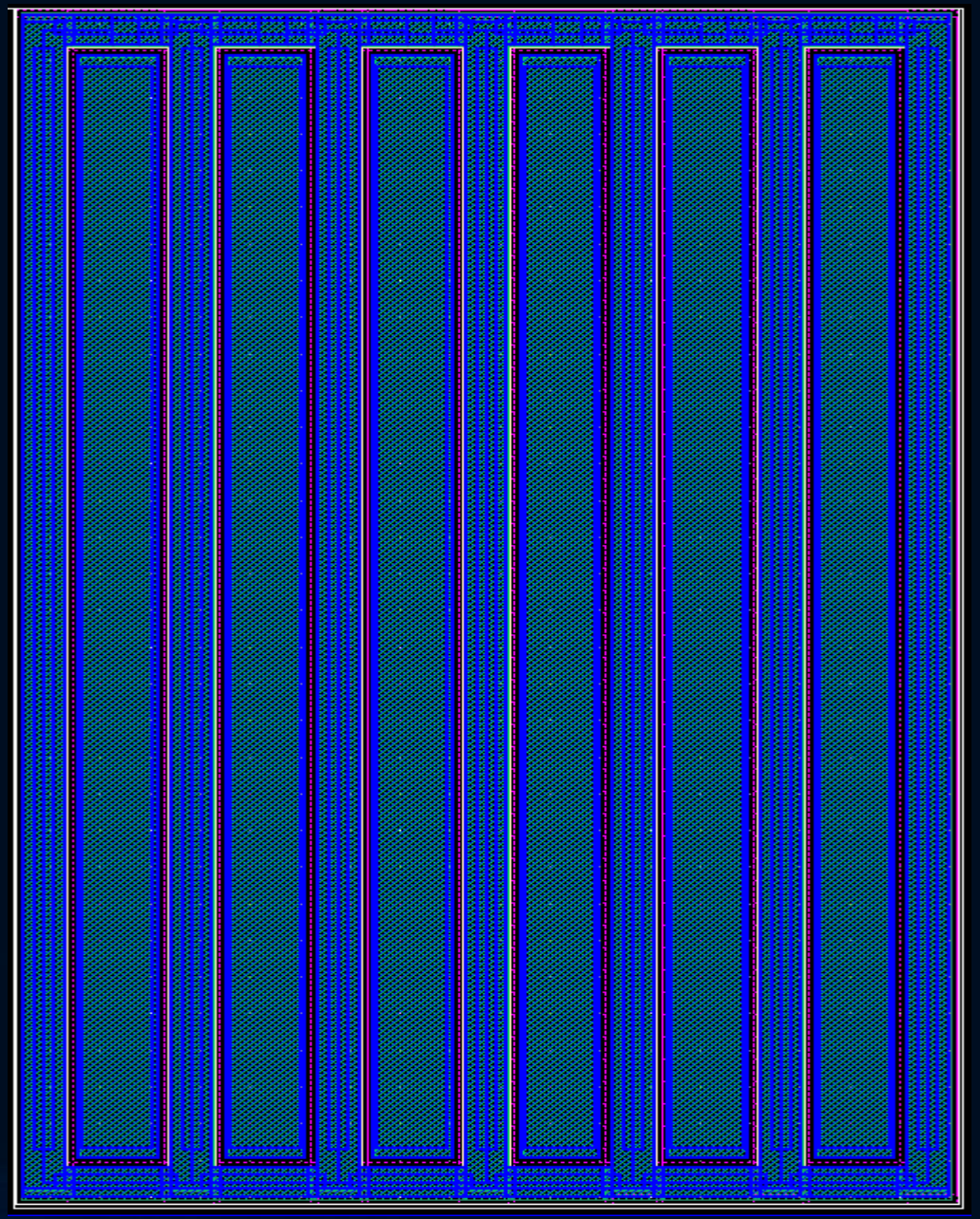


nmosfet

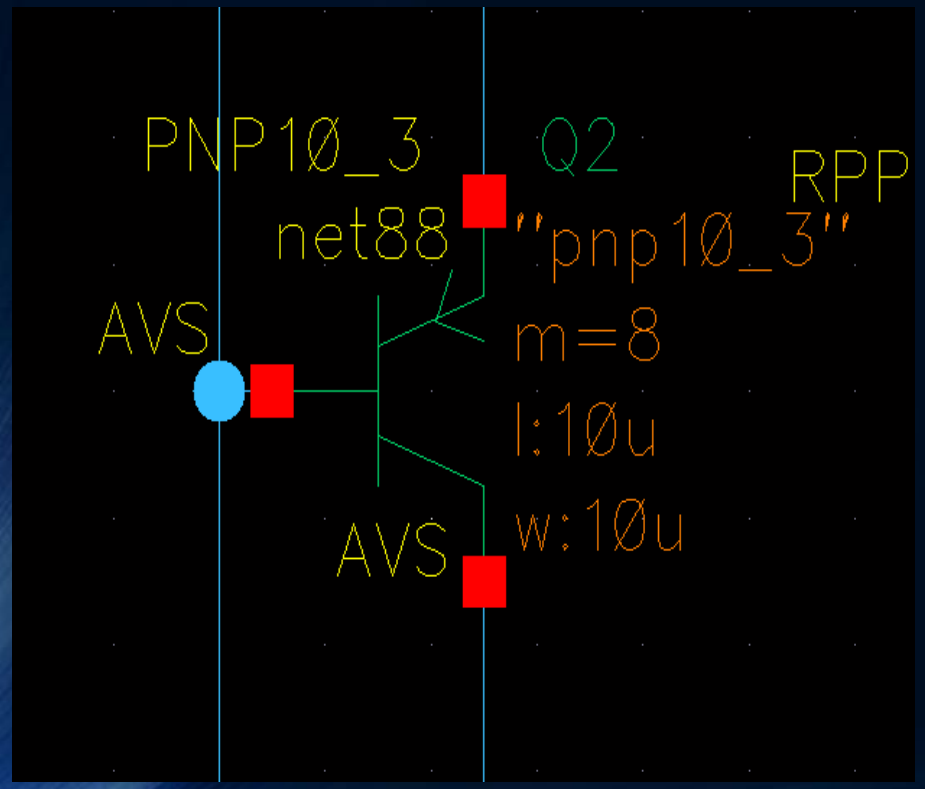


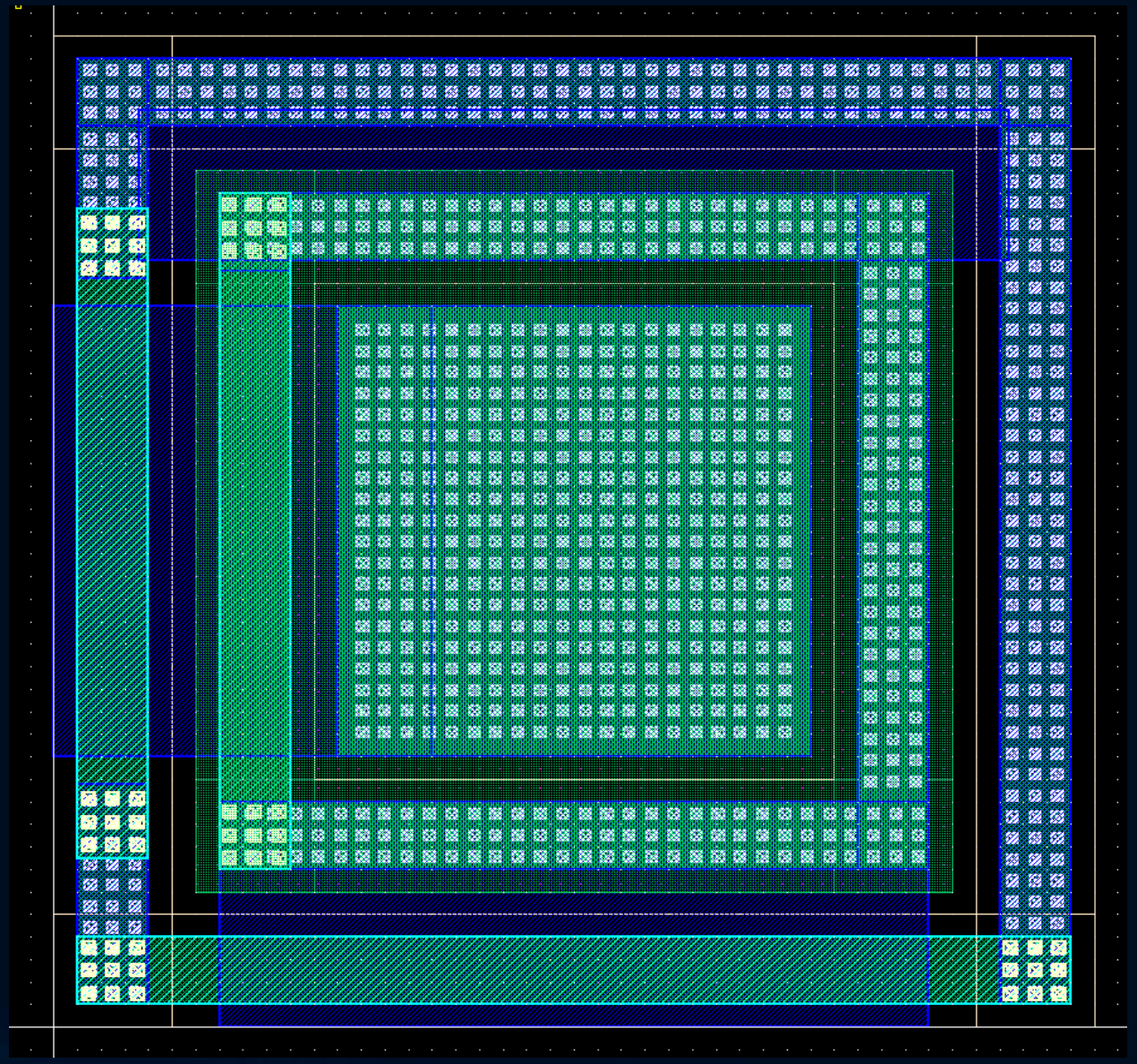
3.2 Diode二极管


D0
"pdio"
area=270p
m:1
D1
D2
PDIO
VSS1
net28
net38
VSS2
D3
D4
D5
net35
net31
3)
VS



3.3 Bipolar三极管



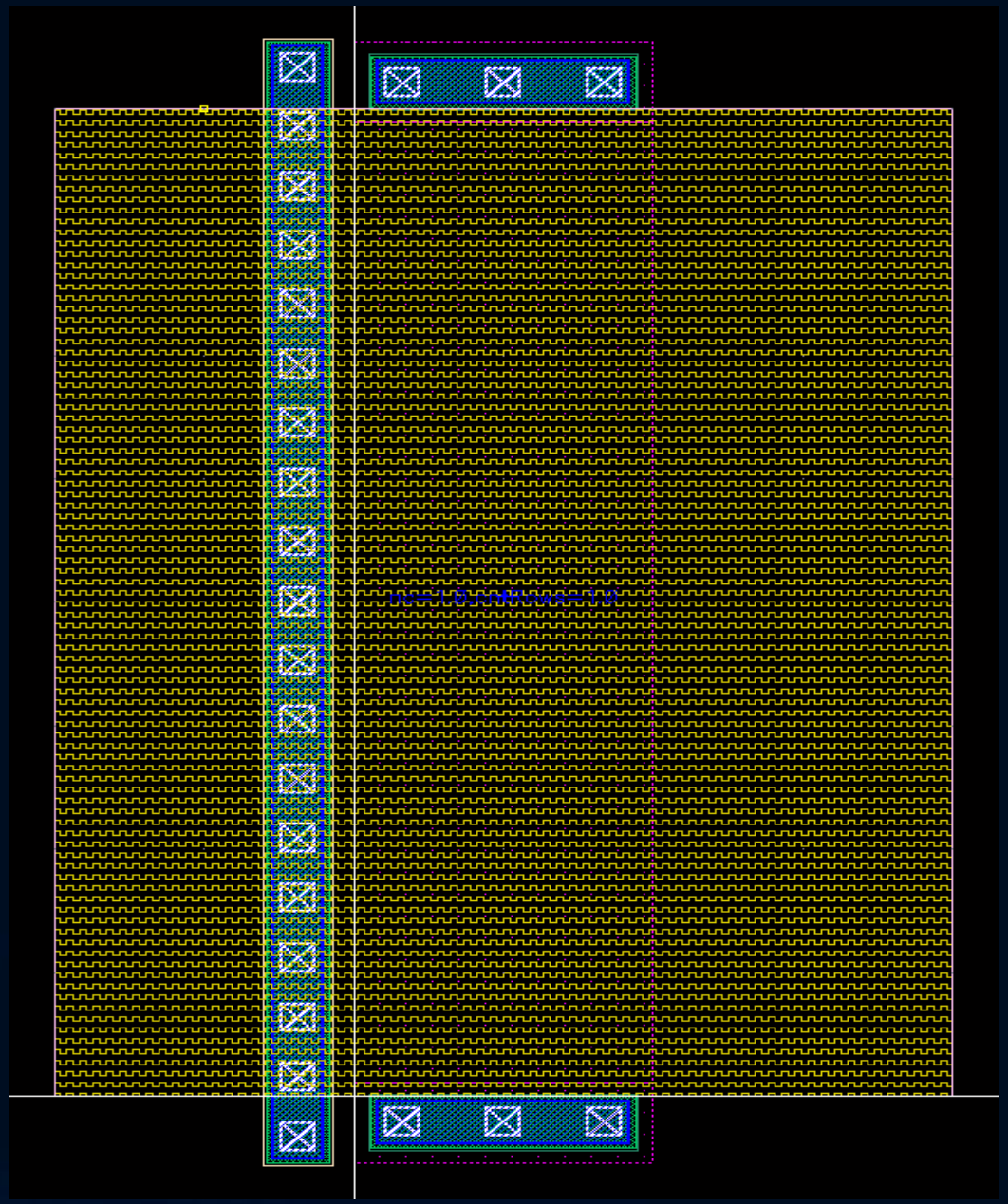


3.4 Resistor电阻

Poly Resistor

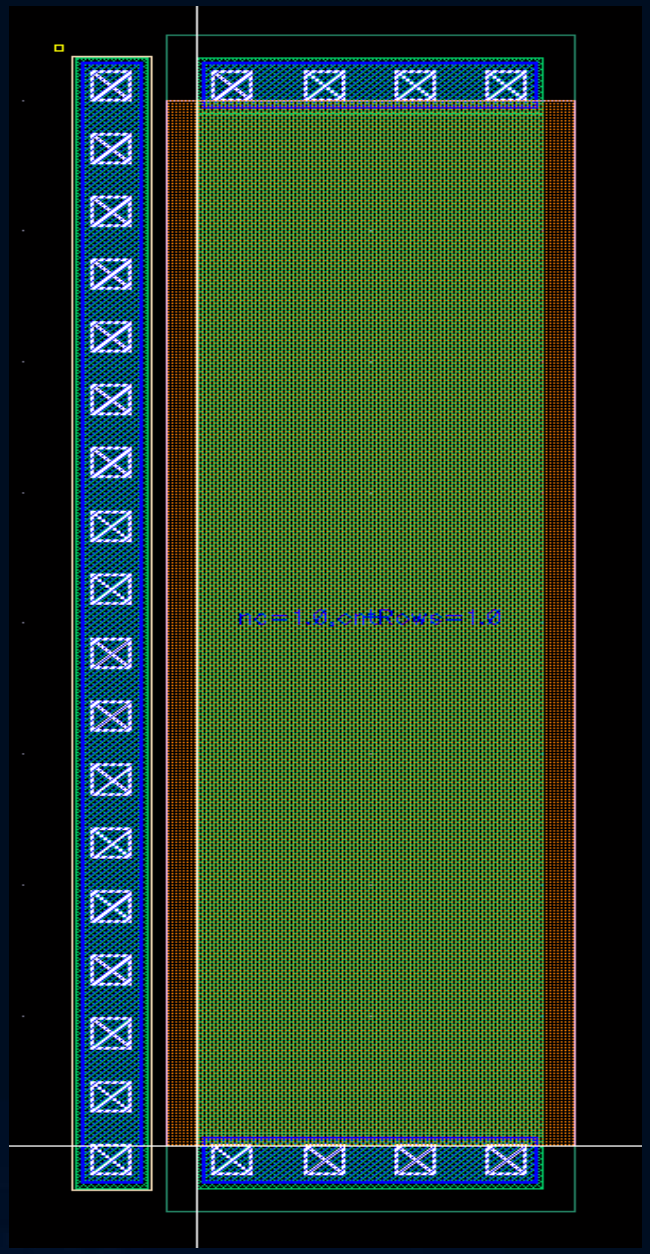
3.4 Resistor电阻

Nwell Resistor



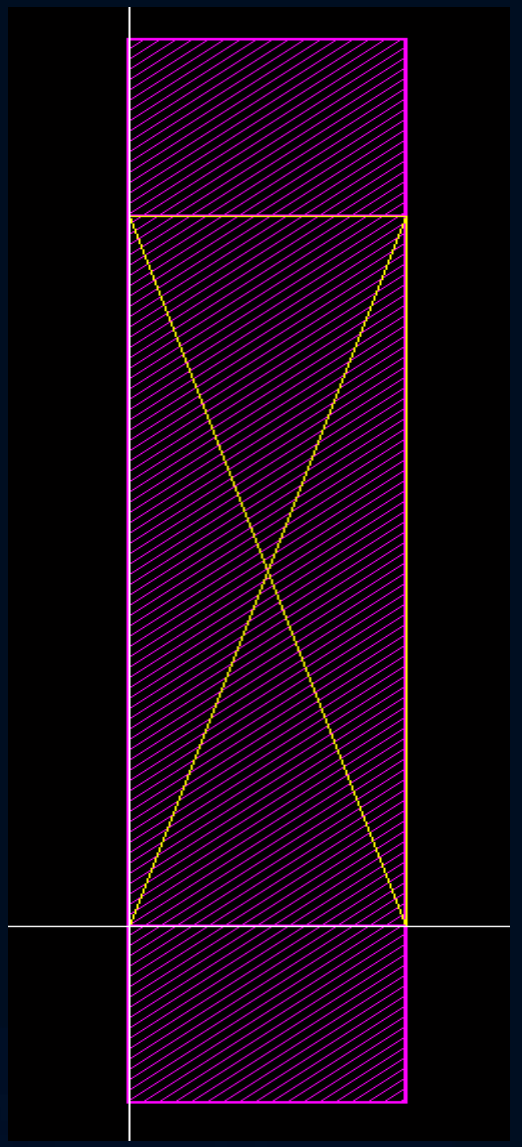
3.4 Resistor电阻

Nplus Resistor



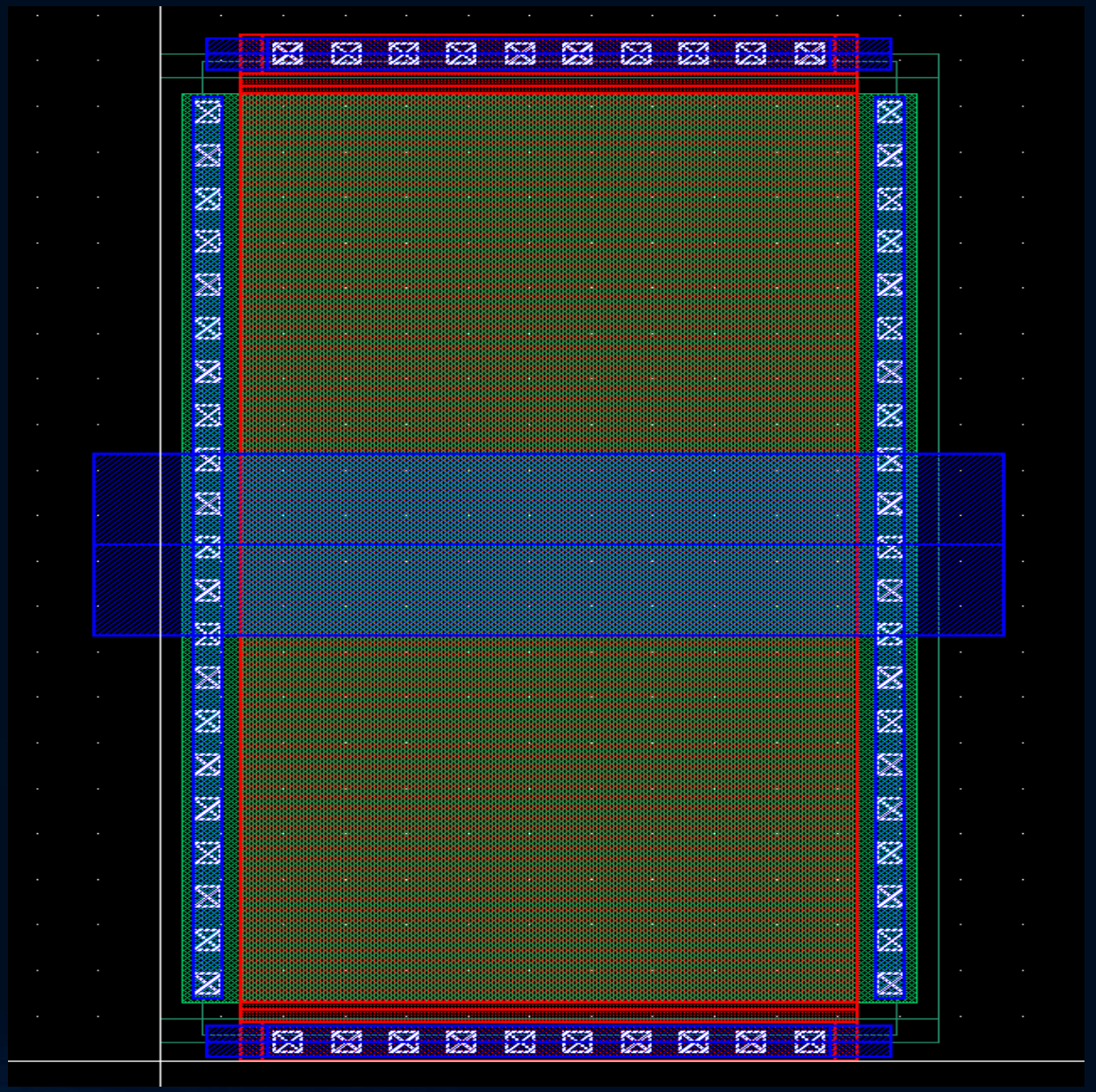
3.4 Resistor电阻

Metal Resistor



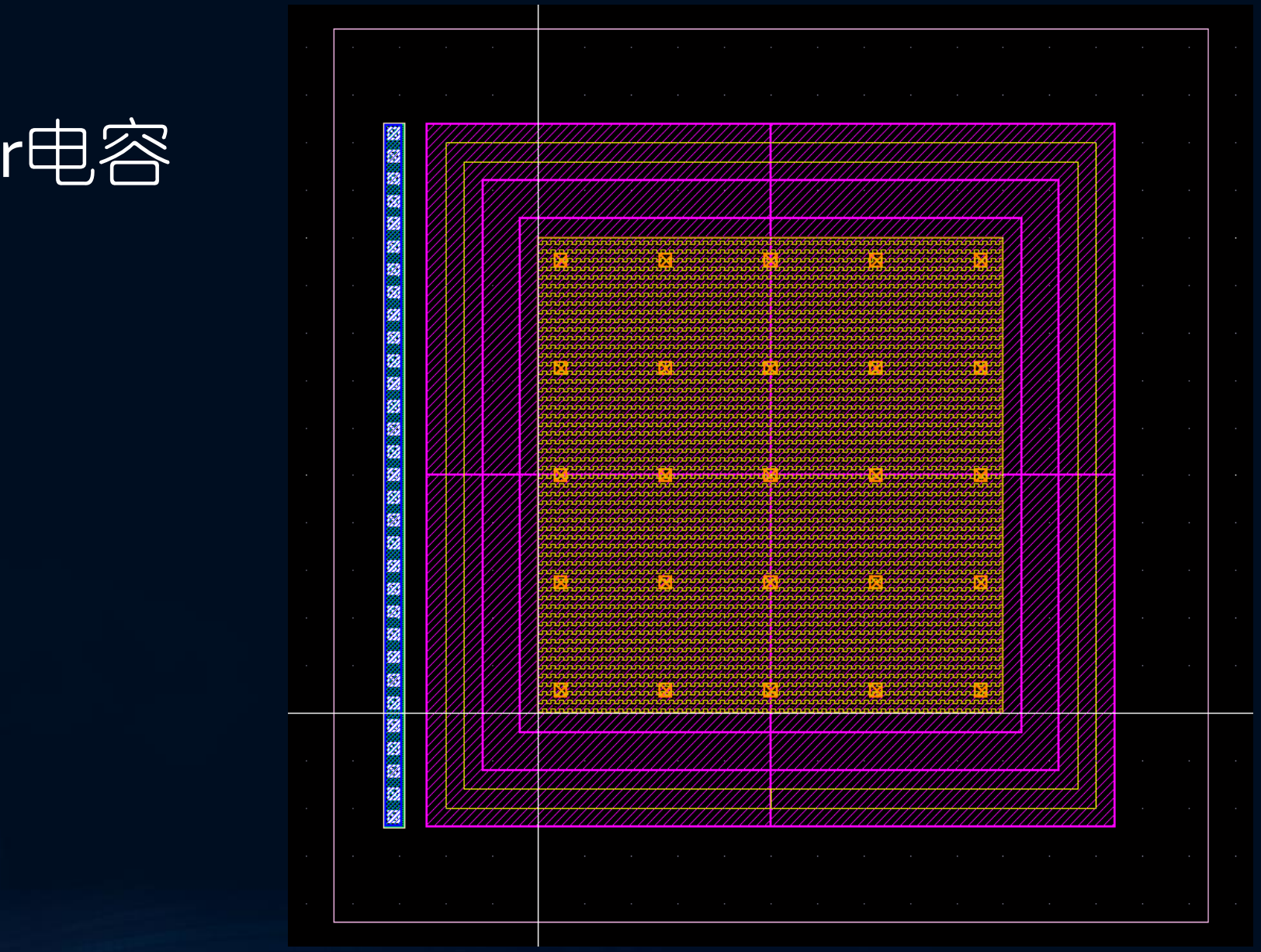
3.5 Capacitor电容

Moscap

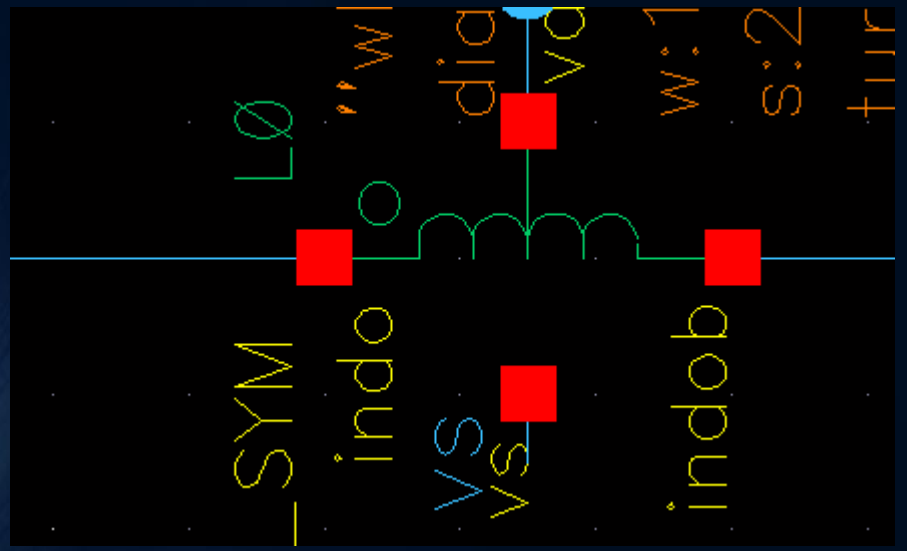


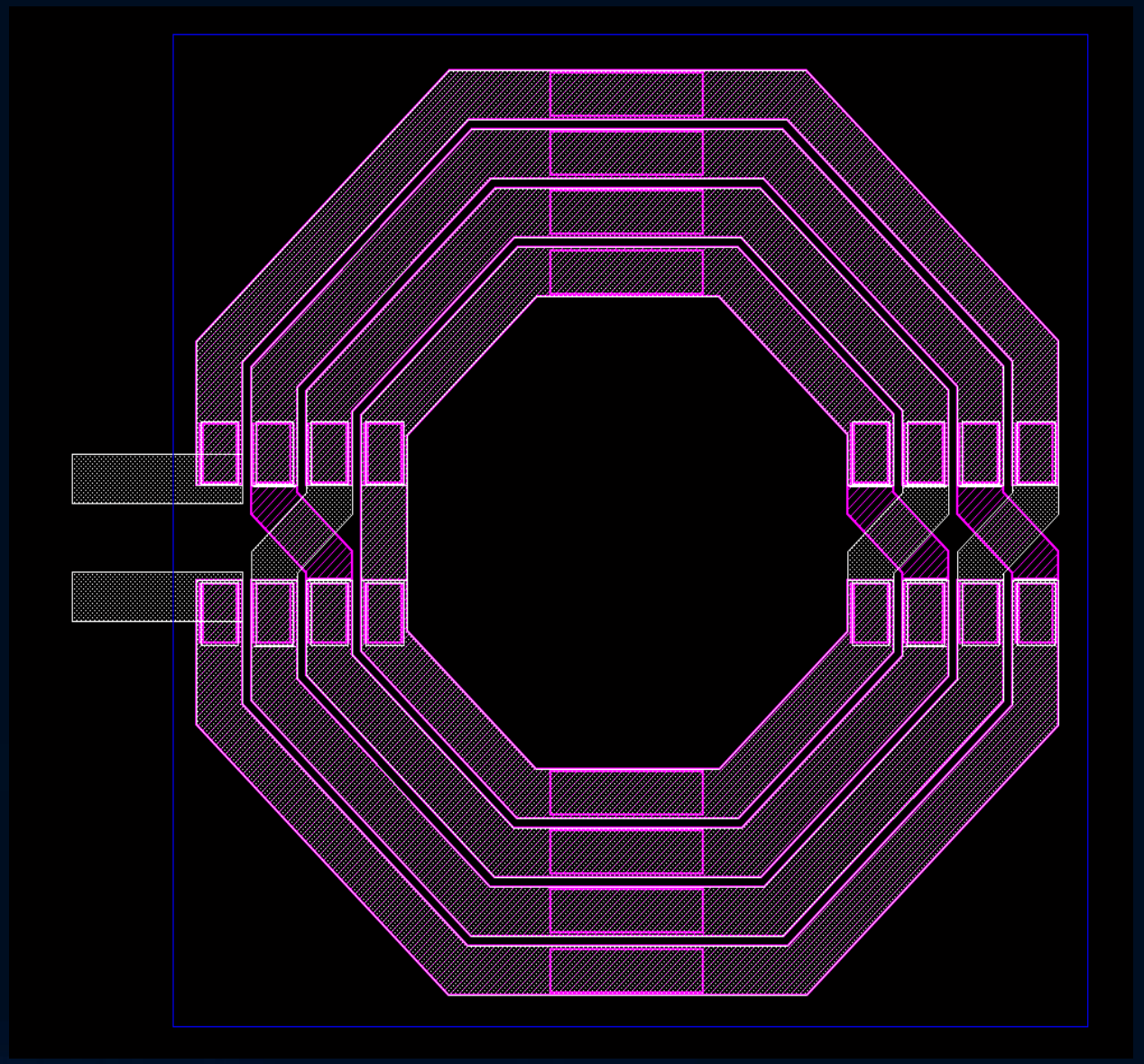
3.5 Capacitor电容

MIMCAP

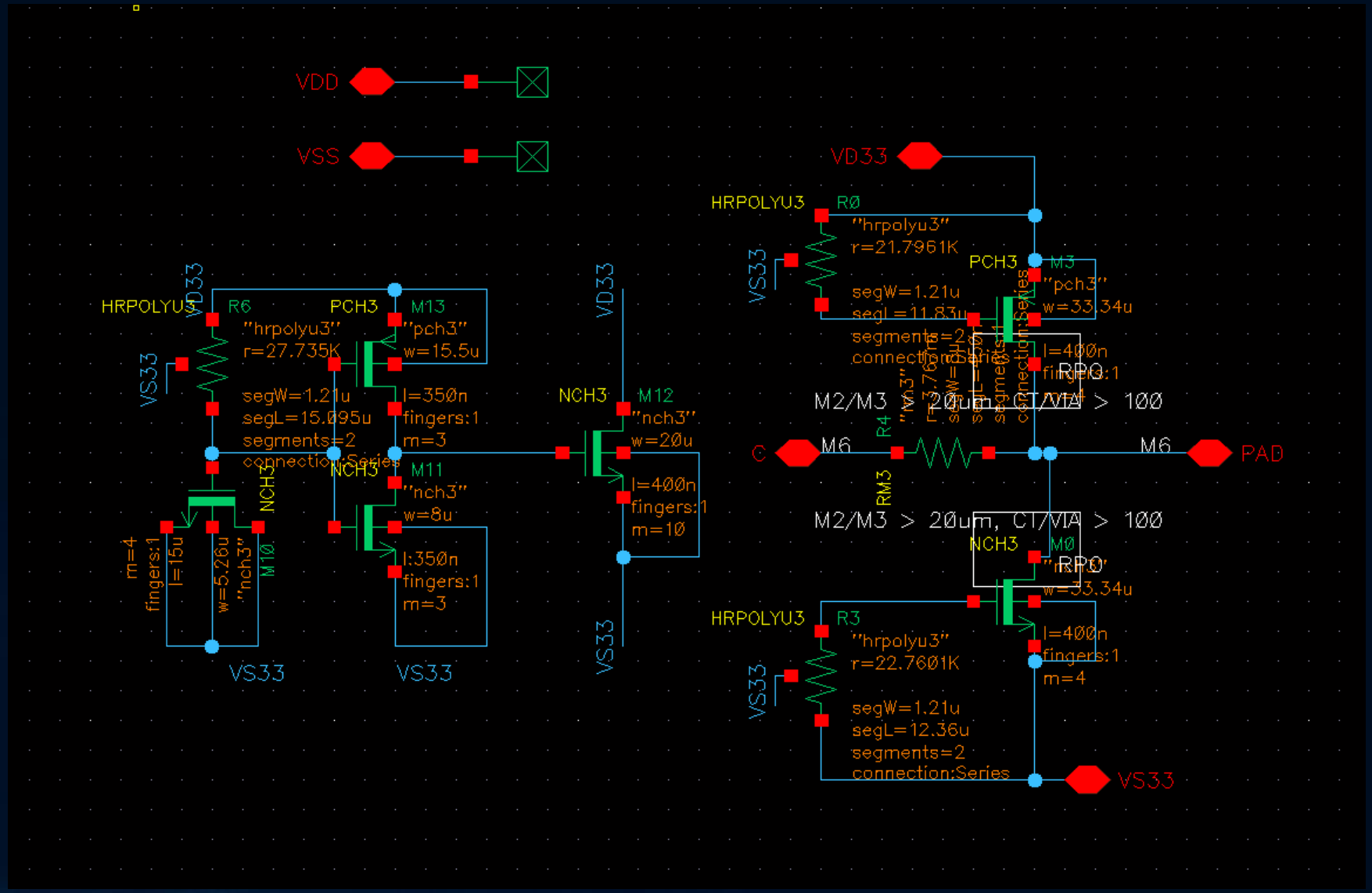


3.6 Ind电感

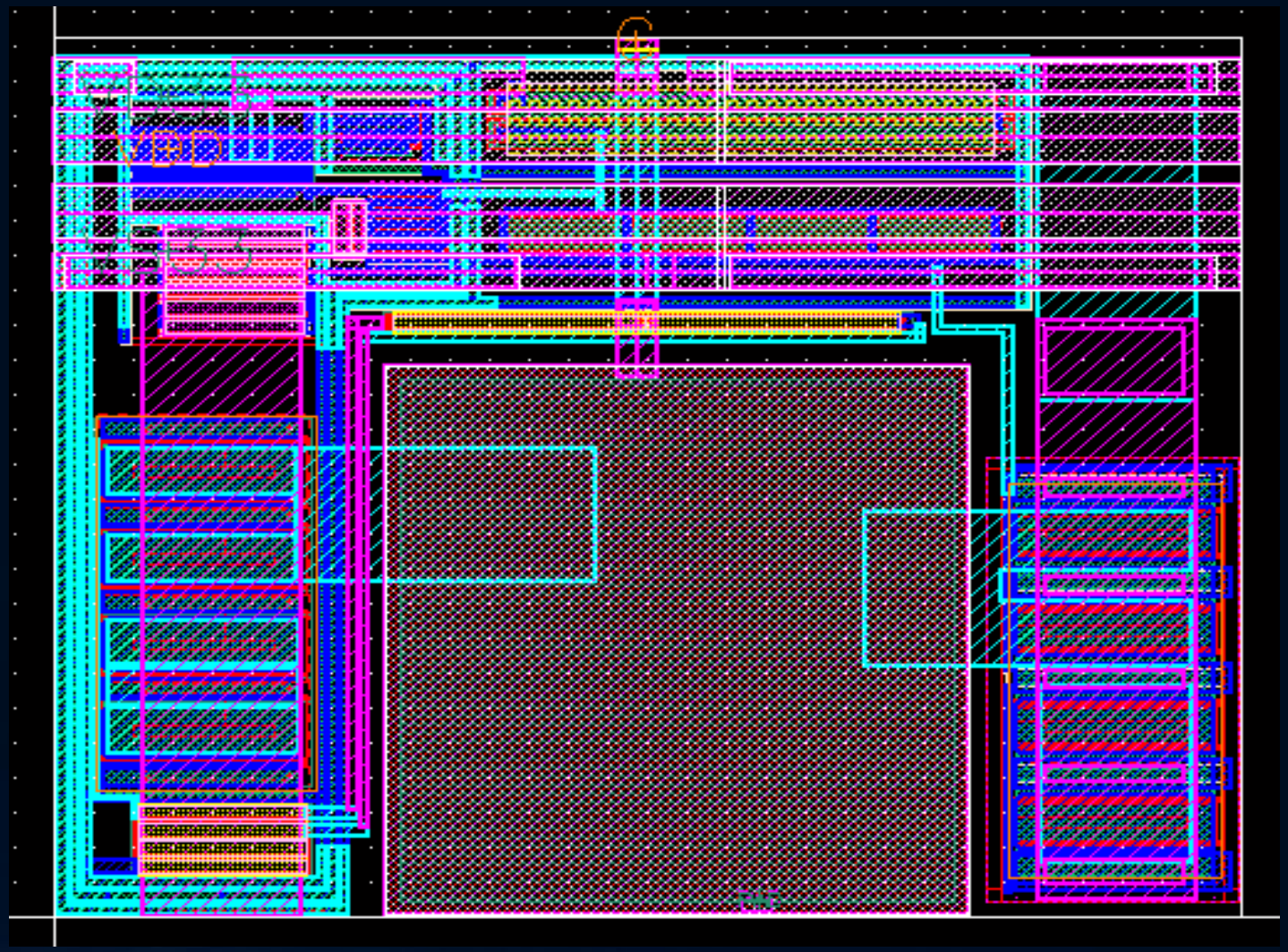




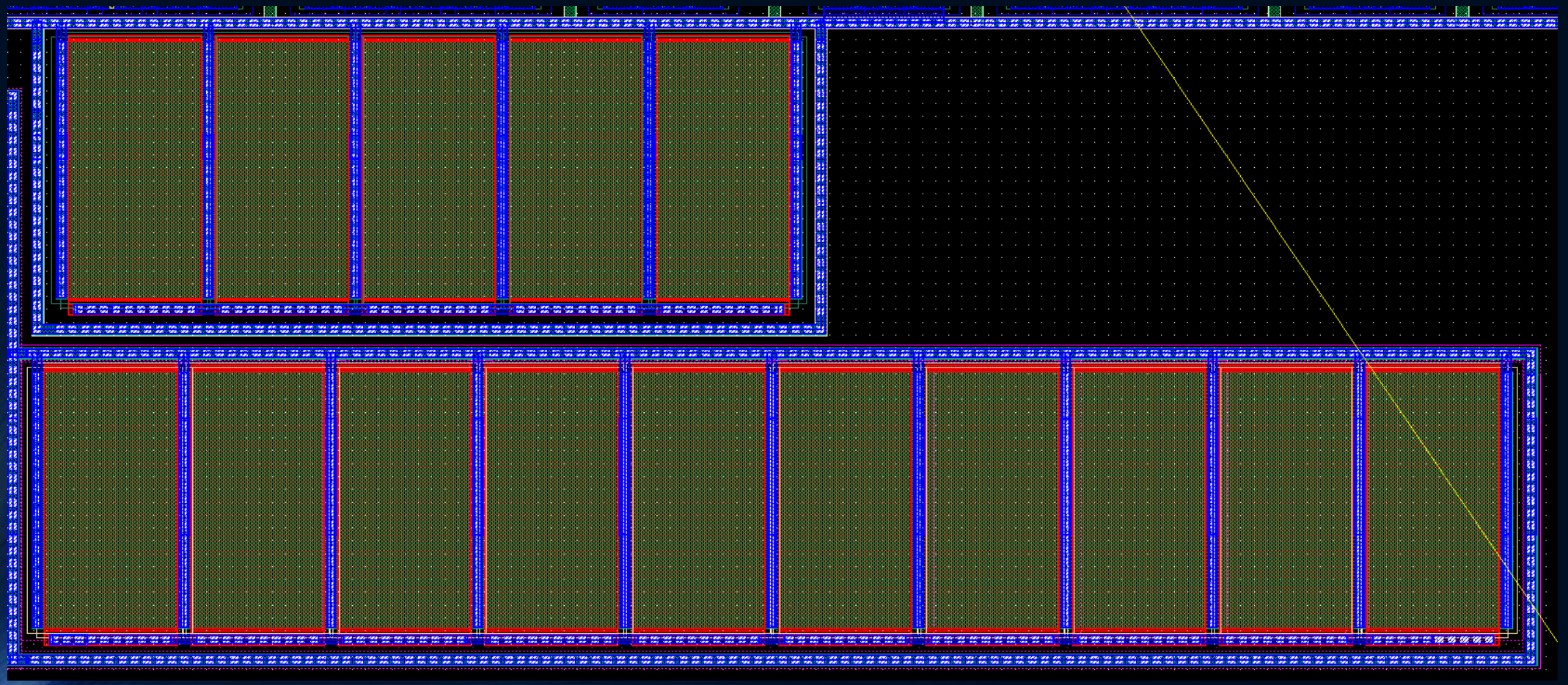
3.7 PAD


VDD
VSS
VD33
HRPOLYU3
R6
"hrpolyu3"
r=27.735K
segW=1.21u
segL=15.095u
segments=2
connection:Series
VS33
PCH3
M13
"pch3"
w=15.5u
l=350n
fingers:1
m=3
NCH3
M11
"nch3"
w=8u
l:350n
fingers:1
m=3
M10
"nch3"
w=5.26u
l=15u
m=4
fingers:1
VS33
VS33
VD33
NCH3
M12
"nch3"
w=20u
l=400n
fingers:1
m=10
VS33
VD33
HRPOLYU3
R0
"hrpolyu3"
r=21.7961K
segW=1.21u
segL=11.83u
segments=2
connection:Series
VS33
PCH3
M3
"pch3"
w=33.34u
l=400n
fingers:1
M2/M3 > 20um, CT/VIA > 100
C
M6
M6
PAD
RM3
M2/M3 > 20um, CT/VIA > 100
NCH3
M0
"nch3"
w=33.34u
l=400n
fingers:1
m=4
HRPOLYU3
R3
"hrpolyu3"
r=22.7601K
segW=1.21u
segL=12.36u
segments=2
connection:Series
VS33
VS33

3.7 PAD



3.8 psub, nsub, guardring



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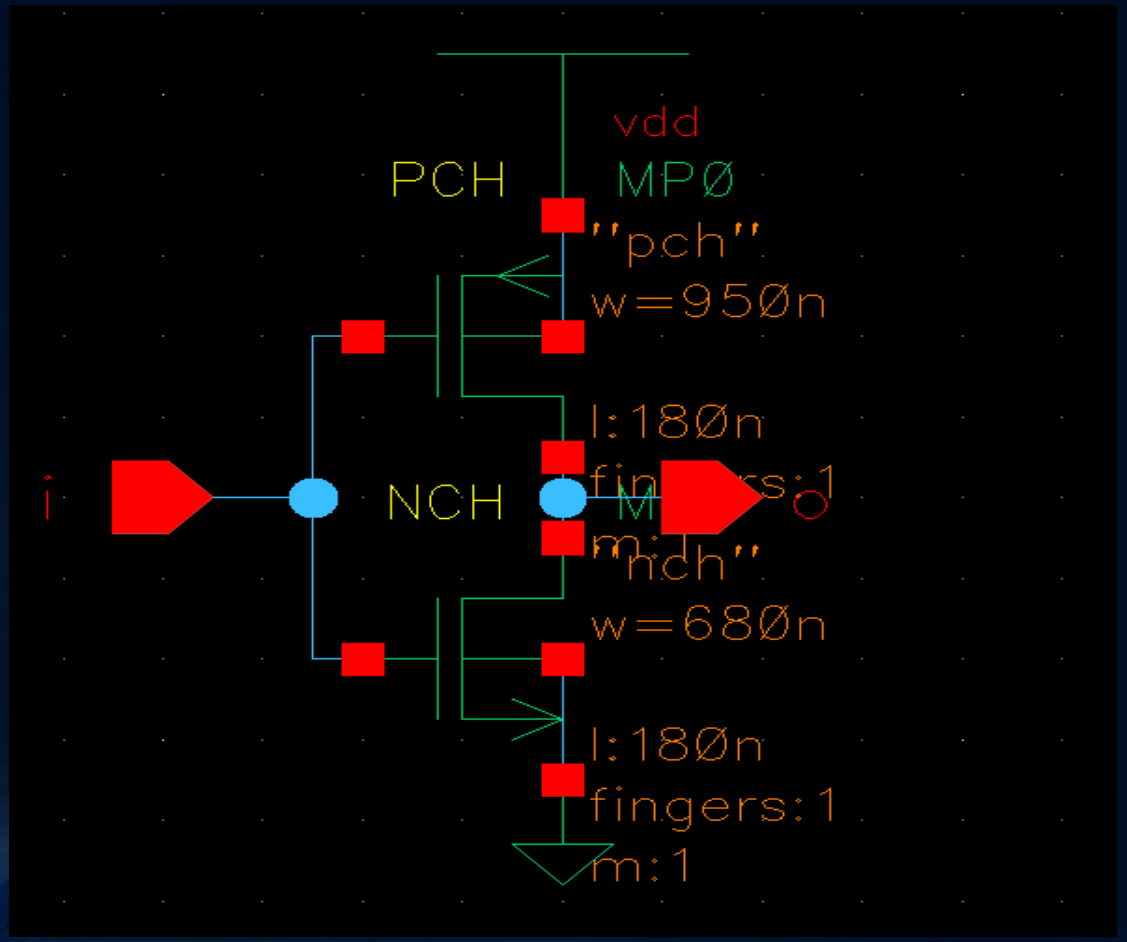
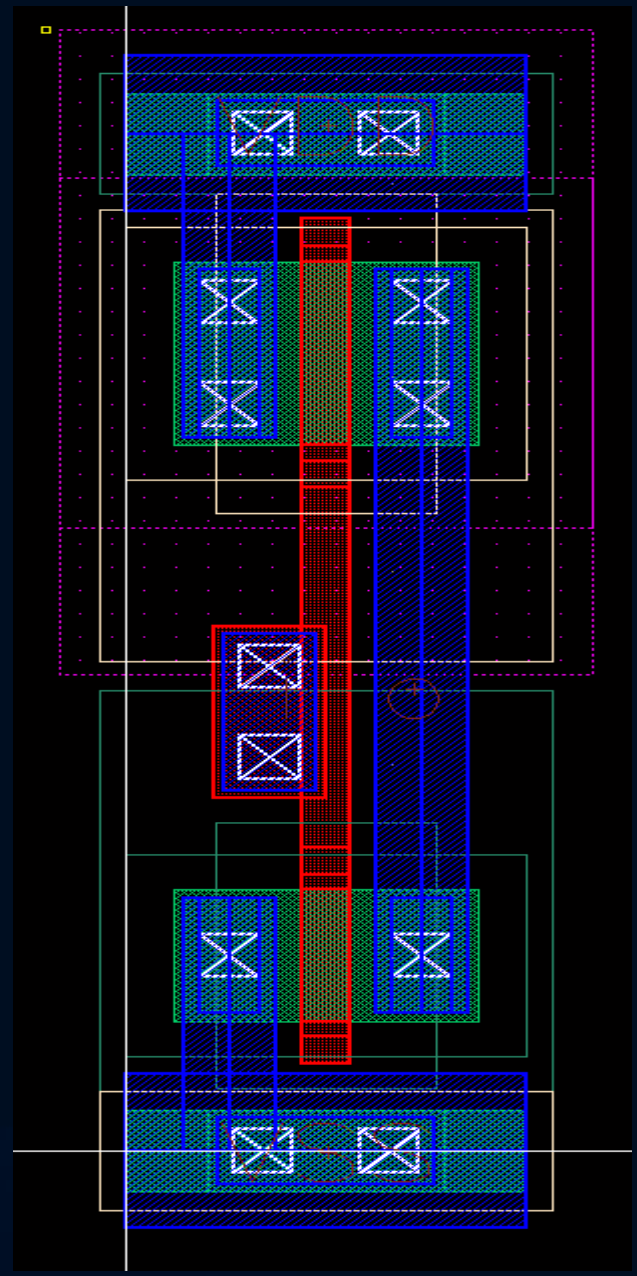
4，Stdcell 标准单元

学习CMOS stdcell标准单元，熟悉各个单元的schmatic和layout结构，学习版图的画法。

Invertor
NAND
NOR
AND
OR
Latch
DFF

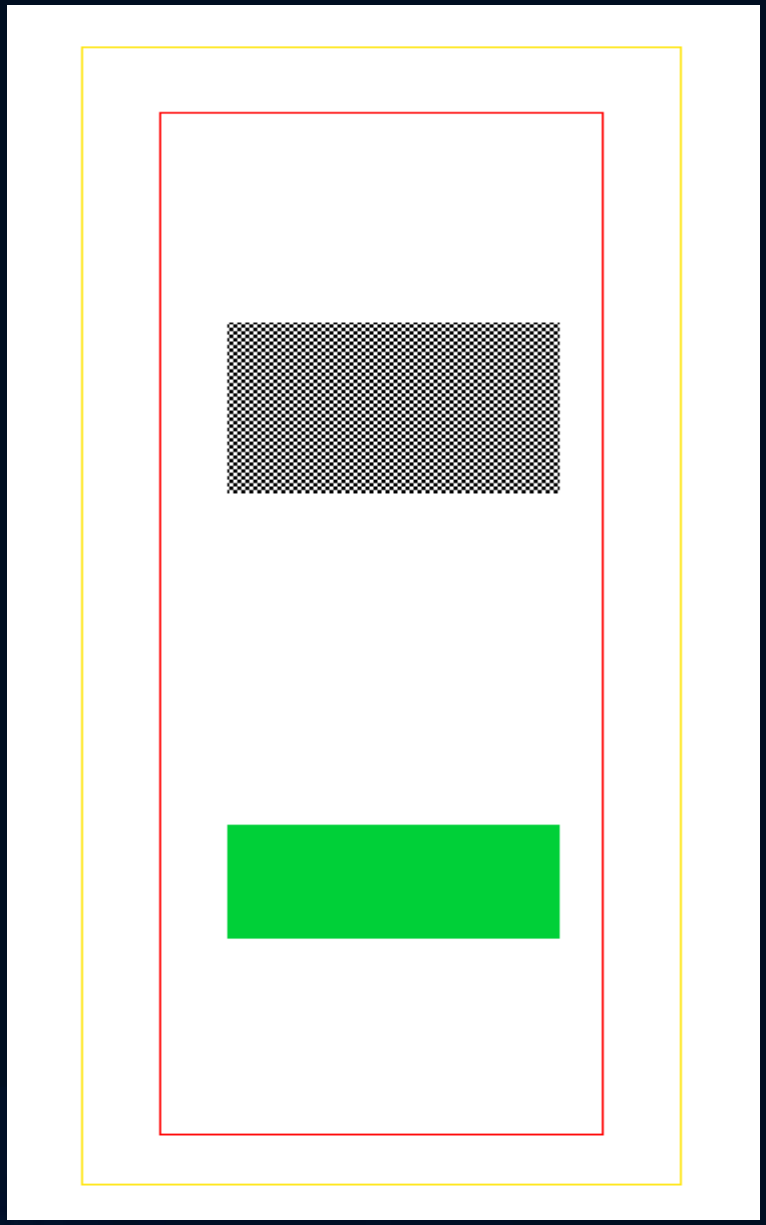
4,1 Invertor 反相器





4,1 Invertor step by step

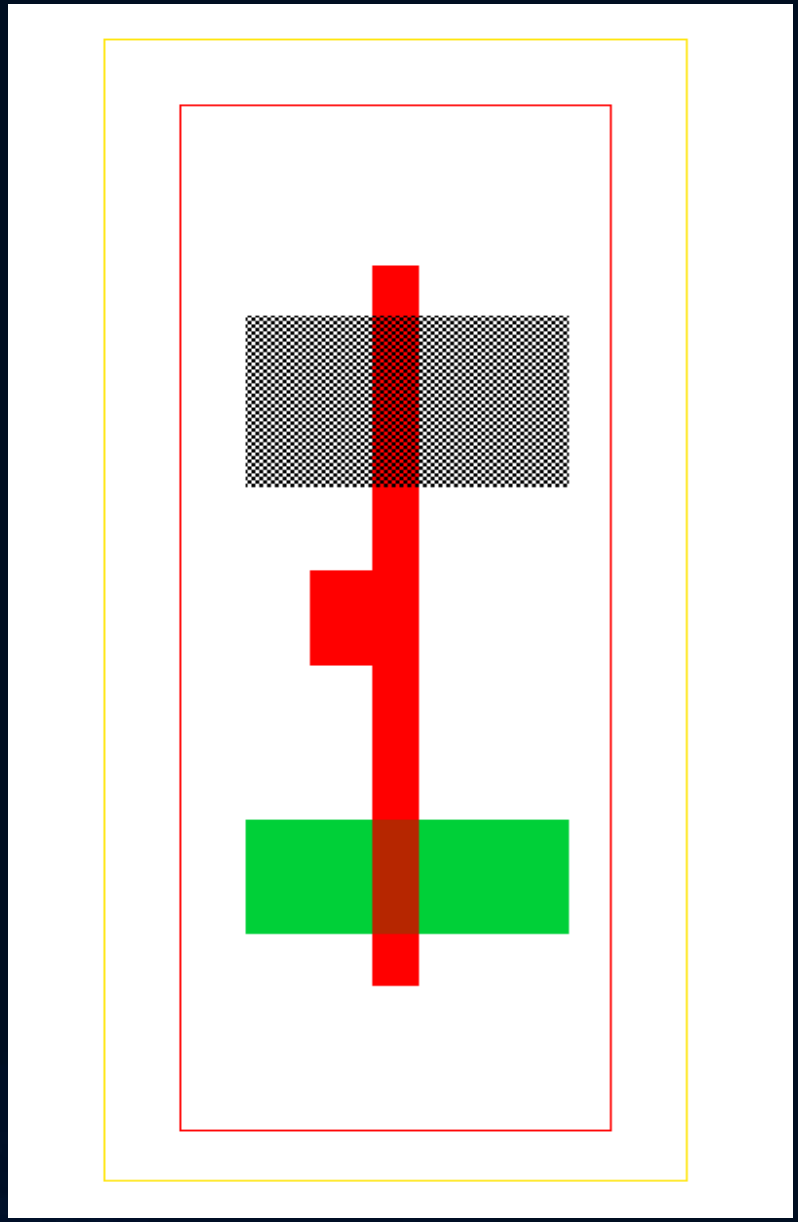
Step 1: 画P & N diffP diff
1. 注意两个扩散区之间的间距



4,1 Invertor step by step

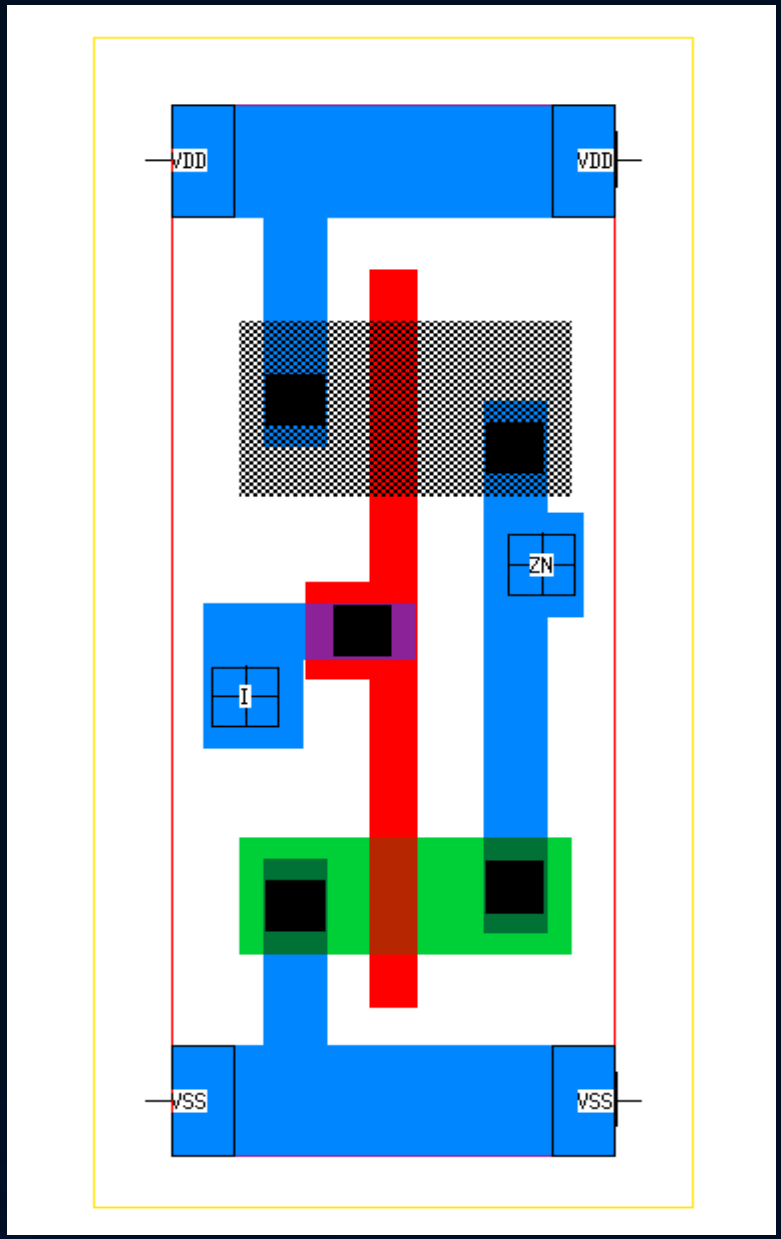
Step 2: 画poly over diffspoly diffs

- 1、关于宽长比W/ L.
- 2、多晶硅要在overlap扩散区
- 3、扩散区与多晶硅之间的最小间距
- 4、poly and poly的间距



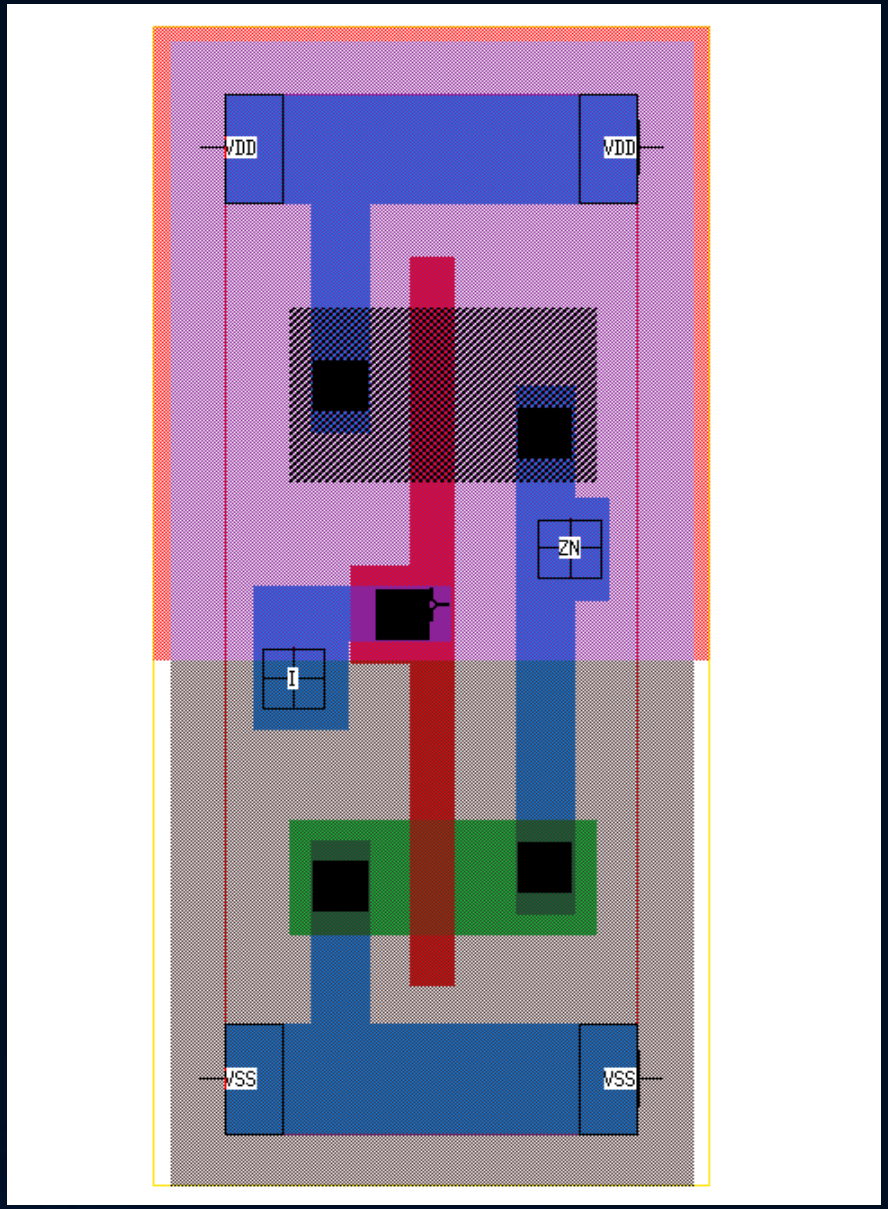
4,1 Invertor step by step

Step 3: 连接各信号线
1、使用Contact来连接metal1&diff 或者poly & metal1.
2、两个contacts 之间的间距，以及contact 与poly的间距.
3、metal和poly之间的最小\overlap
4、metal1之间的间距.
5、尽可能多的排列contacts & vias

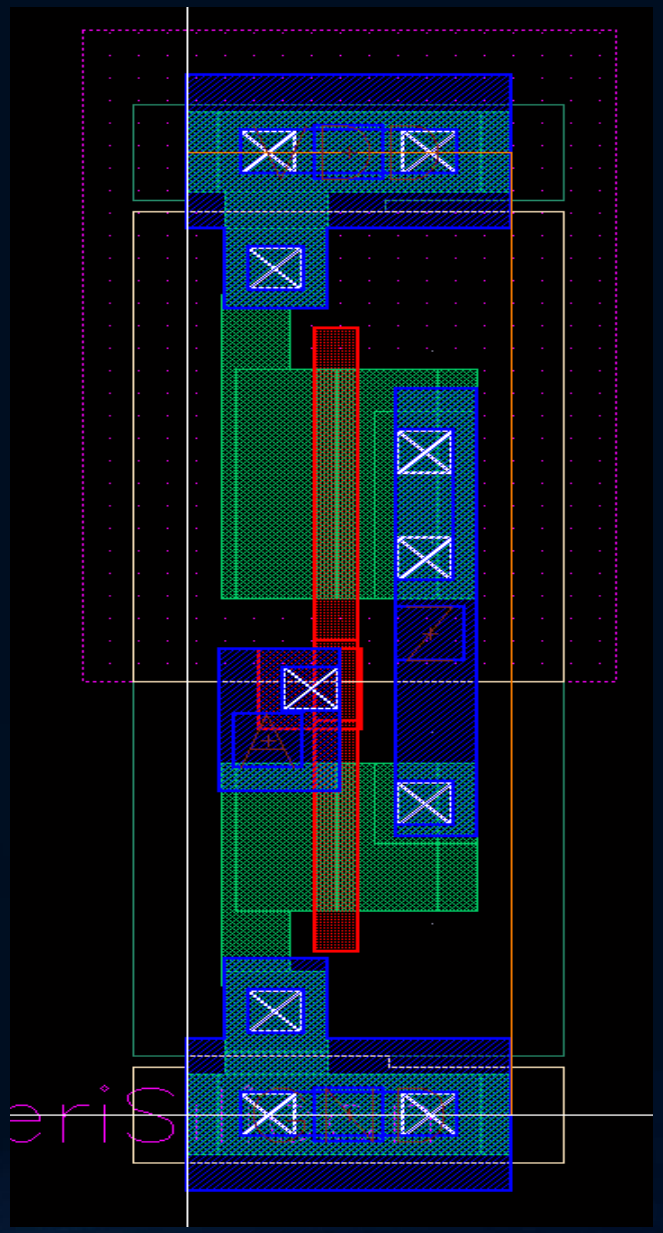


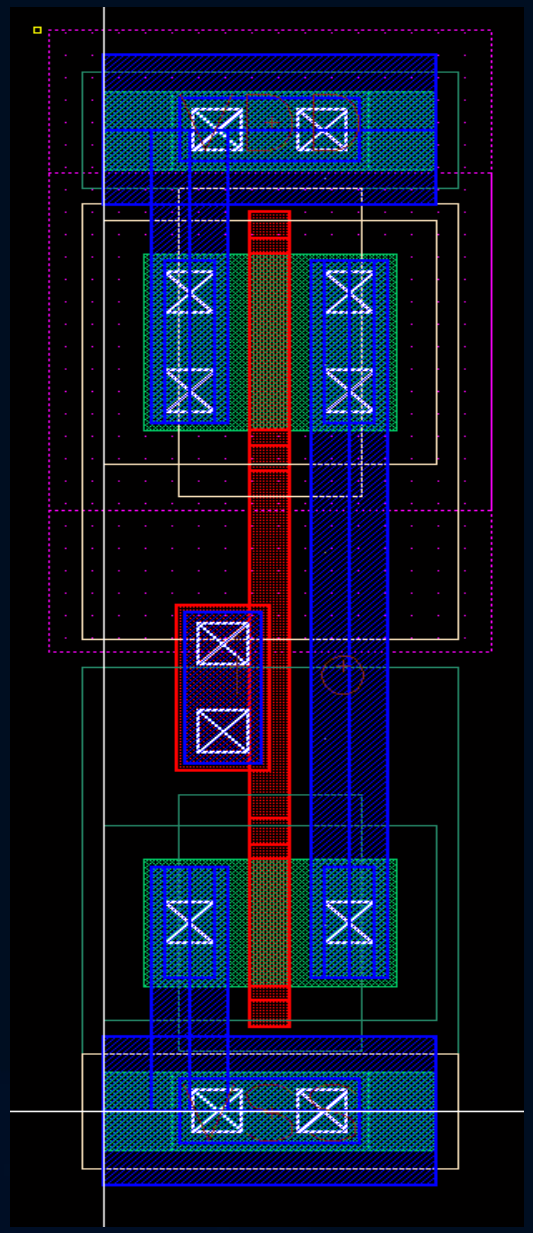
4,1 Invertor step by step

Step 4.Well and ImplsStep
ImplsNotice:
1、最小宽度和面积
2、Well overlap diff 以及 imploverlap diff的规则要求.Draw connson metals, poly, diffsor to mark the signals and the edges of cell.Two kinds of conns: internal and AB conn.

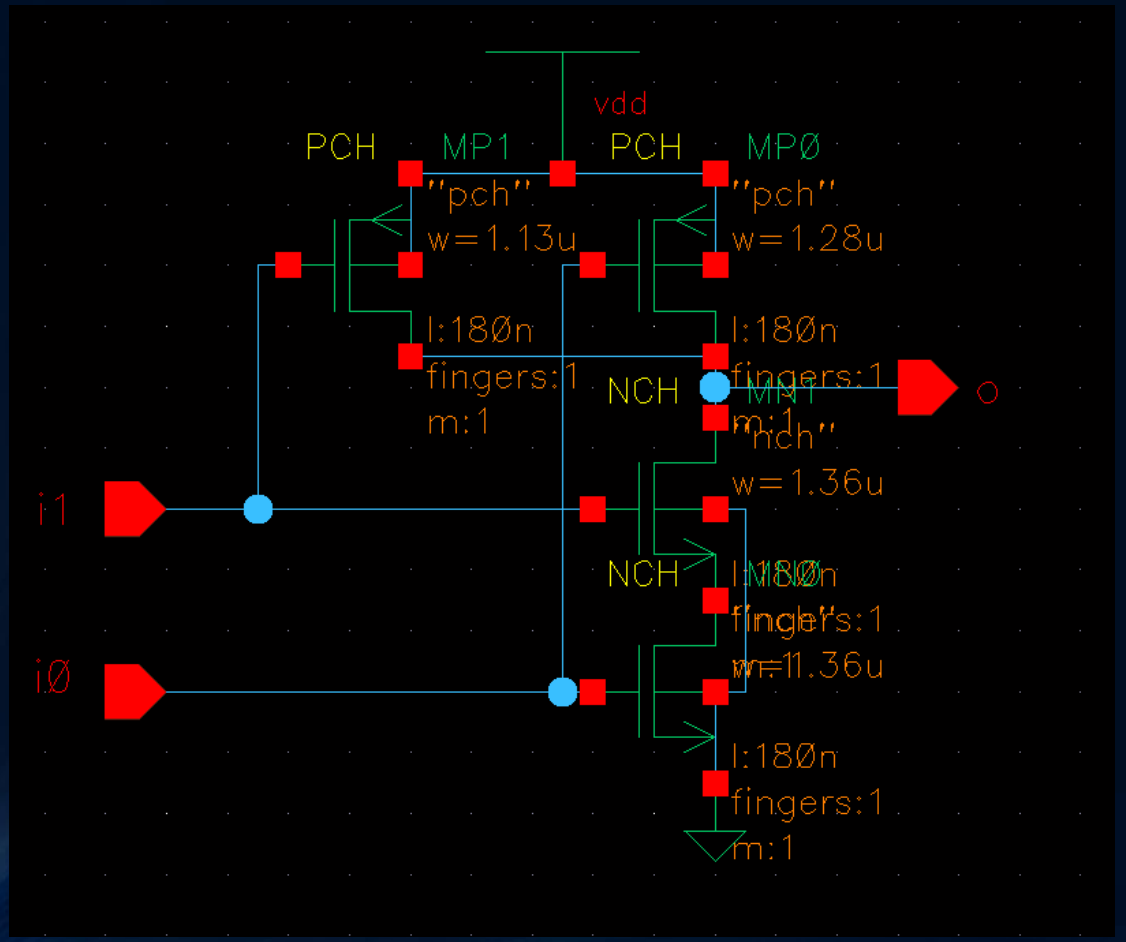


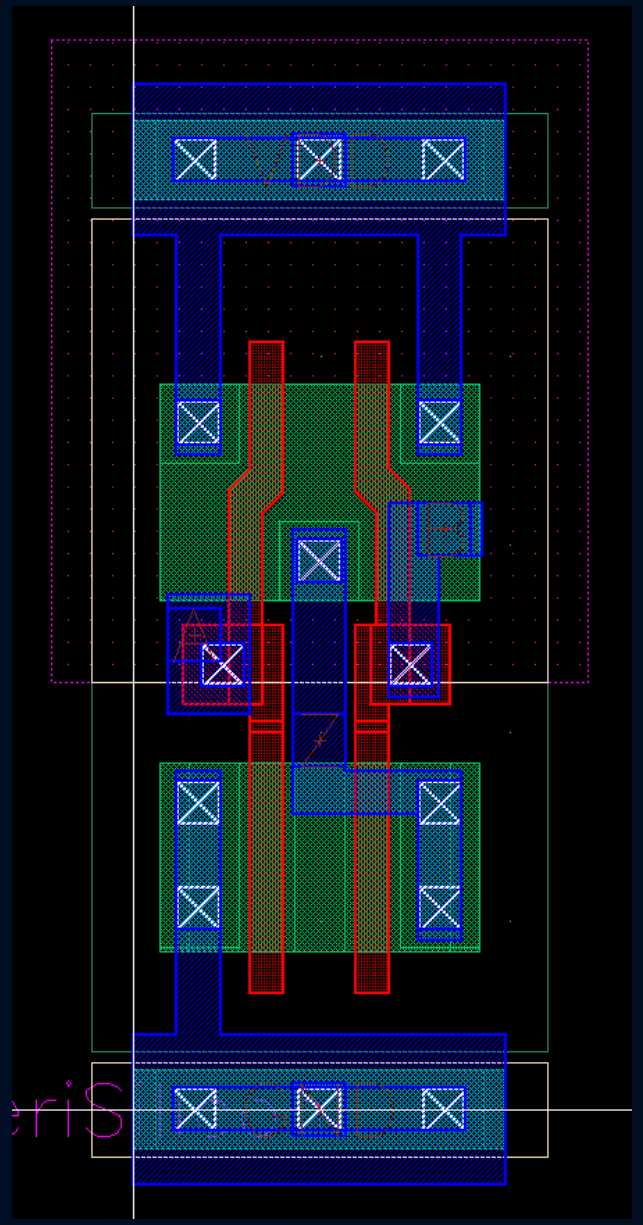
4,1 Invertor



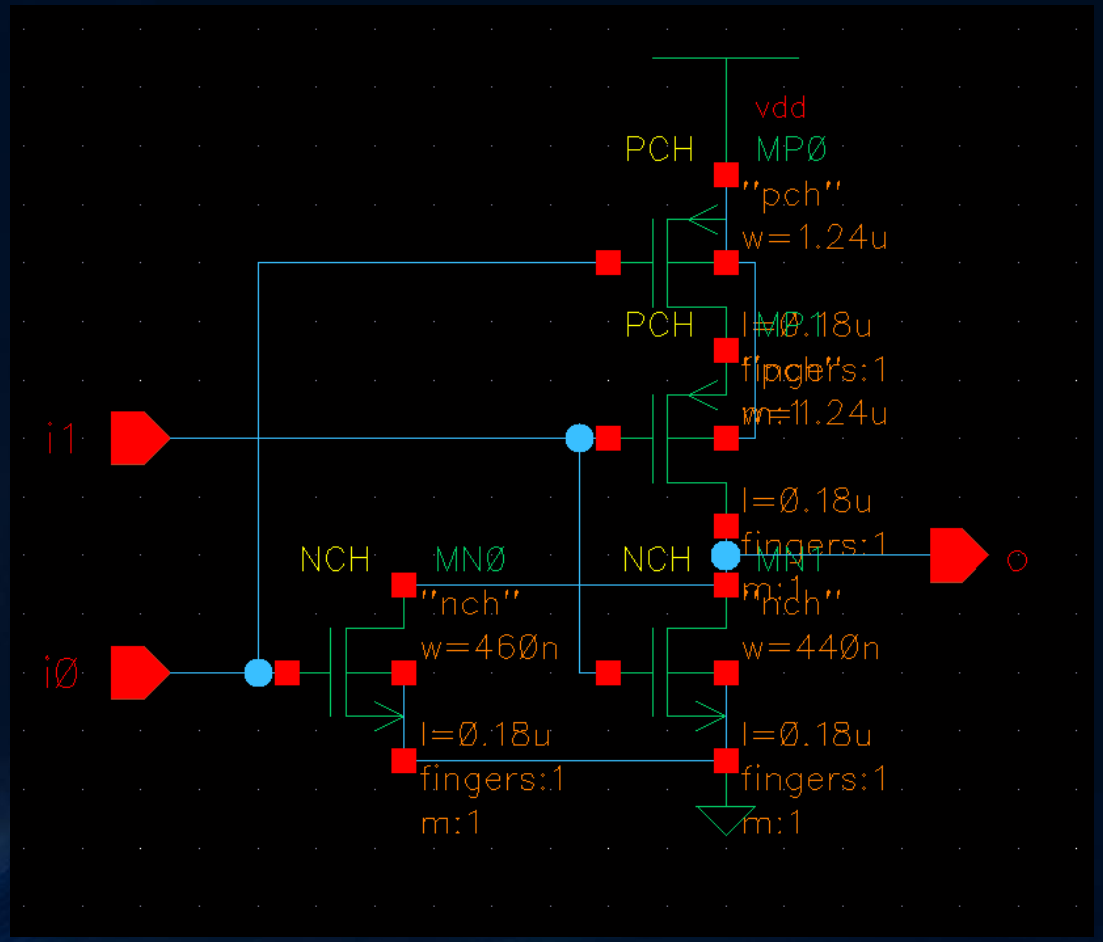


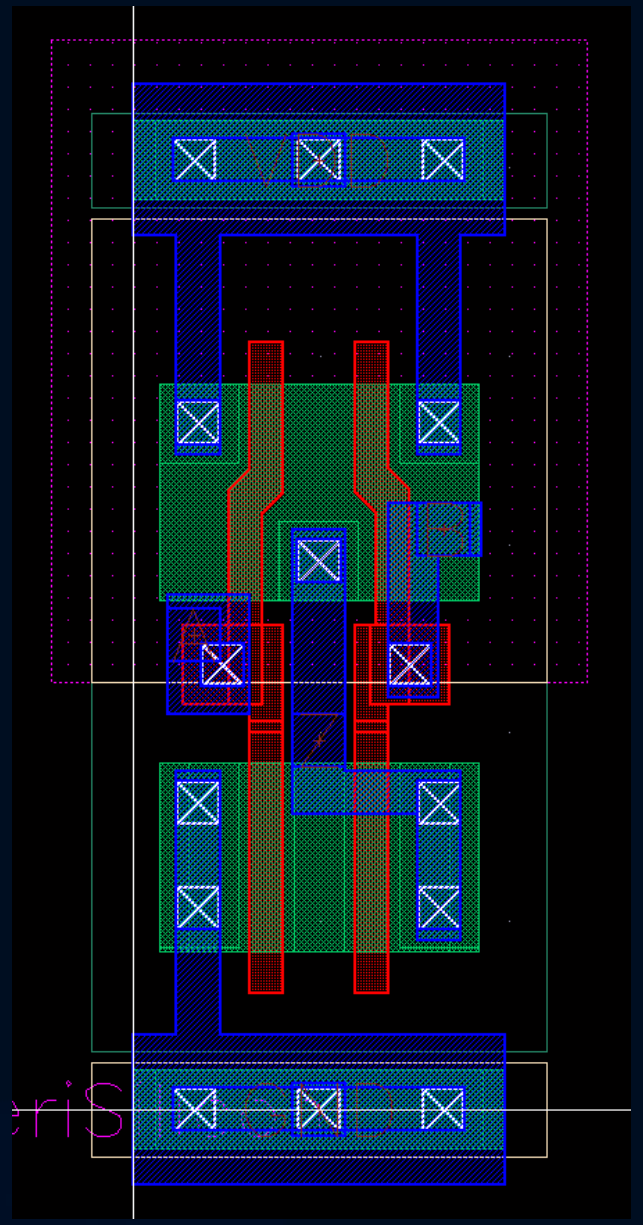
4,2 NAND 与非门


vdd
PCH
MP1
"pch"
w=1.13u
l:180n
fingers:1
m:1
PCH
MPØ
"pch"
w=1.28u
l:180n
fingers:1
m:1
NCH
MN1
"nch"
w=1.36u
o
i1
NCH
iØ
l:180n
fingers:1
m:1

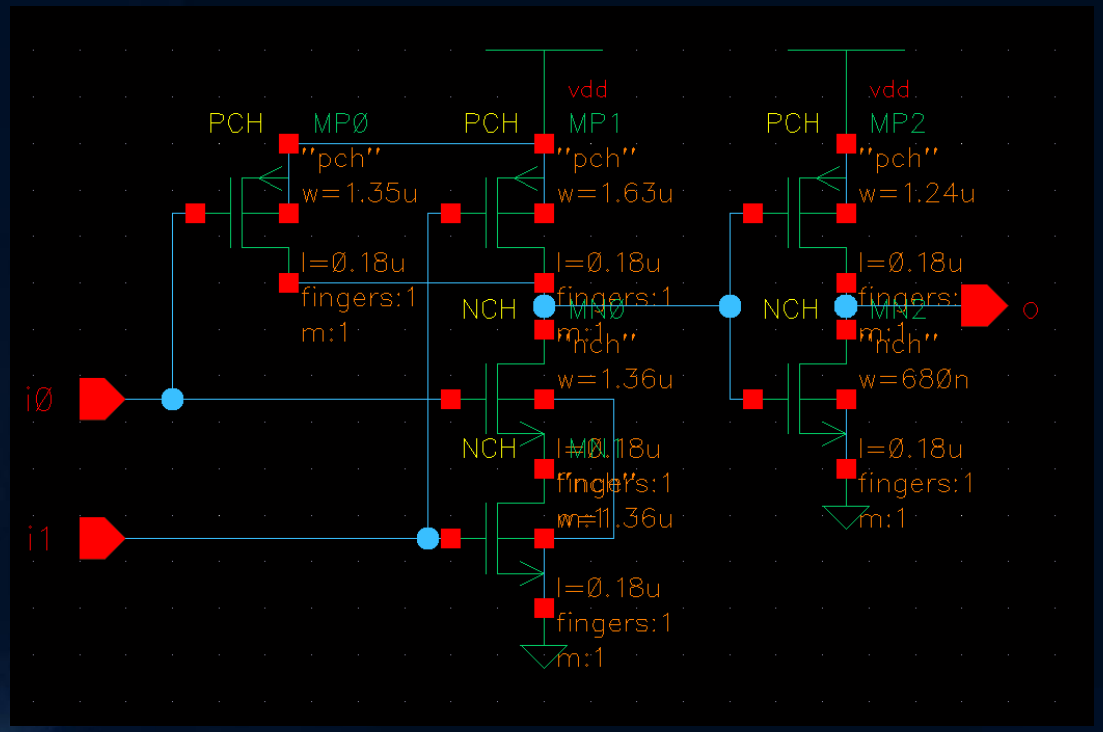


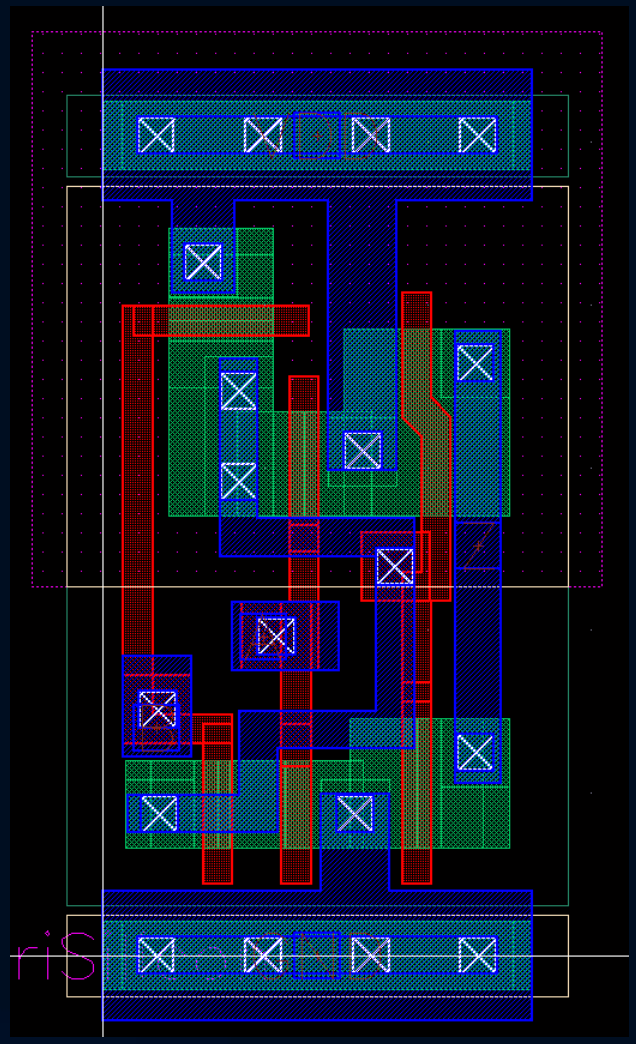
4,3 NOR 或非门


vdd
PCH
MPØ
"pch"
w=1.24u
PCH
l=Ø.18u
fingers:1
m:1
w=1.24u
i1
l=Ø.18u
fingers:1
m:1
NCH
MNØ
NCH
"nch"
w=460n
"nch"
w=440n
iØ
o
l=Ø.18u
fingers:1
m:1
l=Ø.18u
fingers:1
m:1

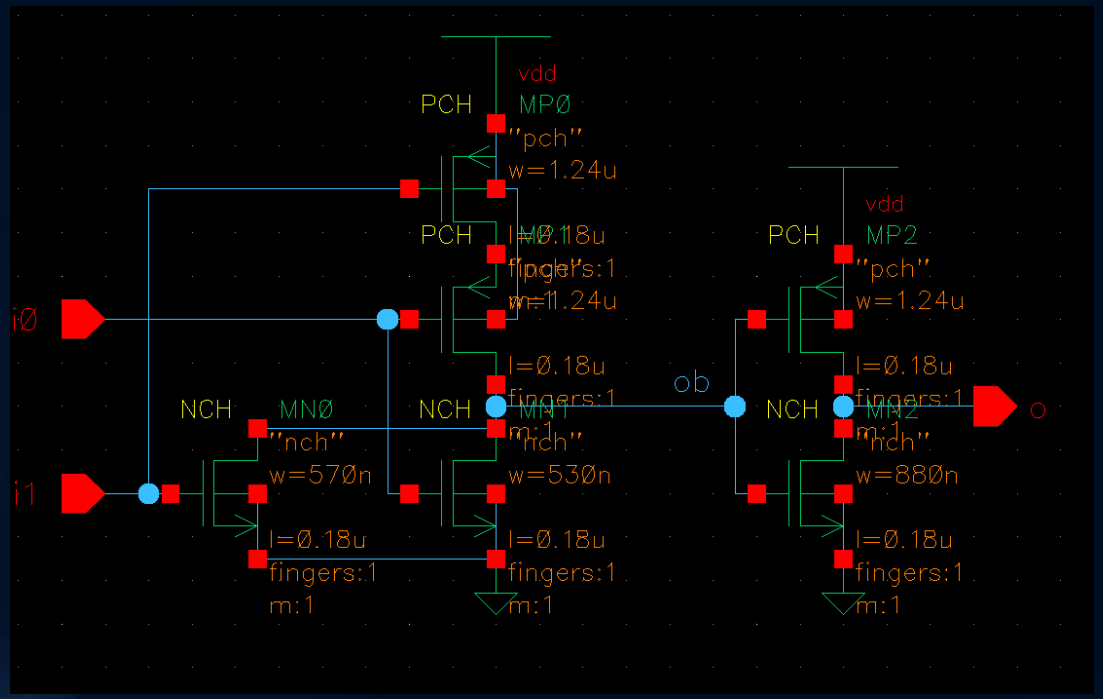


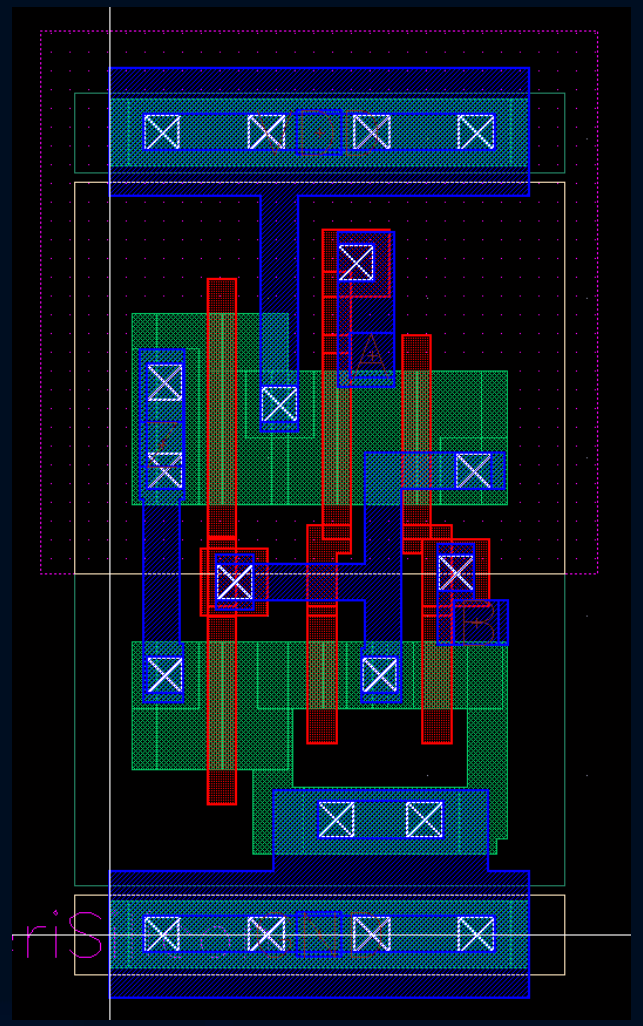
4,4 AND 与门


vdd
PCH
MP0
"pch"
w=1.35u
l=0.18u
fingers:1
m:1
PCH
MP1
"pch"
w=1.63u
l=0.18u
fingers:1
m:1
NCH
MN0
"nch"
w=1.36u
l=0.18u
fingers:1
m:1
NCH
l=0.18u
fingers:1
m:1
i0
i1
vdd
PCH
MP2
"pch"
w=1.24u
l=0.18u
fingers:1
m:1
NCH
MN2
"nch"
w=680n
l=0.18u
fingers:1
m:1
o

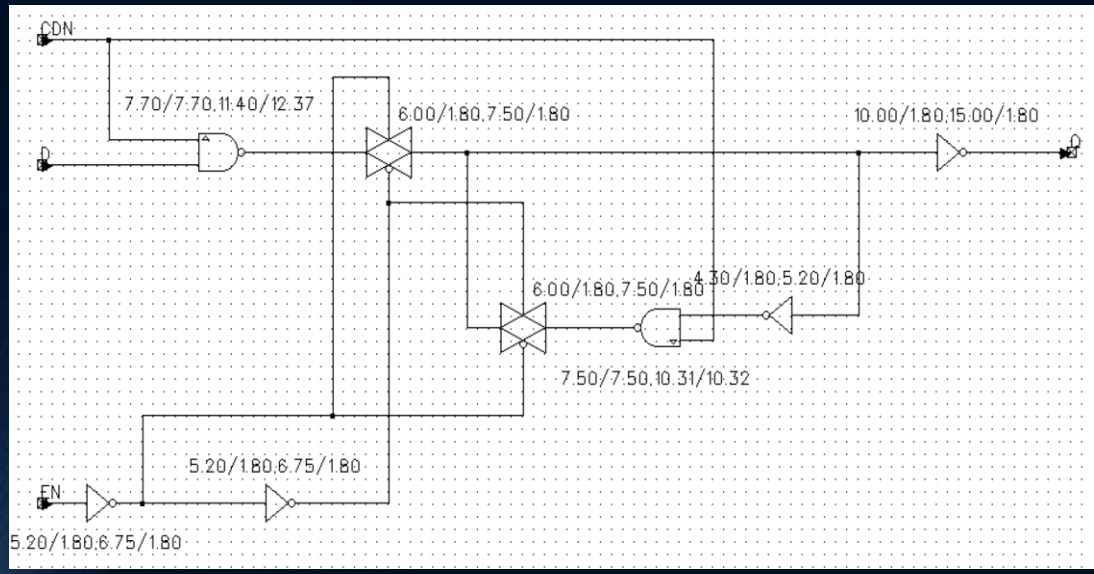


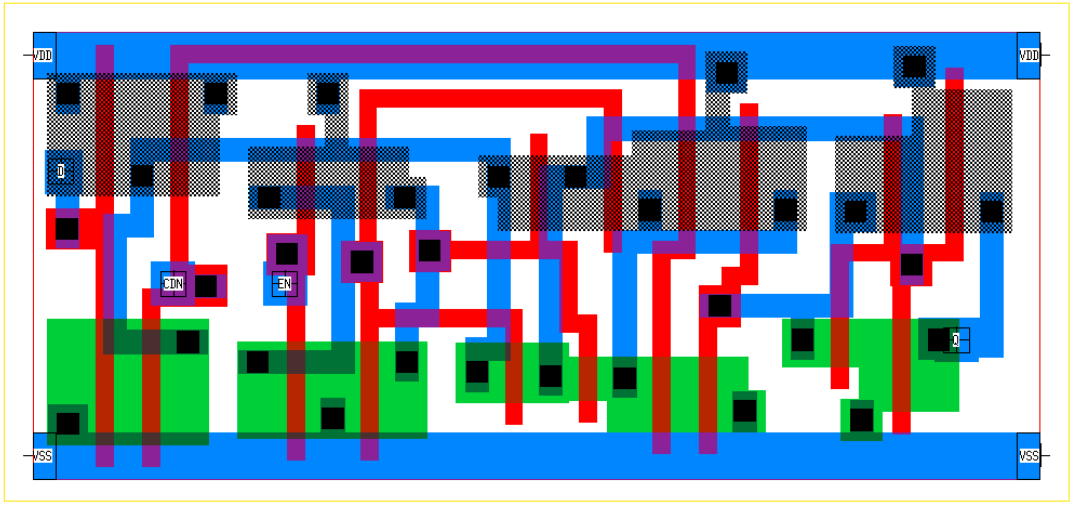
4,5 OR 或门


vdd
PCH
MP0
"pch"
w=1.24u
PCH
l=0.18u
fingers:1
m:1
w=1.24u
i0
i1
NCH
MN0
"nch"
w=570n
l=0.18u
fingers:1
m:1
NCH
MN1
"nch"
w=530n
l=0.18u
fingers:1
m:1
ob
vdd
PCH
MP2
"pch"
w=1.24u
l=0.18u
fingers:1
m:1
NCH
MN2
"nch"
w=880n
l=0.18u
fingers:1
m:1
o

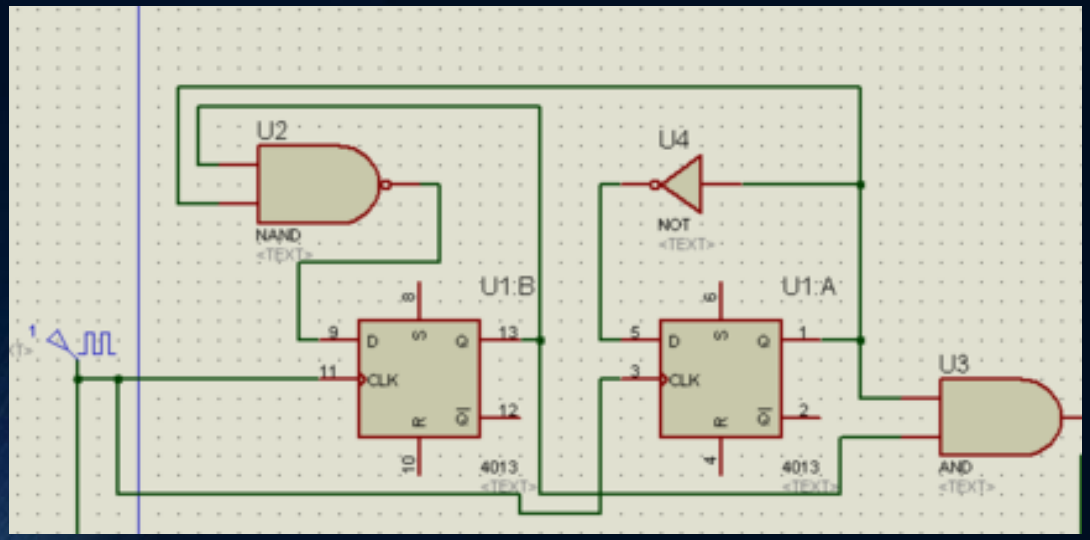


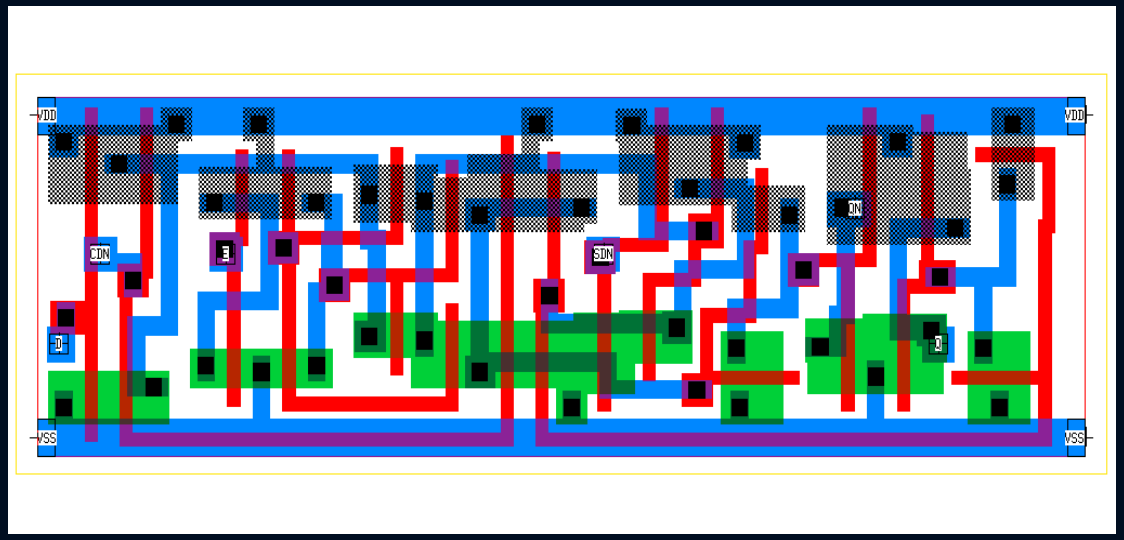
4,6 Latch 锁存器


CDN
D
7.70/7.70,11.40/12.37
6.00/1.80,7.50/1.80
10.00/1.80,15.00/1.80
Q
6.00/1.80,7.50/1.80
4.30/1.80,5.20/1.80
7.50/7.50,10.31/10.32
5.20/1.80,6.75/1.80
EN
5.20/1.80,6.75/1.80


VDD
VDD
D
CDN
EN
Q
VSS
VSS

4,6 DFF 触发器


U2
NAND
U4
NOT
U1:B
U1:A
U3
AND
4013
4013
CLK
CLK


VDD
VSS
CDN
SDN
D
Q

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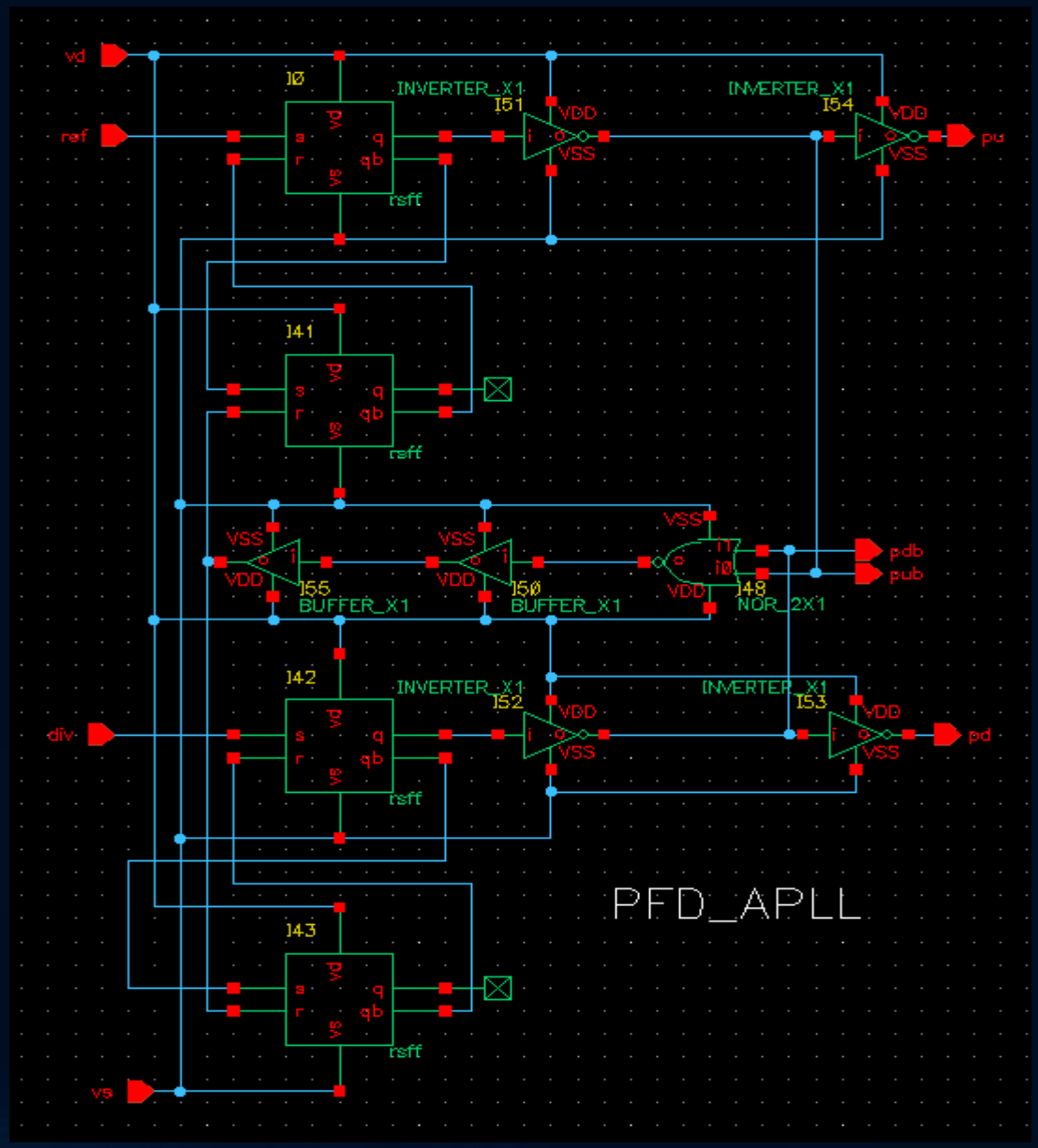
5. 数字电路
6. 模拟电路
7. 模拟电路高级技能

5，数字电路

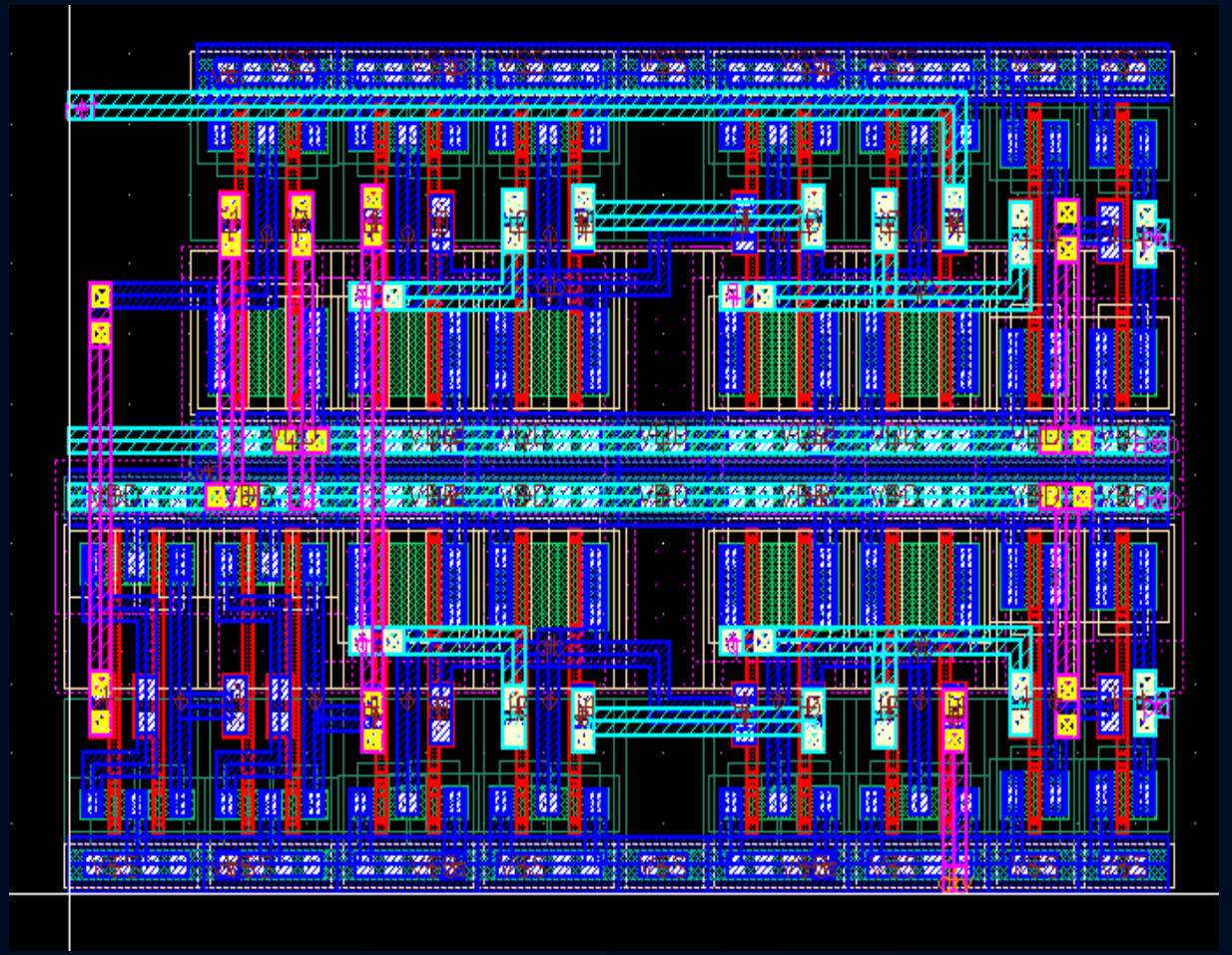
以一个pfd为例子，了解简单数字电路的schmatic，并画出对应的layout，完成版图物理验证drc/lvs。

数字电路板图设计时的关注点
-速度
-负载能力
-所用的面积

5，数字电路


vd
ref
div
vs
I0
I41
I42
I43
rsff
INVERTER_X1
I51
I52
I53
I54
VDD
VSS
pu
pd
pdb
pub
BUFFER_X1
I55
I50
NOR_2X1
I48
PFD_APLL

5，数字电路



课程内容

1. DEA软件使用 — 版图编辑和物理验证工具
2. CMOS工艺中的层次
3. 基本器件和单元的版图结构
4. Stdcell 标准单元
5. 数字电路
6. 模拟电路
7. 模拟电路高级技能

6, 模拟电路

以一个bandgap为例子，了解简单模拟电路的schmatic，
并画出对应的layout，完成版图物理验证drc/lvs。

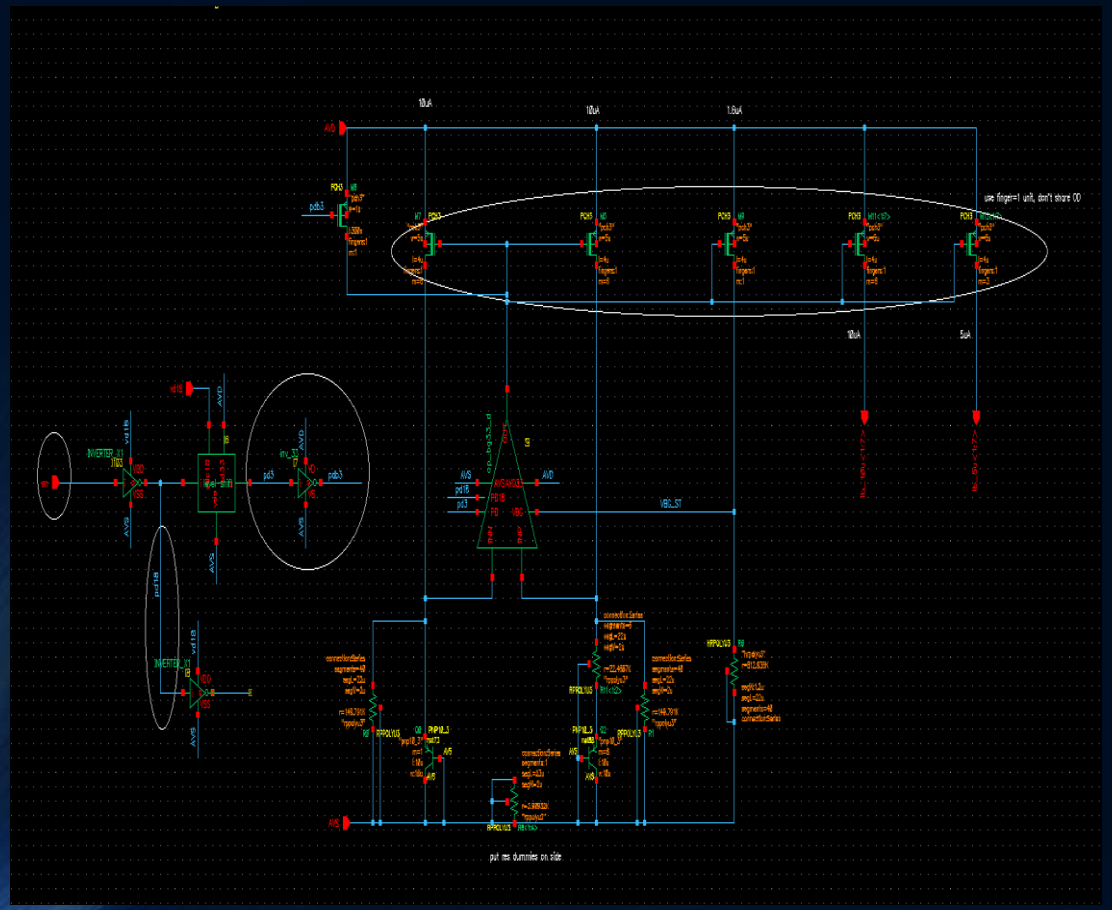
数字电路和模拟电路的差别：

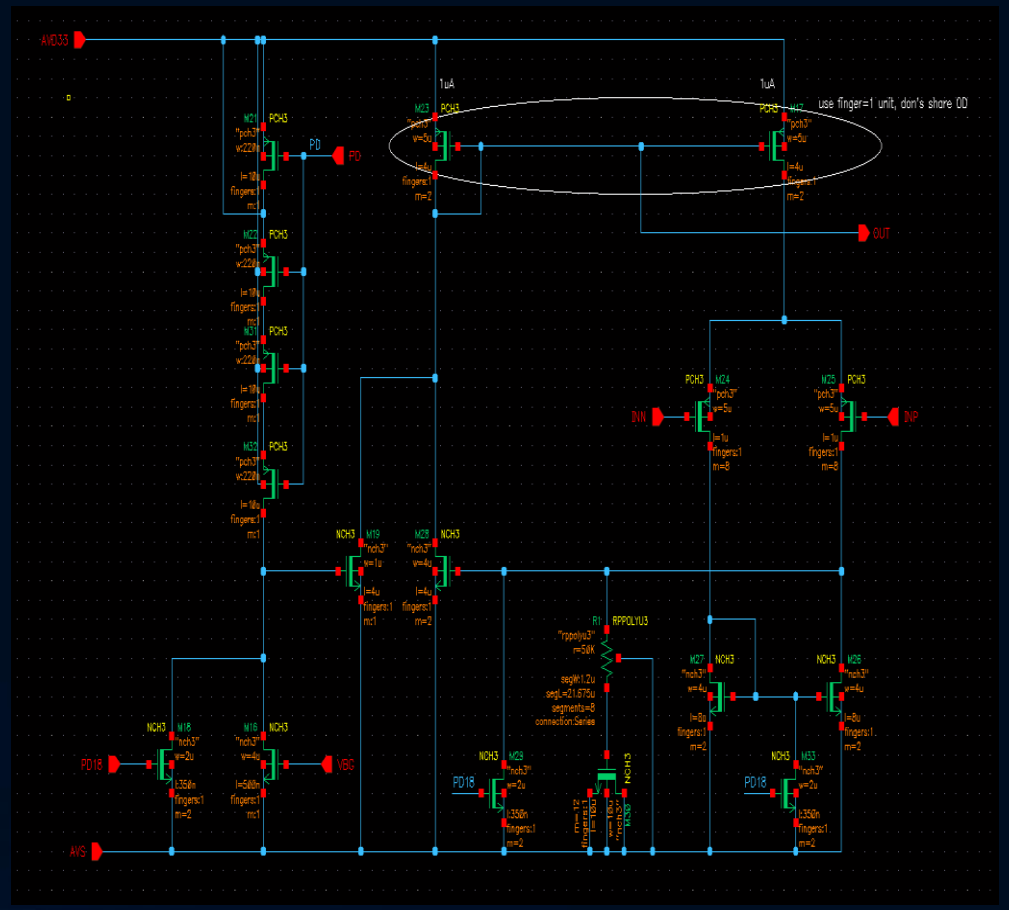
数字电路和模拟电路的首要目标不同，
数字电路关注的是面积，什么都是最小化
•Astro、appollo等自动布局布线工具
模拟电路关注的是功能，电路性能、匹配、速度等
•没有EDA软件能全自动实现，所以需要手工处理

6，模拟电路

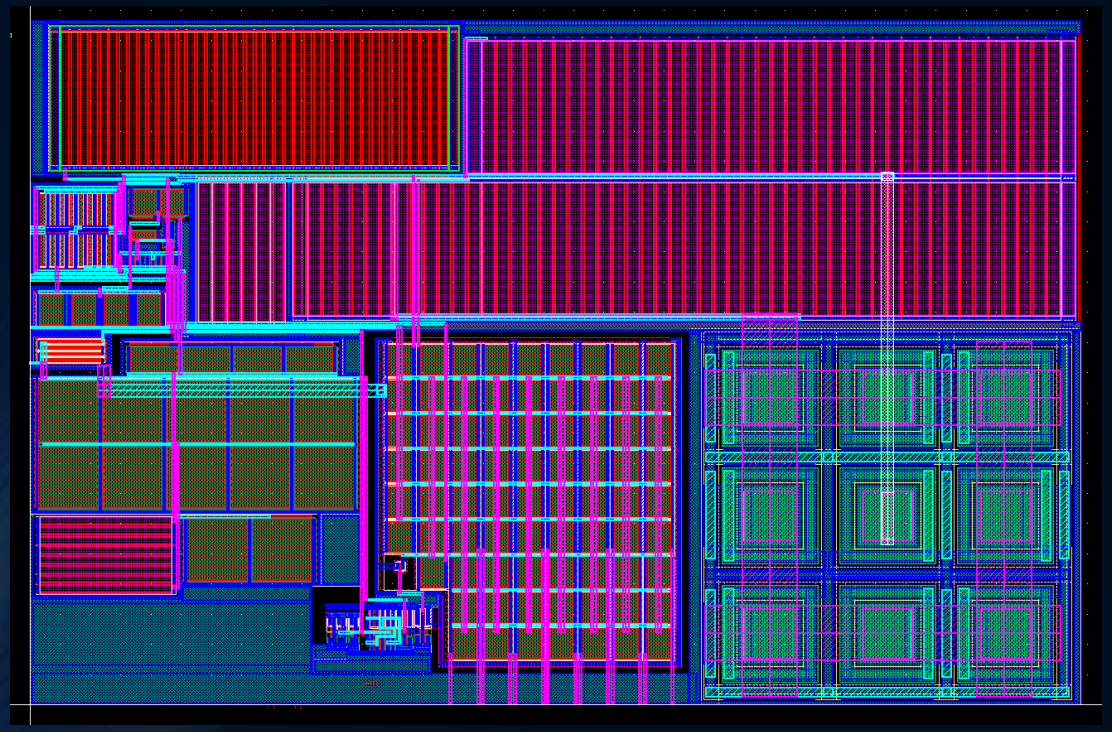
模拟电路版图设计首先考虑三大问题
- 此电路是做什么用的
- 确定一些问题，如隔离、匹配、布局等
- 需要多少电流
- 金属线宽（外部互连，内部源漏）
- 电流流动方向
- 匹配性问题

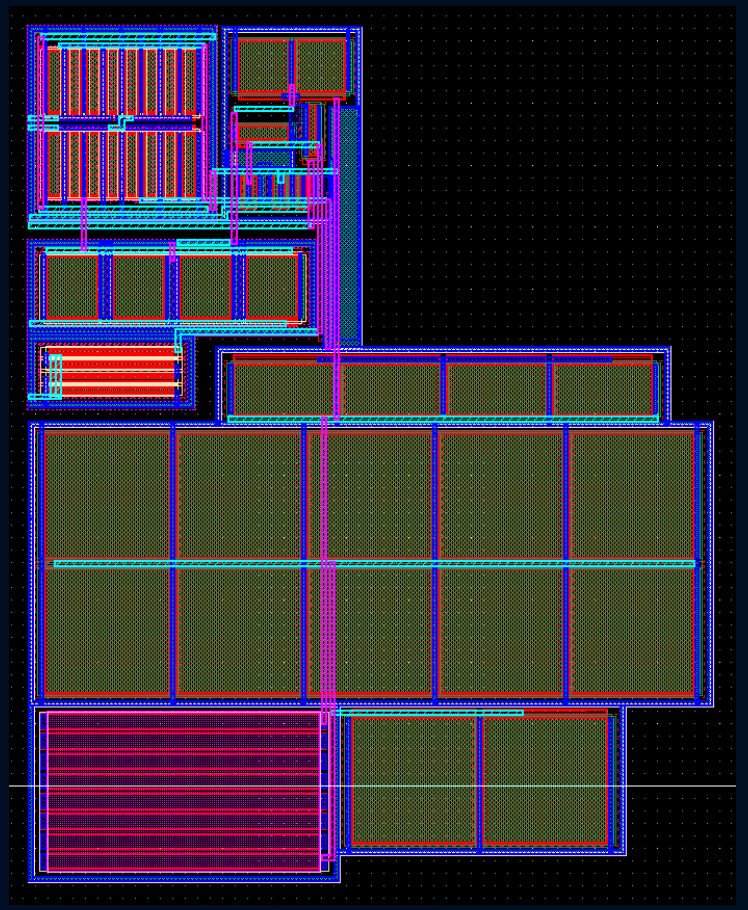
6, 模拟电路


10uA
10uA
1.6uA
use finger=1 unit, don't share OD
10uA
5uA
VBG_ST
put res dummies on side


AVD33
1uA
1uA
use finger=1 unit, don't share OD
PD
OUT
INN
INP
PD18
VBG
AVS

6, 模拟电路





课程内容

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7, Art of Layout

在能独立完成简单模拟电路的版图之后，需要了解模拟电路的高阶要求。

对称 Match
隔离 Shielding
可靠性规则 Rules for Reliability
闩锁效应 Latchup
静电保护 ESD
金属密度规则 Density
天线规则 Antenna
电迁移 Electromigration

7.1 Match

Matching（匹配），精确的宽长比（W/L），噪声（noise）等因素不是非常重要。

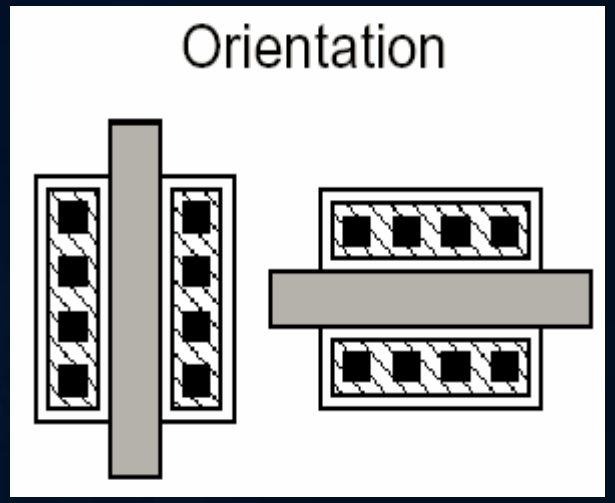
匹配问题

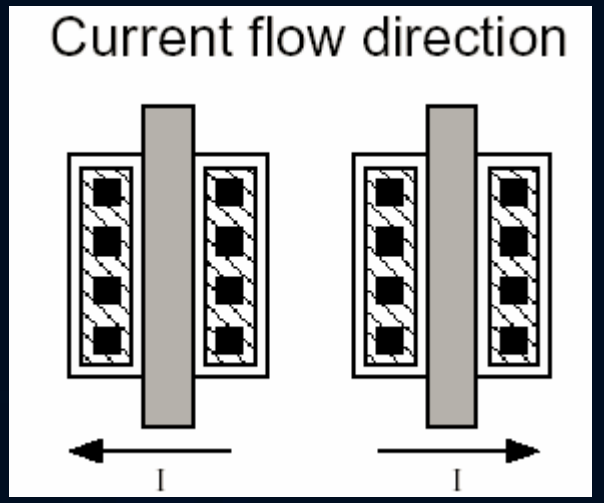
- -差分对、电流镜…?
- -误差
- -工艺导致不匹配

- 不统一的扩散
- 不统一的注入
- CMP后的不完美平面
  - -片上变化导致不匹配
- 温度梯度
- 电压变化

7.1 Match

使所有的东西尽量理想，使要匹配的器件被相同的因素以相同的方式影响





7.2 Latch up

1.避免闩锁效应：最常见的Latch up诱因是**电源、地的瞬态脉冲**，这种瞬态脉冲可能的产生原因是瞬时电源中断等，它可能会使引脚电位高于vdd或低于vss，容易发生latch up。因此对于电路中有连接到电源或地的MOS管，周围需要加保护环。

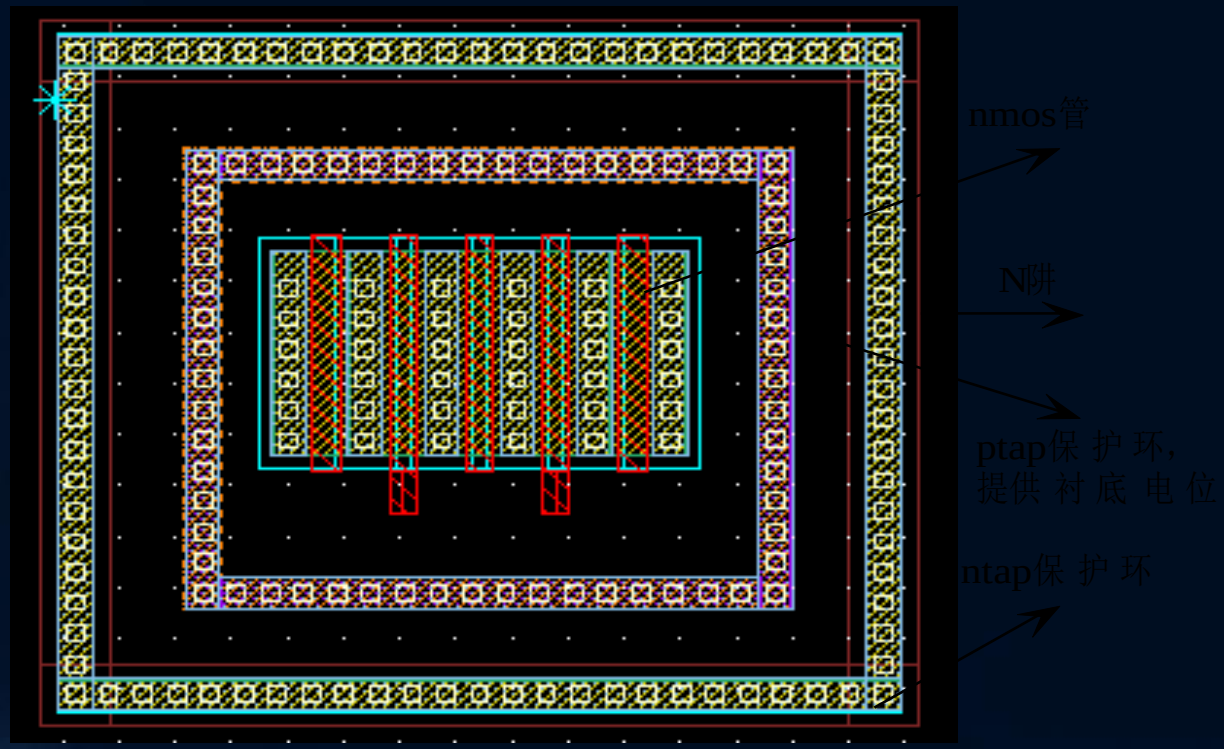
2.容易发生latch up的地方：任何不与power supply、substrate相连的引脚都可能。所以精度要求高时，要查看是否有引脚引线既不连power supply，也不连substrate，凡是和这样的引线相连的源区、漏区都要接保护环。

3.**保护环要起到有效的作用就应该使保护环宽度较宽、电阻较低，而且用深扩散材料。**

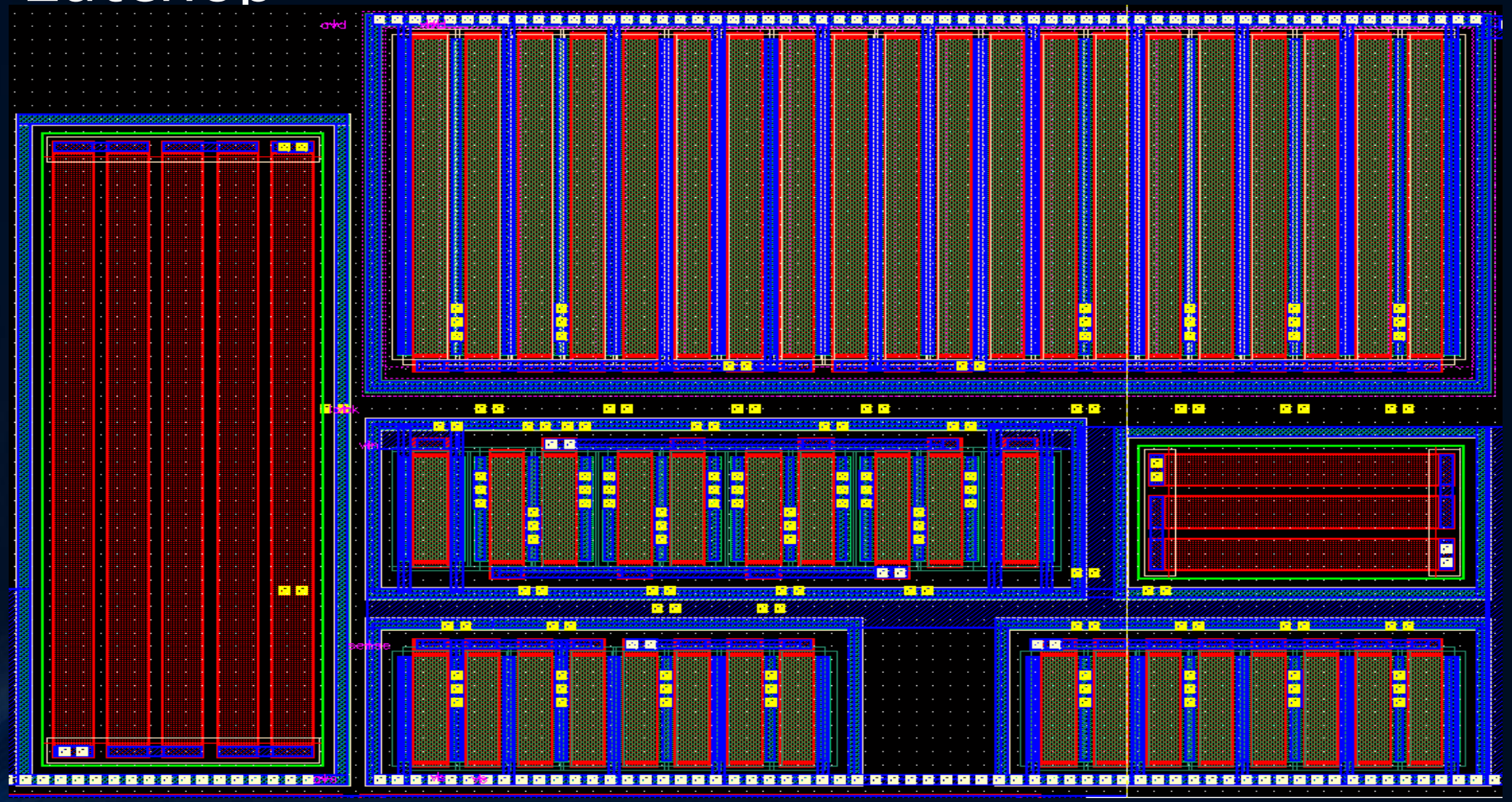
4. **N管的周围应该加吸收少子电子的N型保护环（ntap），ntap环接vdd；P管的周围应该加吸收少子空穴的P型保护环（ptap），ptap环接gnd。双环对少子的吸收效果比单环好。**

7.2 Latchup

7.2 Latchup

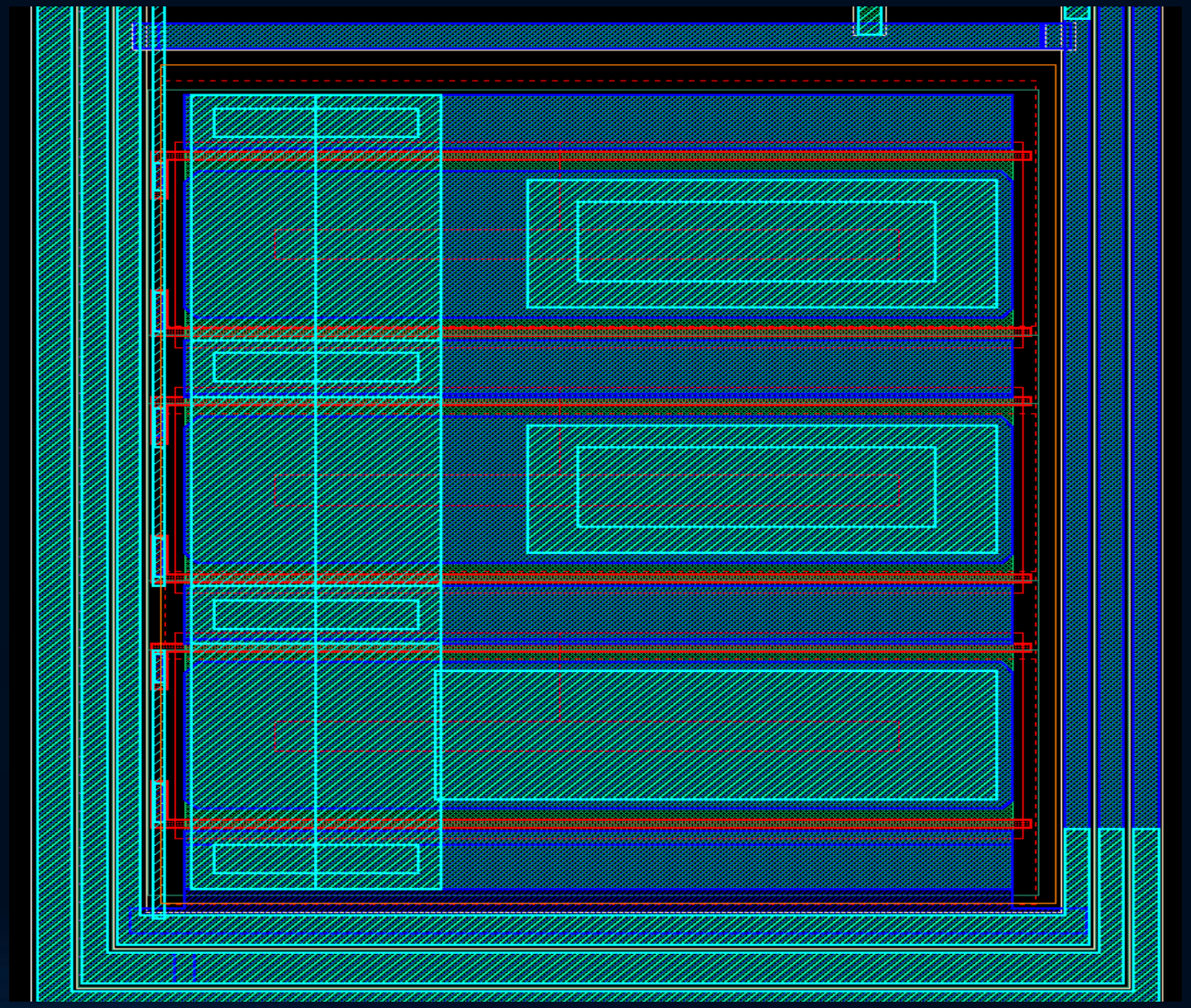


7.2 Latchup



7.3 ESD

增加接pad的mos的drain到gate的距离，起到了增加限流电阻的作用。



7.4 Density

每个层次都有密度的要求，不能过高，也不能过低。

7.5 Antenna

天线效应——长金属线（面积较大的金属线）在刻蚀的时候，会吸引大量的电荷（因为工艺中刻蚀金属是在强场中进行的），这时如果该金属直接与管子栅（相当于有栅电容）相连的话，可能会在栅极形成高电压会影响栅极氧化层的质量，降低电路的可靠性和寿命。

天线效应的解决方法：用另外一层更高一层的金属来割断本层的大面积金属。

7.6 Electromigration

电迁移效应：所谓电迁移效应是指当传输电流过大时，电子碰撞金属原子，导致原子移位而使金属断线。

根据电路在最坏情况下的电流值来决定金属线的宽度以及接触孔的排列方式和数目，以避免电迁移。

7.7 高阶要求

布局规划
- 考虑pad的位置影响来决定模块的摆放及其输入输出方向
- 考虑模块间的连接关系确定整个布局

•尽量短的连线
•尽量少的交叉
•尽量不要在模块上通过连线
- 考虑信号的要求来决定模块布局

•如信号的绝对对称性
- 面积估算

•模块间留下足够的距离布线
•要考虑电源线走线、有对称要求的差分信号走线、有隔离要求的信号走线等，预留足够空间
- 估计连线问题

7.7 高阶要求

一些小提示

- 不要受最小尺寸限制，适当放大间距、宽度之类
- 不要用最小线宽布线，而更应关注寄生电阻是否较低
- 多打通孔，既保证连接，又减小寄生电阻
- 尽量让所有的管子保持在同一个方向
- 对于模拟电路，不要在模块上，或者任何元件上，走信号线
- 敏感信号和比较噪的信号线不要经过任何元件上方
- 信号线不要经过电容上方
- 提前关注敏感信号和比较噪的信号，想好是否屏蔽或者如何屏蔽

7.8 高阶要求

一些小提示

- -电源线宽度尽量宽些
- -高频信号线，尽量用寄生电容最小的那层金属走线
- -不要让噪声进入衬底
- -如果版图看起来很漂亮，简单的，对称的，很好的信号流，没有交叉……那么它将很好地工作。设想自己是一个电子。
- -了解工艺流程
- -不要过分要求

7.8 高阶要求

减小寄生电容的方法

- 寄生电容＝金属线宽×金属长度×单位面积电容
- 敏感信号线尽量短
- 选择高层金属走线

• 最高层金属，离衬底最远，单位面积电容最小

- 敏感信号彼此远离
- 不宜长距离一起走线
- 电路模块上尽量不要走线
- 绕开敏感节点

7.8 高阶要求

减小寄生电阻

- -寄生电阻＝（金属长度/金属宽度）×方块电阻
- -加大金属线宽，减小金属长度
- -如果金属线太宽，可以采用几层金属并联走线

•M1M2M3三层金属并联布线，总的寄生电阻减小1/3