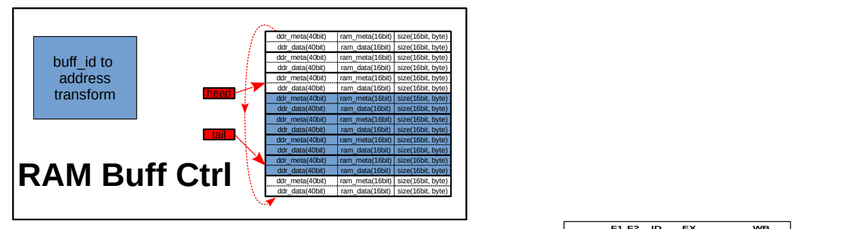
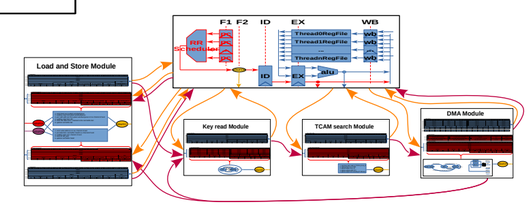
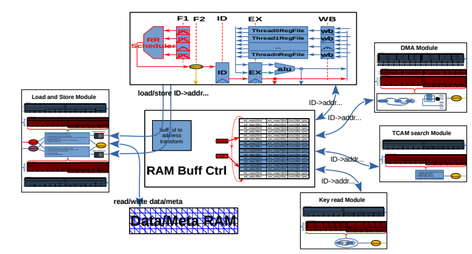
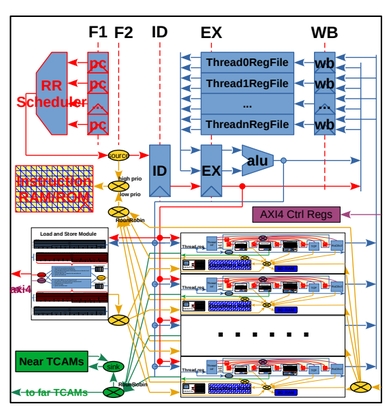
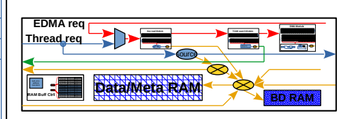
dma bd format
mv bd
dist_addr_offset to meta/data
src_addr_offset to meta/data
reserved
size
opcode: 1

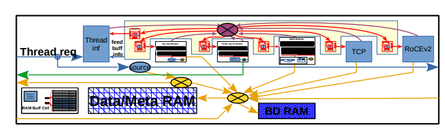

buff_id to address transform
head
tail
RAM Buff Ctrl
ddr_meta(40bit)
ddr_data(40bit)
ram_meta(16bit)
ram_data(16bit)
size(16bit, byte)

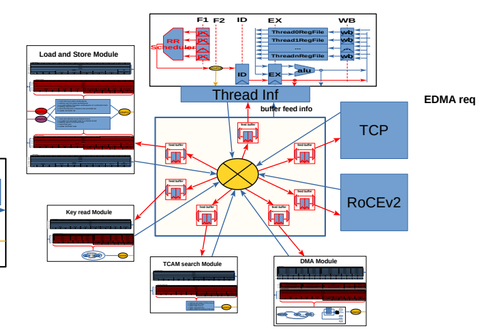

F1 F2 ID EX WB
Load and Store Module
Key read Module
TCAM search Module
DMA Module

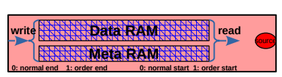

F1 F2 ID EX WB
Load and Store Module
load/store ID->addr...
ID->addr...
RAM Buff Ctrl
read/write data/meta
Data/Meta RAM
DMA Module
TCAM search Module
Key read Module

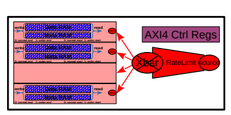

F1 F2 ID EX WB
RR Scheduler
pc
Thread0RegFile
Thread1RegFile
ThreadnRegFile
wb
ID
EX
alu
Instruction RAM/ROM
AXI4 Ctrl Regs
Load and Store Module
Near TCAMs
to far TCAMs

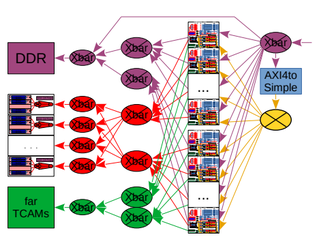

EDMA req
Thread req
Data/Meta RAM
BD RAM

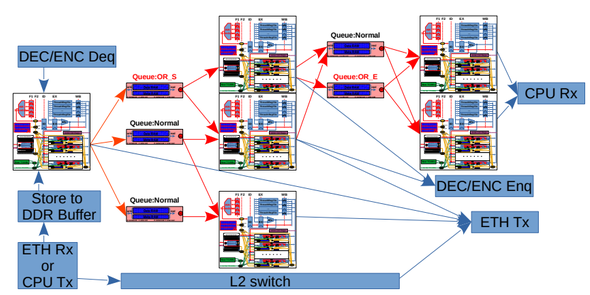

Thread req
Thread inf
TCP
RoCEv2
Data/Meta RAM
BD RAM


F1 F2 ID EX WB
Load and Store Module
Thread Inf
buffer feed info
EDMA req
TCP
RoCEv2
Key read Module
TCAM search Module
DMA Module


write
Data RAM
Meta RAM
read
0: normal end
1: order end
0: normal start
1: order start


AXI4 Ctrl Regs
RateLimit


DDR
far TCAMs
AXI4to Simple


DEC/ENC Deq
Queue:OR_S
Queue:Normal
Queue:OR_E
CPU Rx
DEC/ENC Enq
Store to DDR Buffer
ETH Tx
ETH Rx or CPU Tx
L2 switch