EET 122 Midterm **Name**_____

Date_____

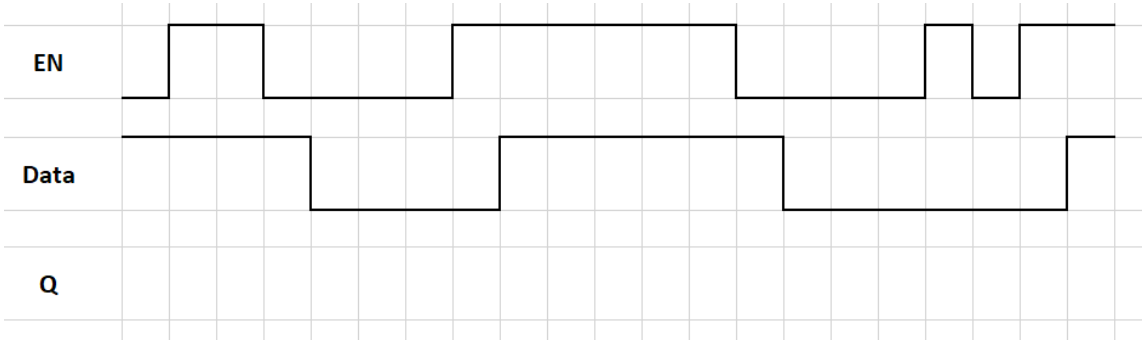
1. Draw the following for a D-type flip-flop (DFF):

a) (5 pts) The symbol with a falling edge clock input

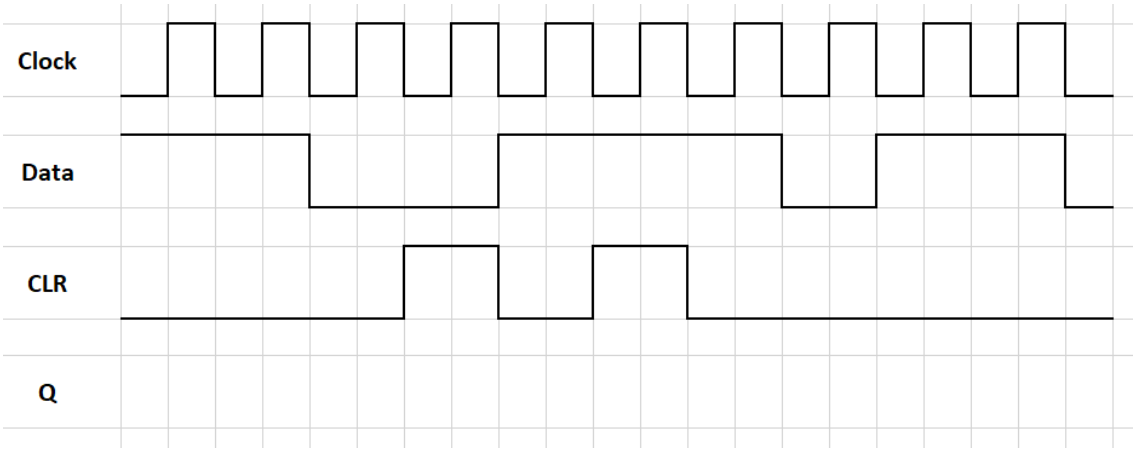
b) (5 pts) The truth/function table

c) (5 pts) A timing diagram showing one clock cycle, the input D, and the output Q. The diagram must include the propagation delay, the setup time, and the hold time.

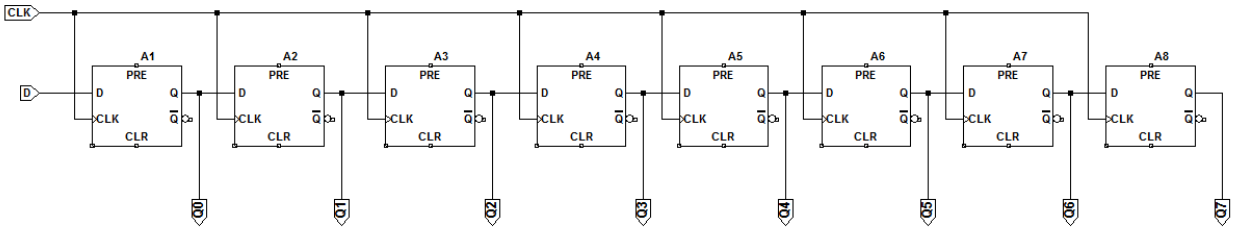
2. (10 pts) Draw the Q output for a D-type latch with the following EN and D inputs. The EN input is active HIGH. Assume that the Q output starts in the LOW state.



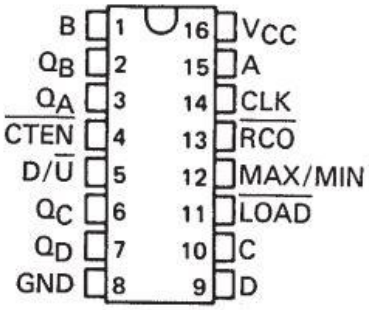
3. (10 pts) Draw the Q output for a D-type flip-flop with the following CLK/EN and D inputs. The DFF is rising-edge-triggered. Assume that the Q output starts in the LOW state. The CLR input is asynchronous.



4. (15 pts) Consider the shift register below, where D = 0, and Q0 is the LSB. Assume that all of the preset (PRE) and clear (CLR) inputs are inactive. If the initial value of Q is 0X1C (Q0, the furthest to the left, is the LSB), what are the hex values (states) for each of the next three clock pulses?



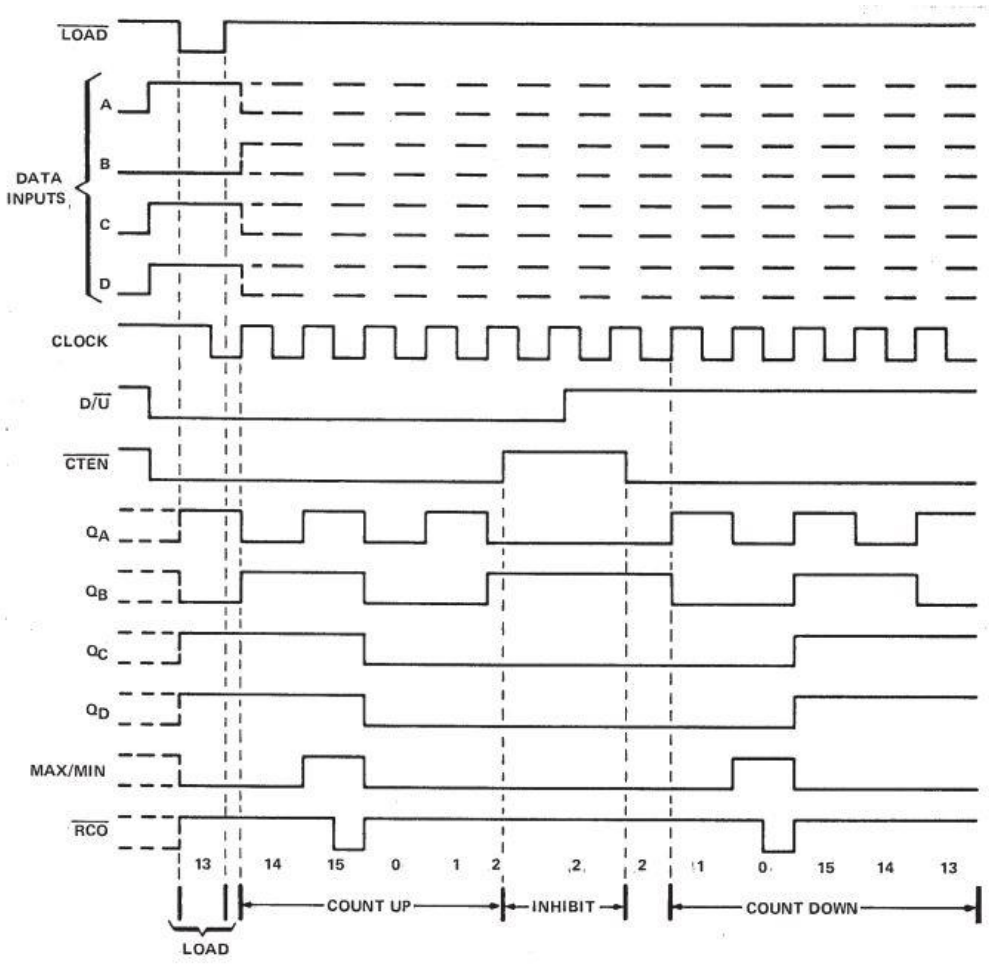
5. A 74LS191 counter IC is shown below (see the timing diagram below).



a) (10 pts) Draw VDD and GND signals and connect them to the load inputs, to load the value 0xD.

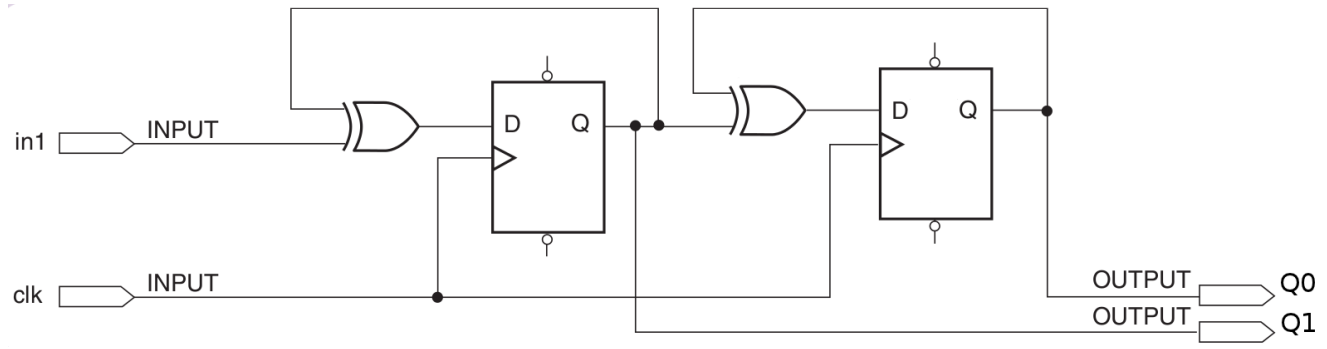
b) (10 pts) Draw a clock input and any other connections required to make this a down counter.

c) (10 pts) Add any logic that may be needed to count down from 0xD to 0x4 and then back to 0xD again.

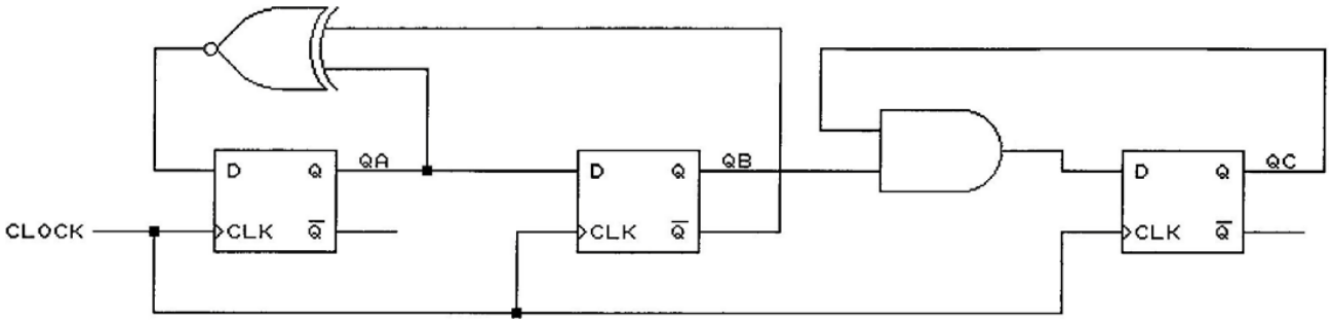


(Workspace for problem 5)

6. (10 pts) Create a next-state table for the circuit below. Preset and clear are each set to HIGH (Inactive).



7. (10 pts) For the schematic shown below QA = 0, QB = 1, and QC = 1. From this state, what are the next four states in the sequence?



011, _____, _____, _____, _____

8. EXTRA CREDIT (10 pts) Consider the 4-bit shift register on the right. Note the following:

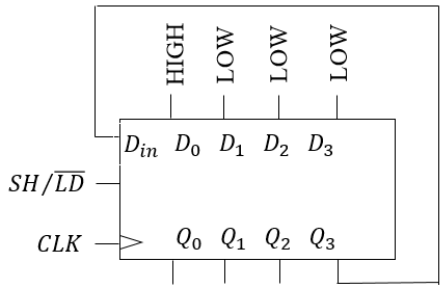
-Parallel inputs are labeled D_0 to D_3.

-Serial input is D_{in}, which is the input to the Q_0 flip-flop.

-Data shifts from Q_0 toward Q_3.

-Q's are initially 0.

-SH/LD is the (synchronous) shift/load input.



Complete the timing diagram below.