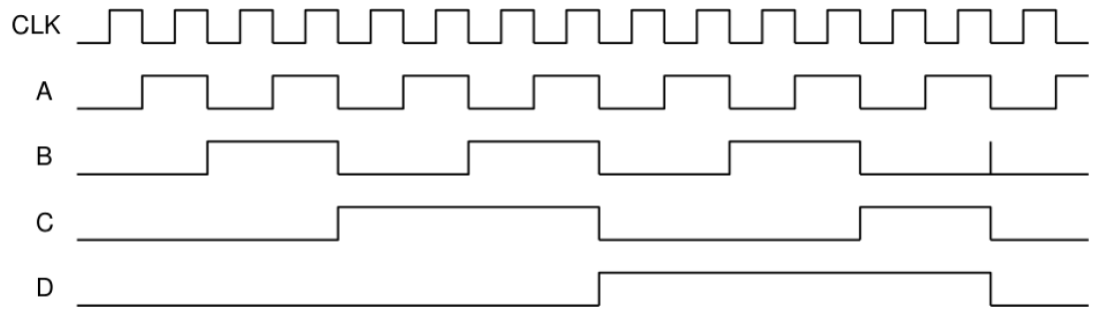
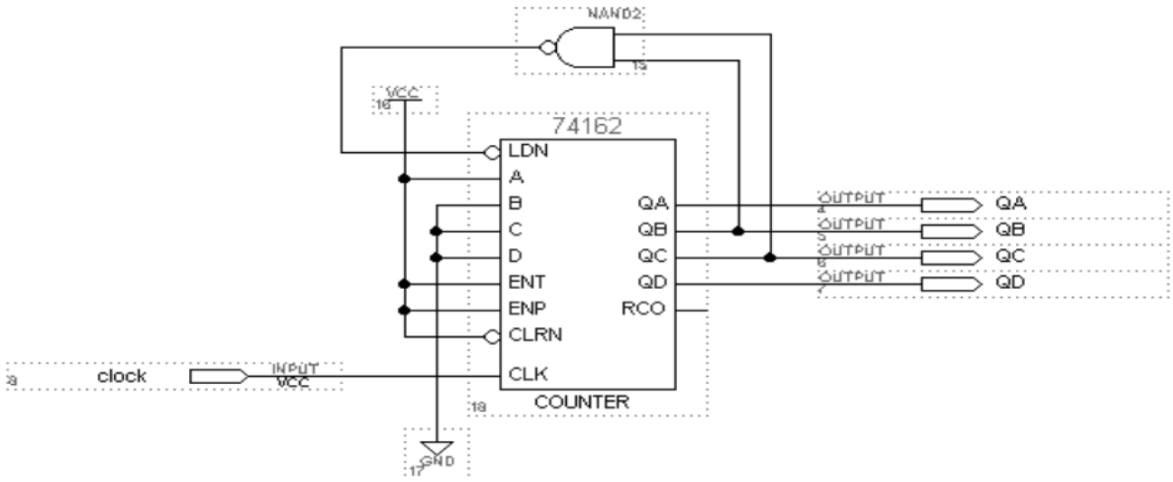
Homework 3

1. Draw a timing diagram for a 4-bit up counter.

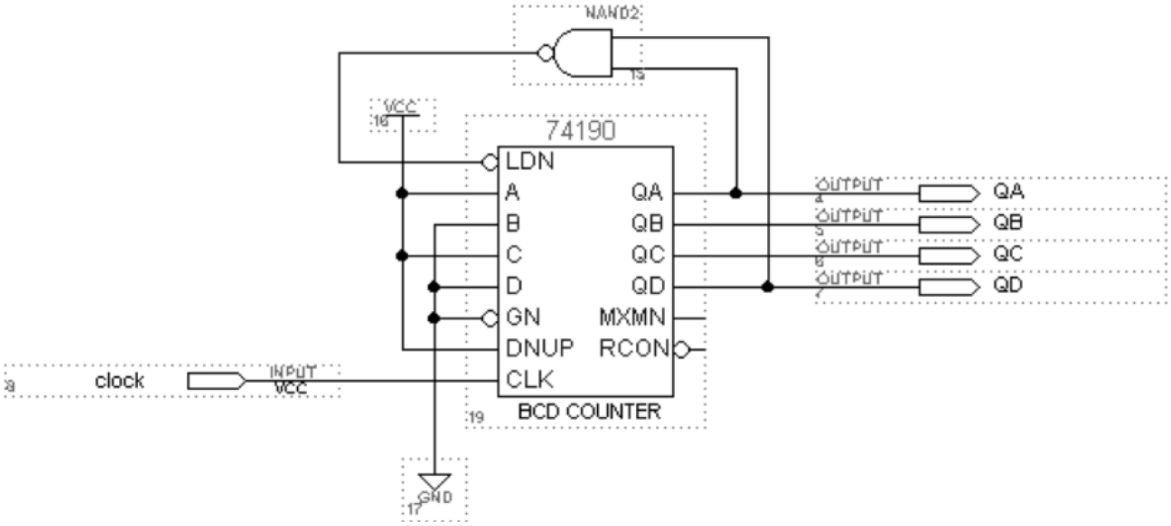


2. Determine the count sequence for the following schematic:



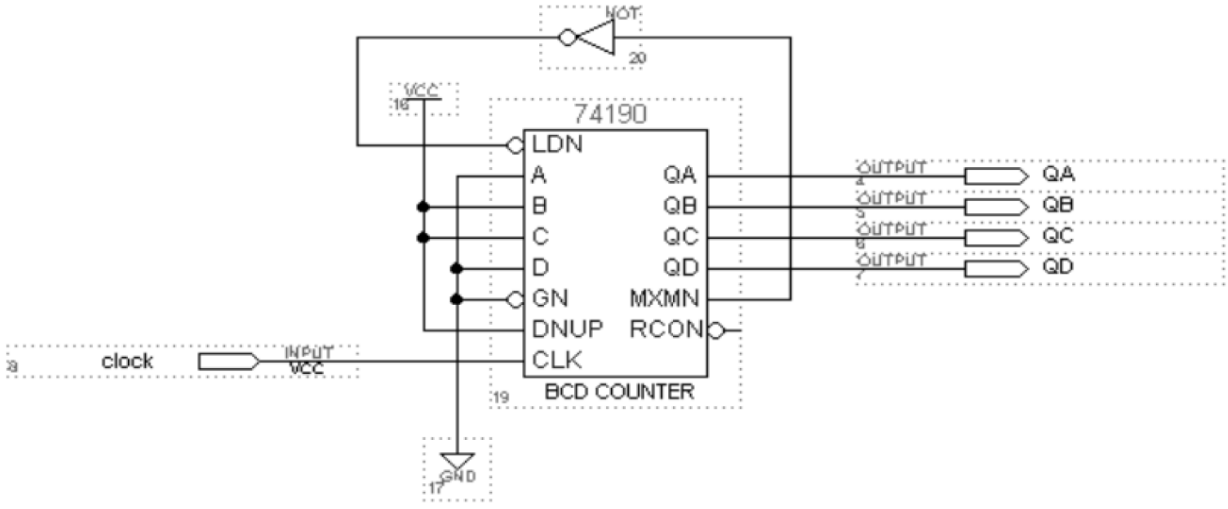
From the 74162 datasheet, A is the input LSB and QA is the output LSB. Since ENT and ENP are high, it is in a count-up mode. It will count from initial state 0001 = 0x1 (this is the pre-load) to 0110 = 0x6 (which drives the pre-load) and repeat.

3. Determine the count sequence for the following schematic:



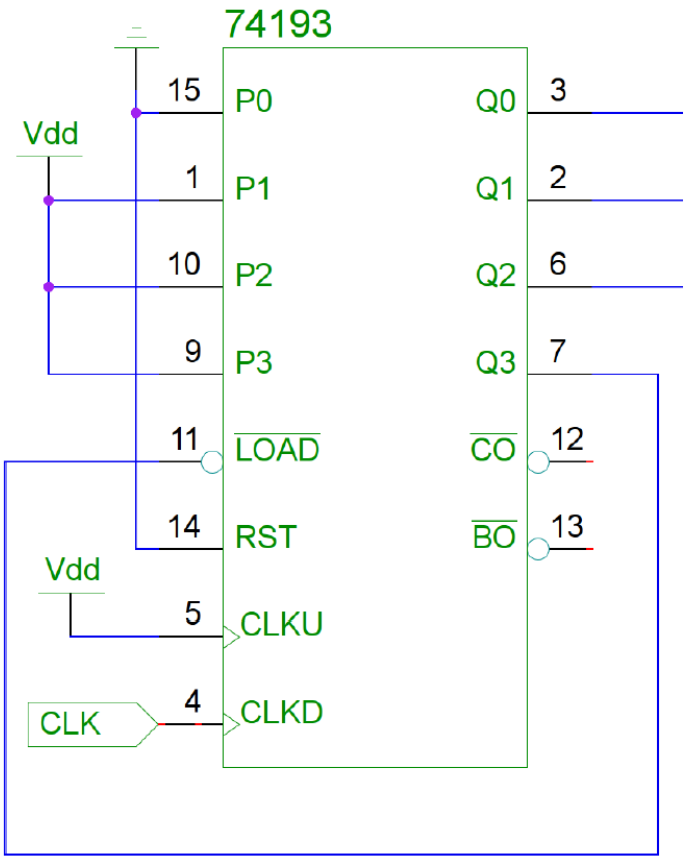
From the 74190 datasheet, A is the input LSB and QA is the output LSB. Since DNUP is high, it is in count-down mode. It will count from initial state 0101 = 0x5 (this is the pre-load) down to 1001 = 0x9 (which drives the pre-load) and repeat.

4. Determine the count sequence for the following schematic:

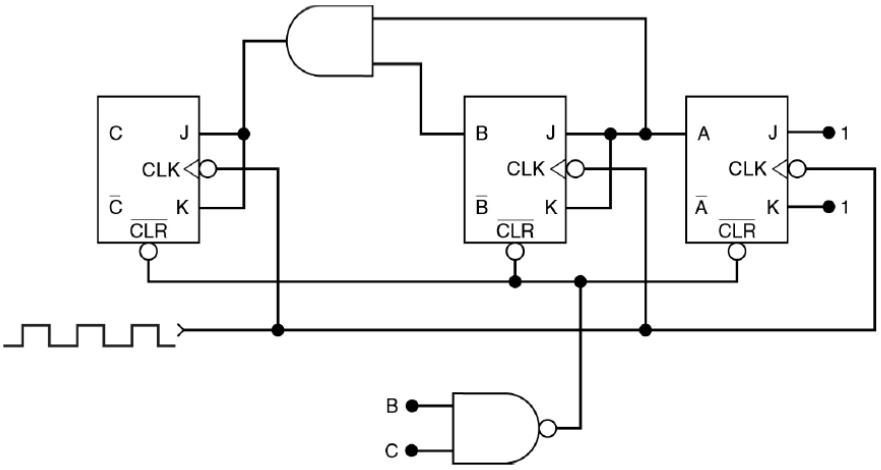


Again, the 74190 is in count-down mode. It will count from initial state 0110 = 0x6 (the pre-load) down to 0, at which point MXMN drives the pre-load and it repeats.

5. Draw a schematic using a 74193 that counts from 0xE to 0x8.



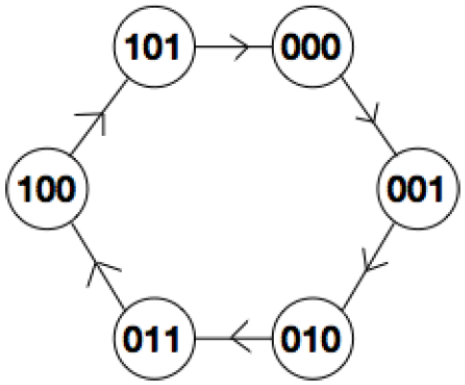
6. Consider the following schematic:



a) If the clock frequency is 11.0592 MHz, what is the frequency of A?

The first flip-flop is in toggle mode, so the frequency of A will be half that of the clock. F = 5.5296MHz.

b) Draw the state diagram.



c) If the clock frequency is 11.0592 MHz, what is the frequency of C?

This is a divide-by-six counter, so the frequency of C will be one sixth that of the clock. F = 1.8432MHz.

7. Describe what it means for a flip-flop to have a negative hold time.

A flip-flop with a negative hold time allows D to start changing before the clock edge arrives.