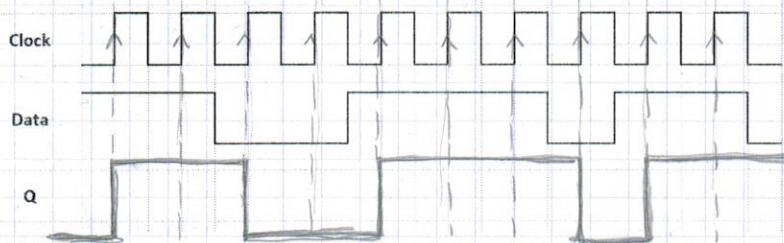
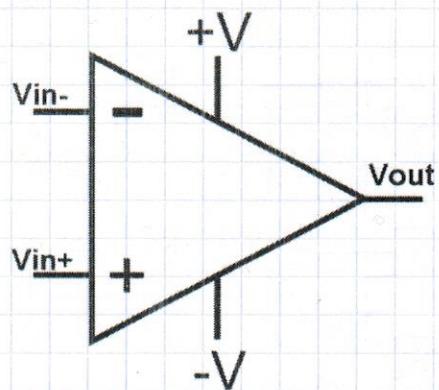


1. (5 pts) Draw the Q output for a D-type flip-flop with the following CLK and D inputs. The DFF is rising-edge-triggered. Assume that the Q output starts in the LOW state.



2. Rules for op-amps (great for D-A and A-D conversion):



a. (5 pts) Approximate input impedance for V_{in^-} and V_{in^+} : INFINITE

b. (5 pts) Approximate gain (amplification) of an op-amp: INFINITE

c. (5 pts) If the op-amp is configured correctly and V_{in^+} is grounded, what is the voltage measured at V_{in^-} ? _____

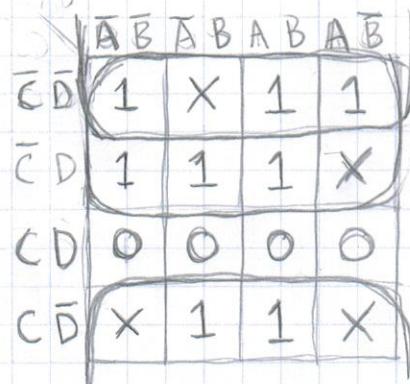
V_{in^-} WILL BE VIRTUAL GROUND

VOLTAGE AT V_{in^+} WILL BE THE SAME AS V_{in^-} .

3. For the truth table below:

Inputs				Output
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	X
0	0	1	1	0
0	1	0	0	X
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	X
1	0	1	0	X
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

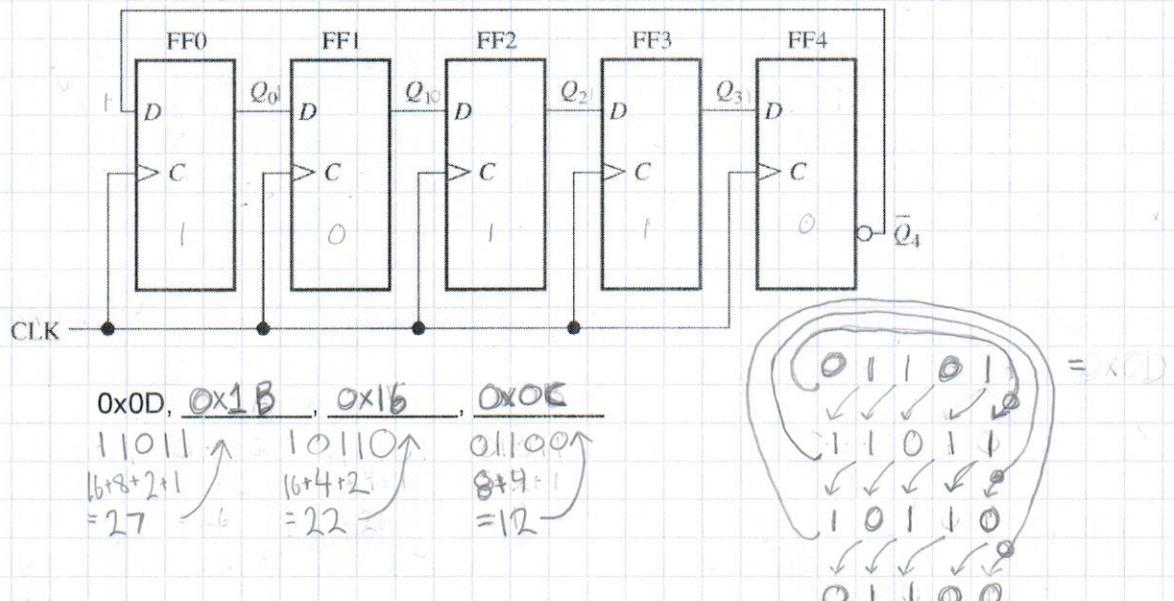
a. (10 pts) Draw the Karnaugh map.



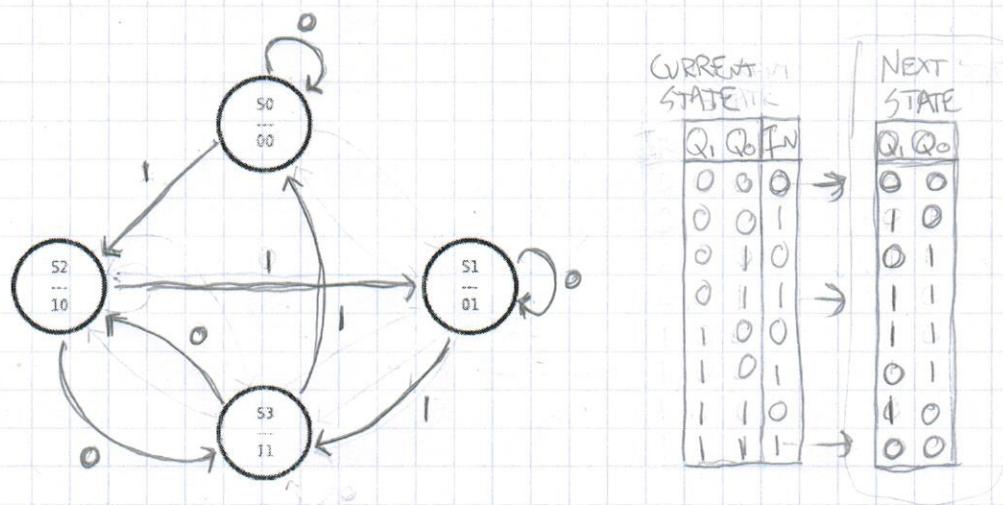
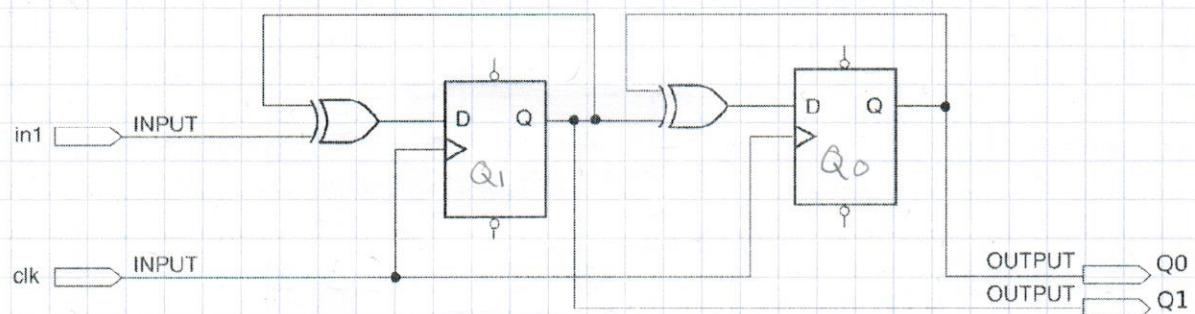
b. (5 pts) Write the minimized Boolean logic expression.

$$\bar{D} + \bar{C}D$$

4. (10 pts) For the circuit below: if the initial value of Q is 0x0D, what are the values (in hexadecimal) for the next three clock pulses? (Q₄ is the MSB.)



5. (15 pts) Draw the state diagram and the next-state table for the circuit below. (Q₀ is the LSB.)



CURRENT STATE

Q_1	Q_0	IN
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

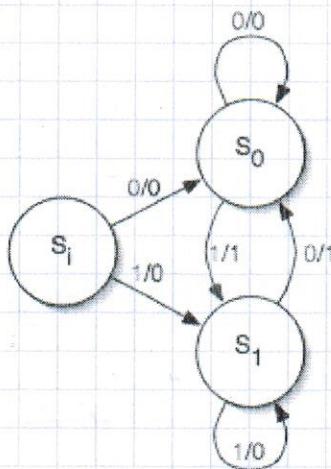
NEXT STATE

Q_1	Q_0
0	0
1	0
0	1
1	1
1	1
0	1
1	0
0	0

XOR

$0\ 0 \rightarrow 0$
$0\ 1 \rightarrow 1$
$1\ 0 \rightarrow 1$
$1\ 1 \rightarrow 0$

6. For the state diagram shown below:



- a. (10 pts) Does the state diagram represent a Moore machine or a Mealy machine? Explain your answer.

MEALY MACHINE

BECAUSE THERE IS BOTH AN INPUT AND OUTPUT

- b. (10 pts) How many flip-flops would be needed to implement this machine? Explain your answer.

1 FLIP FLOP IS NEEDED

BECAUSE IT IS ONLY 1 BIT

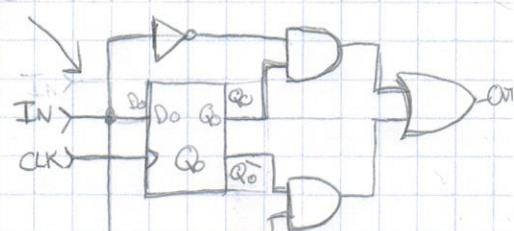
	Q_0 IN	D_o
s_1	X 0	0 0
	X 1	1 0
s_0	0 0	0 0
	0 1	1 1
s_1	1 0	0 1
	1 1	1 0

Q_0	IN	IN
Q0	0	1
	0	1

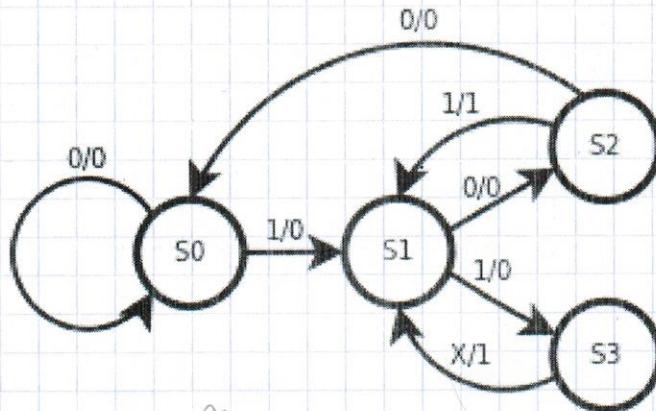
$$IN = D_o$$

Q_0	IN	IN
Q0	0	1
	1	0

$$\bar{Q}_0 \bar{I}N + Q_0 \bar{I}N = OUT$$



7. (20 pts) Design a state machine to implement the state diagram below. Include all the other state machine steps in the procedure. The last step in your procedure should be a schematic which uses D flip-flops. Show all the steps.



	CURRENT $Q_1\ Q_0\ IN$	NEXT $Q_1\ Q_0\ OUT$
S0	0 0 0	0 0 0
	0 0 1	0 1 0
	0 1 0	1 0 0
S1	0 1 1	1 1 0
	1 0 0	0 0 0
	1 0 1	0 1 1
S2	1 1 0	X X X
	1 1 1	X X X
S3		

D1	$\bar{Q}_1\ \bar{Q}_0$	$Q_1\ Q_0$	$\bar{Q}_1\ Q_0$	$Q_1\ \bar{Q}_0$
IN	0	1	X	0
IN	0	1	X	0

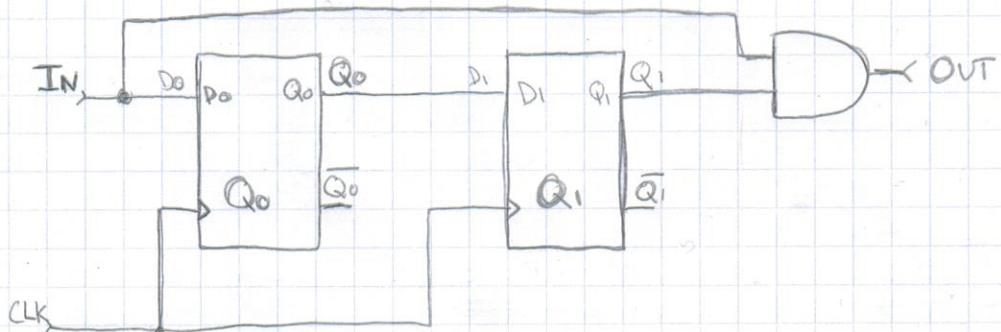
$$Q_0 = D_1$$

D0	$\bar{Q}_1\ \bar{Q}_0$	$\bar{Q}_1\ Q_0$	$Q_1\ Q_0$	$\bar{Q}_1\ Q_0$	$Q_1\ \bar{Q}_0$
IN	0	0	X	0	
IN	1	1	X	1	

$$IN = D_0$$

OUT	$\bar{Q}_1\ \bar{Q}_0$	$\bar{Q}_1\ Q_0$	$Q_1\ Q_0$	$\bar{Q}_1\ Q_0$	$Q_1\ \bar{Q}_0$
IN	0	0	X	0	
IN	0	0	X	1	

$$Q_1\ IN = OUT$$



8 4 2
0 0 0

8. (EXTRA CREDIT) Complete the following for a flash ADC:

- a. (2 pts) In general, how many comparators would be needed for a 12-bit flash ADC?

$$2^{12} - 1 = \\ 4096 - 1 = \boxed{4095}$$

- b. (2 pts) Name and describe an advantage of a flash ADC.

MUCH FASTER, BUT TAKES UP MORE SPACE,

- c. (6 pts) Draw a schematic of a 3-bit flash ADC that shows how all the important components are connected.

