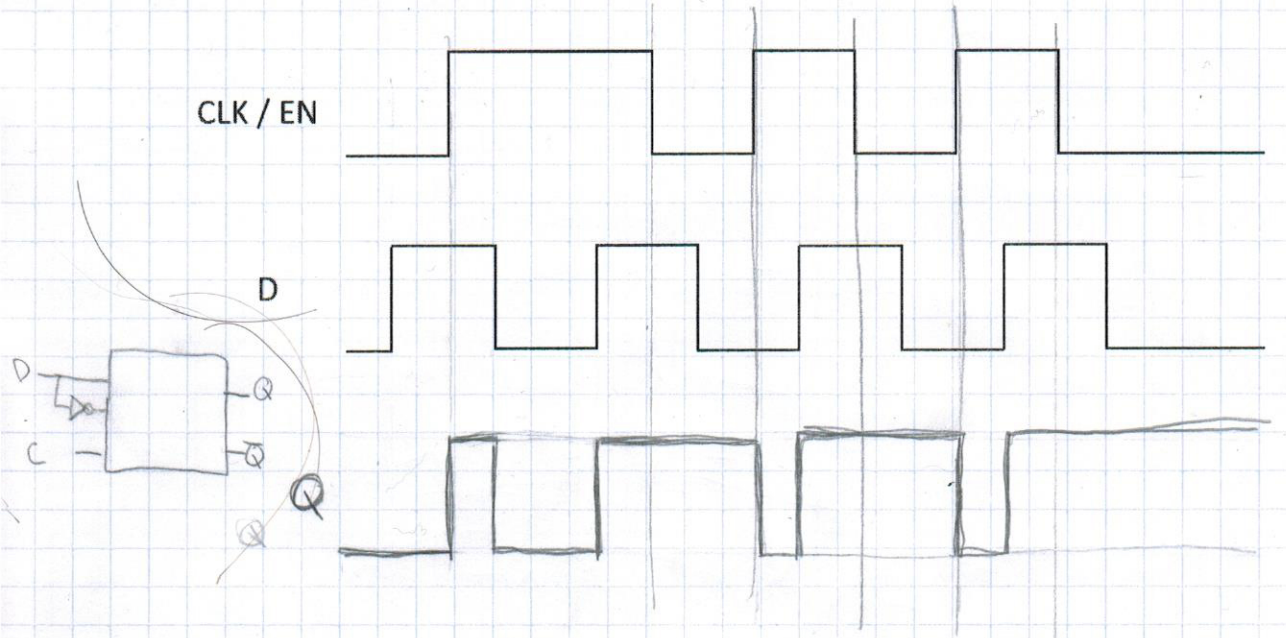
EET 122 **4/16/20**

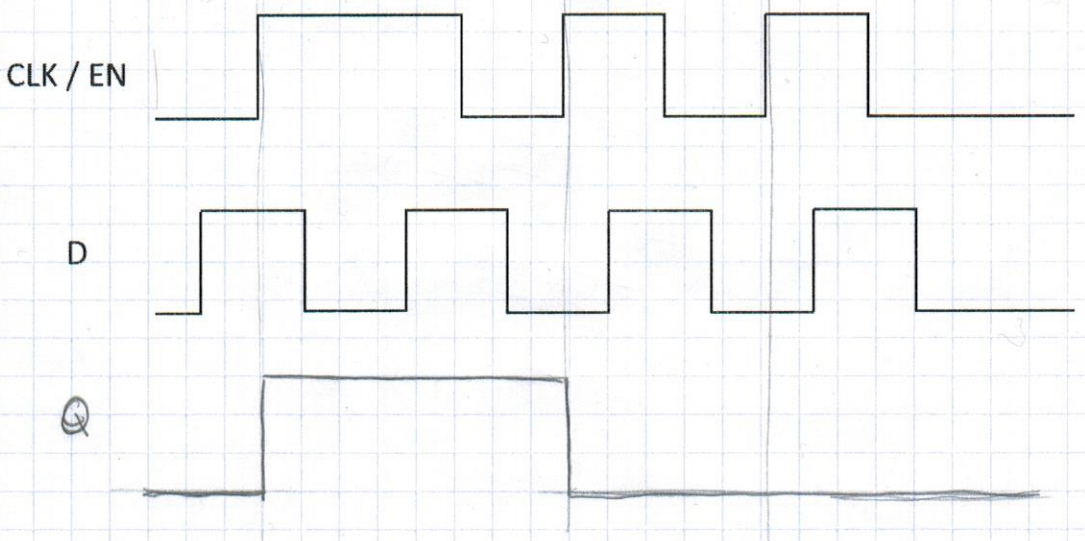
Quiz 1

Name: ZACH D'AGOSTINO

1. (2 pts) Given the input waveforms shown below, sketch the output Q of a D latch.



2. (2 pts) Using the same input waveforms from problem 1, sketch the output Q of a D flip-flop.



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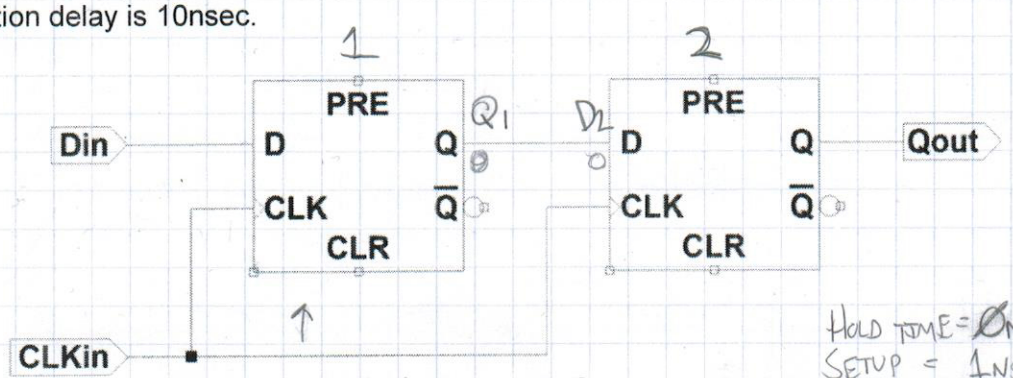
Quiz 1

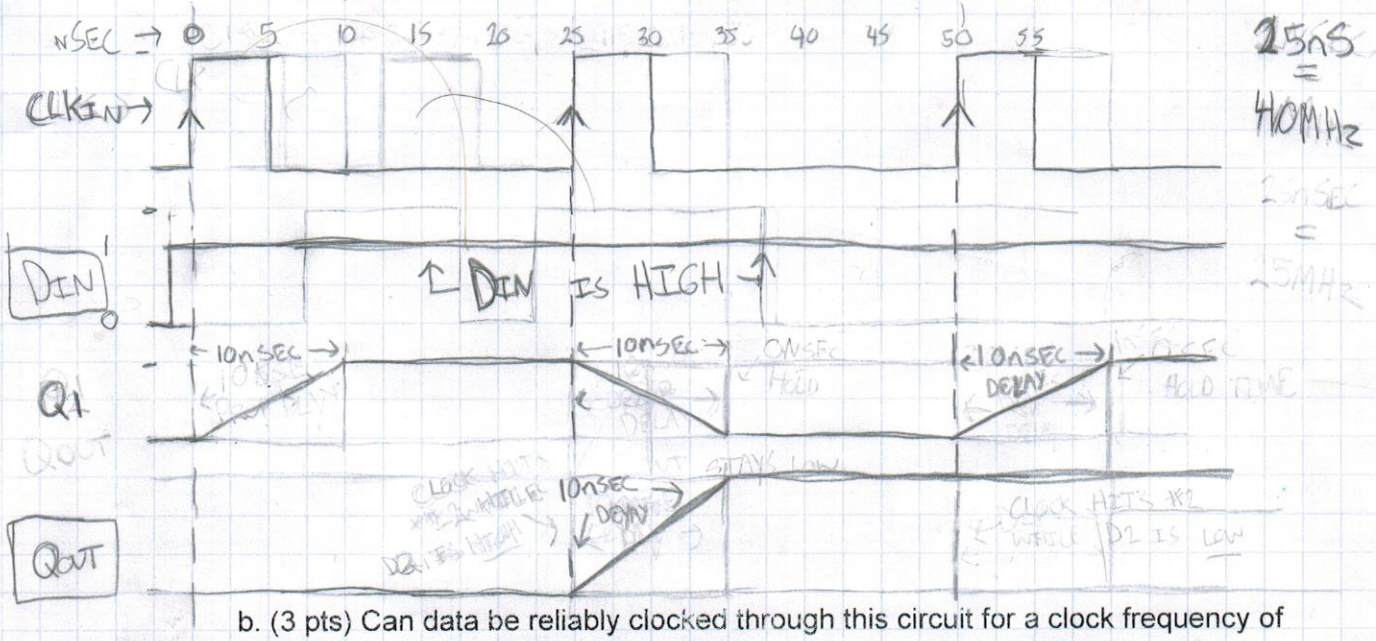
3. For both flip-flops in the circuit below, the setup time is 1nsec, the hold time is 0nsec, and the propagation delay is 10nsec.



HOLD TIME = 0NSEC
SETUP = 1NSEC
PROPDLY = 10NSEC

$CLK \rightarrow Q1 = \frac{CLK}{2} \rightarrow Q2 = \frac{Q2}{2} = \frac{CLK}{4}$

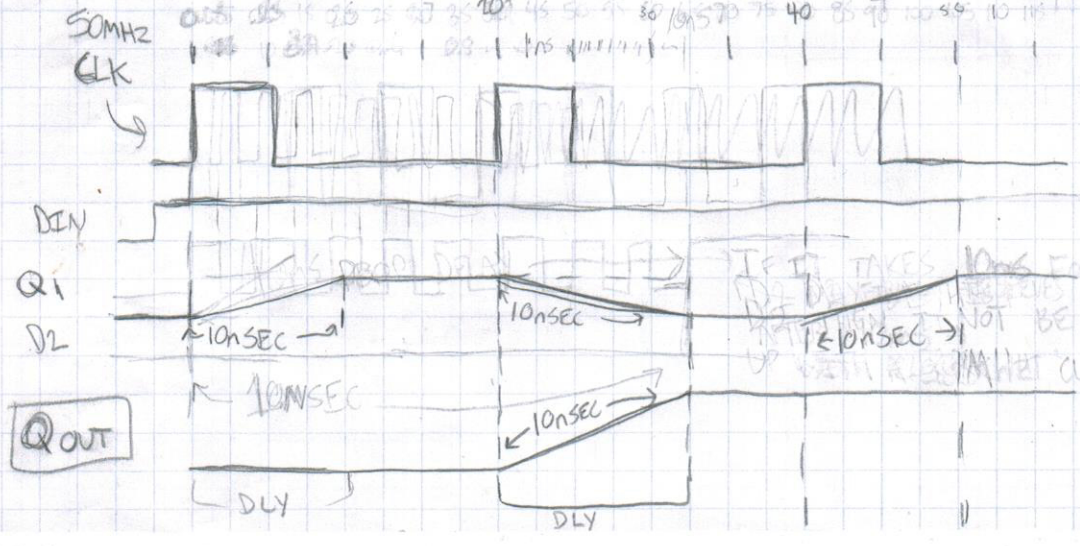
a. (3 pts) Draw a timing diagram showing two clock periods, the data input Din, and the data output Qout. Assume a clock period of 25nsec. Label all delays in nsec.



b. (3 pts) Can data be reliably clocked through this circuit for a clock frequency of 50MHz? Draw a timing diagram to explain your answer, labeling all delays in nsec.

50MHz = 20nSEC

$CLK \rightarrow Q1 = \frac{CLK}{2} \rightarrow Q2 = \frac{Q2}{2} = \frac{CLK}{4} \rightarrow \frac{50MHz}{4} = 12.5MHz$



YES, DATA CAN BE RELIABLY CLOCKED THROUGH THIS CIRCUIT.