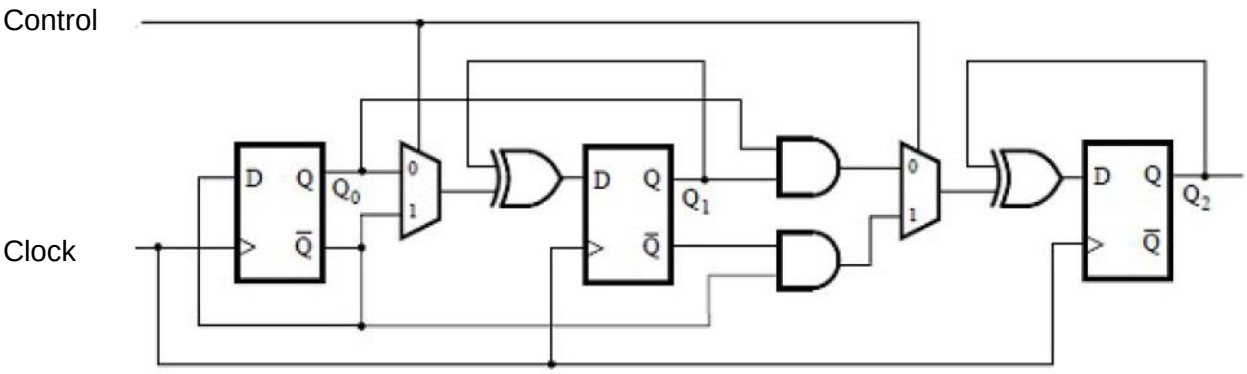
Homework 2

1. The following schematic has two inputs, a clock and a control signal (the MUX inputs). Determine the Q-bit sequence for this circuit for each control signal possibility.



This is a 3-bit counter (000, 001, 010, 011,...) with multiplexers to control if it counts up or down.

First stage: Q_0 is a divide-by-two.

Second stage: Q_1 toggles if previous Q_0 is high (count up) or if previous Q_0 is low (count down).

Third stage: Q_2 toggles if previous Q_1 and Q_0 are high (count up) or if previous Q_1 and Q_0 are low (count down) .

2. The following questions refer to a 3-bit up counter:

a) If the counter starts at 000, what will the counter be after 13 clock pulses?

101

b) If the counter starts at 000, what will the counter be after 99 clock pulses?

011

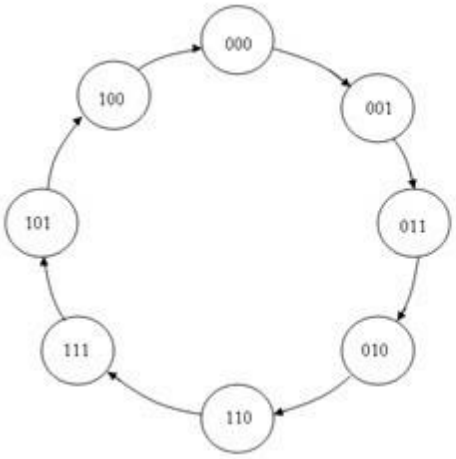
c) If the counter starts at 000, what will the counter be after 256 clock pulses?

000

d) If the clock is 16 MHz, what is the frequency of the Q-bit of the MSB?

16MHz / 8 = 2MHz

3. Draw the state diagram for a 3-bit Gray code sequence.



Present State			Next State		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

4. Suppose a ring oscillator is built from N inverters connected in a loop. Each inverter has a minimum delay of t_{cd} and a maximum delay of t_{pd}. If N is odd, determine the range of frequencies at which the oscillator might operate.

Total delay through N stages: Nt_{cd} (minimum), Nt_{pd} (maximum).

Note that the ring oscillator will transition high-to-low or low-to-high after this total delay. Therefore, a total period will be twice this delay, and

$2\,Nt_{cd} < T < 2\,Nt_{pd}$

Therefore, since the frequency is 1/T,

Frequency: $1/(2Nt_{pd}) < f < 1/(2Nt_{cd})$

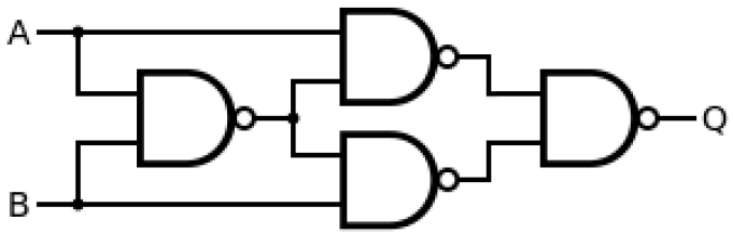
5. Why must N be odd in problem 5?

If N is even the ring is stable and will not oscillate.

6. You are designing an elevator controller for a building with 25 floors. The controller has two inputs: UP and DOWN. It produces an output indicating the floor that the elevator is on. There is no floor 13 (bad luck, you know). What is the minimum number of bits of state in the controller?

There are a total of 24 floors in the building (24 – 1). Therefore it needs 24 states. For 24 states, you need 5 bits (4 bits would only allow $2^4 = 16$ states, but 5 bits allow $2^5 = 32$ states).

7. Sketch a schematic for a two-input XOR function using only NAND gates. What is the smallest number of NAND gates that you need?



Four is the minimum number of NAND gates needed.

8. What is the difference between a latch and a flip-flop? Under what circumstances is each one preferable?

A latch is level sensitive and a FF is edge sensitive. FF are used to ensure data movements are precisely timed. Latches are generally smaller.