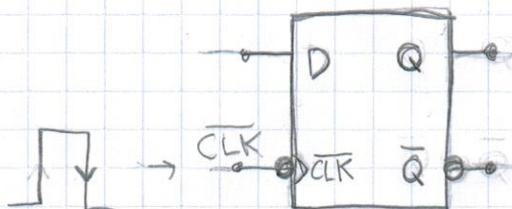


1. Draw the following for a D-type flip-flop (DFF):

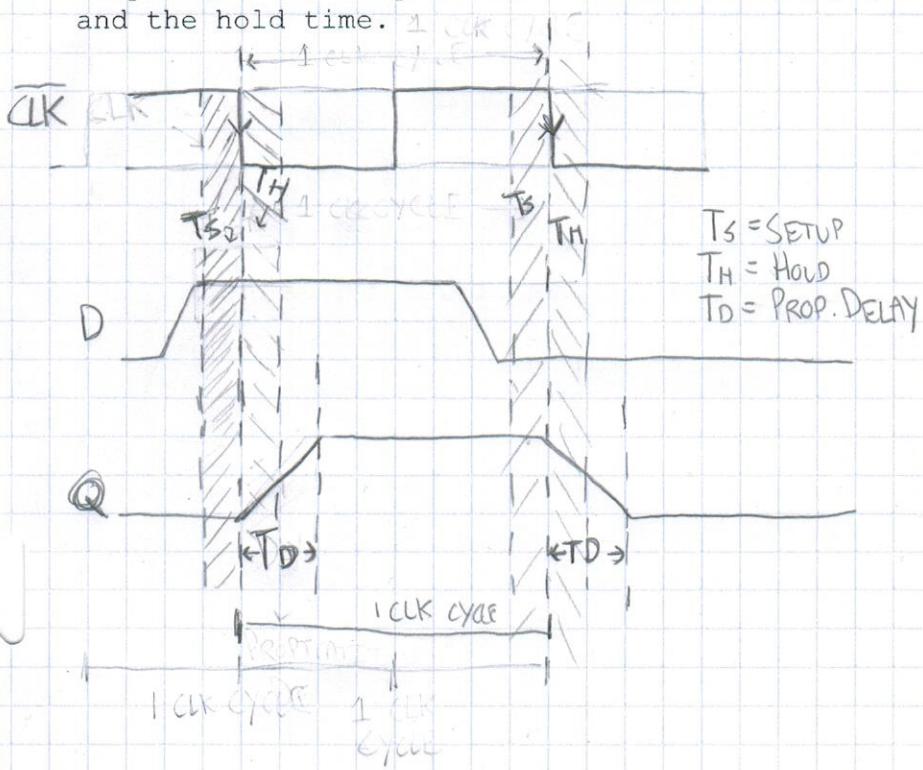
a) (5 pts) The symbol with a falling edge clock input



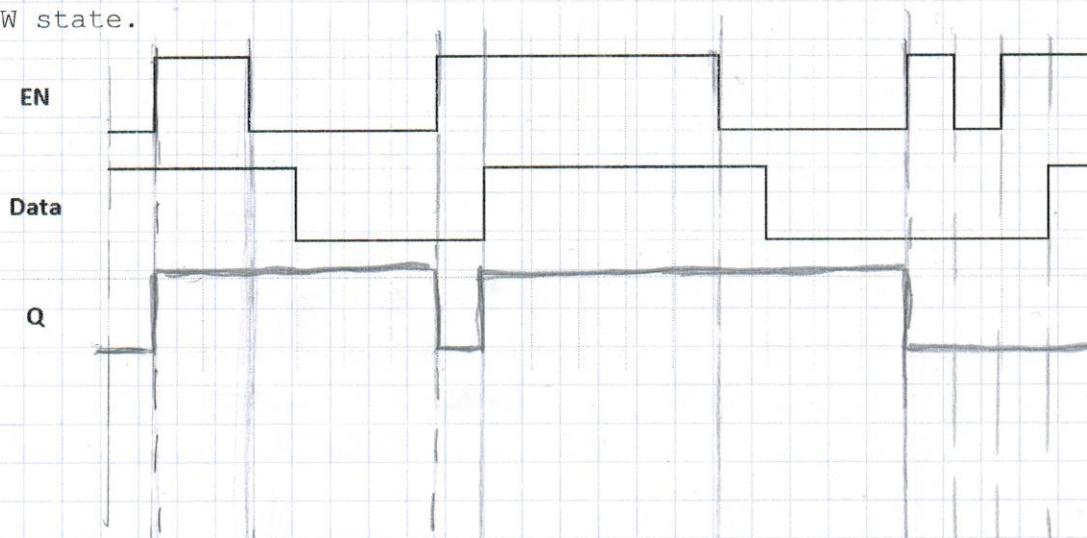
b) (5 pts) The truth/function table

D	$\bar{CLK}$	$Q$	$\bar{Q}$
0	↓	0	1
1	↓	1	0

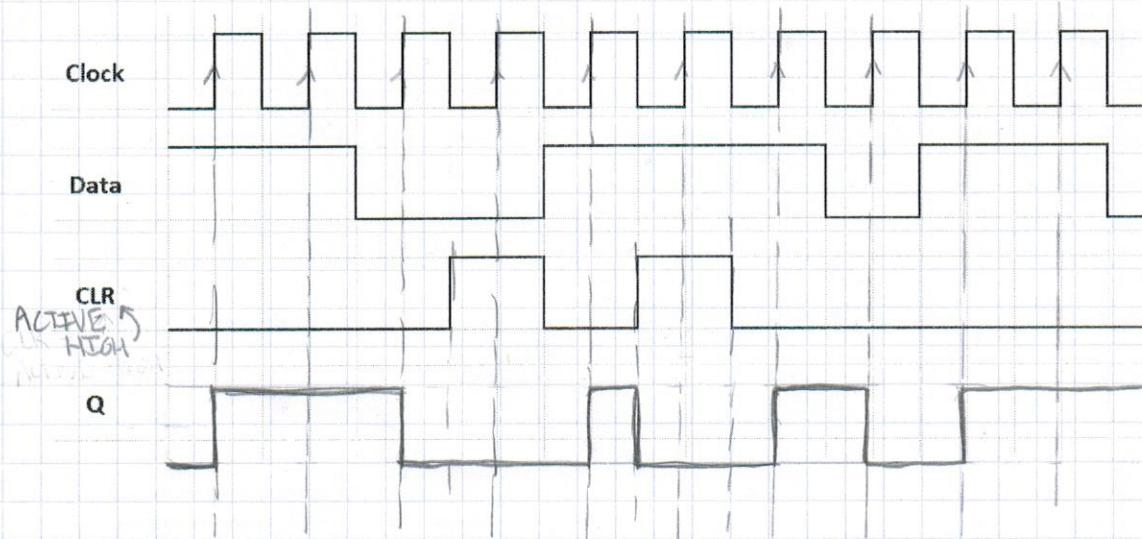
c) (5 pts) A timing diagram showing one clock cycle, the input D, and the output Q. The diagram must include the propagation delay, the setup time, and the hold time.



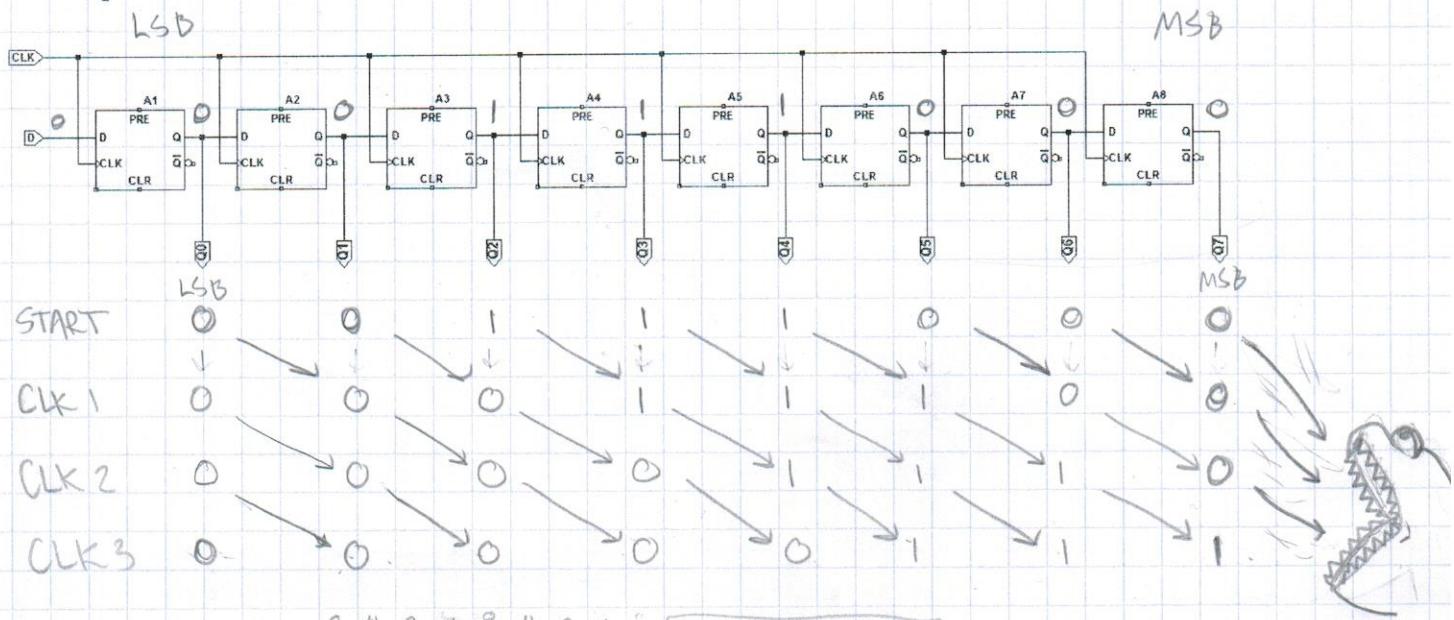
2. (10 pts) Draw the Q output for a D-type latch with the following EN and D inputs. The EN input is active HIGH. Assume that the Q output starts in the LOW state.



3. (10 pts) Draw the Q output for a D-type flip-flop with the following CLK/EN and D inputs. The DFF is rising-edge-triggered. Assume that the Q output starts in the LOW state. The CLR input is asynchronous.



4. (15 pts) Consider the shift register below, where D = 0, and Q0 is the LSB. Assume that all of the preset (PRE) and clear (CLR) inputs are inactive. If the initial value of Q is 0X1C (Q0, the furthest to the left, is the LSB), what are the hex values (states) for each of the next three clock pulses?



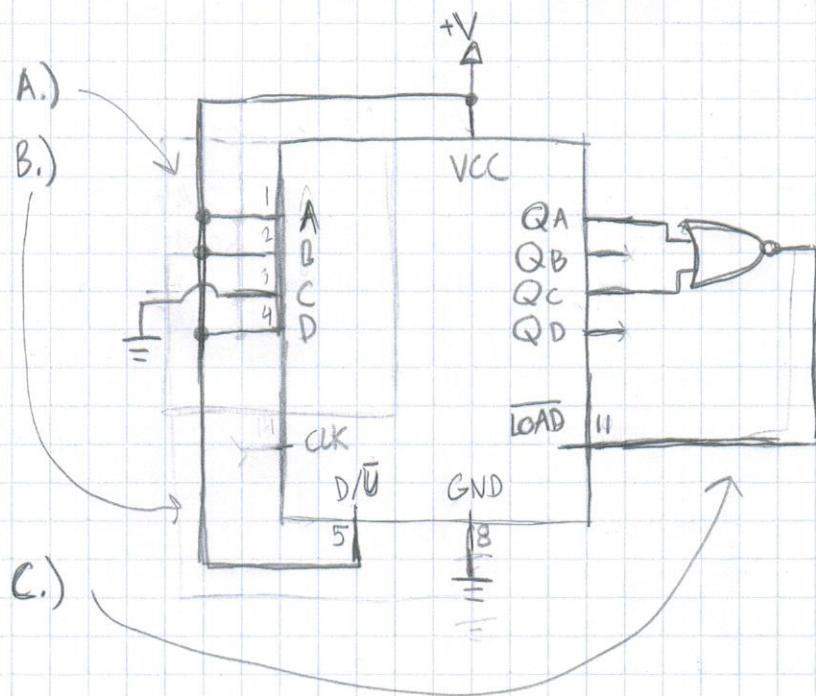
$$\begin{aligned}
 \text{START} &= 0000111000 = 1C \rightarrow 0X1C \\
 \text{CLK 1} &\rightarrow 0011110000 = 38 \rightarrow 0X38 \\
 \text{CLK 2} &\rightarrow 0111100000 = 90 \rightarrow 0X90 \\
 \text{CLK 3} &\rightarrow 1111000000 = E0 \rightarrow 0XE0
 \end{aligned}$$

(Workspace for problem 5)

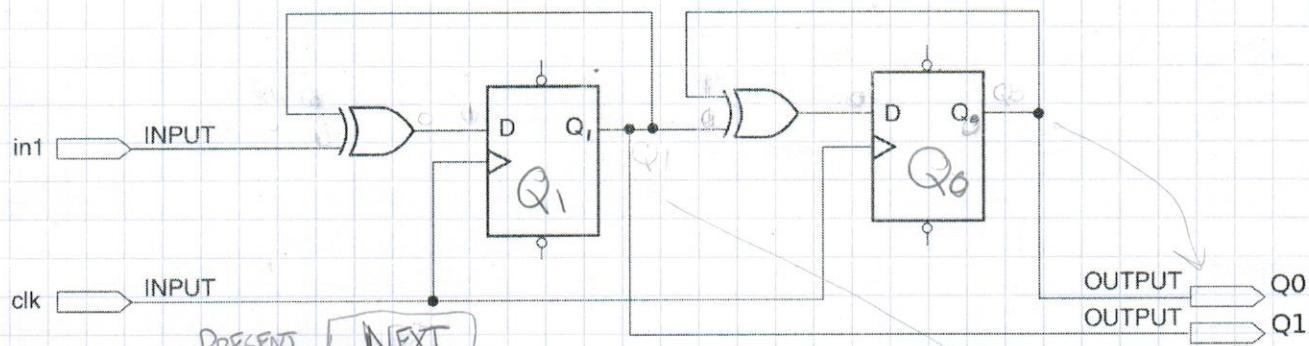
$$0XD = 13 = A \ 1 \ 0 \ 1$$

$$\begin{array}{r} 8 \ 4 \ 2 \ 1 \\ Q_A \ Q_B \ Q_C \ Q_D \\ \text{LOAD} \ 1 \ 1 \ 0 \ 1 = 0XD \\ 1 \ 1 \ 0 \ 0 \\ 1 \ 0 \ 1 \ 1 \\ 1 \ 0 \ 1 \ 0 \\ 1 \ 0 \ 0 \ 1 \\ 1 \ 0 \ 0 \ 0 \\ 0 \ 1 \ 1 \ 1 \\ 0 \ 1 \ 1 \ 0 \\ 0 \ 1 \ 0 \ 1 \\ \boxed{0 \ 1 \ 0 \ 0} = 0X4 \\ \text{A} \backslash \text{C} \end{array}$$

UNIQUE PATTERN

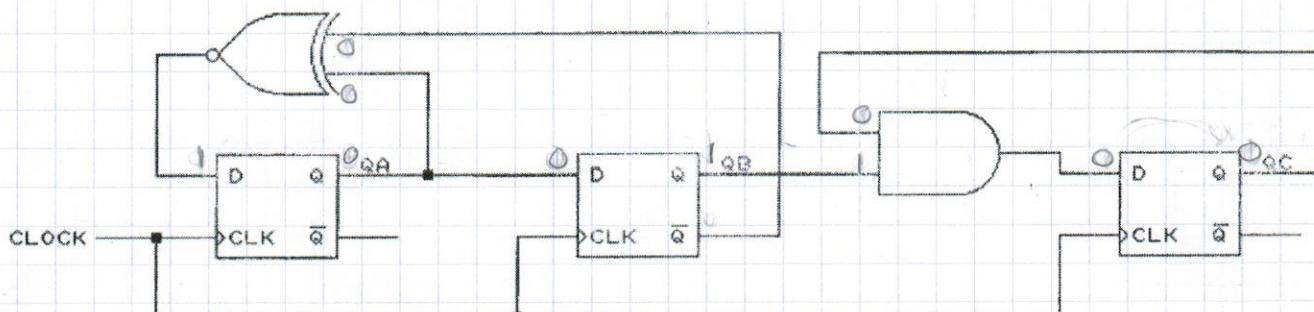


6. (10 pts) Create a next-state table for the circuit below. Preset and clear are each set to HIGH (Inactive).



PRESENT		NEXT
IN	Q <sub>1</sub> Q <sub>0</sub>	Q <sub>1</sub> Q <sub>0</sub>
XOR	0 0   0	0 0   0
0 0   0	0 0   0	0 0   0
1 0   1	0 0   1	0 1   1
0 1   1	0 1   0	1 1   1
1 1   0	0 1   1	1 0   0
	1 0   0	1 0   0
	1 0   1	1 1   1
	1 1   0	0 1   1
	1 1   1	0 0   0

7. (10 pts) For the schematic shown below QA = 0, QB = 1, and QC = 1. From this state, what are the next four states in the sequence?

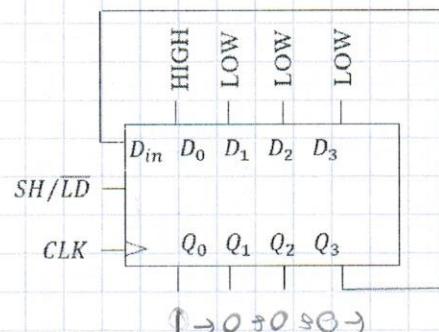


011, 101, 110, 010, 100

XNOR	
0 0	1
1 0	0
0 1	0
1 1	1

8. EXTRA CREDIT (10 pts) Consider the 4-bit shift register on the right.  
 Note the following:

- Parallel inputs are labeled  $D_0$  to  $D_3$ .
- Serial input is  $D_{in}$ , which is the input to the  $Q_0$  flip-flop.
- Data shifts from  $Q_0$  toward  $Q_3$ .
- $Q$ 's are initially 0.
- SH/LD is the (synchronous) shift/load input.



Complete the timing diagram below.

