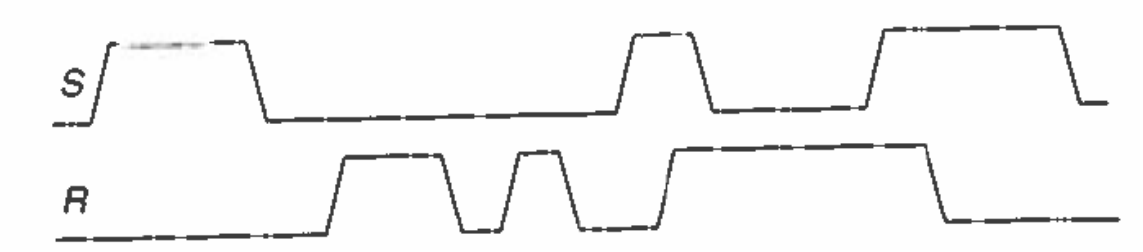
Homework 1

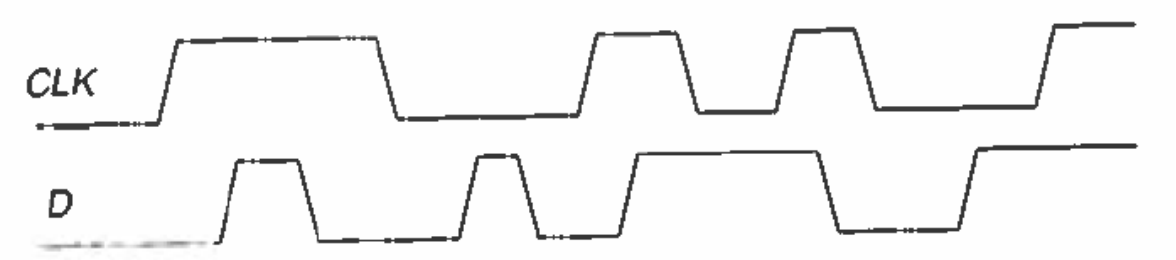
1. Starting with the schematic of an SR flip-flop, show how it can be wired so that on the rising edge of the clock pulse the Q output toggles.

2. Starting with the schematic of a D flip-flop (DFF) show how it can be wired so that on the rising edge of the clock pulse the Q output toggles.

3. Given the input waveforms shown below, sketch the output Q of an SR latch.



4. Given the input waveforms shown below, sketch the output Q of a D latch.



5. Using the same input waveforms from problem 4, sketch the output Q of a D flip-flop.