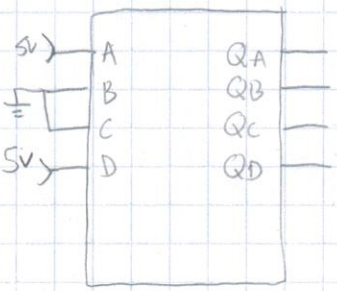
Homework 5 (Problem 2 on other side!)

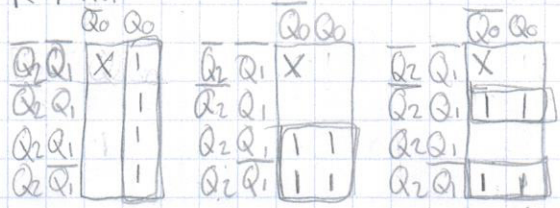
1. Design a counter to produce the following binary sequence (use D flip-flops): 9, 12, 11, 13, 15, 14, 10, 9,...

8	4	2	1	
Q_3	Q_2	Q_1	Q_0	
1	0	0	1	= 9
1	1	0	0	= 12
1	0	1	1	11
1	1	0	1	13
1	1	1	1	15
1	1	1	0	14
1	0	1	0	10
1	0	0	1	9



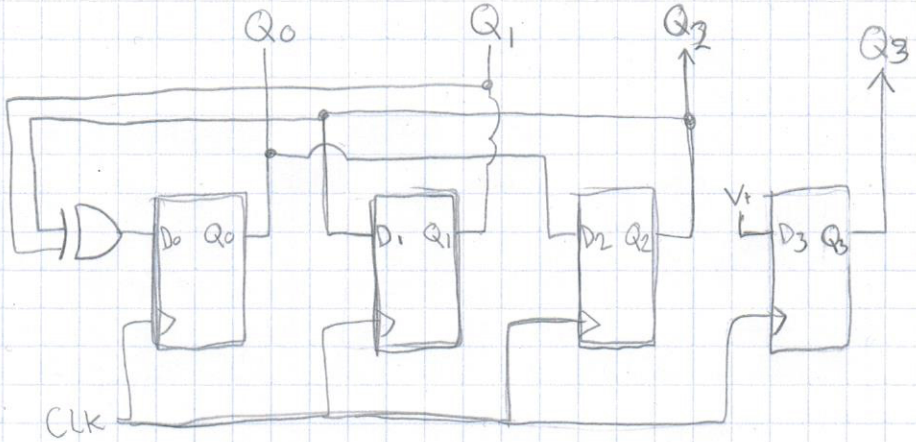
Q_2	Q_1	Q_0		Q_2	Q_1	Q_0
0	0	0	→	X	X	X
0	0	1	→	1	0	0
0	1	0	→	0	0	1
0	1	1	→	1	0	1
1	0	0	→	0	1	1
1	0	1	→	1	1	1
1	1	0	→	0	1	0
1	1	1	→	1	1	0
				D_2	D_1	D_0

K-MAP



$D_2 = Q_0$ $D_1 = Q_2$ $D_0 = \overline{Q_2}\,Q_1 + Q_2\,\overline{Q_1}$

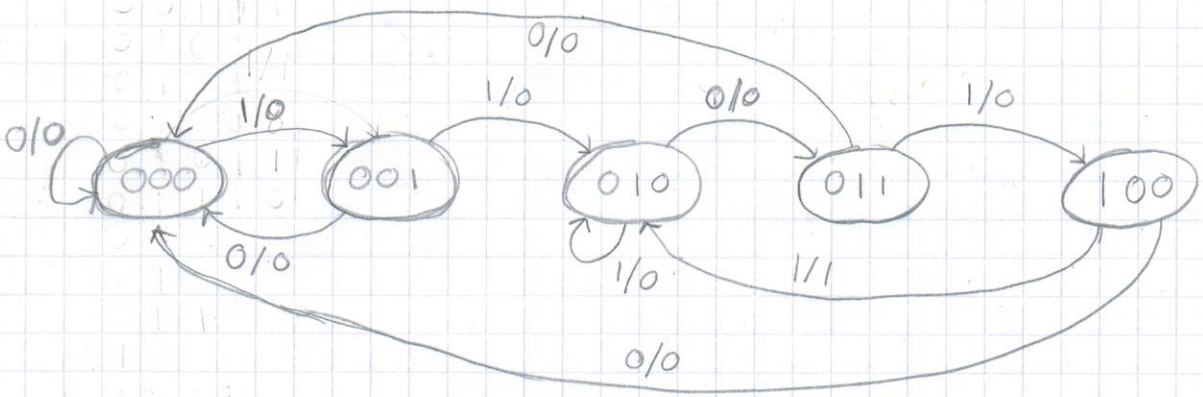
$D_0 = Q_2 \oplus Q_1$



2. Design a Mealy circuit to find the pattern ...11011... in a series of binary numbers, where each new bit appears on the input to the circuit with each clock pulse. An output should be switched to high when the last number in the pattern is detected. Allow overlapping patterns.

1 1 0 1 1 — 5 STATES →

	Q_2	Q_1	Q_0	A
0	0	0	0	
1	0	0	1	
2	0	1	0	
3	0	1	1	
4	1	0	0	



$D_0 = Q_1\overline{Q_0}A + Q_2Q_1$

Q_2Q_1 \ Q_0A	$\overline{Q_0}A$	$\overline{Q_0}\overline{A}$	Q_0A	$Q_0\overline{A}$
$\overline{Q_2}\overline{Q_1}$	0	1	0	0
$\overline{Q_2}Q_1$	1	0	0	0
Q_2Q_1	X	X	X	X
$Q_2\overline{Q_1}$	0	0	X	X

$D_1 = Q_1\overline{Q_0} + Q_2A + \overline{Q_1}Q_0A$

Q_2Q_1 \ Q_0A	$\overline{Q_0}\overline{A}$	$\overline{Q_0}A$	Q_0A	$Q_0\overline{A}$
00			1	
01	1	1		
11	X	X	X	X
10		1	X	X

$D_2 = Q_1Q_0A$

Q_2Q_1 \ Q_0A	$\overline{Q_0}\overline{A}$	$\overline{Q_0}A$	Q_0A	$Q_0\overline{A}$
00				
01			1	
11	X	X	X	X
10			X	X

OUTPUT → $Q_2\overline{Q_1}\overline{Q_0}A$

Q_2Q_1 \ Q_0A	$\overline{Q_0}\overline{A}$	$\overline{Q_0}A$	Q_0A	$Q_0\overline{A}$
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	1	0	0

Q_2	Q_1	Q_0	IN		Q_1	Q_0		OUT
0	0	0	0	→	0	0	0	0
0	0	0	1	→	0	0	1	0
0	0	1	0	→	0	0	0	0
0	0	1	1	→	0	1	0	0
0	1	0	0	→	0	1	1	0
0	1	0	1	→	0	1	0	0
0	1	1	0	→	0	0	0	0
0	1	1	1	→	1	0	0	0
1	0	0	0	→	0	0	0	0
1	0	0	1	→	0	1	0	1
1	0	1	0		X	X	X	
1	0	1	1		X	X	X	
1	1	0	0		X	X	X	
1	1	0	1		X	X	X	
1	1	1	0		X	X	X	
1	1	1	1		X	X	X	