调试记录：

2019-05-27：R288 改为 11K

Title	<Title>	
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24V->IN12V->1.2V->1.8V->3.3V

Title	<Title>	
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[9,10] DSP_EMA_A[14:0] — DSP_EMA_A[14:0]

[9,10] DSP_EMA_D[15:0] — DSP_EMA_D[15:0]

[9] DSP_EMA_WAIT0 — DSP_EMA_WAIT0
[10] DSP_EMA_WAIT1 — DSP_EMA_WAIT1
[9,10] DSP_EMA_OEn — DSP_EMA_OEn
[10] DSP_EMA_CS2n — DSP_EMA_CS2n
[9] DSP_EMA_CS3n — DSP_EMA_CS3n
[10] DSP_EMA_CS4n — DSP_EMA_CS4n
[10] DSP_EMA_CS5n — DSP_EMA_CS5n

[9,10] DSP_EMA_WEn — DSP_EMA_WEn

[10] DSP_EMA_A_RW — DSP_EMA_A_RW
[10] DSP_EMA_BA0 — DSP_EMA_BA0
[10] DSP_EMA_BA1 — DSP_EMA_BA1

[21] DSP_RESETn — DSP_RESETn
[10] DSP_RESETOUTn — DSP_RESETOUTn

[21] DSP_CLK — DSP_CLK

[11] FPGA_DONE — FPGA_DONE

U1A

DSP_RESETn — K14 RESET#
R1 10K DSP_RESETOUTn — T17 RESETOUT#/UHPI_HAS#/PRU1_R30[14]/GP6[15]
VDD3V3 R2 10K — J17 NMI#
DSP_CLK — L19 OSCIN
K19 OSCOUT
L18 OSCVSS
TP1 OCLK 1 — T18 CLKOUT/UHPI_HDS2#/PRU1_R30[13]/GP6[14]
DSP_PLL_VDDA 1.2V — L15 PLL0_VDDA
M17 PLL0_VSSA
N15 PLL1_VDDA
M15 PLL1_VSSA

EMA_CS0:SDRAM
EMA_CS2:NOR FLASH
EMA_CS3:NAND_FLASH

VDD3V3 R3 4.7K DSP_EMA_CS2n — A18 EMA_CS[0]#/GP2[0]
R4 4.7K DSP_EMA_CS3n — B17 EMA_CS[2]#/GP3[15]
R5 4.7K DSP_EMA_CS4n — A17 EMA_CS[3]#/GP3[14]
R6 4.7K DSP_EMA_CS5n — F9 EMA_CS[4]#/GP3[13]
B16 EMA_CS[5]#/GP3[12]

DSP_EMA_A_RW — D10 EMA_A_RW/GP3[9]
VDD3V3 R7 4.7K DSP_EMA_OEn — B15 EMA_OE#/GP3[10]

B7 EMA_CLK/PRU0_R30[5]/GP2[7]/PRU0_R31[5]

DSP_EMA_WAIT0 — B18 EMA_WAIT[0]/PRU0_R30[0]/GP3[8]/PRU0_R31[0]
DSP_EMA_WAIT1 — B19 EMA_WAIT[1]/PRU0_R30[1]/GP2[1]/PRU0_R31[1]

RTC_VSS C1 22pF — J19 RTC_XI
H19 RTC_XO
Y1 FX135A-327
C2 22pF — H18 RTC_CVDD
RTC_CVDD R8 0R — L14 RTC_VSS
F4 RTC_ALARM/UART2_CTS#/GP0[8]/DEEPSLEEP#
RTC_VSS — E9 MMCSD0_CLK/PRU1_R30[31]/GP4[7]
F1 MMCSD1_DAT[7]/PRU1_R30[7]/GP8[11]
FPGA_DONE R9 0R — F2 MMCSD1_DAT[6]/PRU1_R30[6]/GP8[10]/PRU1_R31[7]
H4 MMCSD1_DAT[5]/PRU1_R30[5]/GP8[9]/PRU1_R31[6]
G4 MMCSD1_DAT[4]/PRU1_R30[4]/GP8[8]/PRU1_R31[5]

DSP_TMS — L16 TMS
DSP_TDI — M16 TDI
DSP_TDO R11 22R — J18 TDO
VDD3V3 R12 4.7K DSP_TCK — J15 TCK
DSP_TRSTn — L17 TRST#

DSP_EMU0 — J16 EMU0
DSP_EMU1 — K16 EMU1
DSP_RTCK R14 22R — K17 RTCK/GP8[0]

TMS320C6748BZWTA3

EMA_D[15]/GP3[7] — E6 DSP_EMA_D15
EMA_D[14]/GP3[6] — C7 DSP_EMA_D14
EMA_D[13]/GP3[5] — B6 DSP_EMA_D13
EMA_D[12]/GP3[4] — A6 DSP_EMA_D12
EMA_D[11]/GP3[3] — D6 DSP_EMA_D11
EMA_D[10]/GP3[2] — A7 DSP_EMA_D10
EMA_D[9]/GP3[1] — D9 DSP_EMA_D9
EMA_D[8]/GP3[0] — E10 DSP_EMA_D8
EMA_D[7]/GP4[15] — D7 DSP_EMA_D7
EMA_D[6]/GP4[14] — C6 DSP_EMA_D6
EMA_D[5]/GP4[13] — E7 DSP_EMA_D5
EMA_D[4]/GP4[12] — B5 DSP_EMA_D4
EMA_D[3]/GP4[11] — E8 DSP_EMA_D3
EMA_D[2]/GP4[10] — B8 DSP_EMA_D2
EMA_D[1]/GP4[9] — A8 DSP_EMA_D1
EMA_D[0]/GP4[8] — C9 DSP_EMA_D0

EMA_A[22]/MMCSD0_CMD/PRU1_R30[30]/GP4[6] — A10
EMA_A[21]/MMCSD0_DAT[0]/PRU1_R30[29]/GP4[5] — B10
EMA_A[20]/MMCSD0_DAT[1]/PRU1_R30[28]/GP4[4] — A11
EMA_A[19]/MMCSD0_DAT[2]/PRU1_R30[27]/GP4[3] — C10
EMA_A[18]/MMCSD0_DAT[3]/PRU1_R30[26]/GP4[2] — E11
EMA_A[17]/MMCSD0_DAT[4]/PRU1_R30[25]/GP4[1] — B11
EMA_A[16]/MMCSD0_DAT[5]/PRU1_R30[24]/GP4[0] — E12
EMA_A[15]/MMCSD0_DAT[6]/PRU1_R30[23]/GP5[15]/PRU1_R31[23] — C11
EMA_A[14]/MMCSD0_DAT[7]/PRU1_R30[22]/GP5[14]/PRU1_R31[22] — A12 DSP_EMA_A14
EMA_A[13]/PRU0_R30[21]/PRU1_R30[21]/GP5[13]/PRU1_R31[21] — D11 DSP_EMA_A13
EMA_A[12]/PRU1_R30[20]/GP5[12]/PRU1_R31[20] — D13 DSP_EMA_A12
EMA_A[11]/PRU1_R30[19]/GP5[11]/PRU1_R31[19] — B12 DSP_EMA_A11
EMA_A[10]/PRU1_R30[18]/GP5[10]/PRU1_R31[18] — C12 DSP_EMA_A10
EMA_A[9]/PRU1_R30[17]/GP5[9] — D12 DSP_EMA_A9
EMA_A[8]/PRU1_R30[16]/GP5[8] — A13 DSP_EMA_A8
EMA_A[7]/PRU1_R30[15]/GP5[7] — B13 DSP_EMA_A7
EMA_A[6]/GP5[6] — E13 DSP_EMA_A6
EMA_A[5]/GP5[5] — C13 DSP_EMA_A5
EMA_A[4]/GP5[4] — A14 DSP_EMA_A4
EMA_A[3]/GP5[3] — D14 DSP_EMA_A3
EMA_A[2]/GP5[2] — B14 DSP_EMA_A2
EMA_A[1]/GP5[1] — D15 DSP_EMA_A1
EMA_A[0]/GP5[0] — C14 DSP_EMA_A0

EMA_BA[0]/GP2[8] — C15 DSP_EMA_BA0
EMA_BA[1]/GP2[9] — A15 DSP_EMA_BA1

EMA_WEN_DQM[0]#/GP2[3] — C8
EMA_WEN_DQM[1]#/GP2[2] — A5
EMA_SDCKE/PRU0_R30[4]/GP2[6]/PRU0_R31[4] — D8 DSP_RUN_S
D1 LED Green R10 330R VDD3V3
EMA_CAS#/PRU0_R30[2]/GP2[4]/PRU0_R31[2] — A9
EMA_RAS#/PRU0_R30[3]/GP2[5]/PRU0_R31[3] — A16
EMA_WE#/GP3[11] — B9 DSP_EMA_WEn
R13 4.7K VDD3V3

D2 BAT43W
VDD3V3
J1 D3 BAT43W
CR1220
弹簧片为负电级
CR1220电池底座
U2 TPS79912DDCR
IN OUT GND EN NR
C7 0.1uF
C8 0.1uF
C9 2.2uF
RTC_CVDD

露出壳体
R15 4.7K DSP_TMS — J2 1
R17 4.7K DSP_TDI — 3
R18 100R — 5
DSP_TDO — 7
DSP_RTCK — 9
DSP_TCK R19 22R — 11
R20 4.7K DSP_EMU0 — 13
2 4 8 10 12 14
DSP_TRSTn R16 4.7K
DSP_EMU1 R21 4.7K VDD3V3
VDD3V3
67997-414LF

VDD1V2 FB1 CBG201209U601 DSP_PLL_VDDA
C3 10uF/25V
C4 0.1uF
C5 0.1uF
C6 0.1uF

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[8] DSP_DDR2_A[13:0] — DSP_DDR2_A[13:0]

[8] DSP_DDR2_DQ[15:0] — DSP_DDR2_DQ[15:0]

[8] DSP_DDR2_BA[2:0] — DSP_DDR2_BA[2:0]

[8] DSP_DDR2_DQS[1:0] — DSP_DDR2_DQS[1:0]

[8] DSP_DDR2_DQM[1:0] — DSP_DDR2_DQM[1:0]

[8] DSP_DDR2_CSn — DSP_DDR2_CSn

[8] DSP_DDR2_CASn — DSP_DDR2_CASn

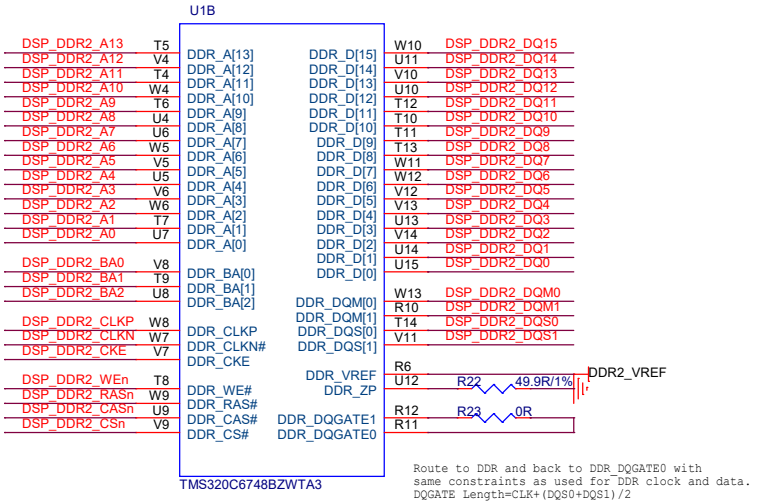
[8] DSP_DDR2_RASn — DSP_DDR2_RASn

[8] DSP_DDR2_WEn — DSP_DDR2_WEn

[8] DSP_DDR2_CKE — DSP_DDR2_CKE

[8] DSP_DDR2_CLKP — DSP_DDR2_CLKP

[8] DSP_DDR2_CLKN — DSP_DDR2_CLKN



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[16] LAN8710_MDIO
[16] LAN8710_MDC
LAN8710_MDIO
LAN8710_MDC

[16] LAN8710_RXD3
[16] LAN8710_RXD2
[16] LAN8710_RXD1
[16] LAN8710_RXD0
[16] LAN8710_RXDV
[16] LAN8710_RXCLK
[16] LAN8710_RXER
LAN8710_RXD3
LAN8710_RXD2
LAN8710_RXD1
LAN8710_RXD0
LAN8710_RXDV
LAN8710_RXCLK
LAN8710_RXER

[16] LAN8710_TXCLK
[16] LAN8710_TXEN
[16] LAN8710_TXD0
[16] LAN8710_TXD1
[16] LAN8710_TXD2
[16] LAN8710_TXD3
[16] LAN8710_COL
[16] LAN8710_CRS
LAN8710_TXCLK
LAN8710_TXEN
LAN8710_TXD0
LAN8710_TXD1
LAN8710_TXD2
LAN8710_TXD3
LAN8710_COL
LAN8710_CRS

[16] LAN8710_nINT
LAN8710_nINT

[15,20] DSP_SDA
[15,20] DSP_SCL
DSP_SDA
DSP_SCL

[20] MPU6050_INT
[15] AT24CXX_WP
MPU6050_INT
AT24CXX_WP

[14] DSP_DEG_TX
[14] DSP_DEB_RX
DSP_DEG_TX
DSP_DEB_RX

[10] DSP_FPGA_D[7:0]
DSP_FPGA_D[7:0]

[18] MCP2515_RSTn1
[18] MCP2515_RSTn2
MCP2515_RSTn1
MCP2515_RSTn2

[10] FPGA_SPI_CSn
[18] MCP2515_CSn1
[18] MCP2515_CSn2
[10,18] MCP2515_SO
[10,18] MCP2515_SI
[10,18] MCP2515_SCK
[18] MCP2515_INTn1
[18] MCP2515_INTn2
FPGA_SPI_CSn
MCP2515_CSn1
MCP2515_CSn2
MCP2515_SO
MCP2515_SI
MCP2515_SCK
MCP2515_INTn1
MCP2515_INTn2

U1C

LAN8710_RXD0 D16
LAN8710_RXCLK D19
LAN8710_RXDV C17
LAN8710_MDIO D17
LAN8710_MDC E16
LAN8710_RXD1 E17
LAN8710_RXD2 D18
LAN8710_RXD3 C19
LAN8710_CRS C18
LAN8710_RXER C16
MCP2515_SCK G19
H16
MCP2515_CSn1 E19
MCP2515_CSn2 F18
DSP_DEG_TX F19
DSP_DEB_RX E18
F16
FPGA_SPI_CSn F17
DSP_SDA G18
DSP_SCL G16
MCP2515_SI G17
MCP2515_SO H17
AT24CXX_WP R17
MCP2515_INTn1 R16
MCP2515_INTn2 U17
MPU6050_INT W15
U16
RST_SW T15
G1
MCP2515_RSTn1 G2
MCP2515_RSTn2 J4
G3
LED_RUN R5

SPI0_SCS[2]#/UART0_RTS#/GP8[1]/MII_RXD[0]
SPI0_CLK/EPWM0A/GP1[8]/MII_RXCLK
SPI0_ENA#/EPWM0B/PRU0_R30[6]/MII_RXDV
SPI0_SCS[0]#/TM64P1_OUT12/GP1[6]/MDIO_D/TM64P1_IN12
SPI0_SCS[1]#/TM64P0_OUT12/GP1[7]/MDIO_CLK/TM64PO_IN12
SPI0_SCS[3]#/UART0_CTS#/GP8[2]/MII_RXD[1]
SPI0_SCS[4]#/UART0_TXD/GP8[3]/MII_RXD[2]
SPI0_SCS[5]#/UART0_RXD/GP8[4]/MII_RXD[3]
SPI0_SIMO/EPWMSYNCO/GP8[5]/MII_CRS
SPI0_SOMI/EPWMSYNCI/GP8[6]/MII_RXER
SPI1_CLK/GP2[13]
SPI1_ENA/GP2[12]
SPI1_SCS[0]#/EPWM1B/PRU0_R30[7]/GP2[14]/TM64P3_IN12
SPI1_SCS[1]#/EPWM1A/PRU0_R30[8]/GP2[15]/TM64P2_IN12
SPI1_SCS[2]#/UART1_TXD/GP1[0]
SPI1_SCS[3]#/UART1_RXD/GP1[1]
SPI1_SCS[4]#/UART2_TXD/I2C1_SDA/GP1[2]
SPI1_SCS[5]#/UART2_RXD/I2C1_SCL/GP1[3]
SPI1_SCS[6]#/I2C0_SDA/TM64P3_OUT12/GP1[4]
SPI1_SCS[7]#/I2C0_SCL/TM64P2_OUT12/GP1[5]
SPI1_SIMO/GP2[10]
SPI1_SOMI/GP2[11]
PRU0_R30[31]/UHPI_HRDY#/PRU1_R30[12]/GP6[13]
PRU0_R30[30]/UHPI_HINT#/PRU1_R30[11]/GP6[12]
PRU0_R30[29]/UHPI_HCNTL0/UPP_CHA_CLOCK/GP6[11]
PRU0_R30[28]/UHPI_HCNTL1/UPP_CHA_START/GP6[10]
PRU0_R30[27]/UHPI_HHWIL/UPP_CHA_ENABLE/GP6[9]
PRU0_R30[26]/UHPI_HRW#/UPP_CHA_WAIT/GP6[8]PRU1_R31[17]
PRU0_R30[25]/MMCSD1_DAT[0]/UPP_CHB_CLOCK/GP8[15]/PRU1_R31[27]
PRU0_R30[24]/MMCSD1_CLK/UPP_CHB_START/GP8[14]/PRU1_R31[26]
PRU0_R30[23]/MMCSD1_CMD/UPP_CHB_ENABLE/GP8[13]/PRU1_R31[25]
PRU0_R30[22]/PRU1_R30[8]/UPP_CHB_WAIT/GP8[12]/PRU1_R31[24]
GP6[0]/PRU1_R31[28]

AXR15/EPWM0TZ[0]/ECAP2_APWM2/GP0[7]
AXR14/CLKR1/GP0[6]
AXR13/CLKX1/GP0[5]
AXR12/FSR1/GP0[4]
AXR11/FSX1/GP0[3]
AXR10/DR1/GP0[2]
AXR9/DX1/GP0[1]
AXR8/CLKS1/ECAP1_APWM1/GP0[0]/PRU0_R31[8]
AXR7/EPWM1TZ[0]/PRU0_R30[17]/GP1[15]/PRU0_R31[7]
AXR6/CLKR0/GP1[14]/MII_TXEN/PRU0_R31[6]
AXR5/CLKX0/GP1[13]/MII_TXCLK
AXR4/FSR0/GP1[12]/MII_COL
AXR3/FSX0/GP1[11]/MII_TXD[3]
AXR2/DR0/GP1[10]/MII_TXD[2]
AXR1/DX0/GP1[9]/MII_TXD[1]
AXR0/ECAP0_APWM0/GP8[7]/MII_TXD[0]/CLKS0
AHCLKX3/USB_REFCLKIN/UART1_CTS#/GP0[10]/PRU0_R31[17]
ACLKX/PRU0_R30[19]/GP0[14]/PRU0_R31[21]
AFSX/GP0[12]/PRU0_R31[19]
AHCLKR/PRU0_R30[18]/UART1_RTS#/GP0[11]/PRU0_R31[18]
ACLKR/PRU0_R30[20]/GP0[15]/PRU0_R31[22]
AFSR/GP0[13]/PRU0_R31[20]
AMUTE/PRU0_R30[16]/UART2_RTS#/GP0[9]/PRU0_R31[16]

USB0_DRVVBUS
USB0_VBUS
USB0_ID
USB0_DP
USB0_DM
USB1_DP
USB1_DM
SATA_REFCLKN#
SATA_REFCLKP
SATA_TXN#
SATA_TXP
SATA_RXN#
SATA_RXP

A4 DSP_FPGA_D7
B4 DSP_FPGA_D6
B3 DSP_FPGA_D5
C4 DSP_FPGA_D4
C5 DSP_FPGA_D3
D4 DSP_FPGA_D2
C3 DSP_FPGA_D1
E4 DSP_FPGA_D0
D2
C1 LAN8710_TXEN
D3 LAN8710_TXCLK
D1 LAN8710_COL
E3 R24 100R LAN8710_TXD3
E2 R25 100R LAN8710_TXD2
E1 R26 100R LAN8710_TXD1
F3 R27 100R LAN8710_TXD0
A3
B1
B2
A2
A1 LAN8710_nINT
C2
D5

K18
N19
P16
M19
M18
NOT USE USB
P19
P18
N1
N2
J2
J1
NOT USE SATA
L2
L1

TMS320C6748BZWTA3

SW PUSHBUTTON-SPST-2
C10 0.1uF
R28 10K
4 1 RST_SW
3 2 R29 1K VDD3V3
SW1

D4
R30 10K VDD24V
LED_RUN
R33 1K VDD3V3
SSB-LX2300

DSP_SDA R31 2K
DSP_SCL R32 2K VDD3V3

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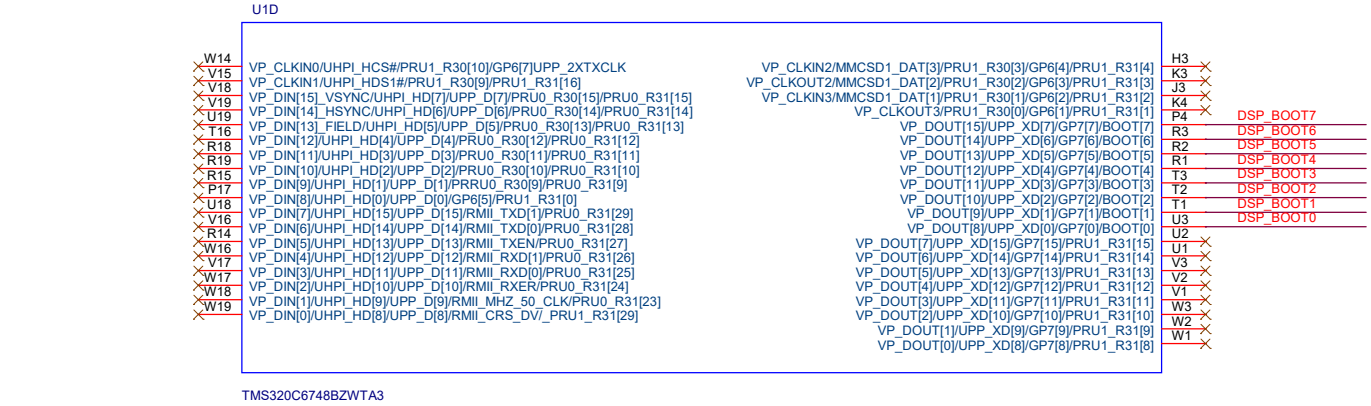
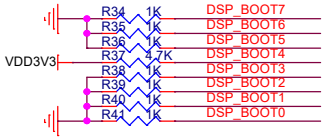


BOOT[7:0]	BOOT MODE	AIS
0xx1 0000	NAND16	Yes

BOOT[6:5]	BLOCK	PLL0 Applied
00	1	None
01	1	PLLM=24,POSTDIV=3,SYSCLK3=2
10	0	None
11	0	PLLM=24,POSTDIV=3,SYSCLK3=2



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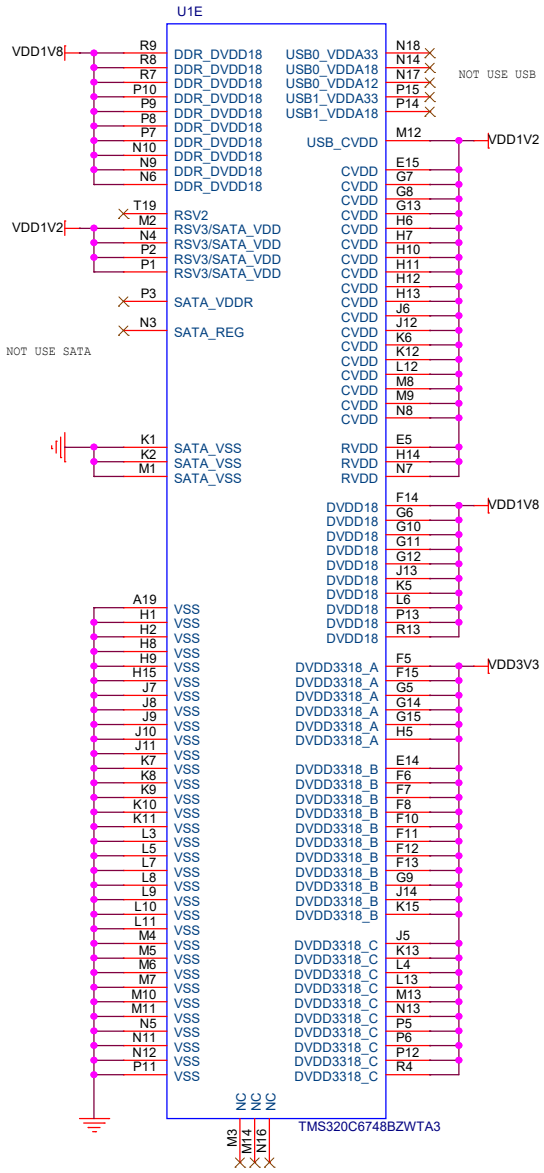

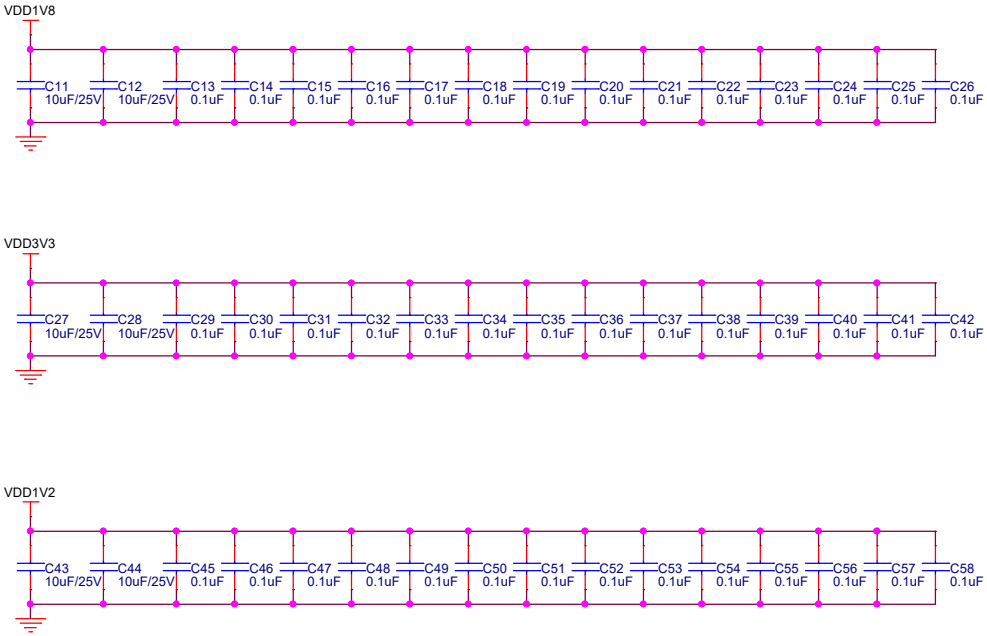

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[4] DSP_DDR2_A[13:0] — DSP_DDR2_A[13:0]
[4] DSP_DDR2_DQ[15:0] — DSP_DDR2_DQ[15:0]
[4] DSP_DDR2_BA[2:0] — DSP_DDR2_BA[2:0]
[4] DSP_DDR2_DQS[1:0] — DSP_DDR2_DQS[1:0]
[4] DSP_DDR2_DQM[1:0] — DSP_DDR2_DQM[1:0]
[4] DSP_DDR2_CSn — DSP_DDR2_CSn
[4] DSP_DDR2_CASn — DSP_DDR2_CASn
[4] DSP_DDR2_RASn — DSP_DDR2_RASn
[4] DSP_DDR2_WEn — DSP_DDR2_WEn
[4] DSP_DDR2_CKE — DSP_DDR2_CKE
[4] DSP_DDR2_CLKP — DSP_DDR2_CLKP
[4] DSP_DDR2_CLKN — DSP_DDR2_CLKN

DDR-2 128MByte

U3 — MT47H64M16HR

DSP_DDR2_A0 R42 10R M8 — A0
DSP_DDR2_A1 R43 10R M3 — A1
DSP_DDR2_A2 R44 10R M7 — A2
DSP_DDR2_A3 R45 10R N2 — A3
DSP_DDR2_A4 R46 10R N8 — A4
DSP_DDR2_A5 R52 10R N3 — A5
DSP_DDR2_A6 R53 10R N7 — A6
DSP_DDR2_A7 R54 10R P2 — A7
DSP_DDR2_A8 R47 10R P8 — A8
DSP_DDR2_A9 R48 10R P3 — A9
DSP_DDR2_A10 R49 10R M2 — A10
DSP_DDR2_A11 R50 10R P7 — A11
DSP_DDR2_A12 R51 10R R2 — A12

DSP_DDR2_BA0 R55 22R L2 — BA0
DSP_DDR2_BA1 R56 22R L3 — BA1
DSP_DDR2_BA2 R57 22R L1 — BA2

R59 4.7K/1% K9 — ODT
DSP_DDR2_CSn R61 22R L8 — CSn
DSP_DDR2_CASn R63 22R L7 — CASn
DSP_DDR2_RASn R65 22R K7 — RASn
DSP_DDR2_WEn R66 22R K3 — WEn
DSP_DDR2_CKE R67 22R K2 — CKE

DSP_DDR2_CLKP R72 10R J8 — CK
DSP_DDR2_CLKN R73 10R K8 — CKn

DSP_DDR2_DQS1 R77 22R B7 — UDQS
DSP_DDR2_DQS0 R79 22R F7 — LDQS

DSP_DDR2_DQM1 R83 22R B3 — UDM
DSP_DDR2_DQM0 R85 22R F3 — LDM

A2 — NC1
E2 — NC2
A8 — UDQSn/NU
E8 — LDQSn/NU

R3 — RFU2
R7 — RFU3
DSP_DDR2_A13 R88 10R R8 — RFU1

VDD1V8:
VDD5 A1, VDD4 E1, VDD3 M9, VDD2 R1, VDD1 J9, VDDL J1, VDDQ10 A9, VDDQ9 C1, VDDQ8 C3, VDDQ7 C7, VDDQ6 C9, VDDQ5 G3, VDDQ4 E9, VDDQ3 G1, VDDQ2 G7, VDDQ1 G9

VREF J2 DSP_DDR2_VREF — DDR2_VREF

DQ0 G8 R58 10R DSP_DDR2_DQ0
DQ1 G2 R60 10R DSP_DDR2_DQ1
DQ2 H7 R62 10R DSP_DDR2_DQ2
DQ3 H3 R64 10R DSP_DDR2_DQ3
DQ4 H1 R68 10R DSP_DDR2_DQ4
DQ5 H9 R69 10R DSP_DDR2_DQ5
DQ6 F1 R70 10R DSP_DDR2_DQ6
DQ7 F9 R71 10R DSP_DDR2_DQ7
DQ8 C8 R74 10R DSP_DDR2_DQ8
DQ9 C2 R75 10R DSP_DDR2_DQ9
DQ10 D7 R76 10R DSP_DDR2_DQ10
DQ11 D3 R78 10R DSP_DDR2_DQ11
DQ12 D1 R81 10R DSP_DDR2_DQ12
DQ13 D9 R82 10R DSP_DDR2_DQ13
DQ14 B1 R84 10R DSP_DDR2_DQ14
DQ15 B9 R86 10R DSP_DDR2_DQ15

VSS5 A3, VSS4 E3, VSS3 J3, VSS2 N1, VSS1 P9, VSSQ10 A7, VSSQ9 B2, VSSQ8 B8, VSSQ7 D2, VSSQ6 D8, VSSQ5 E7, VSSQ4 F2, VSSQ3 F8, VSSQ2 H2, VSSQ1 H8, VSSDL J7

VDD1V8
C60 0.1uF, C61 0.1uF, C62 0.1uF, C63 0.1uF, C59 0.1uF, C64 0.1uF, C65 10uF/25V

VDD1V8
C66 0.1uF, C67 0.1uF, C68 0.1uF, C69 0.1uF, C70 0.1uF, C71 0.1uF, C72 0.1uF, C73 0.1uF, C74 0.1uF, C75 10uF/25V, C76 0.1uF

VDD1V8
C77 0.1uF, R80 1K/1%
DDR2_VREF — DDR2_VREF
C78 0.1uF, R87 1K/1%

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Size B	Document Number <Doc>	Rev <RevCode>
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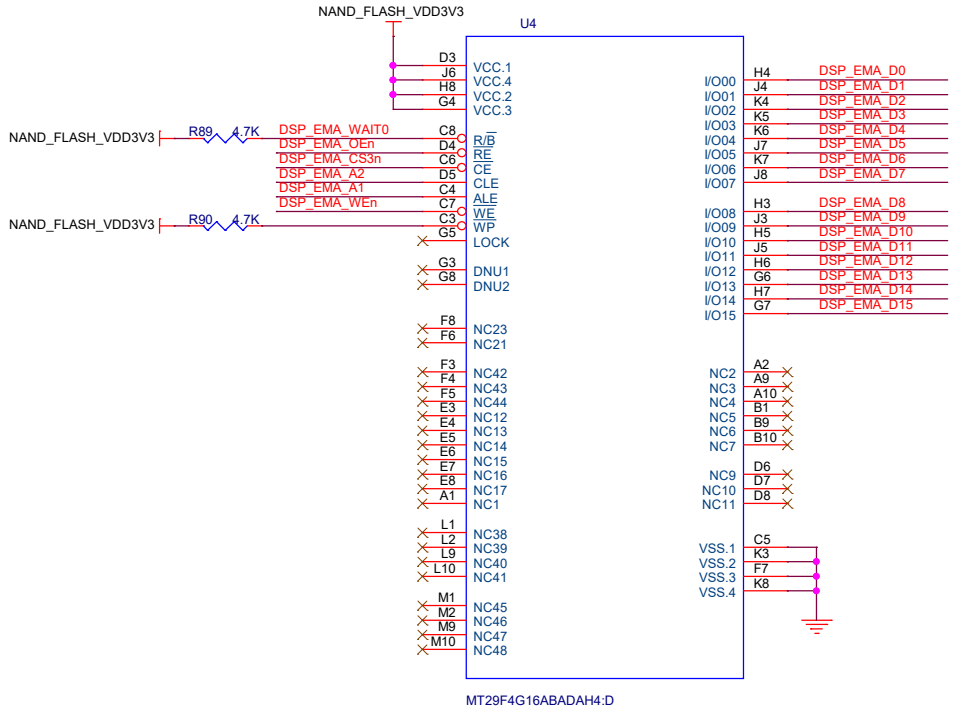
[3,10] DSP_EMA_D[15:0] — DSP_EMA_D[15:0]

[3] DSP_EMA_WAIT0 — DSP_EMA_WAIT0
[3,10] DSP_EMA_OEn — DSP_EMA_OEn
[3] DSP_EMA_CS3n — DSP_EMA_CS3n
[3,10] DSP_EMA_WEn — DSP_EMA_WEn

[3,10] DSP_EMA_A2 — DSP_EMA_A2
[3,10] DSP_EMA_A1 — DSP_EMA_A1

NAND FLASH 512MByte



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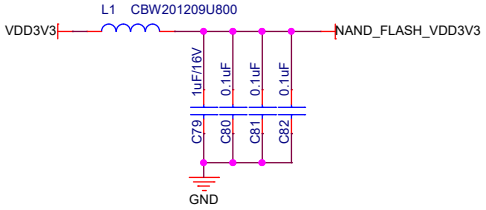
DECAPs FOR FLASH



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[3,9] DSP_EMA_A[14:0] — DSP_EMA_A[14:0]

[3,9] DSP_EMA_D[15:0] — DSP_EMA_D[15:0]

[3] DSP_EMA_WAIT1 — DSP_EMA_WAIT1
[3,9] DSP_EMA_OEn — DSP_EMA_OEn
[3] DSP_EMA_CS2n — DSP_EMA_CS2n
[3] DSP_EMA_CS4n — DSP_EMA_CS4n
[3] DSP_EMA_CS5n — DSP_EMA_CS5n

[3,9] DSP_EMA_WEn — DSP_EMA_WEn

[3] DSP_EMA_A_RW — DSP_EMA_A_RW
[3] DSP_EMA_BA0 — DSP_EMA_BA0
[3] DSP_EMA_BA1 — DSP_EMA_BA1

[19] FPGA_CANR[3:0] — FPGA_CANR[3:0]
[19] FPGA_CAND[3:0] — FPGA_CAND[3:0]

[21] FPGA_CLK — FPGA_CLK

[5] FPGA_SPI_CSn — FPGA_SPI_CSn
[5,18] MCP2515_SO — MCP2515_SO
[5,18] MCP2515_SI — MCP2515_SI
[5,18] MCP2515_SCK — MCP2515_SCK

[22] SPK_CN — SPK_CN

[3] DSP_RESETOUTn — DSP_RESETOUTn

[16] LAN8710_nRST — LAN8710_nRST

[5] DSP_FPGA_D[7:0] — DSP_FPGA_D[7:0]

U5A

R91 1K

	A3	IO_L1P_HSWAPEN_0	
	A4	IO_L1N_VREF_0	
DSP_EMA_A_RW	C5	IO_L2P_0	
DSP_EMA_A11	A5	IO_L2N_0	
DSP_EMA_A13	D6	IO_L3P_0	
DSP_EMA_D8	C6	IO_L3N_0	
DSP_EMA_D9	B6	IO_L4P_0	
DSP_EMA_CS4n	A6	IO_L4N_0	
DSP_EMA_D11	C7	IO_L5P_0	
DSP_EMA_D10	A7	IO_L5N_0	
DSP_EMA_D12	B8	IO_L6P_0	
DSP_EMA_CS2n	A8	IO_L6N_0	
DSP_EMA_A4	D9	IO_L7P_0	
DSP_EMA_D13	C8	IO_L7N_0	
DSP_EMA_D14	C9	IO_L8P_0	
DSP_EMA_A14	A9	IO_L8N_VREF_0	
DSP_EMA_A9	E8	IO_L14P_0	
DSP_EMA_A7	F8	IO_L14N_0	
DSP_EMA_A8	G8	IO_L15P_0	
DSP_EMA_A0	F9	IO_L15N_0	
DSP_EMA_A12	G9	IO_L16P_0	
DSP_EMA_WAIT1	H10	IO_L16N_0	
	E10	IO_L17P_0	
	F10	IO_L17N_0	
	G11	IO_L18P_0	
	H11	IO_L18N_0	
DSP_EMA_A10	D7	IO_L32P_0	
DSP_EMA_CS5n	D8	IO_L32N_0	
DSP_EMA_BA1	D10	IO_L33P_0	
DSP_EMA_A1	C10	IO_L33N_0	
DSP_EMA_D15	B10	IO_L34P_GCLK19_0	
DSP_EMA_WEn	A10	IO_L34N_GCLK18_0	
DSP_EMA_OEn	C11	IO_L35P_GCLK17_0	
DSP_EMA_A2	A11	IO_L35N_GCLK16_0	

	D11	IO_L36P_GCLK15_0	
	C12	IO_L36N_GCLK14_0	
DSP_EMA_D1	B12	IO_L37P_GCLK13_0	
DSP_EMA_D2	A12	IO_L37N_GCLK12_0	
	C13	IO_L38P_0	
DSP_EMA_D4	A13	IO_L38N_VREF_0	
DSP_EMA_D0	E12	IO_L43P_0	
DSP_FPGA_D7	D12	IO_L43N_0	
	H12	IO_L44P_0	
DSP_EMA_A5	F12	IO_L44N_0	
	F13	IO_L45P_0	
DSP_FPGA_D6	D13	IO_L45N_0	
DSP_EMA_A3	H13	IO_L46P_0	
DSP_EMA_BA0	G13	IO_L46N_0	
DSP_EMA_D3	E14	IO_L47P_0	
DSP_EMA_D5	F15	IO_L47N_0	
	F14	IO_L48P_0	
DSP_EMA_A6	H14	IO_L48N_0	
DSP_FPGA_D5	D14	IO_L49P_0	
DSP_EMA_D6	C14	IO_L49N_0	
DSP_FPGA_D4	B14	IO_L50P_0	
FPGA_SPI_CSn	A14	IO_L50N_0	
MCP2515_SO	C15	IO_L51P_0	
MCP2515_SI	A15	IO_L51N_0	
MCP2515_SCK	D15	IO_L62P_0	
	C16	IO_L62N_VREF_0	
DSP_FPGA_D1	B16	IO_L63P_SCP7_0	
	A16	IO_L63N_SCP6_0	
	C17	IO_L64P_SCP5_0	
DSP_FPGA_D3	A17	IO_L64N_SCP4_0	
DSP_FPGA_D2	B18	IO_L65P_SCP3_0	
DSP_FPGA_D0	A18	IO_L65N_SCP2_0	
DSP_EMA_D7	E16	IO_L66P_SCP1_0	
	D17	IO_L66N_SCP0_0	

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U5B

	C19	IO_L1P_A25_1	
	B20	IO_L1N_A24_VREF_1	
FPGA_CAND1	G16	IO_L9P_1	
FPGA_CANR0	G17	IO_L9N_1	
FPGA_CAND2	F16	IO_L10P_1	
FPGA_CAND0	F17	IO_L10N_1	
	B21	IO_L19P_1	
	B22	IO_L19N_1	
	A20	IO_L20P_1	
	A21	IO_L20N_1	
	K16	IO_L21P_1	
FPGA_CAND3	J16	IO_L21N_1	
FPGA_CANR1	H16	IO_L28P_1	
FPGA_CANR2	H17	IO_L28N_VREF_1	
	D19	IO_L29P_A23_M1A13_1	
	D20	IO_L29N_A22_M1A14_1	
	F18	IO_L30P_A21_M1RESET_1	
	F19	IO_L30N_A20_M1A11_1	
	D21	IO_L31P_A19_M1CKE_1	
	D22	IO_L31N_A18_M1A12_1	
	C20	IO_L32P_A17_M1A8_1	
	C22	IO_L32N_A16_M1A9_1	
	G19	IO_L33P_A15_M1A10_1	
	F20	IO_L33N_A14_M1A4_1	
	H19	IO_L34P_A13_M1WE_1	
	H18	IO_L34N_A12_M1BA2_1	
	E20	IO_L35P_A11_M1A7_1	
	E22	IO_L35N_A10_M1A2_1	
	J17	IO_L36P_A9_M1BA0_1	
	K17	IO_L36N_A8_M1BA1_1	
	F21	IO_L37P_A7_M1A0_1	
	F22	IO_L37N_A6_M1A1_1	
	H20	IO_L38P_A5_M1CLK_1	
	J19	IO_L38N_A4_M1CLKN_1	
	G20	IO_L39P_M1A3_1	
	G22	IO_L39N_M1ODT_1	
	K20	IO_L40P_GCLK11_M1A5_1	
	K19	IO_L40N_GCLK10_M1A6_1	
	H21	IO_L41P_GCLK9_IRDY1_M1RASN_1	
	H22	IO_L41N_GCLK8_M1CASN_1	
	M20	IO_L42P_GCLK7_M1UDM_1	
	L19	IO_L42N_GCLK6_TRDY1_M1LDM_1	

	J20	IO_L43P_GCLK5_M1DQ4_1	
FPGA_CLK	J22	IO_L43N_GCLK4_M1DQ5_1	
	K21	IO_L44P_A3_M1DQ6_1	
	K22	IO_L44N_A2_M1DQ7_1	
	L20	IO_L45P_A1_M1LDQS_1	
	L22	IO_L45N_A0_M1LDQSN_1	
	M21	IO_L46P_FCS_B_M1DQ2_1	
	M22	IO_L46N_FOE_B_M1DQ3_1	
LAN8710_nRST	N20	IO_L47P_FWE_B_M1DQ0_1	
	N22	IO_L47N_LDC_M1DQ1_1	
	P21	IO_L48P_HDC_M1DQ8_1	
	P22	IO_L48N_M1DQ9_1	
	R20	IO_L49P_M1DQ10_1	
	R22	IO_L49N_M1DQ11_1	
	T21	IO_L50P_M1UDQS_1	
	T22	IO_L50N_M1UDQSN_1	
	U20	IO_L51P_M1DQ12_1	
	U22	IO_L51N_M1DQ13_1	
	V21	IO_L52P_M1DQ14_1	
	V22	IO_L52N_M1DQ15_1	
	M19	IO_L53P_1	
FPGA_CANR3	N19	IO_L53N_VREF_1	
	M16	IO_L58P_1	
	L15	IO_L58N_1	
	P19	IO_L59P_1	
	T20	IO_L74N_DOUT_BUSY_1	
DSP_RESETOUTn	P20	IO_L59N_1	
	W20	IO_L60P_1	
	W22	IO_L60N_1	
	L17	IO_L61P_1	
	K18	IO_L61N_1	
	U19	IO_L70P_1	
	V20	IO_L70N_1	
	M17	IO_L71P_1	
	M18	IO_L71N_1	
	P17	IO_L72P_1	
	N16	IO_L72N_1	
FPGA_RUN_S	P18	IO_L73P_1	
SPK_CN	R19	IO_L73N_1	
	T19	IO_L74P_AWAKE_1	

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D5 LED Green
FPGA_RUN_S — R92 330R — VDD3V3

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[3] FPGA_DONE — FPGA_DONE

[13] CFG_SPI_CS — CFG_SPI_CS
[13] CFG_SPI_MISO — CFG_SPI_MISO
[13] CFG_SPI_CCLK — CFG_SPI_CCLK
[13] CFG_SPI_MOSI — CFG_SPI_MOSI

[13] FPGA_M0 — FPGA_M0
[13] FPGA_M1 — FPGA_M1

[17] SJA_L_AD0 — SJA_L_AD0
[17] SJA_L_AD1 — SJA_L_AD1
[17] SJA_L_AD2 — SJA_L_AD2
[17] SJA_L_AD3 — SJA_L_AD3
[17] SJA_L_AD4 — SJA_L_AD4
[17] SJA_L_AD5 — SJA_L_AD5
[17] SJA_L_AD6 — SJA_L_AD6
[17] SJA_L_AD7 — SJA_L_AD7
[17] SJA_L_ALE — SJA_L_ALE
[17] SJA_L_CSn — SJA_L_CSn
[17] SJA_L_RDn — SJA_L_RDn
[17] SJA_L_WRn — SJA_L_WRn
[17] SJA_L_RSTn — SJA_L_RSTn
[17] SJA_L_INTn — SJA_L_INTn

U5C

VDD3V3 — R93 4.7K — FPGA_DONE
CFG_SPI_CCLK
FPGA_M0
CFG_SPI_MISO
CFG_SPI_MOSI
FPGA_M1

	CMPCS_B_2	IO_L40P_2	R11
Y20	DONE_2	IO_L40N_2	T11
Y22	IO_L1P_CCLK_2	IO_L41P_2	AA10
Y21	IO_L1N_M0_CMPMISO_2	IO_L41N_VREF_2	AB10
AA22	IO_L2P_CMPCLK_2	IO_L42P_2	V11
AA21	IO_L2N_CMPMOSI_2	IO_L42N_2	W11
AB21	IO_L3P_D0_DIN_MISO_MISO1_2	IO_L43P_2	Y9
AA20	IO_L3N_MOSI_CSI_B_MISO0_2	IO_L43N_2	AB9
AB20	IO_L4P_2	IO_L44P_2	W10
T18	IO_L4N_VREF_2	IO_L44N_2	Y10
T17	IO_L5P_2	IO_L45P_2	AA8
Y19	IO_L5N_2	IO_L45N_2	AB8
AB19	IO_L6P_2	IO_L46P_2	W8
W18	IO_L6N_2	IO_L46N_2	V7
Y18	IO_L7P_2	IO_L47P_2	W9
T16	IO_L7N_2	IO_L47N_2	Y8
T15	IO_L8P_2	IO_L48P_D7_2	Y7
U17	IO_L8N_2	IO_L48N_RDWR_B_VREF_2	AB7
U16	IO_L9P_2	IO_L49P_D3_2	AA6
V19	IO_L9N_2	IO_L49N_D4_2	AB6
V18	IO_L10P_2	IO_L50P_2	U9
R16	IO_L10N_2	IO_L50N_2	V9
R15	IO_L11P_2	IO_L57P_2	AA4
V17	IO_L11N_2	IO_L57N_2	AB4
W17	IO_L12P_D1_MISO2_2	IO_L58P_2	Y3
U14	IO_L12N_D2_MISO3_2	IO_L58N_2	AB3
U13	IO_L13P_M1_2	IO_L59P_2	R9
U15	IO_L13N_D10_2	IO_L59N_2	R8
V15	IO_L14P_D11_2	IO_L60P_2	T7
AA18	IO_L14N_D12_2	IO_L60N_2	R7
AB18	IO_L15P_2	IO_L62P_D5_2	W4
Y17	IO_L15N_2	IO_L62N_D6_2	Y4
AB17	IO_L16P_2	IO_L63P_2	U6
AA14	IO_L16N_VREF_2	IO_L63N_2	V5
AB14	IO_L18P_2	IO_L64P_D8_2	AA2
V13	IO_L18N_2	IO_L64N_D9_2	AB2
W13	IO_L19P_2	IO_L65P_INIT_B_2	T6
AA16	IO_L19N_2	IO_L65N_CSO_B_2	T5
AB16	IO_L20P_2	PROGRAM_B_2	AA1
W14	IO_L20N_2		U12
Y14	IO_L21P_2	N.C.	T12
Y15	IO_L21N_2	N.C.	Y16
AB15	IO_L23P_2	N.C.	W15
T14	IO_L23N_2	N.C.	T8
R13	IO_L29P_GCLK3_2	N.C.	U8
W12	IO_L29N_GCLK2_2	N.C.	T10
Y12	IO_L30P_GCLK1_D13_2	N.C.	U10
Y13	IO_L30N_GCLK0_USERCCLK_2	N.C.	AB5
AB13	IO_L31P_GCLK31_D14_2	N.C.	Y5
AA12	IO_L31N_GCLK30_D15_2	N.C.	Y6
AB12	IO_L32P_GCLK29_2	N.C.	W6
Y11	IO_L32N_GCLK28_2	N.C.	
AB11			

FPGA_INIT
CFG_SPI_CS
R94 4.7K — VDD3V3

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U5D

SJA_L_AD0 Y2	IO_L1P_3	IO_L42P_GCLK25_TRDY2_M3UDM_3	M3
SJA_L_AD1 Y1	IO_L1N_VREF_3	IO_L42N_GCLK24_M3LDM_3	L4
SJA_L_AD2 W3	IO_L2P_3	IO_L43P_GCLK23_M3RASN_3	K5
SJA_L_AD3 W1	IO_L2N_3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K4
SJA_L_AD4 P8	IO_L7P_3	IO_L44P_GCLK21_M3A5_3	K3
SJA_L_AD5 P7	IO_L7N_3	IO_L44N_GCLK20_M3A6_3	J4
SJA_L_AD6 P6	IO_L8P_3	IO_L45P_M3A3_3	K6
SJA_L_AD7 P5	IO_L8N_3	IO_L45N_M3ODT_3	J6
SJA_L_ALE T4	IO_L9P_3	IO_L46P_M3CLK_3	H4
SJA_L_CSn T3	IO_L9N_3	IO_L46N_M3CLKN_3	H3
SJA_L_RDn U4	IO_L10P_3	IO_L47P_M3A0_3	H2
SJA_L_WRn V3	IO_L10N_3	IO_L47N_M3A1_3	H1
SJA_L_RSTn N6	IO_L11P_3	IO_L48P_M3BA0_3	G3
SJA_L_INTn N7	IO_L11N_3	IO_L48N_M3BA1_3	G1
M7	IO_L23P_3	IO_L49P_M3A7_3	H6
M8	IO_L23N_3	IO_L49N_M3A2_3	H5
R4	IO_L24P_3	IO_L50P_M3WE_3	F2
P4	IO_L24N_3	IO_L50N_M3BA2_3	F1
M6	IO_L25P_3	IO_L51P_M3A10_3	G4
L6	IO_L25N_3	IO_L51N_M3A4_3	F3
P3	IO_L26P_3	IO_L52P_M3A8_3	E3
N4	IO_L26N_3	IO_L52N_M3A9_3	E1
M5	IO_L31P_3	IO_L53P_M3CKE_3	D2
M4	IO_L31N_VREF_3	IO_L53N_M3A12_3	D1
V2	IO_L32P_M3DQ14_3	IO_L54P_M3RESET_3	C3
V1	IO_L32N_M3DQ15_3	IO_L54N_M3A11_3	C1
U3	IO_L33P_M3DQ12_3	IO_L55P_M3A13_3	G6
U1	IO_L33N_M3DQ13_3	IO_L55N_M3A14_3	F5
T2	IO_L34P_M3UDQS_3	IO_L57P_3	K7
T1	IO_L34N_M3UDQSN_3	IO_L57N_VREF_3	K8
R3	IO_L35P_M3DQ10_3	IO_L58P_3	D5
R1	IO_L35N_M3DQ11_3	IO_L58N_3	E4
P2	IO_L36P_M3DQ8_3	IO_L59P_3	J7
P1	IO_L36N_M3DQ9_3	IO_L59N_3	H8
N3	IO_L37P_M3DQ0_3	IO_L60P_3	B2
N1	IO_L37N_M3DQ1_3	IO_L60N_3	B1
M2	IO_L38P_M3DQ2_3	IO_L80P_3	G7
M1	IO_L38N_M3DQ3_3	IO_L80N_3	F7
L3	IO_L39P_M3LDQS_3	IO_L81P_3	D3
L1	IO_L39N_M3LDQSN_3	IO_L81N_3	C4
K2	IO_L40P_M3DQ6_3	IO_L82P_3	E5
K1	IO_L40N_M3DQ7_3	IO_L82N_3	E6
J3	IO_L41P_GCLK27_M3DQ4_3	IO_L83P_3	A2
J1	IO_L41N_GCLK26_M3DQ5_3	IO_L83N_VREF_3	B3

XC6SLX100-2FGG484I

VDD3V3 — R96 330R — FPGA_DONE — Q1 2N7002 — D6 LED Green — R95 330R — VDD3V3
GND

VDD3V3 — R98 330R — FPGA_INIT — Q2 2N7002 — D7 LED Green — R97 330R — VDD3V3
GND

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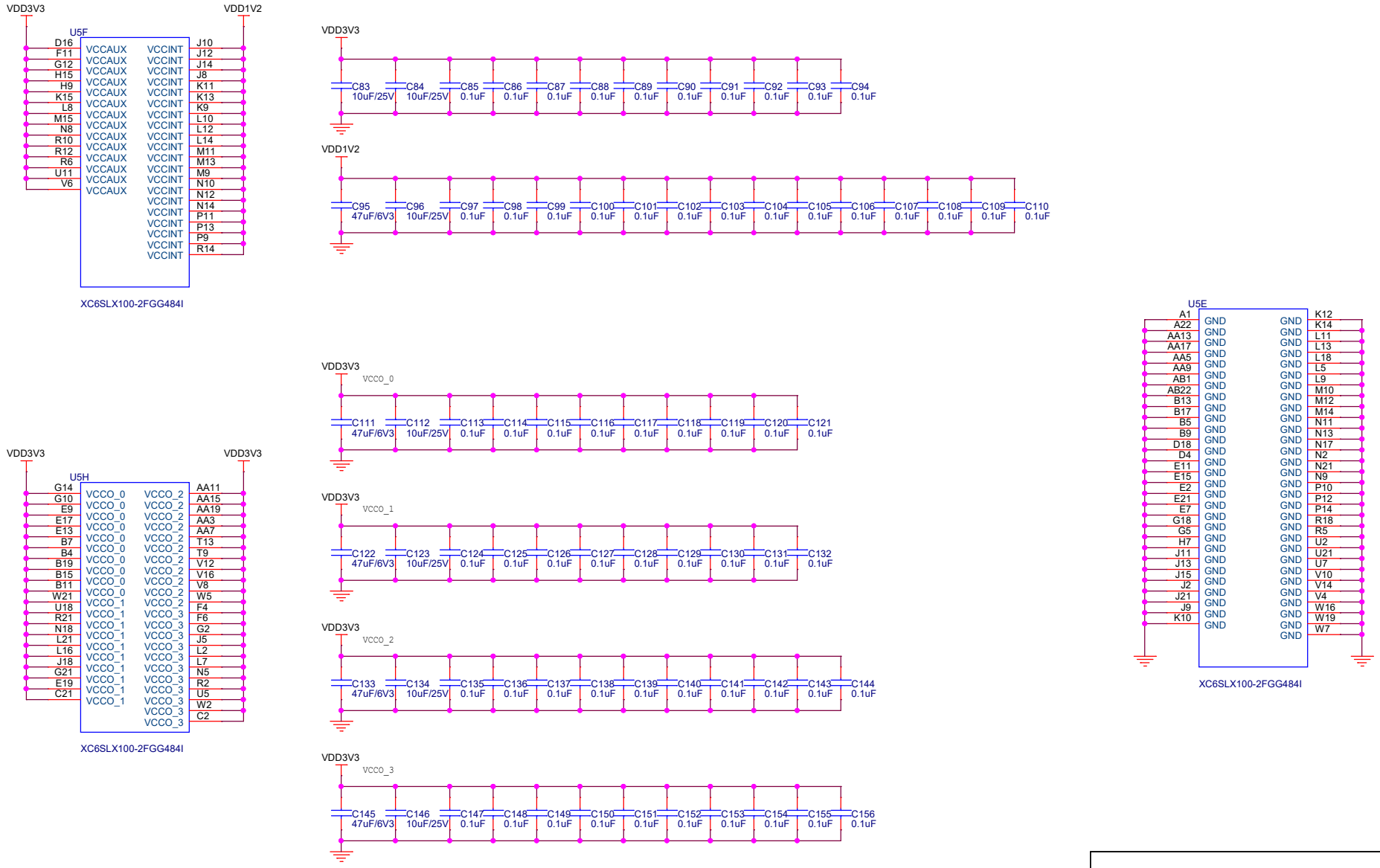

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Size B	Document Number <Doc>	Rev <RevCode>
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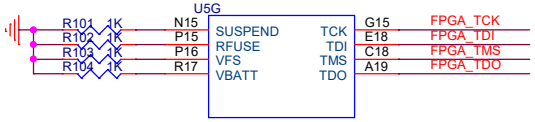
[11] FPGA_M0
[11] FPGA_M1
FPGA_M0
FPGA_M1

[11] CFG_SPI_CS
[11] CFG_SPI_MISO
[11] CFG_SPI_CCLK
[11] CFG_SPI_MOSI
CFG_SPI_CS
CFG_SPI_MISO
CFG_SPI_CCLK
CFG_SPI_MOSI

When not programming or when not using the key EFUSE,
connecting RFUSE,VFS,VBATT to VCCAUX or GND is recommended.



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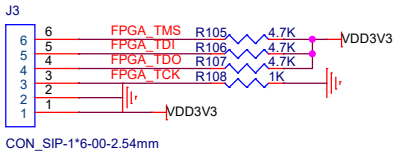
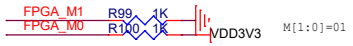
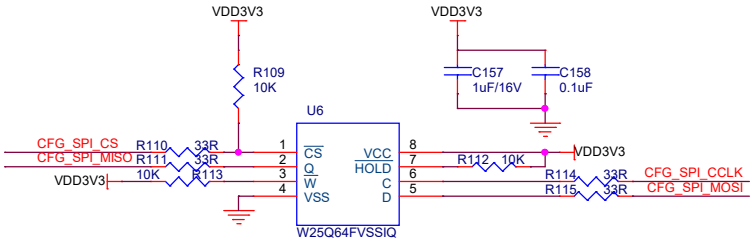


CON_SIP-1*6-00-2.54mm

露出壳体



Configuration Mode	M[1:0]	Bus Width	CCLK Direction
Master Serial/SPI	01	1, 2, 4(1)	Output
Master SelectMAP/BPI(2)	00	8, 16	Output
JTAG(3)	xx	1	Input (TCK)
Slave SelectMAP(2)	10	8, 16	Input
Slave Serial(4)	11	1	Input



W25Q64FVSSIQ

Title	<Title>	
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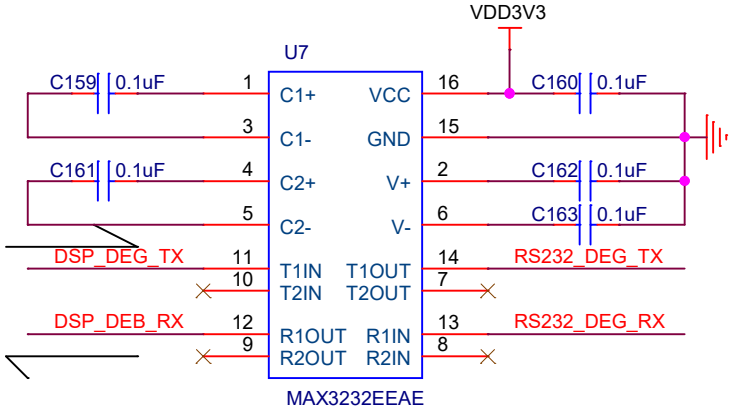
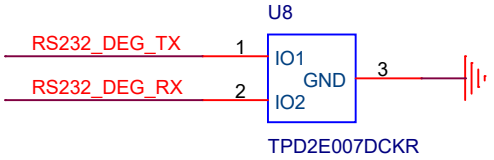
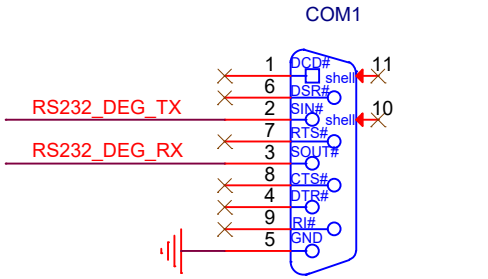
[5] DSP_DEG_TX
[5] DSP_DEB_RX

DSP_DEG_TX
DSP_DEB_RX





UART TR要交差 已改



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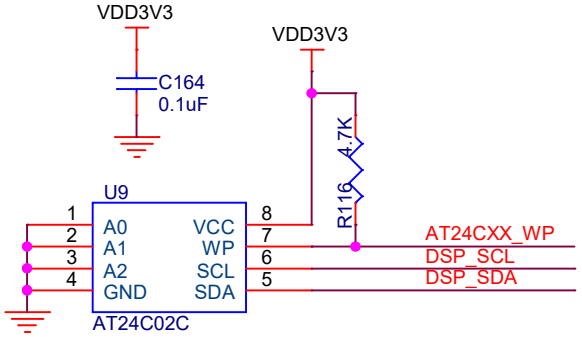
[5,20] DSP_SDA
[5,20] DSP_SCL
[5] AT24CXX_WP

DSP_SDA
DSP_SCL
AT24CXX_WP



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Size: A	Document Number: <Doc>	Rev: 1.0
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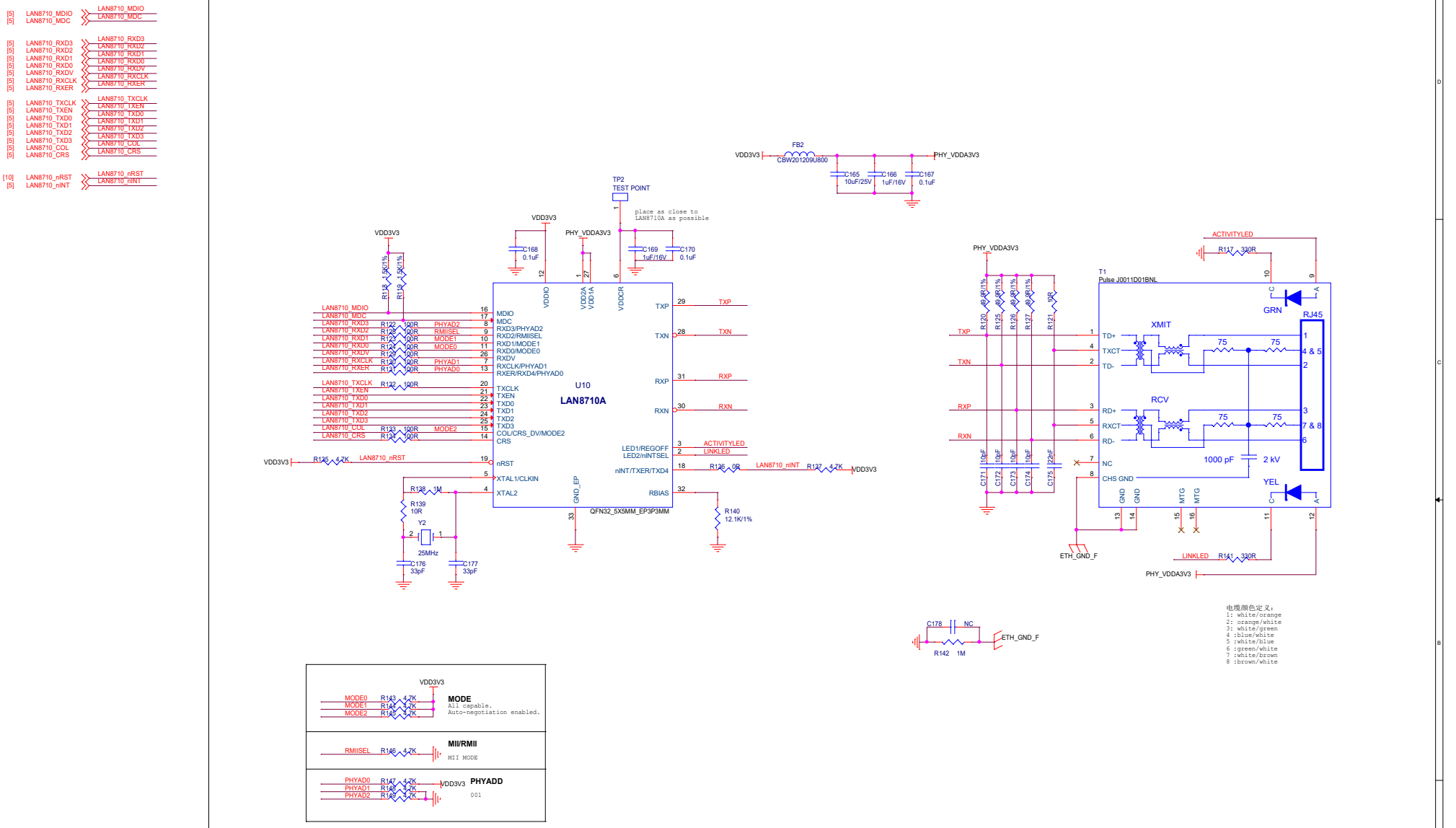

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Size C	Document Number <Doc>		Rev <RevCode>
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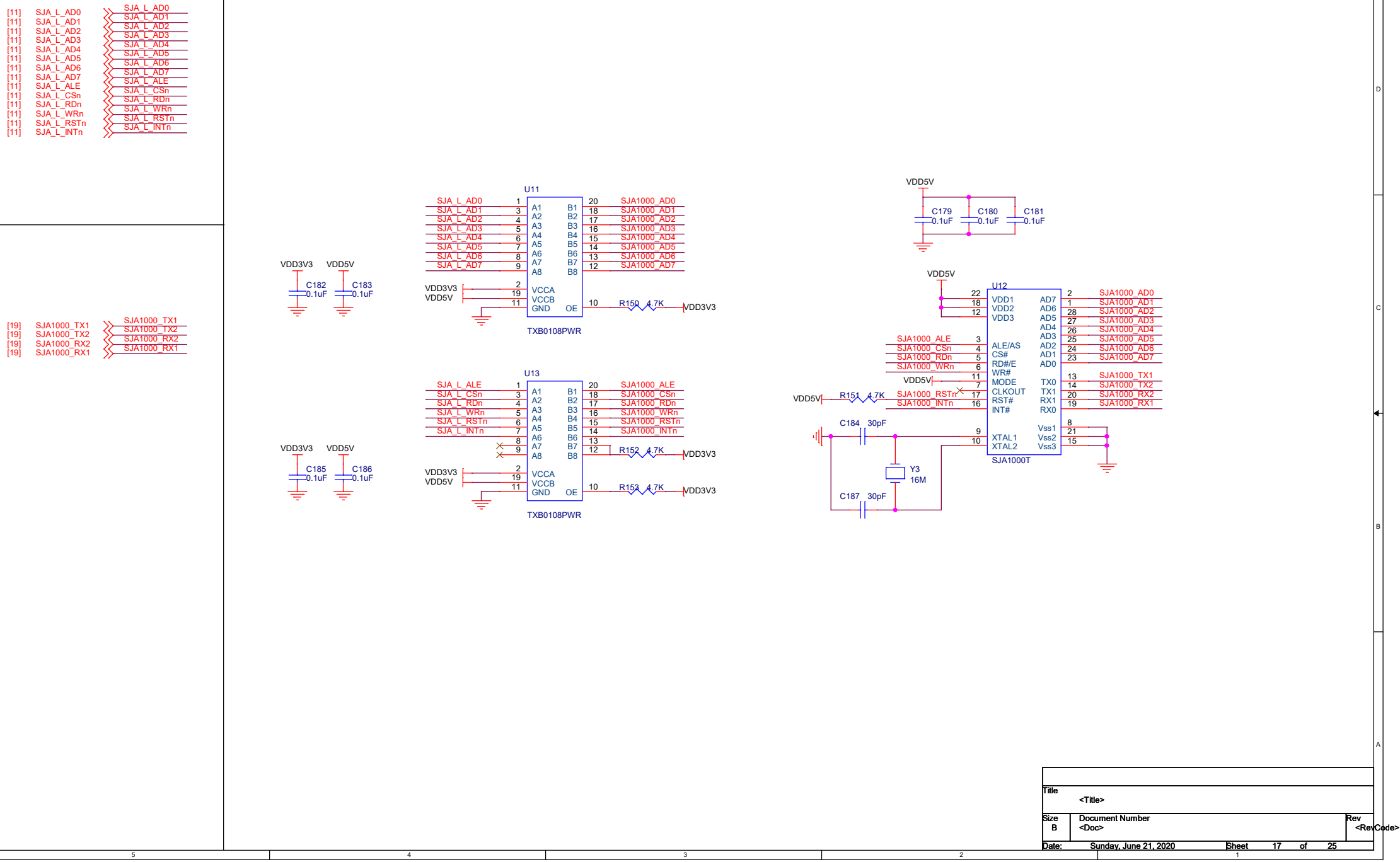

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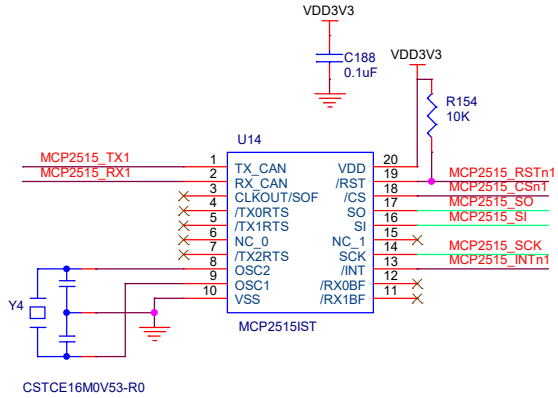
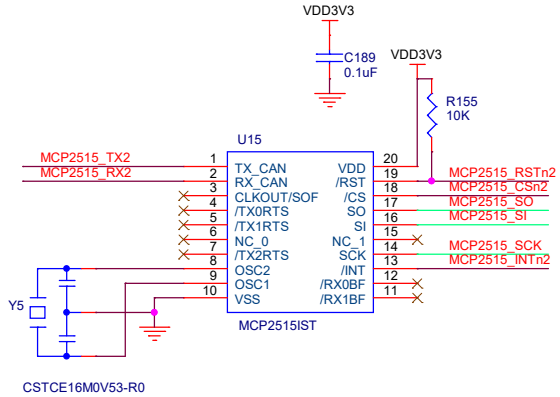
[5] MCP2515_RSTn1 → MCP2515_RSTn1
[5] MCP2515_RSTn2 → MCP2515_RSTn2

[5] MCP2515_CSn1 → MCP2515_CSn1
[5] MCP2515_CSn2 → MCP2515_CSn2
[5,10] MCP2515_SO → MCP2515_SO
[5,10] MCP2515_SI → MCP2515_SI
[5,10] MCP2515_SCK → MCP2515_SCK
[5] MCP2515_INTn1 → MCP2515_INTn1
[5] MCP2515_INTn2 → MCP2515_INTn2

[19] MCP2515_TX1 → MCP2515_TX1
[19] MCP2515_RX1 → MCP2515_RX1
[19] MCP2515_TX2 → MCP2515_TX2
[19] MCP2515_RX2 → MCP2515_RX2





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[10] FPGA_CANR[3:0] FPGA_CANR[3:0]

[10] FPGA_CAND[3:0] FPGA_CAND[3:0]

[25] CANH[7:0] CANH[7:0]

[25] CANL[7:0] CANL[7:0]

[18] MCP2515_TX1 MCP2515_TX1

[18] MCP2515_RX1 MCP2515_RX1

[18] MCP2515_TX2 MCP2515_TX2

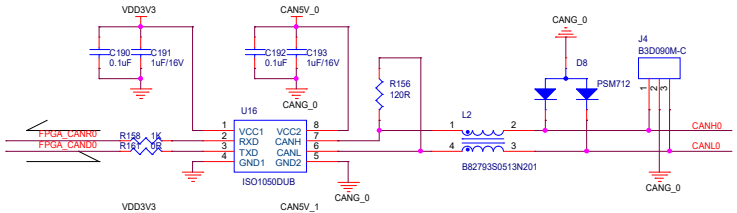
[18] MCP2515_RX2 MCP2515_RX2

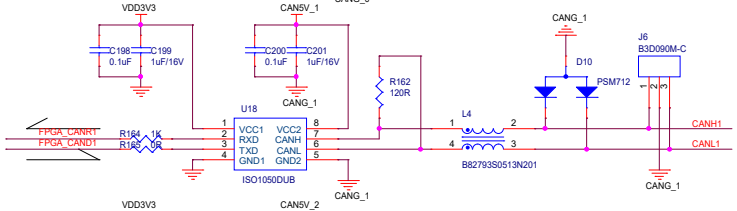
[17] SJA1000_TX1 SJA1000_TX1

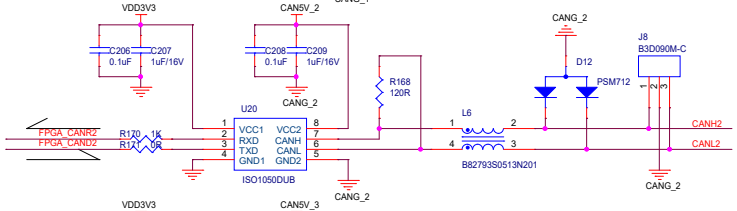
[17] SJA1000_TX2 SJA1000_TX2

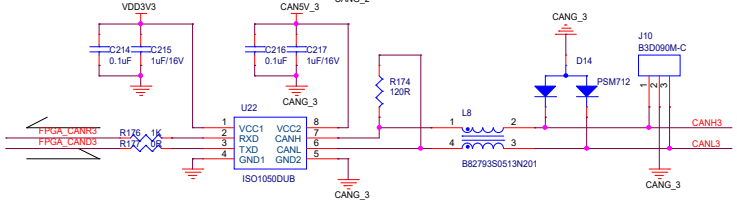
[17] SJA1000_RX2 SJA1000_RX2

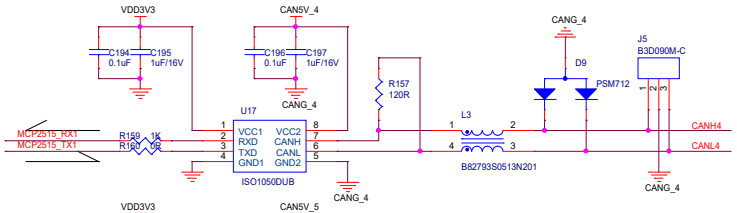
[17] SJA1000_RX1 SJA1000_RX1

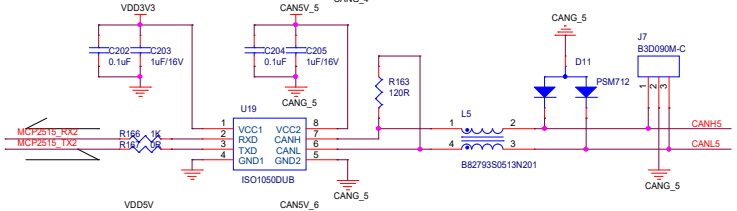


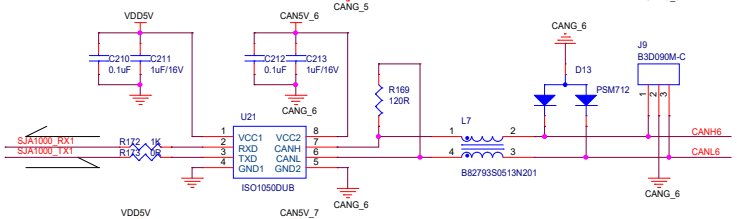


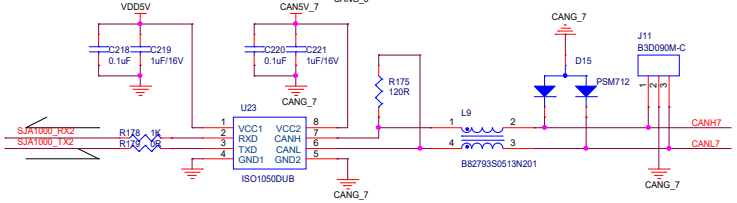


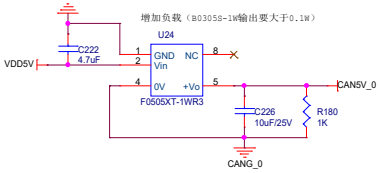


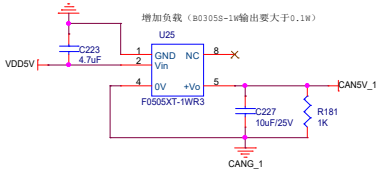


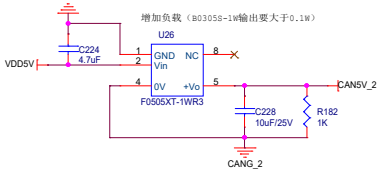


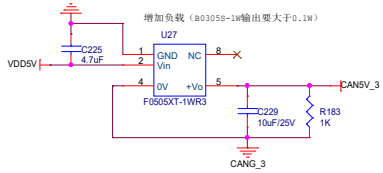


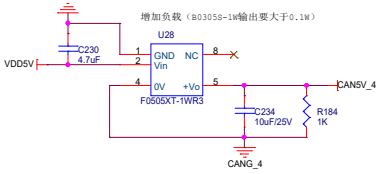


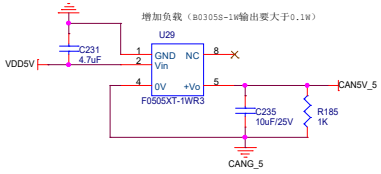


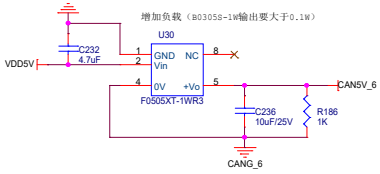


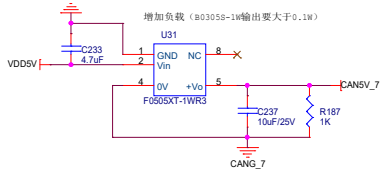












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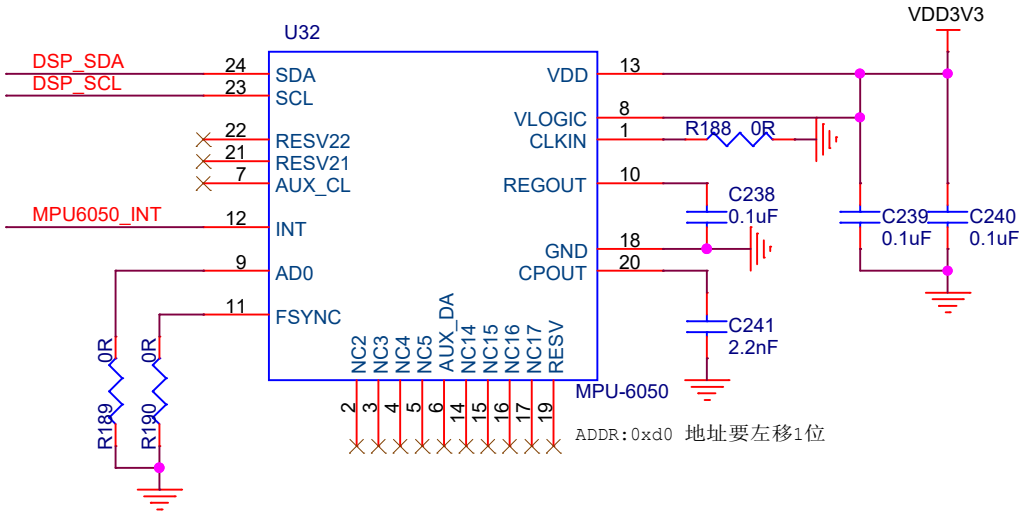
[5,15] DSP_SDA
[5,15] DSP_SCL
[5] MPU6050_INT



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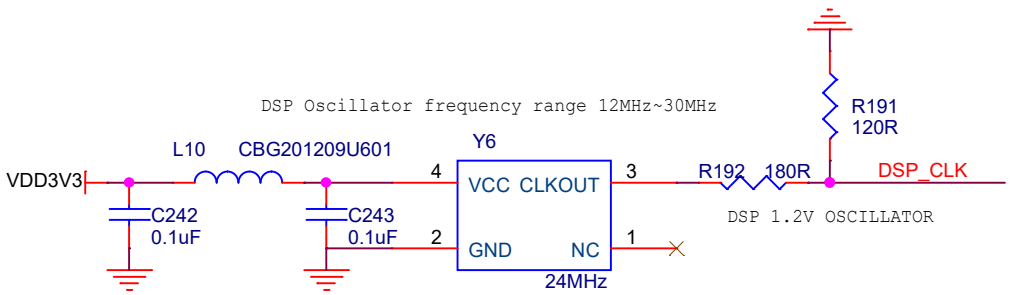
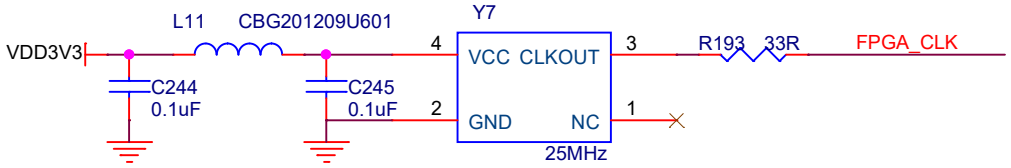
[3] DSP_RESETn >> DSP_RESETn

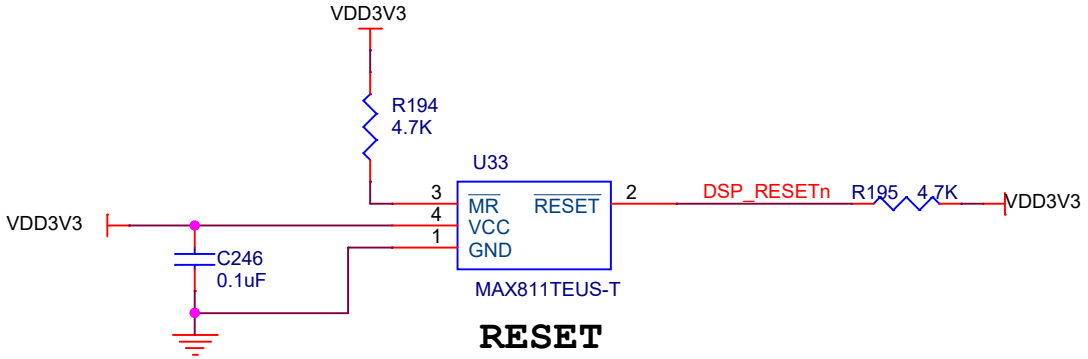
[3] DSP_CLK >> DSP_CLK

[10] FPGA_CLK >> FPGA_CLK





使用两个时钟方便更改为不同的频率



RESET

2018-10-24 CHECK OK

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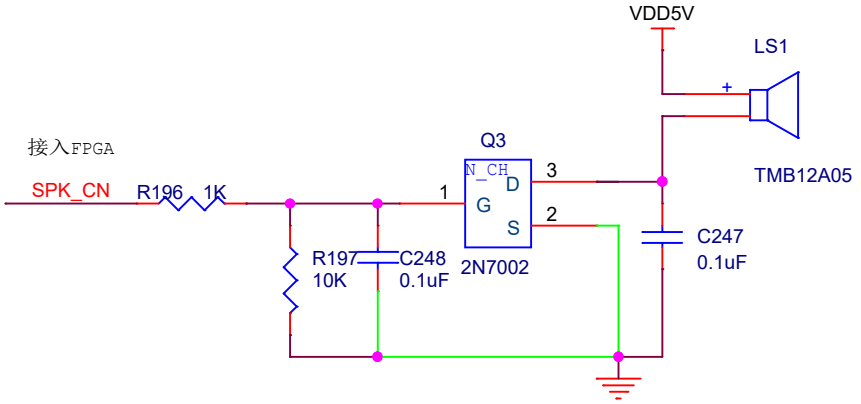
[10] SPK_CN SPK_CN



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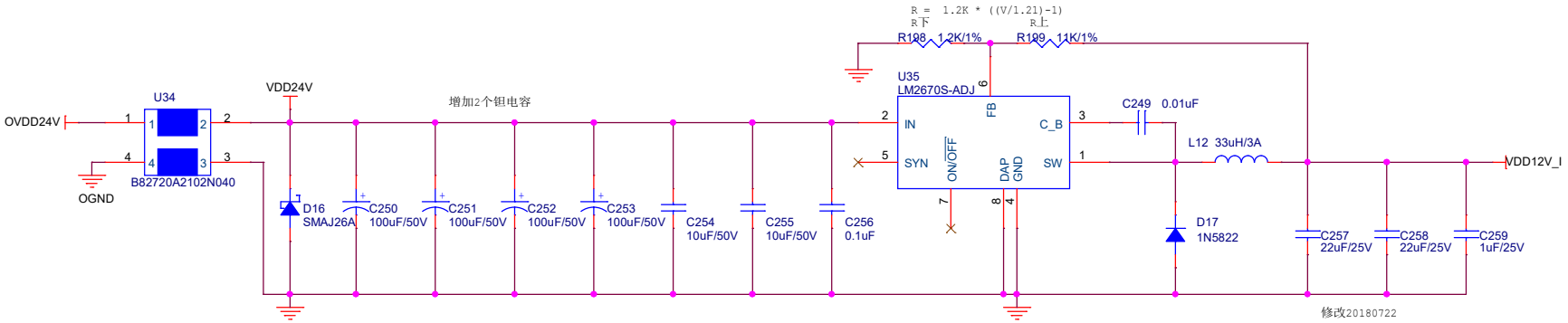

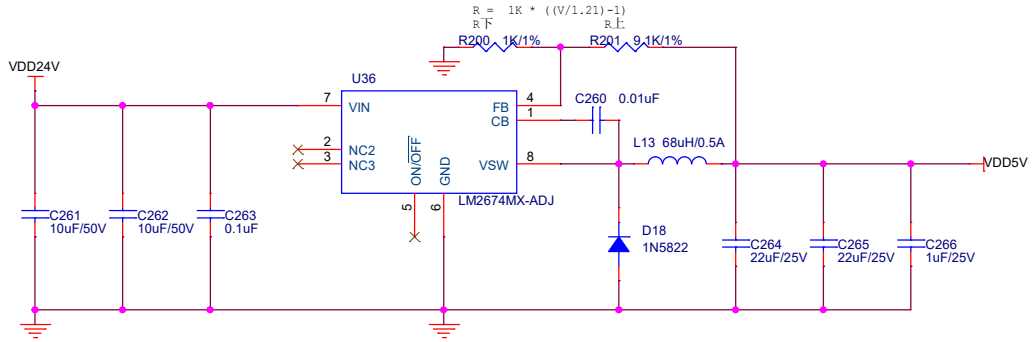

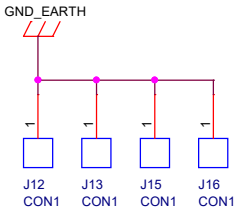

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Size B	Document Number <Doc>	Rev <RevCode>
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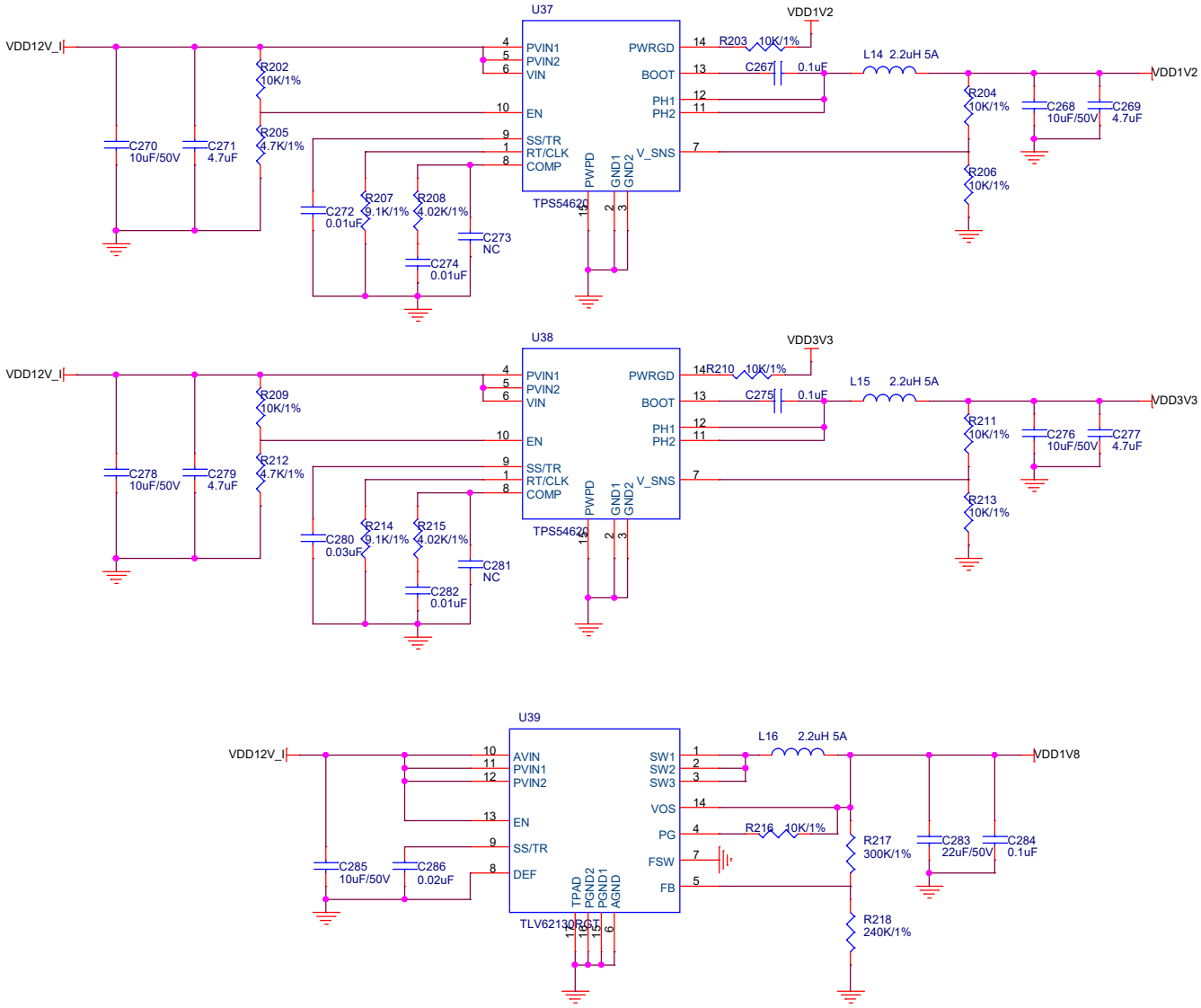

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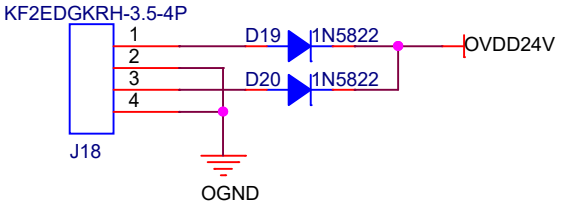
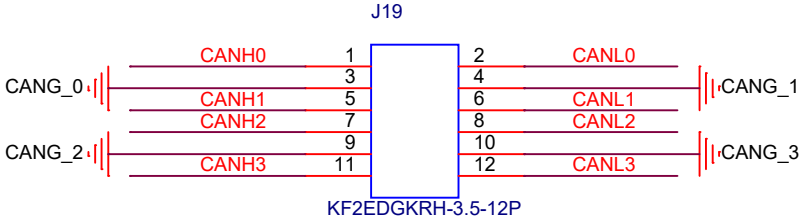
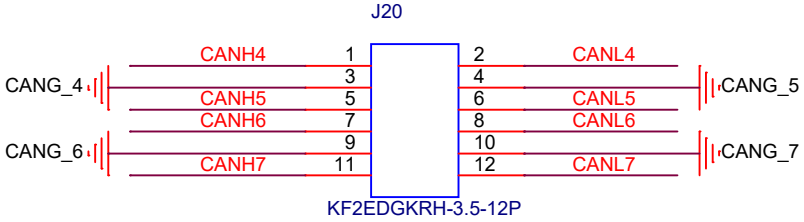
[19] CANH[7:0] CANH[7:0]

[19] CANL[7:0] CANL[7:0]







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