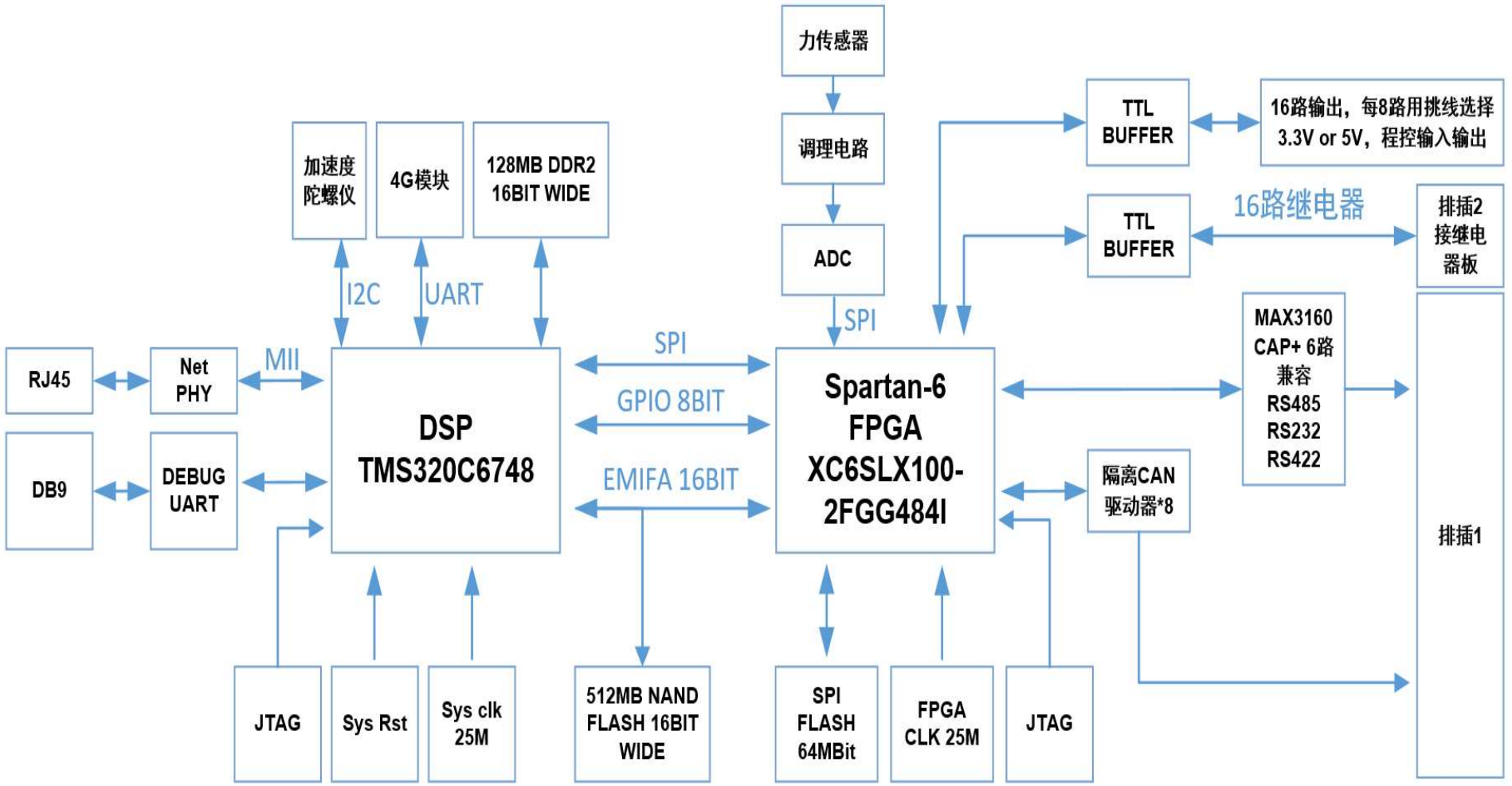
01_NOTE
02_BLOCK_DIAGRAM
03_C6748_MEMORY_IF_JTAG
04_C6748_DDR
05_C6748_PHERIPERALS
06_C6748_VP_CFG
07_C6748_PW
08_DDR2
09_NAND_FLASH
10_FPGA_BANK0_1
11_FPGA_BANK2_3
12_FPGA_PW
13_FPGA_CFG
14_DSP_UART
15_EEPROM
16_LAN8710_MII
17_LTE_MODULE
18_ISO_CAN
19_FPGA_UART
20_RELAY
21_DIGITAL_BUF
22_MEA_P
23_MPU9250
24_RST_CLK
25_POWER1
26_POWER2
27_PORT

调试记录：

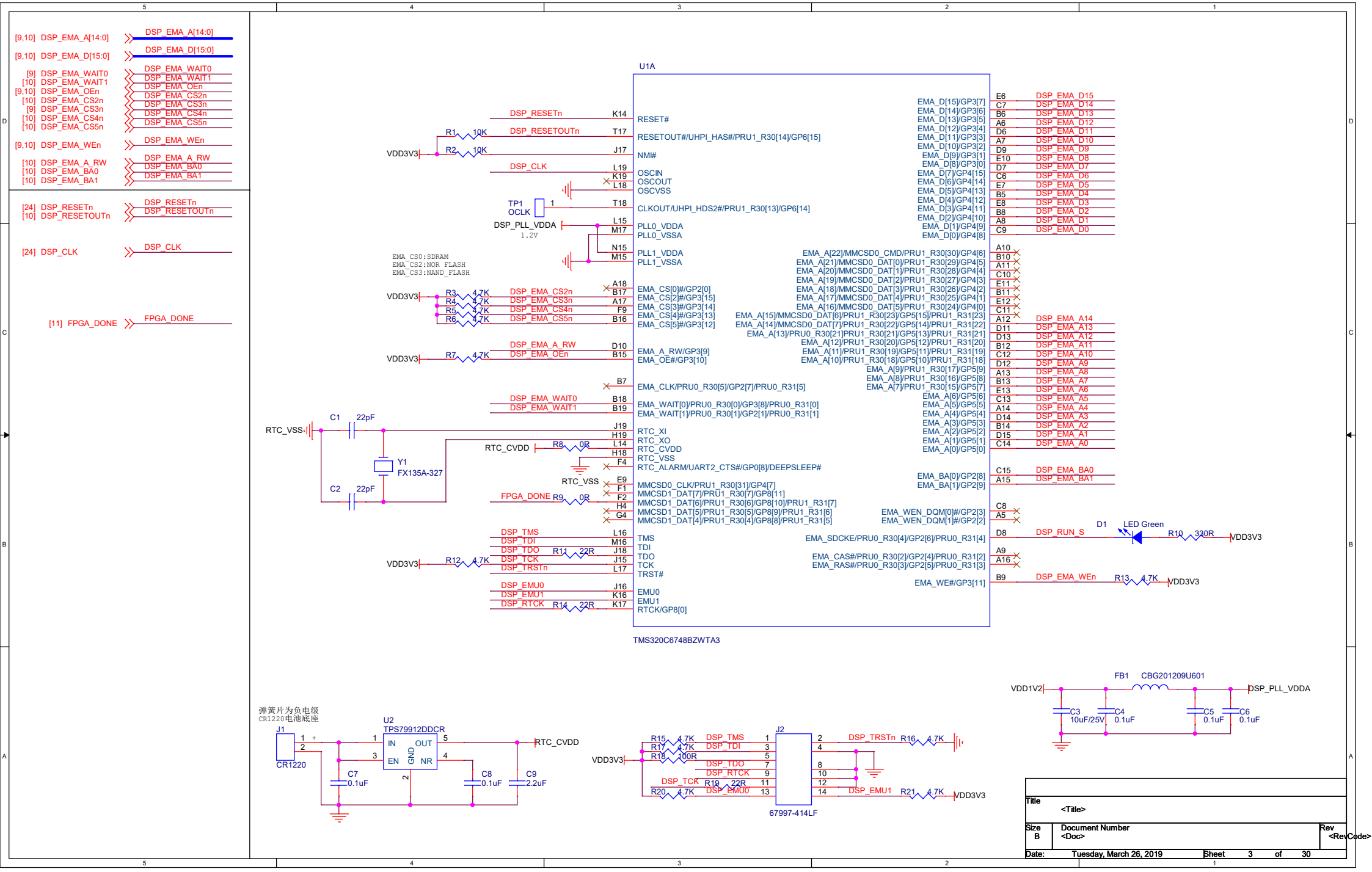
2018-11-19：R294改为11K，R295改为2.4K，R283改为9.1K
2018-12-10：R300改为1K，R301改为2K

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 1 of 30	




```
24V->IN12V->1.2V->1.8V->3.3V,5V->3.8V
   ->12VP->10VA
   ->12VN
```

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 2 of 30	


[9,10] DSP_EMA_A[14:0]
DSP_EMA_A[14:0]
[9,10] DSP_EMA_D[15:0]
DSP_EMA_D[15:0]
[9] DSP_EMA_WAIT0
[10] DSP_EMA_WAIT1
[9,10] DSP_EMA_OEn
[10] DSP_EMA_CS2n
[9] DSP_EMA_CS3n
[10] DSP_EMA_CS4n
[10] DSP_EMA_CS5n
[9,10] DSP_EMA_WEn
[10] DSP_EMA_A_RW
[10] DSP_EMA_BA0
[10] DSP_EMA_BA1
[24] DSP_RESETn
[10] DSP_RESETOUTn
[24] DSP_CLK
[11] FPGA_DONE
U1A
DSP_RESETn
DSP_RESETOUTn
DSP_CLK
DSP_PLL_VDDA
1.2V
EMA_CS0:SDRAM
EMA_CS2:NOR_FLASH
EMA_CS3:NAND_FLASH
DSP_EMA_CS2n
DSP_EMA_CS3n
DSP_EMA_CS4n
DSP_EMA_CS5n
DSP_EMA_A_RW
DSP_EMA_OEn
DSP_EMA_WAIT0
DSP_EMA_WAIT1
RTC_VSS
RTC_CVDD
FPGA_DONE
DSP_TMS
DSP_TDI
DSP_TDO
DSP_TCK
DSP_TRSTn
DSP_EMU0
DSP_EMU1
DSP_RTCK
TMS320C6748BZWTA3
弹簧片为负电级
CR1220电池底座
CR1220
TPS79912DDCR
DSP_RUN_S
LED Green
DSP_EMA_WEn
FB1
CBG201209U601
DSP_PLL_VDDA
67997-414LF
Title
<Title>
Size
B
Document Number
<Doc>
Rev
<RevCode>
Date:
Tuesday, March 26, 2019
Sheet
3
of
30

[8] DSP_DDR2_A[13:0] — DSP_DDR2_A[13:0]

[8] DSP_DDR2_DQ[15:0] — DSP_DDR2_DQ[15:0]

[8] DSP_DDR2_BA[2:0] — DSP_DDR2_BA[2:0]

[8] DSP_DDR2_DQS[1:0] — DSP_DDR2_DQS[1:0]

[8] DSP_DDR2_DQM[1:0] — DSP_DDR2_DQM[1:0]

[8] DSP_DDR2_CSn — DSP_DDR2_CSn

[8] DSP_DDR2_CASn — DSP_DDR2_CASn

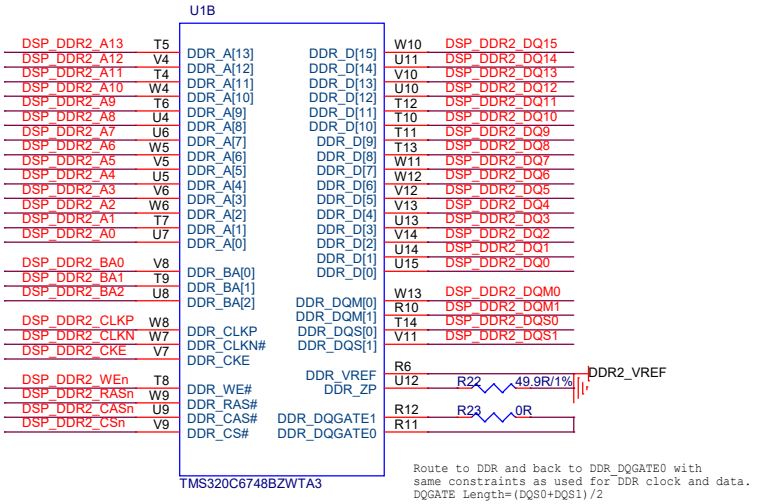
[8] DSP_DDR2_RASn — DSP_DDR2_RASn

[8] DSP_DDR2_WEn — DSP_DDR2_WEn

[8] DSP_DDR2_CKE — DSP_DDR2_CKE

[8] DSP_DDR2_CLKP — DSP_DDR2_CLKP

[8] DSP_DDR2_CLKN — DSP_DDR2_CLKN



Route to DDR and back to DDR_DQGATE0 with
same constraints as used for DDR clock and data.
DQGATE Length=(DQS0+DQS1)/2

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 4 of 30	

[16] LAN8710_MDIO
[16] LAN8710_MDC

[16] LAN8710_RXD3
[16] LAN8710_RXD2
[16] LAN8710_RXD1
[16] LAN8710_RXD0
[16] LAN8710_RXDV
[16] LAN8710_RXCLK
[16] LAN8710_RXER

[16] LAN8710_TXCLK
[16] LAN8710_TXEN
[16] LAN8710_TXD0
[16] LAN8710_TXD1
[16] LAN8710_TXD2
[16] LAN8710_TXD3
[16] LAN8710_COL
[16] LAN8710_CRS

[16] LAN8710_nINT

[15,23] DSP_SDA
[15,23] DSP_SCL

[23] MPU9250_INT
[15] AT24CXX_WP

[14] DSP_DEG_TX
[14] DSP_DEB_RX

[17] LTE_UART_TXD
[17] LTE_UART_RXD
[17] LTE_RESET

[10] DSP_FPGA_SCLK
[10] DSP_FPGA_nCS
[10] DSP_FPGA_SDI
[10] DSP_FPGA_SDO

[10] DSP_FPGA_D[7:0]

U1C

LAN8710_RXD0 D16
LAN8710_RXCLK D19
LAN8710_RXDV C17
LAN8710_MDIO D17
LAN8710_MDC E16
LAN8710_RXD1 E17
LAN8710_RXD2 D18
LAN8710_RXD3 C19
LAN8710_CRS C18
LAN8710_RXER C16

DSP_FPGA_SCLK G19
H16
DSP_FPGA_nCS E19
LTE_RESET F18
DSP_DEG_TX F19
DSP_DEB_RX E18
LTE_UART_TXD F16
LTE_UART_RXD F17
DSP_SDA G18
DSP_SCL G16
DSP_FPGA_SDI G17
DSP_FPGA_SDO H17

AT24CXX_WP R17
R16
U17
MPU9250_INT W15
U16
RST_SW T15
G1
G2
J4
G3

LED_RUN R5

SPI0_SCS[2]#/UART0_RTS#/GP8[1]/MII_RXD[0]
SPI0_CLK/EPWM0A/GP1[8]/MII_RXCLK
SPI0_ENA#/EPWM0B/PRU0_R30[6]/MII_RXDV
SPI0_SCS[0]#/TM64P1_OUT12/GP1[6]/MDIO_D/TM64P1_IN12
SPI0_SCS[1]#/TM64P0_OUT12/GP1[7]/MDIO_CLK/TM64PO_IN12
SPI0_SCS[3]#/UART0_CTS#/GP8[2]/MII_RXD[1]
SPI0_SCS[4]#/UART0_TXD/GP8[3]/MII_RXD[2]
SPI0_SCS[5]#/UART0_RXD/GP8[4]/MII_RXD[3]
SPI0_SIMO/EPWMSYNCO/GP8[5]/MII_CRS
SPI0_SOMI/EPWMSYNCI/GP8[6]/MII_RXER

SPI1_CLK/GP2[13]
SPI1_ENA/GP2[12]
SPI1_SCS[0]#/EPWM1B/PRU0_R30[7]/GP2[14]/TM64P3_IN12
SPI1_SCS[1]#/EPWM1A/PRU0_R30[8]/GP2[15]/TM64P2_IN12
SPI1_SCS[2]#/UART1_TXD/GP1[0]
SPI1_SCS[3]#/UART1_RXD/GP1[1]
SPI1_SCS[4]#/UART2_TXD/I2C1_SDA/GP1[2]
SPI1_SCS[5]#/UART2_RXD/I2C1_SCL/GP1[3]
SPI1_SCS[6]#/I2C0_SDA/TM64P3_OUT12/GP1[4]
SPI1_SCS[7]#/I2C0_SCL/TM64P2_OUT12/GP1[5]
SPI1_SIMO/GP2[10]
SPI1_SOMI/GP2[11]

PRU0_R30[31]/UHPI_HRDY#/PRU1_R30[12]/GP6[13]
PRU0_R30[30]/UHPI_HINT#/PRU1_R30[11]/GP6[12]
PRU0_R30[29]/UHPI_HCNTL0/UPP_CHA_CLOCK/GP6[11]
PRU0_R30[28]/UHPI_HCNTL1/UPP_CHA_START/GP6[10]
PRU0_R30[27]/UHPI_HHWIL/UPP_CHA_ENABLE/GP6[9]
PRU0_R30[26]/UHPI_HRW#/UPP_CHA_WAIT/GP6[8]PRU1_R31[17]
PRU0_R30[25]/MMCSD1_DAT[0]/UPP_CHB_CLOCK/GP8[15]/PRU1_R31[27]
PRU0_R30[24]/MMCSD1_CLK/UPP_CHB_START/GP8[14]/PRU1_R31[26]
PRU0_R30[23]/MMCSD1_CMD/UPP_CHB_ENABLE/GP8[13]/PRU1_R31[25]
PRU0_R30[22]/PRU1_R30[8]/UPP_CHB_WAIT/GP8[12]/PRU1_R31[24]

GP6[0]/PRU1_R31[28]

AXR15/EPWM0TZ[0]/ECAP2_APWM2/GP0[7]
AXR14/CLKR1/GP0[6]
AXR13/CLKX1/GP0[5]
AXR12/FSR1/GP0[4]
AXR11/FSX1/GP0[3]
AXR10/DR1/GP0[2]
AXR9/DX1/GP0[1]
AXR8/CLKS1/ECAP1_APWM1/GP0[0]/PRU0_R31[8]
AXR7/EPWM1TZ[0]/PRU0_R30[17]/GP1[15]/PRU0_R31[7]
AXR6/CLKR0/GP1[14]/MII_TXEN/PRU0_R31[6]
AXR5/CLKX0/GP1[13]/MII_TXCLK
AXR4/FSR0/GP1[12]/MII_COL
AXR3/FSX0/GP1[11]/MII_TXD[3]
AXR2/DR0/GP1[10]/MII_TXD[2]
AXR1/DX0/GP1[9]/MII_TXD[1]
AXR0/ECAP0_APWM0/GP8[7]/MII_TXD[0]/CLKS0
AHCLKX3/USB_REFCLKIN/UART1_CTS#/GP0[10]/PRU0_R31[17]
ACLKX/PRU0_R30[19]/GP0[14]/PRU0_R31[21]
AFSX/GP0[12]/PRU0_R31[19]
AHCLKR/PRU0_R30[18]/UART1_RTS#/GP0[11]/PRU0_R31[18]
ACLKR/PRU0_R30[20]/GP0[15]/PRU0_R31[22]
AFSR/GP0[13]/PRU0_R31[20]
AMUTE/PRU0_R30[16]/UART2_RTS#/GP0[9]/PRU0_R31[16]

A4 DSP_FPGA_D7
B4 DSP_FPGA_D6
B3 DSP_FPGA_D5
C4 DSP_FPGA_D4
C5 DSP_FPGA_D3
D4 DSP_FPGA_D2
C3 DSP_FPGA_D1
E4 DSP_FPGA_D0
D2
C1 LAN8710_TXEN
D3 LAN8710_TXCLK
D1 LAN8710_COL
E3 R24 100R LAN8710_TXD3
E2 R25 100R LAN8710_TXD2
E1 R26 100R LAN8710_TXD1
F3 R27 100R LAN8710_TXD0
A3
B1
B2
A2
A1 LAN8710_nINT
C2
D5

K18
N19
P16
M19
M18 NOT USE USB

P19
P18

N1
N2
J2
J1 NOT USE SATA
L2
L1

USB0_DRVVBUS
USB0_VBUS
USB0_ID
USB0_DP
USB0_DM

USB1_DP
USB1_DM

SATA_REFCLKN#
SATA_REFCLKP
SATA_TXN#
SATA_TXP
SATA_RXN#
SATA_RXP

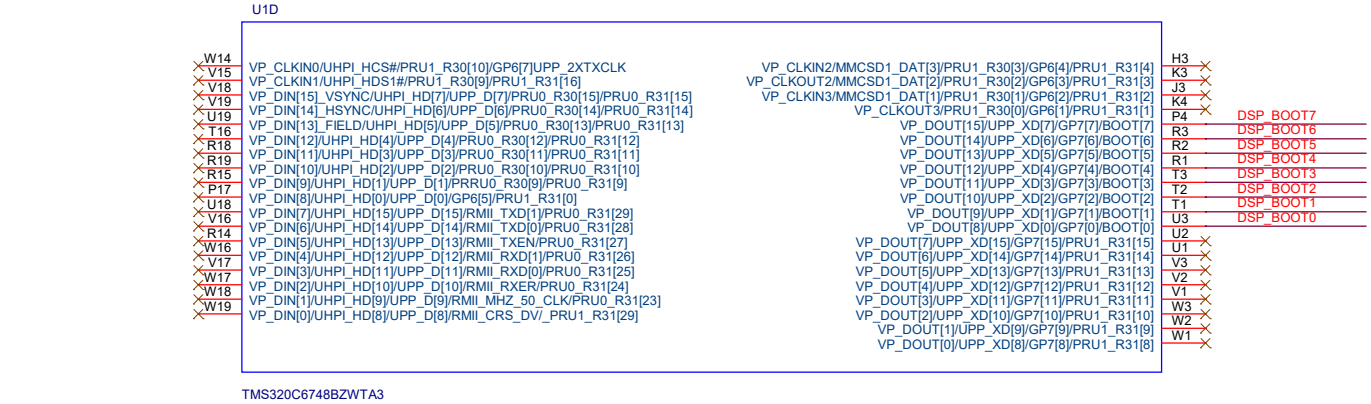
TMS320C6748BZWTA3

SW PUSHBUTTON-SPST-2
C10 0.1uF
R28 10K
4 1 RST_SW
3 2 R29 1K VDD3V3
SW1

D2
R30 10K VDD24V
LED_RUN
R33 1K VDD3V3
SSB-LX2300

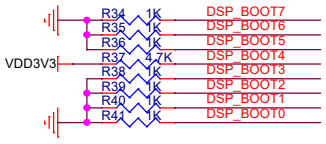
DSP_SDA R31 2K VDD3V3
DSP_SCL R32 2K

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 5 of 30	



BOOT[7:0]	BOOT MODE	AIS
0xx1 0000	NAND16	Yes

BOOT[6:5]	BLOCK	PLL0 Applied
00	1	None
01	1	PLLM=24,POSTDIV=3,SYSCLK3=2
10	0	None
11	0	PLLM=24,POSTDIV=3,SYSCLK3=2



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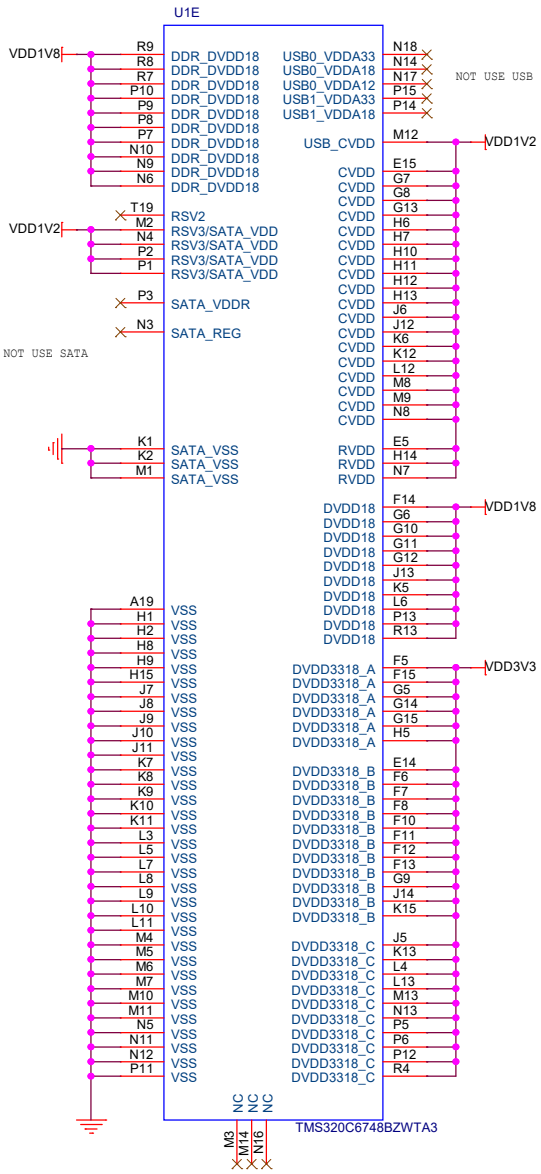
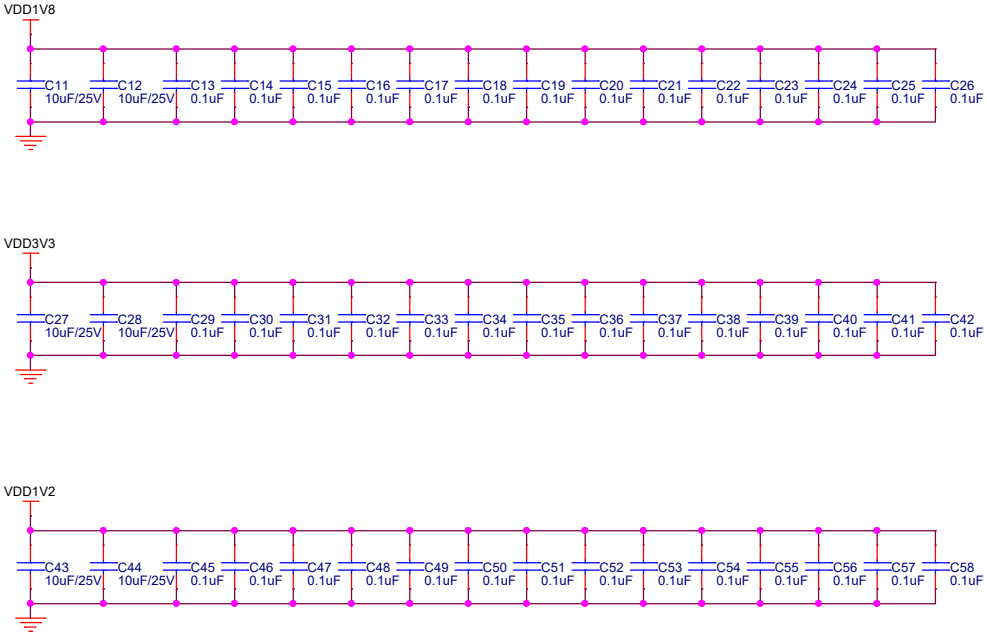
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 6 of 30	





Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 7 of 30	

[4] DSP_DDR2_A[13:0] — DSP_DDR2_A[13:0]
[4] DSP_DDR2_DQ[15:0] — DSP_DDR2_DQ[15:0]
[4] DSP_DDR2_BA[2:0] — DSP_DDR2_BA[2:0]
[4] DSP_DDR2_DQS[1:0] — DSP_DDR2_DQS[1:0]
[4] DSP_DDR2_DQM[1:0] — DSP_DDR2_DQM[1:0]
[4] DSP_DDR2_CSn — DSP_DDR2_CSn
[4] DSP_DDR2_CASn — DSP_DDR2_CASn
[4] DSP_DDR2_RASn — DSP_DDR2_RASn
[4] DSP_DDR2_WEn — DSP_DDR2_WEn
[4] DSP_DDR2_CKE — DSP_DDR2_CKE
[4] DSP_DDR2_CLKP — DSP_DDR2_CLKP
[4] DSP_DDR2_CLKN — DSP_DDR2_CLKN

DDR-2 128MByte

U3 — MT47H64M16HR

DSP_DDR2_A0	R42	10R	M8	A0			
DSP_DDR2_A1	R43	10R	M3	A1			
DSP_DDR2_A2	R44	10R	M7	A2			
DSP_DDR2_A3	R45	10R	N2	A3			
DSP_DDR2_A4	R46	10R	N8	A4			
DSP_DDR2_A5	R52	10R	N3	A5			
DSP_DDR2_A6	R53	10R	N7	A6			
DSP_DDR2_A7	R54	10R	P2	A7			
DSP_DDR2_A8	R47	10R	P8	A8			
DSP_DDR2_A9	R48	10R	P3	A9			
DSP_DDR2_A10	R49	10R	M2	A10			
DSP_DDR2_A11	R50	10R	P7	A11			
DSP_DDR2_A12	R51	10R	R2	A12			
DSP_DDR2_BA0	R55	22R	L2	BA0			
DSP_DDR2_BA1	R56	22R	L3	BA1			
DSP_DDR2_BA2	R57	22R	L1	BA2			
	R59	4.7K/1%	K9	ODT			
DSP_DDR2_CSn	R61	22R	L8	CSn			
DSP_DDR2_CASn	R63	22R	L7	CASn			
DSP_DDR2_RASn	R65	22R	K7	RASn			
DSP_DDR2_WEn	R66	22R	K3	WEn			
DSP_DDR2_CKE	R67	22R	K2	CKE			
DSP_DDR2_CLKP	R72	10R	J8	CK			
DSP_DDR2_CLKN	R73	10R	K8	CKn			
DSP_DDR2_DQS1	R77	22R	B7	UDQS			
DSP_DDR2_DQS0	R79	22R	F7	LDQS			
DSP_DDR2_DQM1	R83	22R	B3	UDM			
DSP_DDR2_DQM0	R85	22R	F3	LDM			
			A2	NC1			
			E2	NC2			
			A8	UDQSn/NU			
			E8	LDQSn/NU			
			R3	RFU2			
			R7	RFU3			
DSP_DDR2_A13	R88	10R	R8	RFU1			

VDD1V8				VDD5	A1		
				VDD4	E1		
				VDD3	M9		
				VDD2	R1		
				VDD1	J9		
				VDDL	J1		
				VDDQ10	A9		
				VDDQ9	C1		
				VDDQ8	C3		
				VDDQ7	C7		
				VDDQ6	C9		
				VDDQ5	G3		
				VDDQ4	E9		
				VDDQ3	G1		
				VDDQ2	G7		
				VDDQ1	G9		
DDR2_VREF				VREF	J2		
DSP_DDR2_DQ0	R58	10R	G8	DQ0			
DSP_DDR2_DQ1	R60	10R	G2	DQ1			
DSP_DDR2_DQ2	R62	10R	H7	DQ2			
DSP_DDR2_DQ3	R64	10R	H3	DQ3			
DSP_DDR2_DQ4	R68	10R	H1	DQ4			
DSP_DDR2_DQ5	R69	10R	H9	DQ5			
DSP_DDR2_DQ6	R70	10R	F1	DQ6			
DSP_DDR2_DQ7	R71	10R	F9	DQ7			
DSP_DDR2_DQ8	R74	10R	C8	DQ8			
DSP_DDR2_DQ9	R75	10R	C2	DQ9			
DSP_DDR2_DQ10	R76	10R	D7	DQ10			
DSP_DDR2_DQ11	R78	10R	D3	DQ11			
DSP_DDR2_DQ12	R81	10R	D1	DQ12			
DSP_DDR2_DQ13	R82	10R	D9	DQ13			
DSP_DDR2_DQ14	R84	10R	B1	DQ14			
DSP_DDR2_DQ15	R86	10R	B9	DQ15			
			A3	VSS5			
			E3	VSS4			
			J3	VSS3			
			N1	VSS2			
			P9	VSS1			
			A7	VSSQ10			
			B2	VSSQ9			
			B8	VSSQ8			
			D2	VSSQ7			
			D8	VSSQ6			
			E7	VSSQ5			
			F2	VSSQ4			
			F8	VSSQ3			
			H2	VSSQ2			
			H8	VSSQ1			
			J7	VSSDL			

VDD1V8
C60 0.1uF, C61 0.1uF, C62 0.1uF, C63 0.1uF, C59 0.1uF, C64 0.1uF, C65 10uF/25V

VDD1V8
C66 0.1uF, C67 0.1uF, C68 0.1uF, C69 0.1uF, C70 0.1uF, C71 0.1uF, C72 0.1uF, C73 0.1uF, C74 0.1uF, C75 0.1uF, C76 10uF/25V

VDD1V8
DDR2_VREF
C77 0.1uF, R80 1K/1%
C78 0.1uF, R87 1K/1%

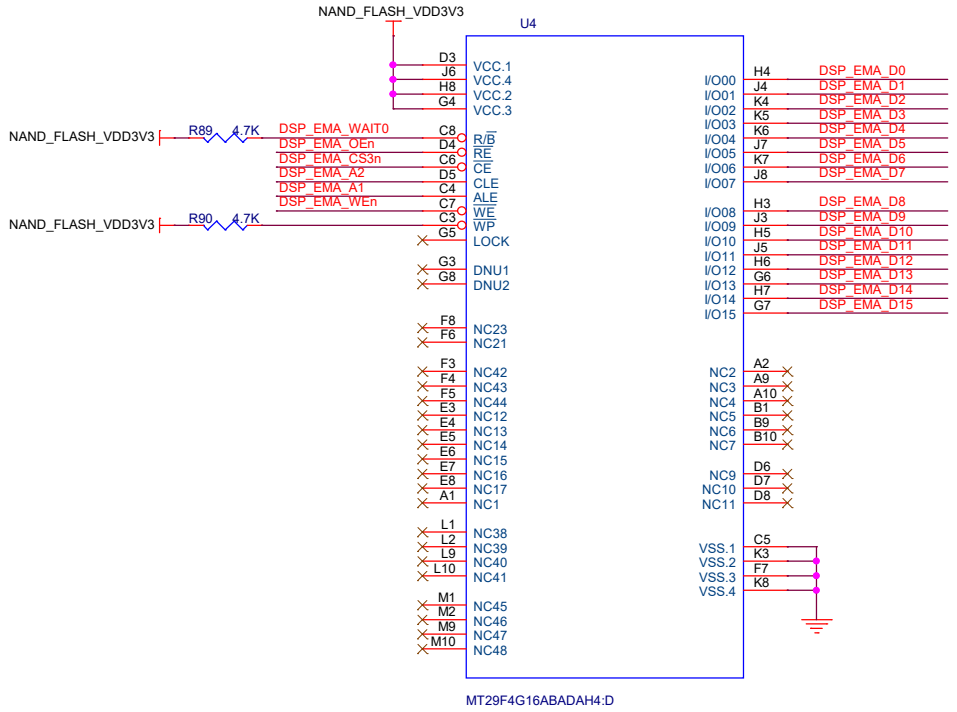
Title	<Title>		
Size B	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 8 of 30		

[3,10] DSP_EMA_D[15:0] — DSP_EMA_D[15:0]

[3] DSP_EMA_WAIT0 — DSP_EMA_WAIT0
[3,10] DSP_EMA_OEn — DSP_EMA_OEn
[3] DSP_EMA_CS3n — DSP_EMA_CS3n
[3,10] DSP_EMA_WEn — DSP_EMA_WEn

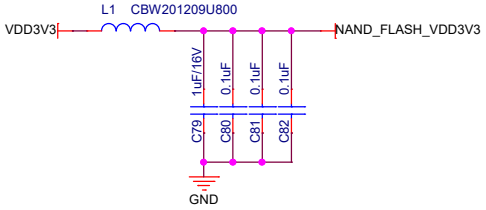
[3,10] DSP_EMA_A[12:0] — DSP_EMA_A[12:0]

NAND FLASH 512MByte



MT29F4G16ABADAH4:D

DECAPs FOR FLASH



Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 9 of 30	

[3,9] DSP_EMA_A[14:0] — DSP_EMA_A[14:0]

[3,9] DSP_EMA_D[15:0] — DSP_EMA_D[15:0]

[3] DSP_EMA_WAIT1 — DSP_EMA_WAIT1
[3,9] DSP_EMA_OEn — DSP_EMA_OEn
[3] DSP_EMA_CS2n — DSP_EMA_CS2n
[3] DSP_EMA_CS4n — DSP_EMA_CS4n
[3] DSP_EMA_CS5n — DSP_EMA_CS5n

[3,9] DSP_EMA_WEn — DSP_EMA_WEn

[3] DSP_EMA_A_RW — DSP_EMA_A_RW
[3] DSP_EMA_BA0 — DSP_EMA_BA0
[3] DSP_EMA_BA1 — DSP_EMA_BA1

[18] FPGA_CANR[7:0] — FPGA_CANR[7:0]
[18] FPGA_CAND[7:0] — FPGA_CAND[7:0]

[24] FPGA_CLK — FPGA_CLK

[27] IO_LVTTL1 — IO_LVTTL1
[27] IO_LVTTL2 — IO_LVTTL2
[27] IO_LVTTL3 — IO_LVTTL3
[27] IO_LVTTL4 — IO_LVTTL4
[27] IO_LVTTL5 — IO_LVTTL5
[27] IO_LVTTL6 — IO_LVTTL6
[27] IO_LVTTL7 — IO_LVTTL7
[27] IO_LVTTL8 — IO_LVTTL8

[25] SPK_CN — SPK_CN

[27] IO_LVTTLEN — IO_LVTTLEN

[17] GPS_RXD — GPS_RXD
[17] GPS_TXD — GPS_TXD
[17] GPS_PPS — GPS_PPS

[3] DSP_RESETOUTn — DSP_RESETOUTn

[16] LAN8710_nRST — LAN8710_nRST

[5] DSP_FPGA_SCLK — DSP_FPGA_SCLK
[5] DSP_FPGA_nCS — DSP_FPGA_nCS
[5] DSP_FPGA_SDI — DSP_FPGA_SDI
[5] DSP_FPGA_SDO — DSP_FPGA_SDO

[5] DSP_FPGA_D[7:0] — DSP_FPGA_D[7:0]

U5A

R91 1K

	A3	IO_L1P_HSWAPEN_0	IO_L36P_GCLK15_0	D11	
	A4	IO_L1N_VREF_0	IO_L36N_GCLK14_0	C12	DSP_EMA_D1
DSP_EMA_A_RW	C5	IO_L2P_0	IO_L37P_GCLK13_0	B12	DSP_EMA_D2
DSP_EMA_A11	A5	IO_L2N_0	IO_L37N_GCLK12_0	A12	
DSP_EMA_A13	D6	IO_L3P_0	IO_L38P_0	C13	
DSP_EMA_D8	C6	IO_L3N_0	IO_L38N_VREF_0	A13	DSP_EMA_D4
DSP_EMA_D9	B6	IO_L4P_0	IO_L43P_0	E12	DSP_EMA_D0
DSP_EMA_CS4n	A6	IO_L4N_0	IO_L43N_0	D12	DSP_FPGA_D7
DSP_EMA_D11	C7	IO_L5P_0	IO_L44P_0	H12	DSP_FPGA_SDO
DSP_EMA_D10	A7	IO_L5N_0	IO_L44N_0	F12	DSP_EMA_A5
DSP_EMA_D12	B8	IO_L6P_0	IO_L45P_0	F13	DSP_FPGA_nCS
DSP_EMA_CS2n	A8	IO_L6N_0	IO_L45N_0	D13	DSP_FPGA_D6
DSP_EMA_A4	D9	IO_L7P_0	IO_L46P_0	H13	DSP_EMA_A3
DSP_EMA_D13	C8	IO_L7N_0	IO_L46N_0	G13	DSP_EMA_BA0
DSP_EMA_D14	C9	IO_L8P_0	IO_L47P_0	E14	DSP_EMA_D3
DSP_EMA_A14	A9	IO_L8N_VREF_0	IO_L47N_0	F15	DSP_EMA_D5
DSP_EMA_A9	E8	IO_L14P_0	IO_L48P_0	F14	DSP_FPGA_SDI
DSP_EMA_A7	F8	IO_L14N_0	IO_L48N_0	H14	DSP_EMA_A6
DSP_EMA_A8	G8	IO_L15P_0	IO_L49P_0	D14	DSP_FPGA_D5
DSP_EMA_A0	F9	IO_L15N_0	IO_L49N_0	C14	DSP_EMA_D6
DSP_EMA_A12	G9	IO_L16P_0	IO_L50P_0	B14	DSP_FPGA_D4
DSP_EMA_WAIT1	H10	IO_L16N_0	IO_L50N_0	A14	
	E10	IO_L17P_0	IO_L51P_0	C15	
DSP_FPGA_SCLK	F10	IO_L17N_0	IO_L51N_0	A15	IO_LVTTLEN
	G11	IO_L18P_0	IO_L62P_0	D15	
DSP_EMA_A10	H11	IO_L18N_0	IO_L62N_VREF_0	C16	
DSP_EMA_CS5n	D7	IO_L32P_0	IO_L63P_SCP7_0	B16	DSP_FPGA_D1
DSP_EMA_BA1	D8	IO_L32N_0	IO_L63N_SCP6_0	A16	
DSP_EMA_A1	D10	IO_L33P_0	IO_L64P_SCP5_0	C17	
DSP_EMA_D15	C10	IO_L33N_0	IO_L64N_SCP4_0	A17	DSP_FPGA_D3
DSP_EMA_WEn	B10	IO_L34P_GCLK19_0	IO_L65P_SCP3_0	B18	DSP_FPGA_D2
DSP_EMA_OEn	A10	IO_L34N_GCLK18_0	IO_L65N_SCP2_0	A18	DSP_FPGA_D0
DSP_EMA_A2	C11	IO_L35P_GCLK17_0	IO_L66P_SCP1_0	E16	DSP_EMA_D7
	A11	IO_L35N_GCLK16_0	IO_L66N_SCP0_0	D17	

XC6SLX100-2FGG484I

U5B

	C19	IO_L1P_A25_1	IO_L43P_GCLK5_M1DQ4_1	J20	
	B20	IO_L1N_A24_VREF_1	IO_L43N_GCLK4_M1DQ5_1	J22	FPGA_CLK
FPGA_CAND1	G16	IO_L9P_1	IO_L44P_A3_M1DQ6_1	K21	
FPGA_CANR0	G17	IO_L9N_1	IO_L44N_A2_M1DQ7_1	K22	
FPGA_CAND2	F16	IO_L10P_1	IO_L45P_A1_M1LDQS_1	L20	
FPGA_CAND0	F17	IO_L10N_1	IO_L45N_A0_M1LDQSN_1	L22	
FPGA_CAND5	B21	IO_L19P_1	IO_L46P_FCS_B_M1DQ2_1	M21	
	B22	IO_L19N_1	IO_L46N_FOE_B_M1DQ3_1	M22	
FPGA_CANR5	A20	IO_L20P_1	IO_L47P_FWE_B_M1DQ0_1	N20	LAN8710_nRST
FPGA_CANR4	A21	IO_L20N_1	IO_L47N_LDC_M1DQ1_1	N22	
	K16	IO_L21P_1	IO_L48P_HDC_M1DQ8_1	P21	
FPGA_CAND3	J16	IO_L21N_1	IO_L48N_M1DQ9_1	P22	
FPGA_CANR1	H16	IO_L28P_1	IO_L49P_M1DQ10_1	R20	
FPGA_CANR2	H17	IO_L28N_VREF_1	IO_L49N_M1DQ11_1	R22	IO_LVTTL1
FPGA_CAND7	D19	IO_L29P_A23_M1A13_1	IO_L50P_M1UDQS_1	T21	IO_LVTTL4
FPGA_CAND6	D20	IO_L29N_A22_M1A14_1	IO_L50N_M1UDQSN_1	T22	IO_LVTTL6
FPGA_CANR7	F18	IO_L30P_A21_M1RESET_1	IO_L51P_M1DQ12_1	U20	IO_LVTTL3
FPGA_CANR6	F19	IO_L30N_A20_M1A11_1	IO_L51N_M1DQ13_1	U22	IO_LVTTL2
FPGA_CAND4	D21	IO_L31P_A19_M1CKE_1	IO_L52P_M1DQ14_1	V21	IO_LVTTL5
	D22	IO_L31N_A18_M1A12_1	IO_L52N_M1DQ15_1	V22	
	C20	IO_L32P_A17_M1A8_1	IO_L53P_1	M19	IO_LVTTL8
	C22	IO_L32N_A16_M1A9_1	IO_L53N_VREF_1	N19	FPGA_CANR3
	G19	IO_L33P_A15_M1A10_1	IO_L58P_1	M16	
	F20	IO_L33N_A14_M1A4_1	IO_L58N_1	L15	
	H19	IO_L34P_A13_M1WE_1	IO_L59P_1	P19	
	H18	IO_L34N_A12_M1BA2_1	IO_L74N_DOUT_BUSY_1	T20	
	E20	IO_L35P_A11_M1A7_1	IO_L59N_1	P20	DSP_RESETOUTn
	E22	IO_L35N_A10_M1A2_1	IO_L60P_1	W20	
	J17	IO_L36P_A9_M1BA0_1	IO_L60N_1	W22	
	K17	IO_L36N_A8_M1BA1_1	IO_L61P_1	L17	
	F21	IO_L37P_A7_M1A0_1	IO_L61N_1	K18	
	F22	IO_L37N_A6_M1A1_1	IO_L70P_1	U19	IO_LVTTL7
	H20	IO_L38P_A5_M1CLK_1	IO_L70N_1	V20	
	J19	IO_L38N_A4_M1CLKN_1	IO_L71P_1	M17	
	G20	IO_L39P_M1A3_1	IO_L71N_1	M18	
	G22	IO_L39N_M1ODT_1	IO_L72P_1	P17	
GPS_RXD	K20	IO_L40P_GCLK11_M1A5_1	IO_L72N_1	N16	
GPS_TXD	K19	IO_L40N_GCLK10_M1A6_1	IO_L73P_1	P18	FPGA_RUN_S
GPS_PPS	H21	IO_L41P_GCLK9_IRDY1_M1RASN_1	IO_L73N_1	R19	SPK_CN
	H22	IO_L41N_GCLK8_M1CASN_1	IO_L74P_AWAKE_1	T19	
	M20	IO_L42P_GCLK7_M1UDM_1			
	L19	IO_L42N_GCLK6_TRDY1_M1LDM_1			

XC6SLX100-2FGG484I

FPGA_RUN_S — D3 LED Green — R92 330R — VDD3V3

Title	<Title>		
Size B	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 10 of 30		

[3] FPGA_DONE — FPGA_DONE

[13] CFG_SPI_CS — CFG_SPI_CS
[13] CFG_SPI_MISO — CFG_SPI_MISO
[13] CFG_SPI_CCLK — CFG_SPI_CCLK
[13] CFG_SPI_MOSI — CFG_SPI_MOSI

[13] FPGA_M0 — FPGA_M0
[13] FPGA_M1 — FPGA_M1

[19] RS485_RX1 — RS485_RX1
[19] RS485_RX2 — RS485_RX2
[19] RS485_RX3 — RS485_RX3
[19] RS485_RX4 — RS485_RX4

[19] RS485_TX1 — RS485_TX1
[19] RS485_TX2 — RS485_TX2
[19] RS485_TX3 — RS485_TX3
[19] RS485_TX4 — RS485_TX4

[19] RS485_RD1 — RS485_RD1
[19] RS485_RD2 — RS485_RD2
[19] RS485_RD3 — RS485_RD3
[19] RS485_RD4 — RS485_RD4

[19] UART_TX1 — UART_TX1
[19] UART_TX2 — UART_TX2
[19] UART_TX3 — UART_TX3
[19] UART_TX4 — UART_TX4

[19] UART_RX1 — UART_RX1
[19] UART_RX2 — UART_RX2
[19] UART_RX3 — UART_RX3
[19] UART_RX4 — UART_RX4

[21] LVTTL_I1 — LVTTL_I1
[21] LVTTL_I2 — LVTTL_I2
[21] LVTTL_I3 — LVTTL_I3
[21] LVTTL_I4 — LVTTL_I4
[21] LVTTL_I5 — LVTTL_I5
[21] LVTTL_I6 — LVTTL_I6
[21] LVTTL_I7 — LVTTL_I7
[21] LVTTL_I8 — LVTTL_I8

[21] LVTTL_O1 — LVTTL_O1
[21] LVTTL_O2 — LVTTL_O2
[21] LVTTL_O3 — LVTTL_O3
[21] LVTTL_O4 — LVTTL_O4
[21] LVTTL_O5 — LVTTL_O5
[21] LVTTL_O6 — LVTTL_O6
[21] LVTTL_O7 — LVTTL_O7
[21] LVTTL_O8 — LVTTL_O8

[20] BUF_RELAY_CON1 — BUF_RELAY_CON1
[20] BUF_RELAY_CON2 — BUF_RELAY_CON2
[20] BUF_RELAY_CON3 — BUF_RELAY_CON3
[20] BUF_RELAY_CON4 — BUF_RELAY_CON4
[20] BUF_RELAY_OEn — BUF_RELAY_OEn

[22] DB[0..15] — DB[0..15]
[22] REF_SELECT — REF_SELECT
[22] FRSTDATA — FRSTDATA
[22] BUSY — BUSY
[22] #RD/SCLK — #RD/SCLK
[22] RESET — RESET
[22] CONVST_B — CONVST_B
[22] CONVST_A — CONVST_A
[22] RANGE — RANGE
[22] #STBY — #STBY
[22] #P/S_SEL — #P/S_SEL
[22] OS_0 — OS_0
[22] OS_1 — OS_1
[22] OS_2 — OS_2
[22] #CS — #CS

[21] TTL2LVTTL_OEn — TTL2LVTTL_OEn

U5C

VDD3V3 — R93 4.7K — FPGA_DONE
CFG_SPI_CCLK
FPGA_M0
CFG_SPI_MISO
CFG_SPI_MOSI
TTL2LVTTL_OEn
LVTTL_O3
FPGA_M1
LVTTL_O2
LVTTL_O1
LVTTL_O4
LVTTL_O7
LVTTL_I4
LVTTL_I6
LVTTL_O6
LVTTL_I5
LVTTL_O5
LVTTL_O8
LVTTL_I1
LVTTL_I2
LVTTL_I8
LVTTL_I7
OS_0
OS_1

Y20	CMPCS_B_2	IO_L40P_2	R11
Y22	DONE_2	IO_L40N_2	T11
Y21	IO_L1P_CCLK_2	IO_L41P_2	AA10 OS_2
AA22	IO_L1N_M0_CMPMISO_2	IO_L41N_VREF_2	AB10 CONVST_A
AA21	IO_L2P_CMPCLK_2	IO_L42P_2	V11
AB21	IO_L2N_CMPMOSI_2	IO_L42N_2	W11 #P/S_SEL
AA20	IO_L3P_D0_DIN_MISO_MISO1_2	IO_L43P_2	Y9 #RD/SCLK
AB20	IO_L3N_MOSI_CSI_B_MISO0_2	IO_L43N_2	AB9 RESET
T18	IO_L4P_2	IO_L44P_2	W10 RANGE
T17	IO_L4N_VREF_2	IO_L44N_2	Y10 CONVST_B
Y19	IO_L5P_2	IO_L45P_2	AA8 BUSY
AB19	IO_L5N_2	IO_L45N_2	AB8 #CS
W18	IO_L6P_2	IO_L46P_2	W8 DB4
Y18	IO_L6N_2	IO_L46N_2	V7 DB7
T16	IO_L7P_2	IO_L47P_2	W9 #STBY
T15	IO_L7N_2	IO_L47N_2	Y8 DB2
U17	IO_L8P_2	IO_L48P_D7_2	Y7 DB0
U16	IO_L8N_2	IO_L48N_RDWR_B_VREF_2	AB7 FRSTDATA
V19	IO_L9P_2	IO_L49P_D3_2	AA6 DB3
V18	IO_L9N_2	IO_L49N_D4_2	AB6 DB1
R16	IO_L10P_2	IO_L50P_2	U9
R15	IO_L10N_2	IO_L50N_2	V9 DB6
V17	IO_L11P_2	IO_L57P_2	AA4 DB8
W17	IO_L11N_2	IO_L57N_2	AB4 DB5
U14	IO_L12P_D1_MISO2_2	IO_L58P_2	Y3 DB10
U13	IO_L12N_D2_MISO3_2	IO_L58N_2	AB3 DB9
U15	IO_L13P_M1_2	IO_L59P_2	R9
V15	IO_L13N_D10_2	IO_L59N_2	R8
AA18	IO_L14P_D11_2	IO_L60P_2	T7
AB18	IO_L14N_D12_2	IO_L60N_2	R7
Y17	IO_L15P_2	IO_L62P_D5_2	W4 DB14
AB17	IO_L15N_2	IO_L62N_D6_2	Y4 DB12
AA14	IO_L16P_2	IO_L63P_2	U6 DB15
AB14	IO_L16N_VREF_2	IO_L63N_2	V5 REF_SELECT
V13	IO_L18P_2	IO_L64P_D8_2	AA2 DB13
W13	IO_L18N_2	IO_L64N_D9_2	AB2 DB11
AA16	IO_L19P_2	IO_L65P_INIT_B_2	T6 FPGA_INIT
AB16	IO_L19N_2	IO_L65N_CSO_B_2	T5 CFG_SPI_CS
W14	IO_L20P_2	PROGRAM_B_2	AA1 R94 4.7K — VDD3V3
Y14	IO_L20N_2	N.C.	U12
Y15	IO_L21P_2	N.C.	T12
AB15	IO_L21N_2	N.C.	Y16
T14	IO_L23P_2	N.C.	W15
R13	IO_L23N_2	N.C.	T8
W12	IO_L29P_GCLK3_2	N.C.	U8
Y12	IO_L29N_GCLK2_2	N.C.	T10
Y13	IO_L30P_GCLK1_D13_2	N.C.	U10
AB13	IO_L30N_GCLK0_USERCCLK_2	N.C.	AB5
AA12	IO_L31P_GCLK31_D14_2	N.C.	Y5
AB12	IO_L31N_GCLK30_D15_2	N.C.	Y6
Y11	IO_L32P_GCLK29_2	N.C.	W6
AB11	IO_L32N_GCLK28_2	N.C.	

XC6SLX100-2FGG484I

U5D

BUF_RELAY_OEn
BUF_RELAY_CON4
BUF_RELAY_CON3
BUF_RELAY_CON2
BUF_RELAY_CON1
RS485_TX2
UART_TX3
RS485_RD3
RS485_RD1
RS485_TX1
UART_RX3
RS485_RD4
RS485_RX4
RS485_TX4
RS485_RX2
RS485_RD2
RS485_RX3
RS485_RX1
RS485_TX3
UART_RX4
UART_RX1

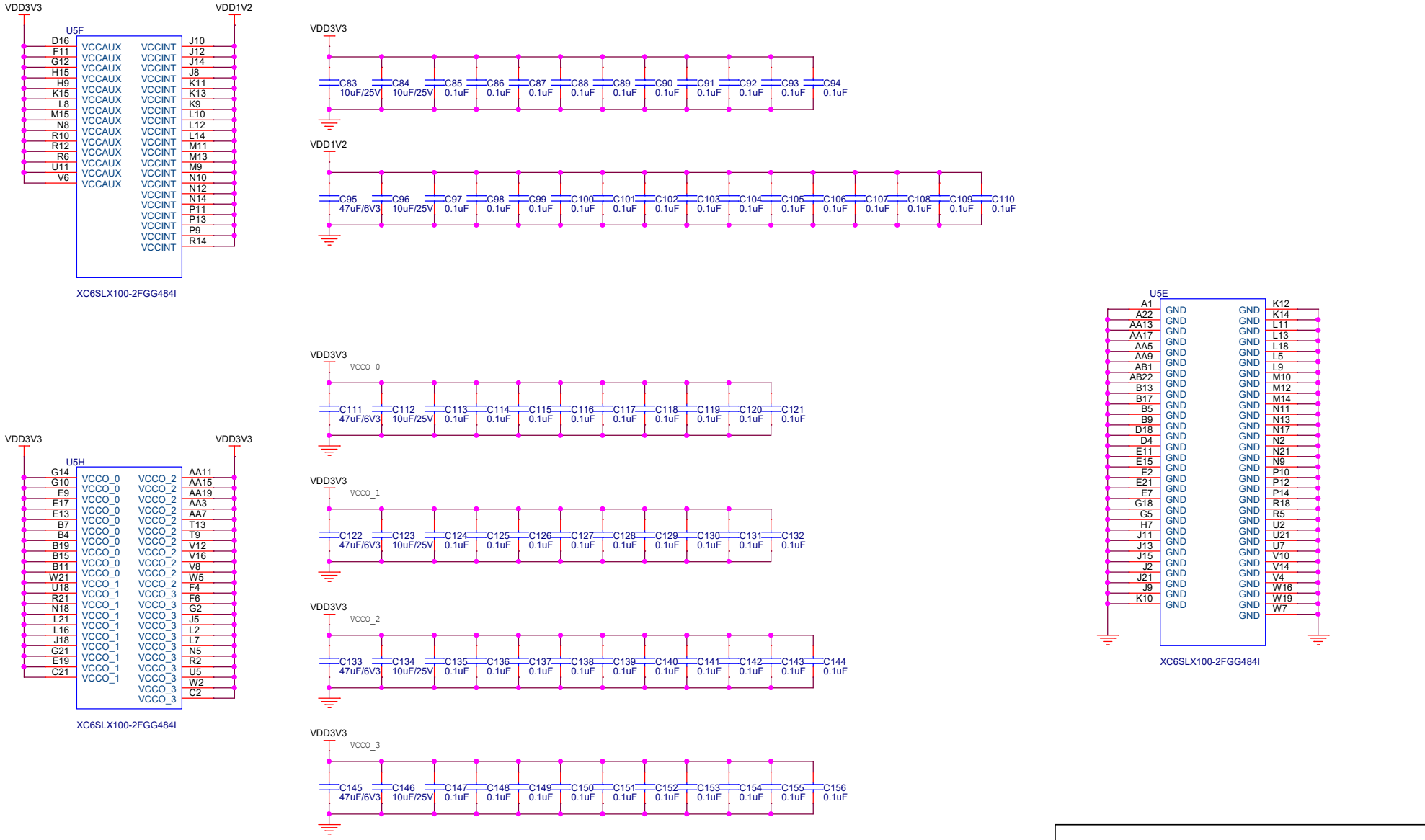
Y2	IO_L1P_3	IO_L42P_GCLK25_TRDY2_M3UDM_3	M3
Y1	IO_L1N_VREF_3	IO_L42N_GCLK24_M3LDM_3	L4
W3	IO_L2P_3	IO_L43P_GCLK23_M3RASN_3	K5
W1	IO_L2N_3	IO_L43N_GCLK22_IRDY2_M3CASN_3	K4 UART_TX1
P8	IO_L7P_3	IO_L44P_GCLK21_M3A5_3	K3 UART_TX2
P7	IO_L7N_3	IO_L44N_GCLK20_M3A6_3	J4 UART_RX2
P6	IO_L8P_3	IO_L45P_M3A3_3	K6 UART_TX4
P5	IO_L8N_3	IO_L45N_M3ODT_3	J6
T4	IO_L9P_3	IO_L46P_M3CLK_3	H4
T3	IO_L9N_3	IO_L46N_M3CLKN_3	H3
U4	IO_L10P_3	IO_L47P_M3A0_3	H2
V3	IO_L10N_3	IO_L47N_M3A1_3	H1
N6	IO_L11P_3	IO_L48P_M3BA0_3	G3
N7	IO_L11N_3	IO_L48N_M3BA1_3	G1
M7	IO_L23P_3	IO_L49P_M3A7_3	H6
M8	IO_L23N_3	IO_L49N_M3A2_3	H5
R4	IO_L24P_3	IO_L50P_M3WE_3	F2
P4	IO_L24N_3	IO_L50N_M3BA2_3	F1
M6	IO_L25P_3	IO_L51P_M3A10_3	G4
L6	IO_L25N_3	IO_L51N_M3A4_3	F3
P3	IO_L26P_3	IO_L52P_M3A8_3	E3
N4	IO_L26N_3	IO_L52N_M3A9_3	E1
M5	IO_L31P_3	IO_L53P_M3CKE_3	D2
M4	IO_L31N_VREF_3	IO_L53N_M3A12_3	D1
V2	IO_L32P_M3DQ14_3	IO_L54P_M3RESET_3	C3
V1	IO_L32N_M3DQ15_3	IO_L54N_M3A11_3	C1
U3	IO_L33P_M3DQ12_3	IO_L55P_M3A13_3	G6
U1	IO_L33N_M3DQ13_3	IO_L55N_M3A14_3	F5
T2	IO_L34P_M3UDQS_3	IO_L57P_3	K7
T1	IO_L34N_M3UDQSN_3	IO_L57N_VREF_3	K8
R3	IO_L35P_M3DQ10_3	IO_L58P_3	D5
R1	IO_L35N_M3DQ11_3	IO_L58N_3	E4
P2	IO_L36P_M3DQ8_3	IO_L59P_3	J7
P1	IO_L36N_M3DQ9_3	IO_L59N_3	H8
N3	IO_L37P_M3DQ0_3	IO_L60P_3	B2
N1	IO_L37N_M3DQ1_3	IO_L60N_3	B1
M2	IO_L38P_M3DQ2_3	IO_L80P_3	G7
M1	IO_L38N_M3DQ3_3	IO_L80N_3	F7
L3	IO_L39P_M3LDQS_3	IO_L81P_3	D3
L1	IO_L39N_M3LDQSN_3	IO_L81N_3	C4
K2	IO_L40P_M3DQ6_3	IO_L82P_3	E5
K1	IO_L40N_M3DQ7_3	IO_L82N_3	E6
J3	IO_L41P_GCLK27_M3DQ4_3	IO_L83P_3	A2
J1	IO_L41N_GCLK26_M3DQ5_3	IO_L83N_VREF_3	B3

XC6SLX100-2FGG484I

VDD3V3 — R96 330R — FPGA_DONE — Q1 2N7002 — D4 LED Green — R95 330R — VDD3V3 — GND

VDD3V3 — R98 330R — FPGA_INIT — Q2 2N7002 — D5 LED Green — R97 330R — VDD3V3 — GND

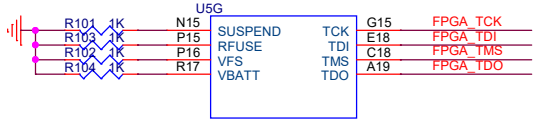
Title	<Title>		
Size B	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 11 of 30		


VDD3V3
VDD1V2
U5F
D16 F11 G12 H15 H9 K15 L8 M15 N8 R10 R12 R6 U11 V6
VCCAUX
J10 J12 J14 J8 K11 K13 K9 L10 L12 L14 M11 M13 M9 N10 N12 N14 P11 P13 P9 R14
VCCINT
XC6SLX100-2FGG484I
C83 10uF/25V C84 10uF/25V C85 0.1uF C86 0.1uF C87 0.1uF C88 0.1uF C89 0.1uF C90 0.1uF C91 0.1uF C92 0.1uF C93 0.1uF C94 0.1uF
C95 47uF/6V3 C96 10uF/25V C97 0.1uF C98 0.1uF C99 0.1uF C100 0.1uF C101 0.1uF C102 0.1uF C103 0.1uF C104 0.1uF C105 0.1uF C106 0.1uF C107 0.1uF C108 0.1uF C109 0.1uF C110 0.1uF
VDD3V3
VDD3V3
U5H
G14 G10 E9 E17 E13 B7 B4 B19 B15 B11 W21 U18 R21 N18 L21 L16 J18 G21 E19 C21
VCCO_0
VCCO_1
VCCO_2
AA11 AA15 AA19 AA3 AA7 T13 T9 V12 V16 V8 W5 F4 F6 G2 J5 L2 L7 N5 R2 U5 W2 C2
VCCO_3
XC6SLX100-2FGG484I
VDD3V3
VCCO_0
C111 47uF/6V3 C112 10uF/25V C113 0.1uF C114 0.1uF C115 0.1uF C116 0.1uF C117 0.1uF C118 0.1uF C119 0.1uF C120 0.1uF C121 0.1uF
VDD3V3
VCCO_1
C122 47uF/6V3 C123 10uF/25V C124 0.1uF C125 0.1uF C126 0.1uF C127 0.1uF C128 0.1uF C129 0.1uF C130 0.1uF C131 0.1uF C132 0.1uF
VDD3V3
VCCO_2
C133 47uF/6V3 C134 10uF/25V C135 0.1uF C136 0.1uF C137 0.1uF C138 0.1uF C139 0.1uF C140 0.1uF C141 0.1uF C142 0.1uF C143 0.1uF C144 0.1uF
VDD3V3
VCCO_3
C145 47uF/6V3 C146 10uF/25V C147 0.1uF C148 0.1uF C149 0.1uF C150 0.1uF C151 0.1uF C152 0.1uF C153 0.1uF C154 0.1uF C155 0.1uF C156 0.1uF
U5E
A1 A22 AA13 AA17 AA5 AA9 AB1 AB22 B13 B17 B5 B9 D18 D4 E11 E15 E2 E21 E7 G18 G5 H7 J11 J13 J15 J2 J21 J9 K10
GND
K12 K14 L11 L13 L18 L5 L9 M10 M12 M14 N11 N13 N17 N2 N21 N9 P10 P12 P14 R18 R5 U2 U21 U7 V10 V14 V4 W16 W19 W7
XC6SLX100-2FGG484I
Title
<Title>
Size B
Document Number
<Doc>
Rev
<RevCode>
Date: Tuesday, March 26, 2019
Sheet 12 of 30

[11] FPGA_M0
[11] FPGA_M1
FPGA_M0
FPGA_M1

[11] CFG_SPI_CS
[11] CFG_SPI_MISO
[11] CFG_SPI_CCLK
[11] CFG_SPI_MOSI
CFG_SPI_CS
CFG_SPI_MISO
CFG_SPI_CCLK
CFG_SPI_MOSI

When not programming or when not using the key EFUSE,
connecting RFUSE,VFS,VBATT to VCCAUX or GND is recommended.



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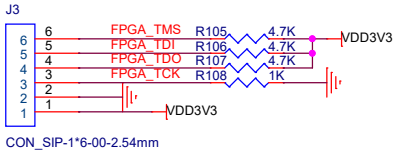
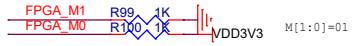
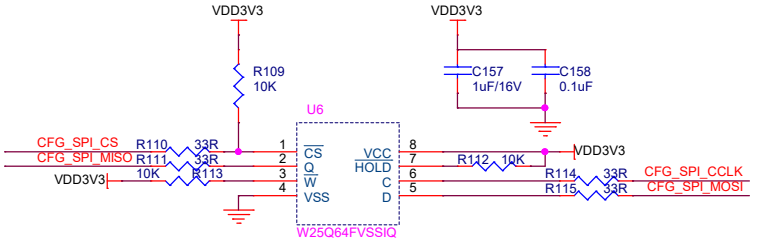


CON_SIP-1*6-00-2.54mm



Configuration Mode	M[1:0]	Bus Width	CCLK Direction
Master Serial/SPI	01	1, 2, 4(1)	Output
Master SelectMAP/BPI(2)	00	8, 16	Output
JTAG(3)	xx	1	Input (TCK)
Slave SelectMAP(2)	10	8, 16	Input
Slave Serial(4)	11	1	Input

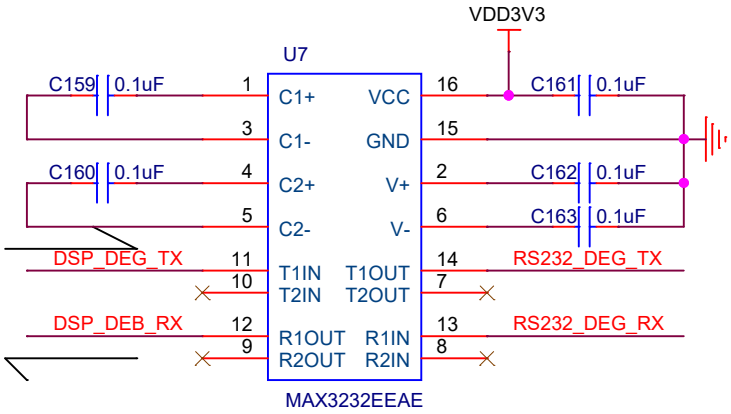


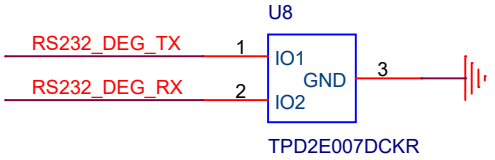
W25Q64FVSSIQ

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 13 of 30	

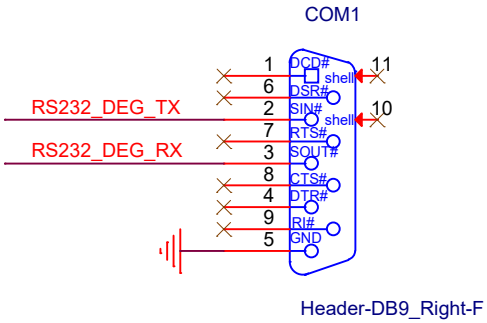
[5] DSP_DEG_TX
[5] DSP_DEB_RX

DSP_DEG_TX
DSP_DEB_RX





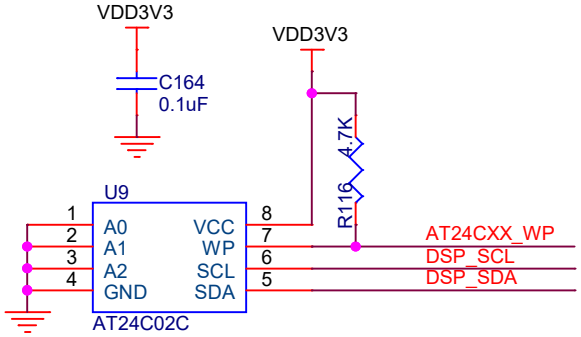
UART TR要交差 已改



Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 14 of 30	

[5,23] DSP_SDA
[5,23] DSP_SCL
[5] AT24CXX_WP

DSP_SDA
DSP_SCL
AT24CXX_WP



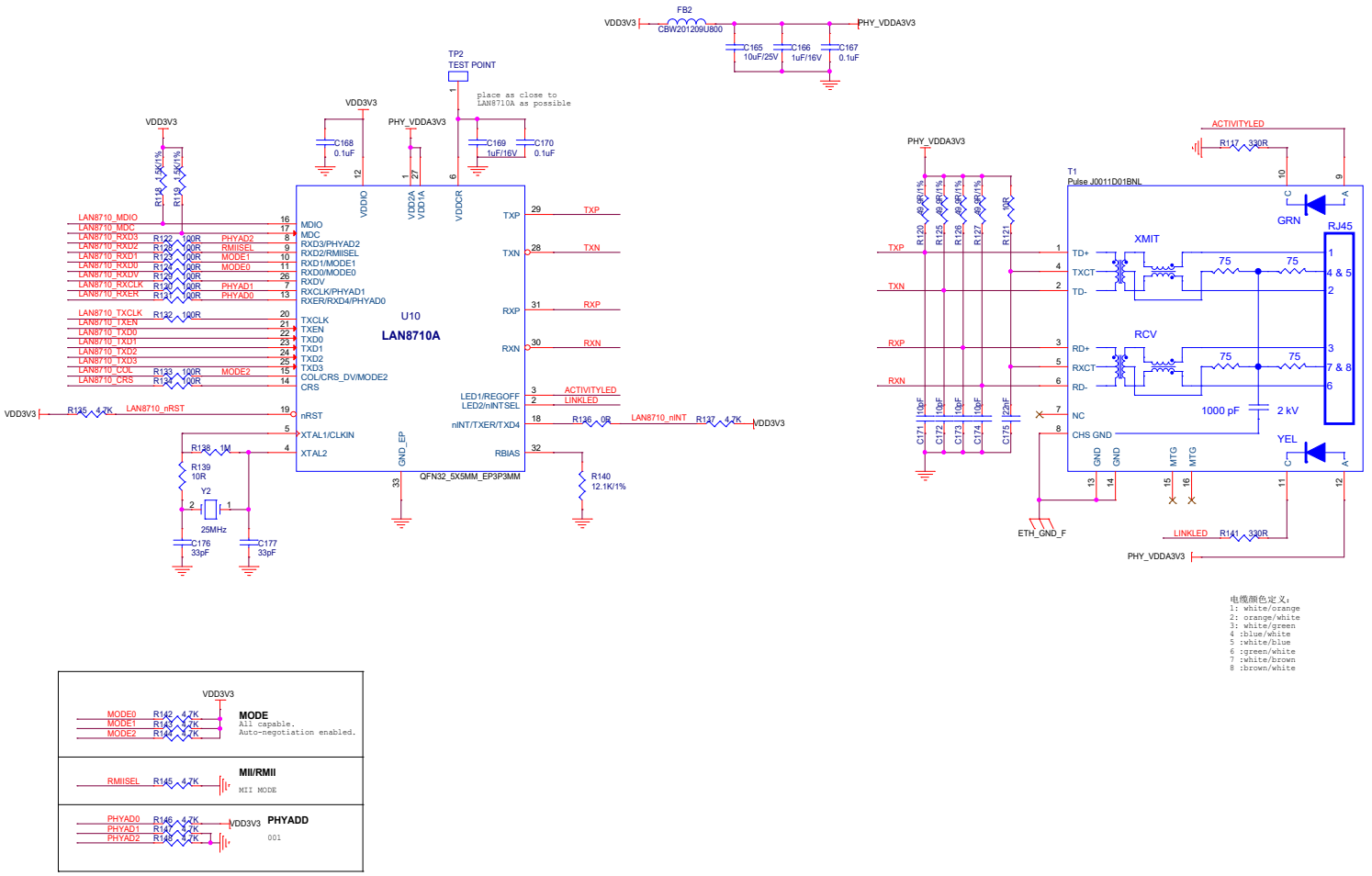
Title	AT24C08	
Size: A	Document Number: <Doc>	Rev: 1.0
Date: Tuesday, March 26, 2019	Sheet 15 of 30	

[5] LAN8710_MDIO
[5] LAN8710_MDC

[5] LAN8710_RXD3
[5] LAN8710_RXD2
[5] LAN8710_RXD1
[5] LAN8710_RXD0
[5] LAN8710_RXDV
[5] LAN8710_RXCLK
[5] LAN8710_RXER

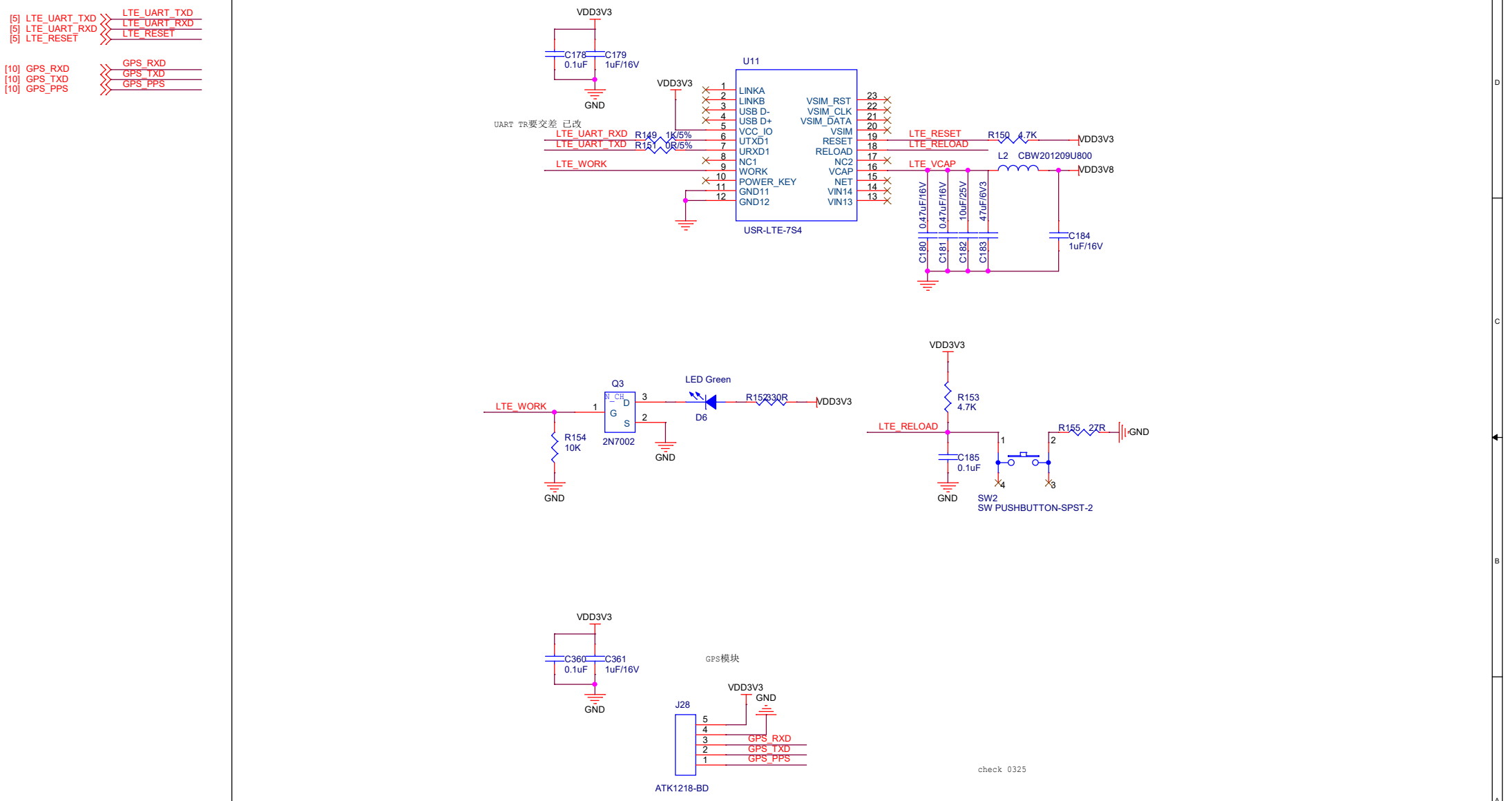
[5] LAN8710_TXCLK
[5] LAN8710_TXEN
[5] LAN8710_TXD0
[5] LAN8710_TXD1
[5] LAN8710_TXD2
[5] LAN8710_TXD3
[5] LAN8710_COL
[5] LAN8710_CRS

[10] LAN8710_nRST
[5] LAN8710_nINT



电缆颜色定义：
1: white/orange
2: orange/white
3: white/green
4 :blue/white
5 :white/blue
6 :green/white
7 :white/brown
8 :brown/white

Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 16 of 30		



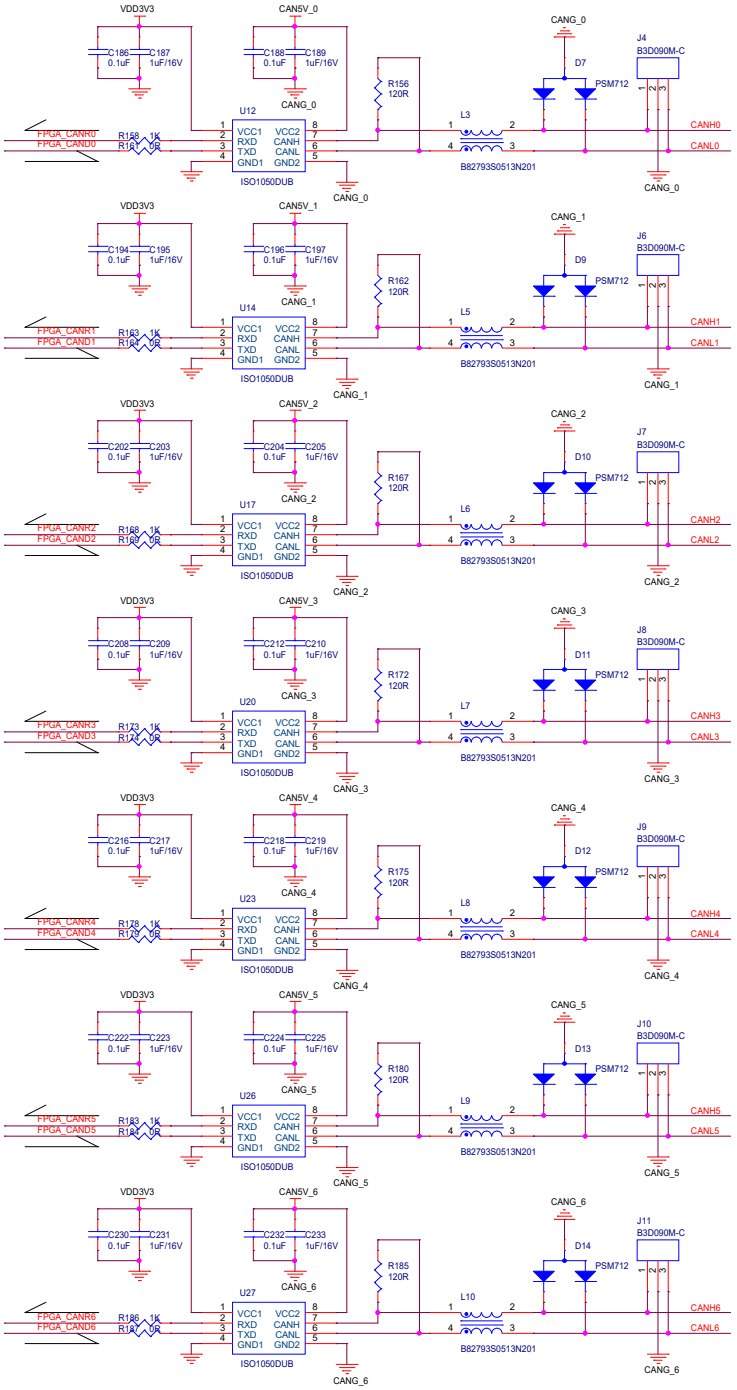
Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 17 of 30	

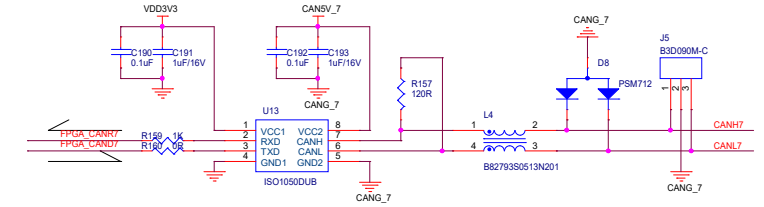
[10] FPGA_CANR[7:0] → FPGA_CANR[7:0]

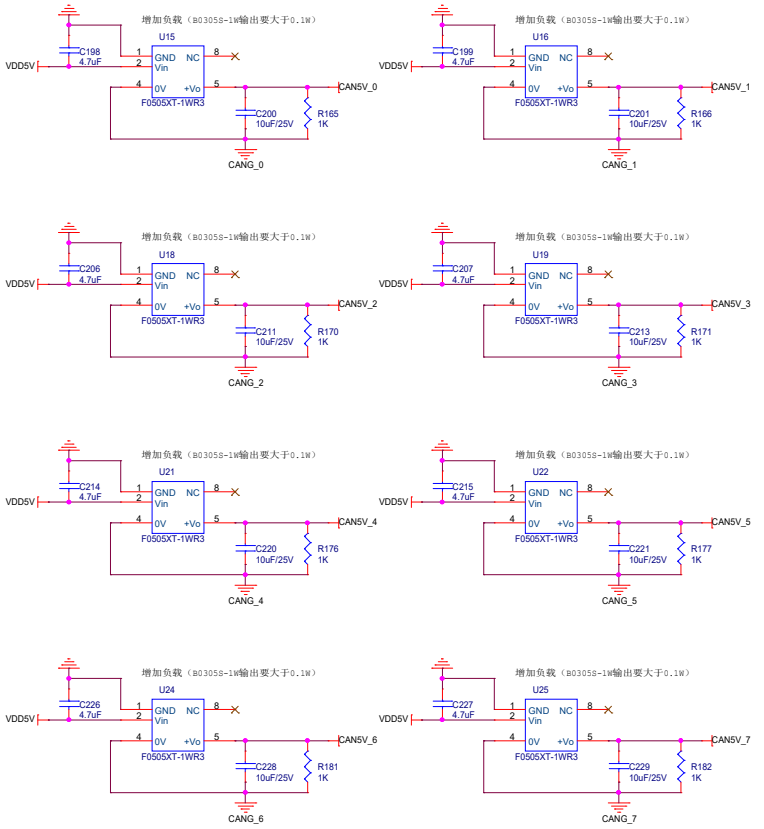
[10] FPGA_CAND[7:0] → FPGA_CAND[7:0]

[30] CANH[7:0] → CANH[7:0]

[30] CANL[7:0] → CANL[7:0]







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Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 18 of 30		

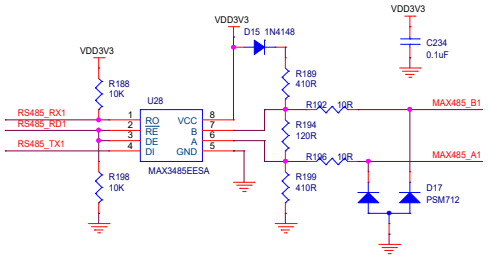
[11] RS485_RX1
[11] RS485_RX2
[11] RS485_RX3
[11] RS485_RX4
RS485_RX1
RS485_RX2
RS485_RX3
RS485_RX4

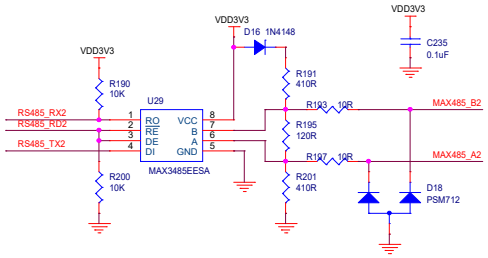
[11] RS485_TX1
[11] RS485_TX2
[11] RS485_TX3
[11] RS485_TX4
RS485_TX1
RS485_TX2
RS485_TX3
RS485_TX4

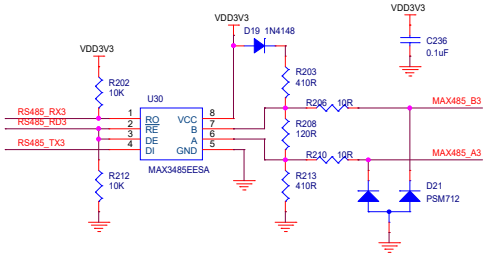
[11] RS485_RD1
[11] RS485_RD2
[11] RS485_RD3
[11] RS485_RD4
RS485_RD1
RS485_RD2
RS485_RD3
RS485_RD4

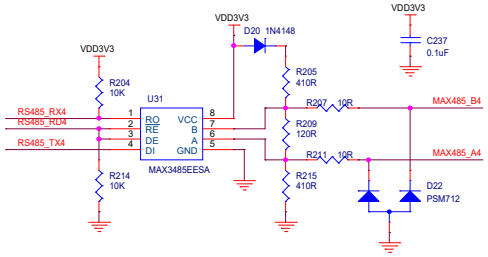
[30] MAX485_A1
[30] MAX485_A2
[30] MAX485_A3
[30] MAX485_A4
MAX485_A1
MAX485_A2
MAX485_A3
MAX485_A4

[30] MAX485_B1
[30] MAX485_B2
[30] MAX485_B3
[30] MAX485_B4
MAX485_B1
MAX485_B2
MAX485_B3
MAX485_B4







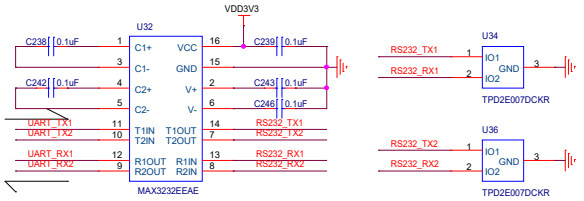


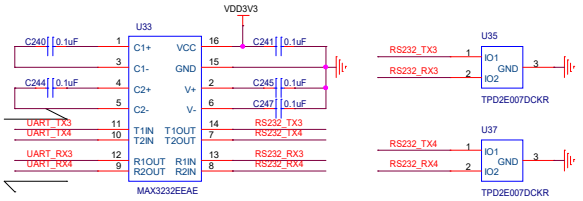
[11] UART_TX1
[11] UART_TX2
[11] UART_TX3
[11] UART_TX4
UART_TX1
UART_TX2
UART_TX3
UART_TX4

[11] UART_RX1
[11] UART_RX2
[11] UART_RX3
[11] UART_RX4
UART_RX1
UART_RX2
UART_RX3
UART_RX4

[30] RS232_TX1
[30] RS232_TX2
[30] RS232_TX3
[30] RS232_TX4
RS232_TX1
RS232_TX2
RS232_TX3
RS232_TX4

[30] RS232_RX1
[30] RS232_RX2
[30] RS232_RX3
[30] RS232_RX4
RS232_RX1
RS232_RX2
RS232_RX3
RS232_RX4





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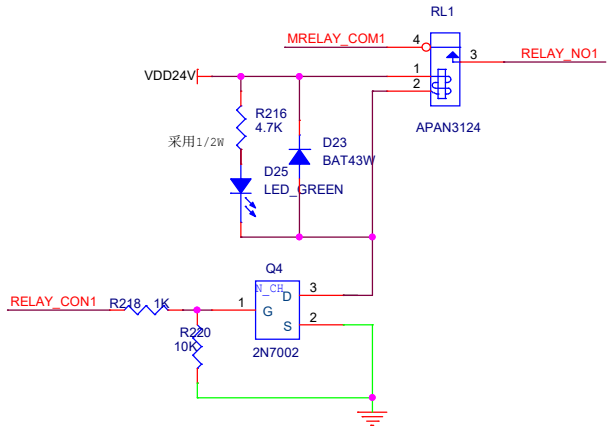
Title	UART	
Size C	Document Number <Doc>	Rev 1.0
Date: Tuesday, March 26, 2019	Sheet 19 of 30	

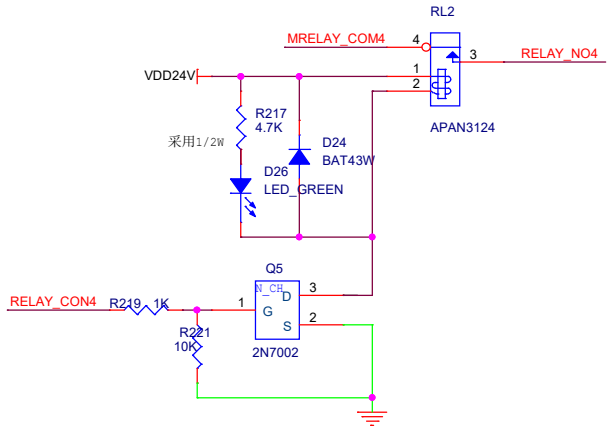
[11] BUF_RELAY_CON1 — BUF_RELAY_CON1
[11] BUF_RELAY_CON2 — BUF_RELAY_CON2
[11] BUF_RELAY_CON3 — BUF_RELAY_CON3
[11] BUF_RELAY_CON4 — BUF_RELAY_CON4

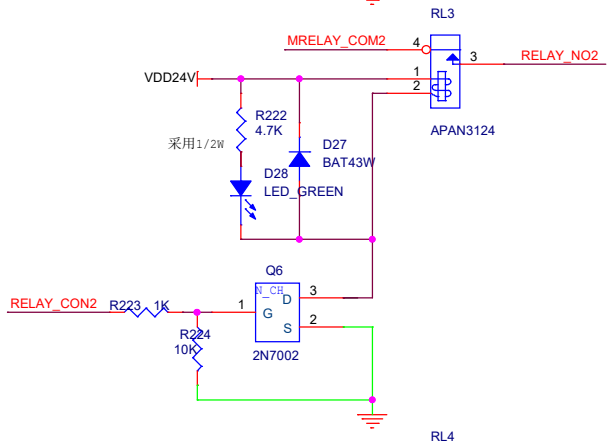
[11] BUF_RELAY_OEn — BUF_RELAY_OEn

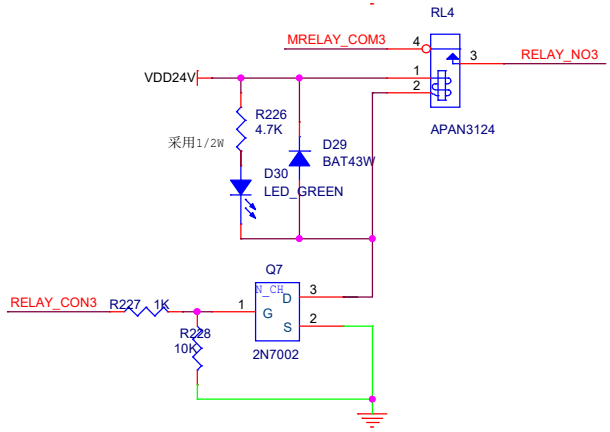
[30] MRELAY_COM1 — MRELAY_COM1
[30] MRELAY_COM2 — MRELAY_COM2
[30] MRELAY_COM3 — MRELAY_COM3
[30] MRELAY_COM4 — MRELAY_COM4

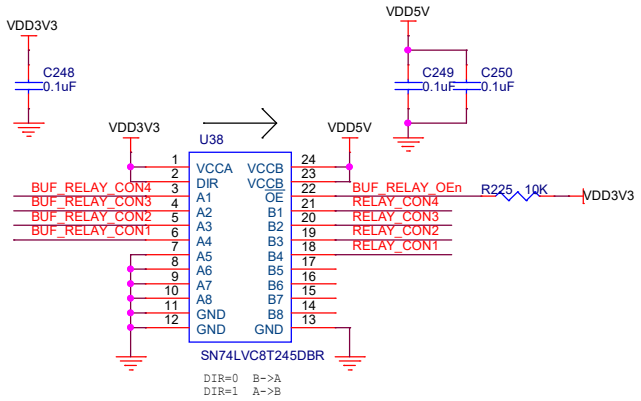
[30] RELAY_NO1 — RELAY_NO1
[30] RELAY_NO2 — RELAY_NO2
[30] RELAY_NO3 — RELAY_NO3
[30] RELAY_NO4 — RELAY_NO4











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Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 20 of 30	

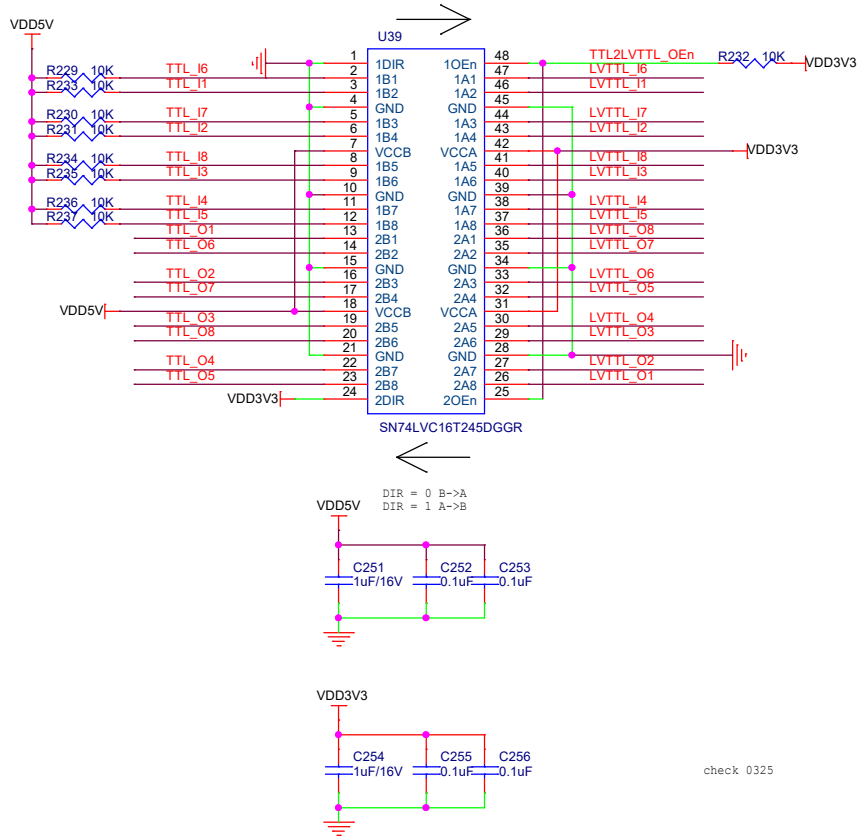
[30] TTL_I1 → TTL_I1
[30] TTL_I2 → TTL_I2
[30] TTL_I3 → TTL_I3
[30] TTL_I4 → TTL_I4
[30] TTL_I5 → TTL_I5
[30] TTL_I6 → TTL_I6
[30] TTL_I7 → TTL_I7
[30] TTL_I8 → TTL_I8

[30] TTL_O1 → TTL_O1
[30] TTL_O2 → TTL_O2
[30] TTL_O3 → TTL_O3
[30] TTL_O4 → TTL_O4
[30] TTL_O5 → TTL_O5
[30] TTL_O6 → TTL_O6
[30] TTL_O7 → TTL_O7
[30] TTL_O8 → TTL_O8

[11] LVTTL_I1 → LVTTL_I1
[11] LVTTL_I2 → LVTTL_I2
[11] LVTTL_I3 → LVTTL_I3
[11] LVTTL_I4 → LVTTL_I4
[11] LVTTL_I5 → LVTTL_I5
[11] LVTTL_I6 → LVTTL_I6
[11] LVTTL_I7 → LVTTL_I7
[11] LVTTL_I8 → LVTTL_I8

[11] LVTTL_O1 → LVTTL_O1
[11] LVTTL_O2 → LVTTL_O2
[11] LVTTL_O3 → LVTTL_O3
[11] LVTTL_O4 → LVTTL_O4
[11] LVTTL_O5 → LVTTL_O5
[11] LVTTL_O6 → LVTTL_O6
[11] LVTTL_O7 → LVTTL_O7
[11] LVTTL_O8 → LVTTL_O8

[11] TTL2LVTTL_OEn → TTL2LVTTL_OEn



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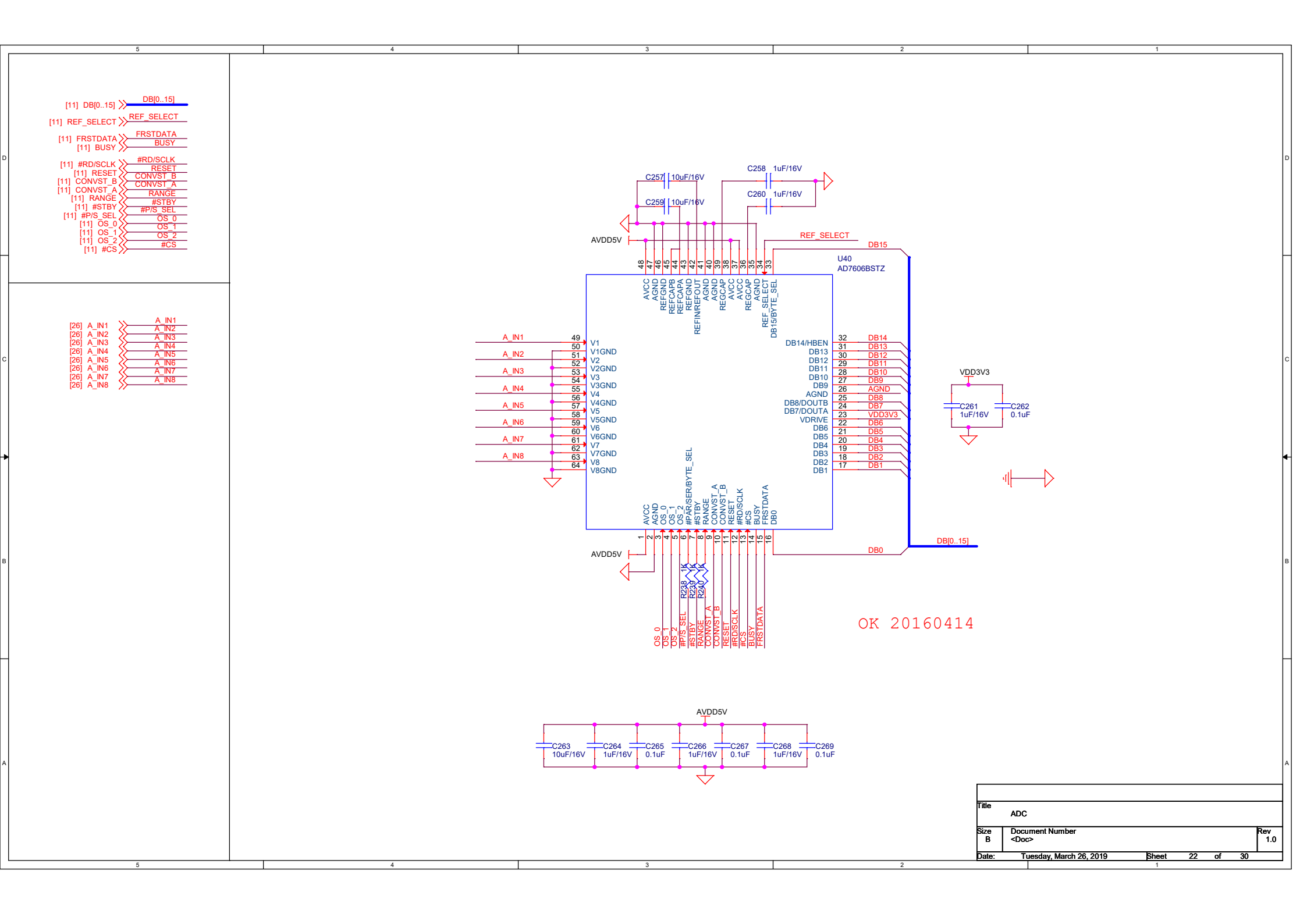
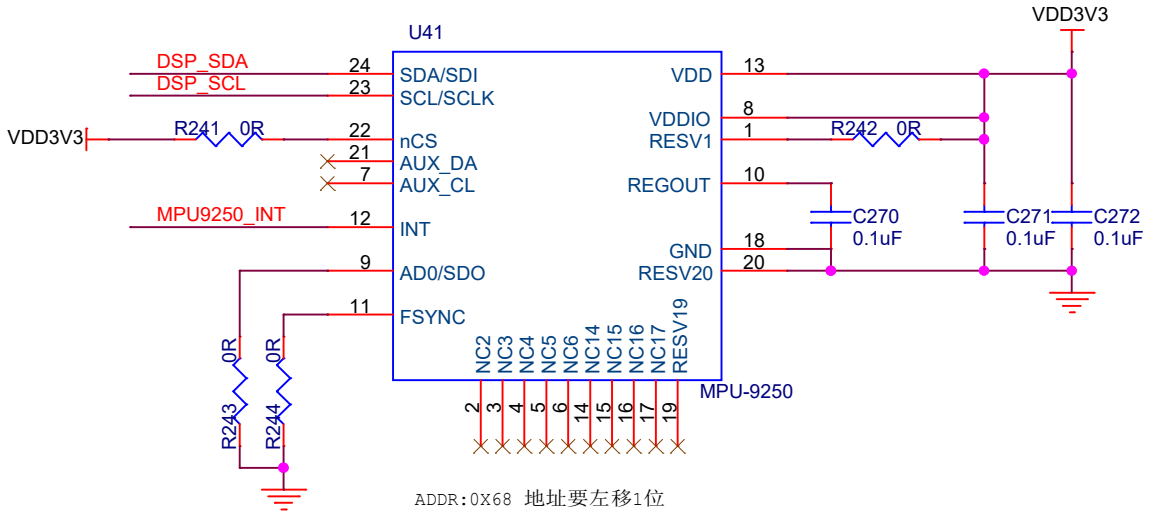
Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 21 of 30	


[11] DB[0..15]
DB[0..15]
[11] REF_SELECT
REF_SELECT
[11] FRSTDATA
FRSTDATA
[11] BUSY
BUSY
[11] #RD/SCLK
#RD/SCLK
[11] RESET
RESET
[11] CONVST_B
CONVST_B
[11] CONVST_A
CONVST_A
[11] RANGE
RANGE
[11] #STBY
#STBY
[11] #P/S_SEL
#P/S_SEL
[11] OS_0
OS_0
[11] OS_1
OS_1
[11] OS_2
OS_2
[11] #CS
#CS
[26] A_IN1
A_IN1
[26] A_IN2
A_IN2
[26] A_IN3
A_IN3
[26] A_IN4
A_IN4
[26] A_IN5
A_IN5
[26] A_IN6
A_IN6
[26] A_IN7
A_IN7
[26] A_IN8
A_IN8
C257 10uF/16V
C258 1uF/16V
C259 10uF/16V
C260 1uF/16V
AVDD5V
REF_SELECT
DB15
U40
AD7606BSTZ
AVCC
AGND
REFGND
REFCAPB
REFCAPA
REFGND
REFIN/REFOUT
AGND
AGND
REGCAP
AVCC
AVCC
REGCAP
AGND
REF_SELECT
DB15/BYTE_SEL
V1
V1GND
V2
V2GND
V3
V3GND
V4
V4GND
V5
V5GND
V6
V6GND
V7
V7GND
V8
V8GND
DB14/HBEN
DB13
DB12
DB11
DB10
DB9
AGND
DB8/DOUTB
DB7/DOUTA
VDRIVE
DB6
DB5
DB4
DB3
DB2
DB1
DB14
DB13
DB12
DB11
DB10
DB9
AGND
DB8
DB7
VDD3V3
DB6
DB5
DB4
DB3
DB2
DB1
VDD3V3
C261 1uF/16V
C262 0.1uF
AVCC
AGND
OS_0
OS_1
OS_2
#PAR/SER/BYTE_SEL
#STBY
RANGE
CONVST_A
CONVST_B
RESET
#RD/SCLK
#CS
BUSY
FRSTDATA
DB0
AVDD5V
R238 1K
R239 1K
R240 1K
DB0
DB[0..15]
OS_0
OS_1
OS_2
#P/S_SEL
#STBY
RANGE
CONVST_A
CONVST_B
RESET
#RD/SCLK
#CS
BUSY
FRSTDATA
OK 20160414
AVDD5V
C263 10uF/16V
C264 1uF/16V
C265 0.1uF
C266 1uF/16V
C267 0.1uF
C268 1uF/16V
C269 0.1uF
Title
ADC
Size B
Document Number
<Doc>
Rev 1.0
Date: Tuesday, March 26, 2019
Sheet 22 of 30

[5,15] DSP_SDA
[5,15] DSP_SCL
DSP_SDA
DSP_SCL

[5] MPU9250_INT
MPU9250_INT



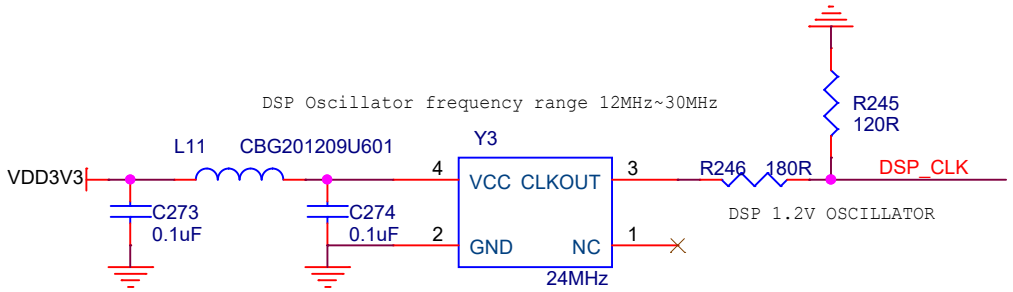
ADDR:0X68 地址要左移1位

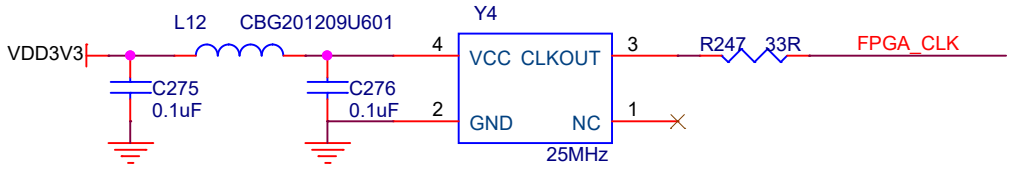
Title	陀螺，加速度	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 23 of 30	

[3] DSP_RESETn >> DSP_RESETn

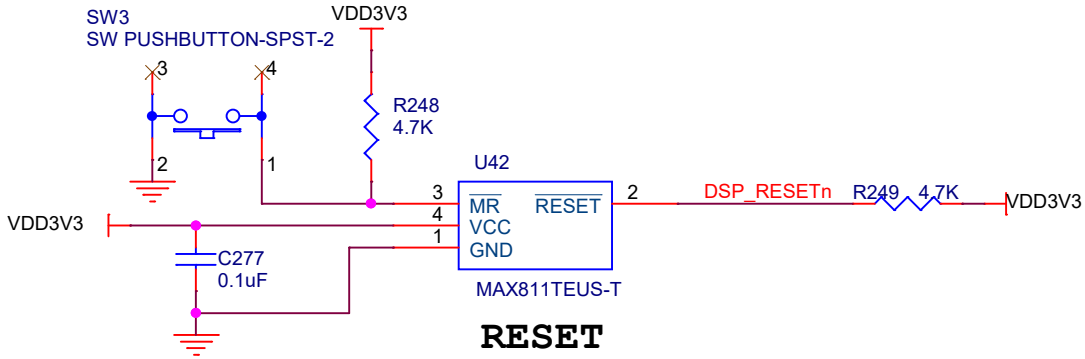
[3] DSP_CLK >> DSP_CLK

[10] FPGA_CLK >> FPGA_CLK





使用两个时钟方便更改为不同的频率



2018-10-24 CHECK OK

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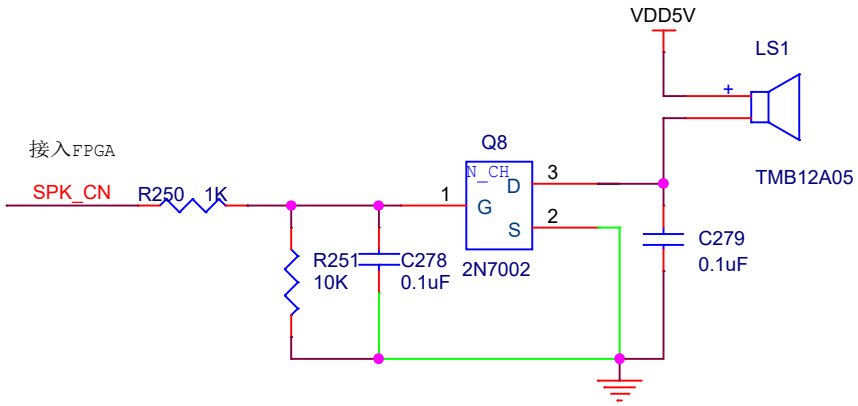
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 24 of 30	

[10] SPK_CN SPK_CN



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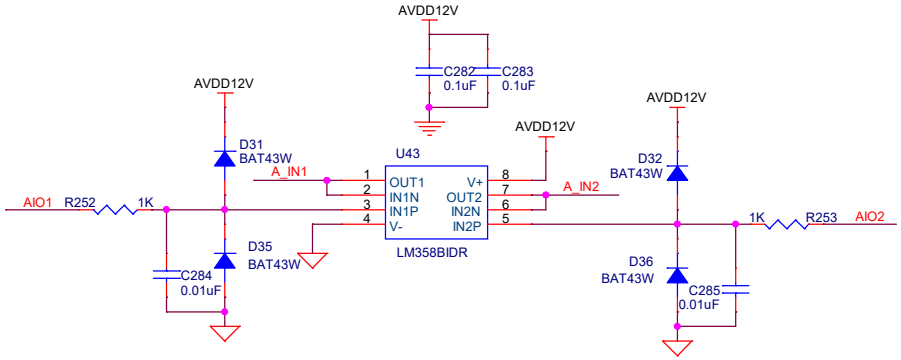
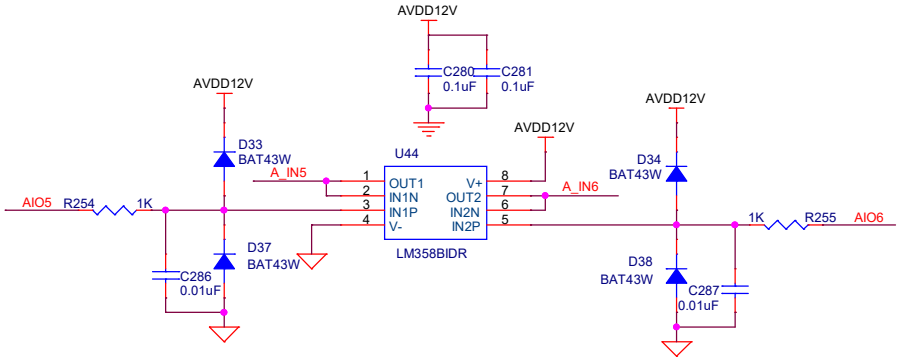
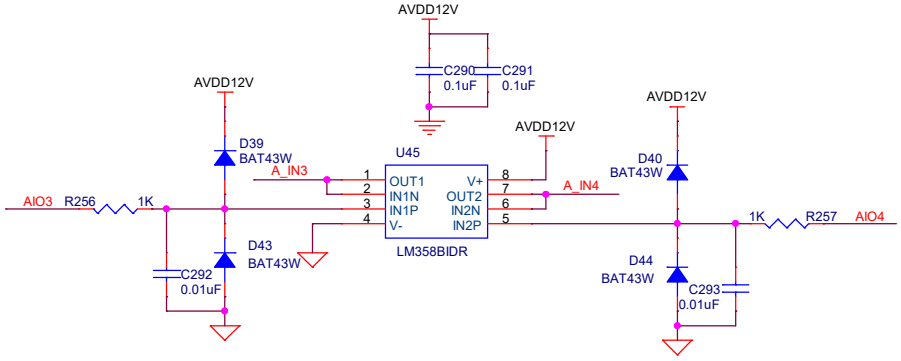
Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 25 of 30	

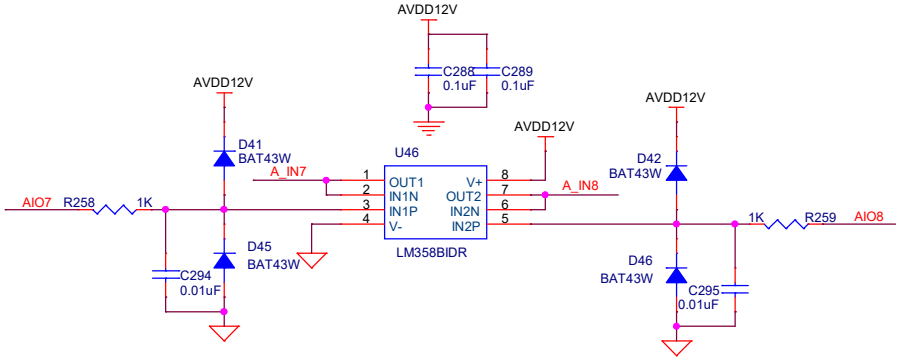
[30] AIO1 — AIO1
[30] AIO2 — AIO2
[30] AIO3 — AIO3
[30] AIO4 — AIO4
[30] AIO5 — AIO5
[30] AIO6 — AIO6
[30] AIO7 — AIO7
[30] AIO8 — AIO8

[22] A_IN1 — A_IN1
[22] A_IN2 — A_IN2
[22] A_IN3 — A_IN3
[22] A_IN4 — A_IN4
[22] A_IN5 — A_IN5
[22] A_IN6 — A_IN6
[22] A_IN7 — A_IN7
[22] A_IN8 — A_IN8









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Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 26 of 30	

[30] IO1 — IO1
[30] IO2 — IO2
[30] IO3 — IO3
[30] IO4 — IO4
[30] IO5 — IO5
[30] IO6 — IO6
[30] IO7 — IO7
[30] IO8 — IO8

[10] IO_LVTTL1 — IO_LVTTL1
[10] IO_LVTTL2 — IO_LVTTL2
[10] IO_LVTTL3 — IO_LVTTL3
[10] IO_LVTTL4 — IO_LVTTL4
[10] IO_LVTTL5 — IO_LVTTL5
[10] IO_LVTTL6 — IO_LVTTL6
[10] IO_LVTTL7 — IO_LVTTL7
[10] IO_LVTTL8 — IO_LVTTL8

[10] IO_LVTTLEN — IO_LVTTLEN

VDD24V — R260 2K — IO1 — R284 4.7K — C296 0.1uF — U47 ANODE COLLECTOR CATHODE EMITTER EL357 — R261 4.7K — VDD5V — IO_TTL1
forward current 5ma VF=1.4V

VDD24V — R262 2K — IO5 — R285 4.7K — C297 0.1uF — U48 ANODE COLLECTOR CATHODE EMITTER EL357 — R263 4.7K — VDD5V — IO_TTL5
forward current 5ma VF=1.4V

VDD24V — R266 2K — IO2 — R270 4.7K — C298 0.1uF — U49 ANODE COLLECTOR CATHODE EMITTER EL357 — R267 4.7K — VDD5V — IO_TTL2
forward current 5ma VF=1.4V

VDD24V — R268 2K — IO6 — R271 4.7K — C299 0.1uF — U50 ANODE COLLECTOR CATHODE EMITTER EL357 — R269 4.7K — VDD5V — IO_TTL6
forward current 5ma VF=1.4V

VDD24V — R272 2K — IO3 — R276 4.7K — C300 0.1uF — U51 ANODE COLLECTOR CATHODE EMITTER EL357 — R273 4.7K — VDD5V — IO_TTL3
forward current 5ma VF=1.4V

VDD24V — R274 2K — IO7 — R277 4.7K — C301 0.1uF — U52 ANODE COLLECTOR CATHODE EMITTER EL357 — R275 4.7K — VDD5V — IO_TTL7
forward current 5ma VF=1.4V

VDD24V — R278 2K — IO4 — R282 4.7K — C302 0.1uF — U53 ANODE COLLECTOR CATHODE EMITTER EL357 — R279 4.7K — VDD5V — IO_TTL4
forward current 5ma VF=1.4V

VDD24V — R280 2K — IO8 — R283 4.7K — C303 0.1uF — U54 ANODE COLLECTOR CATHODE EMITTER EL357 — R281 4.7K — VDD5V — IO_TTL8
forward current 5ma VF=1.4V

U55 SN74LVC16T245DGGR

	1	1DIR	1OEn	48	
IO_TTL5	2	1B1	1A1	47	IO_LVTTLEN
	3	1B2	1A2	46	IO_LVTTL5
	4	GND	GND	45	
IO_TTL2	5	1B3	1A3	44	
	6	1B4	1A4	43	IO_LVTTL2
VDD5V	7	VCCB	VCCA	42	VDD3V3
IO_TTL3	8	1B5	1A5	41	IO_LVTTL3
	9	1B6	1A6	40	
	10	GND	GND	39	
IO_TTL1	11	1B7	1A7	38	IO_LVTTL1
IO_TTL4	12	1B8	1A8	37	IO_LVTTL4
	13	2B1	2A1	36	
	14	2B2	2A2	35	
IO_TTL6	15	GND	GND	34	IO_LVTTL6
	16	2B3	2A3	33	
	17	2B4	2A4	32	
IO_TTL7	18	VCCB	VCCA	31	IO_LVTTL7
	19	2B5	2A5	30	
	20	2B6	2A6	29	
IO_TTL8	21	GND	GND	28	IO_LVTTL8
	22	2B7	2A7	27	
	23	2B8	2A8	26	
	24	2DIR	2OEn	25	

R284 4.7K — VDD3V3

DIR = 0 B->A
DIR = 1 A->B

VDD5V — C304 1uF/16V — C305 0.1uF — C306 0.1uF

VDD3V3 — C307 1uF/16V — C308 0.1uF — C309 0.1uF

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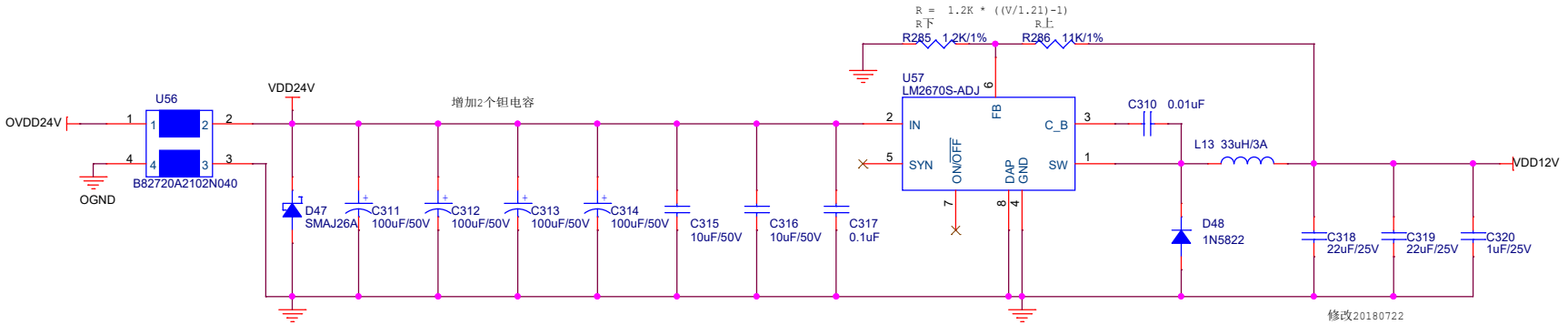
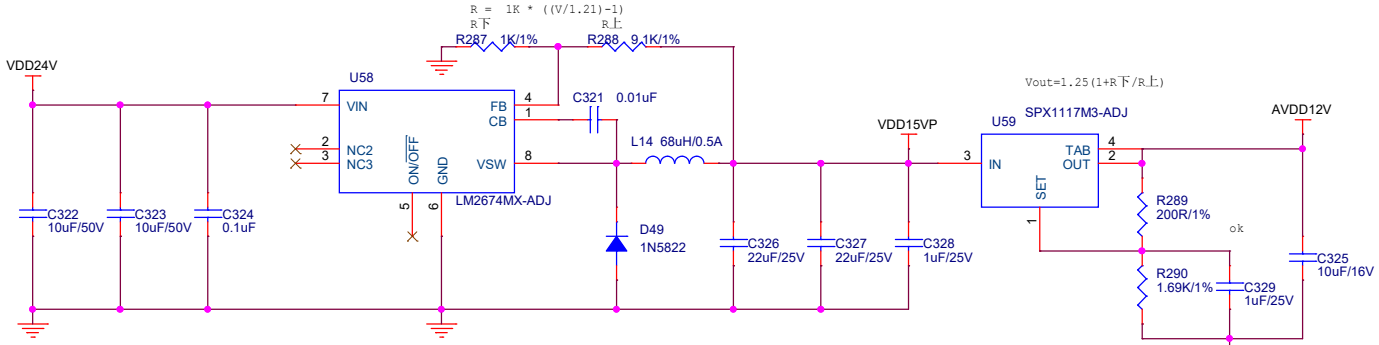
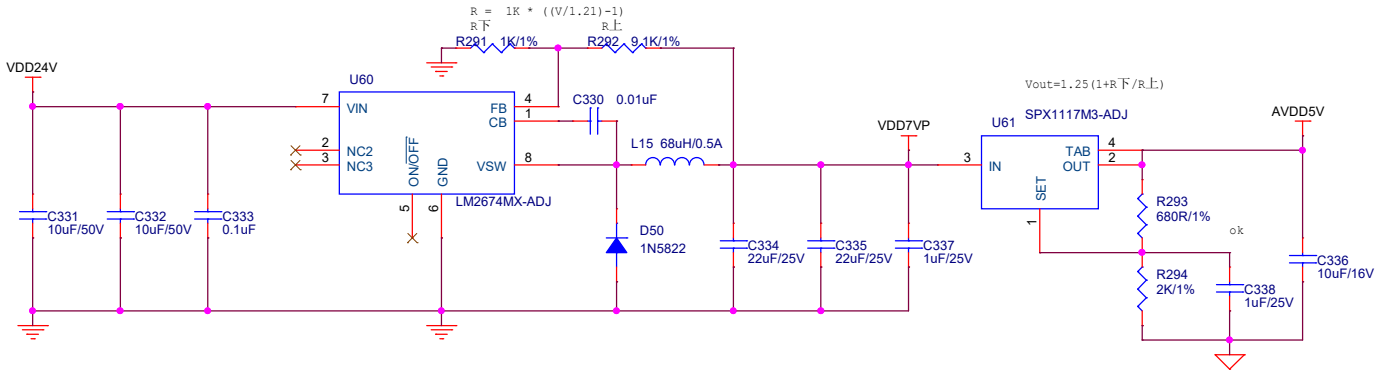
Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 27 of 30		







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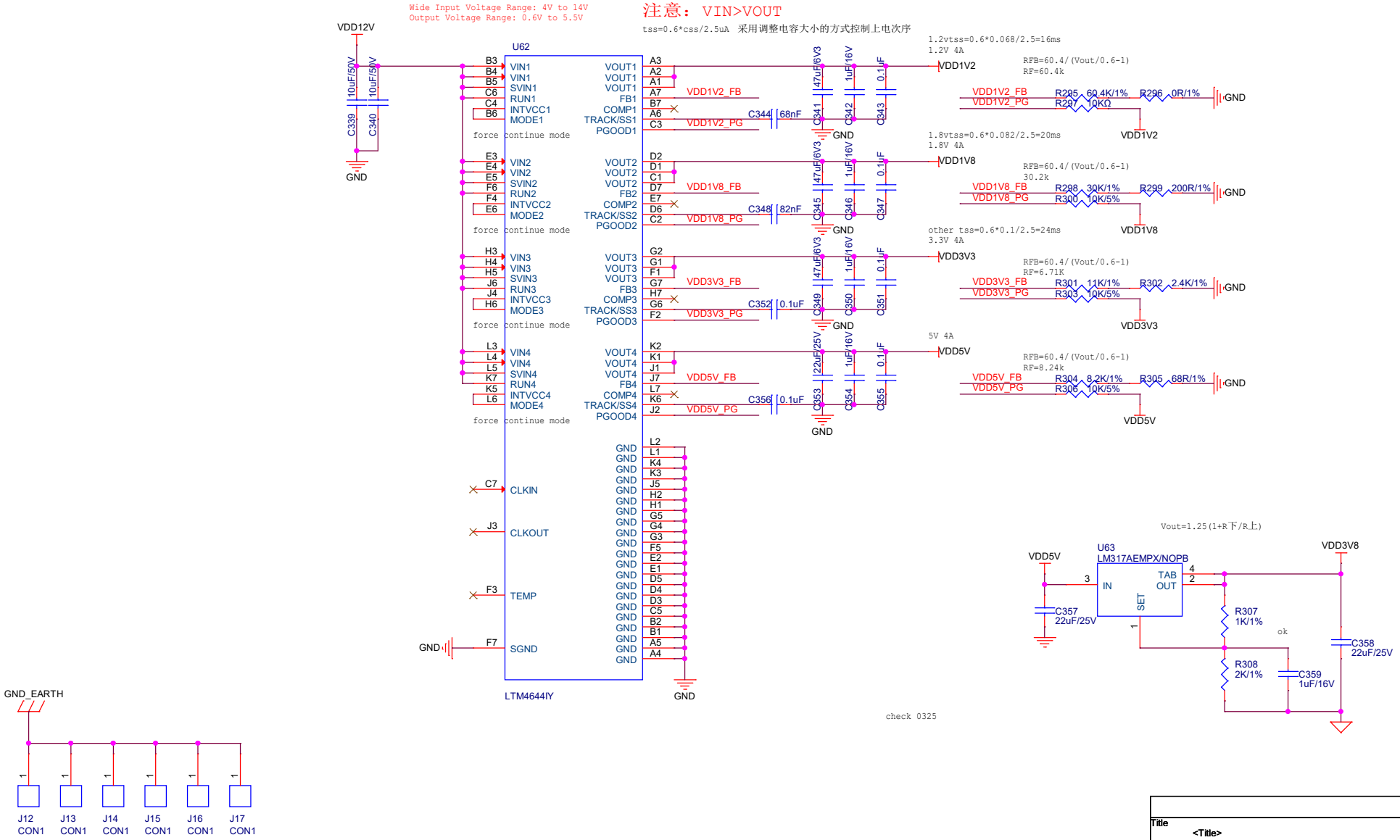
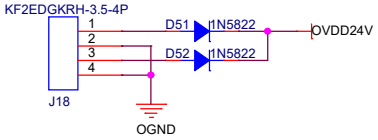
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 28 of 30	

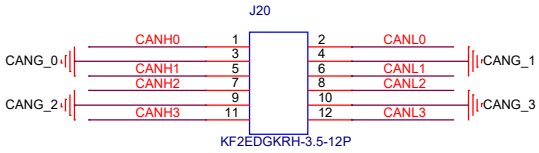


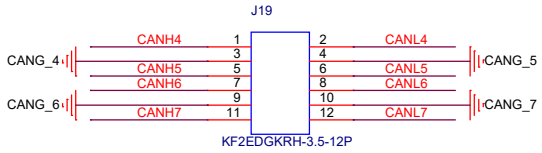
Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 29 of 30	

[18] CANH[7:0] — CANH[7:0]

[18] CANL[7:0] — CANL[7:0]

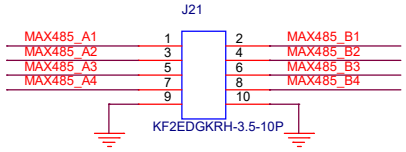


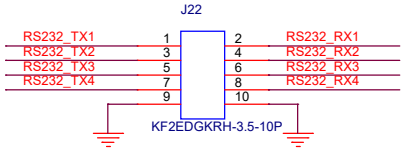




[19] MAX485_A1 — MAX485_A1
[19] MAX485_A2 — MAX485_A2
[19] MAX485_A3 — MAX485_A3
[19] MAX485_A4 — MAX485_A4

[19] MAX485_B1 — MAX485_B1
[19] MAX485_B2 — MAX485_B2
[19] MAX485_B3 — MAX485_B3
[19] MAX485_B4 — MAX485_B4





[19] RS232_TX1 — RS232_TX1
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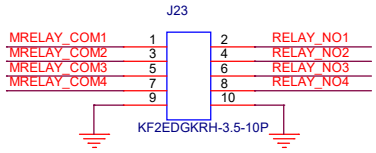
[19] RS232_TX3 — RS232_TX3
[19] RS232_TX4 — RS232_TX4

[19] RS232_RX1 — RS232_RX1
[19] RS232_RX2 — RS232_RX2
[19] RS232_RX3 — RS232_RX3
[19] RS232_RX4 — RS232_RX4

左下角为第一脚

[20] MRELAY_COM1 — MRELAY_COM1
[20] MRELAY_COM2 — MRELAY_COM2
[20] MRELAY_COM3 — MRELAY_COM3
[20] MRELAY_COM4 — MRELAY_COM4

[20] RELAY_NO1 — RELAY_NO1
[20] RELAY_NO2 — RELAY_NO2
[20] RELAY_NO3 — RELAY_NO3
[20] RELAY_NO4 — RELAY_NO4



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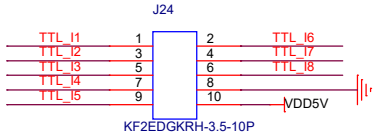
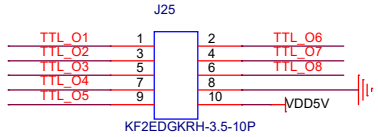
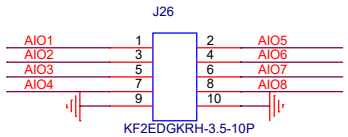
[21] TTL_I2 — TTL_I2
[21] TTL_I3 — TTL_I3
[21] TTL_I4 — TTL_I4
[21] TTL_I5 — TTL_I5
[21] TTL_I6 — TTL_I6
[21] TTL_I7 — TTL_I7
[21] TTL_I8 — TTL_I8

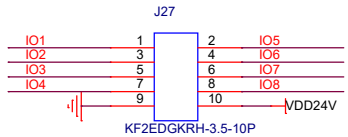
[21] TTL_O1 — TTL_O1
[21] TTL_O2 — TTL_O2
[21] TTL_O3 — TTL_O3
[21] TTL_O4 — TTL_O4
[21] TTL_O5 — TTL_O5
[21] TTL_O6 — TTL_O6
[21] TTL_O7 — TTL_O7
[21] TTL_O8 — TTL_O8





[26] AIO1 — AIO1
[26] AIO2 — AIO2
[26] AIO3 — AIO3
[26] AIO4 — AIO4
[26] AIO5 — AIO5
[26] AIO6 — AIO6
[26] AIO7 — AIO7
[26] AIO8 — AIO8





[27] IO1 — IO1
[27] IO2 — IO2
[27] IO3 — IO3
[27] IO4 — IO4
[27] IO5 — IO5
[27] IO6 — IO6
[27] IO7 — IO7
[27] IO8 — IO8

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Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, March 26, 2019	Sheet 30 of 30	