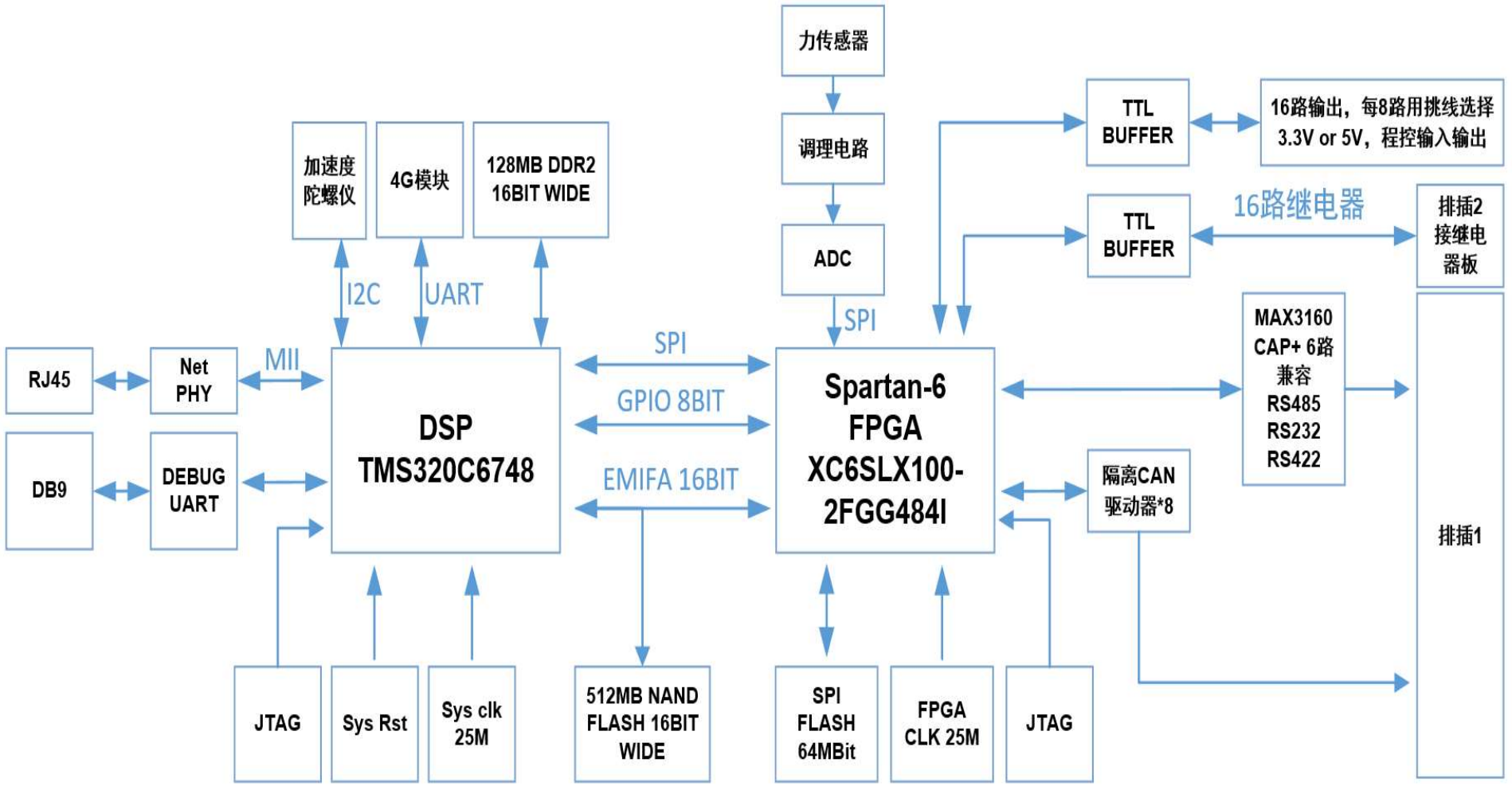
01_NOTE
02_BLOCK_DIAGRAM
03_C6748_MEMORY_IF_JTAG
04_C6748_DDR
05_C6748_PHERIPERALS
06_C6748_VP_CFG
07_C6748_PW
08_DDR2
09_NAND_FLASH
10_FPGA_BANK0_1
11_FPGA_BANK2_3
12_FPGA_PW
13_FPGA_CFG
14_DSP_UART
15_EEPROM
16_LAN8710_MII
17_LTE_MODULE
18_ISO_CAN
19_FPGA_UART
20_RELAY
21_DIGITAL_BUF
22_MEA_P
23_MPU9250
24_RST_CLK
25_POWER1
26_POWER2
27_PORT

调试记录：

2018-11-19：R294改为11K，R295改为2.4K，R283改为9.1K

Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Monday, November 19, 2018	Sheet 1 of 27	




```
24V->IN12V->1.2V->1.8V->3.3V,5V->3.8V
   ->12VP->10VA
   ->12VN
```

Title	<Title>	
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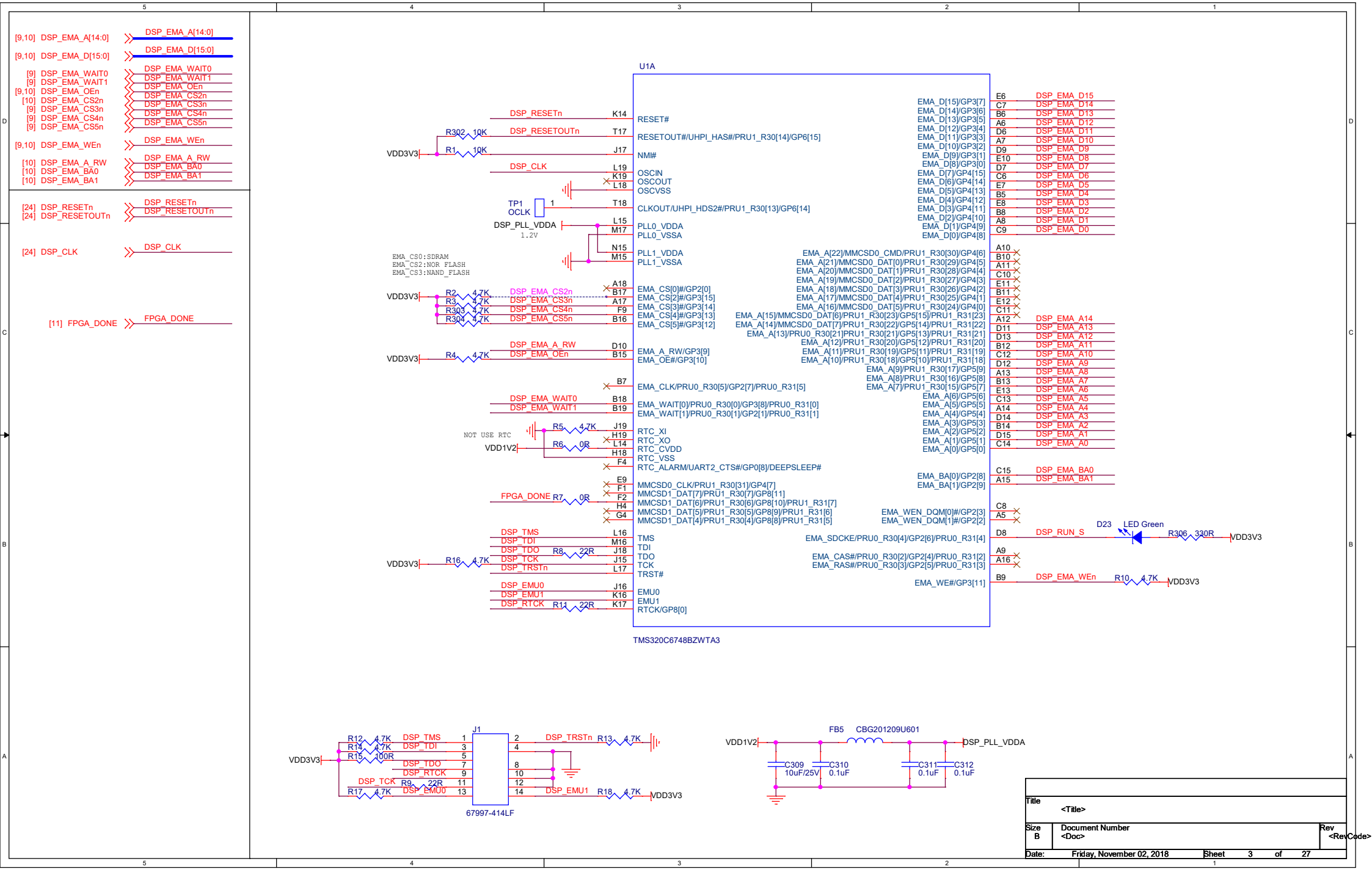
[9,10] DSP_EMA_A[14:0]
DSP_EMA_A[14:0]
[9,10] DSP_EMA_D[15:0]
DSP_EMA_D[15:0]
[9] DSP_EMA_WAIT0
[9] DSP_EMA_WAIT1
[9,10] DSP_EMA_OEn
[10] DSP_EMA_CS2n
[9] DSP_EMA_CS3n
[9] DSP_EMA_CS4n
[9] DSP_EMA_CS5n
[9,10] DSP_EMA_WEn
[10] DSP_EMA_A_RW
[10] DSP_EMA_BA0
[10] DSP_EMA_BA1
[24] DSP_RESETn
[24] DSP_RESETOUTn
[24] DSP_CLK
[11] FPGA_DONE
FPGA_DONE
U1A
DSP_RESETn
K14
RESET#
R302 10K
DSP_RESETOUTn
T17
RESETOUT#/UHPI_HAS#/PRU1_R30[14]/GP6[15]
VDD3V3
R1 10K
J17
NMI#
DSP_CLK
L19
OSCIN
K19
OSCOUT
L18
OSCVSS
TP1
OCLK
1
T18
CLKOUT/UHPI_HDS2#/PRU1_R30[13]/GP6[14]
DSP_PLL_VDDA
1.2V
L15
PLL0_VDDA
M17
PLL0_VSSA
N15
PLL1_VDDA
M15
PLL1_VSSA
EMA_CS0:SDRAM
EMA_CS2:NOR_FLASH
EMA_CS3:NAND_FLASH
R2 4.7K
DSP_EMA_CS2n
A18
EMA_CS[0]#/GP2[0]
R3 4.7K
DSP_EMA_CS3n
B17
EMA_CS[2]#/GP3[15]
R303 4.7K
DSP_EMA_CS4n
A17
EMA_CS[3]#/GP3[14]
R304 4.7K
DSP_EMA_CS5n
F9
EMA_CS[4]#/GP3[13]
B16
EMA_CS[5]#/GP3[12]
DSP_EMA_A_RW
D10
EMA_A_RW/GP3[9]
R4 4.7K
DSP_EMA_OEn
B15
EMA_OE#/GP3[10]
B7
EMA_CLK/PRU0_R30[5]/GP2[7]/PRU0_R31[5]
DSP_EMA_WAIT0
B18
EMA_WAIT[0]/PRU0_R30[0]/GP3[8]/PRU0_R31[0]
DSP_EMA_WAIT1
B19
EMA_WAIT[1]/PRU0_R30[1]/GP2[1]/PRU0_R31[1]
R5 4.7K
J19
RTC_XI
NOT USE RTC
H19
RTC_XO
VDD1V2
R6 0R
L14
RTC_CVDD
H18
RTC_VSS
F4
RTC_ALARM/UART2_CTS#/GP0[8]/DEEPSLEEP#
E9
MMCSD0_CLK/PRU1_R30[31]/GP4[7]
F1
MMCSD1_DAT[7]/PRU1_R30[7]/GP8[11]
FPGA_DONE R7 0R
F2
MMCSD1_DAT[6]/PRU1_R30[6]/GP8[10]/PRU1_R31[7]
H4
MMCSD1_DAT[5]/PRU1_R30[5]/GP8[9]/PRU1_R31[6]
G4
MMCSD1_DAT[4]/PRU1_R30[4]/GP8[8]/PRU1_R31[5]
DSP_TMS
L16
TMS
DSP_TDI
M16
TDI
DSP_TDO
R8 22R
J18
TDO
VDD3V3
R16 4.7K
DSP_TCK
J15
TCK
DSP_TRSTn
L17
TRST#
DSP_EMU0
J16
EMU0
DSP_EMU1
K16
EMU1
DSP_RTCK
R11 22R
K17
RTCK/GP8[0]
TMS320C6748BZWTA3
EMA_D[15]/GP3[7]
EMA_D[14]/GP3[6]
EMA_D[13]/GP3[5]
EMA_D[12]/GP3[4]
EMA_D[11]/GP3[3]
EMA_D[10]/GP3[2]
EMA_D[9]/GP3[1]
EMA_D[8]/GP3[0]
EMA_D[7]/GP4[15]
EMA_D[6]/GP4[14]
EMA_D[5]/GP4[13]
EMA_D[4]/GP4[12]
EMA_D[3]/GP4[11]
EMA_D[2]/GP4[10]
EMA_D[1]/GP4[9]
EMA_D[0]/GP4[8]
E6 DSP_EMA_D15
C7 DSP_EMA_D14
B6 DSP_EMA_D13
A6 DSP_EMA_D12
D6 DSP_EMA_D11
A7 DSP_EMA_D10
D9 DSP_EMA_D9
E10 DSP_EMA_D8
D7 DSP_EMA_D7
C6 DSP_EMA_D6
E7 DSP_EMA_D5
B5 DSP_EMA_D4
E8 DSP_EMA_D3
B8 DSP_EMA_D2
A8 DSP_EMA_D1
C9 DSP_EMA_D0
EMA_A[22]/MMCSD0_CMD/PRU1_R30[30]/GP4[6]
EMA_A[21]/MMCSD0_DAT[0]/PRU1_R30[29]/GP4[5]
EMA_A[20]/MMCSD0_DAT[1]/PRU1_R30[28]/GP4[4]
EMA_A[19]/MMCSD0_DAT[2]/PRU1_R30[27]/GP4[3]
EMA_A[18]/MMCSD0_DAT[3]/PRU1_R30[26]/GP4[2]
EMA_A[17]/MMCSD0_DAT[4]/PRU1_R30[25]/GP4[1]
EMA_A[16]/MMCSD0_DAT[5]/PRU1_R30[24]/GP4[0]
EMA_A[15]/MMCSD0_DAT[6]/PRU1_R30[23]/GP5[15]/PRU1_R31[23]
EMA_A[14]/MMCSD0_DAT[7]/PRU1_R30[22]/GP5[14]/PRU1_R31[22]
EMA_A[13]/PRU0_R30[21]/PRU1_R30[21]/GP5[13]/PRU1_R31[21]
EMA_A[12]/PRU1_R30[20]/GP5[12]/PRU1_R31[20]
EMA_A[11]/PRU1_R30[19]/GP5[11]/PRU1_R31[19]
EMA_A[10]/PRU1_R30[18]/GP5[10]/PRU1_R31[18]
EMA_A[9]/PRU1_R30[17]/GP5[9]
EMA_A[8]/PRU1_R30[16]/GP5[8]
EMA_A[7]/PRU1_R30[15]/GP5[7]
EMA_A[6]/GP5[6]
EMA_A[5]/GP5[5]
EMA_A[4]/GP5[4]
EMA_A[3]/GP5[3]
EMA_A[2]/GP5[2]
EMA_A[1]/GP5[1]
EMA_A[0]/GP5[0]
A10
B10
A11
C10
E11
B11
E12
C11
A12 DSP_EMA_A14
D11 DSP_EMA_A13
D13 DSP_EMA_A12
B12 DSP_EMA_A11
C12 DSP_EMA_A10
D12 DSP_EMA_A9
A13 DSP_EMA_A8
B13 DSP_EMA_A7
E13 DSP_EMA_A6
C13 DSP_EMA_A5
A14 DSP_EMA_A4
D14 DSP_EMA_A3
B14 DSP_EMA_A2
D15 DSP_EMA_A1
C14 DSP_EMA_A0
EMA_BA[0]/GP2[8]
EMA_BA[1]/GP2[9]
C15 DSP_EMA_BA0
A15 DSP_EMA_BA1
EMA_WEN_DQM[0]#/GP2[3]
EMA_WEN_DQM[1]#/GP2[2]
C8
A5
EMA_SDCKE/PRU0_R30[4]/GP2[6]/PRU0_R31[4]
D23 LED Green
D8 DSP_RUN_S
R306 330R
VDD3V3
EMA_CAS#/PRU0_R30[2]/GP2[4]/PRU0_R31[2]
EMA_RAS#/PRU0_R30[3]/GP2[5]/PRU0_R31[3]
A9
A16
EMA_WE#/GP3[11]
B9 DSP_EMA_WEn
R10 4.7K
VDD3V3
J1
R12 4.7K
DSP_TMS
1
2
DSP_TRSTn
R13 4.7K
R14 4.7K
DSP_TDI
3
4
VDD3V3
R15 100R
5
DSP_TDO
7
8
DSP_RTCK
9
10
DSP_TCK
R9 22R
11
12
DSP_EMU1
R18 4.7K
VDD3V3
R17 4.7K
DSP_EMU0
13
14
67997-414LF
VDD1V2
FB5 CBG201209U601
DSP_PLL_VDDA
C309 10uF/25V
C310 0.1uF
C311 0.1uF
C312 0.1uF
Title
<Title>
Size B
Document Number
<Doc>
Rev
<RevCode>
Date: Friday, November 02, 2018
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[8] DSP_DDR2_A[13:0] — DSP_DDR2_A[13:0]

[8] DSP_DDR2_DQ[15:0] — DSP_DDR2_DQ[15:0]

[8] DSP_DDR2_BA[2:0] — DSP_DDR2_BA[2:0]

[8] DSP_DDR2_DQS[1:0] — DSP_DDR2_DQS[1:0]

[8] DSP_DDR2_DQM[1:0] — DSP_DDR2_DQM[1:0]

[8] DSP_DDR2_CSn — DSP_DDR2_CSn

[8] DSP_DDR2_CASn — DSP_DDR2_CASn

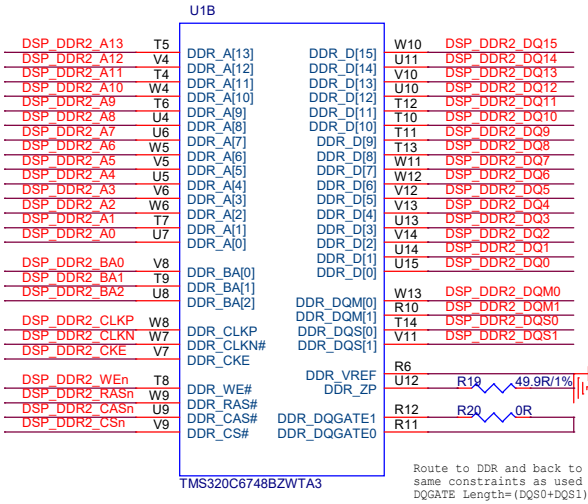
[8] DSP_DDR2_RASn — DSP_DDR2_RASn

[8] DSP_DDR2_WEn — DSP_DDR2_WEn

[8] DSP_DDR2_CKE — DSP_DDR2_CKE

[8] DSP_DDR2_CLKP — DSP_DDR2_CLKP

[8] DSP_DDR2_CLKN — DSP_DDR2_CLKN



Route to DDR and back to DDR_DQGATE0 with same constraints as used for DDR clock and data. DQGATE Length=(DQS0+DQS1)/2

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[16] LAN8710_MDIO
[16] LAN8710_MDC

[16] LAN8710_RXD3
[16] LAN8710_RXD2
[16] LAN8710_RXD1
[16] LAN8710_RXD0
[16] LAN8710_RXDV
[16] LAN8710_RXCLK
[16] LAN8710_RXER

[16] LAN8710_TXCLK
[16] LAN8710_TXEN
[16] LAN8710_TXD0
[16] LAN8710_TXD1
[16] LAN8710_TXD2
[16] LAN8710_TXD3
[16] LAN8710_COL
[16] LAN8710_CRS

[16] LAN8710_nINT

[15,23] DSP_SDA
[15,23] DSP_SCL

[23] MPU9250_INT
[15] AT24CXX_WP

[14] DSP_DEG_TX
[14] DSP_DEB_RX

[17] LTE_UART_TXD
[17] LTE_UART_RXD
[17] LTE_RESET

[10] DSP_FPGA_SCLK
[10] DSP_FPGA_nCS
[10] DSP_FPGA_SDI
[10] DSP_FPGA_SDO

[10] DSP_FPGA_D[7:0]

U1C

LAN8710_RXD0 D16
LAN8710_RXCLK D19
LAN8710_RXDV C17
LAN8710_MDIO D17
LAN8710_MDC E16
LAN8710_RXD1 E17
LAN8710_RXD2 D18
LAN8710_RXD3 C19
LAN8710_CRS C18
LAN8710_RXER C16

DSP_FPGA_SCLK G19
H16
DSP_FPGA_nCS E19
LTE_RESET F18
DSP_DEG_TX F19
DSP_DEB_RX E18
LTE_UART_TXD F16
LTE_UART_RXD F17
DSP_SDA G18
DSP_SCL G16
DSP_FPGA_SDI G17
DSP_FPGA_SDO H17

AT24CXX_WP R17
R16
U17
MPU9250_INT W15
U16
T15
G1
G2
J4
G3

LED_RUN R5

SPI0_SCS[2]#/UART0_RTS#/GP8[1]/MII_RXD[0]
SPI0_CLK/EPWM0A/GP1[8]/MII_RXCLK
SPI0_ENA#/EPWM0B/PRU0_R30[6]/MII_RXDV
SPI0_SCS[0]#/TM64P1_OUT12/GP1[6]/MDIO_D/TM64P1_IN12
SPI0_SCS[1]#/TM64P0_OUT12/GP1[7]/MDIO_CLK/TM64PO_IN12
SPI0_SCS[3]#/UART0_CTS#/GP8[2]/MII_RXD[1]
SPI0_SCS[4]#/UART0_TXD/GP8[3]/MII_RXD[2]
SPI0_SCS[5]#/UART0_RXD/GP8[4]/MII_RXD[3]
SPI0_SIMO/EPWMSYNCO/GP8[5]/MII_CRS
SPI0_SOMI/EPWMSYNCI/GP8[6]/MII_RXER

SPI1_CLK/GP2[13]
SPI1_ENA/GP2[12]
SPI1_SCS[0]#/EPWM1B/PRU0_R30[7]/GP2[14]/TM64P3_IN12
SPI1_SCS[1]#/EPWM1A/PRU0_R30[8]/GP2[15]/TM64P2_IN12
SPI1_SCS[2]#/UART1_TXD/GP1[0]
SPI1_SCS[3]#/UART1_RXD/GP1[1]
SPI1_SCS[4]#/UART2_TXD/I2C1_SDA/GP1[2]
SPI1_SCS[5]#/UART2_RXD/I2C1_SCL/GP1[3]
SPI1_SCS[6]#/I2C0_SDA/TM64P3_OUT12/GP1[4]
SPI1_SCS[7]#/I2C0_SCL/TM64P2_OUT12/GP1[5]
SPI1_SIMO/GP2[10]
SPI1_SOMI/GP2[11]

PRU0_R30[31]/UHPI_HRDY#/PRU1_R30[12]/GP6[13]
PRU0_R30[30]/UHPI_HINT#/PRU1_R30[11]/GP6[12]
PRU0_R30[29]/UHPI_HCNTL0/UPP_CHA_CLOCK/GP6[11]
PRU0_R30[28]/UHPI_HCNTL1/UPP_CHA_START/GP6[10]
PRU0_R30[27]/UHPI_HHWIL/UPP_CHA_ENABLE/GP6[9]
PRU0_R30[26]/UHPI_HRW#/UPP_CHA_WAIT/GP6[8]PRU1_R31[17]
PRU0_R30[25]/MMCSD1_DAT[0]/UPP_CHB_CLOCK/GP8[15]/PRU1_R31[27]
PRU0_R30[24]/MMCSD1_CLK/UPP_CHB_START/GP8[14]/PRU1_R31[26]
PRU0_R30[23]/MMCSD1_CMD/UPP_CHB_ENABLE/GP8[13]/PRU1_R31[25]
PRU0_R30[22]/PRU1_R30[8]/UPP_CHB_WAIT/GP8[12]/PRU1_R31[24]

GP6[0]/PRU1_R31[28]

AXR15/EPWM0TZ[0]/ECAP2_APWM2/GP0[7]
AXR14/CLKR1/GP0[6]
AXR13/CLKX1/GP0[5]
AXR12/FSR1/GP0[4]
AXR11/FSX1/GP0[3]
AXR10/DR1/GP0[2]
AXR9/DX1/GP0[1]
AXR8/CLKS1/ECAP1_APWM1/GP0[0]/PRU0_R31[8]
AXR7/EPWM1TZ[0]/PRU0_R30[17]/GP1[15]/PRU0_R31[7]
AXR6/CLKR0/GP1[14]/MII_TXEN/PRU0_R31[6]
AXR5/CLKX0/GP1[13]/MII_TXCLK
AXR4/FSR0/GP1[12]/MII_COL
AXR3/FSX0/GP1[11]/MII_TXD[3]
AXR2/DR0/GP1[10]/MII_TXD[2]
AXR1/DX0/GP1[9]/MII_TXD[1]
AXR0/ECAP0_APWM0/GP8[7]/MII_TXD[0]/CLKS0
AHCLKX3/USB_REFCLKIN/UART1_CTS#/GP0[10]/PRU0_R31[17]
ACLKX/PRU0_R30[19]/GP0[14]/PRU0_R31[21]
AFSX/GP0[12]/PRU0_R31[19]
AHCLKR/PRU0_R30[18]/UART1_RTS#/GP0[11]/PRU0_R31[18]
ACLKR/PRU0_R30[20]/GP0[15]/PRU0_R31[22]
AFSR/GP0[13]/PRU0_R31[20]
AMUTE/PRU0_R30[16]/UART2_RTS#/GP0[9]/PRU0_R31[16]

USB0_DRVVBUS
USB0_VBUS
USB0_ID
USB0_DP
USB0_DM

USB1_DP
USB1_DM

SATA_REFCLKN#
SATA_REFCLKP
SATA_TXN#
SATA_TXP
SATA_RXN#
SATA_RXP

A4 DSP_FPGA_D7
B4 DSP_FPGA_D6
B3 DSP_FPGA_D5
C4 DSP_FPGA_D4
C5 DSP_FPGA_D3
D4 DSP_FPGA_D2
C3 DSP_FPGA_D1
E4 DSP_FPGA_D0
D2
C1 LAN8710_TXEN
D3 LAN8710_TXCLK
D1 LAN8710_COL
E3 R21 100R LAN8710_TXD3
E2 R22 100R LAN8710_TXD2
E1 R23 100R LAN8710_TXD1
F3 R24 100R LAN8710_TXD0
A3
B1
B2
A2
A1 LAN8710_nINT
C2
D5

K18
N19
P16
M19
M18 NOT USE USB

P19
P18

N1
N2
J2
J1 NOT USE SATA
L2
L1

TMS320C6748BZWTA3

D1
R25 10K VDD24V
LED_RUN
R26 1K VDD3V3
SSB-LX2300

Title	<Title>	
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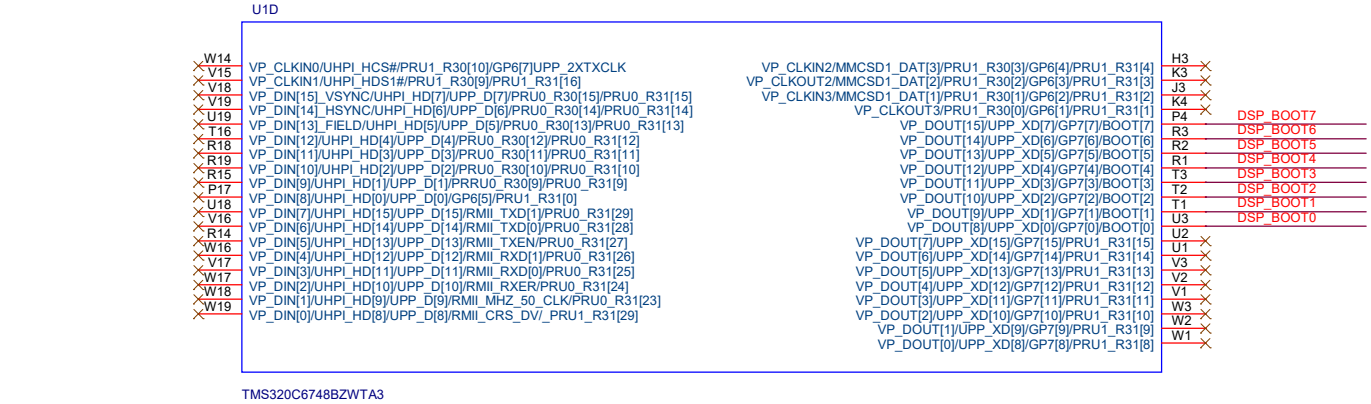
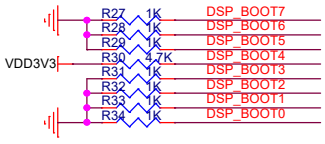


BOOT[7:0]	BOOT MODE	AIS
0xx1 0000	NAND16	Yes

BOOT[6:5]	BLOCK	PLL0 Applied
00	1	None
01	1	PLLM=24,POSTDIV=3,SYSCLK3=2
10	0	None
11	0	PLLM=24,POSTDIV=3,SYSCLK3=2



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Size B	Document Number <Doc>	Rev <RevCode>
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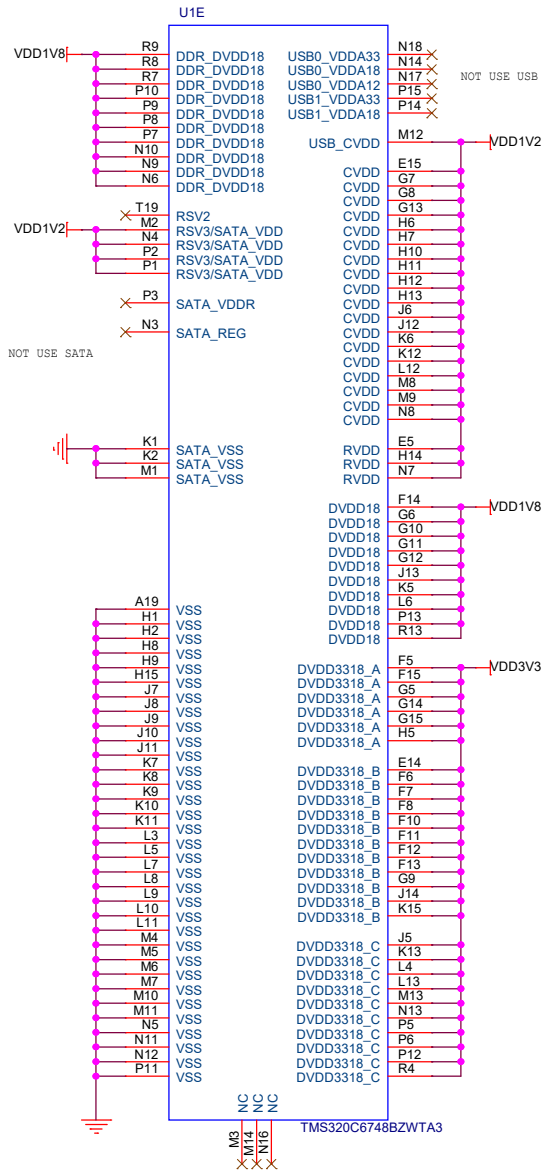

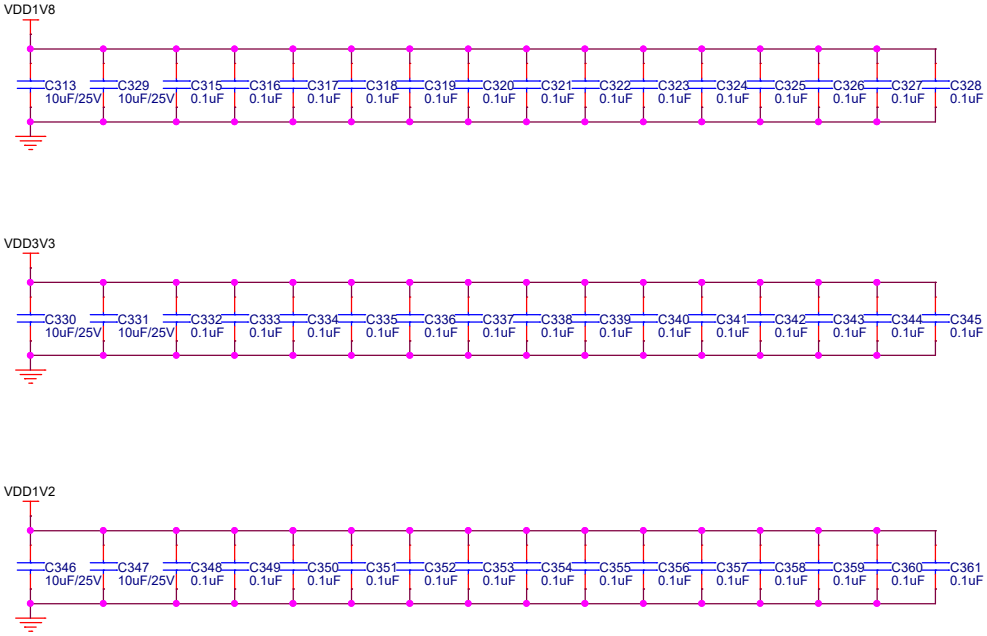

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Size B	Document Number <Doc>	Rev <RevCode>
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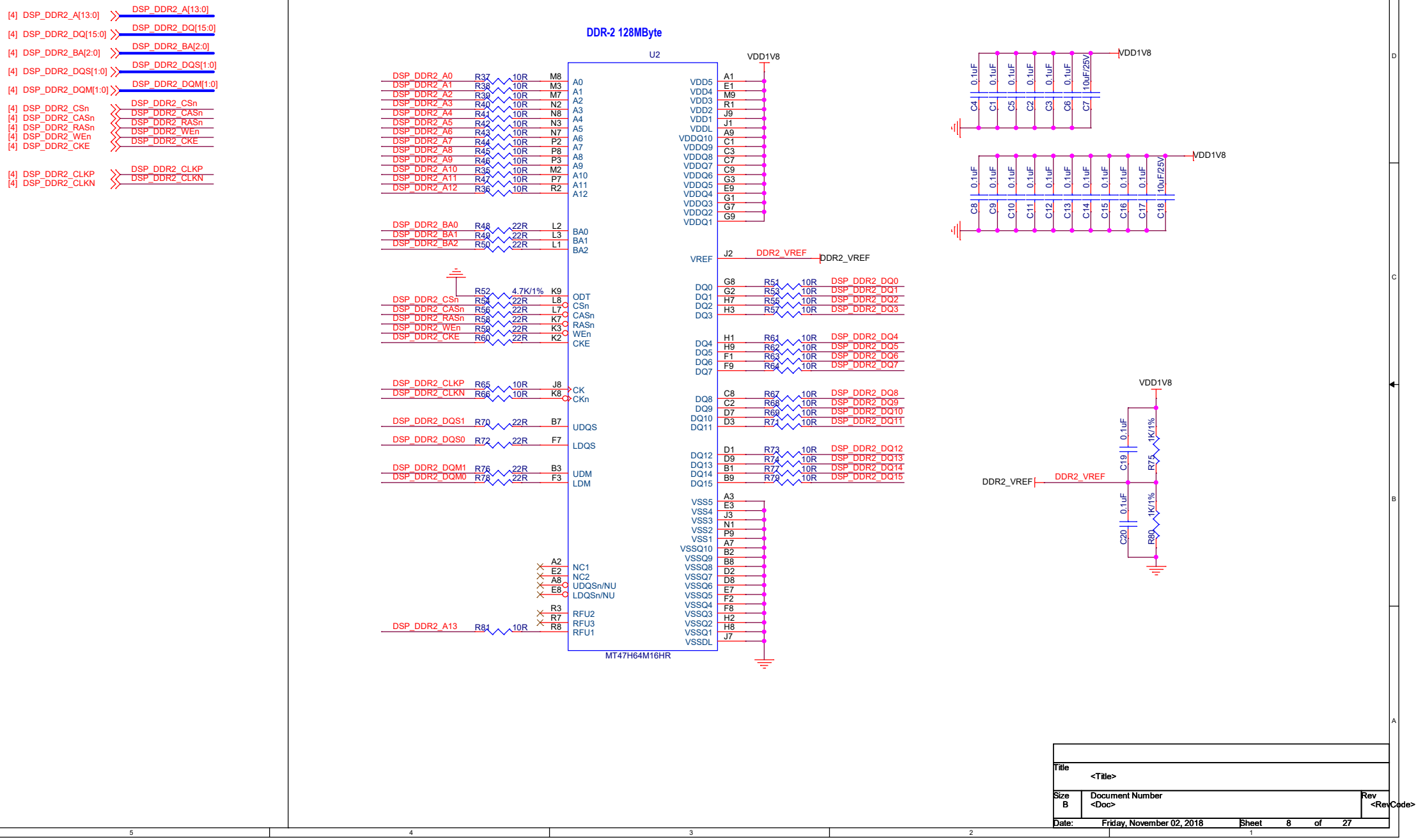
[4] DSP_DDR2_A[13:0]
DSP_DDR2_A[13:0]
[4] DSP_DDR2_DQ[15:0]
DSP_DDR2_DQ[15:0]
[4] DSP_DDR2_BA[2:0]
DSP_DDR2_BA[2:0]
[4] DSP_DDR2_DQS[1:0]
DSP_DDR2_DQS[1:0]
[4] DSP_DDR2_DQM[1:0]
DSP_DDR2_DQM[1:0]
[4] DSP_DDR2_CSn
[4] DSP_DDR2_CASn
[4] DSP_DDR2_RASn
[4] DSP_DDR2_WEn
[4] DSP_DDR2_CKE
DSP_DDR2_CSn
DSP_DDR2_CASn
DSP_DDR2_RASn
DSP_DDR2_WEn
DSP_DDR2_CKE
[4] DSP_DDR2_CLKP
[4] DSP_DDR2_CLKN
DSP_DDR2_CLKP
DSP_DDR2_CLKN
DDR-2 128MByte
U2
MT47H64M16HR
VDD1V8
DDR2_VREF
DSP_DDR2_A0
DSP_DDR2_A1
DSP_DDR2_A2
DSP_DDR2_A3
DSP_DDR2_A4
DSP_DDR2_A5
DSP_DDR2_A6
DSP_DDR2_A7
DSP_DDR2_A8
DSP_DDR2_A9
DSP_DDR2_A10
DSP_DDR2_A11
DSP_DDR2_A12
DSP_DDR2_BA0
DSP_DDR2_BA1
DSP_DDR2_BA2
DSP_DDR2_CSn
DSP_DDR2_CASn
DSP_DDR2_RASn
DSP_DDR2_WEn
DSP_DDR2_CKE
DSP_DDR2_CLKP
DSP_DDR2_CLKN
DSP_DDR2_DQS1
DSP_DDR2_DQS0
DSP_DDR2_DQM1
DSP_DDR2_DQM0
DSP_DDR2_A13
DSP_DDR2_DQ0
DSP_DDR2_DQ1
DSP_DDR2_DQ2
DSP_DDR2_DQ3
DSP_DDR2_DQ4
DSP_DDR2_DQ5
DSP_DDR2_DQ6
DSP_DDR2_DQ7
DSP_DDR2_DQ8
DSP_DDR2_DQ9
DSP_DDR2_DQ10
DSP_DDR2_DQ11
DSP_DDR2_DQ12
DSP_DDR2_DQ13
DSP_DDR2_DQ14
DSP_DDR2_DQ15
Title
<Title>
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Document Number
<Doc>
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<RevCode>
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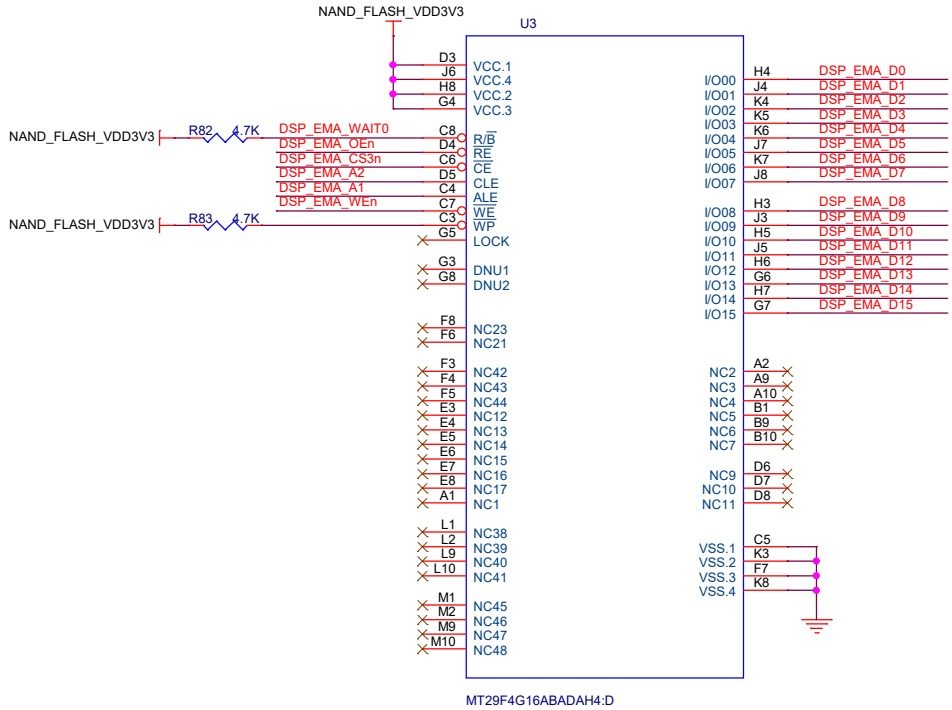
[3,10] DSP_EMA_D[15:0] — DSP_EMA_D[15:0]

[3] DSP_EMA_WAIT0 — DSP_EMA_WAIT0
[3,10] DSP_EMA_OEn — DSP_EMA_OEn
[3] DSP_EMA_CS3n — DSP_EMA_CS3n
[3,10] DSP_EMA_WEn — DSP_EMA_WEn

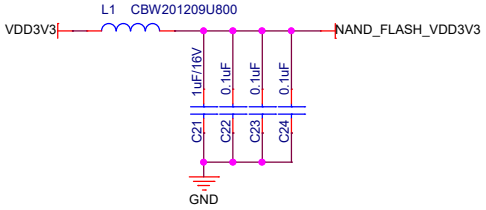
[3,10] DSP_EMA_A[12:0] — DSP_EMA_A[12:0]

NAND FLASH 512MByte



MT29F4G16ABADAH4:D

DECAPs FOR FLASH



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Size B	Document Number <Doc>	Rev <RevCode>
Date: Thursday, October 25, 2018	Sheet 9 of 27	

[3,9] DSP_EMA_A[14:0] — DSP_EMA_A[14:0]

[3,9] DSP_EMA_D[15:0] — DSP_EMA_D[15:0]

[9] DSP_EMA_WAIT1 — DSP_EMA_WAIT1
[3,9] DSP_EMA_OEn — DSP_EMA_OEn
[3] DSP_EMA_CS2n — DSP_EMA_CS2n
[9] DSP_EMA_CS4n — DSP_EMA_CS4n
[9] DSP_EMA_CS5n — DSP_EMA_CS5n

[3,9] DSP_EMA_WEn — DSP_EMA_WEn

[10] DSP_EMA_A_RW — DSP_EMA_A_RW
[10] DSP_EMA_BA0 — DSP_EMA_BA0
[3] DSP_EMA_BA1 — DSP_EMA_BA1

[18] FPGA_CANR[7:0] — FPGA_CANR[7:0]

[18] FPGA_CAND[7:0] — FPGA_CAND[7:0]

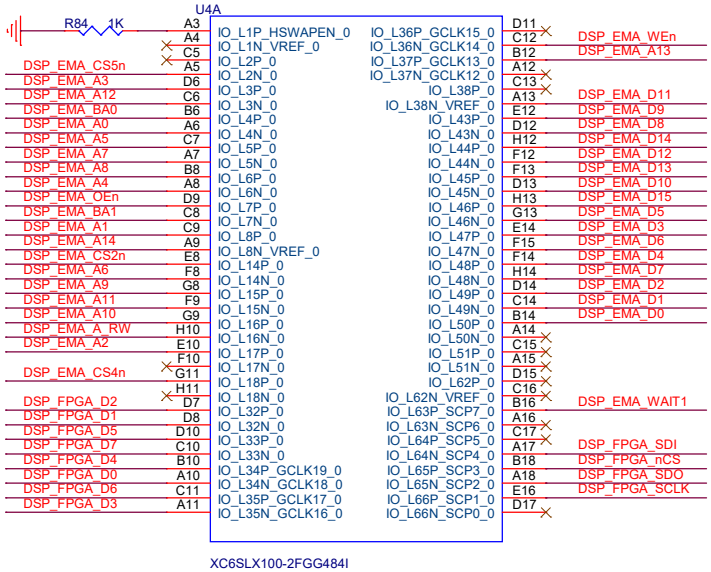
[24] FPGA_CLK — FPGA_CLK

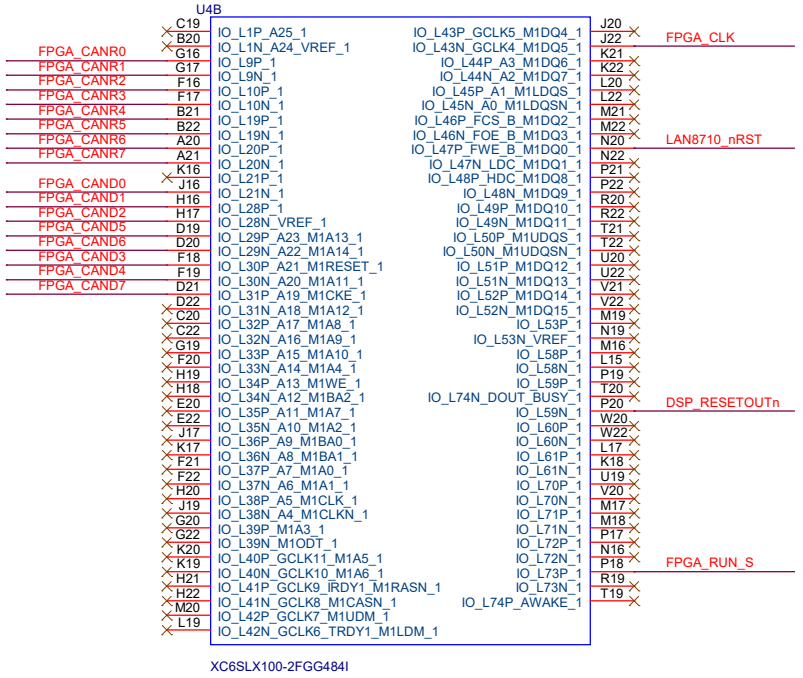
[24] DSP_RESETOUTn — DSP_RESETOUTn

[16] LAN8710_nRST — LAN8710_nRST

[5] DSP_FPGA_SCLK — DSP_FPGA_SCLK
[5] DSP_FPGA_nCS — DSP_FPGA_nCS
[5] DSP_FPGA_SDI — DSP_FPGA_SDI
[5] DSP_FPGA_SDO — DSP_FPGA_SDO

[5] DSP_FPGA_D[7:0] — DSP_FPGA_D[7:0]





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Size B	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, October 24, 2018	Sheet 10 of 27	

[3] FPGA_DONE — FPGA_DONE

[13] CFG_SPI_CS — CFG_SPI_CS
[13] CFG_SPI_MISO — CFG_SPI_MISO
[13] CFG_SPI_CCLK — CFG_SPI_CCLK
[13] CFG_SPI_MOSI — CFG_SPI_MOSI

[13] FPGA_M0 — FPGA_M0
[13] FPGA_M1 — FPGA_M1

[19] UART1_TX1 — UART1_TX1
[19] UART1_TX2 — UART1_TX2
[19] UART2_TX1 — UART2_TX1
[19] UART2_TX2 — UART2_TX2
[19] UART3_TX1 — UART3_TX1
[19] UART3_TX2 — UART3_TX2
[19] UART4_TX1 — UART4_TX1
[19] UART4_TX2 — UART4_TX2
[19] UART5_TX1 — UART5_TX1
[19] UART5_TX2 — UART5_TX2
[19] UART6_TX1 — UART6_TX1
[19] UART6_TX2 — UART6_TX2

[19] UART1_RX1 — UART1_RX1
[19] UART1_RX2 — UART1_RX2
[19] UART2_RX1 — UART2_RX1
[19] UART2_RX2 — UART2_RX2
[19] UART3_RX1 — UART3_RX1
[19] UART3_RX2 — UART3_RX2
[19] UART4_RX1 — UART4_RX1
[19] UART4_RX2 — UART4_RX2
[19] UART5_RX1 — UART5_RX1
[19] UART5_RX2 — UART5_RX2
[19] UART6_RX1 — UART6_RX1
[19] UART6_RX2 — UART6_RX2

[19] UART1_485_232 — UART1_485_232
[19] UART2_485_232 — UART2_485_232
[19] UART3_485_232 — UART3_485_232
[19] UART4_485_232 — UART4_485_232
[19] UART5_485_232 — UART5_485_232
[19] UART6_485_232 — UART6_485_232

[20] F_RELAY_DET[16:1] — F_RELAY_DET[16:1]
[20] F_RELAY_CON[16:1] — F_RELAY_CON[16:1]
[20] F_RELAY_OEn[2:1] — F_RELAY_OEn[2:1]

[21] F_TTL_D[15:0] — F_TTL_D[15:0]
[21] F_TTL_DIR1 — F_TTL_DIR1
[21] F_TTL_DIR2 — F_TTL_DIR2
[21] F_TTL_En — F_TTL_En

[22] AD7321_DOUT — AD7321_DOUT
[22] AD7321_SCLK — AD7321_SCLK
[22] AD7321_CSn — AD7321_CSn
[22] AD7321_DIN — AD7321_DIN

U4C

VDD3V3 — R85 4.7K — FPGA_DONE
CFG_SPI_CCLK
FPGA_M0
CFG_SPI_MISO
CFG_SPI_MOSI
F_TTL_D12
F_TTL_D14
F_TTL_D6
F_TTL_D8
F_TTL_D10
F_TTL_D11
F_TTL_D9
F_TTL_En
F_TTL_D13
F_TTL_D15
FPGA_M1
F_TTL_D4
F_TTL_DIR2
F_TTL_D2
F_TTL_DIR1
F_TTL_D3
F_TTL_D7
F_TTL_D5
F_TTL_D1
AD7321_DOUT
AD7321_SCLK
AD7321_CSn
AD7321_DIN

CMPCS_B_2	Y20	IO_L40P_2	R11
DONE_2	Y22	IO_L40N_2	T11
IO_L1P_CCLK_2	Y21	IO_L41P_2	AA10
IO_L1N_M0_CMPMISO_2	AA22	IO_L41N_VREF_2	AB10
IO_L2P_CMPCLK_2	AA21	IO_L42P_2	V11
IO_L2N_CMPMOSI_2	AB21	IO_L42N_2	W11
IO_L3P_D0_DIN_MISO_MISO1_2	AA20	IO_L43P_2	Y9
IO_L3N_MOSI_CSI_B_MISO0_2	AB20	IO_L43N_2	AB9
IO_L4P_2	T18	IO_L44P_2	W10
IO_L4N_VREF_2	T17	IO_L44N_2	Y10
IO_L5P_2	Y19	IO_L44N_2	AA8
IO_L5N_2	AB19	IO_L45P_2	AB8
IO_L6P_2	W18	IO_L45N_2	W8
IO_L6N_2	Y18	IO_L46P_2	V7
IO_L7P_2	T16	IO_L46N_2	W9
IO_L7N_2	T15	IO_L47P_2	Y8
IO_L8P_2	U17	IO_L47N_2	Y7
IO_L8N_2	U16	IO_L48P_D7_2	AB7
IO_L9P_2	V19	IO_L48N_RDWR_B_VREF_2	AA6
IO_L9N_2	V18	IO_L49P_D3_2	AB6
IO_L10P_2	R16	IO_L49N_D4_2	U9
IO_L10N_2	R15	IO_L50P_2	V9
IO_L11P_2	V17	IO_L50N_2	AA4
IO_L11N_2	W17	IO_L57P_2	AB4
IO_L12P_D1_MISO2_2	U14	IO_L57N_2	Y3
IO_L12N_D2_MISO3_2	U13	IO_L58P_2	AB3
IO_L13P_M1_2	U15	IO_L58N_2	R9
IO_L13N_D10_2	V15	IO_L59P_2	R8
IO_L14P_D11_2	AA18	IO_L59N_2	T7
IO_L14N_D12_2	AB18	IO_L60P_2	R7
IO_L15P_2	Y17	IO_L60N_2	W4
IO_L15N_2	AB17	IO_L62P_D5_2	Y4
IO_L16P_2	AA14	IO_L62N_D6_2	U6
IO_L16N_VREF_2	AB14	IO_L63P_2	V5
IO_L18P_2	V13	IO_L63N_2	AA2
IO_L18N_2	W13	IO_L64P_D8_2	AB2
IO_L19P_2	AA16	IO_L64N_D9_2	T6
IO_L19N_2	AB16	IO_L65P_INIT_B_2	T5
IO_L20P_2	W14	IO_L65N_CSO_B_2	AA1
IO_L20N_2	Y14	PROGRAM_B_2	
IO_L21P_2	Y15	N.C.	U12
IO_L21N_2	AB15	N.C.	T12
IO_L23P_2	T14	N.C.	Y16
IO_L23N_2	R13	N.C.	W15
IO_L29P_GCLK3_2	W12	N.C.	T8
IO_L29N_GCLK2_2	Y12	N.C.	U8
IO_L30P_GCLK1_D13_2	Y13	N.C.	T10
IO_L30N_GCLK0_USERCCLK_2	AB13	N.C.	U10
IO_L31P_GCLK31_D14_2	AA12	N.C.	AB5
IO_L31N_GCLK30_D15_2	AB12	N.C.	Y5
IO_L32P_GCLK29_2	Y11	N.C.	Y6
IO_L32N_GCLK28_2	AB11	N.C.	W6

FPGA_INIT
CFG_SPI_CS
R86 4.7K — VDD3V3

XC6SLX100-2FGG484I

U4D

F_RELAY_DET16	Y2	IO_L1P_3	M3
F_RELAY_DET15	Y1	IO_L1N_VREF_3	L4
F_RELAY_DET13	W3	IO_L2P_3	K5
F_RELAY_DET14	W1	IO_L2N_3	K4
F_RELAY_DET4	P8	IO_L7P_3	K3
F_RELAY_DET3	P7	IO_L7N_3	J4
F_RELAY_OEn1	P6	IO_L8P_3	K6
F_RELAY_OEn2	P5	IO_L8N_3	J6
F_RELAY_DET10	T4	IO_L9P_3	H4
F_RELAY_DET9	T3	IO_L9N_3	H3
F_RELAY_DET12	U4	IO_L10P_3	H2
F_RELAY_DET11	V3	IO_L10N_3	H1
F_RELAY_DET1	N6	IO_L11P_3	G3
F_RELAY_DET2	N7	IO_L11N_3	G1
F_RELAY_DET5	M7	IO_L23P_3	H6
F_RELAY_DET8	M8	IO_L23N_3	H5
	R4	IO_L24P_3	F2
F_RELAY_CON7	P4	IO_L24N_3	F1
F_RELAY_CON8	M6	IO_L25P_3	G4
F_RELAY_CON10	L6	IO_L25N_3	F3
F_RELAY_CON4	P3	IO_L26P_3	E3
F_RELAY_CON5	N4	IO_L26N_3	E1
F_RELAY_CON6	M5	IO_L31P_3	D2
F_RELAY_CON15	M4	IO_L31N_VREF_3	D1
F_RELAY_CON13	V2	IO_L32P_M3DQ14_3	C3
F_RELAY_CON16	V1	IO_L32N_M3DQ15_3	C1
F_RELAY_CON11	U3	IO_L33P_M3DQ12_3	G6
F_RELAY_CON14	U1	IO_L33N_M3DQ13_3	F5
F_RELAY_CON9	T2	IO_L34P_M3UDQS_3	K7
F_RELAY_CON12	T1	IO_L34N_M3UDQSN_3	K8
F_RELAY_CON1	R3	IO_L35P_M3DQ10_3	D5
F_RELAY_CON2	R1	IO_L35N_M3DQ11_3	E4
F_RELAY_CON3	P2	IO_L36P_M3DQ8_3	J7
	P1	IO_L36N_M3DQ9_3	H8
	N3	IO_L37P_M3DQ0_3	B2
	N1	IO_L37N_M3DQ1_3	B1
	M2	IO_L38P_M3DQ2_3	G7
	M1	IO_L38N_M3DQ3_3	F7
F_RELAY_DET7	L3	IO_L39P_M3LDQS_3	D3
F_RELAY_DET6	L1	IO_L39N_M3LDQSN_3	C4
	K2	IO_L40P_M3DQ6_3	E5
	K1	IO_L40N_M3DQ7_3	E6
	J3	IO_L41P_GCLK27_M3DQ4_3	A2
	J1	IO_L41N_GCLK26_M3DQ5_3	B3
		IO_L42P_GCLK25_TRDY2_M3UDM_3	M3
		IO_L42N_GCLK24_M3LDM_3	L4
		IO_L43P_GCLK23_M3RASN_3	K5
		IO_L43N_GCLK22_IRDY2_M3CASN_3	K4
		IO_L44P_GCLK21_M3A5_3	K3
		IO_L44N_GCLK20_M3A6_3	J4
		IO_L45P_M3A3_3	K6
		IO_L45N_M3ODT_3	J6
		IO_L46P_M3CLK_3	H4
		IO_L46N_M3CLKN_3	H3
		IO_L47P_M3A0_3	H2
		IO_L47N_M3A1_3	H1
		IO_L48P_M3BA0_3	G3
		IO_L48N_M3BA1_3	G1
		IO_L49P_M3A7_3	H6
		IO_L49N_M3A2_3	H5
		IO_L50P_M3WE_3	F2
		IO_L50N_M3BA2_3	F1
		IO_L51P_M3A10_3	G4
		IO_L51N_M3A4_3	F3
		IO_L52P_M3A8_3	E3
		IO_L52N_M3A9_3	E1
		IO_L53P_M3CKE_3	D2
		IO_L53N_M3A12_3	D1
		IO_L54P_M3RESET_3	C3
		IO_L54N_M3A11_3	C1
		IO_L55P_M3A13_3	G6
		IO_L55N_M3A14_3	F5
		IO_L57P_3	K7
		IO_L57N_VREF_3	K8
		IO_L58P_3	D5
		IO_L58N_3	E4
		IO_L59P_3	J7
		IO_L59N_3	H8
		IO_L60P_3	B2
		IO_L60N_3	B1
		IO_L80P_3	G7
		IO_L80N_3	F7
		IO_L81P_3	D3
		IO_L81N_3	C4
		IO_L82P_3	E5
		IO_L82N_3	E6
		IO_L83P_3	A2
		IO_L83N_VREF_3	B3

UART2_TX2
UART2_TX1
UART1_TX2
UART3_TX2
UART3_TX1
UART1_TX1
UART5_TX1
UART6_TX1
UART4_TX1
UART1_RX1
UART2_RX1
UART6_RX2
UART6_RX1
UART5_RX2
UART5_RX1
UART4_RX2
UART4_RX1
UART3_RX2
UART2_RX2
UART3_RX1
UART3_485_232
UART2_485_232
UART4_485_232
UART5_485_232
UART1_485_232
UART6_485_232

XC6SLX100-2FGG484I

VDD3V3 — R88 330R — FPGA_DONE — Q1 2N7002 — D2 LED Green — R87 330R — VDD3V3 — GND
VDD3V3 — R90 330R — FPGA_INIT — Q2 2N7002 — D3 LED Green — R89 330R — VDD3V3 — GND

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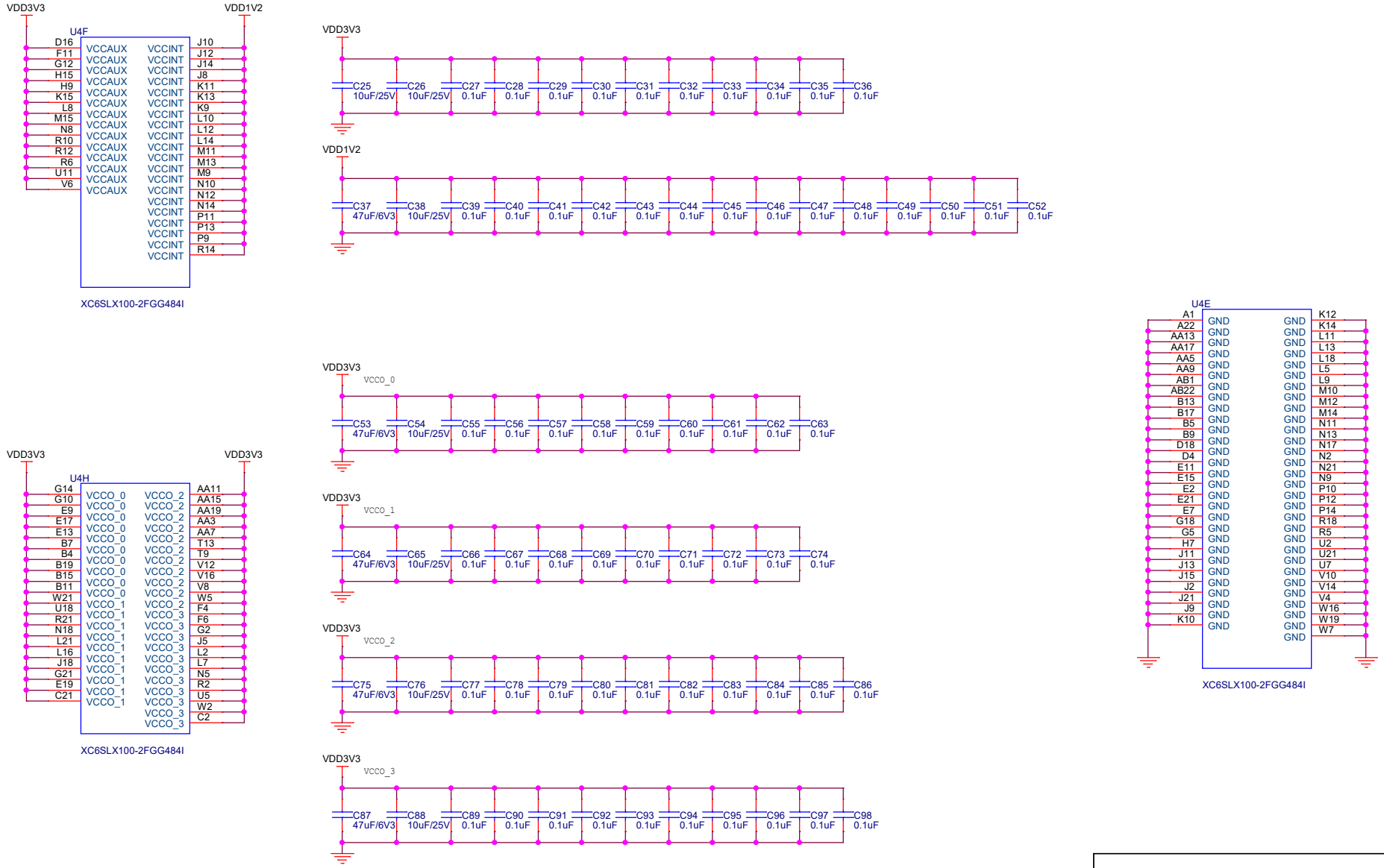

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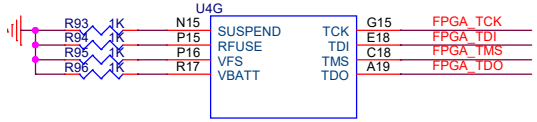
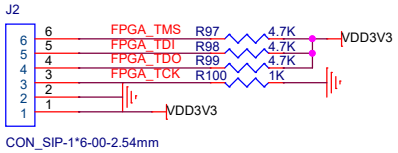
[11] FPGA_M0
[11] FPGA_M1
FPGA_M0
FPGA_M1

[11] CFG_SPI_CS
[11] CFG_SPI_MISO
[11] CFG_SPI_CCLK
[11] CFG_SPI_MOSI
CFG_SPI_CS
CFG_SPI_MISO
CFG_SPI_CCLK
CFG_SPI_MOSI

When not programming or when not using the key EFUSE,
connecting RFUSE,VFS,VBATT to VCCAUX or GND is recommended.

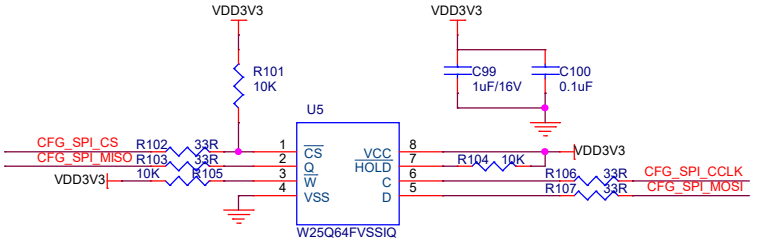


XC6SLX100-2FGG484I



CON_SIP-1*6-00-2.54mm

Configuration Mode	M[1:0]	Bus Width	CCLK Direction
Master Serial/SPI	01	1, 2, 4(1)	Output
Master SelectMAP/BPI(2)	00	8, 16	Output
JTAG(3)	xx	1	Input (TCK)
Slave SelectMAP(2)	10	8, 16	Input
Slave Serial(4)	11	1	Input



W25Q64FVSSIQ

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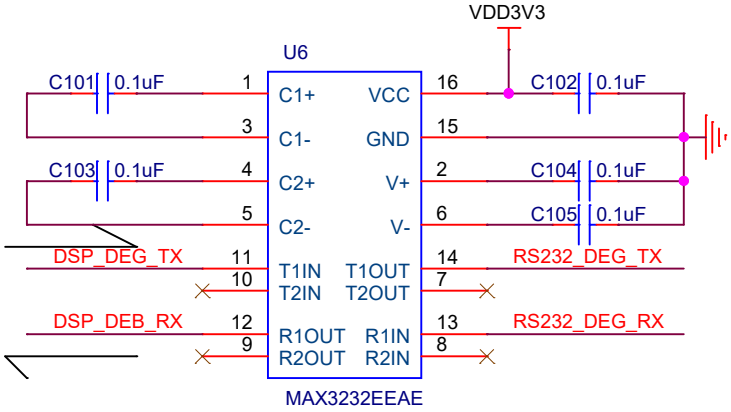
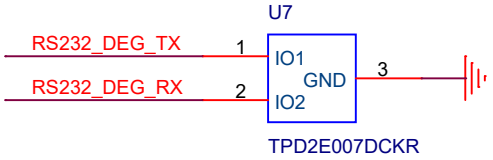
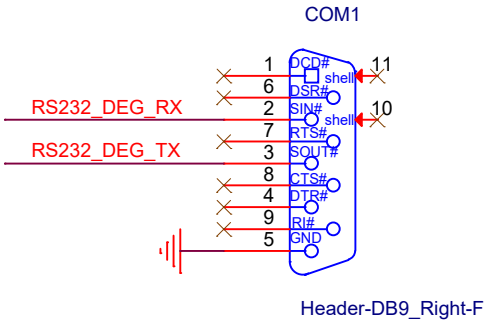
[5] DSP_DEG_TX
[5] DSP_DEB_RX







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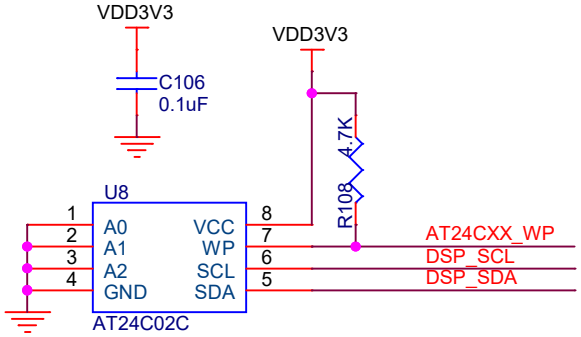
[5,23] DSP_SDA
[5,23] DSP_SCL
[5] AT24CXX_WP

DSP_SDA
DSP_SCL
AT24CXX_WP



Title	AT24C08	
Size A	Document Number <Doc>	Rev 1.0
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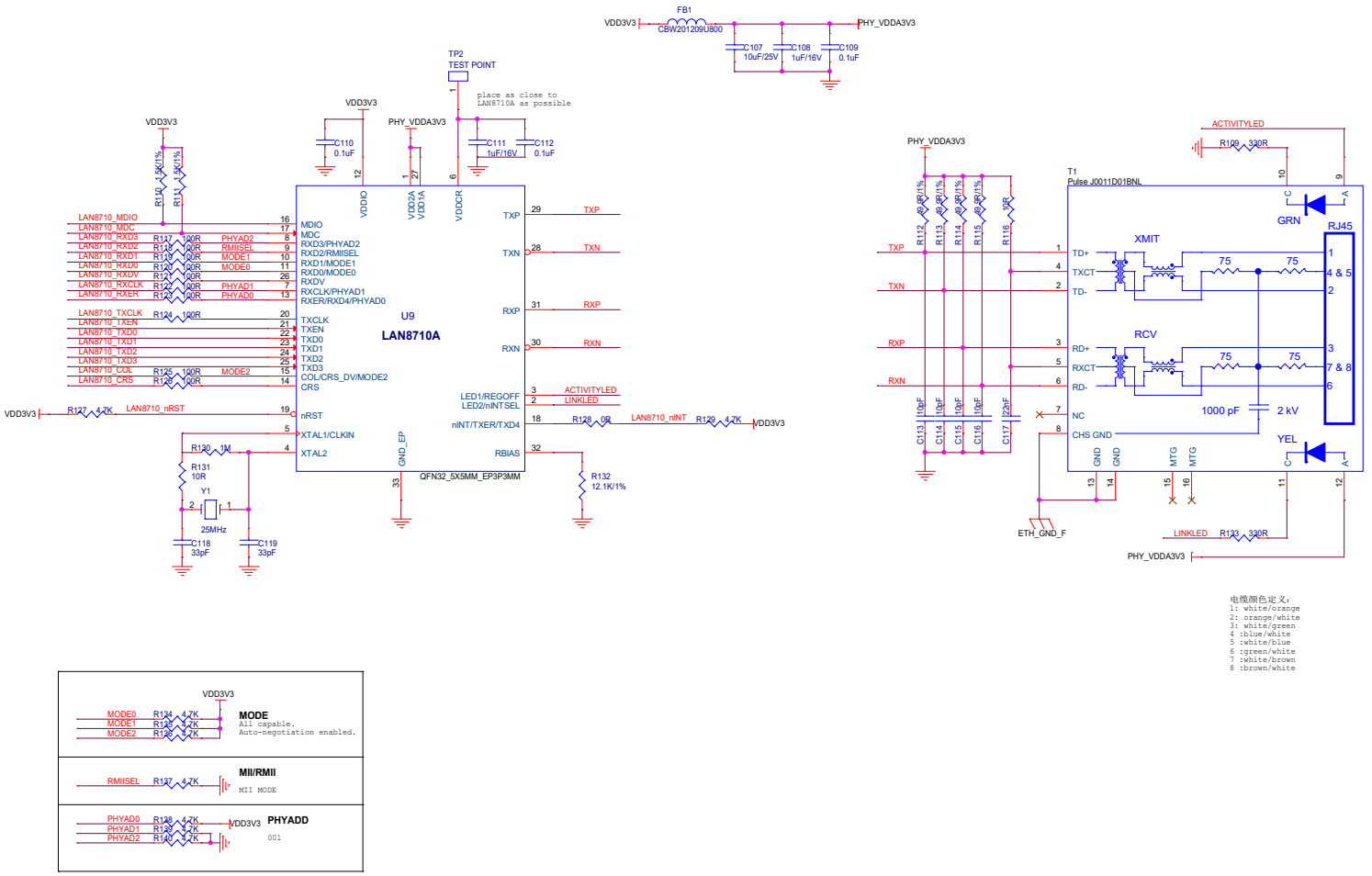
[5] LAN8710_MDIO
[5] LAN8710_MDC

[5] LAN8710_RXD3
[5] LAN8710_RXD2
[5] LAN8710_RXD1
[5] LAN8710_RXD0
[5] LAN8710_RXDV
[5] LAN8710_RXCLK
[5] LAN8710_RXER

[5] LAN8710_TXCLK
[5] LAN8710_TXEN
[5] LAN8710_TXD0
[5] LAN8710_TXD1
[5] LAN8710_TXD2
[5] LAN8710_TXD3
[5] LAN8710_COL
[5] LAN8710_CRS

[10] LAN8710_nRST
[5] LAN8710_nINT



电缆颜色定义：
1: white/orange
2: orange/white
3: white/green
4 :blue/white
5 :white/blue
6 :green/white
7 :white/brown
8 :brown/white

MODE
All capable.
Auto-negotiation enabled.

MII/RMII
MII MODE

PHYADD
001

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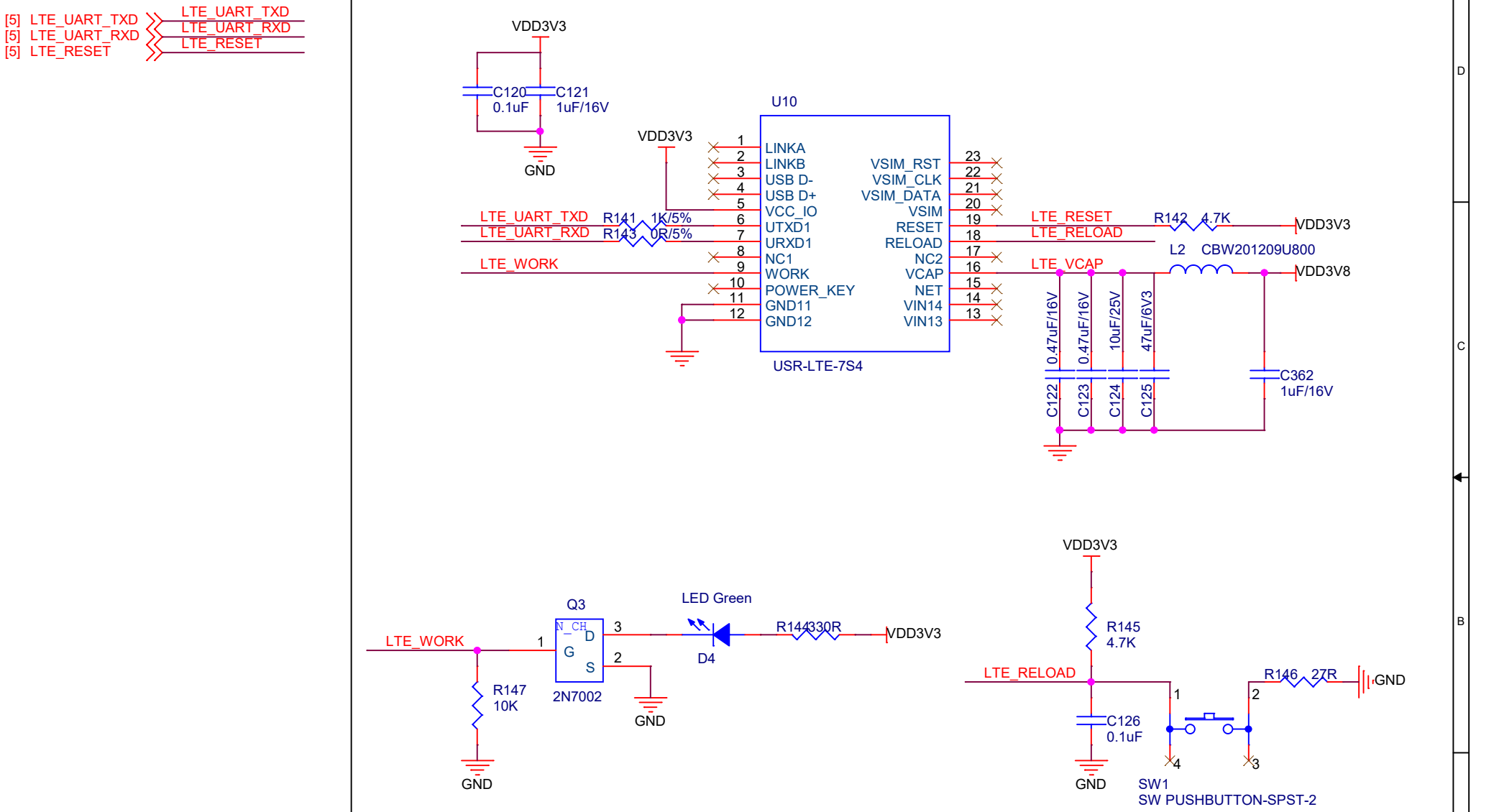

Title	<Title>	
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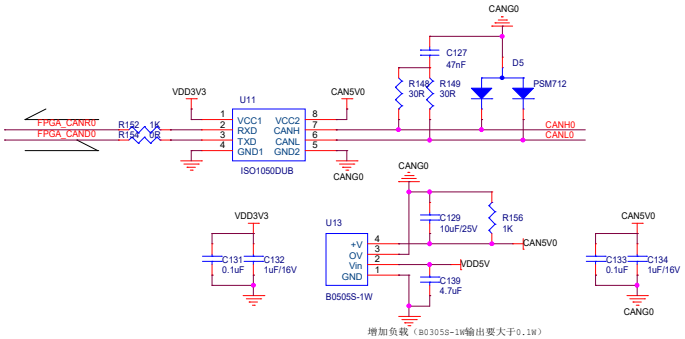
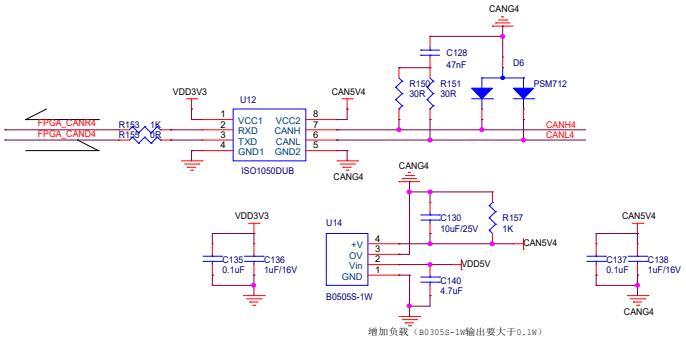
[10] FPGA_CANR[7:0] FPGA_CANR[7:0]

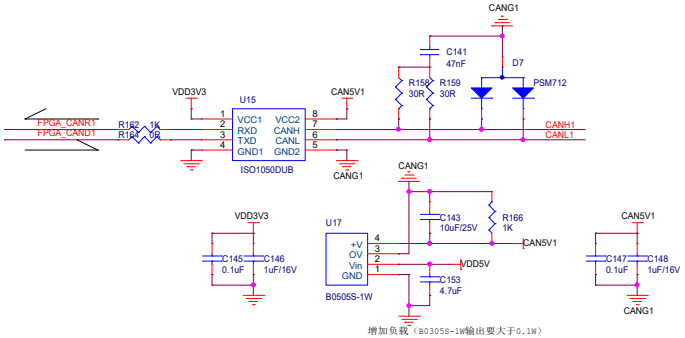
[10] FPGA_CAND[7:0] FPGA_CAND[7:0]

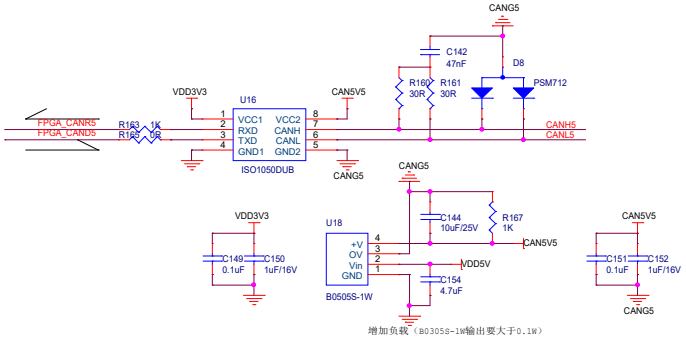
[27] CANH[7:0] CANH[7:0]

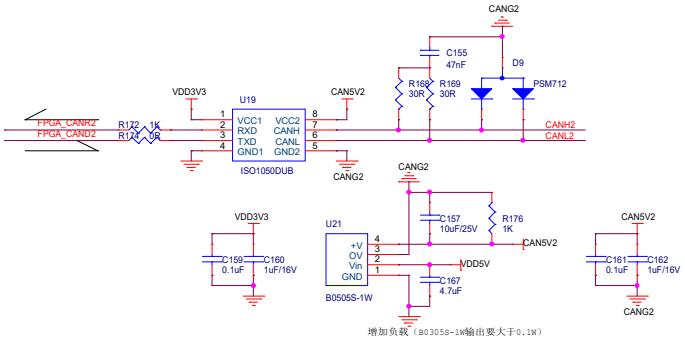
[27] CANL[7:0] CANL[7:0]

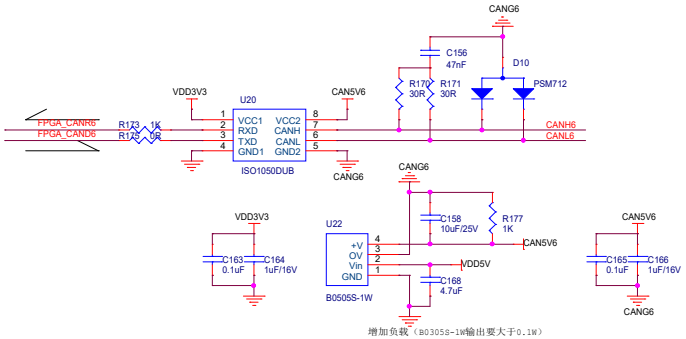


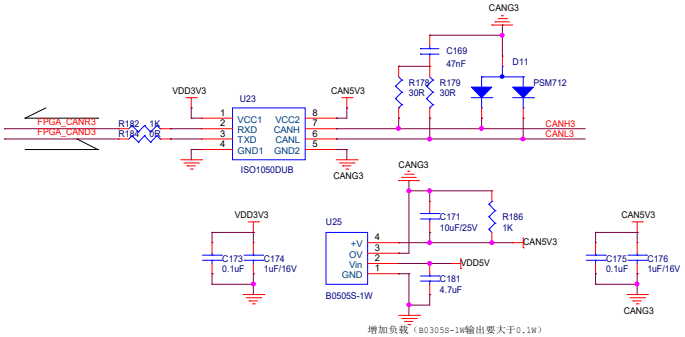


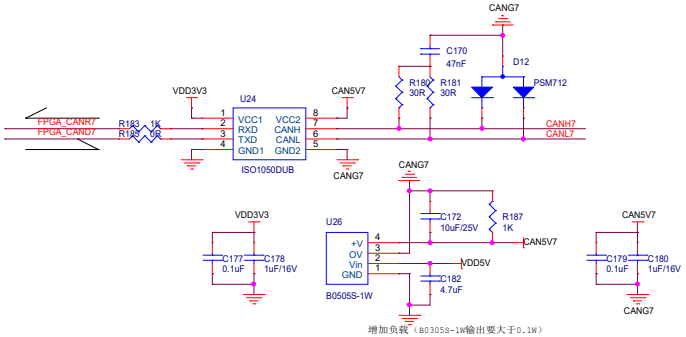












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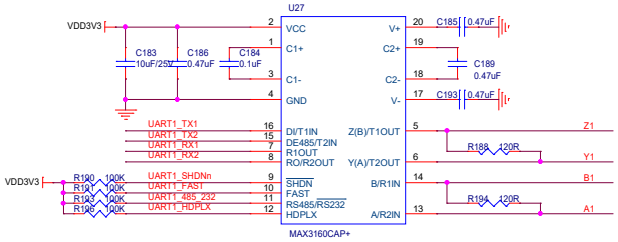
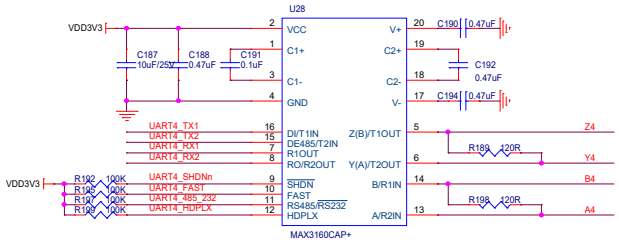
[11] UART1_TX1 — UART1_TX1
[11] UART1_TX2 — UART1_TX2
[11] UART2_TX1 — UART2_TX1
[11] UART2_TX2 — UART2_TX2
[11] UART3_TX1 — UART3_TX1
[11] UART3_TX2 — UART3_TX2
[11] UART4_TX1 — UART4_TX1
[11] UART4_TX2 — UART4_TX2
[11] UART5_TX1 — UART5_TX1
[11] UART5_TX2 — UART5_TX2
[11] UART6_TX1 — UART6_TX1
[11] UART6_TX2 — UART6_TX2

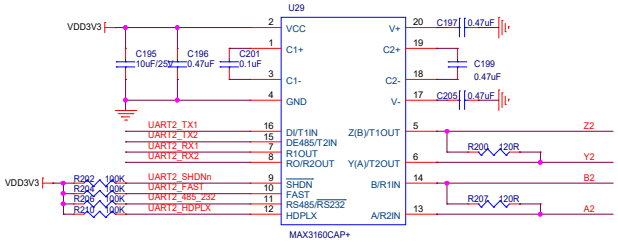
[11] UART1_RX1 — UART1_RX1
[11] UART1_RX2 — UART1_RX2
[11] UART2_RX1 — UART2_RX1
[11] UART2_RX2 — UART2_RX2
[11] UART3_RX1 — UART3_RX1
[11] UART3_RX2 — UART3_RX2
[11] UART4_RX1 — UART4_RX1
[11] UART4_RX2 — UART4_RX2
[11] UART5_RX1 — UART5_RX1
[11] UART5_RX2 — UART5_RX2
[11] UART6_RX1 — UART6_RX1
[11] UART6_RX2 — UART6_RX2

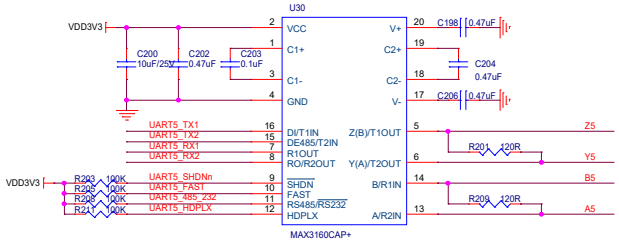
[11] UART1_485_232 — UART1_485_232
[11] UART2_485_232 — UART2_485_232
[11] UART3_485_232 — UART3_485_232
[11] UART4_485_232 — UART4_485_232
[11] UART5_485_232 — UART5_485_232
[11] UART6_485_232 — UART6_485_232

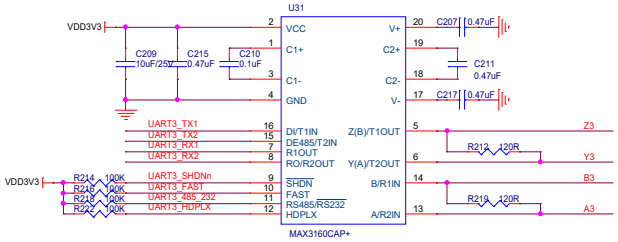
[27] Z[6:1] — Z[6:1]
[27] Y[6:1] — Y[6:1]
[27] B[6:1] — B[6:1]
[27] A[6:1] — A[6:1]

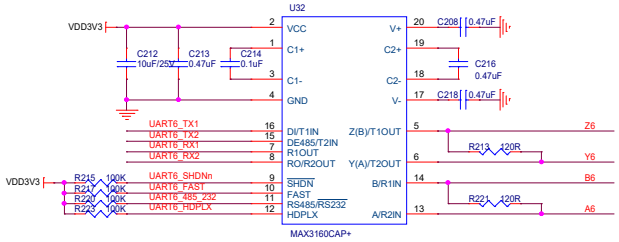












Title: UART		
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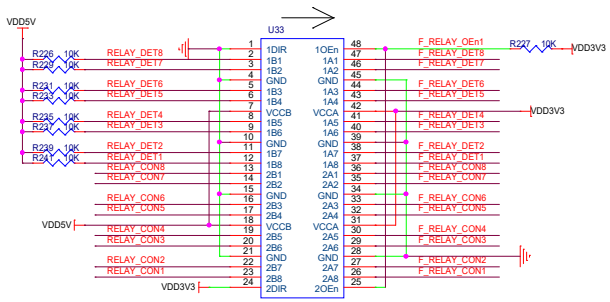
[11] F_RELAY_DET[16:1] → F_RELAY_DET[16:1]

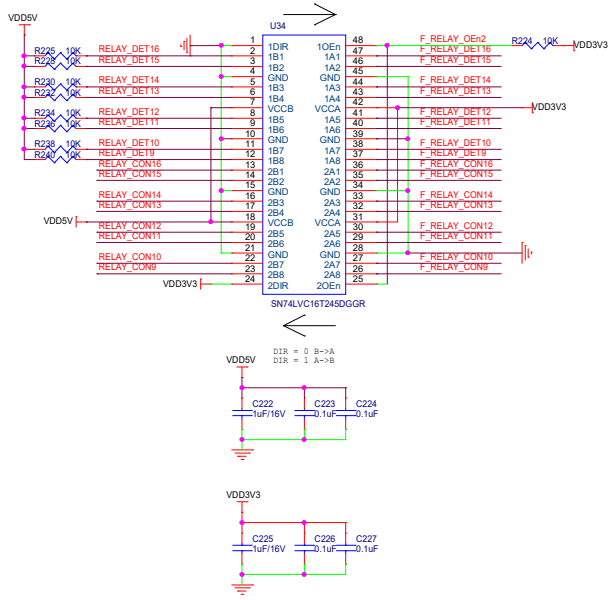
[11] F_RELAY_CON[16:1] → F_RELAY_CON[16:1]

[11] F_RELAY_OEn[2:1] → F_RELAY_OEn[2:1]

[27] RELAY_CON[16:1] → RELAY_CON[16:1]

[27] RELAY_DET[16:1] → RELAY_DET[16:1]





Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
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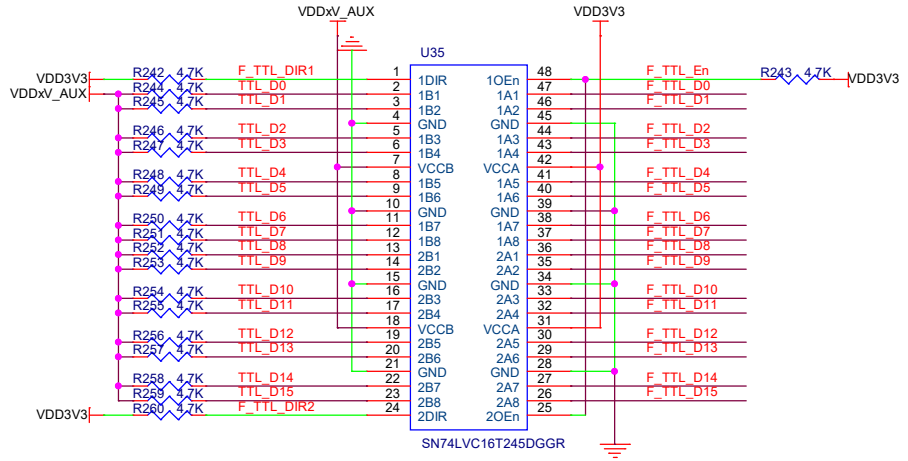
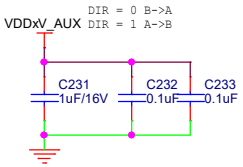
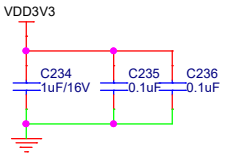
[11] F_TTL_D[15:0] → F_TTL_D[15:0]

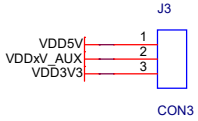
[11] F_TTL_DIR1 → F_TTL_DIR1
[11] F_TTL_DIR2 → F_TTL_DIR2
[11] F_TTL_En → F_TTL_En

[27] TTL_D[15:0] → TTL_D[15:0]









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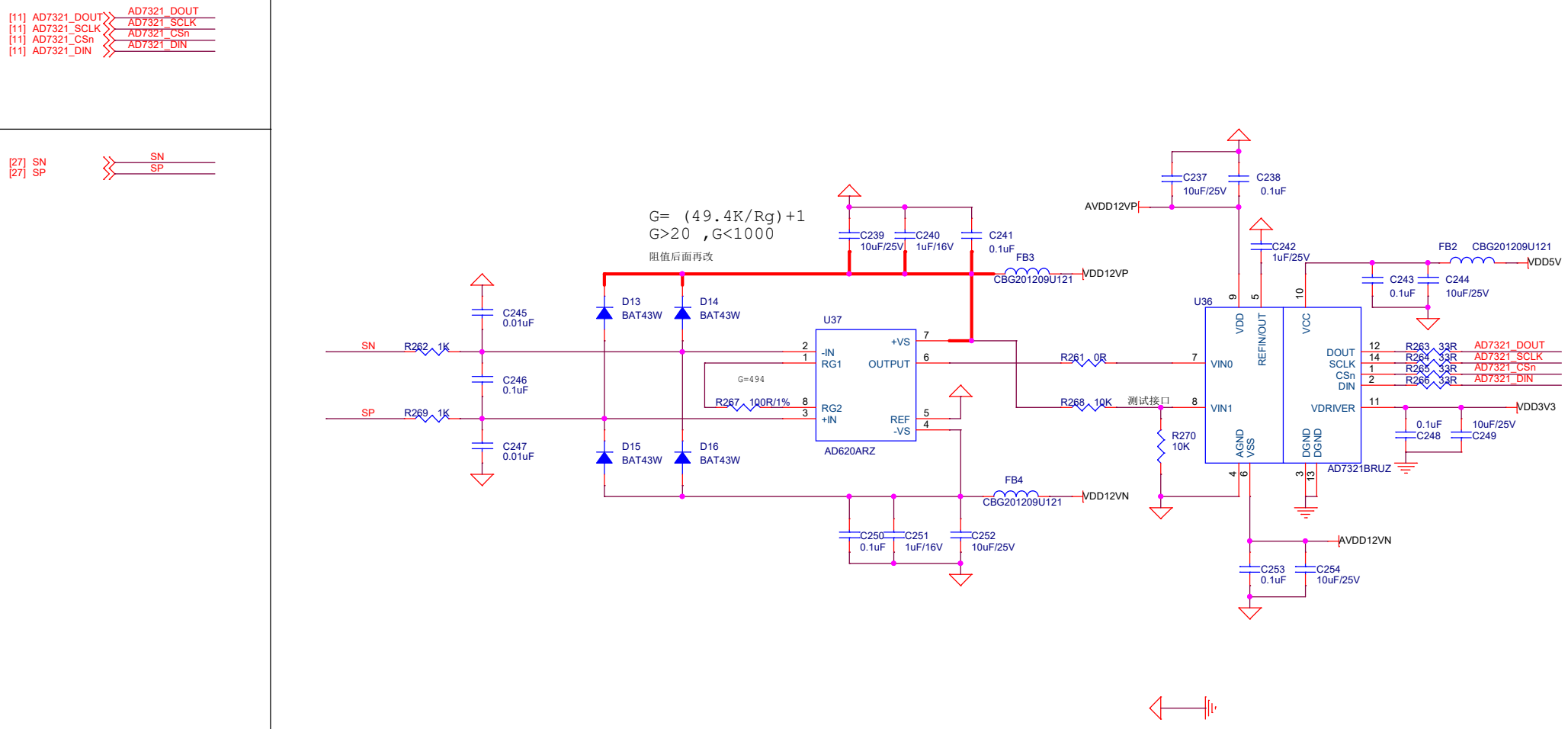
[11] AD7321_DOUT
[11] AD7321_SCLK
[11] AD7321_CSn
[11] AD7321_DIN
AD7321_DOUT
AD7321_SCLK
AD7321_CSn
AD7321_DIN
[27] SN
[27] SP
SN
SP
G= (49.4K/Rg)+1
G>20 ,G<1000
阻值后面再改
C239 10uF/25V
C240 1uF/16V
C241 0.1uF
FB3
CBG201209U121
VDD12VP
C245 0.01uF
C246 0.1uF
C247 0.01uF
D13 BAT43W
D14 BAT43W
D15 BAT43W
D16 BAT43W
U37
SN
SP
R262 1K
R269 1K
R267 100R/1%
G=494
-IN
RG1
RG2
+IN
+VS
OUTPUT
REF
-VS
AD620ARZ
R261 0R
R268 10K
测试接口
R270 10K
FB4
CBG201209U121
VDD12VN
C250 0.1uF
C251 1uF/16V
C252 10uF/25V
AVDD12VP
C237 10uF/25V
C238 0.1uF
C242 1uF/25V
U36
VDD
REFIN/OUT
VCC
VIN0
VIN1
AGND
VSS
DGND
DGND
VDRIVER
DOUT
SCLK
CSn
DIN
AD7321BRUZ
FB2
CBG201209U121
VDD5V
C243 0.1uF
C244 10uF/25V
R263 33R
R264 33R
R265 33R
R266 33R
AD7321_DOUT
AD7321_SCLK
AD7321_CSn
AD7321_DIN
VDD3V3
C248 0.1uF
C249 10uF/25V
AVDD12VN
C253 0.1uF
C254 10uF/25V
Title
<Title>
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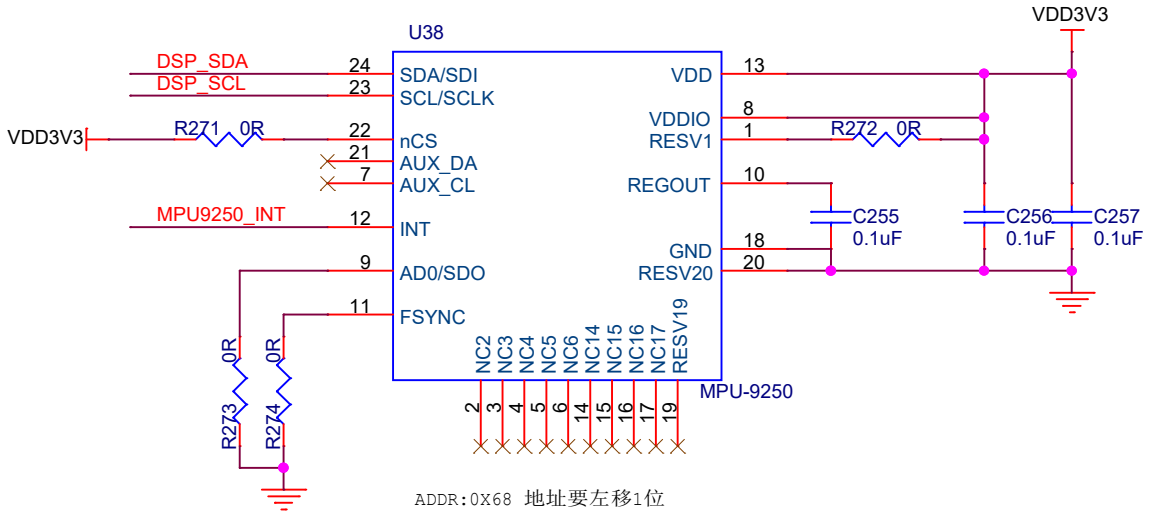
[5,15] DSP_SDA
[5,15] DSP_SCL
DSP_SDA
DSP_SCL

[5] MPU9250_INT
MPU9250_INT



ADDR:0X68 地址要左移1位

Title	陀螺，加速度	
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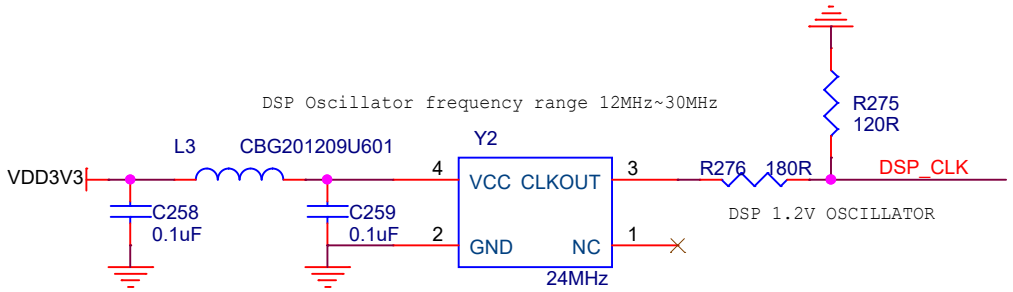
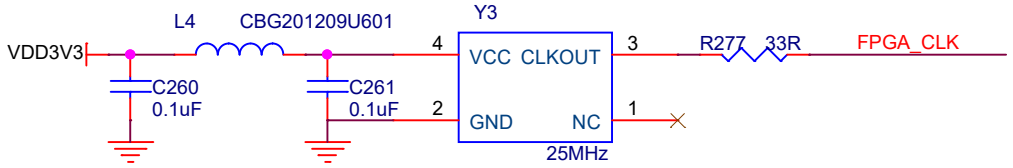
[3] DSP_RESETn >> DSP_RESETn

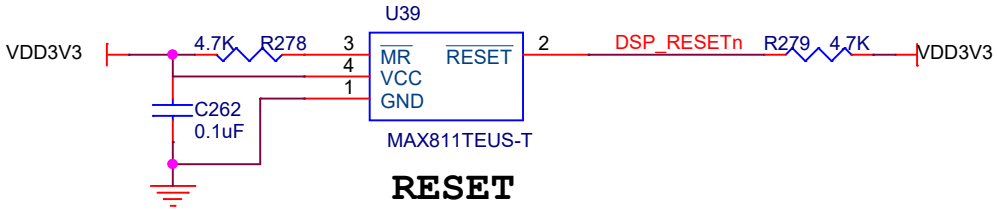
[3] DSP_CLK >> DSP_CLK

[10] FPGA_CLK >> FPGA_CLK





使用两个时钟方便更改为不同的频率



2018-10-24 CHECK OK

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Size A	Document Number <Doc>	Rev <RevCode>
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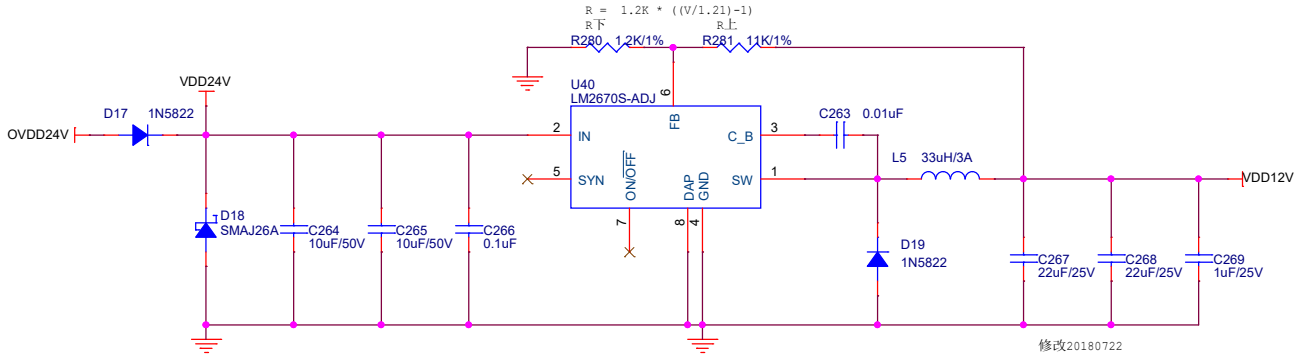

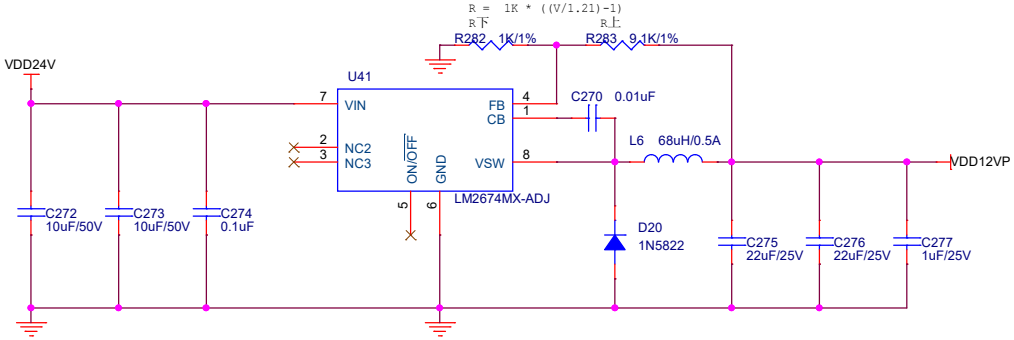

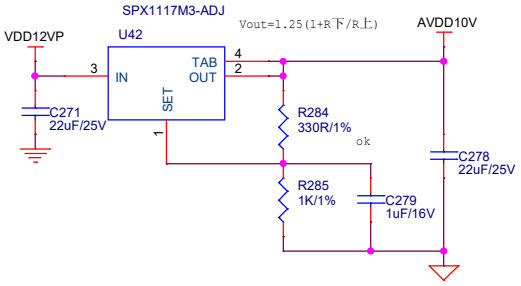

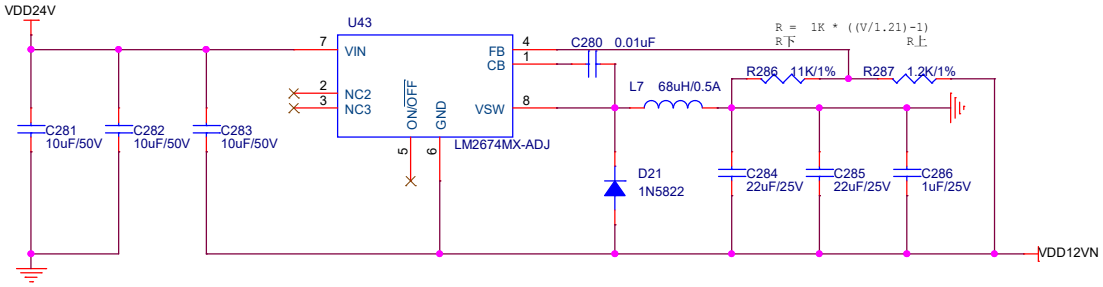

Title	<Title>	
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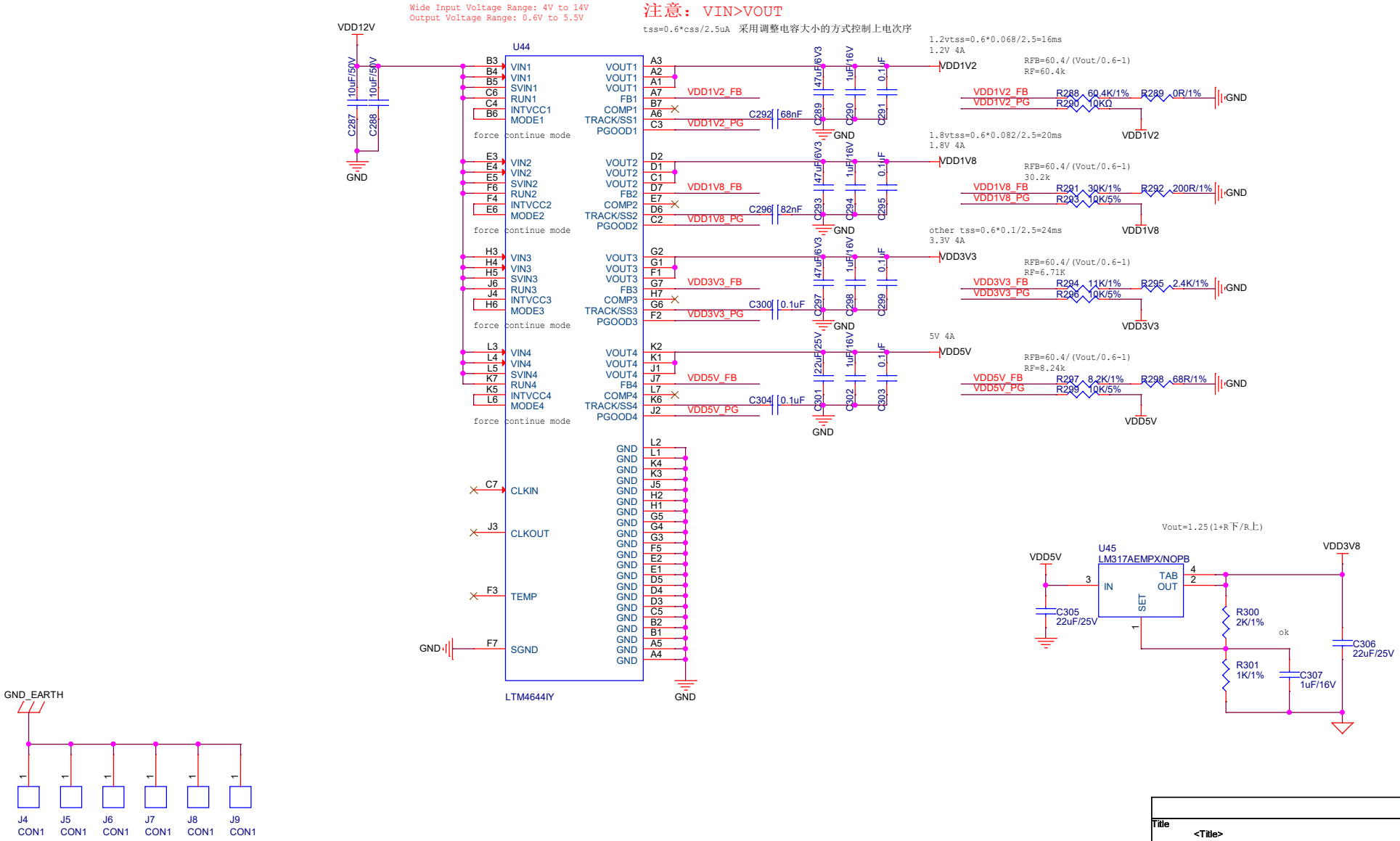

Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
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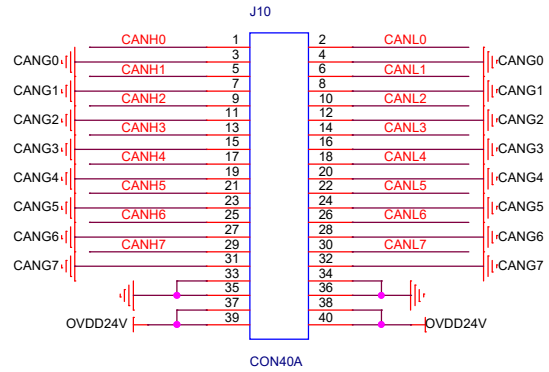
[18] CANH[7:0] CANH[7:0]
[18] CANL[7:0] CANL[7:0]

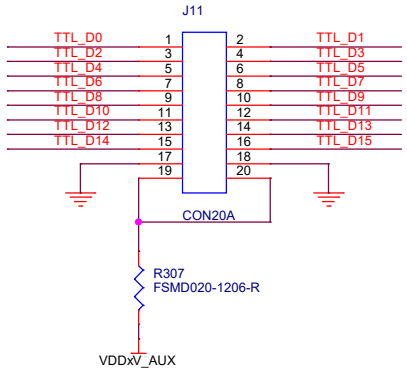
[19] Z[6:1] Z[6:1]
[19] Y[6:1] Y[6:1]
[19] B[6:1] B[6:1]
[19] A[6:1] A[6:1]

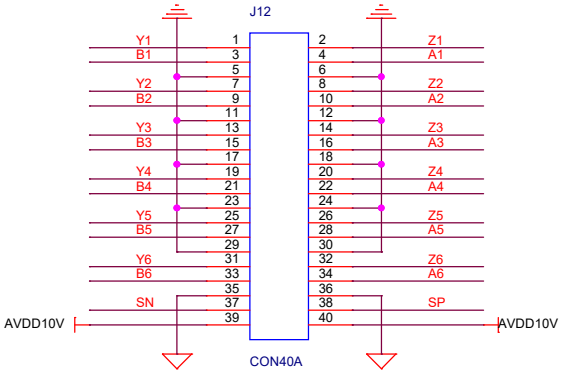
[20] RELAY_CON[16:1] RELAY_CON[16:1]
[20] RELAY_DET[16:1] RELAY_DET[16:1]

[22] SN SN
[22] SP SP

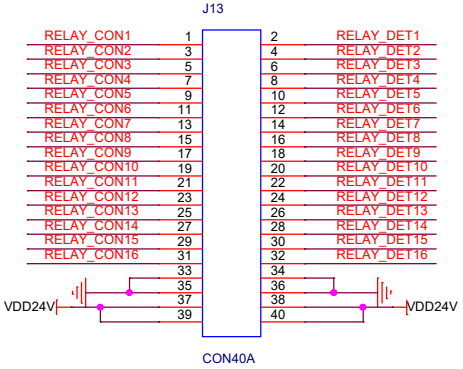
[21] TTL_D[15:0] TTL_D[15:0]







AVDD10V供力传感器



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