流水线设计

寄存器设计

IF/ID寄存器设计：

|  |  |  |  |
| --- | --- | --- | --- |
| 属性 | 寄存器 | 寄存内容 | 备注 |
| 数据通路 | IF\_ID\_PC\_plus\_4 | PC\_plus\_4[31:0] |  |
|  | IF\_ID\_Instruction | Mux6\_out [31:0] |  |
| 接收控制 | / | Stall |  |

ID/EX寄存器设计：

|  |  |  |  |
| --- | --- | --- | --- |
| 属性 | 寄存器 | 寄存内容 | 备注 |
| 数据通路 | ID\_EX\_PC\_plus\_4 | IF\_ID\_PC\_plus\_4[31:0] | jal-wb |
| ID\_EX\_shamt | IF\_ID\_Instruction[10:6] | Shamt(sll) |
| ID\_EX\_Databus1 | Databus1[31:0] |  |
| ID\_EX\_Databus2 | Databus2[31:0] |  |
| ID\_EX\_ LU\_out | LU\_out[31:0] |  |
| ID\_EX\_rt | IF\_ID\_Instruction[20:16] | rt |
| ID\_EX\_rd | IF\_ID\_Instruction[15:11] | Rd |
| ID\_EX\_rs | IF\_ID\_Instruction[25:21] | rs |
| ID\_EX\_funct | IF\_ID\_Instruction[5:0] |  |
| 控制信号 | ID\_EX\_RegDst | RegDst[1:0] |  |
| ID\_EX\_ALUSrc1 | ALUSrc1 |  |
| ID\_EX\_ALUSrc2 | ALUSrc2 |  |
| ID\_EX\_ALUOp | ALUOp[3:0] |  |
| ID\_EX\_MemRead | MemRead |  |
| ID\_EX\_MemWrite | MemWrite |  |
| ID\_EX\_MemtoReg | MemtoReg[1:0] |  |
| ID\_EX\_RegWrite | RegWrite |  |

EX/MEM寄存器设计：

|  |  |  |  |
| --- | --- | --- | --- |
| 属性 | 寄存器 | 寄存内容 | 备注 |
| 数据通路 | EX\_MEM\_ PC\_plus\_4 | ID\_EX\_PC\_plus\_4[31:0] | jal-wb |
| EX\_MEM\_ALU\_out | ALU\_out[31:0] |  |
| EX\_MEM\_mux1\_out | Mux1\_out[31:0] |  |
| EX\_MEM\_mux2\_out | Mux2\_out[4:0] |  |
| 控制信号 | EX\_MEM\_MemRead | ID\_EX\_MemRead |  |
| EX\_MEM\_MemWrite | ID\_EX\_MemWrite |  |
| EX\_MEM\_MemtoReg | ID\_EX\_MemtoReg[1:0] |  |
| EX\_MEM\_RegWrite | ID\_EX\_RegWrite |  |

MEM/WB寄存器设计：

|  |  |  |  |
| --- | --- | --- | --- |
| 属性 | 寄存器 | 寄存内容 | 备注 |
| 数据通路 | MEM\_WB\_ PC\_plus\_4 | EX\_MEM\_PC\_plus\_4[31:0] | jal-wb |
| MEM\_WB\_Read\_data | Read\_data[31:0] |  |
| MEM\_WB\_ALU\_out | EX\_MEM\_ALU\_out[31:0] |  |
| MEM\_WB\_mux2\_out | EX\_MEM\_Mux2\_out[4:0] |  |
| 控制信号 | MEM\_WB\_MemtoReg | EX\_MEM\_MemtoReg[1:0] |  |
| MEM\_WB\_RegWrite | EX\_MEM\_RegWrite |  |

关键模块设计

ForwardUnit for R-beq设计：

|  |  |
| --- | --- |
| 输入 | Branch |
| EX\_MEM\_Mux2\_out[4:0] |
| Instruction[20:16](rt) |
| Instruction[20:16](rs) |
|  | EX\_MEM\_MemRead |
|  |  |
| 输出  (两个共两位控制信号) | mux3\_control[1:0] |
| mux4\_control[1:0] |

ForwardUnit for load-use设计：

|  |  |
| --- | --- |
| 输入 | EX/MEM\_RegWrite |
| MEM\_WB\_RegWrite |
| EX\_MEM\_Mux2\_out[4:0] |
| MEM\_WB\_Mux2\_out[4:0] |
| ID\_EX\_rs[4:0] |
| ID\_EX\_rt[4:0] |
| 输出  (两个共四位控制信号) | Mux1\_control[1:0] |
| Mux5\_control[1:0] |

Hazardunit设计

|  |  |
| --- | --- |
| 输入 | And\_out |
| PCSrc[1:0] |
| ID\_EX\_MemRead |
| Mux2\_out[4:0] |
| Instruction[25:21](rs) |
|  | Instruction[20:16](rt) |
| 输出  (两个共四位控制信号) | Stall(三处分发) |
| IF\_Flush |

PC接受一控制信号:若stall为1则保持原值不变

EX阶段的两个mux

ID阶段的三个mux和一个compare

If阶段的一个mux

关键路径设计

Jr

Jal

Ppt流水线的几处修改

Jr

Jal

Lui

Shamt（sll）和pc+4（jal）的传递

Lw+其他+beq指令的转发判断

先写后读——negedge