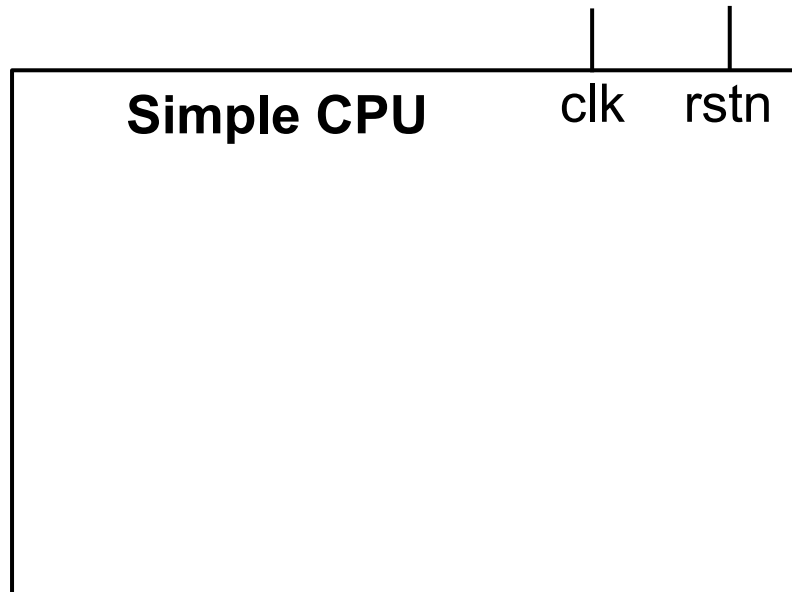


Place MUXs  
as you like

You should add wires to this diagram to complete the project

# Ports



- Input
  - clk : clock input
  - rstn : for resetting the cpu

# Ports



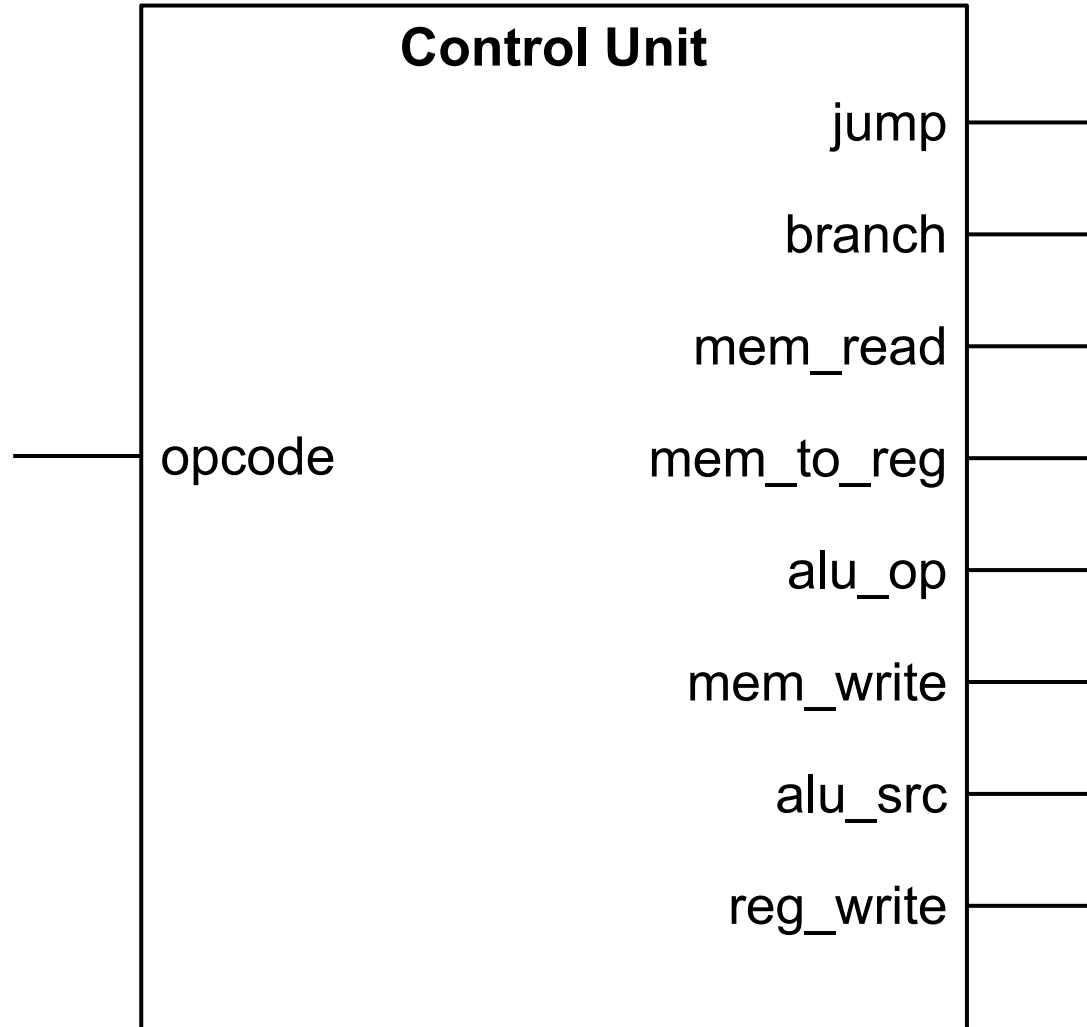
- Input
  - PC (32b) : address of instruction
- Output
  - instruction (32b) : instruction for current PC

# Ports



- Input
  - instruction (32b): instruction
- Output
  - sextimm (32b): sign-extended immediate

# Ports



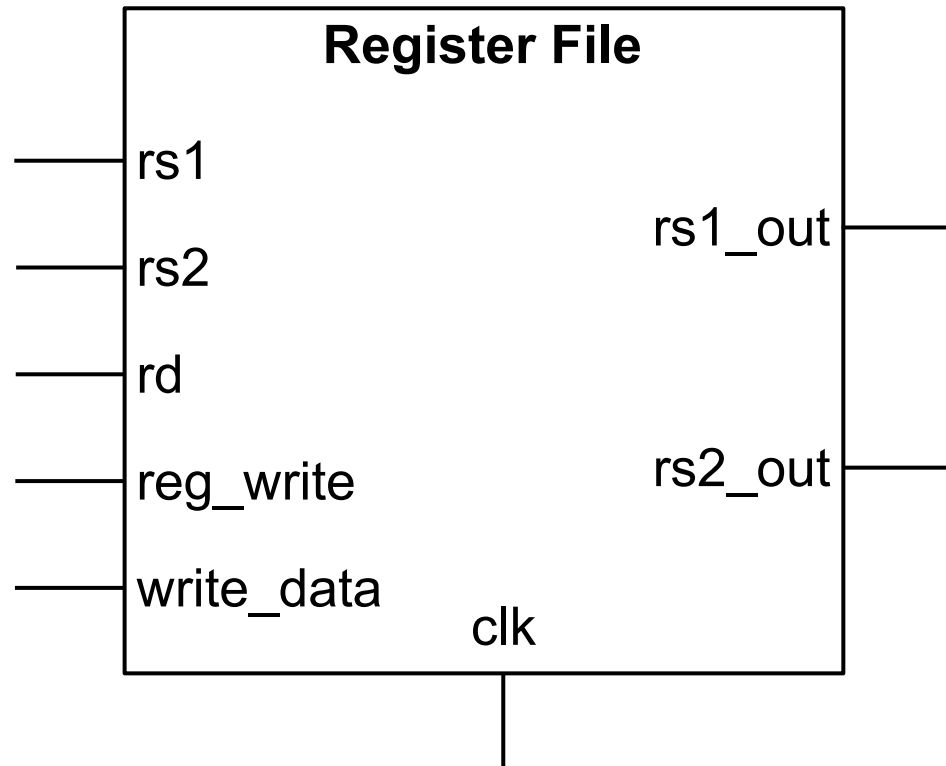
- **Input**

- opcode (7b) : opcode from instruction

- **Output**

- jump (2b) : indicates if this inst is “jal” or “jalr”
- branch (1b) : indicates if this inst is a branch type
- mem\_read (1b) : indicates whether to read from memory
- mem\_to\_reg (1b)
  - 0 : writeback source is from ALU
  - 1 : writeback source is from memory
- alu\_op (2b) : control signal sent to ALU control
- mem\_write (1b) : indicates whether to write to memory
- alu\_src (1b)
  - 0 : in\_b of ALU is from the register file
  - 1 : in\_b of ALU is from the immediate generator
- reg\_write (1b) : indicates whether to perform writeback to the register file

# Ports



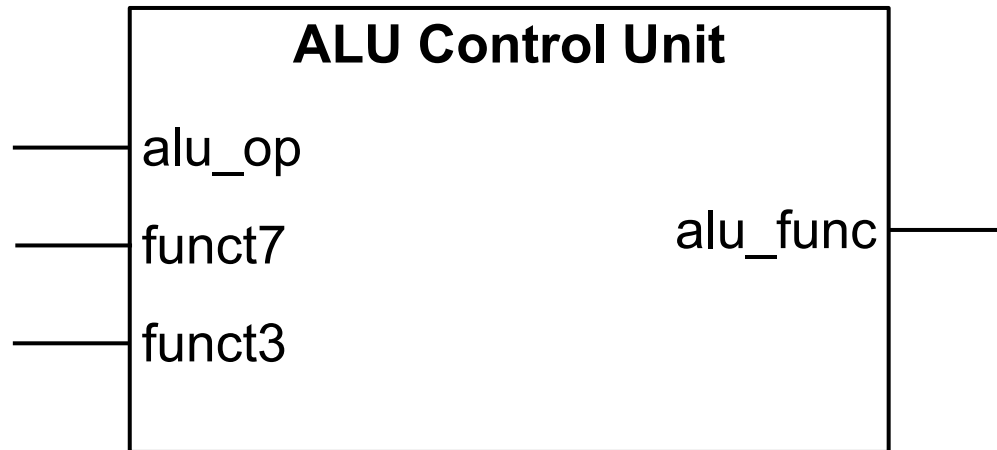
- Input

- rs1 (5b) : source 1 register file index
- rs2 (5b) : source 2 register file index
- rd (5b) : destination register file index
- reg\_write (1b)
  - 0 : do not write write\_data to register file
  - 1 : update rd with write\_data
- write\_data (32b) : data which will be written to the register file

- Output

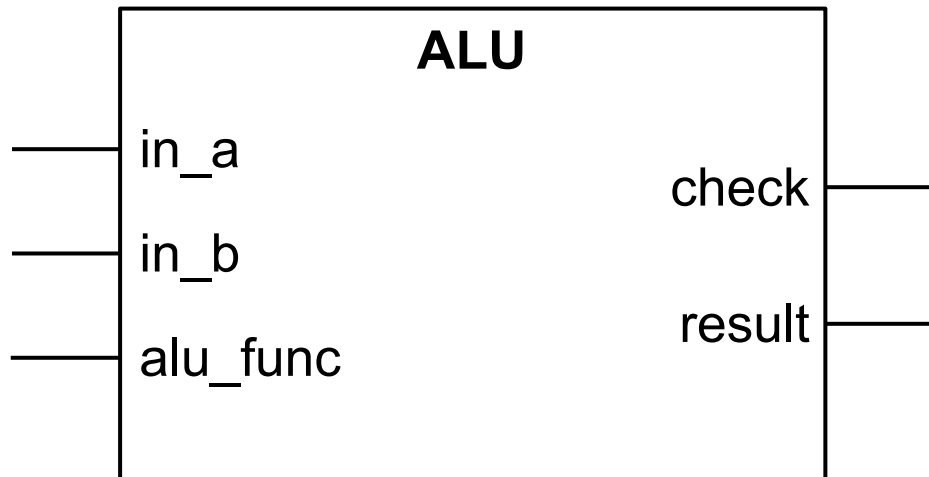
- rs1\_out (32b) : data from rs1
- rs2\_out (32b) : data from rs2

# Ports



- Input
  - alu\_op (2b) : from control unit
    - ▶ 00 : select operation for loads/stores
    - ▶ 01 : select operation for branches
    - ▶ 10 : select operation for R types
    - ▶ 11 : select operation for I types
  - funct7 (7b) : from instruction
  - funct3 (3b) : from instruction
- Output
  - alu\_func (4b) : ALU operation control signals

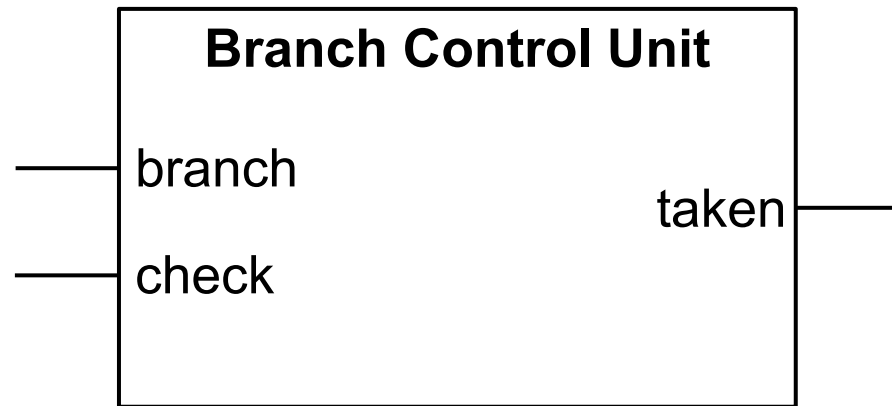
# Ports



- Input
  - in\_a (32b) : ALU source operand
  - in\_b (32b) : ALU source operand
  - alu\_func (4b) : specifies which operation the ALU should execute
- Output
  - result (32b) : ALU operation result
  - check (1b) : check flag for branches

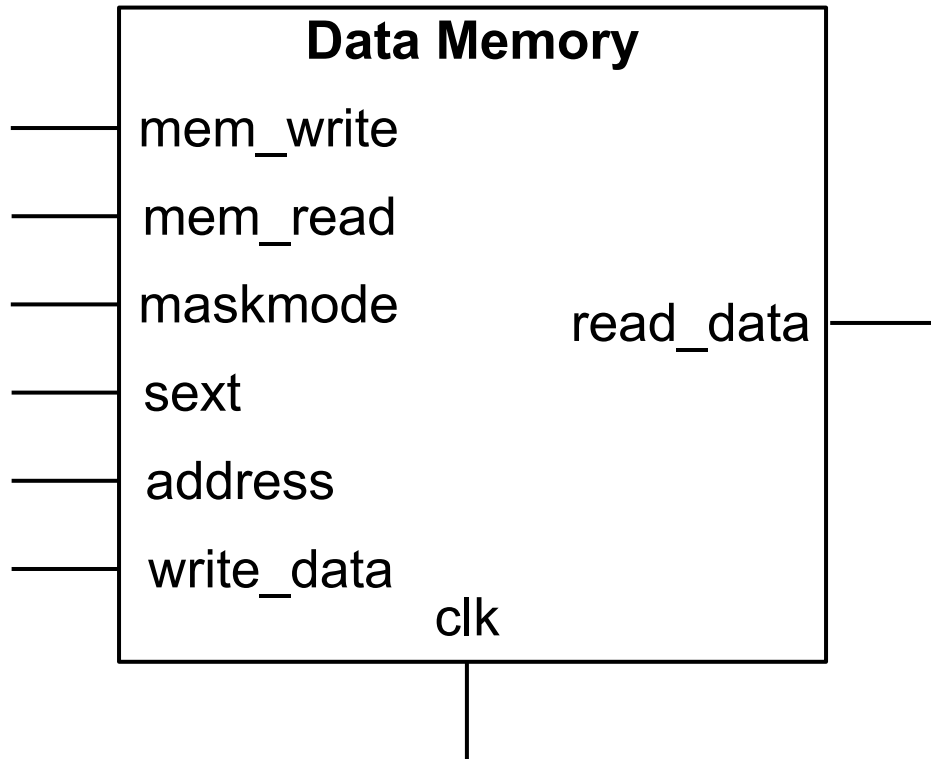


# Ports



- Input
  - branch (1b) : instruction is a branch type or not
  - check (1b) : output from ALU
- Output
  - taken (1b) : set to 1 if branch is taken

# Ports



- Input
  - address (32b) : memory address
  - write\_data (32b) : data which will be written
  - mem\_read (1b) : indicates whether to read from memory
  - mem\_write (1b) : indicates whether to write to memory
  - maskmode (2b)
    - 0 : byte
    - 1 : half-word
    - 2 : word
  - sext (1b)
    - 0 : output read\_data as sign extend
    - 1 : output read\_data as unsigned (zero extend)
- Output
  - read\_data (32b) : data read from the memory