Component Specification

This **component specification** in conjunction with **following specifications** listed below is the supply specification. If there are differences between these specifications, the component specification has higher priority.

Quality Grade:	1
Type:	ATIC116
Device:	*Rotational speed and position sensor*
Package Outline:	*SSOP16 medium*
Operating Temperature Range:	*-40°C to +140°C*
Shipment:	Tape and reel (IEC 68286 Part 3)
Lead Finish:	*pure SN*

SUPPLIER's FIELD: MANDATORY FOR THE SUPPLIER TO FILL OUT:

❍ accepted with Vendor Addendum ❍ accepted without Vendor Addendum

Supplier Name .....

Signature(s) by Supplier .....

Date / Name / Position .....
(in printed letters)

Ordering code .....

Component Name .....

Component Family .....

Manufacturing Plant (frontend) .....

(backend) .....

Manufacturing Technology .....

Humidity Class (IPC/JEDEC J-STD-020) .....
(Shipment with drypack is necessary for moisture sensitivity level > 2)

Document version	Previous version	Change description (including number)
Rev A		

Designed by: Author: O. Zappa/ S. Haimerl	Date: 03/12/2009	Department: S&T A IC
Released by: Author	Date	Department

Continental

Designation
ATIC116
Rotational speed and position sensor

Status

Documentkey
A2C00046207

Pages
1 of 162

 A4 : 2002-03

General Requirements

This component specification in conjunction with the following specifications (last mutual agreed version including possible Vendor Addenda) is the supply specification.

A2C00053611AAA	General Quality Agreement for Automotive Suppliers
A2C00052909AAA	Category Quality Requirements (CQR) for Semiconductors
A2C00052908AAA	Quality Process Requirements (QPR) for EMC
A2C00052905AAA	Quality Process Requirements (QPR) for Process Change Notifications (PCN) of purchased components

If there are differences between these specifications, the ATIC116 component specification has higher priority.

TABLE OF CONTENTS

1 GENERAL

1.1 QUALITY AND RELIABILITY

Quality	Goal: 0 ppm
Service Life	19 years (standby at 40°C) 300,000 km 9,000 hours Test cycles are still to be determined No special aging effects that lead to absolute undefined or safety-critical values are allowed to arise during the service life.

Note:

Following devices are not taken into account while calculating the fault rate:

- Faults due to damages during processes following the production and test are under control of the supplier.
- E.g. :
  - Electrical overstress such as ESD, voltage or current overstress exceeding the product specifications
  - Excessive mechanical or thermal shocks.

For qualification, the Category Quality Requirements (CQR) for Semiconductors (A2C00052909AAA) is valid.

The following tests are specifically required for ATIC116.

1.2 SERIES TEST

1.2.1 IDDQ TEST

All blocks of ATIC116 on wafer and on package level. Applicable, to be defined by the supplier and agreed by Continental.

1.2.2 PART AVERAGE TEST

Applicable, to be defined by supplier and agreed by Continental.

Preferred is the 'Dynamic part average test' as defined in the AEC-Q100.

1.3 LIFETEST CONDITIONS

The life test during qualification procedure (HTOL) will be provided with test loads, according to application needs. Supplier and Continental define the exact schematic and dynamic operating conditions together (life test boards and stimuli). Duration of the HTOL test is defined for 1500h at a junction temperature of 150°C.

1.4 TEMPERATURE PROFILE OF TYPICAL APPLICATION

	T_{AMB} [°C]	Duration [h]
Operation	-40 …-25	80
	40	1440
	80	1800
	90	3604
	100	1700
	105	120
	110	80
	115	80
	140	96
Standby time	35	157440
Total operating time		**13000**

Table 1: Typical temperature profile

Remark: Standby time means operation in chop-mode: -> additional ~4000h operating time

1.5 RAMP – UP MONITORING

3-Temperature test and burn-in requirements are described in the Category Quality Requirements (CQR) for Semiconductors (A2C00052909AAA).

Minimum first 100kpcs, 48hrs (burn-in duration can be reduced, if the supplier is able to prove that a lower duration is sufficient).

Exit criteria for burn-in: Zero reject with respect to burn-in.

1.6 DYNAMIC BURN-IN

Supplier and Continental define the exact schematic and dynamic operating conditions for burn-in together.

1.7 FMEA / FTA

The safety analysis methods FMEA and FTA according to ISO IEC1025 and IEC812 shall be performed at lowest component level, when necessary (supplier/ Continental agreement). It must be worked out in parallel to the design itself and has to be finalized for the final design review.
For the FMEA, results have to be provided with the help of IQ-FMEA V4.0 software, or ISO compatible format.
For the FTA, the analysis must include fit rate for each branch and elements.
Design FMEA is required.

1.8 TEST COVERAGE

Refer to the Category Quality Requirements (CQR) for Semiconductors (A2C00052909AAA).

All electrical parameters have to be tested, if not otherwise specified (for example, use of scan path methodology).

1.9 TESTABILITY REQUIREMENTS

For test requirements, refer to Category Quality Requirements (CQR) for Semiconductors (A2C00052909AAA).

1.10 TRACEABILITY

Traceability has to be provided by the supplier, see General Quality Agreement (A2C00053611) .

1.11 PACKAGING FOR SHIPMENT

The shipment must be according to IPC/JEDEC J-STD-033. The components must be delivered in ESD protected blister belts in dry package for packaged devices if MSL=3. Ship-to-stock delivery with Quality Assurance agreement is required.

1.12 EARLY QUALIFICATION TESTS WITH B1 SILICON

Full approach:

The Pre-Qualification has to be considered as reliability pre-assessment.
The ATIC116 pre-qualification plan will include the following tests:

1.	ESD/latch up; latch up will be performed at hot (140 degrees C)	(m)
2.	CPK characterization for 3 temperatures	(m)
3.	HTOL (incl. preconditioning): 3 lots (77 pieces) at 150 degrees C for 1500 hrs.	(m)
4.	Temperature cycling: 500 times -65 degrees C to 150 degrees C	(m)
5.	Unbiased HAST: 96 hrs; 130 degrees C; 85% RH	(o)
6.	Biased humidity (THB) 1000 hrs	(m)
7.	HT storage (3 lots; 15 devices): 150 degrees C; 1000 hrs	(o)

(m): mandatory
(o): optional

Concerning the test itself:

- ATE before the stress
- then pre qualification test(s)
- ATE at the end.

- ATE testing is performed with the test program (test coverage).
- It is recommended to perform the statistical analysis during the pre-qualification with the ATE as it is specified.

1.13 VOLTAGES

In the table below an overview of the most important ASIC voltages and their symbols is shown

Symbol	Function	Comment
VDD	Supply voltage, ASIC	Supplied to the ASIC from an outside source
3V3A	Supply voltage, analog part	Generated on-chip; Used in active mode
AVss	Analog GND	Generated on-chip; Used in active mode
3V3D	Supply voltage, digital part	Generated on-chip; Used in active mode
DVss	Digital GND	Generated on-chip; Used in active mode
MR+	Supply voltage, MR bridge	Generated on-chip; Used in active mode
MR-	MR bridge GND	Generated on-chip; Used in active mode
OUTMR+	MR bridge output voltage	Output for diagnosis in ECU; Must have the same voltage as MR+ in active mode, no voltage in low-power mode and chopping mode

LPVDD	Low-power supply voltage	Used in low-power mode and chopping mode for analog part and digital part
LPMR+	Supply voltage, MR bridge	Generated on-chip; Used in low-power mode and chopping mode
LPMR-	MR bridge GND	Generated on-chip; Used in low-power mode and chopping mode

Table 2: Voltages and their symbols

1.14 ABBREVIATIONS

In the table below the abbreviations used in this document are shown. Please note: the corresponding overview of abbreviations regarding SPI communications is given in the chapter on SPI.

Abbreviation	Meaning
AFE	Analog Front End
ATE	Automated Test Equipment
CA	Coefficient of Amplitude
CO	Coefficient of Offset
CP	Compensation Parameters
CRC	Cyclic Redundancy Check
DED	Decrement (for error debouncing)
DNL	Differential Nonlinearity error
DSP	Digital Signal Processing
eppm	electric periods per minute
EPS	Electric Power Steering
EMC	Electro-Magnetic Compatibility
ECU	Electronic Control Unit
ESD	Electrostatic Discharge
EXER	Excentricity Error
FMEA	Failure Mode and Effects Analysis
FTA	Fault Tree Analysis
GAZ	Gain Stage with Auto-Zero
GQAS	General Quality and Approval Standard
HW	Hardware
HP-POR	High Power - Power On Reset
HT	High Temperature (125°C)
HTOL	High Temperature Operating Life
HAST	Highly Accelerated Stress Test
IDDQ	Idd Quiescent (Integrated Circuit Quiescent Current)
INC	Increment (for error debouncing)
INL	Integral Nonlinearity error
LSB	Least Significant Byte (Bit)
LSS	Least Significant Section

LP-POR	Low Power - Power On Reset
LT	Low Temperature (-40°C)
MR sensor	Magnetoresistive sensor
MLX	Melexis
µC	microController
MSB	Most Significant Byte (Bit)
MSS	Most Significant Section
MCM	Multi Chip Module
ppm	parts per million
PLD	Power Loss Detection
CPK	Process Capability Index
PGA	Programmable Gain Array
PWM	Pulse Width Modulation
R&R	Request & Response
RT	Room Temperature (25°C)
rms	root mean squared
rpm	rotations per minute
S&H	Sample & Hold
SPI bus	Serial Peripherial bus
SSOP	Shrink Small-Outline Package
SW	Software
SM	State Machine
S1 - S4	State machine states
TCA	Temperature Coefficient of Amplitude
TCO	Temperature Coefficient of Offset
THB test	Temperature, Humidity, Bias test
THR	Threshold (error debouncing)
VHT	Very High Temperature (140°C)

Table 3: Abbreviations overview

2 MECHANICAL DATA

2.1 DIMENSIONS

The outlines of the *SSOP16* package are shown below.

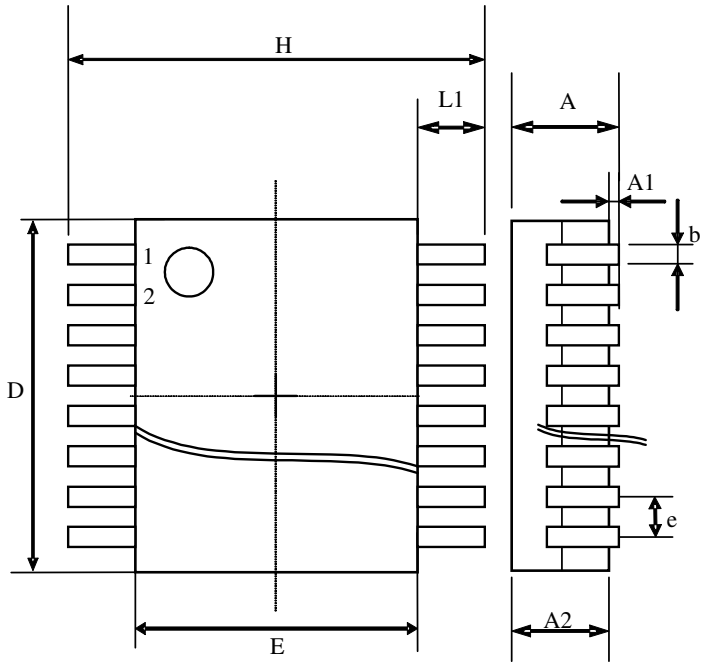


Figure 1: Package drawing

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.25	-	0.38
D	6.07	6.20	6.33
E	5.20	5.30	5.38
H	7.65	7.80	7.90
e	-	0.65	-
L1	0.63	0.75	0.95

Table 4: SSOP16 dimensions

2.2 IDENTIFICATION CODE

a) Packaged parts

Back side: no marking

Top side: Manufacturer number: "MLX 14604"
Revision number and packaging date code (1 week resolution): AAA_yyww
Conti number : ”A2C46207”
Lot number data: xxxxxx

Date Code: yyww: year and week of production

Revision number (AAA): BDC: ATIC116 B3 Version

The marking is shown in the figure below.

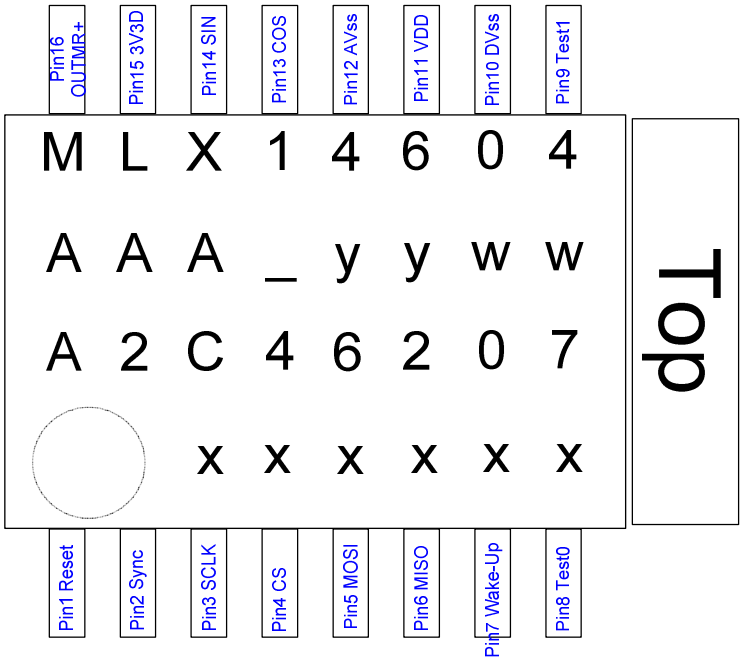


Figure 2: ATIC 116 marking

2.3 MR Bridge Placement in SSOP16 Package

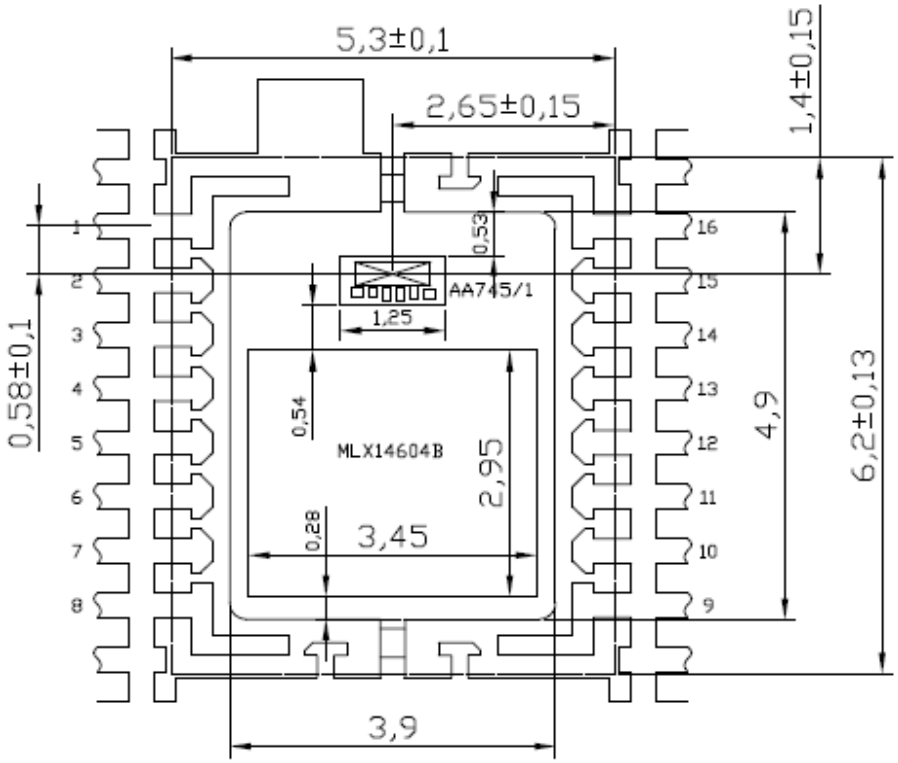
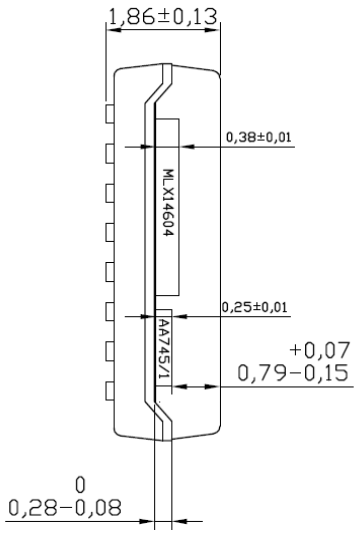


Figure 3: MR Bridge Placement in SSOP16 Package



NOTE:
1. ALL DIMENSIONS ARE IN MM.
2. ROTATION TOLERANCE OF MR SENSOR IS +/-2DEG IN ALL DIRECTIONS.
3. VERTICAL TOLERANCE DEPENDS ON THE DOWNSET OF THE LEADFRAME WHICH STILL HAS TO BE DEFINED.

3 ELECTRICAL CHARACTERISTICS

3.1 System Overview

3.1.1 Purpose of ATIC 116

Most cars are equipped with some kind of a servo-steering mechanism. Such systems are usually hydraulic-based. ATIC 116 will be part of a novel servo-steering system called EPS; in this system the torque necessary to support the driver's steering action will be generated by an electric DC motor. The basic system set-up is shown in the diagram below:

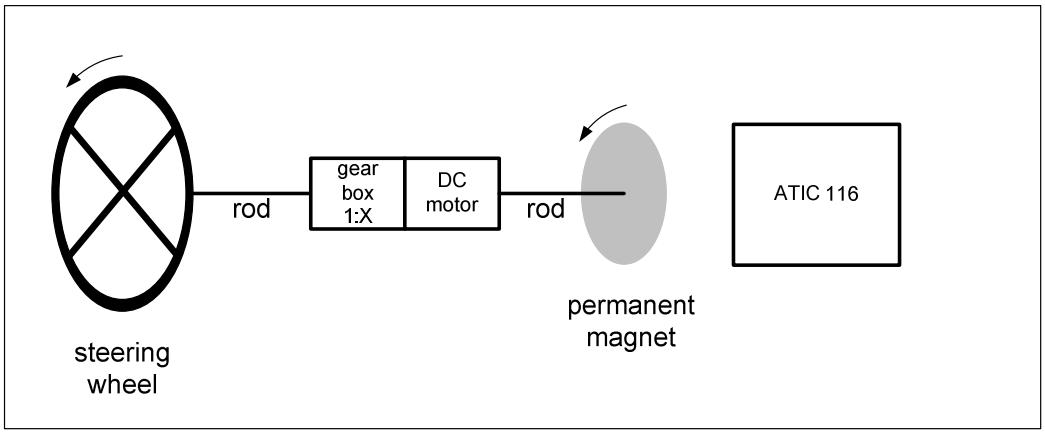


Figure 4: EPS System set-up

The following blocks can be recognized:

1) Steering wheel, rotated by the driver
2) Steering rod
3) Gear box with a transmission ratio of 1:X (for example 1:24)
4) DC motor for the servo-steering mechanism
5) DC motor rod
6) Permanent magnet, rotates in the same direction as the steering wheel but X times faster and generates a rotating magnetic field
7) ATIC 116, measures the magnetic field and converts it into digital outputs

Purpose of ATIC 116

The purpose of the ATIC 116 is to measure: (a) the DC motor' angle (the angle between the rotor and the stator), and (b) the DC motor's angular speed. An additional feature is to count motor rotations.

3.1.2 Measurement Set-up

An example of ATIC 116 measurement set-up can be presented as follows: the ATIC 116 measures the magnetic field using two magnetoresistive bridges (MR bridges) and calculates the motor's angular speed, angle, and number of rotations. These values are then communicated to the master ECU over SPI bus. This ECU, in turn, controls the electric DC motor.

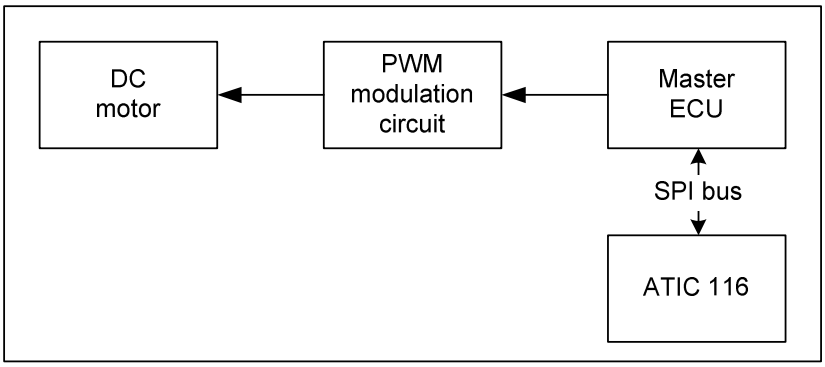


Figure 5: Measurement set-up

The MR bridge and the ASIC will be realized as an MCM (Multi Chip Module) containing two separate dies in one package as shown in the figure below.

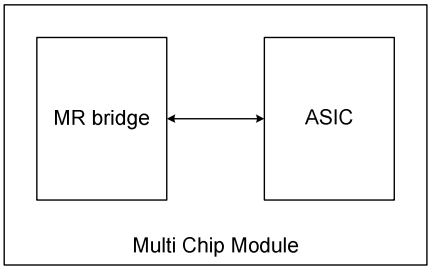


Figure 6: ATIC 116 as Multi Chip Module

ATIC 116

Whenever the term "ATIC 116" is used in this document, it means the Multi Chip Module with:

- MR bridge sensor
- ASIC.

ASIC

Whenever the term "ASIC" will be used in this document, it means the Application-Specific Integrated Circuit for signal generation and processing, without the MR bridge.

3.1.3 MR Bridge

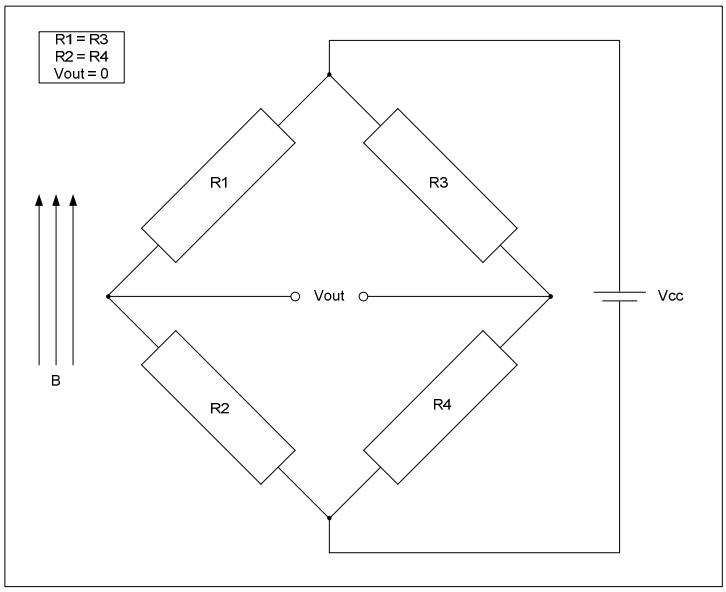


Figure 7: Single MR bridge

In the figure above, an ideal MR (magnetoresistive) bridge can be seen. It consists of 4 identical magneto-resistive elements in a Wheatstone bridge configuration.

The resistivity of an MR element changes with the angle between the element itself and force lines of a magnetic field B: the resistivity is maximal for an angle of 0° (element parallel to B) and minimal for an angle of 90° (element perpendicular to B).

If the direction of the magnetic force lines is like in the above diagram, then all MR elements will have the same resistivity, and the bridge output voltage Vout will be 0 Volts.

If, however, the magnetic field is rotated, then the resistivity of 2 opposite elements will increase, and the resistivity of the other 2 elements will decrease. The resulting un-balance produces a bridge output voltage which is different from 0 Volts.

The bridge output voltage Vout is a function of the rotation angle by which the magnetic force lines have been rotated. This function is shown in the diagram below.

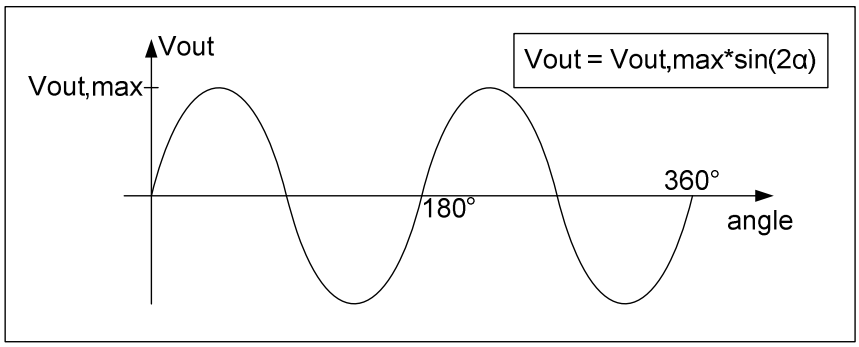


Figure 8: Vout as function of rotation angle

Thus, it is possible to determine the rotation angle within an interval of 0-180° by using the arcsin function, if the amplitude of Vout is known.

This approach has one disadvantage: the sine value of φ=10° is the same as sine value of φ=80°, etc. It means that for each voltage value, two angle values are possible.

This problem can be solved by using a sine/cosine configuration. This configuration, which consists of two separate MR bridges, is shown in the figure below. The bridges are placed at an angle of 45° with respect to each other.

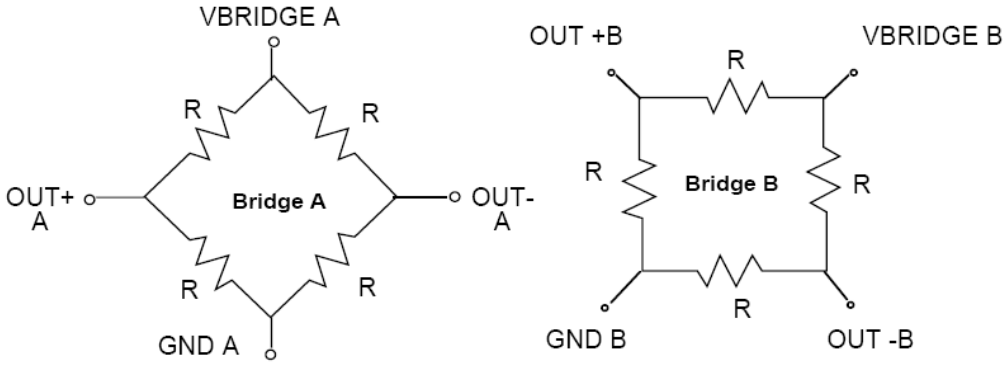


Figure 9: Double MR bridge

The bridge output voltages as function of the rotation angle are shown below. It can be clearly seen that the output voltage of the bridge "A" can be described by sine function, whereas the output voltage of the bridge "B" can be described by cosine function. Hence, these outputs are often referred to as "sine output" and "cosine output".

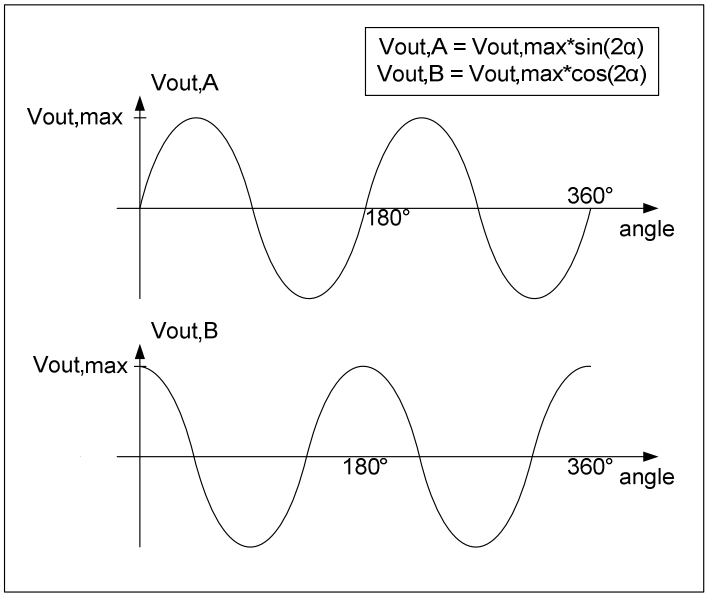


Figure 10: Vout as function of rotation angle (double MR bridge)

NOTE:

From now on, whenever an MR bridge (or MR sensor) is mentioned, it is a double MR bridge with sine and cosine outputs like described above, unless otherwise specified. Sometimes, the MR bridge will also be called "sensor".

Electrical angle and mechanical angle

As can be seen in the diagrams above, there is a ratio of 2 between mechanical rotations of the magnet, and the electric periods of the output signals: for every magnet rotation, there will be two sine and cosine periods.

It must be kept in mind that what is sensed by the "ATIC 116" is not the rotation of the magnet or the steering wheel, but the sine and cosine signals generated by the MR bridge. For that reason, the terms "electrical angle" and "mechanical angle" are introduced.

The electrical angle refers to the sine and cosine signals. Mechanical angle refers to the rotation of the magnet. The relationship between these two angles is visualized in the diagram below.

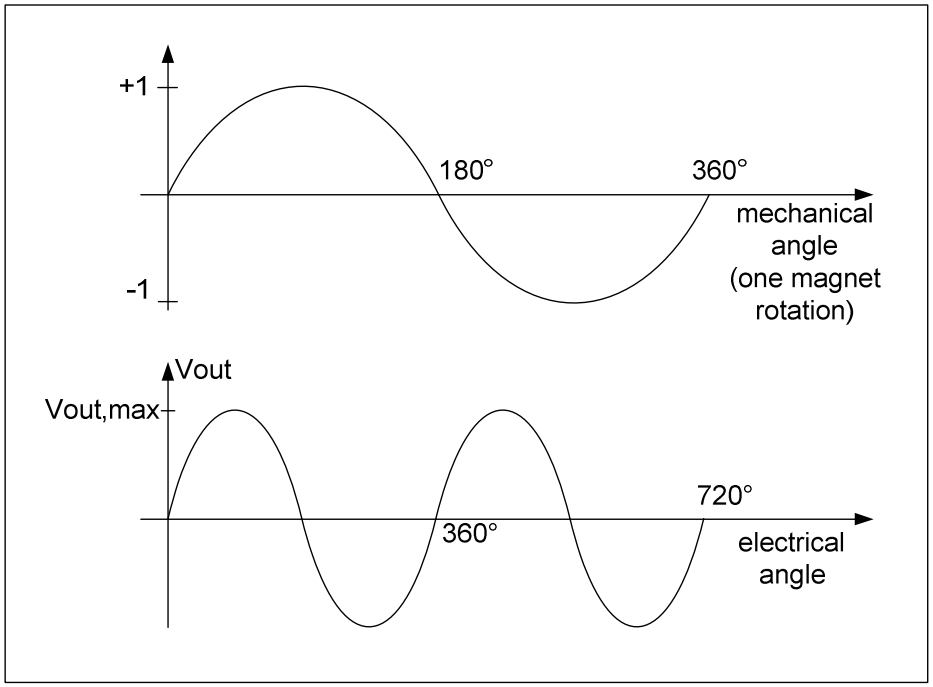


Figure 11: Mechanical vs. electrical angle

The same is true for rotations: one mechanical rotation of the magnet will result in two "electric rotations": two periods of the electric sine and cosine output signals.

NOTE:

Whenever in this document "speed", "angle", and "number of turns" are mentioned, electrical values are used and not mechanical values, unless specified otherwise.

For the sake of clarity, the following conventions are made:

speed:	the number of electric periods per time unit
angle:	current electric angle
rotation (turn):	one full electric period
number of rotations (turns):	number of full electric periods, counted from the time when the magnet was in zero-position for the last time

3.1.4 Tracking loop

There are many ways to calculate the angle from the sine and cosine values generated by the MR bridge. Tracking loop – which is one of them – will be implemented in the "ATIC 116".

Tracking loop in s-domain

Tracking loop is a closed-loop feedback system which compares the input angle (alpha) with the estimation of that angle (alpha_est) and changes the estimation accordingly. It is shown in the figure below.

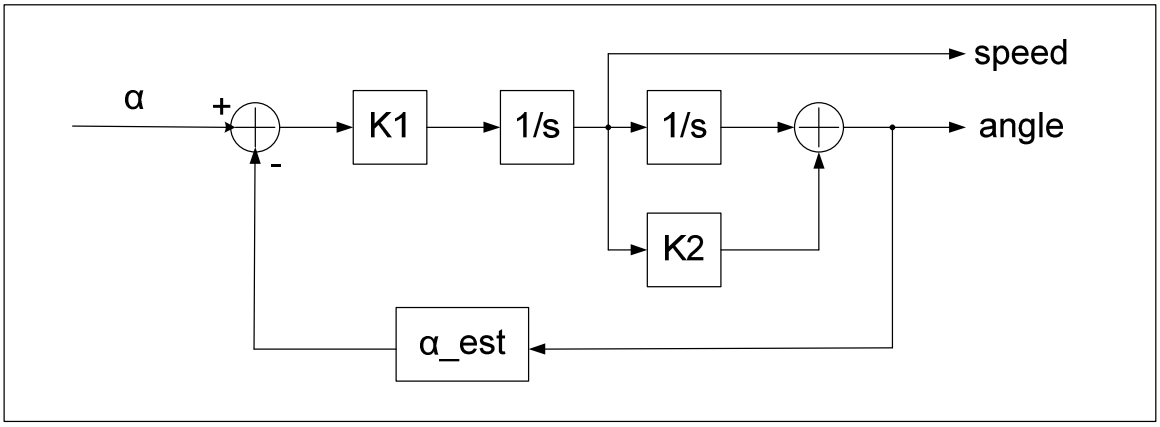


Figure 12: Tracking loop in s-domain

The tracking loop behavior is characterized by the following parameters:

- natural frequency ω
- damping factor δ

The loop parameters K1 and K2 are then given as:

$$K_1 = \omega_n^2 \qquad K_2 = \frac{2\delta}{\omega}$$

Tracking loop in s-domain for small angles

For small angles, the following equations are true:

$$\alpha \approx \sin(\alpha)$$

So for angles which differ only slightly from each other:

$$\alpha - \beta \approx \sin(\alpha - \beta)$$

It is also:

$$\sin(\alpha - \beta) = \sin(\alpha) \cdot \cos(\beta) - \cos(\alpha) \cdot \sin(\beta)$$

Thus if the difference between alpha and alpha_est is small:

$$\alpha - \alpha_{est} \approx \sin(\alpha) \cdot \cos(\alpha_{est}) - \cos(\alpha) \cdot \sin(\alpha_{est})$$

According to the above equations, the small-angle approximation of the tracking loop can be realized in the following way:

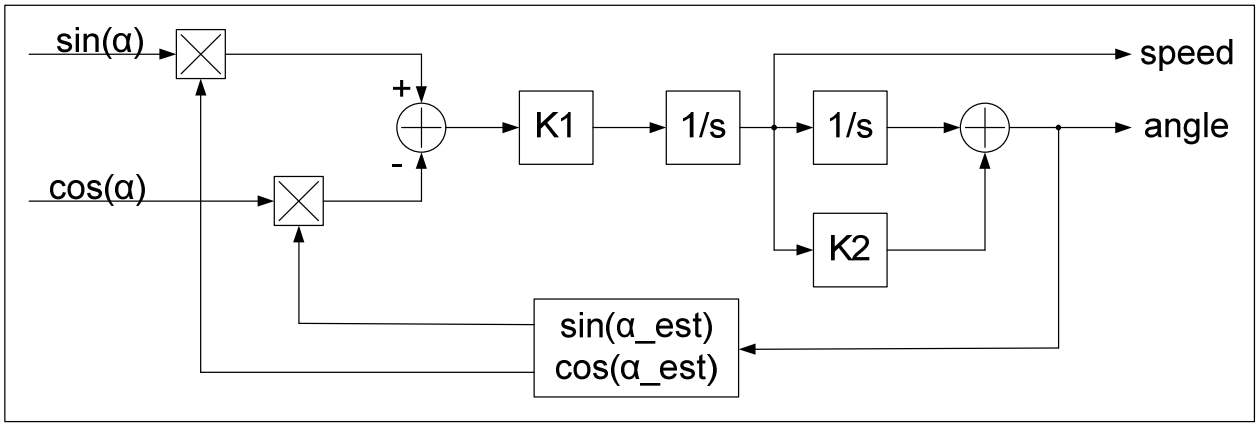


Figure 13: Tracking loop (realization for small angle differences)

Tracking loop in z-domain

The above diagram shows the tracking loop in s-domain. To be implemented in the "ATIC 116", it has to be translated into z-domain. Additionally, the tracking loop is slightly modified for better implementation in the microcontroller.

The tracking loop actually used in the "ATIC 116" is shown in the figure below.

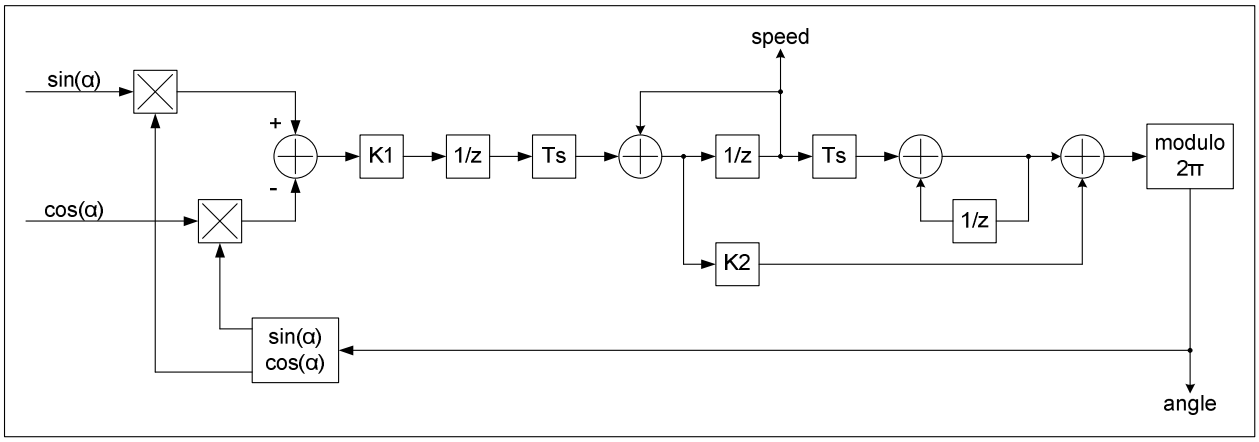


Figure 14: Tracking loop in the z-domain

In the z-domain there is an additional tracking loop parameter: sample frequency fs. It describes how many times per second the tracking loop performs its calculation and updates its output.

The small-angle approximation is valid because the sample frequency will be high enough so that the difference between alpha and alpha_est will always be small.

3.1.5 Speed Filtering

The speed value calculated by the tracking loop will be sent through a moving-average filter. The averaging is done over the last 3 values. The averaging can be enabled or disabled with the flag Calibmode [7] (EEPROM address: 0x2052):

Calibmode[7] = 0 ==> speed filtering disabled

Calibmode[7] = 1 ==> speed filtering enabled

3.1.6 Modes of Operation

The "ATIC 116" will operate in four modes:

- active mode (car's engine ON)
- low-power mode (car's engine OFF, magnet being rotated)
- chopping mode (car's engine OFF, magnet not being rotated)
- transport mode (car's engine OFF, no magnet rotation monitoring)

Active mode

This is the normal operation mode. The "ATIC 116" will go into the active mode whenever the car's engine is switched on. In this mode, the "ATIC 116" runs continuously, estimates speed and angle using tracking loop, and counts the number of turns using the counter circuitry.

Chopping mode

This is the default mode whenever the car's engine is switched off. During the chopping mode, no measurement of speed or angle is performed. The "ATIC 116" only has to detect and count turns in case the magnet is being rotated while the engine is off. The mode itself consists of two sub-modes:

- sleep mode (MR bridge supply voltage is OFF)
- peek mode (MR bridge supply voltage is ON)

In sleep mode, no activities are performed. After a defined period of time (sleep period), the "ATIC 116" goes from sleep mode to peek mode and performs one measurement.

If no magnet rotation is detected during the peek mode, the "ATIC 116" goes back to sleep mode for another sleep period. If any magnet rotation is detected, the "ATIC 116" enters the low-power mode

The overall current consumption (MR bridge and ASIC combined) in chopping mode does not exceed 100 µA (see also Vendor Addendum).

Chopping frequency is the number of "peeks" per second. The chopping frequency is min f=100 Hz (coming out of acceleration situations derived out of complete steering systems).

Low-power mode

In this mode, the MR bridge is ON and the "ATIC 116" counts turns as the magnet is being rotated. Both MR bridge supply voltage and counting activity are maintained until "end of counting". "End of counting" is defined as a certain period (e.g. 50 ms) in which no magnet rotation has been detected (rotation has ended). Is this the case, the ASIC goes back to the chopping mode.

In this mode, the current consumption may exceed 100 µA (see Vendor Addendum) and is max. 5mA.

Transport mode

This mode is identical to chopping mode, except that no turn counting is done. This mode is used during transport (e.g. per ship) to prevent the "ATIC 116" from drawing current from the car's battery by preventing ATIC116 from going into low-power mode.

In the figure below, the transitions between all three modes are shown:

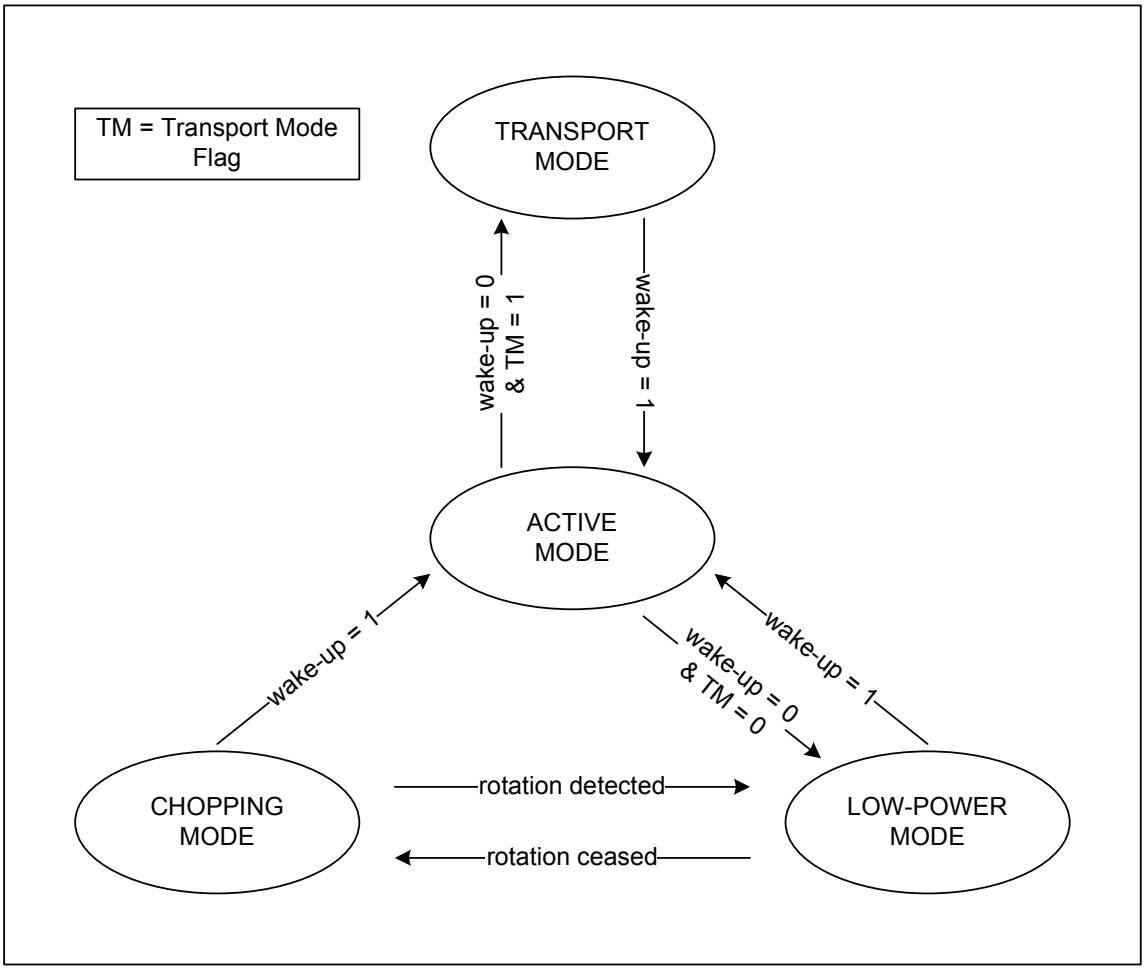


Figure 15: Transitions between modes

Necessity of stand-alone counter circuitry

The tracking loop is capable of estimating the speed, angle, and number of turns by itself. However, the tracking loop will be working only during the active mode.

Since the counting of turns must be performed during all modes besides transport mode (active mode, chopping mode, and low-power mode), it will be necessary to implement a stand-alone circuit capable of counting the turns. This circuit will be working during the three modes active, chopping and low-power mode, but not in transport mode.

"ATIC 116" functional blocks

In the figure below, the functional blocks of the "ATIC 116" are shown. For clarity, only the most important blocks and pins are included.

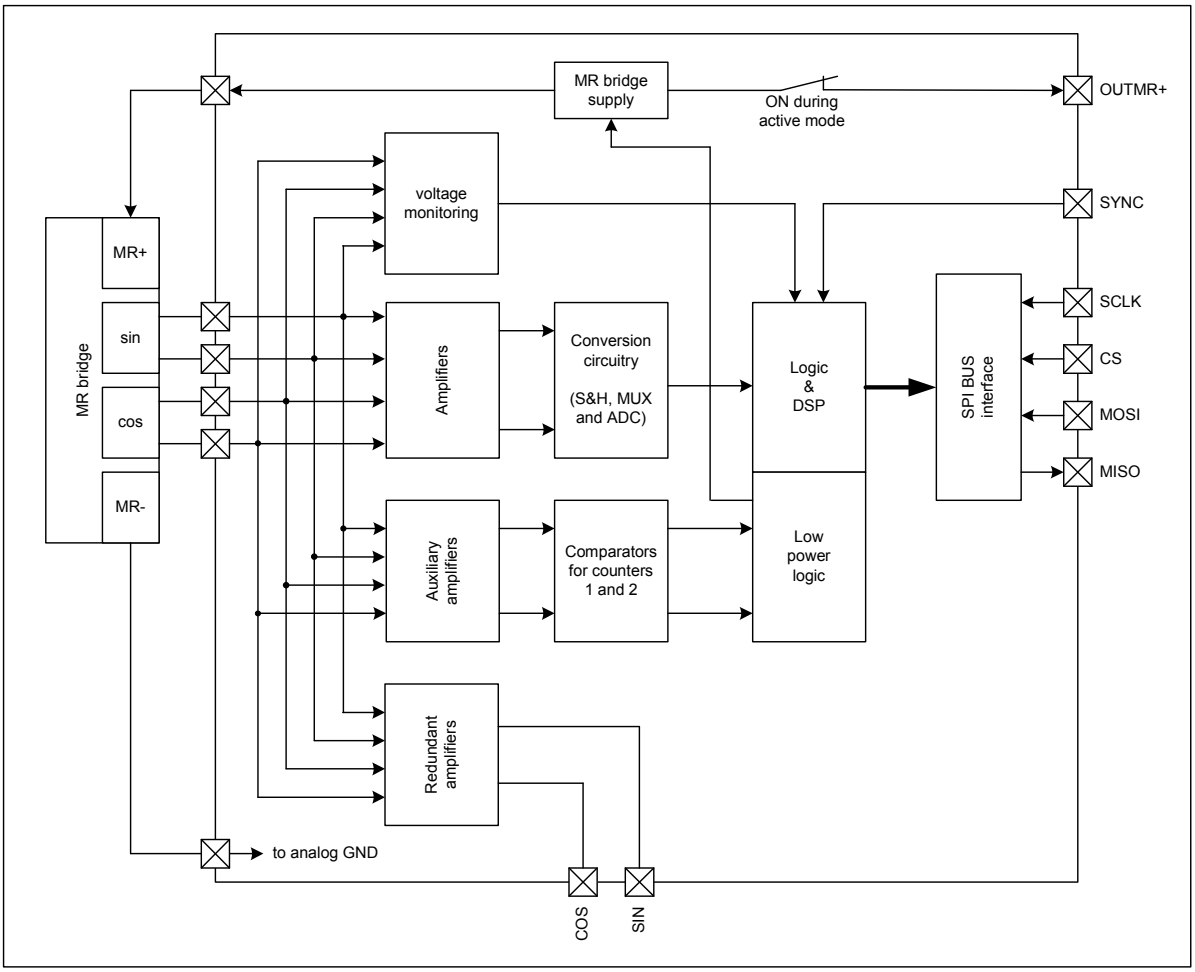


Figure 16: ATIC 116 functional blocks

Short description of the functional blocks is given below (detailed descriptions of all blocks will be given in following chapters):

Main path

Here, the MR bridge output signals are amplified, converted to digital, and processed to yield speed and angle values. Temperature measurement using an on-chip temperature sensor is done here. Also, the main path logic is responsible for communication with the ECU via SPI bus. It contains the following functional blocks:

Amplifiers

Amplification of MR bridge output signals

Conversion circuitry

Analog-to-digital conversion of amplified analog signals from the MR bridge. It contains two S&H stages, one multiplexer, and one ADC

Logic and DSP

In the main-path logic, the following tasks are performed: compensation of MR bridge errors, estimation of speed and angle data using tracking loop, communication with the ECU, and error handling. The logic is implemented as µC.

Auxiliary path

Here, the turn counting is performed. The auxiliary path contains the following functional blocks:

Auxiliary amplifiers

Amplification of MR bridge output signals. The amplifiers are implemented as low-power amplifiers

Comparators

Conversion of MR output signals into patterns of "0" and "1".

Low-power logic

In this block, two state machines are implemented to analyze the bit patterns delivered by the comparators. These state machines, in turn, control two counters which count the number of turns. The low-power logic also switches the MR bridge ON and OFF.

Redundant path

The task of the redundant path is to amplify the MR output signals, so that they can be fed to the ECU for analysis. It contains two independent amplifiers, one for the sin and one for the cos channel of the MR bridge.

In addition to the three paths, the following blocks can be recognized:

MR bridge supply

This block generates stable supply voltage for the MR bridge. The supply voltage can be switched ON and OFF by the low-power logic block

Voltage monitoring

It monitors the MR bridge output signals and determines if they are still within a specified "plausibility window".

BUS Interface:

It communicates with the master ECU using SPI protocol.

The above functional blocks will be operational during the following modes:

Main path	(1)
Auxiliary path	(1,2,3)
Redundant path	(1)
Voltage monitoring	(1)
BUS Interface	(1)
MR bridge supply	ON in active mode and low-power mode; switched ON and OFF by low-power logic in chopping mode

(1)	active mode
(1,2,3)	active mode, chopping mode, and low-power mode

NOTE: In transport mode the only active function is low-power logic waiting for wake-up signal.

3.2 System description

3.2.1 Requirements (error budget)

The "ATIC 116" will have to fulfill the specified requirements. These requirements are:

Data to be calculated

The "ATIC 116" will have to calculate the following data:

- speed in eppm (1)
- angle in degrees (1)
- number of rotations (1,2,3)
- power-loss detection (1,2,3)
- error status (1)

(1) Data calculated in active mode only

(1,2,3) Data calculated in active mode, chopping mode, and low-power mode

eppm: electric periods per minute (keep in mind that speed and angle values are electric values, not steering wheel or magnet values).

Remark: counter state-machine may enter an error state during low power mode in case of counting error. Such error will be reported upon next wake-up.

Update rate

The update rate is controlled only by the external Sync signal; it describes how many times per second the "ATIC 116" output is updated . The update rate implemented by "ATIC 116" must be a "true" update rate. It means that each new output value contains new calculated information which was not present in the previous output value.

The update rate is specified to be:

Active mode: Sync pulse frequency, see below for details

Chopping mode: no output required, internal data processing only

Low-power mode: no output required, internal data processing only

Sample Time Ts

The sample time Ts describes how often the tracking loop calculation is executed. Ts = 125µs means that the tracking loop is executed once every 125µs. Each new tracking loop execution yields a new set of output values (speed and angle).

The sample time is determined by the Sync pulse: each new Sync pulse from the ECU triggers new tracking loop execution. Thus if consecutive Sync pulses are generated by the ECU every 150µs, the resulting sample time will be Ts = 150µs.

The "ATIC 116" can process sample times in the range of 100...485 µs.

NOTE:

It is not enough to determine the sample time by the Sync pulse; it is also necessary to set the corresponding EEPROM parameter (EE_Ts, address 0x204C). Detailed description can be found in the chapter on EEPROM.

Resolution and accuracy requirements

The resolution and accuracy requirements are summarized in the table below. The measurement errors mentioned in the "Comment" column will be explained in detail later on.

Parameter	Value	Comment
Angle measurement range	0...360°	
Angle resolution	0.2°	
Angle accuracy	< +/-2°	incl. all errors such as : initial accuracy, temperature, supply voltage, mechanical offset, aging, evaluation / adjustment of signals in the ECU, EMC, ...
Speed measurement range	-16384...+16383.5 eppm	Active measurement range
	|16383| ... |30000| eppm	Passive measurement range
Speed resolution	< 4 eppm	
Speed accuracy *) (speed ripple=maximum difference to average speed)	< +/- 20 eppm	0 eppm to 2000 rpm
	< +/- 40 eppm	2000 eppm to 4000 eppm
	< +/- 60 eppm	4000 eppm to 6000 eppm
	< +/- 100 eppm	6000 eppm to 16382 eppm
Speed accuracy (averaged over one electrical rotation)	< +/- 2 eppm	< 2000eppm
	< +/- 4 eppm	@ 2000 ... 4000eppm
	< +/- 6 eppm	@ 4000...6000eppm
	< +/- 20 eppm	@ >6000eppm
Acceleration	< 2e6 eppm / sec	

*): *according Vendor Addendum speed ripple specification of +/-2% with dynamic compensation active is guaranted by supplier.*

Passive measurement range:

The "ATIC 116" must be able to measure speeds up to +16383.5 eppm (down to -16384). This is the active measurement range. If the measured speed is larger then +16383.5 eppm (smaller then 16383 eppm), the output signal is clipped at that

value, and the "ATIC 116" enters the passive measurement range.

In the passive measurement range, "ATIC 116" must be able to track the speed (internally), but there is no requirement regarding the measurement accuracy. But the "ATIC 116" must be able to smoothly resume tracking the speed (with the required accuracy) once the speed decreases and enters the active measurement range again.

Error budget

The angle accuracy must be 2° or better. This is the overall system accuracy. The allowable error is distributed as follows:

1.2°	"ATIC 116"	(MR bridge, AFE, ADC, etc)
0.8°	mechanics	(placement of magnet and "ATIC 116" in the module, etc)

Supply voltage requirement

The following supply voltages are foreseen:

- active mode (full functionality): 4.75...5.25 Volts
- active mode (turn counting only): 3.0.....5.25 Volts
- low-power mode: 3.0.....5.25 Volts
- chopping mode 3.0.....5.25 Volts
- transport mode 3.0.....5.25 Volts

NOTE:

The standard supply voltage during active mode is 4.75...5.25 Volts. In this range full functionality (speed, angle, and turn counting) must be guaranteed.

Nowadays, however, many car manufacturers are using "stop and start" feature when waiting at a traffic light. The resulting battery cranking (battery voltage drop) may cause the supply voltage to drop down to 3.0 Volts.

If such situation occurs during active mode, the "ATIC 116" does not have to be able to continue measuring speed and angle, but it must be able to continue turn counting.

This is called "undervoltage case" and will be described in more detail below.

Current consumption requirement

The following current consumptions are not exceeded:

- active mode: 30 mA
- low-power mode 5 mA
- chopping mode: 100 µA (see Vendor Addendum)
- transport mode: < 80uA

NOTE:

The current consumption in chopping mode is the combined average current consumption in sleep mode and peek mode.

3.2.2 Acquisition sequence in active mode

The outline of the acquisition circuit is shown in the figure below. It can be seen that the analog signals from MR bridges are sampled by fully differential S&H stages; the signals are then fed into a fully differential ADC via multiplexer (MUX).

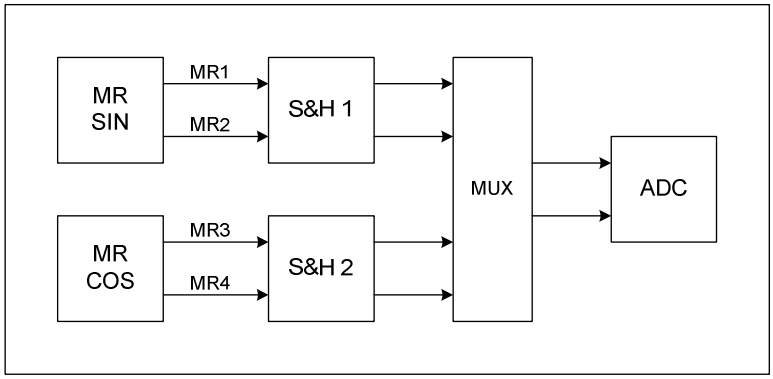


Figure 17: Acquisition circuit

The "ATIC 116" will be in direct proximity of the servo-mechanism DC motor. The rotational speed of this DC motor is controlled by a PWM modulation which results in very significant amount of electro-magnetic noise. This noise will disturb the MR bridge output signals so much that a meaningful measurement will not be possible during the PWM modulation phase.

For that reason, the "ATIC 116" will have to perform the measurement (or at least the Sample-and-Hold operation) when the PWM modulation is not active.

This is visualized in the diagram below. In the time period T1 no PWM takes place, and S&H is possible. In the time period T2 PWM takes place, and S&H operation is not possible. T1 and T2 form one time frame of the duration Ts = T1+T2.

The duration of the time frame Ts is identical to the sample time Ts discussed above (for that reason, the same symbol Ts is used). The time period T1 is constant; it is T1 = 2.5µs. The time period T2 is then T2 = Ts – T1.

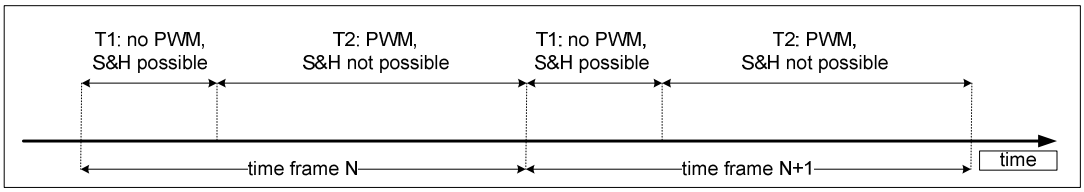


Figure 18: Phases of PWM modulation for DC motor speed control

NOTE 1:

The minimal time frame duration Ts is 100µs (nominal), however, due to the tolerances in the ECU the actual Ts (as determined by the Sync pulse) can deviate from the nominal Ts by +/-5%. It means that nominal Ts of 100 µs will correspond to actual Ts of 95...105 µs.

The actual acquisition in active mode is shown in the figures below.

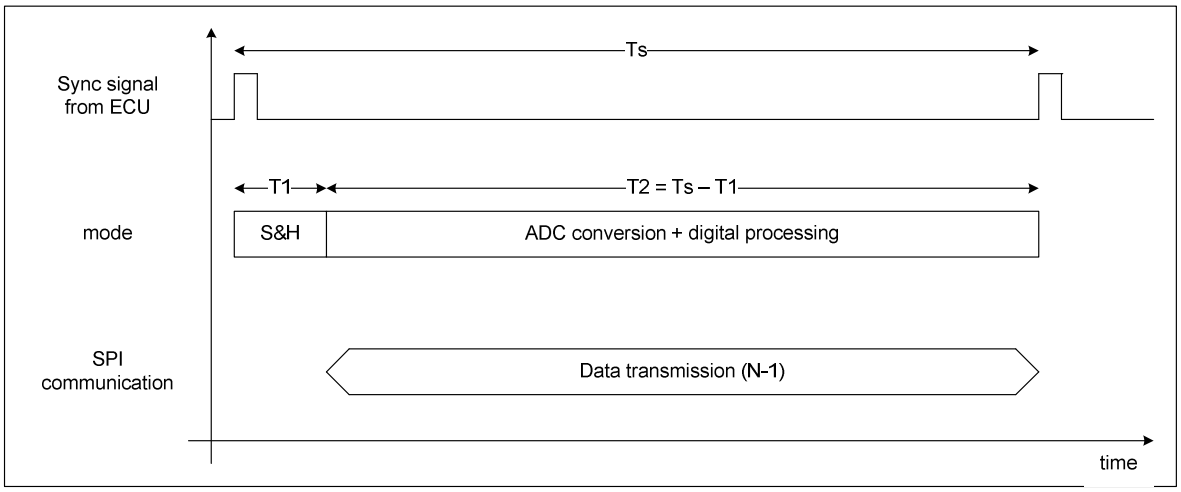


Figure 19: Active mode acquisition sequence

When output values for current time frame are being obtained (N), values from previous time frame (N-1) are transmitted via BUS interface to the ECU.

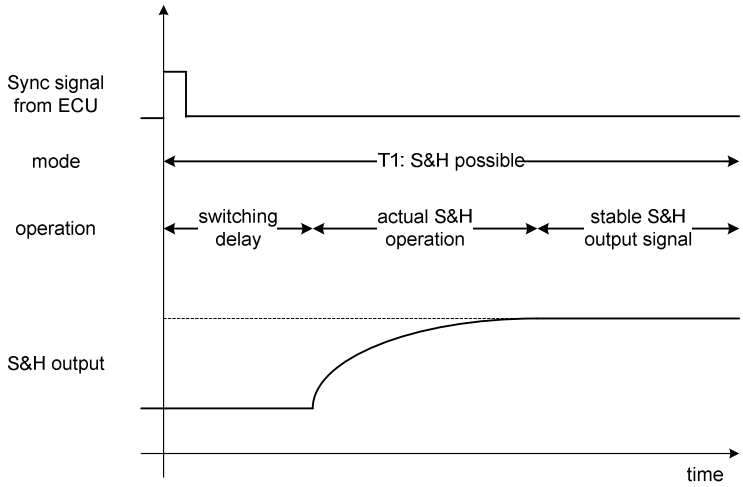


Figure 20: Actual S&H operation

The S&H operation (described for a single S&H stage) is done as follows:

- "Sync" pulse from the ECU indicates that new PWM-free time window (T1, 2.5µs) begins.
- Internal circuit detects the "Sync" pulse, and sends a "sample pulse" to the S&H stage.
- S&H stage performs sampling till stable output signal is reached; between the "sample pulse" and sampling there will probably be some delay called "switching delay".
- Stable S&H output is fed into the ADC via MUX stage.

The sampling circuitry must be designed in such a way that a stable S&H output signal is reached before the PWM-free T1 time window is over. Within this window, the following periods can be recognized:

- switching delay of the S&H stage
- S&H operation proper (inclusively S&H settling time)
- stable S&H output signals are present at the S&H output

All these 3 periods combined may not exceed T1. The entire acquisition sequence is shown in the figure below:

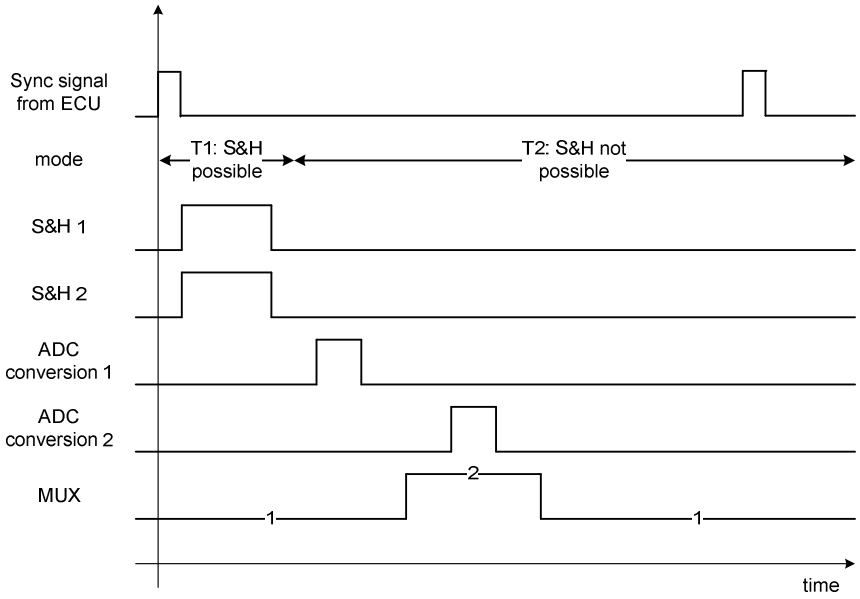


Figure 21: Complete acquisition sequence

The following actions can be recognized:

- "Sync" pulses signalizes new PWM-free time window (T1)
- S&H stages carry out the sampling operation. Stable S&H output signals are available before time window T1 is over. The sampling is done simultaneously in both S&H stages
- PWM-free time window T1 is over, PWM-distorted time window T2 begins
- ADC performs the A-D conversion of the output signal of S&H stage #1
- MUX switches from "S&H 1" to "S&H 2"
- ADC performs the A-D conversion of the output signal of S&H stage #2
- MUX switches from "S&H 2" to "S&H 1"
- Digitized values are available for further digital processing

Sync pulse duration (user hint)
The Sync rising edge determines the exact begin of the PWM-free time window (2.5 µs) during which S&H is performed. If the Sync falling edge is less then 2.5 µs after the rising edge, then it will interfere with the S&H operation. For that reason, the Sync falling edge must be 3-4 µs after the Sync rising edge.

3.2.3 Block Diagram (ASIC)

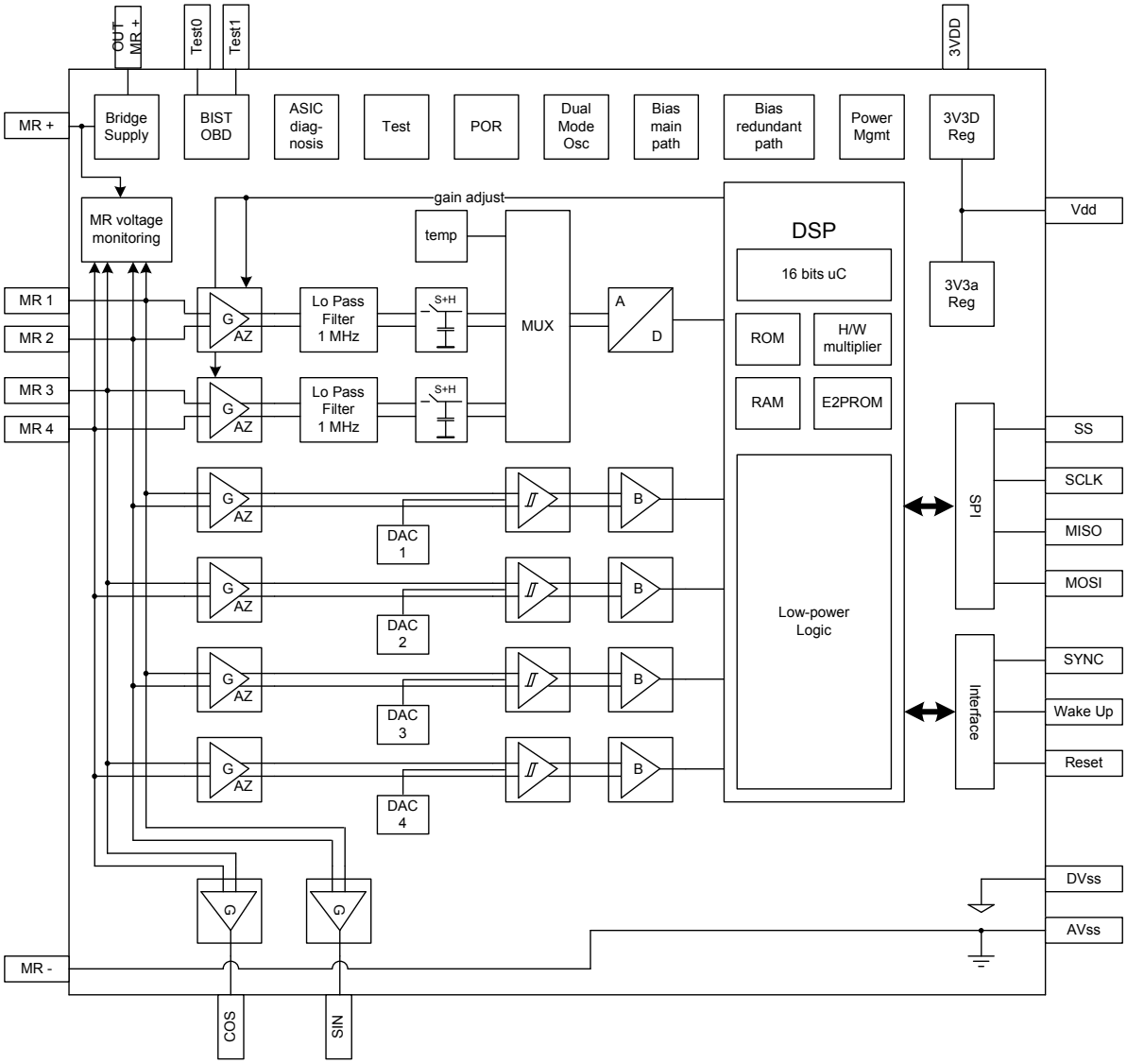


Figure 22: ASIC block diagram (MR bridge not shown)

In the figure above, the block diagram of the ASIC (w.o. MR bridge) is shown. The following main structures can be recognized:

- main path / main logic (speed and angle measurement)
- auxiliary path / auxiliary logic (turn counting)
- redundant path (feed sine and cosine signals to the ECU)

The main path / main logic and the redundant path are operated in the active mode only. The auxiliary path / auxiliary logic are operated in all three modes (active, chopping, and low-power mode).

Main path

This path is also referred to as main analog front end (main AFE). It consists of the following elements:

PGAs:

amplify the MR output signals. They are fully differential amplification stages. They feature programmable gain and offset compensation.

S&Hs:

sample the PGA output signals.

MUX:

time-multiplexes the output signals of the S&H stages.

ADC:

converts analog signals into digital signals. After digitization, in each 100 µs time frame two digital numbers are obtained: one of them corresponds with the sine signal, the other corresponds with the cosine signal of the MR bridge.

Main logic

The most important functions of the main logic block are:

- compensation of sensor and main AFE errors (discussed in detail later on)
- implementation of the tracking loop

Auxiliary path

The most important function of this path is to count turns. It consists of:

- Low-power amplifiers
- 4 Comparators with individual reference DACs
- Buffers
- State machines
- Counters

Low-power logic

This block performs the following functions:

- Switching between sub-modes (sleep and peek mode) in the chopping mode
- Switching from chopping mode to low-power mode and back again to chopping mode
- Switching the MR bridge OFF during sleep mode and ON during peek mode
- Calculation of rotations (using analog signals from the auxiliary path.
- Switching from active mode to either low-power mode or transport mode (depending on content of the transport mode flag) and back

Redundant path

Consists of two simple amplifiers with no gain adjust or auto-zero. They directly amplify the MR bridge output signals and feed them to the ECU for further processing.

In addition to the circuitry described above, the following functional blocks will be implemented:

- EEPROM
- BUS interface (SPI)
- CLOCK generator (used in active mode)
- Low-power oscillator (used in chopping and low-power mode)
- Synchronous interface
- Transistor switch for switching MR bridge supply voltage ON and OFF
- ESD protection structures (all "ATIC 116" pins must be ESD protected)
- On-chip temperature sensor
- "ATIC 116" diagnose block

For referencing purposes, the following blocks will be implemented:

- bias current source
- bandgap reference voltage source

For diagnosis, the following blocks are implemented:

- MR bridge signal diagnosis (monitors MR bridge output signals)
- cross-check of both oscillators (CLK generator and low-power oscillator) (only after wake-up)
- power-loss detection

3.2.4 MR bridge positioning within the "ATIC 116"

For the "ATIC 116" to function properly, it is necessary that the excentricity error be small. Excentricity error is the mismatch between the rotation axis of the magnet and the center point of the MR bridge; for geometries see chapter “MR bridge placement in ATIC116”.

3.2.5 Main path

The actual realization of the main path is shown in the figure below.

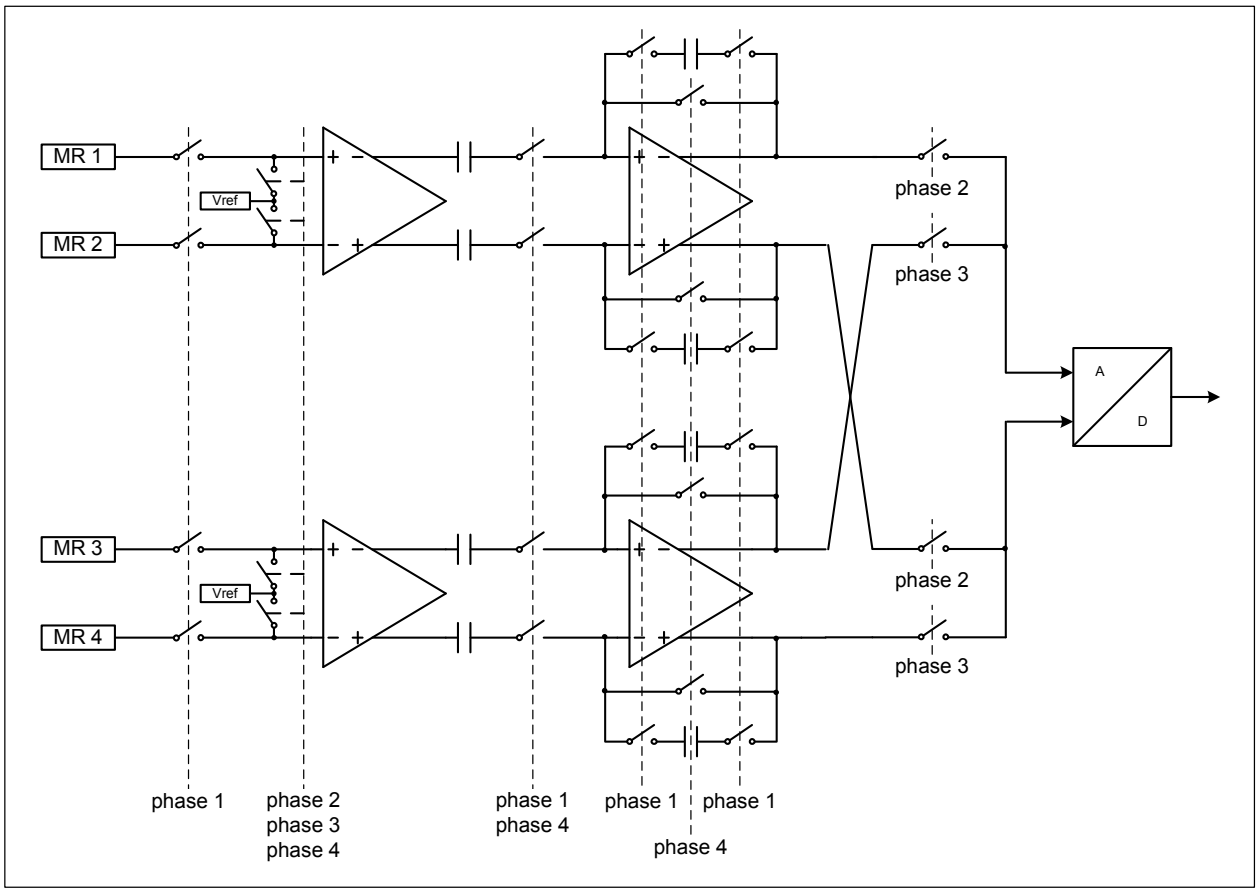


Figure 23: Main path

The following features can be recognized:

- the amplifiers and S&H stages are fully differential
- an auto-zero function will be performed in which the amplifier offset in both signal chains will be compensated; one signal chain consists of an amplifier and a S&H stage
- sampled signals are fed to an ADC converter; the input of the ADC converter is fully differential

Timing

The AFE operation will be divided into four phases:

1) both analog signals are amplified and sampled; at the end of this phase a stable output signal is delivered by the S&H stages
2) one sampled signal is fed via MUX to ADC and converted to digital
3) second sampled signal is fed via MUX to ADC and converted to digital
4) auto-zero is performed of both signal chains

The duration of phase #1 cannot exceed T1. The duration of the entire cycle is Ts. This is shown in the diagram below:

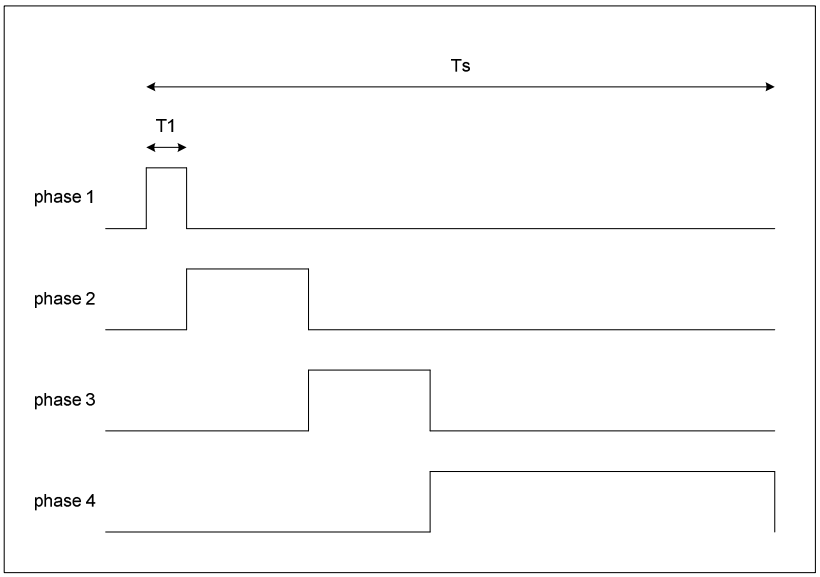


Figure 24: AFE timing

3.2.6 Auxiliary path

Counter circuitry

Parameter	Value	Comment
Complete counting range	-128...+127	electric periods
Current consumption in chopping mode	<100µA (see Vendor Addendum)	Overall average current consumption for ASIC and MR bridge during sleep sub-mode and peek sub-mode
Chopping frequency	min 100 Hz	
"ATIC 116" supply voltage VDD	3 V to 5.25 V	For counter function

The counter circuitry must be working during the following modes

- active mode
- low-power mode
- chopping mode (only during the peek mode)

During these modes, the MR bridge power supply must be ON in order to obtain a measurable output signal. Without this output signal, it would not be possible to detect any magnet rotations. During the sleep sub-mode of the chopping mode, the MR bridge power supply is OFF.

OVERRUN:

Under normal conditions, the counter range (-128...127) is large enough to prevent counter overrun. If, however, at any moment the counter value is not correct (for whatever reason), the result can be that the counter will overrun, either by trying to increment from "127" to "128" (upper overrun), or by trying to decrement from "-128" to "-129" (lower overrun).

If such situation occurs, the counter must have a circular behavior. One possibility to achieve that is two's complement:

counter value	0	1	***	126	127	128	129	***	254	255
number of el. periods	0	1	***	126	127	-128	-127		-2	-1

Counter circuitry design

During each magnet half turn, both MR bridge outputs go through a full sine or cosine period. This is shown in the figure below:

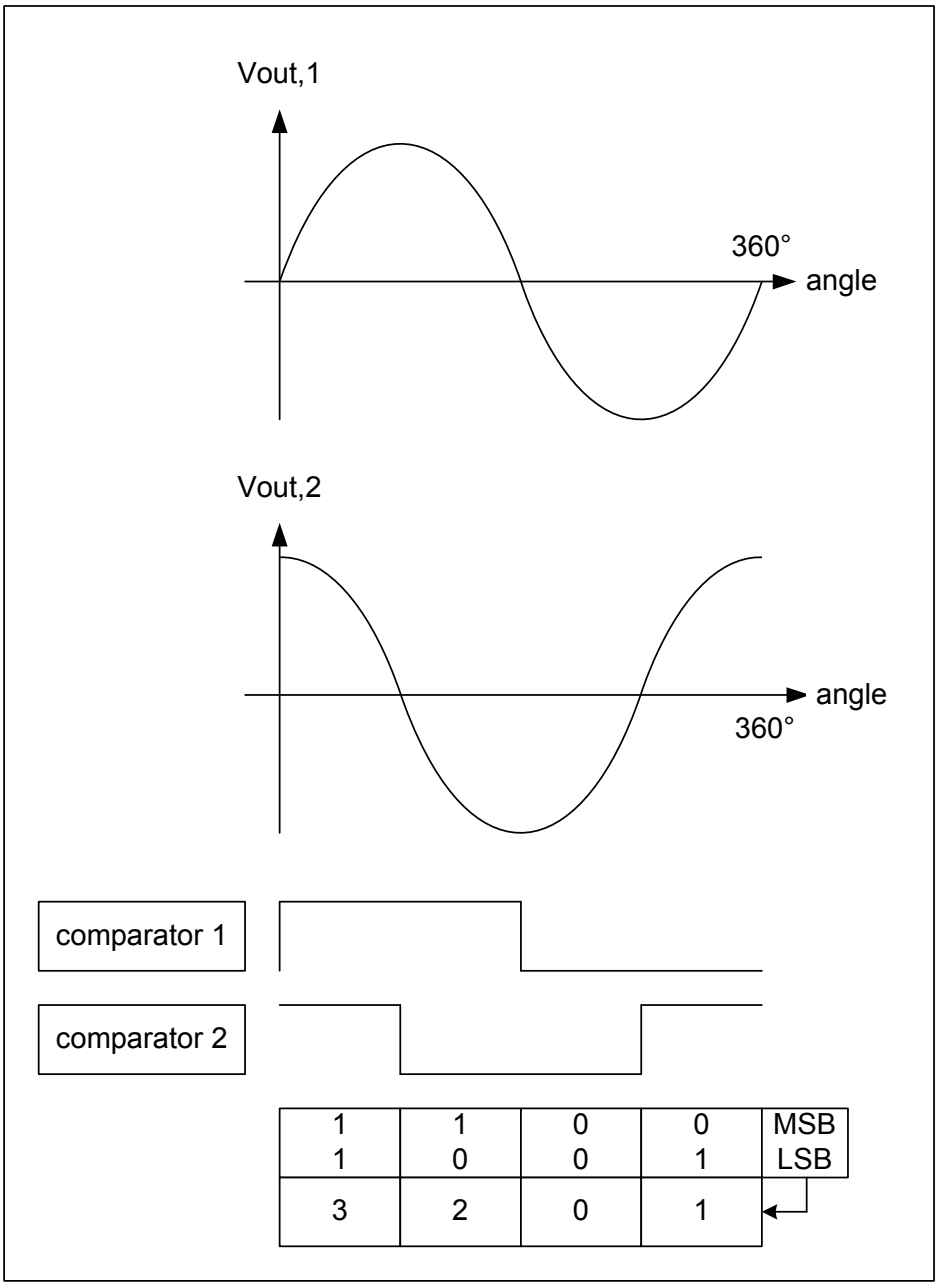


Figure 25: MR output signals during a magnet half turn

This behavior can be used to calculate the number of electric periods of the sine and cosine signals. Each MR bridge output is fed into a comparator (comparator 1 for the sine signal, comparator 2 for the cosine signal). Whenever the signal value is above comparator threshold voltage, the comparator output is HIGH (boolean 1). Signal values below threshold voltage yield LOW (boolean 0).

Interpreting the sine comparator output as MSB (most significant bit), and the cosine comparator output as LSB (least significant bit) yields the following sequence of numbers: **3201**. It is possible to implement a state machine (SM) capable of detecting this sequence. Whenever such sequence is detected, the SM outputs a "count-up" signal. The subsequent counter increments its value by 1 each time when a "count-up" signal is output by the SM. The appropriate circuit is shown in the next figure.

The same procedure can be used when the magnet is rotating in opposite direction. The corresponding sequence is now **1023**, the SM outputs a "count-down" signal, and the counter decrements its value by 1.

In the figure below, the basic outline of the counter circuitry is shown.

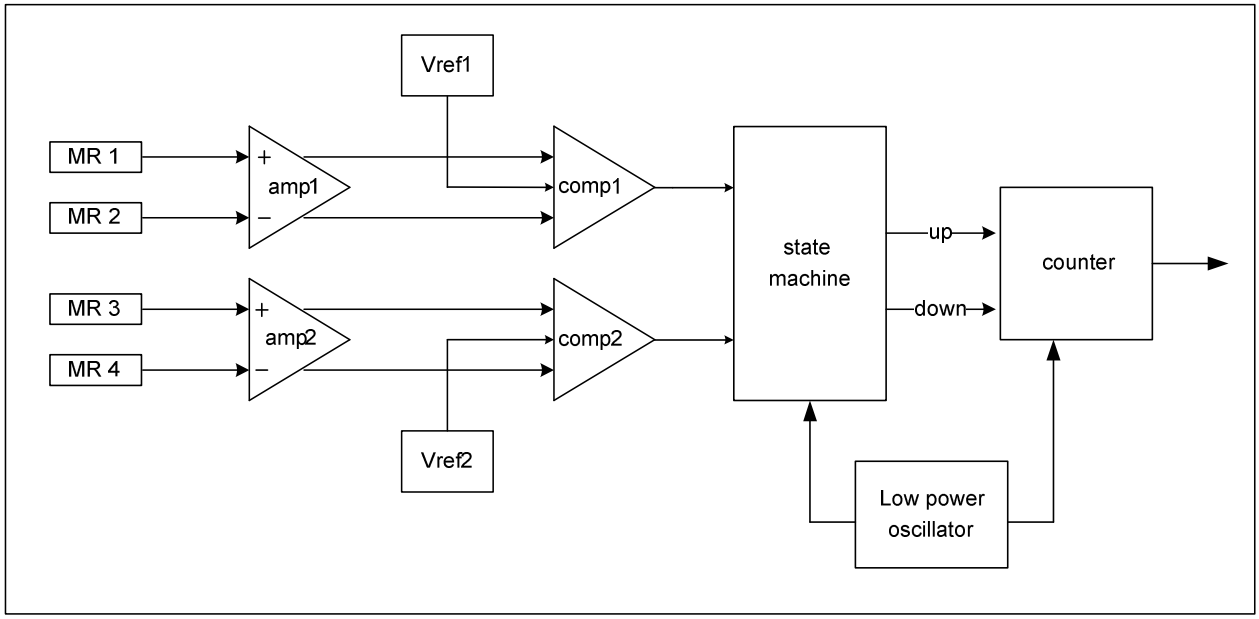


Figure 26: Counter circuitry

The amplifiers used in the counter circuitry are low-power, fully differential amplifiers with an auto-zero function using switched capacitors. They are not the same amplifiers as those used for MR bridge signal amplification in the main path.

The comparators used are fully differential and have a hysteresis. The thresholds (reference voltage) and hysteresis values of the comparators can be set. The threshold voltages are generated by offset DACs, with one DAC for each comparator.

Safety considerations

The "ATIC 116" is designed as a "multi-turn" angle sensor; whenever full angle (360°) is reached, the content of the internal turn counter is incremented by 1. The counter must deliver reliable data about the number of turns since the last power-down; the counter function has to fulfill therefore an ASILB requirement.

For that reason, decision has been made to implement several safety features in the counter circuitry design. These features are:

1) Separate amplifiers for counter 1 and counter 2
2) Two pairs of comparators instead of just one pair of comparators
3) Two separately generated reference voltages for each pair of comparators
4) Two independent state machines for detection of the right sequence of numbers
5) Two independent counters
6) Continuous monitoring of the counters (if they differ by more than 1, the output is not valid)
7) Monitoring of the MR bridge output signals during active mode
8) Monitoring of the low-power oscillator by the main oscillator during active mode once after wake-up.

The purpose is to implement two completely independent counter paths. If an error occurs in one path, it will have no influence upon the other path. Thus, it is possible to detect counting errors by comparing counter values of these two paths to each other. The basic outline of counter circuitry realizing these features is shown in the next figure.

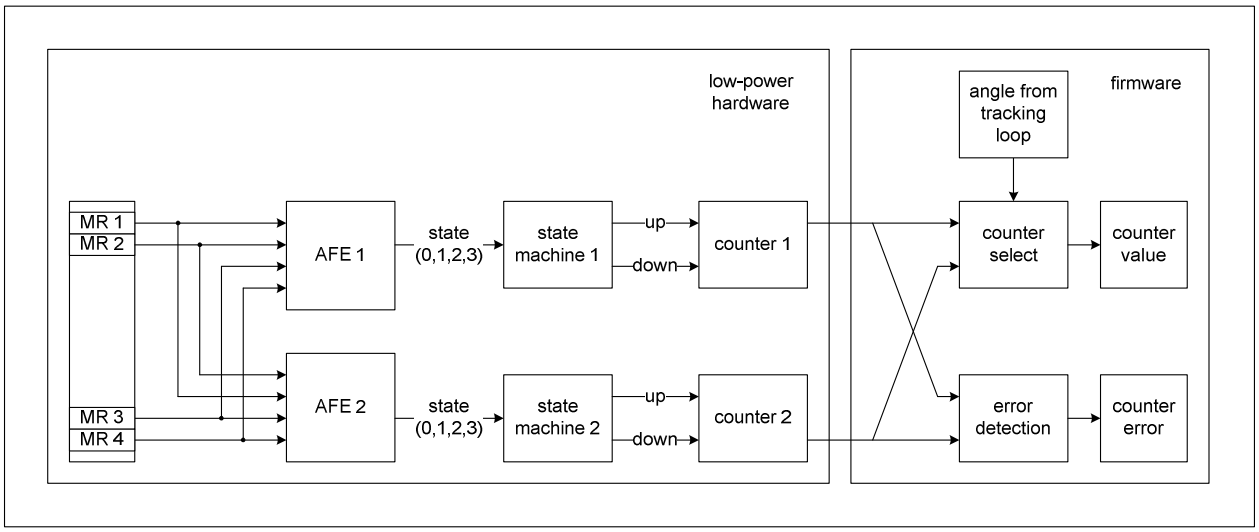


Figure 27: Counter circuitry with safety features

The low-power counter hardware consists now of the following blocks:

1) Counter AFE (analog front end): it contains 2 amplifiers and 2 comparators needed to detect the states 0, 1, 2, and 3 described above. Also, each AFE contains 2 separate offset DACs: one DAC for each comparator.
2) State machine: analyzes the states and generates "count-up" and "count-down" signals accordingly.

3) Counter: increases its content by "1" if "count-up" occurs, decreases its content by "1" if "count-down" occurs.

The following functions are performed in the µC firmware:

4) Counter select: chooses either counter 1 or counter 2, and passes the appropriate value. The choice is made depending on the angle value from the tracking loop. Counter select only has to be operational in active mode because only in this mode data will be sent by "ATIC 116" to ECU.

5) Error detection: detects if the difference between the two counters is greater then 1.

Consequently, the counter circuitry comprises: 4 amplifiers, 4 comparators, 4 offset DACs, 2 state machines, and 2 counters.

Counter path Analog front end (AFE)

The block diagram of the AFE is shown below:

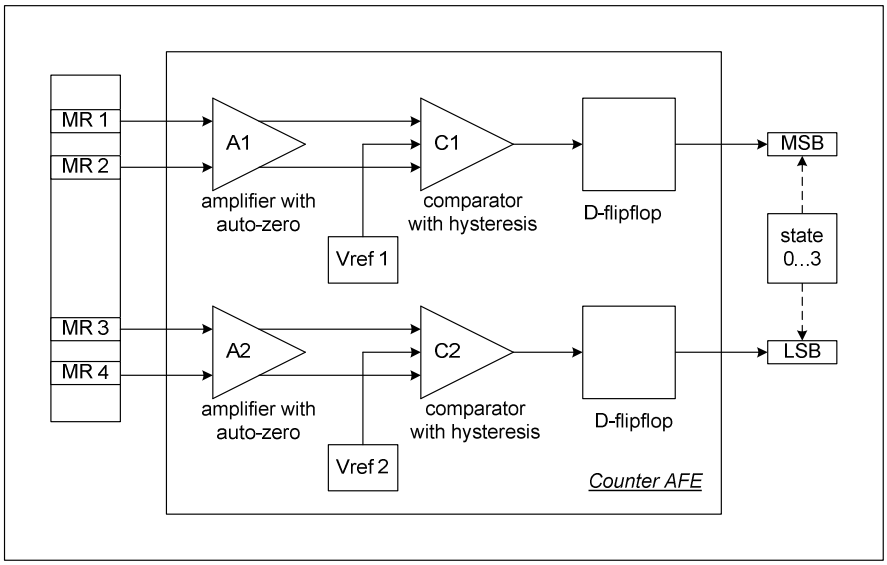


Figure 28: Counter path AFE

The AFE amplifies the MR bridge output signals and converts them into the corresponding states (0...3), interpreting the sine comparator output as MSB, and the cosine comparator output as LSB.

The output of every analog comparator in the AFE will be fed into a D-FlipFlop. This serves to stabilize the output signal and is also necessary for comparator hysteresis generation (see below).

State machines

As has been discussed above, a full periodic period will generate the following states: 3201. Turning the magnet in the opposite direction yields: 1023. These patterns are recognized, and each time they occur, a corresponding signal (count-up or count-down) is given.

For this purpose, two state machines will be implemented, with one machine for each counter. Every state machine will have 4 states (S0 to S3), and a start state (which the machine will automatically enter each time after initialization).

One problem is clearly visible: the patterns 3201 and 1023 are only generated, if the magnet is continuously rotating in one direction or another. But it is possible for the magnet to be oscillating back and forth, without actually achieving full electric

periods. This might result in patterns like: 320202020132. This phenomenon has also to be accounted for by the state machines.

The state machines for both counters are shown below. Note that the up-down transition (the transition at which a count-up or count-down signal is given) is different for each state machine. This will be explained in more detail further below.

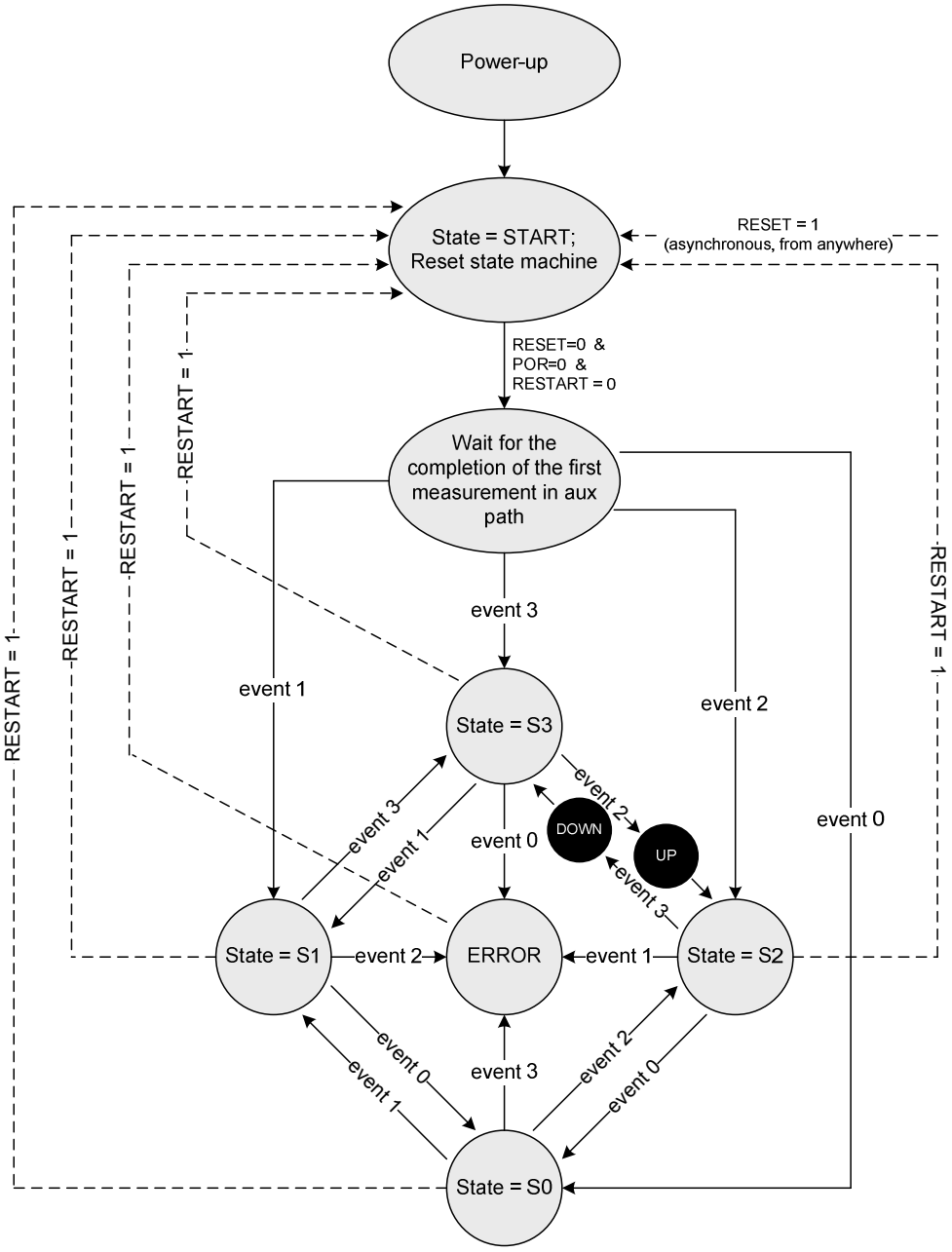


Figure 29: State machine for counter 1

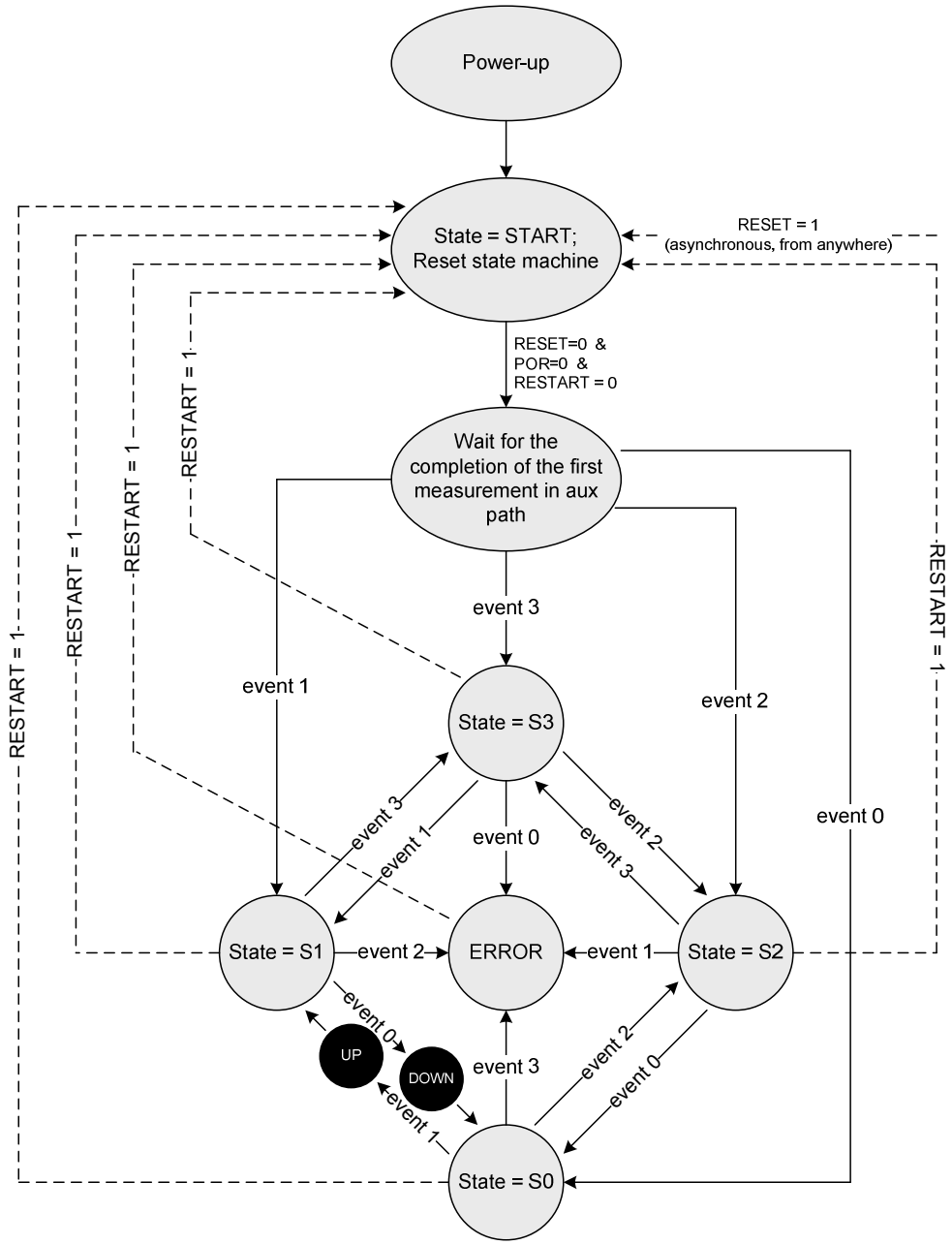


Figure 30: State machine for counter 2

The diagrams can be interpreted as follows:

1) After initialization, the state machine (SM) enters "START state"
2) After that, the SM jumps from state to state as controlled by events
3) In SM for counter 1, upon transition from S3 to S2, a "count-up" signal is given simultaneously with the transition. In similar way, the remaining "up" and "down" sub-states (shown as dark circles) can be interpreted. This is summed up in the table below:

	transition		
counter	**from state**	**to state**	**signal**
1	3	2	up
1	2	3	down
2	0	1	up
2	1	0	down

Table 5: Timing for count-up and count-down signals

When interpreting the SIN and COS signals, SIN is the most significant bit (MSB), and COS is the least significant bit (LSB). This is summed up in the table below:

SIN	***COS***	***STATE***
0	0	S0
0	1	S1
1	0	S2
1	1	S3

Table 6: **State as function of SIN and COS signals**

Event:

An event occurs each time when the state delivered by the AFE is sampled by the state machine. Event numbers and state numbers are same: "state 0" generates upon sampling "event 0", "state 1" generates upon sampling "event 1", etc.

Counters

The figure below demonstrates the function of the counters:

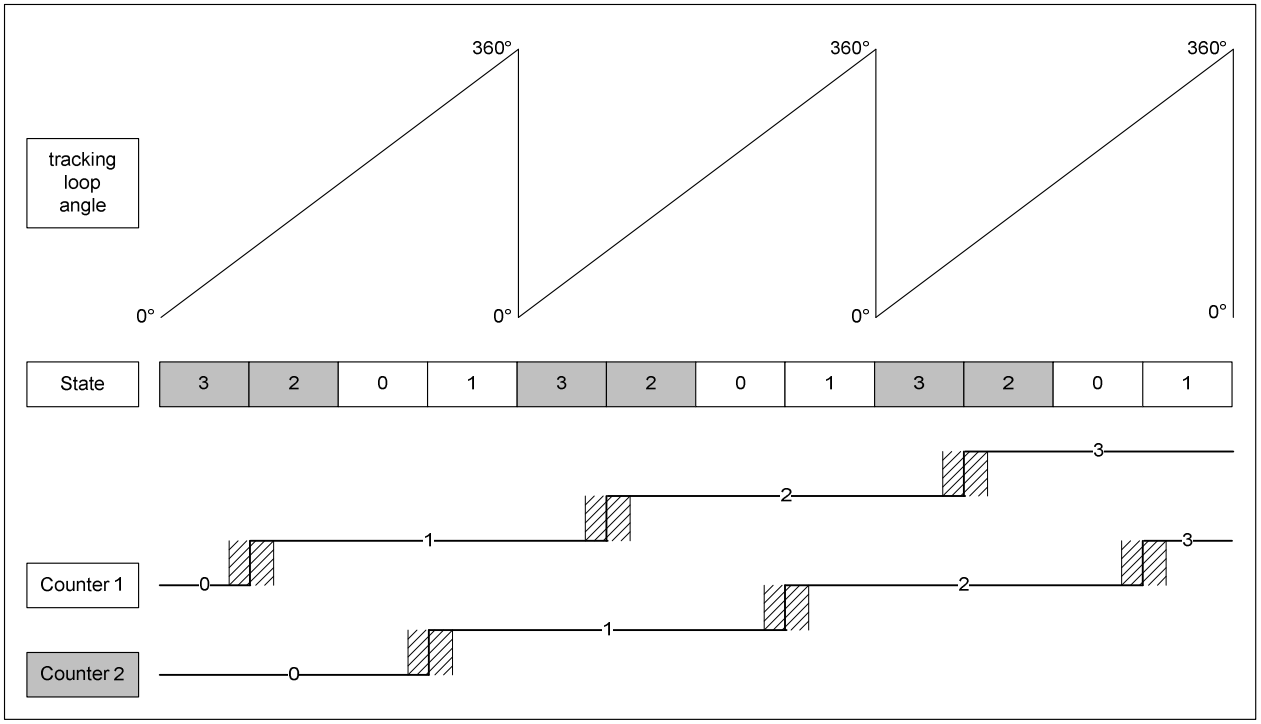


Figure 31: Counters

As the magnet rotates, the states generated by the AFE are: 3201...3201 etc. Counter 1 switches at the transition 3 <--> 2, whereas counter 2 switches at the transition 0 <--> 1.

Due to inaccuracies such as sensor offset, however, the actual counter switching points may be shifted to the left or right, as indicated by the hatched areas in the diagram above. Inside these hatched areas, the content of the particular counter may differ from its ideal value by 1.

For that reason, the switching points are different for counter 1 and counter 2. Thus, if counter 1 is operating within hatched area, counter 2 will be outside hatched area, and will deliver a valid value. On the other hand, if counter 2 is operating within hatched area, counter 1 will be outside hatched area, and will deliver a valid value.

Counter 1 will deliver valid values in states S2 and S0, whereas counter 2 will deliver valid values in states S1 and S3:

counter 1: S0, S1

counter 2: S3, S2

However, due to mismatch between the states delivered by state machines and the angle delivered by the tracking loop, the counter selection will be done based upon the tracking loop angle.

The counters are controlled by "count-up" and "count-down" signals coming from the corresponding state machines. This is

demonstrated in the diagram below:

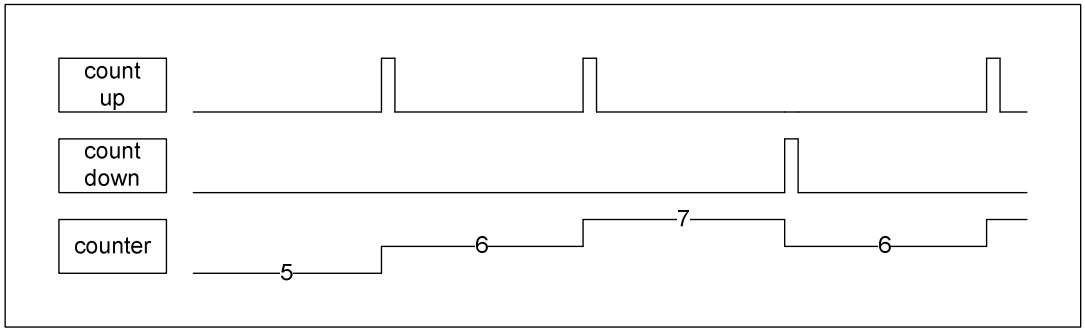


Figure 32: Counter value as function of "count-up" and "count-down" signals from state machine

Counter select

The selection of the valid counter will be done in accordance with the angle φ delivered by the tracking loop using the following algorithm:

$0° \le \varphi < 180°$ counter 2 is valid

$180 \le \varphi \le 360°$ counter 1 is valid

Counter adjust

Prior to being sent to the ECU via SPI, the counter value C must be adjusted according to the following algorithm:

counter 1 is used: $C_{adjusted} = C - 1$

counter 2 is used: $C_{adjusted} = C$

NOTE:

During DATA telegram calculation for time frame "N" (which will be sent via SPI in tame frame "N+1", for details see chapter on SPI), it is necessary to use values for counter and tracking-loop angle obtained in time frame "N".

The procedures "counter select" and "counter adjust" described above use tracking-loop angle as input argument. When performing these procedures, the angle from the current time frame has to be taken.

NOTE:

To choose the correct counter for output over SPI it is necessary to use angle delivered by the tracking loop. Thus the counter information sent to ECU over SPI cannot be trusted until after the tracking-loop swing-in. Depending on the tracking loop parameters (ω and δ) this can take tens or even hundreds of time frames (Ts).

Setting counters via SPI

It must be possible for the content of both counters to be set via SPI. This feature is necessary in case the counters loose their content, for example due to power loss.

If this happens, the ECU must be able to input correct values into the counters. These correct values are obtained by using a referencing sensor mounted on the steering wheel: each time when the steering wheel passes over "zero position" (steering angle is 0), the referencing sensor outputs a "zero position" signal.

It is possible for the steering wheel to pass the "zero position" when the number of full steering wheel rotations is "-1", "0", or "1". In each case, the referencing sensor outputs the same signal. The positions are distinguished by comparing the angular speeds of the front wheels: when driving straight on, both speeds are equal; when turning left or right, the speeds are different.

The ECU sends just one counter value to the "ATIC 116". However, as has been discussed above, the content of the two counters can be the same, or can differ by "1". This is due to the fact that the count-up point is different for each counter. Also, there may be some mismatch between the counters and the tracking loop.

For that reason, the low-power logic must be in the position to generate two correct values and assign them to the counters. This is done in accordance with the following algorithm:

Value adjustment for Counter 1

$0° \le \varphi < 180°$ AND S_{SM1}=3	$C_{adjusted} = C$
$0° \le \varphi < 90°$ AND S_{SM1}=1	$C_{adjusted} = C$
All other cases	$C_{adjusted} = C + 1$

Value adjustment for Counter 2

$180° \le \varphi \le 360°$ AND S_{SM2}=1	$C_{adjusted} = C + 1$
$270° \le \varphi \le 360°$ AND S_{SM2}=3	$C_{adjusted} = C + 1$
All other cases	$C_{adjusted} = C$

"φ"	angle from the tracking loop
"S_{SM1}"	state from state machine 1
"S_{SM2}"	state from state machine 2
"C"	counter value sent by the ECU
"$C_{adjusted}$"	value which is written into the counter.

NOTE:

When the counters are being set, the "ATIC 116" is in "R&R mode" and no tracking-loop calculation is performed. For that reason, the last available angle value (obtained just prior to switching from "burst mode" to "R&R mode") has to be taken.

The workflow during the counter setting procedure can be summarized as follows:

(1) Both state machines go to START state

(2) Both state machines go to state 0...3 depending on the current state delivered by D-FlipFlops

(3) Adjusted counter values are calculated as function of "φ and S_{SM1}" (counter1) or "φ and S_{SM2}" (counter2).

(4) New counter values are written into counters

(5) Auxiliary path resumes normal operation.

NOTE:

During the counter setting procedure, the following problem can occur: the signals "set.counter" and "count-up" (or "count-down") may appear at the same time; a retry of set.counter maybe necessary. See also Note on page 57.

Error detection and reporting

There are three errors in the auxiliary path which will be monitored and reported:

1) Counter mismatch error (error A)

2) State machine error of state machine 1 (error B1)

3) State machine error of state machine 2 (error B2)

Error A occurs when the difference between the two counters is larger then 1. Error B1 occurs when the state machine 1 enters the error state; error B2 occurs when the state machine 2 enters the error state. All three errors are combined to yield the "auxiliary-path error" (error #9 in the error table).

There are three internal error flags in the LP digital: one flag for each error. All three errors are continuously monitored in all modes: an occurrence of an error results in the corresponding internal error flag being set to HIGH. After being set to HIGH, the error flag will remain HIGH until the SPI command "reset.error" is executed.

Example of error handling

An example of counter error handling is shown in the diagram below.

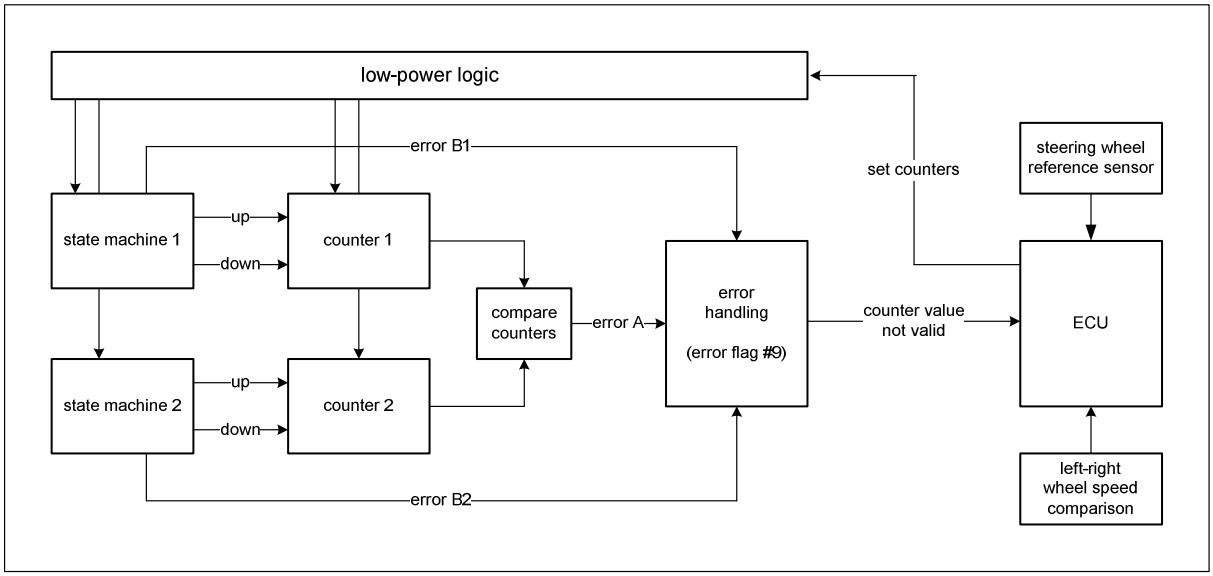


Figure 33: Counter error handling

There are two instances in which the counter error flag will be set to HIGH:

- counter error: see description below (error A)
- state machine error: one of the state machine enters "error state" (error B1 or B2)

The exemplary error handling is then executed as follows (counter error handling by ECU):

- while the error flag is set to HIGH, the counter content is declared "not valid"
- the ECU waits till the steering wheel reaches "zero position". This is detected by the steering wheel reference sensor
- when the steering wheel reaches "zero position", the ECU calculates the actual number of turns by comparing the rotation speeds of the left and right wheel of the car.
- the ECU writes the correct values to the counters using "set.counter". In the process, state machines are reset (see above)
- state machines resume their operation
- counter value is declared "valid"

Counter error:

The following counter values are valid: (a) counter1 = counter2, and (b) counter1 = counter2 + 1. All other combinations of counter values must result in error detection.

Actual counter AFE realization

In the figure below, the actual realization of the counter AFE is shown.

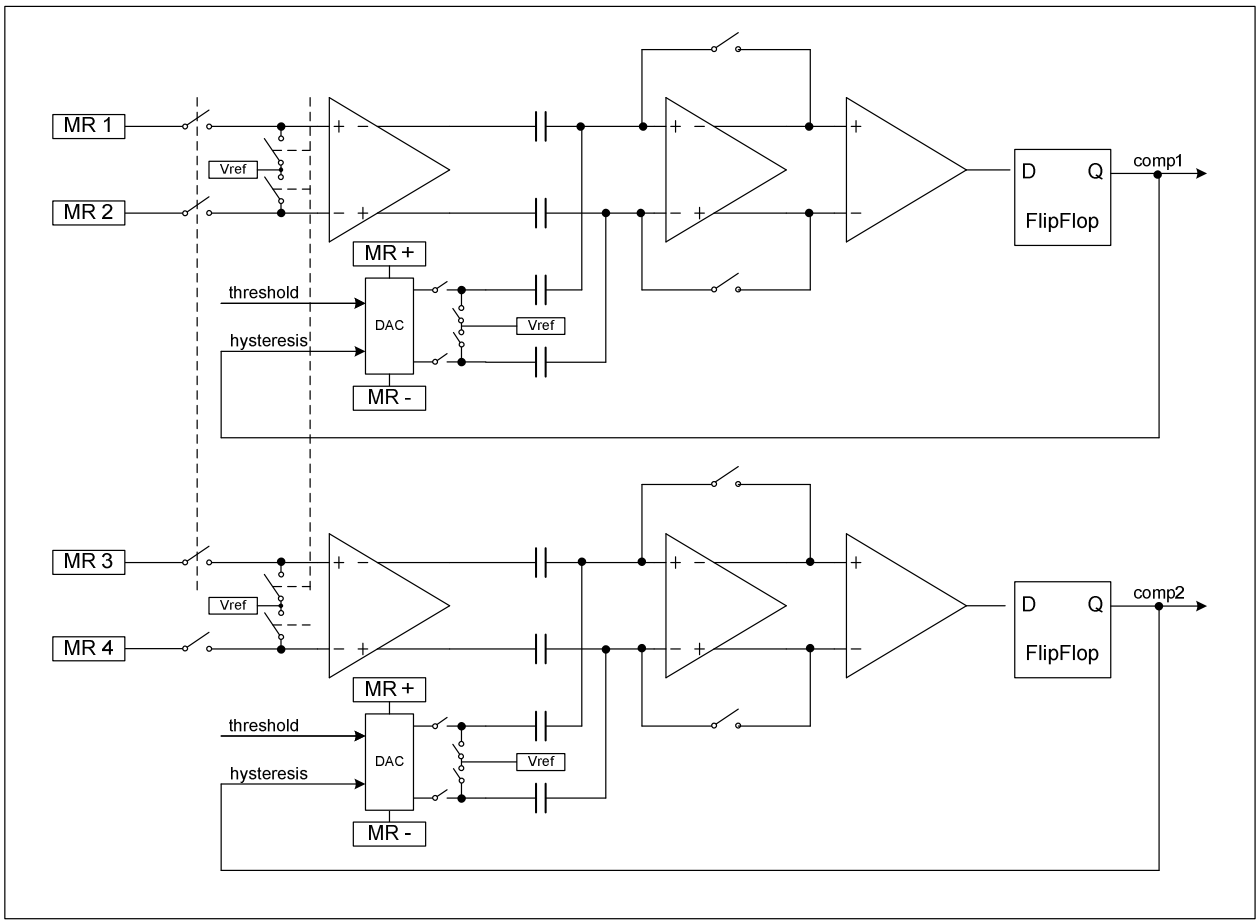


Figure 34: Counter AFE

The following features can be recognized:

- the amplifiers are fully differential and auto-zero
- the comparators are fully differential
- the MR bridge offset can be roughly compensated using an offset DAC; the DAC reference voltage is the same as the MR bridge supply voltage to achieve ratiometric behavior

The counter circuitry contains two identical AFEs: one AFE for each path.

Actual realization of counter-path digital circuitry

The actual realization of the digital part of the counter path is shown in the figure below.

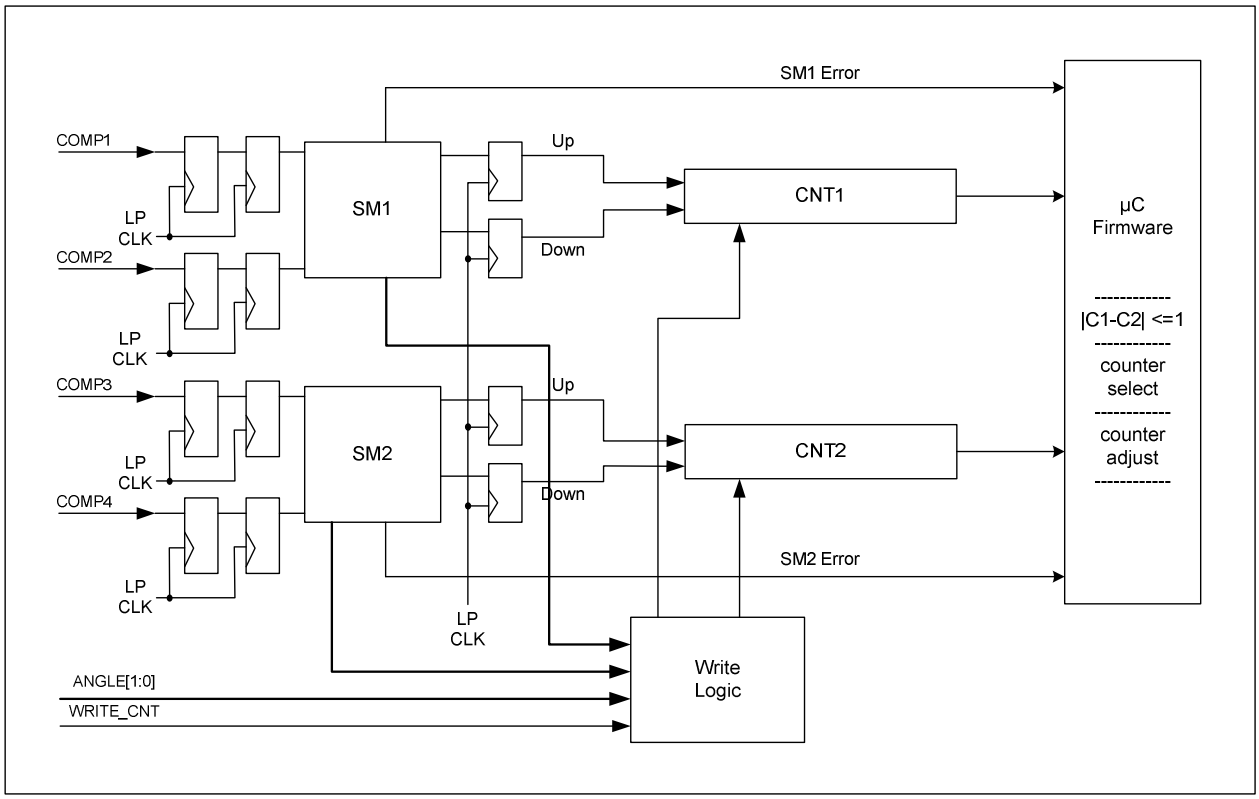


Figure 35: Counter-path digital circuitry

In the circuitry shown above, the following features can be recognized:

1) There are additional D-FlipFlops. Their function is the suppression of unstable and meta-stable states
2) The counter error detection is done in µC firmware
3) The adjustment of counter values during execution of "set.counter" is done in the digital circuitry (Write Logic)
4) The digital circuitry submits the value of both counters to the software. The functions "counter selection" and "counter adjust" are then done by the software.

Timing example

The figure below shows the timing for the "set.counter" procedure.

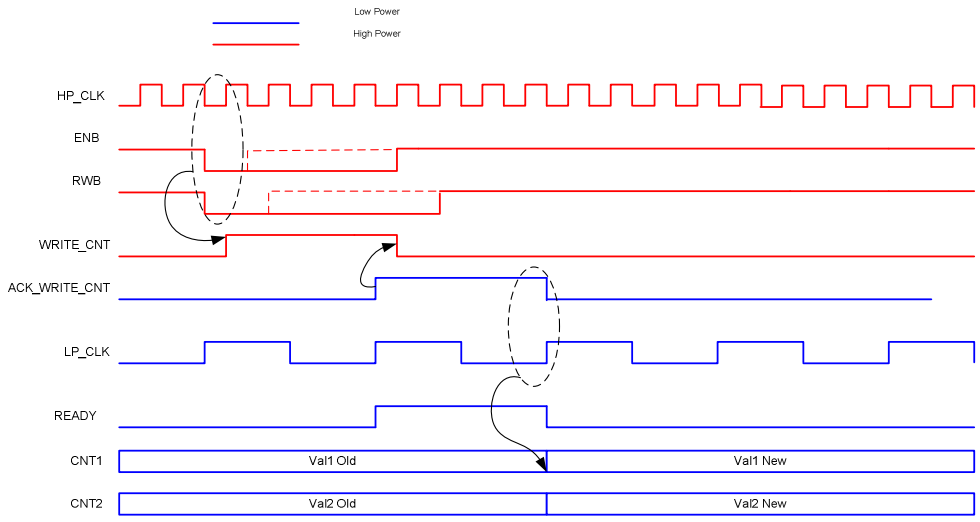


Figure 36: Timing diagram for "set.counter"

The following behavior can be recognized:

1) High-power logic generates the signal WRITE_CNT
2) High-power logic reads the new counter value and generates the signal ACK_WRITE_CNT. Only when this signal is generated, the high-power logic can release the signal WRITE_CNT.
3) The counter logic calculates two counter values (one value for counter1, and one value for counter2), and writes these values into the appropriate counters.

NOTE: *If an count event occurs during set.counter it is possible to have a counter mismatch error. The error will be detected no later then after one electrical period; in such a case a retry of set.counter is necessary.*

3.2.7 Redundant path

The redundant path consists of two amplifiers. These amplifiers gain the MR sensor output signals (sine and cosine) and output them as SIN and COS output signals. The amplifier inputs are fully differential; the amplifier outputs are single-ended, the output reference voltage is 1/2 * 3V3A

NOTE: Since the voltage OUTMR+ is virtually identical to 3VDA, the voltage OUTMR+ can be used as reference voltage for the analog single-ended output signals SIN and COS.

The redundant path is shown in the figure below

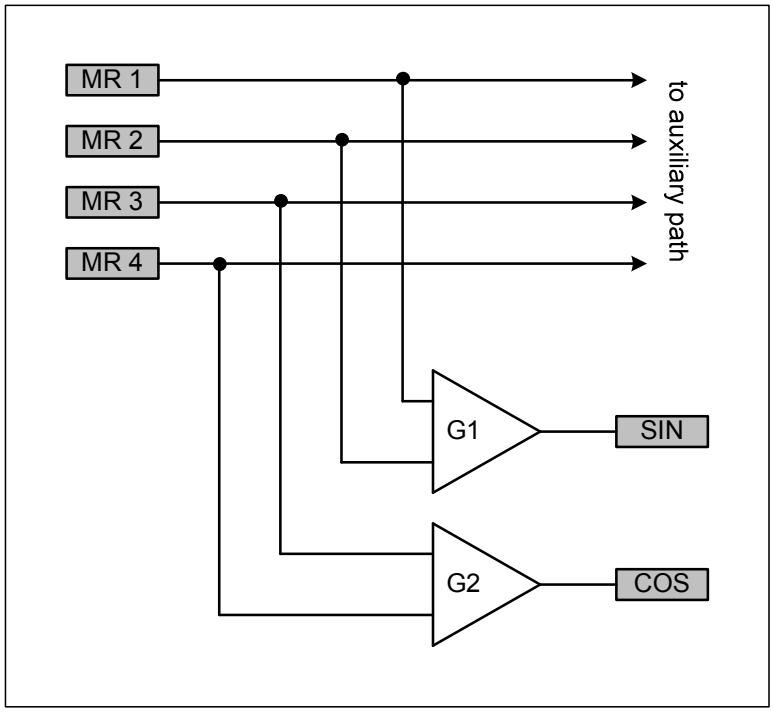


Figure 37: Redundant path

The signals from redundant path are used by the ECU to verify the speed and angle data delivered by the "ATIC 116". It means that the redundant path is safety-relevant. For that reason, the redundant path design must fulfill certain requirements such as:

- Different designer
- Different schematic
- Different power supply (different wire or separate track after bond pad)
- Different area on ASIC layout
- Different biasing circuit

3.2.8 Power loss detection (PLD)

During active mode, the "ATIC 116" supply voltage VDD will be in the range 4.75...5.25 Volts. Within this range, all three ASIC paths must be fully operational: main path, auxiliary path, and redundant path. (An exception here is the undervoltage case which is described below).

During chopping mode and low-power mode, the "ATIC 116" supply voltage can drop (e.g. due to battery cranking) down to 3.0 Volts. In these modes only the auxiliary path has to be operational.

Voltages lower than 3.0 Volts must be detected by the power-loss detection block (PLD). If a power loss is detected, the appropriate error bit is set to high.

To prevent PLD from erroneously reporting a power loss at voltages higher than or equal to 3.0 Volts, the power-loss detection voltage range has been specified to be 2.5...2.9 Volts.

It means that PLD will not detect a power loss for voltages higher than 2.9 Volts, but it certainly will detect power loss for voltages below 2.5 Volts.

The auxiliary path must stay operational at supply voltages down to 2.2 Volts. This is to prevent a situation in which the auxiliary path is not operational any more due to low voltage, but the failure is not yet detected by POR.

The supply voltage ranges are summarized in the table below

	voltage range (VDD)	unit	paths operational	comment
1	4.75...5.25	Volts	main; auxiliary; redundant	specified supply voltage during active mode
2	3.0...5.25	Volts	auxiliary	specified supply voltage during chopping mode and low-power mode
3	2.5...2.9	Volts	auxiliary	power-loss detection range
4	2.2...5.25	Volts	auxiliary	auxiliary path must be operational within this range

Table 7: Supply voltage ranges

NOTE 1: The auxiliary path must stay operational down to VDD= 2.2 Volts. However, VDD is first fed into the on-chip low-power voltage regulator to achieve stable supply voltage for the auxiliary path. Since some voltage drop is necessary for the regulator to work properly, the actual supply voltage for the auxiliary path will be lower then VDD = 2.2V specified above.

NOTE 2: The PLD circuit must not detect and report very short supply voltage outages (0...5 µs); the auxiliary path must remain operational during such events (supply voltage outage is an event during which VDD falls below 3.0 Volts).

3.2.9 Power-on Reset (POR)

The power-on reset block (POR) monitors the "ATIC 116" supply voltages and determines if they are high enough for the high-power circuitry (analog and digital) and low-power circuitry (digital) to work properly.

As long as LPVDD remains too low for the low-power digital circuitry, a reset signal for the low-power digital circuitry (LPPORB) is being generated. In this way, the low-power digital circuitry is prevented from working.

As long as the 3V3D remains too low for the high-power circuitry, a reset signal for the high-power digital circuitry (LPPORB) is being generated. In this way, the high-power digital circuitry is prevented from working.

The switch from "reset" (voltage too low) to "no reset" (voltage high enough) takes place within a voltage range limited by two thresholds: low threshold and high threshold.

The POR block shows a hysteresis. It means that the low and high thresholds will be different for rising voltages and falling voltages.

The reset pin will be coupled to both low-power and high-power reset signals so that the ECU driving that reset pin can force a full reset of the IC without turning off and on again the supply.

The LPPOR resets the complete low-power logic whereas the HPPOR resets the complete high-power logic. The external reset resets the low-power and the high-power logic.

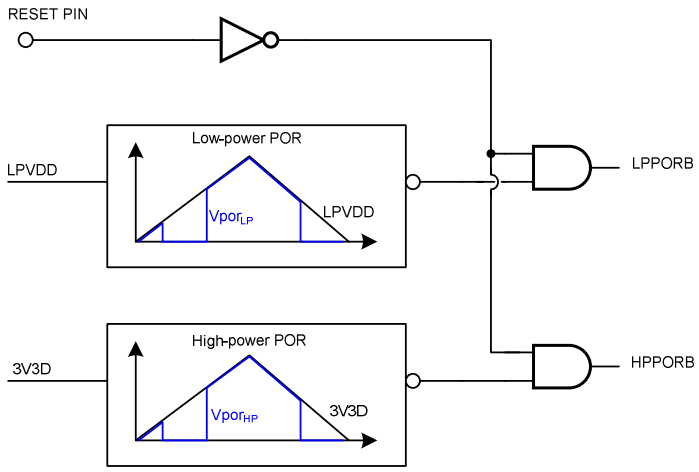


Figure 38: POR and RESET

3.2.10 Undervoltage case

During active mode, the supply voltage VDD must be within the range 4.75...5.25 Volts to ensure full functionality of "ATIC 116" (measurement of speed and angle, counter, SPI communication). It can happen, however, that VDD will temporarily drop down to 3.0 Volts, and then recover to 4.75...5.25 Volts. This is called "undervoltage case".

The ASIC must be able to detect the occurrence of such undervoltage case, and respond accordingly. In particular:

1) Upon detection of undervoltage case, the ASIC transitions from "active mode" to "low-power mode"
2) Upon transition from active mode into low-power mode, the measurement of speed and angle, and the SPI communication with ECU are discontinued; the turn counting is continued without interruption.
3) When VDD recovers to 4.75...5.25, the ASIC reboots into active mode (R&R mode); by sending "set.burst" command it is possible to resume normal burst-mode operation
4) The ASIC must continue proper active-mode operation (speed and angle, turn counting, SPI communication) until undervoltage case is detected and ASIC enters low-power mode

3.2.11 Sensor errors

The output signals of an ideal MR bridge can be described using the following equations:

$$V_{OUT}^{1} = V_{\max} \cdot \sin(\alpha) \qquad V_{OUT}^{2} = V_{\max} \cdot \cos(\alpha)$$

The behavior of a real MR bridge, however, will differ from the ideal behavior described above. The MR bridge errors include:

- sensitivity error
- sensitivity mismatch error
- offset error
- excentricity error
- orthogonality error

Sensitivity error

The sine and cosine amplitude of an ideal MR bridge can be designated as A0. The amplitude of a real MR bridge can be different than A0, though. There are several reasons for this:

- intrinsic sensitivity error at T = 25°C: the MR bridge delivers output signals whose amplitude differs from the ideal amplitude A0.
- sensitivity temperature drift: the amplitude of the output signals can change with temperature
- sensitivity life-time drift: the amplitude of the output signals can change during life time

This is visualized in the figure below. Both the ideal and the real amplitude are shown.

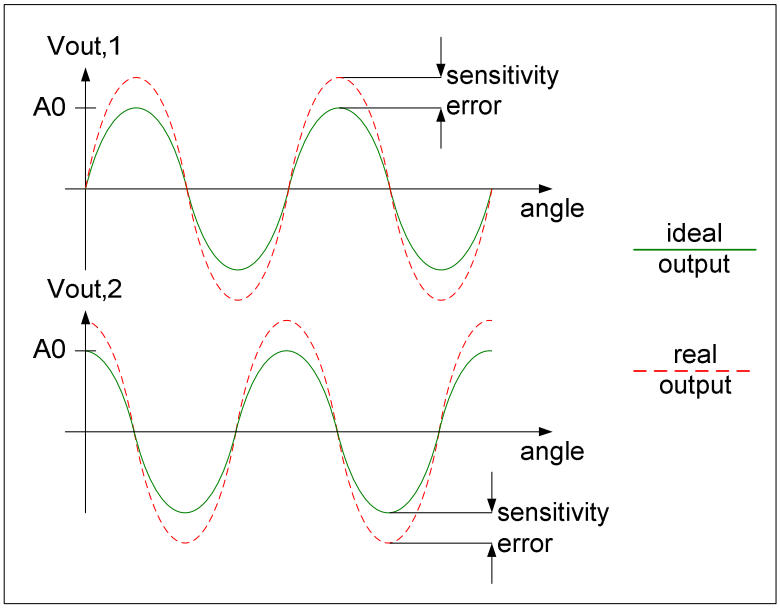


Figure 39: Sensitivity error

Sensitivity mismatch error

So far, it has been implicitly assumed that the amplitude of the sine and cosine signals is the same. In a real sensor, however, they can differ from each other. This is referred to as sensitivity mismatch error and is visualized in the figure below.

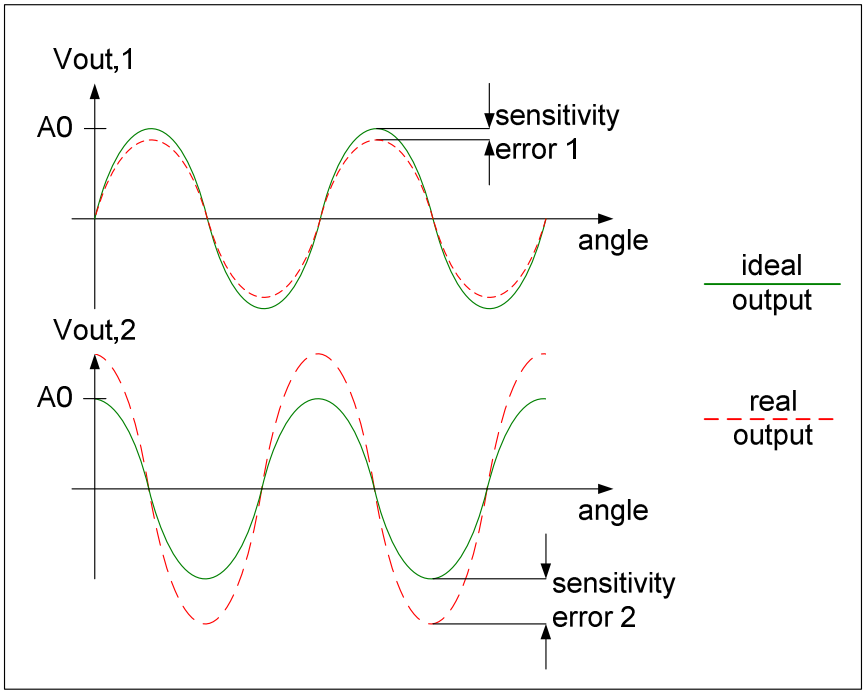


Figure 40: Sensitivity mismatch error

Offset error

There can be some DC offset superimposed upon the sine and cosine signals. This is shown in the next figure

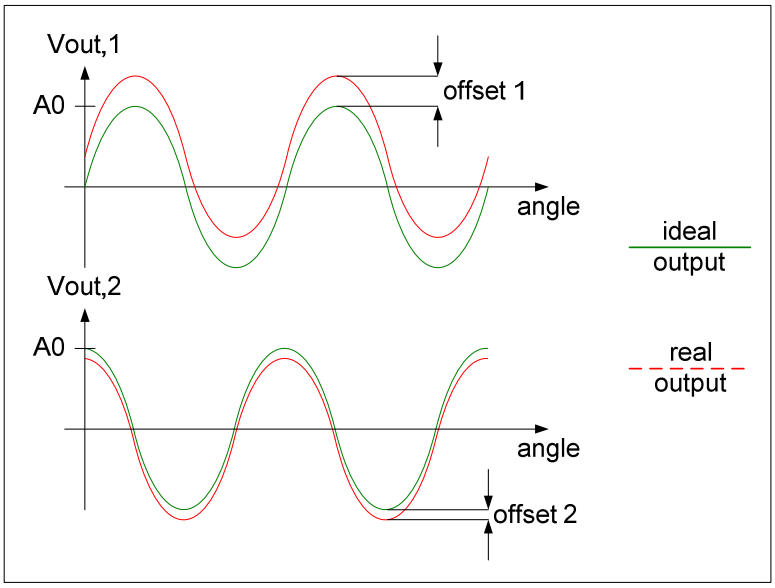


Figure 41: Offset error

Note that the offset error can be different for each channel.

3.2.12 Sensor output signals

The sensor output signals can be expressed as:

$$V_{OUT}^{1} = V_{\max}^{1} \cdot \sin(\alpha) + offset_1 \qquad V_{OUT}^{2} = V_{\max}^{2} \cdot \cos(\alpha) + offset_2$$

Amplitude Vmax and sensor offset will change with the supply voltage Vdd and temperature (Vdd here is the voltage applied to the MR bridge, not the supply voltage of the "ATIC 116" itself). They can be expressed as follows (the result is in mV):

$$A = f(V_{DD}, T) = [C_A V_{DD}] \cdot \left[1 + \frac{TC_A}{100}(T - T_0)\right]$$

$$offset = f(V_{DD}, T) = \left[C_{offset} + \frac{TC_{offset}}{1000}(T - T_0)\right] V_{DD}$$

where:

C_A:	coefficient of amplitude
TC_A:	temperature coefficient of amplitude
C_{offset}:	coefficient of offset
TC_{offset}:	temperature coefficient of offset

The values of the coefficients can be different for the sine and cosine channel. This is the reason for mismatch errors discussed above. The parameter ranges (for the Sensitec sensor) are shown in the table below:

		min	typical	max	unit	comment
C_amplitude	coefficient of amplitude *)	+/-12		+/-14	mV / V	at RT
TC_amplitude	temp coefficient of amplitude	-0,31	-0.35	-0,39	% / K	as % of amplitude at RT
C_offset	coefficient of offset	-2	0	2	mV / V	at RT
TC_offset	temp coeficient of offset	-2	0	2	(uV/V) / K	
k	amplitude synchronism	99.5	100	100.5	%	at RT
TC_k	temp coefficient of k	-0.01	0	0.01	% / K	not specified by Sensor Supplier
CM_voltage	Half bridge to MR-	45		55	% of bridge supply	at all temperatures

Table 8: Sensor parameters

NOTE: the parameter TC_amplitude (temperature coefficient of amplitude) is given as percent value of the sensor's amplitude at room T=25°C.

The parameter "k" (amplitude synchronicity) describes how much the two amplitudes (A1 and A2) can differ from each other. It is defined as k = 100 * (A1/A2). A short calculation yields the following values (Vsupp = 3,3 V)

parameter	value	unit	comment
A_max	46.2	mV	T = 25°C
A_max	57.91	mV	T = -40°C
A_min	39.6	mV	T = 25°C
A_min	21.84	mV	T = 140°C
offset_max	6.6	mV	T = 25°C
offset_max	7.36	mV	T = 140°C

Table 9: MR bridge amplitude and offset

In addition to the sensor offset described by the parameters C_offset and TC_offset, a life-time drift of the sensor offset can be expected. A realistic value by which the sensor offset parameter C_offset might change over life time is 2mV (1500h HTOL). Observed angle drifts over lifetime (1500h HTOL) are in the range of < 2° electrical (compensated via dynamic compensation).

parameter	value	unit	comment
signal max	69.23	mV	A_max + offset_max + life-time drift; MR+ = 3.3 V; T =-40°C
signal min	10.52	mV	A_min - offset_max – life-time drift; MR+ = 3.3 V; T = 140°C

Table 10: MR bridge max and min signals

This calculation gives fairly good estimates of the signals values which can be expected. This information can be used e.g. for dimensioning of devices like amplifier stages or ADC converters. This calculation does not take into account such effects as excentricity error.

3.2.13 Mechanical errors

Mechanical errors stem from positioning tolerances of the MR bridge with respect to the magnet. The sources of these tolerances are:

- positioning of the MR bridge within the "ATIC 116" package
- positioning of the "ATIC 116" package on the PCB
- positioning of the PCB and magnet in the module group

Excentricity error

Ideally, the magnet rotation axis goes exactly through the middle of the MR bridge. Any displacement from the ideal position will result in measurement error. Such a displacement is shown in the figure below. On the left, the ideal position can be seen, and on the right, the magnet center is displaced.

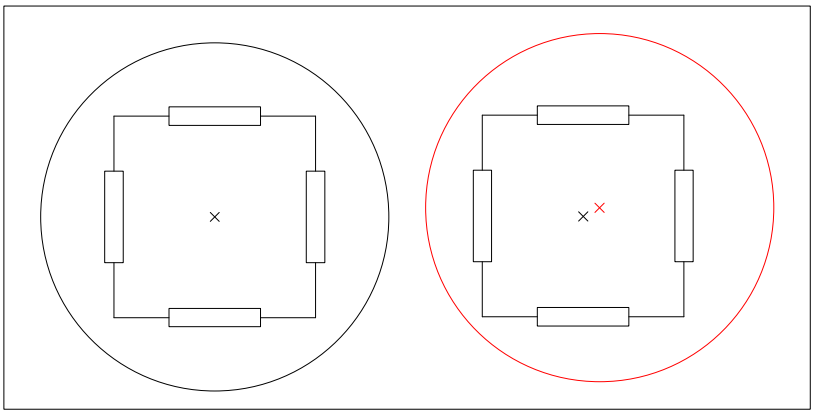


Figure 42: Excentricity error

The excentricity error results in a misshaping of the sine and cosine signals; the resulting angle error is identical to an angle error caused by a sensor offset error. For that reason an excentricity error can be compensated by introducing an additional offset error of the opposite sign.

It is not possible to measure the excentricity error using the "ATIC 116" alone, since the excentricity error depends on the position of the magnet with respect to the "ATIC 116". This error can only be measured after the "ATIC 116" has been placed in the module group.

3.2.14 Sensor error compensation

. There will be three kinds of sensor error compensation:

- static compensation
- dynamic compensation
- excentricity error compensation

In the figure below, the entire compensation chain is shown.

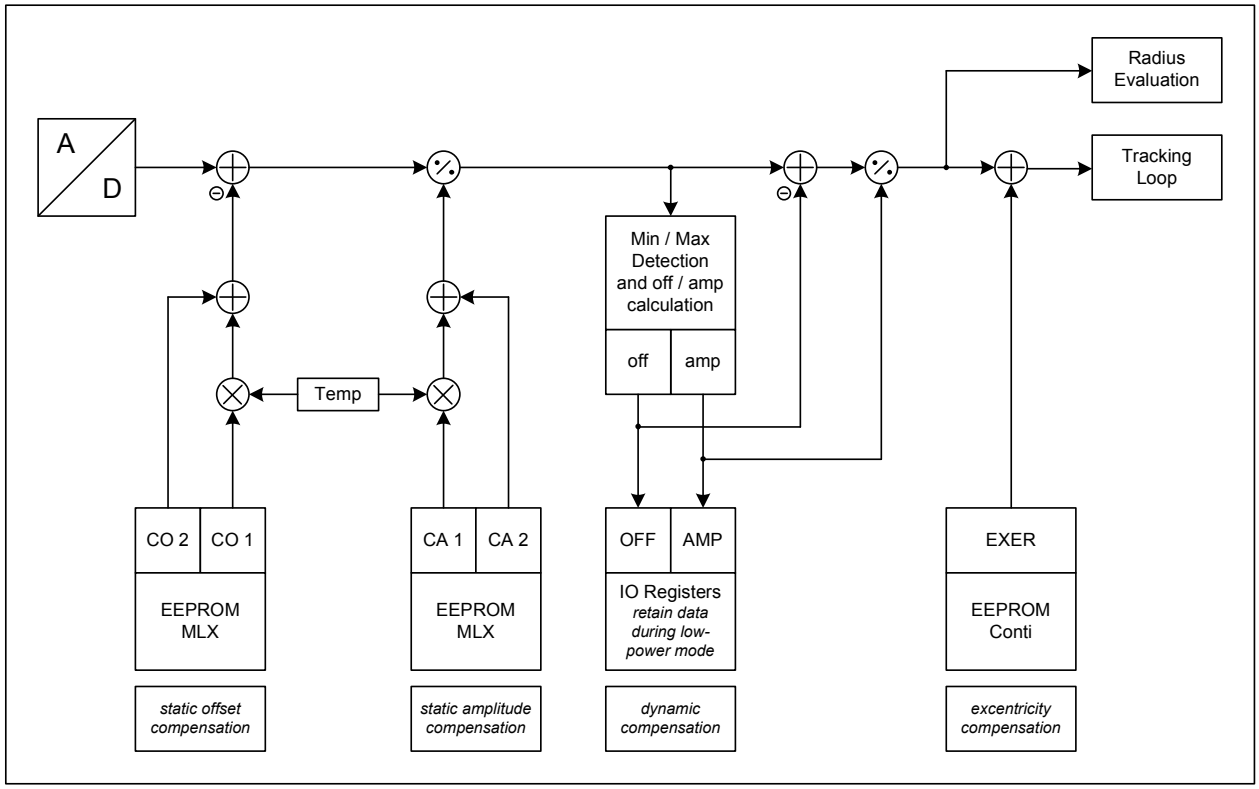


Figure 43: Sensor error compensation

NOTE 1:

The value of "Temp" does not have to be in Celsius or Kelvin. It is enough for the on-chip temperature sensor to provide temperature in arbitrary units (digits) if:

a) the temperature sensor used during sensor calibration is the same as the temperature sensor used during "ATIC 116" operation

b) the linearity error and repeatability error combined do not exceed a value specified in the section "Parameters"

NOTE 2:

The "Radius Evaluation" block shown in the figure above is part of the "ATIC 116" diagnosis functionality and will be described later.

NOTE 3:

The diagram above shows the basic functionality of error compensation. For technical reasons the actual implementation – in particular the storage of OFF and AMP parameters of the dynamic compensation – will be slightly different; it will be described in more detail below.

Static compensation

As has been seen above, the MR bridge output signals will have temperature-dependent amplitude and offset errors. These errors can be compensated using the following equations:

$$A_{compensated} = \frac{A_{uncompensated} - offset(T)}{A(T)}$$

with:

$$A(T) = CA_2 + CA_1 \cdot Temp\,; \qquad offset(T) = CO_2 + CO_1 \cdot Temp$$

where:

CA1: Temperature-related coefficient of amplitude

CA2: Non-temperature-related coefficient of amplitude

CO1: Temperature-related coefficient of offset

CO2: Non-temperature-related coefficient of offset

The compensated values (A_compensated) will ideally be in the interval [-1; 1] which is consistent with values of sine and cosine functions. The coefficients above (CA1, CA2, CO1, CO2) will be obtained during sensor calibration process described below.

NOTE 1:

The coefficients above (CA1, CA2, CO1, CO2) are not the same as the coefficients used in chapter "Sensor output signals" (C_A, TC_A, C_offset, TC_offset). However, their information content is identical as one set of coefficients can be derived from the other set.

NOTE 2:

In the actual firmware implementation, the input value A_uncompensated will not be divided by A(T), but it will be multiplied by the inverse value 1 / A(T).

Dynamic compensation

Both amplitude and offset error of the sensor will be subject to life-time drift. Since the magnitude of the life-time drift is not known in advance, it will be necessary to implement a dynamic scheme capable of compensating the varying life-time drift.

In this dynamic compensation, the parameters "OFF" (for offset) and "AMP (for amplitude) will be determined via evaluation of sensor output signals during "ATIC 116" active mode. This will be done in the following way:

Values of the sensor offset and amplitude error can be estimated if the MIN and MAX values of the output signals are known:

$$OFF = \frac{1}{2}(MAX - MIN) \qquad AMP = MAX - MIN$$

The following procedure for determining MAX and MIN is implemented:

1) After completion of two full electric periods, the values MAX1 and MIN1 are obtained. This action is then repeated twice, and values MAX2, MIN2, MAX3, and MIN3 are obtained. In this way the arrays MAX[] and MIN[] are generated, each array with three elements

2) In the arrays MAX[] and MIN[] the highest and lowest values are discarded; the remaining medium values MAX and MIN are retained and declared valid

3) Once MAX and MIN values are declared valid, they are used to calculate OFF (sensor offset) and AMP (sensor amplitude); see also equations above. The parameters OFF and AMP are then declared valid, too.

4) Valid parameters OFF and AMP are used for dynamic compensation of sensor signals

5) Steps 1...3 are repeated. Once new valid OFF and AMP values are calculated, the old values are discarded and the new values are used instead.

The parameters OFF and AMP are also stored in the ASIC's IO registers (which retain their value during low-power mode) so that they are available immediately after Wake-up.

NOTE 3:

To prevent one-time events from distorting the dynamic compensation, the following measure will be implemented: the maximum values for dynamic compensation of offset and amplitude will be limited to the following values:

amplitude:	5% of the ideal amplitude of 0x4000
offset:	10% of the ideal amplitude of 0x4000

The reasoning behind this measure is this: coarse compensation has already been achieved by static compensation; the function of dynamic compensation is fine-tuning, thus no large changes can be expected.

Calibmode

The calculation of dynamic compensation parameters OFF and MAX can be enabled or disabled. This is done by setting the calibmode flag in EEPROM, address 0x2052.

Calibmode[15] = 1 ==> calculation disabled

Calibmode[15] = 0 ==> calculation enabled

If Calibmode[15] = 1 (calculation disabled) then the dynamic compensation is executed with the last values of OFF and AMP which were declared valid; if no values for OFF and AMP are declared valid (for example after Power-up), then the dynamic compensation is executed with OFF=0 and AMP=1.

If the status of Calibmode[15] is changed, the change only becomes active after the next Wake-Up.

Default value of Calibmode[15] is 0x0 before "ATIC 116" is delivered to Continental.

Sensor error compensation schemes

The following compensation schemes can be distinguished:

1) "ATIC 116" is in active mode: MIN and MAX values are already calculated and declared valid
2) "ATIC 116" is in active mode immediately after wake-up: new MIN and MAX values are not yet calculated and declared valid
3) "ATIC 116" is in active mode immediately after Power-up: MIN and MAX values are not yet declared valid, and the "OFF" and "AMP" parameters stored in the ASIC's IO registers are lost.

Compensation scheme #1

In this scheme, the "OFF" and "AMP" parameters delivered by the "Min / Max detection" block will be used for compensation.

Compensation scheme #2

In this scheme, the "OFF" and "AMP" parameters stored in the ASIC's IO registers will be used for compensation.

Compensation scheme #3

In this scheme, the "OFF" and "AMP" parameters will have the values OFF=0 and AMP=1 until new OFF and AMP values are calculated and declared valid.

Actual implementation of the dynamic compensation

In the description above the functionality of the dynamic compensation is discussed. The actual implementation is slightly different and is shown in the diagram below.

The difference is: in the ASIC's IO registers the intermediate values MAX and MIN are stored, and not the final values OFF and AMP. The final OFF and AMP values are stored in ASIC's RAM registers.

In case of a Wake-up the OFF and MAX values are initialized in a first step to their default values (OFF=0, AMP=1); If dynamic compensation is activated (Calibmode[15]=0) the actual values for OFF and AMP are then calculated from the stored MAX/MIN values in the ASIC's IO register.

In case of a Power-up event the intermediate values MAX and MIN in the IO registers as well as the OFF and AMP values in the ASIC's RAM registers are initialized to their default values.

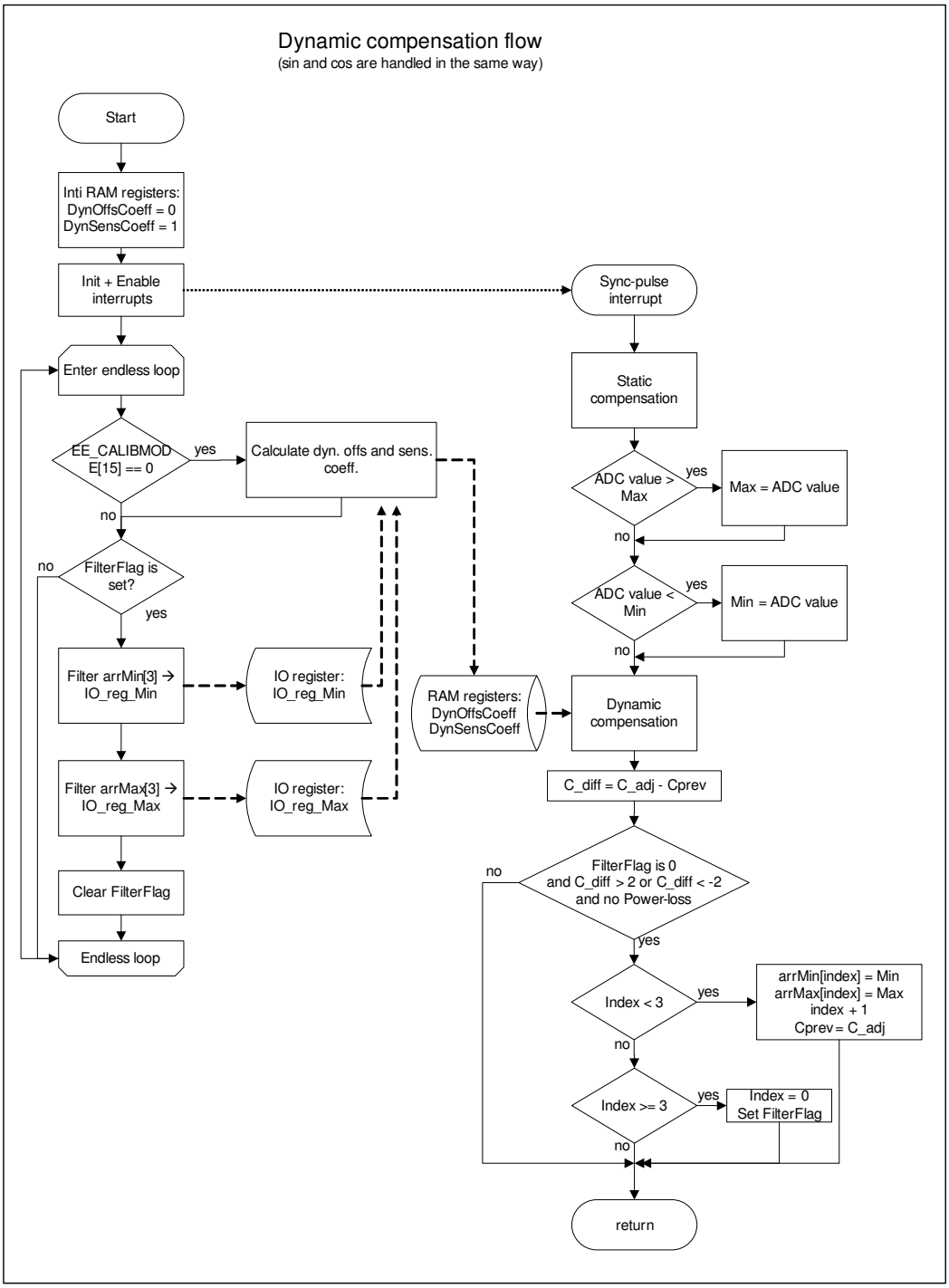


Figure 44: Actual implementation of the dynamic compensation

Document version	Previous version	Change description (including number)
Rev A		

Designed by	Date	Department	
Author: O. Zappa/ S. Haimerl	03/12/2009	S&T A IC	
Released by	Date	Department	
Author			

Designation		Status
ATIC116 **Rotational speed and position sensor**		
Documentkey		Pages
A2C00046207		71 of 162

Excentricity compensation

The excentricity error has been described above. This error shows the same pattern as the offset error. Thus it is possible for the excentricity error to be eliminated by introducing an artificial offset EXER (Excentricity Error). The parameter EXER will be determined during module calibration, see also chapter “Sensor calibration, calibration by customer”.

NOTE:

All three compensation steps described above refer to one channel only. In the "ATIC 116", however, the compensation will have to be performed independently for both channels (sine *and* cosine). It also means that all compensation parameters (CA1, CA2, CO1, CO2, EXER) will have to be independently stored for both channels, thus yielding 10 compensation parameters.

Compensation overview

In the diagram below, the entire compensation scheme (without radius evaluation) is shown again.

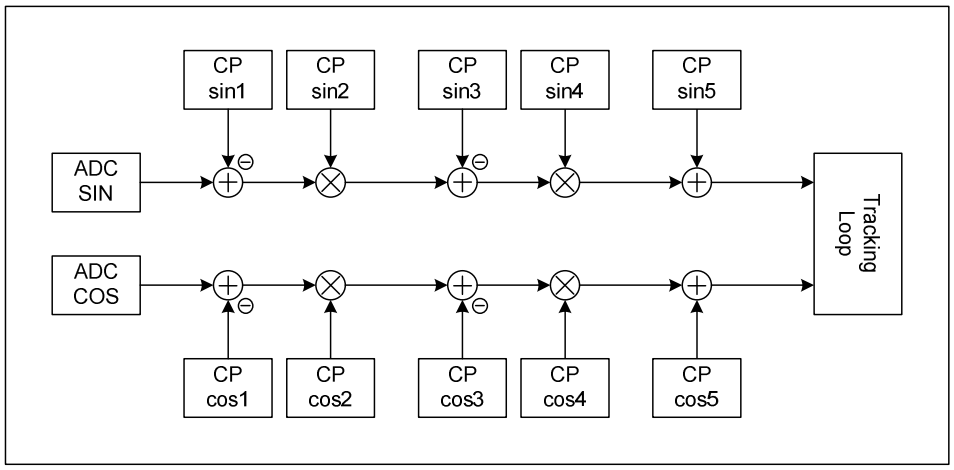


Figure 45: Sensor error compensation overview

The compensation parameters (CP) used in the compensation are explained below.

Value	Description
CP 1	static offset compensation
CP 2	static sensitivity conpensation
CP 3	dynamic offset compensation
CP 4	dynamic sensitivity compensation
CP 5	excentricity compensation

Table 11: Compensation parameters

For each channel (SIN and COS), there are 5 independent compensation parameters.

Introduction of real-time and background:

The compensation itself has to be performed with every Sync signal. But the compensation parameters do not have to be updated with every Sync signal, a much slower update rate will be enough. For that reason, it is possible to divide all compensation tasks into two groups:

(a) Real-time tasks, which are calculated at an update rate of sync frequency

(b) Background tasks, which are calculated at a lower update rate.

This concept will be discussed in more detail below.

3.2.15 Real-time and background loops

In burst mode several tasks have to be performed once with every Sync pulse. Other tasks do not have to be performed so fast; it is enough if they are performed at a much lower update rate. This is the reason for the introduction of:

(a) Real-time loop

(b) Background loop

On every Sync-pulse, depending on the mode (Request & Response- or Burst-mode) the background-loop is halted and an event is triggered. If the ASIC is in R&R-mode, an SPI-interrupt is received and the request is handled. If the chip is in Burst-mode, then the SYNC-pulse:

1. starts a Sample&Hold
2. converts sin & cos
3. if sin & cos are converted an Analog Front End-interrupt (AFE) is generated
4. upon this interrupt the firmware will execute the Real-Time loop

After the real-time function the firmware will return to the halted background-loop and continue it's execution.

The real-time loop contains the following tasks (S&H and ADC conversion before the real-time-loop):

a) Sensor error compensation (static and dynamic)

b) Tracking loop (speed and angle)

c) Calculation of DATA telegrams

d) Diagnosis (fast errors)

e) End of realtime-loop and return

All other tasks are done in the background loop. In particular, the calculation of dynamic compensation parameters is included here.

Real-time diagnosis tasks

There are four fast errors whose diagnosis is performed in the real-time loop. However, the time slot in the real-time loop available for diagnosis is not long enough for all four errors.

For that reason, the fast error diagnosis is divided into 8 tasks: two tasks for each error. Each time when the real-time loop is executed, one task is inserted into the available time slot and executed. It means that after the real-time loop has been executed 8 times, the diagnosis of all four fast errors has been executed once. This is visualized in the next diagram for task 1 and 2 out of these 8 tasks.

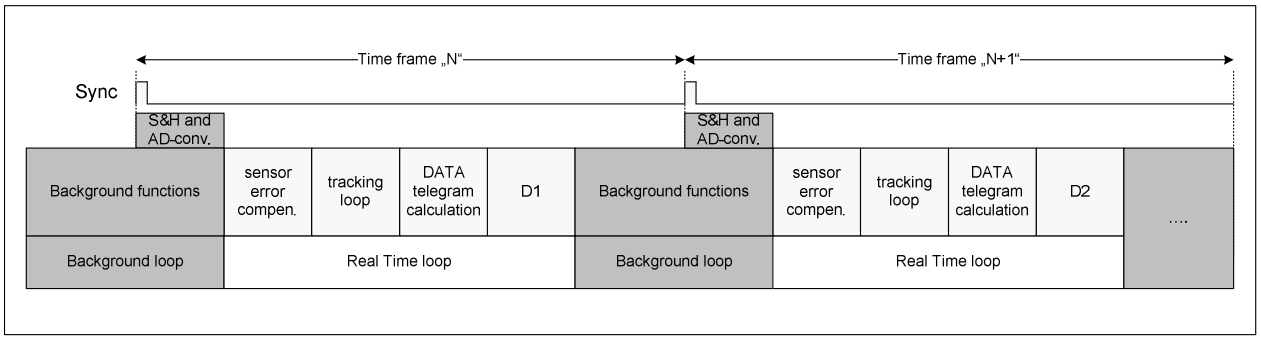


Figure 46: Real-time loop embedded into the background loop, with diagnosis tasks

One consequence of the real-time loop being embedded into the background loop is that if the Sync update rate is reduced (for example, from 100µs to 125 µs) then the update rate of the background loop will increase.

3.2.16 Sensor calibration

It has been shown in the last chapter that for the compensation to be performed, the following sensor parameters must be known:

(1)	CA_1	temperature-related coefficient of amplitude
(2)	CA_2	non-temperature-related coefficient of temperature
(3)	CO_1	temperature-related coefficient of offset
(4)	CO_2	non-temperature-related coefficient of offset
(5)	$EXER$	artificial offset for excentricity error compensation

These parameters will be obtained during sensor calibration. The parameters 1, 2, 3, 4 will be obtained during calibration by supplier ("ATIC 116" calibration), and the parameter EXER will be obtained during calibration by customer (module calibration).

Calibration by Supplier

This step is done before the "ATIC 116" is mounted into the module group. The "ATIC 116" will be placed into an appropriate calibration set-up and exposed to rotating magnetic field and changing temperatures. At the same time, the output signals will be taken. The parameters 1, 2, 3, 4 will then be determined.

The calibration will be done by the supplier. The supplier will also be responsible for developing an appropriate calibration algorithm. The accuracy with which the calibration parameters are obtained must be such that after amplitude and offset error compensation, the remaining error does not exceed the error budget specified in the section "parameters" over the full temperature, voltage and lifetime range.

Calibration by Customer

This step is done after the "ATIC 116" is mounted into the module group. The module's magnet is rotated to create a rotating magnetic field, and the sensor output signals are taken. In the process, the module group is exposed to one temperature only (room temperature). The parameter EXER will be then determined.

This calibration step will be done by the customer.

3.2.17 ATIC116 diagnosis

Error detection

The "ATIC 116" will be monitored during its operation. Several functions and conditions will be selected for monitoring, and whenever mal-function or mal-condition is detected, the corresponding error flag will be set to HIGH. The functions to be monitored can be assigned numbers (form 0 to "n"), which results in "n+1" error flags

Remark: function is e.g. analog-to-digital conversion carried out by the ADC; condition is e.g. the supply voltage 3V3A or 3V3D

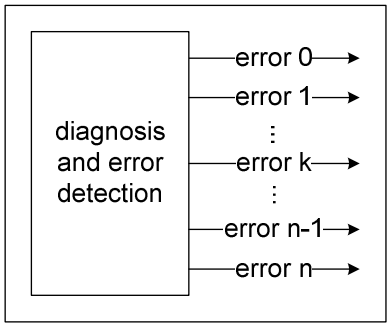


Figure 47: Error flags

The diagnosis function is executed with a repetition rate of once every 8 Sync pulses. It means that for every diagnosable error, every 8 Sync pulses new diagnosis result is obtained. This result can have two values:

0: no error detected

1: error detected

Error debouncing

The classic approach is that once an error is detected, the corresponding error flag is set to HIGH, and appropriate system response (error handling) is initiated.

This approach has one disadvantage: the error handling may prove to be over-sensitive. Many false signals do not stem from "ATIC 116" malfunction, but are caused by one-time events like EMC disturbance. When using the classic approach, however, such one-time events are interpreted as "ATIC 116" errors and lead to the corresponding error handling. This is neither necessary nor desired.

One way to eliminate this over-sensitivity is called "error debouncing". The basic principle is that an error must occur several times before the corresponding flag is set to HIGH. The debouncing is performed using a counter shown below:

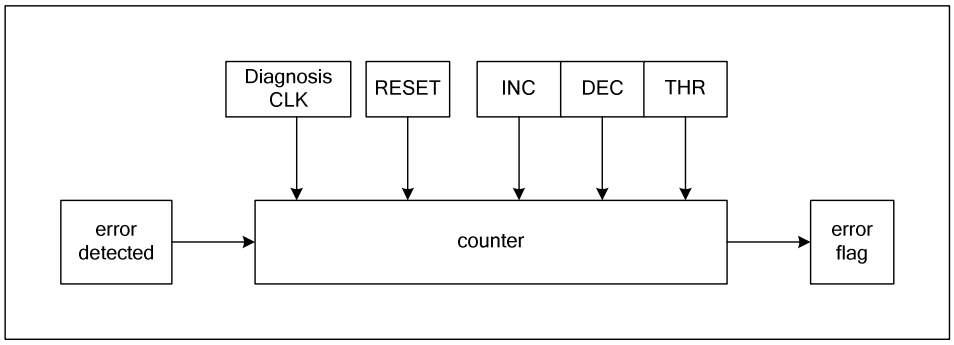


Figure 48: Error counter

There is one counter for each error, the default value is 0 (zero). Each time when an error is detected, the corresponding error counter goes up by value determined by INC. Each time when the error is not detected, the counter content goes down by value determined by DEC.

The counter value is clipped. The upper clipping value is the threshold (THR), the lower clipping value is 0 (zero). This is shown in the diagram below.

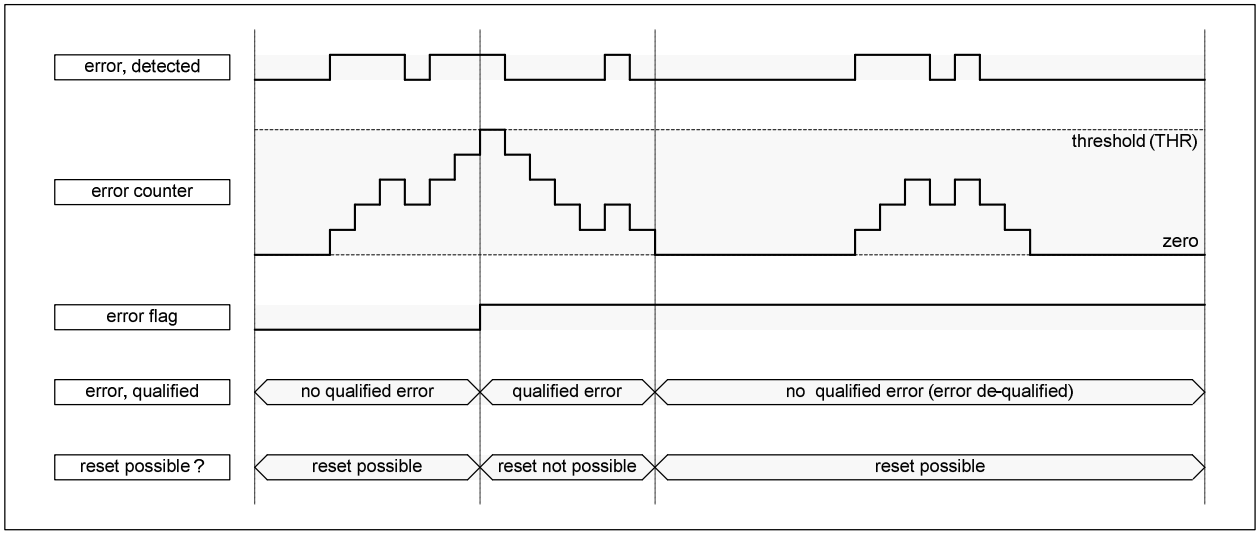


Figure 49: Error debouncing

Qualified errors and de-qualified errors

An error becomes "qualified" (which means that the error is regarded as "present") only if the error occurrence was frequent enough to cause the error counter reach the threshold value THR. If en error becomes "qualified", the corresponding error flag is set to HIGH.

Once an error is "qualified", it remains "qualified". It becomes "de-qualified" (which means the error is regarded as "not present") only after the error counter has reached the "zero" value again. Even then, the error flag is not set to LOW, it remains HIGH. Only an adequate SPI command can reset the error flag.

Resetting the error

The error flag can be reset only by the SPI command "reset.error". When this command is executed, the following points are observed:

- only the error flag is reset, the content of the error counter remains unchanged
- resetting is only possible if the error is not "qualified". If the error is "qualified", then the error flag is not reset, even if "reset.error" command is sent by the ECU
- resetting is possible even if the value of the error counter is different from "zero", as long as the error is not "qualified"

Debouncing parameters in EEPROM

The parameters INC, DEC, and THR are stored in EEPROM. However, to save storage place, they are stored as EE_INC (3 bit), EE_DEC (1 bit), and EE_K (4 bit). The actual parameters are then calculated as follows:

```
INC = EE_INC[2:0] + 1
DEC = EE_DEC[0] + 1
THR = INC * (EE_K[3:0] + 1)
```

Example: if the EEPROM parameters have the following values:

```
EE_INC[2:0] = 011  (binary) = 3 (decimal)
EE_DEC[0]   = 1    (binary) = 1 (decimal)
EE_K[4:0]   = 0110 (binary) = 6 (decimal)
```

Then the actual debouncing parameters are calculated as follows:

```
INC = 3 + 1 = 4
DEC = 1 + 1 = 2
THR = 4 * (6 + 1) = 4 * 7 = 28
```

It means that each time when the error is detected, the error counter is increased by 4; each time the error is not detected, the error counter is decreased by 2. When error counter reaches 28, the error is declared "qualified" and the appropriate error flag is set.

There are three errors upon which debouncing will be performed: error # 23, #19, and #9. It means that there are three different sets of INC, DEC, and THR debouncing parameters. They are stored in EEPROM in the following way:

EEPROM 0x204E		EEPROM 0x2050	
BIT [15]	K_9 [3]	BIT [15]	not used
BIT [14]	K_9 [2]	BIT [14]	not used
BIT [13]	K_9 [1]	BIT [13]	not used
BIT [12]	K_9 [0]	BIT [12]	not used
BIT [11]	INC_9 [2]	BIT [11]	not used
BIT [10]	INC_9 [1]	BIT [10]	not used
BIT [9]	INC_9 [0]	BIT [9]	not used
BIT [8]	DEC_9 [0]	BIT [8]	not used
BIT [7]	K_23 [3]	BIT [7]	K_19 [3]
BIT [6]	K_23 [2]	BIT [6]	K_19 [2]
BIT [5]	K_23 [1]	BIT [5]	K_19 [1]
BIT [4]	K_23 [0]	BIT [4]	K_19 [0]
BIT [3]	INC_23 [2]	BIT [3]	INC_19 [2]
BIT [2]	INC_23 [1]	BIT [2]	INC_19 [1]
BIT [1]	INC_23 [0]	BIT [1]	INC_19 [0]
BIT [0]	DEC_23 [0]	BIT [0]	DEC_19 [0]

Table 12: Debouncing parameters in EEPROM

Error classes and codes

All errors are divided into three severity classes: high, medium, and low. In burst mode, only the classes of flagged errors are sent to the ECU (using a 3-bit code, with every bit coding for one class). If the flag of one or several errors of a particular class is set to HIGH, then the corresponding class bit is HIGH, too.

Using the SPI command "get.error", ECU can obtain detailed information about which errors are flagged. The "ATIC 116" sends as response 24-bit code, in which every bit codes for one particular error. If that error is flagged, the bit is HIGH, otherwise it is LOW.

Error table

All diagnosable errors are shown in the table below.

Error Bit	Errorcode (24 bit)	Priority/Error class	Error description	De-bounce	Fast Error?	Trigger	SW or HW	Reaction
24	0x800000	high/1	CRC error of EEPROM detected (MLX area)	no		only after wake-up	SW	Info to host (SPI)
23	0x400000	high/1	radius evaluation	yes	Fast	Sync signal	SW	Info to host (SPI)
22	0x200000	high/1	RAM check Error	no		only after wake-up	SW	Info to host (SPI)
21	0x100000	high/1	ROM check Error	no		Periodically in background	SW	Info to host (SPI)
20	0x080000	high/1	CRC Error of EEPROM detected (CONTI area)	no		only after wake-up	SW	Info to host (SPI)
19	0x040000	high/1	MR output voltage monitoring	yes	Fast	Sync signal	HW	Info to host (SPI)
18	0x020000	high/1	dynamic RAM check	no (1)	Fast	Sync signal	SW	Info to host (SPI)
17	0x010000	*	*	*		*		*
16	0x008000	*	*	*		*		*
15	0x004000	*	*	*		*		*
14	0x002000	*	*	*		*		*
13	0x001000	*	*	*		*		*
12	0x000800	*	*	*		*		*
11	0x000400	*	*	*		*		*
10	0x000200	middle/2	oscillator check (comparison of HP and LP oscillators)	no		Only after wake-up	HW	Info to host (SPI)
9	0x000100	middle/2	Auxiliary path error (2)	yes	Fast	Sync signal	SW	Info to host (SPI)
8	0x000080	*	*	*		*		*
7	0x000040	*	*	*		*		*
6	0x000020	*	*	*		*		*
5	0x000010	*	*	*		*		*
4	0x000008	low/3	invalid command received in R&R	no		SPI Interrupt	SW	Info to host (SPI)

			Mode					
3	0x000004	*	*	*		*	*	*
2	0x000002	low/3	invalid command received in Program Mode	no	Fast	SPI Interrupt	SW	Info to host (SPI)
1	0x000001	low/3	CRC error detected (communication)	no	Slow	SPI Interrupt	HW	Info to host (SPI)

Table 13: Debouncing parameters

(1) If error is detected, test the same RAM-Cell three times, and then rise error flag if necessary

(2) State-machine errors are not reported in burst-mode, only counter mismatch errors are reported (see below for more details)

Diagnosis repetition rate

In the table below the repetition rate for error diagnosis is listed

Error	Diagnosis Repetition Rate	Mode
1, 2, 4	With each SPI interrupt	R&R mode
9, 18, 19, 23	Every 8 Sync pulses	Burst mode
10, 20, 22, 24	Only during Wake-up	NA
21	Once in every execution of background loop	Burst mode

Table 14: Diagnosis repetition rate

Fast errors

Errors 9, 18, 19, and 23 (which are executed in burst mode every 8 Sync pulses) are called fast errors.

SPI command "get.error"

While in burst mode, the ASIC sends DATA telegrams which contain 3-bit error information. This information only describes if an error of a particular severity class had occurred in the past. Information about which error had occurred can be obtained with the SPI command "get.error".

The response to this command is shown below.

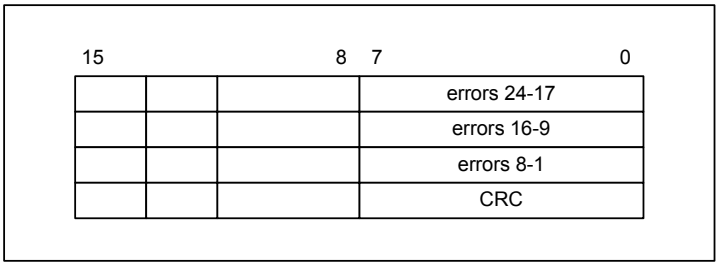


Figure 50: Parsing of response to "get.error"

Each error is represented by one bit. If that bit is HIGH, then the corresponding error had occurred in the past. If that bit is LOW, then the corresponding error had not occurred in the past.

The errors 24-17 are represented in section 1, with bit 7 representing error 24, and bit 0 representing error 17. The errors 16-9 are represented in section 2, with bit 7 representing error 16, and bit 0 representing error 9. The errors 8-1 are represented in section 1, with bit 7 representing error 8, and bit 0 representing error 1.

SPI command "reset.error"

The ECU can reset any error flag of the "ATIC 116", for example because the error has disappeared. This is done with the SPI command "reset.error".

The error representation is similar to that in "get.error": each error is represented by one bit. If a particular error flag is to be reset to LOW, then the corresponding bit in "reset.error" command must be set to HIGH. If a particular error flag is to remain unchanged, then the corresponding bit in "reset.error" must be set to LOW.

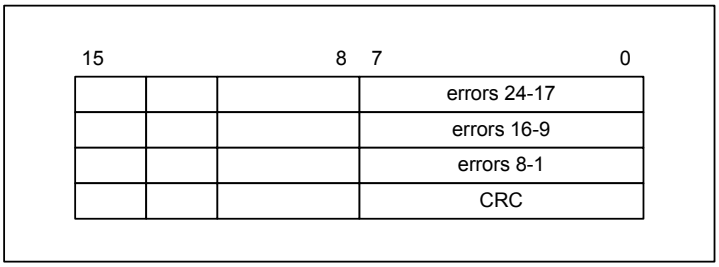


Figure 51: SPI command "reset.error"

SPI response "reset.error"

Upon execution of the SPI command "reset.error", "ATIC 116" send an appropriate SPI response. The error representation is similar to that in "reset.error" command, but inverted. If an error flag was reset to LOW, then the corresponding bit in the response is reset to LOW. If an error flag was left unchanged, then the corresponding bit is set to HIGH.

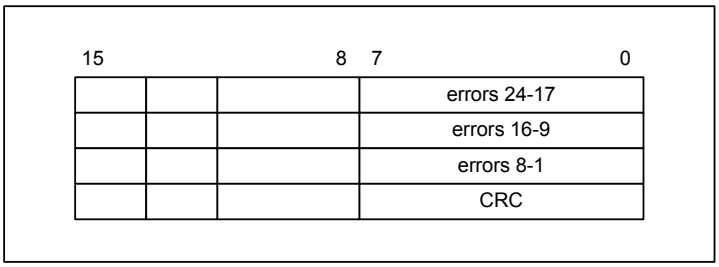


Figure 52: SPI response "reset.error"

Radius evaluation

The MR bridge output signals are sine and cosine of the same angle. According to the theorem

$$\sin^2(\alpha)+\cos^2(\alpha)=1$$

the sum of the squares of the MR bridge output signals SIN and COS should ideally yield the value of "1". This calculation is called "Radius Evaluation" and can be used to check the validity and plausibility of the MR signals. The placement of the "Radius Evaluation" block within the main path is shown in the next figure.

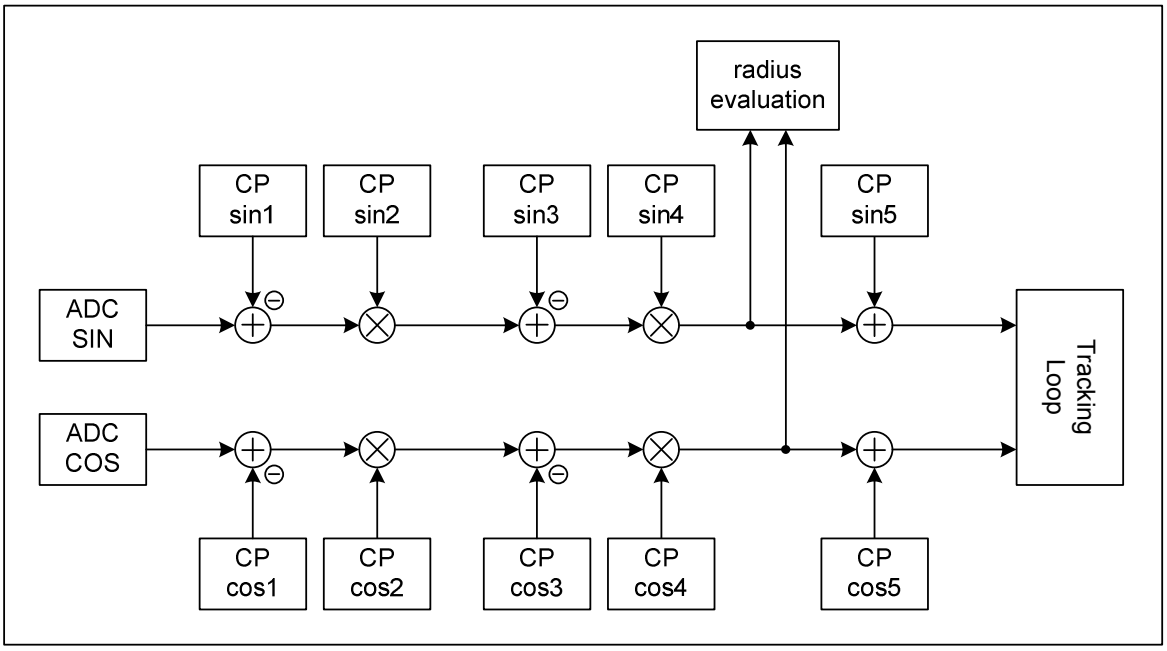


Figure 53: Placement of "Radius Evaluation" block within the main path

CP: compensation parameters described above

Normalization

The theorem $\sin^2(\alpha)+\cos^2(\alpha)=1$ applies only to mathematical sine and cosine functions with values within the interval [-1; 1]. The signals actually taken from the position (1), however, will not be mathematical sine and cosine functions; they will have the form of $A_{\sin}\cdot\sin(\alpha)$ and $A_{\cos}\cdot\cos(\alpha)$ where *Asin* and *Acos* are the amplitudes of the SIN and COS signals expressed in digits. The ideal value of these amplitudes is 0x4000. The actual radius calculation is then performed according to the formula given below.

$$RADIUS\_CALCULATED=\left(ADC_{SIN}^2+ADC_{COS}^2\right)/2^{16}$$

The ideal result value is 0x1000, or 4096.

Radius boundary parameters

Due to sensor and AFE errors, even after normalization, the resulting radius will virtually never be 0x1000, but will have a value which is slightly deferent from 0x1000 (if the signals are valid and plausible) or significantly different from 0x1000 (if the signals are not valid and plausible).

Radius boundary parameters describe the upper and lower limit of the radius values for which the corresponding signals are still considered as valid and plausible. The radius boundary parameters (high limit and low limit) are independently programmable (see EEPROM content).

MR Output Voltage Monitoring

The MR output voltages MR1, MR2, MR3 and MR4 will be monitored during "ATIC 116"'s active mode. If they leave a specified window (high threshold, low threshold), an error flag will be set (Diagnosis Error#19 " MR output voltage monitoring").

Parameter	Symbol	Min.	Typ.	Max.	Units
MR supply voltage	MR+	3	3.3	3.6	V
Lower detection threshold	THR_LOW	35	40	45	% of MR+
Higher detection threshold	THR_HIGH	55	60	65	% of MR+

Table 15: MR output voltage monitoring

Auxiliary path error diagnosis.

As already described above, there are three error conditions which can be detected in the auxiliary path:

Error A:	Counter contents differ by more than 1
Error B1:	State machine 1 enters error state
Error B2:	State machine 2 enters error state

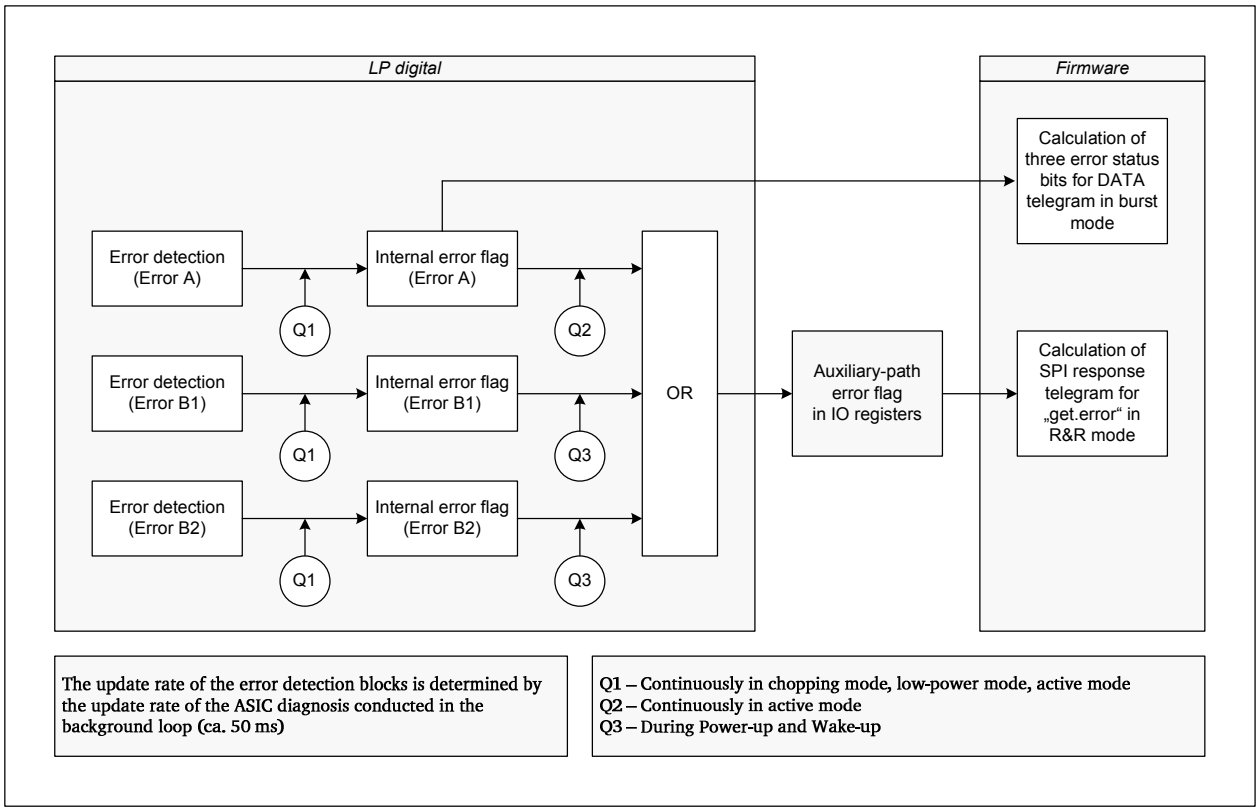


Figure 54: Auxiliary path error diagnosis

The actual diagnosis implementation is shown in the figure above. The following features can be seen:

- Errors A, B1, and B2 are used to determine the status of the error flag #9 (auxiliary path error)
- Only error A is used to determine the status of the error severity class flags in DATA telegram
- If error B1 or B2 occurs, it will be reported as error flag #9 only after the next Wake-up

3.2.18 Application circuit

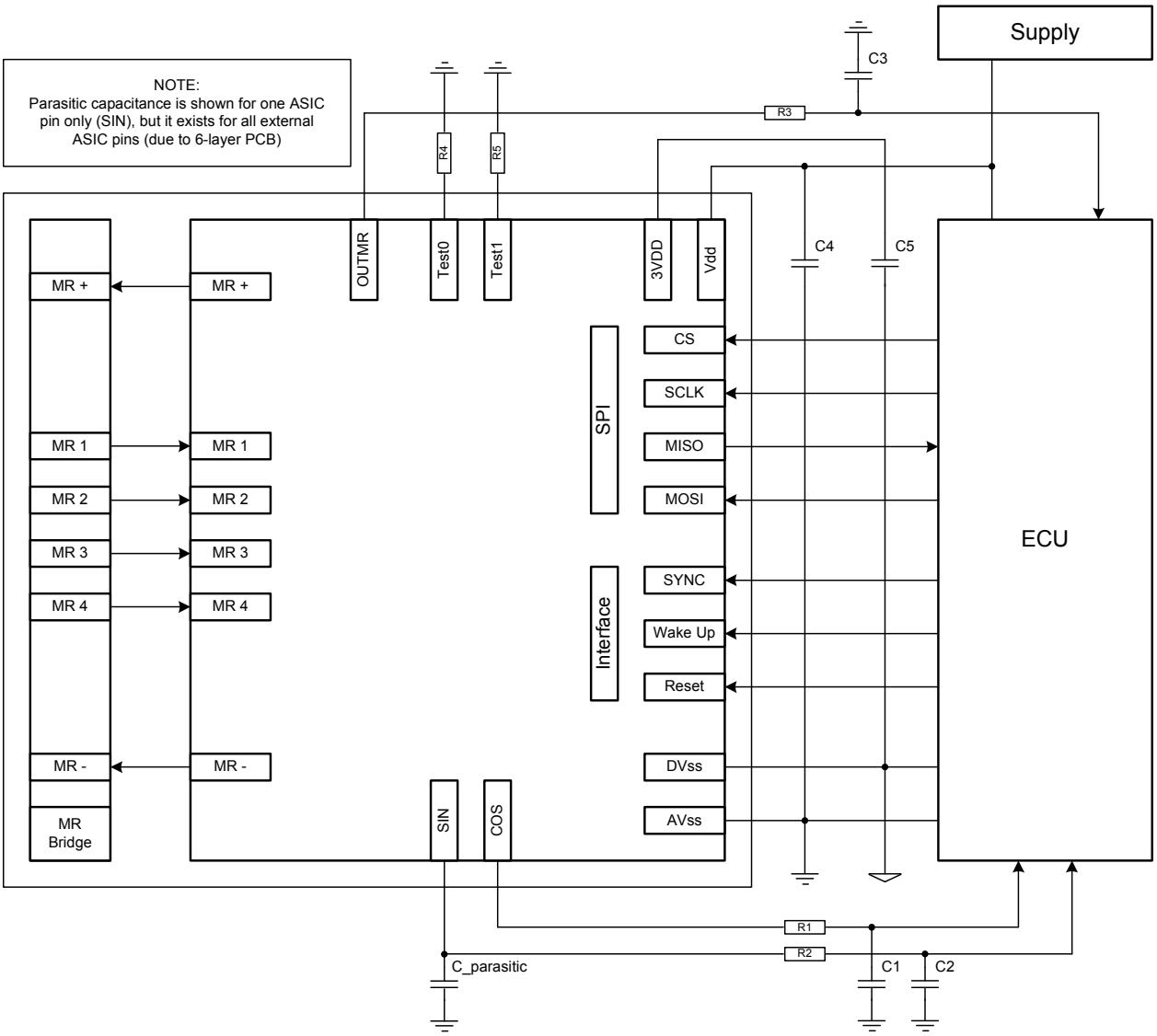


Figure 55: ATIC 116 application circuit

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
1	resistor	R1, R2		1		kOhm	
2	resistor	R3		1		kOhm	
3	resistor	R4, R5		100		Ohm	Prevention of test-mode entry
4	capacitor	C1, C2		47		nF	
5	capacitor	C3		47		nF	
6	capacitor	C4, C5		100		nF	ceramic capacitors
7	capacitance	C_{PAR}		40		pF	parasitic capacitance between pins and PCB

Table 16: External components of the "ATIC 116"

3.2.19 Power distribution

Power distribution scheme is shown in the figure below

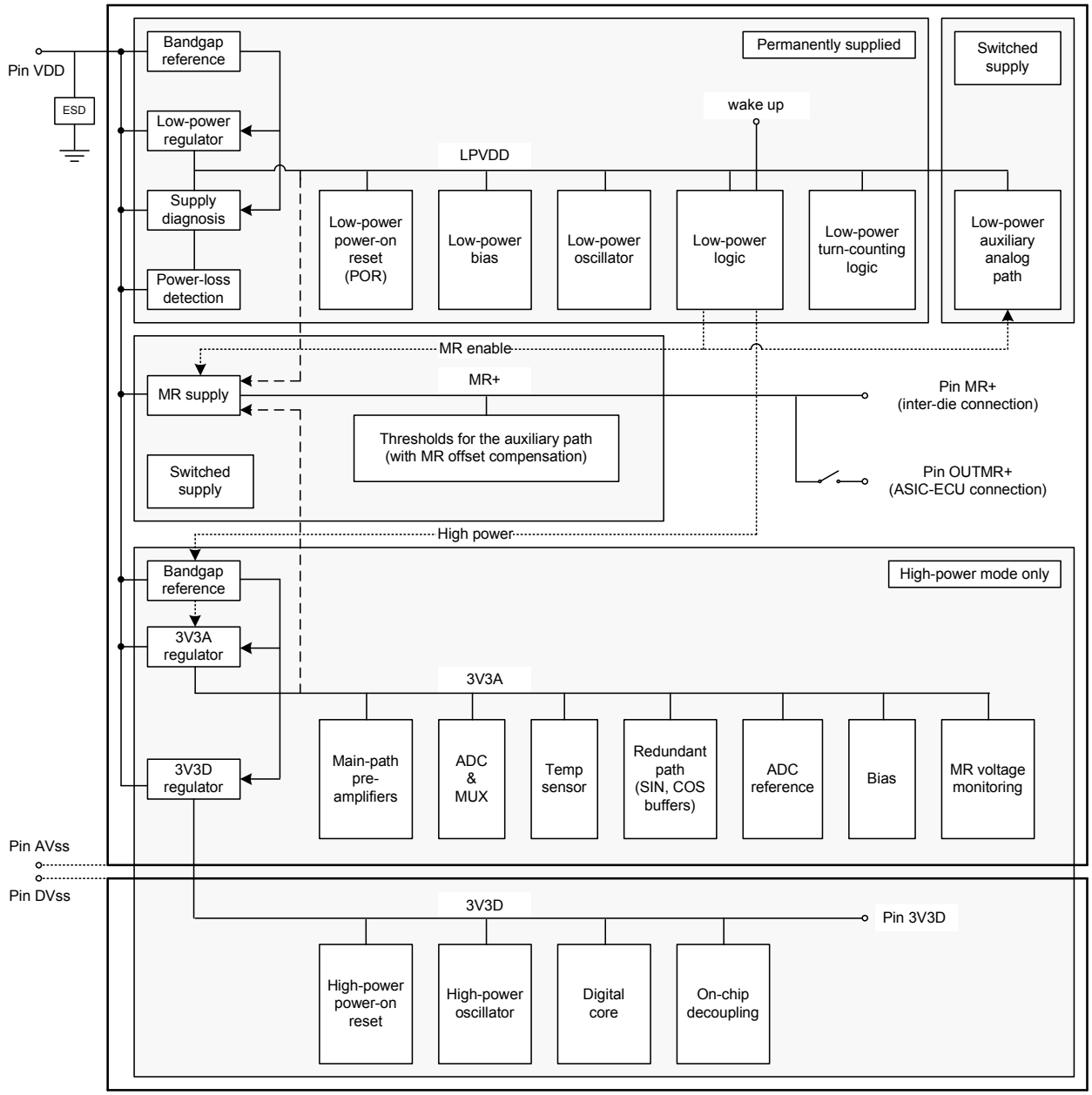


Figure 56: Power distribution

The following features can be recognized:

1) The supply voltage VDD is 4.75...5.25 V (active mode) or 3.0...5.25 V (chopping mode, low-power mode, transport mode).
2) There are two independent band-gap references: bang-gap reference #1 for main path, and band-gap reference #2 for auxiliary and redundant path
3) The MR bridge supply circuit is referenced by band-gap reference 1 (during active mode) or band-gap reference 2 (during chopping mode and low-power mode)

NOTE 1: Ratiometricity considerations

The MR bridge output signals (sin and cos) are proportional to the MR supply voltage (MR+). Any changes in MR+ will also result in corresponding changes in sin and cos, even though the magnetic field has not changed.

For that reason, the ADC reference voltage must track the MR bridge supply voltage to achieve ratiometric behavior. Thus, the ADC reference voltage is derived from the 3V3A regulator

NOTE 2: µC supply voltage

The µC-core is ON (supply voltage supplied to the µC) only in the active mode. In the chopping mode, transport mode, and low-power mode the µC is OFF (no supply voltage).

It must be made sure that it is not possible for the "ATIC 116" to supply the µC core (for example via parasitic channels) during chopping mode and low-power mode.

NOTE 3: VDD Ramp-up

When the car battery is disconnected or discharged, the voltage supply to the "ATIC 116" is temporarily interrupted. When the battery is reconnected or charged again, the supply voltage VDD will undergo a so called ramp-up phase. During this phase, VDD goes from 0V to 5V (4.75...5.25V).

The speed (in Volts/sec) with which this transition takes place can vary significantly. The exact values are specified in chapter 3.3.7 (timing). The "ATIC 116" must be able to cope with all ramp-up speeds within this specified interval. The following situations must be prevented:

1) Reset generators are slope-controlled, not level-controlled; as consequence, the slow VDD ramp-up is not recognized, no reset signal is generated.
2) Analog reset generator generates reset signal later than digital reset generator; as consequence, the digital part is already running, but there is no useful input from the analog part, and the digital part enters a "hang-up" state.
3) Reset generator is implemented as a simple comparator without hysteresis or debouncing; as consequence, when the threshold voltage is reached during slow ramp-up, several consecutive reset signals are generated.

NOTE 4:

The "ATIC 116" must also be in the position to cope with a situation in which the VDD rises for some time, then falls, and then rises again (see figure below).

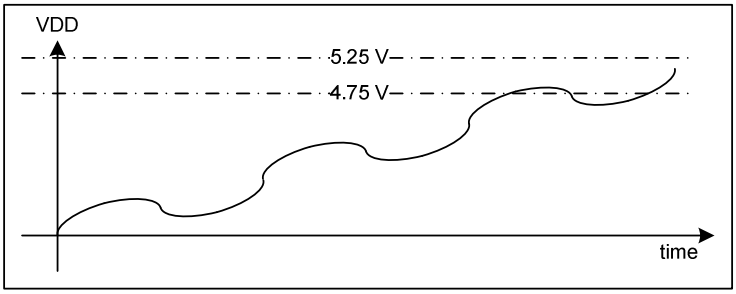


Figure 57: Possible VDD ramp-up scenario

The term "is able to cope with ramp-up" means that once stable "ATIC 116" supply voltage is reached, the "ATIC 116" is fully operational, regardless of the ramp-up history.

NOTE 5: Voltages

In the table below, the most important blocks are shown, together with the corresponding supply voltage sources.

			voltage source	min	typ	max	unit
Active Mode	MR sensor		MR+ with BG_high	3	3.3	3,6	V
	main path	analog	3V3A	3	3.3	3,6	V
		digital	3V3D	3	3.3	3,6	V
	auxiliary path	analog	low-power regulator	3	3.3	3,6	V
		digital	low-power regulator	3	3.3	3,6	V
	redundant path	analog	3V3A	3	3.3	3,6	V
Undervoltage case	MR sensor		MR+ with BG_high	2.0	3.3	3,6	V
	main path	analog	3V3A	2.0	3.3	3,6	V
		digital	3V3D	2.0	3.3	3,6	V
	auxiliary path	analog	low-power regulator	2.0	3.3	3,6	V
		digital	low-power regulator	2.0	3.3	3,6	V
	redundant path	analog	3V3A	2.0	3.3	3,6	V
Low-Power Mode, Chopping Mode, Transport Mode	MR sensor		MR+ with BG_low	3.0	3.3	3.6	V
	main path	analog	not used	***	***	***	***
		digital	not used	***	***	***	***
	auxiliary path	analog	low-power regulator	3.0	3.3	3.6	V
		digital	low-power regulator	3.0	3.3	3.6	V
	redundant path	analog	not used	***	***	***	***

Table 17: Blocks and their supply voltage sources

3.2.20 Pin names and functions

External Pinout

PIN	NAME	TYPE (active mode) See note, page 94	TYPE (low power, chopping and transport mode)	Function
1	RESET	I,D,PD, AH	I,D,PD, AH	Global asynchronous reset input
2	SYNC	I,D,PD, AH	PD	Sync signal input to start MR signal acquisition, active high
3	SCLK	I,D,PD	PD	SPI clock input
4	CS	I,D,PD,AH	PD	Chip select input, high active
5	MOSI	I,D,PD	PD	SPI slave input
6	MISO	O,D	T	SPI slave output
7	WAKE-UP	I,PD	I,PD	Active mode enable input
8	TEST0	I,D,AH,PD	PD	Test mode pin
9	TEST1	I,D,AH,PD	PD	Test mode pin
10	DVss	A,P	A,P	Power supply, digital ground
11	VDD	A,P	A,P	Power Supply
12	AVss	A,P	A,P	Power supply, analog ground
13	COS	O,A	T	Analog redundant path to ECU
14	SIN	O,A	T	Analog redundant path to ECU
15	3V3D	A,P	A,P	Internally generated power supply for the digital
16	OUTMR+	O,A	T	Internally generated power supply for the MR sensor

Table 18: Pin names

Comment1:

Voltage on Pin 16 (OUTMR+) is fed to the ECU; in the ECU it is evaluated for plausibility.

Comment 2:

The value for pull-up and pull-down resistors is 35...65 kOhm (50 kOhm typical).

Internal connections from ASIC to MR Sensor

PIN	NAME	TYPE (active mode)	TYPE (low power mode)	FUNCTION
1	MR1	I ; A		Positive output of bridge #1
2	MR2	I ; A		Negative output of bridge #1
3	MR3	I ; A		Positive output of bridge #2
4	MR4	I ; A		Negative output of bridge #2
5	MR+	O;P		MR bridge supply voltage
6	MR-	O;P		MR bridge supply voltage

Table 19: Internal connections from ASIC to MR Sensor

Note: **A** - Analog; **D** - Digital; **P** - Power Supply;
I – Input; **O** – Output; **PD** - integrated Pull-down; **PU** - integrated Pull-up;
L – Low; **H** – High; **L/H** – Low to high transition; **H/L** – High to low transition;
AL = Active Low; **AH** = Active High; **T** – Tristate (high resistance)

In the figure below the pin-out of the ATIC116 is shown.

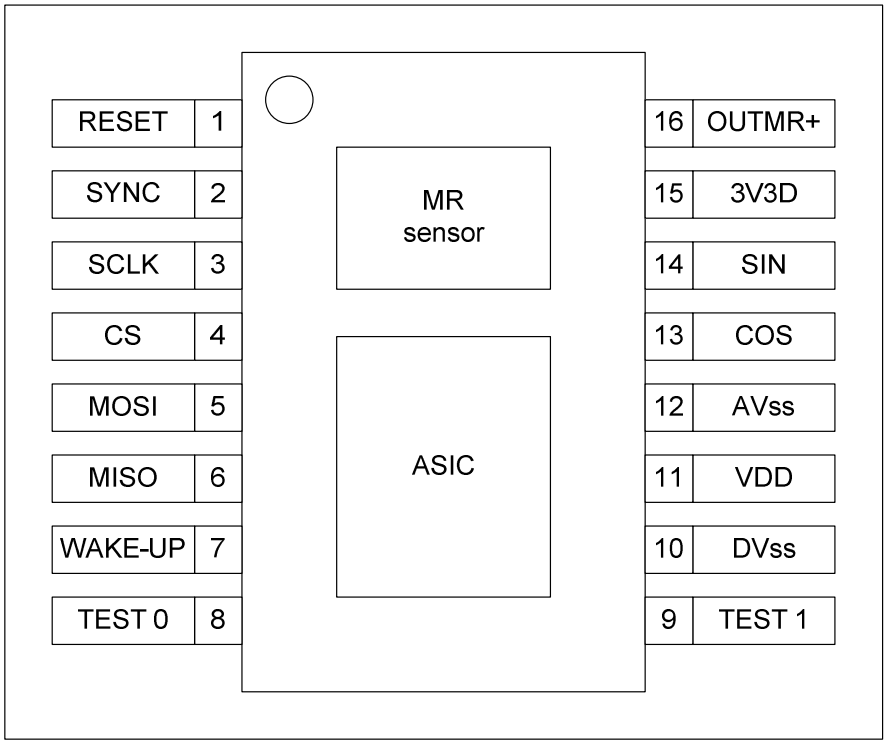


Figure 58: Pin-out

3.2.21 Interface requirements

a) All digital output pins must be capable of tristate operation

b) Intermittent (< 0.5 s) voltage drops to 3 V (start sequence) are not allowed to lead to

- the destruction or preliminary damage of assemblies
- permanent modification outside of the tolerances
- changes in counter value. The "ATIC 116" must be able to count during these voltage drops (without missing motor turns), see undervoltage case for details
- malfunctions
- changes in the previous condition (after startup time)

3.3 Parameters

3.3.1 System requirements

At Tamb = -40...+140 °C; VDD = 4.75...5.25 V if not otherwise specified

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
1	Angle measurement range		0		360	°	
2	Angle resolution				0.2	°	resolution must be 0.2° or smaller (e.g. 0.1°)
3	Angle accuracy				1.2	°	"ATIC 116" errors
4	Speed measurement range (active)		0		16382	eppm	
5	Speed measurement range (passive)		16383		30000	eppm	
6	Speed resolution				4	eppm	
7	Speed accuracy *)		- 20		20	eppm	< 2000eppm
8	(speed ripple=maximum difference to average speed)		- 40		40	eppm	@ 2000 ... 4000eppm
9			- 60		60	eppm	@ 4000...6000eppm
10			- 100		100	eppm	@ >6000eppm
11	Speed accuracy		- 2		2	eppm	< 2000eppm
12	(averaged over one electrical rotation)		- 4		4	eppm	@ 2000 ... 4000eppm
13			- 6		6	eppm	@ 4000...6000eppm
14			- 20		20	eppm	@ >6000eppm
15	acceleration				+/- 2e6	eppm/sec	
16	temperature measurement accuracy		-2.5		+2.5	K	Relative accuracy

*): *according Vendor Addendum speed ripple specification of +/-2% with dynamic compensation active is guaranted by supplier.*

3.3.2 Absolute maximum ratings

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
1	ambient temperature	T	-40		+125	°C	
2	ambient temperature	T	+125		+140	°C	20 min max, 96h in total
3	supply voltage	V_{SUP}	0		6	V	
4	storage temperature	T_S	-40		+140	°C	According to DIN IEC 68-2-1 and 68-2-2 (EN 60068-2) -40°C / 50h: IEC 68-2-1 140 °C / 240h: IEC 68-2-2

NOTE:

Absolute maximum ratings specify conditions which the "ATIC 116" has to withstand without damage. It is not necessary for the "ATIC 116" to be operational within maximum ratings.

3.3.3 Operating conditions

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
1	operating ambient temperature	TB	-40		+125	°C	
2	maximum ambient temperature	TB_{MAX}	+125		+140	°C	20min max, 96h in total
3	supply voltage	VDD	4.75	5	5.25	V	active mode
4	supply voltage	VDD_{CHOP}	3	5	5.25	V	chopping mode, low-power mode, transport mode, undervoltage case

NOTE:

Operating conditions specify conditions within which the "ATIC 116" must be fully operational and fulfill specified requirements like accuracy and resolution.

3.3.4 Magnetic input

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
1	magnetic field strength	B	30		100	mT	no destruction up to 1T
2	angular speed (main path)	Ω_m			8e3	rpm	Input condition is up to 15e3 with clamping at 8191 = 136 Hz magnet rotations per second = 273 Hz at MR electric output
3	Angular speed (auxiliary path)	Ω_m			15e3	rpm	

MR bridge sensor: see table 8 and table 9 for MR bridge sensor parameters see chapter “Sensor output signals”.

3.3.5 Electrical characteristics

At TB = -40...+140 °C; VDD = 4.75...5.25 V if not otherwise specified

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
1	Supply current (active mode)	I_{NORM}			30	mA	
2	Supply current (low-power mode)	I_{LP}			5	mA	
3	Supply current (chopping mode)	I_{CHOP}			100	µA	See Vendor Addendum
3a	Supply current (transport mode)	I_{TRANSP}			80	µA	Low-power mode not entered
4	power-loss detection voltage	V_{PLD}	2.5		2.9	V	auxiliary path must be fully operational down to the MIN value
5	Digital input voltage LO	$V_{DIG\_IN\_LO}$	-0.3		0.8	V	digital input pins must be fully operational when HP-POR is released
6	Digital input voltage HI	$V_{DIG\_IN\_HI}$	2.5		V_{DD}+ 0.8	V	digital input pins must be fully operational when HP-POR is released
7	Digital output voltage LO	$V_{DIG\_OUT\_LO}$			0.5	V	SPI & Control pins
8	Digital output voltage HI	$V_{DIG\_OUT\_HI}$	V_{DD}-0.3			V	SPI & Control pins
9	Rdson MISO Low, High		30	75	150	Ω	
	input capacitance	C_{IN}			10	pF	For information only
10	Minimum voltage required to write to EEPROM	V_{EE_WRITE}	4.75			V	
11	Internal pull-up / pull-down resistors	R_{PULL}	35	50	65	kΩ	valid for pins 1,2,3,4,5,7,8,9
12	internal supply voltage (analog)	3V3A	3.0	3.3	3.6	V	active mode
13	internal supply voltage (digital)	3V3D	3.0	3.3	3.6	V	active mode
14	internal supply voltage (MR sensor)	MR+	3.0	3.3	3.6	V	Active, low-power, chopping, and transport mode, (Vdd=3.0..5,25V)
15	internal supply voltage (analog)	LPVDD	3.0	3.3	3.6	V	low-power, chopping, and transport mode (Vdd=3.0..5,25V)
16	internal supply voltage (digital)	DLVDD	2.7		3.6	V	All modes (Vdd=3,0..5.,25V)
17	internal supply voltage (MR sensor)	MR+	3.0	3.3	3.6	V	low-power, chopping, and transport mode, Vdd=3.0..5,25V

Main Path

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
20	Supply Voltage	3V3A	3.0	3.3	3.6	V	Supply of Main path
21	Differential Input voltage		+/-0		+/-240	mV	For Vdd=5V and PGA trimming factor between 6..40
22	PGA input frequency				300	Hz	Characterized, guaranted by design
23	PGA Gain	G	6		40		PGA gain will be set using a 4-bit parameter
24	MP Gain linearity error				0.1	%	Incl. ADC
25	MP Gain mismatch SIN to COS channel				10	%	Initial Gain mismatch between Sin & Cos channel measured after ADC => compensated via Static Compensation
			-1		1	%	Drift over life (1500h) => compensated via Dynamic Compensation
26	PGA Gain adjustment resolution			4		bits	Programmable via EEPROM during calibration
27	PGA Gain steps			16			Possible Gain settings: 40-(34/15*GAIN_CODE); GAIN_CODE: 0..15
28	PGA Gain temperature coefficient		-100		+100	ppm/°C	Indirectly tested via MPgain max gain test over temperature
29	Settling time				2.5	µs	Guaranted by design
30	Input referred total noise				20	LSB	Incl. MR bridge, PGA and ADC => @10000LSB at ADC input corresponding to 0,2° angle error
31	Input common mode		40	50	60	%	% of supply voltage, characterized, guaranted by design
32	Output common mode		40	50	60	%	% of supply voltage, design parameter
33	PGA time to go out of saturation				2	µs	Design parameter, 5 µs prior to sampling, the ECU will switch high motor current. Disturbance could saturate the PGA
34	S&H time window	Tsh			2.5	µs	time window in each time frame available for S&H operation, guaranted by design
35	Sampling rate (nominal)	Ts	100		485	µs	due to tolerances the actual Ts may differ up to 5% from the nominal Ts, characterized and simulated

Main path, additional parameters, hold mode

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
40	Hold voltage		-1.6		+1.6	V	
41	Drop voltage over Hold time				1	LSB	Change of S&H output during hold time of 24us may cause an ADC drift of no more than 1LSB, characterized, design parameter

MR Monitoring

Pos	Parameter	Symbol	Min	Typ	Max	Unit	Comment
50	MR supply voltage	MR+	3	3.3	3.6	V	
51	Lower detection threshold	T_{HR_LOW}	35	40	45	% of MR+	
52	Higher detection threshold	T_{HR_HIGH}	55	60	65	% of MR+	

ADC

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
60	Input differential voltage @ Vdd=3.3V	V_{IN_ADC}	-1.6		+1.6	V	
61	Input common mode voltage	V_{COM_ADC}	0.25* V_{DD_ADC}	0.5* V_{DD_ADC}	0.75* V_{DD_ADC}	V	V_{DD_ADC}= 3.0 ... 3.6V
62	Nominal resolution			15		bits	
63	INL				3	LSB_{15}	
64	DNL				1.5	LSB_{15}	
65	RMS noise				6	LSB_{15}	
66	ADC accuracy	acc_{ADC}	12			bits	
67	Conversion time	t_{ADC_CONV}			12	µs	To reach <85us processing time

Note: The ADC is part of the signal chain, thus ADC gain and offset error are compensated via Static Compensation.

Redundant Path

Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
80	Supply voltage	3V3A	3.0	3.3	3.6	V	Design parameter
81	Input voltage		± 0		± 100	mV	@depending on MR supply voltage
82	OPAMP gain	G_{RP}	14	14.5	15		
83	RP path input offset drift over temperature (incl. MR sensor)				3	mV	Drift due to temp from 25 to 125° and from -40 to 25°
84	RP path input offset drift over life (incl. MR sensor)				2	mV	Life time drift: 0..1500h acc. Product Qualification Data
85	OPAMP bandwidth	B_{RP}	30		100	kHz	Characterized, guaranted by design
86	OPAMP input referred noise (rms)	V_{n_red}			0.05	mV	RMS, @ signal bandwidth 30 kHz, characterized, guaranted by design
87	OPAMP gain non-linearity error				0.1	%	characterized, guaranted by design
88	Input common mode		40		60	%	see output common mode of the MR sensors
89	Output reference voltage (incl. MR sensor offset)	V_{REF_RP}	45	50	55	%	in % of 3V3A (incl. MR sensor offset) over temperature
90	Output current	I_{OUT}	-1		1	mA	Dynamic test at 70mV input voltage @fin=266Hz, load: 0,9kOhm, 6,8nF.
	Load capacitor (right at the pin)	C_{LOAD}			40	pF	
92	Output voltage range	V_{OUT}	5%		95%		In % of Supply voltage; Tested with 500mV input voltage, load of 3kOhm to be added

Auxiliary path (counter path)

7Pos.	Parameter	Symbol	Min	Typ	Max	Unit	Comment
100	Supply voltage		3.0	3.3	3.6	V	Supply of Aux Path
110	Gain of all amplifiers		17.5	20	21.5		
	Input impedance		1			MOhm	For information only
112	Non-linearity error of all amplifiers				2	%	Design parameter, within the threshold range
113	Input common mode range		40	50	60	%	% of MR bridge supply voltage, characterized, guaranted by design
114	Common mode rejection		40			dB	
115	Gain matching sin-to-cos		-12		+12	%	
116	Gain temperature coefficient		-100		+100	ppm/°C	Design parameter
117	Comparator threshold range (differential, input referred) @ 3.3 V		-9		9	mV	see note below
119	Comparator threshold resolution (adjusted by voltage DACs)			5		bit	
120	Comparator hysteresis		-1.5		+1.5	mV	before amplification (+/- 30 mV after amplification)
121	Comparator threshold temperature coefficient		-100		+100	ppm/°C	Design parameter, indirectly tested
123	Settling time (from end of auto-zero to correct digital comparison result)				2.5	µs	Design parameter
124	DAC voltage range				180	mV	Design parameter
	Switching Threshold of comparators (for counter increase/decrease)		-10		10	°	Electrical angle evaluated in magnetic calibration over 1 electrical period (-2..362°) in active mode

NOTE:

If the turn counting is to function correctly, then the overall offset must be smaller than 35% of the amplitude. The overall offset contains: sensor offset, amplifier offset, comparator offset.

Example: for amplitude of 10.75 mV (minimum sensor amplitude at LPVDD = 2.0V), the overall offset must not exceed 3.75 mV (before amplification); for amplitude of 45 mV (typical sensor amplitude at LPVDD=3.3V and T=25°C), the overall offset must not exceed 13.75 mV.

For that reason, it will be necessary to compensate for the sensor offset. This is done by adjusting the comparator threshold voltage accordingly by using DACs. Such adjustment will be made only once during the "ATIC 116" calibration process.

This adjustment must compensate for the following three factors: sensor offset, amplifier offset, comparator offset. This adjustment will be made at room temperature. Temperature drift and life-time drift of these three parameters will not have to be compensated for.

High-power POR

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
130	Digital Supply voltage	3V3D	3.0	3.3	3.6	V	
131	Low-power supply voltage	LPVDD	1.8		3.6	V	
132	Low-power bandgap reference			1.25		V	
135	POR level at rising supply voltage (referred to 3V3D)	$Vpor_{UP}$	2.0		2.5	V	Threshold levels when the supply is rising, Digital I/Os have to work down to this voltage
136	POR level at falling supply voltage (referred 3V3D)	$Vpor_{DN}$	1.8		2.3	V	Threshold levels when the supply is falling, Digital I/Os have to work down to this voltage
137	Hysteresis	$VporH_{HYS}$		0.2		V	Difference between the threshold when the supply is rising and the threshold when the supply is falling
138	POR delay	TporH	1			µs	

Low-power POR

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
140	Supply voltage	LPVDD	2	3.3	3.6	V	
141	POR level at rising supply voltage (referred to VDD)	$VporL_{UP}$	1.7		2.3	V	Threshold level when the supply is rising
142	POR level at falling supply voltage (referred to VDD)	$VporL_{DN}$	1.5		2.3	V	Threshold level when the supply is falling
143	Hyteresis	$VporH_{HYS}$		0.15		V	Hytsteresis between rising and falling POR level

High-power oscillator

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
150	Supply voltage	3V3D	3	3.3	3.6	V	
151	Oscillator frequency (actual)	$Fosc_{HP}$	23.75	25	26.25	MHz	Oscillator frequency after trimming over the complete temperature range, 3V3D = 3.3V

Low-power oscillator

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
160	Supply voltage	LPVDD	3.0	3.3	3.6	V	
161	Oscillator frequency (actual)	$Fosc_{LP}$	200	210	220	kHz	Oscillator frequency after trimming over the complete temperature range, LPVDD = 3.3V

Temperature sensor

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
170	Supply voltage	3V3A	3	3.3	3.6	V	active mode
171	Repeatability		-2.5		2.5	°C	
172	Linearity error		-2.5		2.5	°C	

Power Distribution

Low-power bandgap

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
180	Supply voltage	Vdd	3.0	5	5.25	V	
181	Output Bandgap voltage	V_{BG_LP}	-5%	1.25	+5%	V	
182	Temperature coefficient	TC_{BG_LP}	-200		+200	ppm/°C	
183	PSR @ f<500Hz	PSR_0	80	85		dB	Design parameter
184	PSR @ f=30kHz	PSR_1	50	60		dB	Design parameter
185	PSR @ f=1MHz	PSR_1	70			dB	Design parameter
186	PSR @ f=20MHz	PSR_2	90			dB	Design parameter

Low-power voltage regulator

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
190	Supply voltage	Vdd	3.0	5	5.25	V	
191	Output voltage (I_{LP} = 0…5mA)	LPVDD	2	3.3	3.6	V	
192	Input reference voltage	V_{ref_LPVDD}		1.25		V	
193	PSR @ f<500Hz	PSR_0	60	70		dB	Design parameter
194	PSR @ f=1MHz	PSR_1	35	45		dB	Design parameter
195	PSR @ f=20MHz	PSR_2	40			dB	Design parameter
196	Settling time when connecting to 2mA load	T_{s_LP}			20	µs	

High-power bandgap

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
200	Supply voltage	Vdd	4.75	5	5.25	V	
201	Supply voltage	Vdd	3.0		5.25	V	undervoltage case
202	Output Bandgap voltage	V_{BG_HP}	-3%	1.25	+3%	V	
203	Temperature coefficient	TC_{BG_HP}	-200		+200	ppm/°C	
204	PSR @ f<500Hz	PSR_0	105			dB	Design parameter
205	PSR @ f=100kHz	PSR_1	70			dB	Design parameter
206	PSR @ f=1MHz	PSR_1	75			dB	Design parameter
207	PSR @ f=20MHz	PSR_2	85			dB	Design parameter
208	Start-up time	$T_{start\_BG\_HP}$			1000	µs	

High-power voltage regulator for the digital

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
210	Supply voltage	Vdd	4.75	5	5.25	V	
211	Supply voltage	Vdd	3.0		5.25	V	undervoltage case
212	Output voltage	3V3D	3.0		3.6	V	
213	Input reference voltage	V_{ref_3V3D}		1.25		V	
214	Output voltage difference when Iload is 0mA or 5mA	V_{drop}			0.05	V	
215	DC Output Current capability	I_{LP}	6			mA	
216	External decoupling capacitor	C_{3V3D}	50	100	150	nF	
217	Start-up time	T_{start_3V3D}			100	µs	

High-power voltage regulator for the analog

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
220	Supply voltage	Vdd	4.75	5	5.25	V	
221	Supply voltage	Vdd	3.0		5.25	V	Undervoltage case
222	Output voltage	3V3A	2	3.3	3.6	V	
223	Input reference voltage	V_{ref_3V3D}		1.25		V	
224	PSR @ f<500Hz	PSR_0	70			dB	Design parameter
225	PSR @ f=100kHz	PSR_1	50			dB	Design parameter

226	PSR @ f=1MHz	PSR_2	35			dB	Design parameter
227	PSR @ f=20MHz	PSR_2	40			dB	Design parameter
228	Start-up time	T_{start_DVDD}			100	µs	

MR bridge supply block

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
230	Supply voltage	Vdd	4.75	5	5.25	V	
231	Supply voltage	Vdd	3.0	5	5.25	V	Undervoltage case
232	Output voltage in active mode	MRVDD	3	3.3	3.6	V	
233	Input reference voltage in active/low-power mode	V_{REF_MR}	3	3.3	3.6	V	
234	MR Supply Offset (Vout – Vref) at 0h		-50		+50	mV	Initial Offset over full temperature range, calibrated via Static Compensation
235	MRSupply Offset Drift (Vout-Vref)				20	mV	Drift over lifetime (1500h), 20mV drift lead to additional angle error of ~0,1° (compensated via dynamic compensation)
236	Bandwidth(@ VDD=5V)	B_{MRVDD}	10			MHz	
237	PSR @ f<500Hz	PSR_0	60			dB	Design parameter
238	PSR @ f=100kHz	PSR_1	50			dB	Design parameter
239	PSR @ f=1MHz	PSR_2	45			dB	Design parameter
240	PSR @ f=20MHz	PSR_2	45			dB	Design parameter
241	Start-up time after power-on	T_{start_DVDD}			100	µs	
242	Wake-up time (chopping mode)				20	µs	

Timing

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
250	Power-up time				15	ms	From "battery connected" to first meaningful SPI communication
251	Start-up time				10	ms	From "Wake-up" to first meaningful SPI communication
252	Chopping frequency		100			Hz	100uA max average current consumption (incl. MR-bridge), derived from LP Oscillator (division factor= 2000)
253	Output update rate in burst mode		10			kHz	The true angle and speed update rate has to be 100us. Characterized, guaranted by design
254	Time to go from low-power mode to chopping mode		50			ms	Time without rotation detected after which low-power mode can be left.
255	Supply voltage (VDD) ramp-up		6.67e-3		100e3	V/sec	VDD ramp-up
256	PLD (Power loss detection) non-detectable voltage outages		0		5	µs	If VDD falls below PLD threshold for shorter duration then the MAX value, the auxiliary path must remain fully operational, and the PLD flag must not be set.
257	Sync Pulse length (minimum)		200			ns	Shorter Sync might be not recognized
258	Sync Pulse length (recommended)		3			µs	Shorter Sync might disturb S&H operation
259	Sync Pulse period Ts		100		485	µs	From rising edge to rising edge
260	Begin of SPI command (R&R mode)				30	µs after Sync	indicated by CS rising edge
270	End of SPI command (R&R mode)				60	µs after Sync	indicated by CS falling edge

Digital parameters

Digital Timing

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
280	Rise time	$t_{DIG\_I/O, RISE}$	5	15	25	ns	C_{load} = 40pF
281	Fall time	$t_{DIG\_I/O, FALL}$	5	15	25	ns	C_{load} = 40pF

Microcontroller core

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
290	Nominal microcontroller clock speed			25		MHz	See also: high-power clock
291	Word length			16		bit	

EEPROM

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
300	Size			64*16		bit	
301	Data Retention		19			years	temperature profile acc. to Table 1
302	EEPROM Write Cycle		40			ms	time before two consecutive EEPROM write cycles
303	EEPROM Write Cycles At Room Temperature At High temp. (115°C)				 100 10	 kcycles kcycles	Max. EEPROM write cycles

Tracking loop

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
310	Natural frequency	ω_N	0		2000		
311	Damping	δ	0		2		

NOTE:

The parameter Ts describes the sample time of the tracking loop. Ts value of 100µs means that the tracking loop is calculated every 100µs. The parameter Ts will be stored as uint16 and will hold values in the range of 95...485µs.

The Sync pulse and the parameter Ts must match: if Ts is set to 250µs, then the Sync pulse must be sent every 250 µs, too.

NOTE:

An ideal tracking loop (floating point double precision) will not introduce any noise by itself. However, if the tracking loop is implemented as integer (e.g. 16 bit), it will introduce some additional noise. This noise must not exceed a value at which it will not be possible for the "ATIC 116" to meet resolution and accuracy requirements specified above.

SPI Interface

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
320	SPI frequency (as used by ECU)		0		4	MHz	No SPI communication during first 2.5µs of each time frame (S&H phase)
321	Telegram format			64		bit	can be divided into smaller packages

NOTE: The SPI frequency specified above refers to the SPI frequency as it is used by the ECU: maximum frequency of 4 MHz means that the SPI frequency used by the ECU will not exceed 4 MHz. Thus the ASIC must be able to process SPI frequencies of at least 4 MHz.

SPI electrical parameters

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
330	Supply voltage	Vdd	4.75	5	5.25	V	
331	Supply voltage	Vdd	3.0	5	5.25	V	Undervoltage case
332	Output low level	$Volow_{SPI}$	0		0.5	V	
333	Output high Level	$Vohigh_{SPI}$	VDD-0.3		VDD	V	
334	Rise time	tr_{SPI}		15	25	ns	Cload = 40pF
335	Fall time	tf_{SPI}		15	25	ns	Cload = 40pF
336	Pulldown resistor value at Reset, Sync, SCLK, MOSI, ...	Rpull	35		65	kOhm	

4 SPI-communication

4.1 Abbreviations

Abbreviation	Meaning
CS	Chip select
ECU	Engine Control Unit (Master to ATIC 116)
SPI	Serial Peripherial Interface
SecCode	Section code
TelCnt	Telegram counter
DATA	Measurement data (speed, angle, No. of turns)
µC	Microcontroller (part of ASIC)

Table 20: Abbreviations

4.2 Timing assumptions

Throughout this chapter, the following timing assumptions are made (worst case)

Task	*description*	*time (µs)*
1	real-time calculation	75
2	background	20
3	time from sync rising edge to SPI shadow register updated	85

Table 21: Timing assumptions

4.3 CRC polynom

There will be a CRC test conducted for the communication between ASIC and ECU. The CRC polynom is:

"X8+X3+X2+1"

4.4 Communication setup

In the figure below, the Communication setup is shown. Note that ECU is SPI master, whereas "ATIC 116" is SPI slave.

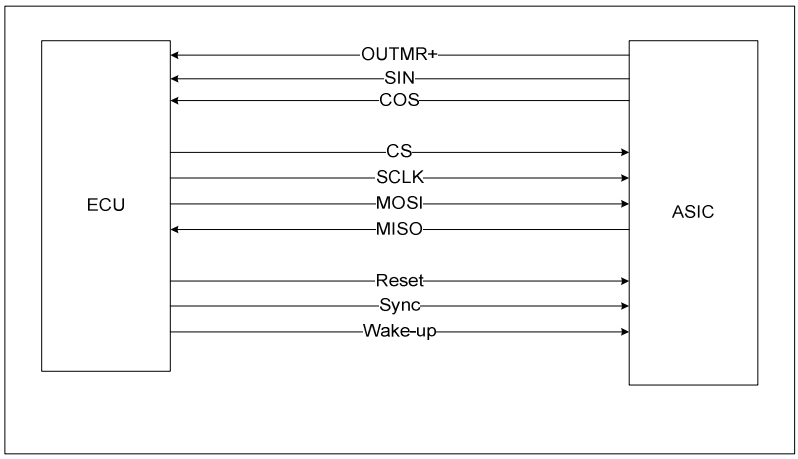


Figure 59: Communication set up

The following signals can be recognized: (a) analog signals, (b) SPI signals, and (c) control signals

Analog signals

- SIN and COS are analog output signals provided by the redundant path.
- OUTMR+ is an MR sensor supply voltage

SPI signals

- SCLK: SPI Clock, used for synchronization of bit transfer between ECU and "ATIC 116".
- CS: Chip Select, used to indicate the transmission beginning (CS rising edge) and transmission end (CS falling edge) of SPI requests and SPI responses in "request & response mode".
- MOSI (Master Out Slave In) and MISO (Master In Slave Out) are used for data transmission between ECU and "ATIC 116".

Control signals:

- Wake-up: sent by ECU, causes the "ATIC 116" to switch from any low-power, chopping or transport mode into active mode.
- Reset: sent by ECU, causes the ASIC to perform a reset, followed by self-test.
- Sync: sent by ECU, used to indicate the beginning of new time frame (one time frame lasts from one sync pulse to the following sync pulse). Sync signal will be sent in "burst mode" and "request & response mode" without any interruption during transitions between modes. Sync has to be forwarded to counters in active mode without any interruption.

4.5 SPI circuitry

In the figure below, the outline of the SPI circuitry is shown.

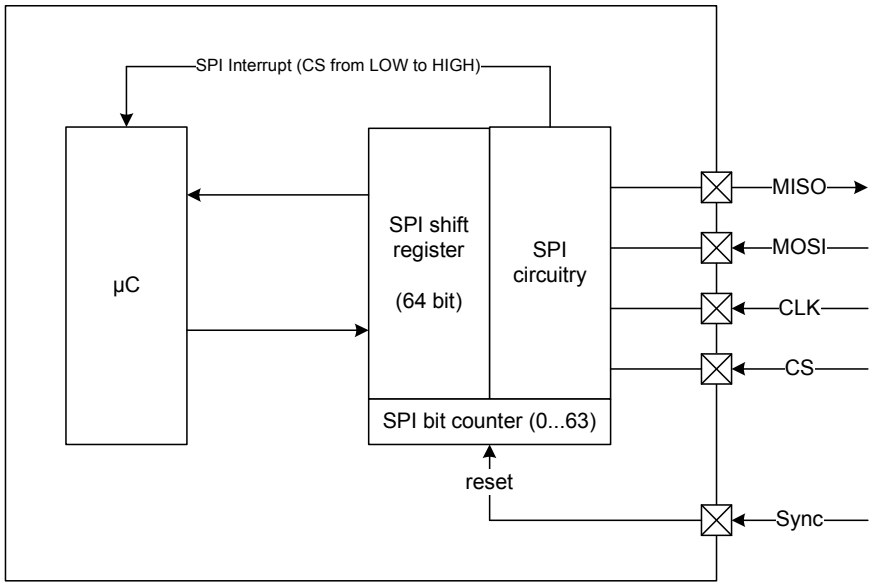


Figure 60: Basic SPI circuitry

- In each time frame, one SPI telegram (64 bit) is prepared to be sent from "SPI shift register" over MISO to ECU
- In each time frame, one SPI telegram (64 bit) could be sent from ECU over MOSI into "SPI shift register"
- One bit is transferred in each direction with each SCLK cycle
- "SPI bit counter" counts bits transferred. With each Sync rising edge (begin of new time frame), the SPI bit counter is reset to zero.
- When CS goes from LOW to HIGH, "SPI interrupt request" is generated and sent to the internal µC

For reasons which will become clear later, it will be necessary to introduce an additional 64 bit register (called SPI shadow register) between the µC and SPI output register.

When µC completes calculation of the SPI telegram, it can then load the results into the SPI shadow register. At the next rising edge of Sync, the SPI shadow register content is shifted into the SPI shift register and can then be transmitted to ECU via SPI.

The transfer from SPI shadow register to SPI shift register is performed by an autonomous circuitry upon Sync rising edge, without any µC participation.

This extended circuitry is shown in the figure below:

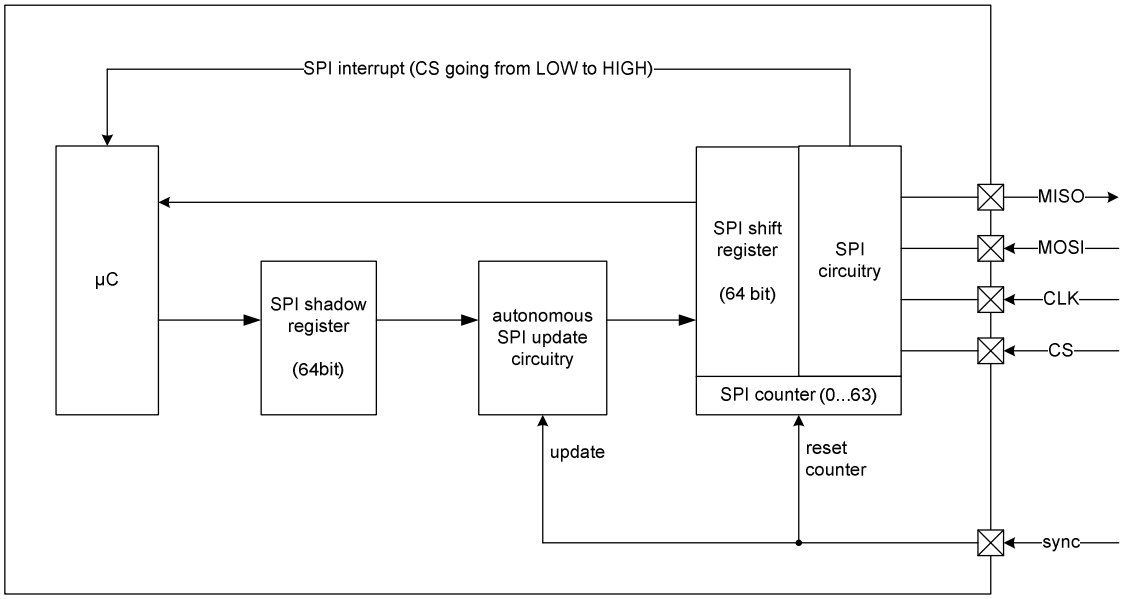


Figure 61: Extended SPI circuitry

SPI shadow update:	transfer of data from µC to SPI shadow register
SPI update:	transfer of data from SPI shadow register to SPI shift register

In the actual implementation, the calculation of the CRC code (see below) will be done by a hard-wired logic instead of µC. Any update of the "SPI shift register" can only be done upon Sync rising edge.

CRC code has to be sent in the same time frame as the data bits used as basis for the calculation. Example: DATA telegram is calculated in time frame "N" and sent in time frame "N+1". The corresponding CRC code has to be sent in time frame "N+1", together with the data bits used for its calculation.

Note:

In case of more than 64 CLK pulses on CLK input without applying a Sync pulse, the data shifted in via MOSI will then be shifted out via MISO (shift register used for input and output).

SPI modes

The "ATIC 116" will support several SPI modes. They are shown in the figure below.

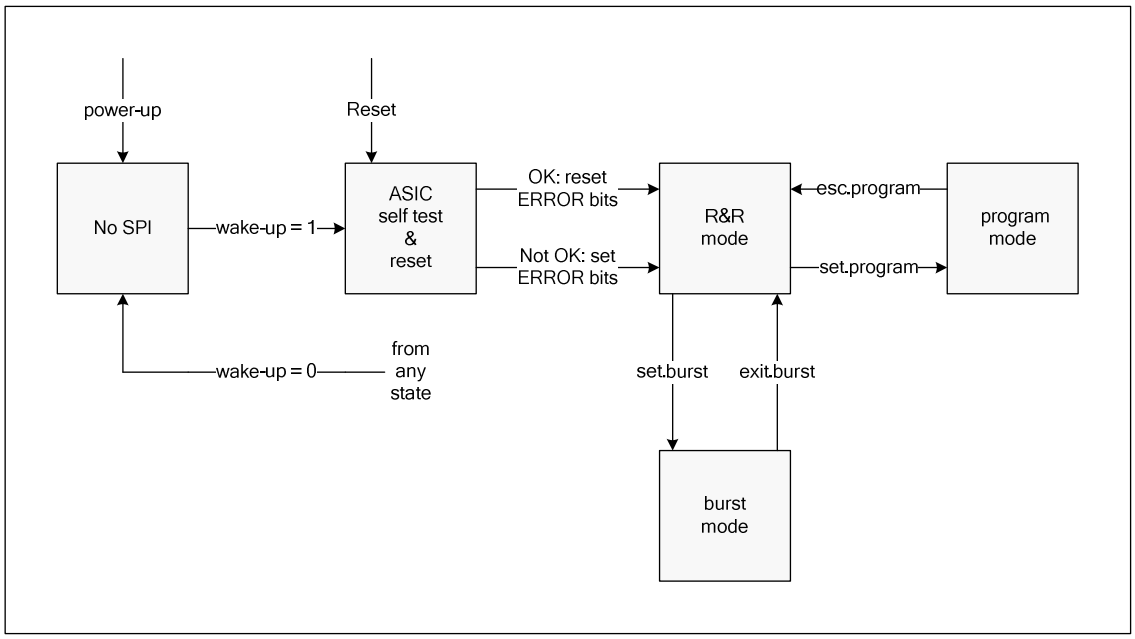


Figure 62: SPI modes

The following SPI modes can be recognized:

No SPI

In this mode, no SPI communication takes place. This mode comprises all low-power modes of the "ATIC 116" (chopping mode, low-power mode, transport mode).

R&R mode

Request and Response: in this mode, "ATIC 116" waits for an SPI request sent by the ECU. After receiving the request, "ATIC 116" sends an SPI response. No DATA are sent by "ATIC 116" to ECU in R&R mode.

Burst mode

In this mode, "ATIC 116" continuously sends DATA to the ECU, one set of DATA per time frame.

Program mode

This mode is used for programming the EEPROM.

4.6 Description of SPI telegram

The data transfer over the SPI bus is conducted using telegrams. Each telegram comprises 64 bits and consists of 4 sections, with each section comprising 16 bits. In the figure below, the telegram format is shown.

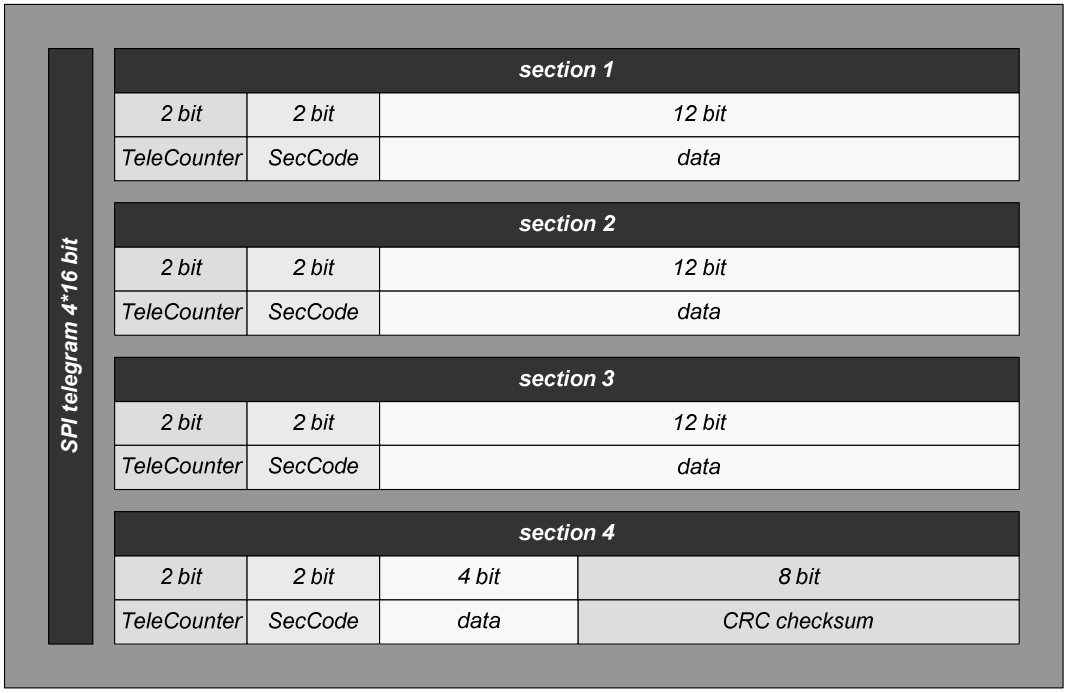


Figure 63: SPI telegram format

The following elements can be recognized:

- TeleCounter (telegram counter) has the same value for every section, but usually increments by "1" with each telegram (more details later)
- SecCode (section code) which increases with each section (0 for section 1, 1 for section 2, 2 for section 3, and 3 for section 4)
- Data bits (40 data bits per telegram); they contain the information proper being transmitted
- CRC checksum (8 bit per telegram). Only the 40 data bits must be protected by the CRC checksum.

4.7 Transmission of SPI telegram

One SPI telegram will be sent from ECU to "ATIC 116" within each time frame, and one SPI telegram will be sent from "ATIC 116" to ECU within each time frame (time frame is the period from one Sync-pulse to the next Sync-pulse). This is shown in the next figure.

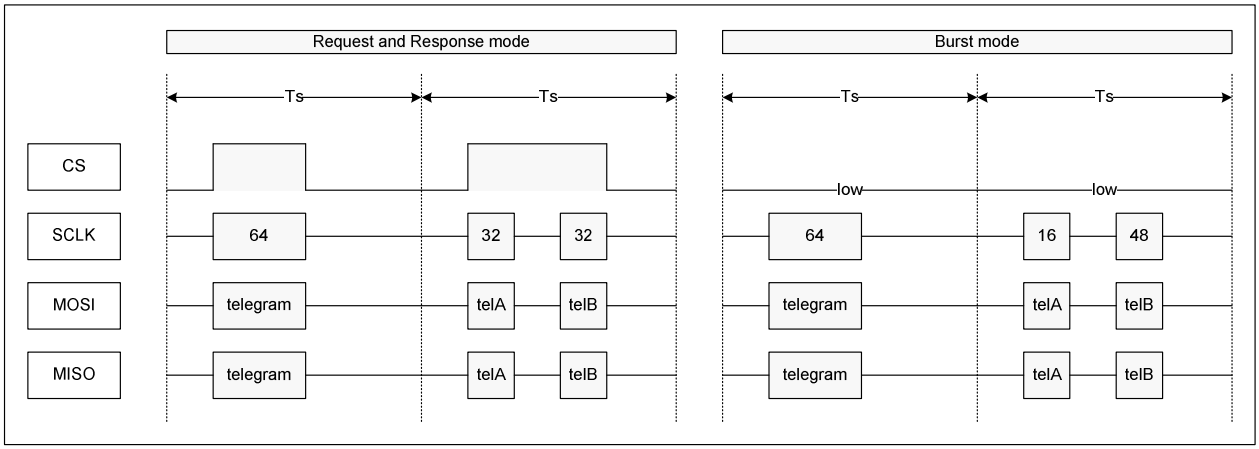


Figure 64: Telegram transmission timing diagram (example)

- In R&R mode, CS changes its state (from LOW to HIGH and then LOW again) to indicate the beginning and end of telegram transmission. In burst mode, no such change takes place, CS can remain LOW.
- The SPI clock (SCLK) is controlled by the ECU. With each clock cycle one bit is transmitted from ECU to "ATIC 116" (MOSI) or from "ATIC 116" to ECU (MISO). When no transmission takes place, SCLK is idle (no clock cycles).
- Telegram transmission does not have to occur in one piece; it can be divided into two or more pieces (e.g. telA and telB), the sum of which comprises 64 bits.
- "ATIC 116" interprets SPI input data only if they are accompanied by CS going from LOW to HIGH (which results in SPI interrupt). If CS = LOW, SPI input data are ignored.
- In R&R mode, CS change from HIGH to LOW indicates end of SPI telegram transmission (with 64 bits transmitted).
- The number of bits transmitted since the beginning of telegram transmission is stored in "SPI bit counter". With each consecutive bit, SPI bit counter value is incremented by "1". With each Sync-pulse rising edge (beginning of new time frame), SPI bit counter is reset to "zero".
- In time window T1, no SPI communication may take place (T1 definition see page 33).

The bit stream during SPI telegram transmission is shown in the figure below

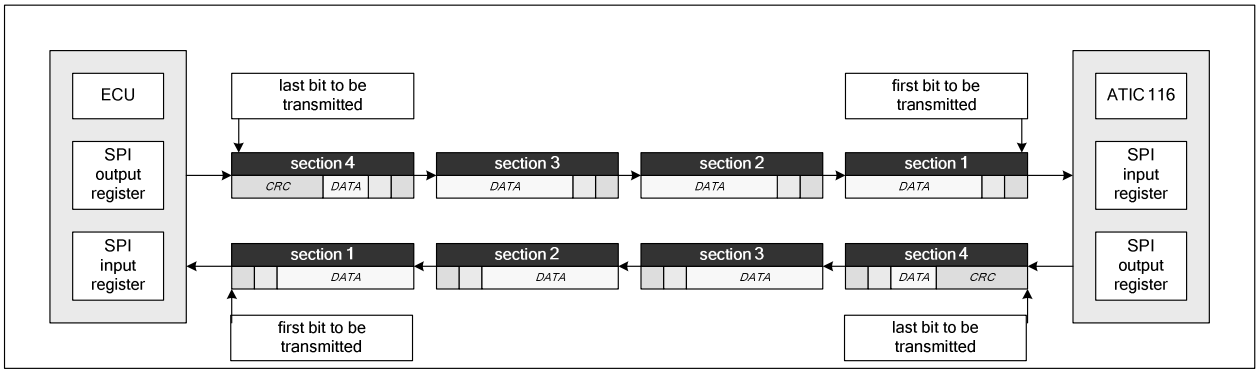


Figure 65: Bit stream during SPI telegram transmission

The first bit to be transmitted is the MSB of TeleCounter in Section 1. The last bit to be transmitted is the LSB of CRC Checksum in Section 4.

4.8 DATA

DATA contains measurement data such as speed and angle. The DATA telegram is shown in the figure below.

	DATA telegram			
TeleCounter	*SecCode*	*angle (MSB→LSB)*		
2 bit	*2 bit*	*12 bit*		
n	**00**	**XXXXXXXXXXXX**		
TeleCounter	*SecCode*	*speed1, MSS (MSB→LSB)*		
2 bit	*2 bit*	*12 bit*		
n	**01**	**XXXXXXXXXXXX**		
TeleCounter	*SecCode*	*speed2, LSS (MSB→LSB)*	*Counter (MSB→LSB)*	
2 bit	*2 bit*	*4 bit*	*8 bit*	
n	**10**	**XXXX**	**XXXXXXXX**	
TeleCounter	*SecCode*	*PWR*	*Error / Diag*	*CRC Checksum*
2 bit	*2 bit*	*1 bit*	*3 bit*	*8 bit*
n	**11**	**X**	**XXX**	**XXXXXXXX**

Figure 66: DATA telegram

- MSS is "most significant section", LSS is "least significant section"
- MSB is "most significant bit", LSB is "least significant bit"
- All values are represented with their MSB to the left, and their LSB to the right
- If a value spans over more than one section (e.g. "speed"), then bits in the section with lower SecCode (e.g. "1") are more significant than bits in the section with higher SecCode (e.g. "2"). These sections are also referred to as "more significant section" (MSS) and "least significant section" (LSS).

The actual representation of DATA values is shown in the table below (note that the resolution in the above table is "nominal resolution", and not "true resolution").

parameter	phys. range		resolution	var range	remark
angle [°]	0	360°-(360/4095)	12Bit	0x000 → 0° 0xFFF → 359,912°	1digit: app: 0.08789°
speed [eppm]	-16384	16383,5	16Bit	-16384 eppm→ 0x8000 16383.5 eppm → 0x7FFF	1digit: 0,5 eppm
sensor period counter [n]	-128	127	8Bit	0x80 → -128 0x7F → 127	1digit: 1 revol. (sensor)
power loss	0	1	1 Bit	0 ... 1	0: no power loss 1: power loss
error class	0	7	1 Bit	0 ... 7	0b100 → high 0b010 → medium 0b001 → low combination of error classes are possible

Table 22: Representation of DATA values

Error bits

All errors which can be diagnosed by the "ATIC 116" are divided into three priority classes: high, medium, and low. The error bits are 3 bits with the following meaning:

(a) 100: Error (or errors) of high-priority class has been diagnosed

(b) 010: Error (or errors) of medium-priority class has been diagnosed

(c) 001: Error (or errors) of low-priority class has been diagnosed

Combinations of (a), (b), and (c) are possible. For example, "110" means that:

- an error (or errors) of high-priority class has been diagnosed
- an error (or errors) of medium-priority class has been diagnosed
- no error (or errors) of low-priority class has been diagnosed

Error bits contain no information about which errors have been diagnosed. This information must be asked by ECU using the SPI request "get.error".

4.9 NOP

NOP means No OPeration. A NOP telegram is used whenever there is no need for SPI communication. For example, there is no need for the ECU to transmit data to "ATIC 116" over SPI if "ATIC 116" is in burst mode and should stay in burst mode.

Below, the NOP telegram is shown. Note that TeleCounter increase with each section (from "0" to "3"), whereas the SecCode remains unchanged at "3" for all 4 sections.

n.m.	*NOP*	
TeleCounter	*SecCode*	---
2 bit	*2 bit*	*12 bit*
00	**11**	**000000000000**
TeleCounter	*SecCode*	---
2 bit	*2 bit*	*12 bit*
01	**11**	**000000000000**
TeleCounter	*SecCode*	---
2 bit	*2 bit*	*12 bit*
10	**11**	**000000000000**
TeleCounter	*SecCode*	---
2 bit	*2 bit*	*12 bit*
11	**11**	**000011111111**

Figure 67: NOP telegram

4.10 Error codes

The error codes are given in the chapter on "ATIC116 diagnosis".

4.11 Burst mode

In burst mode, DATA are continuously sent from "ATIC 116" to ECU, one DATA telegram in each time frame. The transmission is performed as follows:

(1) DATA telegram is calculated in the "ATIC 116" (one DATA telegram is calculated in each time frame).

(2) DATA are shifted from "ATIC 116"'s µC to SPI input register. This is called "SPI register update" or "SPI update" and takes place at the beginning of each time frame (sync rising edge).

(3) DATA telegram is transmitted from "ATIC 116" to ECU. DATA obtained by "ATIC 116" in time frame "N" are thus transmitted over SPI in time frame "N+1".

(4) Simultaneously to (3), SPI telegram is sent from ECU to "ATIC 116". In most cases, this telegram will be NOP (No OPeration).

(5) The transmission in both directions is controlled by ECU using SCLK: with each SCLK cycle, one bit is transferred. No other control signals from the ECU (like CS) are needed in burst mode.

The above is visualized in the diagram below:

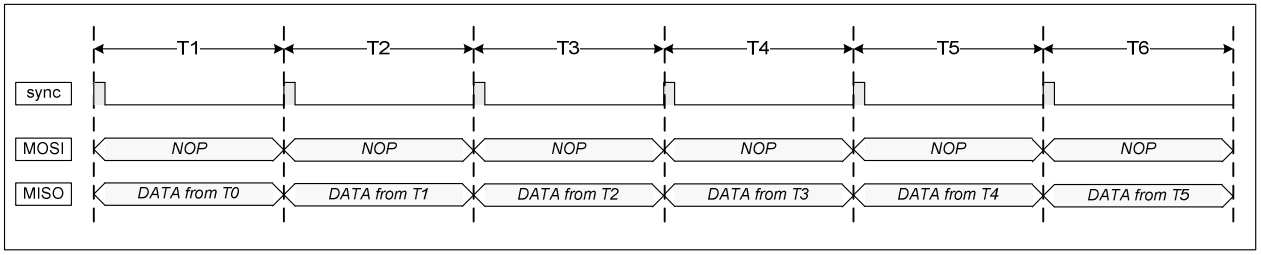


Figure 68: Burst mode

NOTE:

It is not necessary to send a NOP command on each time frame to get out data in Burst Mode. MOSI can even be a static level high or low.

4.12 Request & Response mode

In R&R mode, the communication between "ATIC 116" and ECU is done using "SPI requests" (sent by ECU) and "SPI responses" (sent by "ATIC 116"). An SPI request can be an "SPI command" (e.g. set.counter) or "SPI inquiry" (e.g. get.data).

The communication between "ATIC 116" and ECU in "Request & Response" mode (R&R) is done as follows:

(1) "ATIC 116" is in burst mode.

(2) ECU sends SPI command "exit.burst" to "ATIC 116".

(3) "ATIC 116" transitions from "burst mode" to "R&R mode".

(4) "ATIC 116" sends an SPI request.

(5) "ATIC 116" processes the SPI request, and calculates the appropriate SPI response telegram.

(6) SPI response telegram is sent.

(7) "ATIC 116" waits for new SPI request from the ECU.

(8) "ATIC 116" processes the new SPI request received in (7) and calculates new SPI response telegram, which is then sent to the ECU.

(9) Points (7) and (8) are repeated until the "ATIC 116" receives the SPI command "set.burst". Upon receiving this command, "ATIC 116" goes back to burst mode.

In R&R mode, the following points have to be observed:

- If SPI request is sent in time frame "N", then the corresponding SPI response has to be sent in time frame "N+1".
- If SPI request is sent in time frame "N", the next SPI request can be sent no sooner then in time frame "N+2".
- If the SPI request is a command, then the command execution must be over before the corresponding SPI response is sent.
- In each time frame in which "ATIC 116" sends no SPI response, "ATIC 116" sends NOP telegrams. No DATA telegrams are sent by "ATIC 116" in R&R mode.
- In each time frame in which ECU sends no SPI request, ECU sends NOP.
- The content of the SPI output register can only be updated upon Sync signal.
- CS rising edge indicates the begin of transmission of SPI request (no later than 30 µs after Sync).
- CS falling edge indicates the transmission end of SPI request (no later that 60 µs after Sync).

NOTE: For simplicity, "*after Sync*" means "*after rising edge of Sync*", and "*upon Sync*" means "*upon rising edge of Sync*".

The above points are visualized in the diagram below (at the beginning of the diagram, "ATIC 116" is in burst mode).

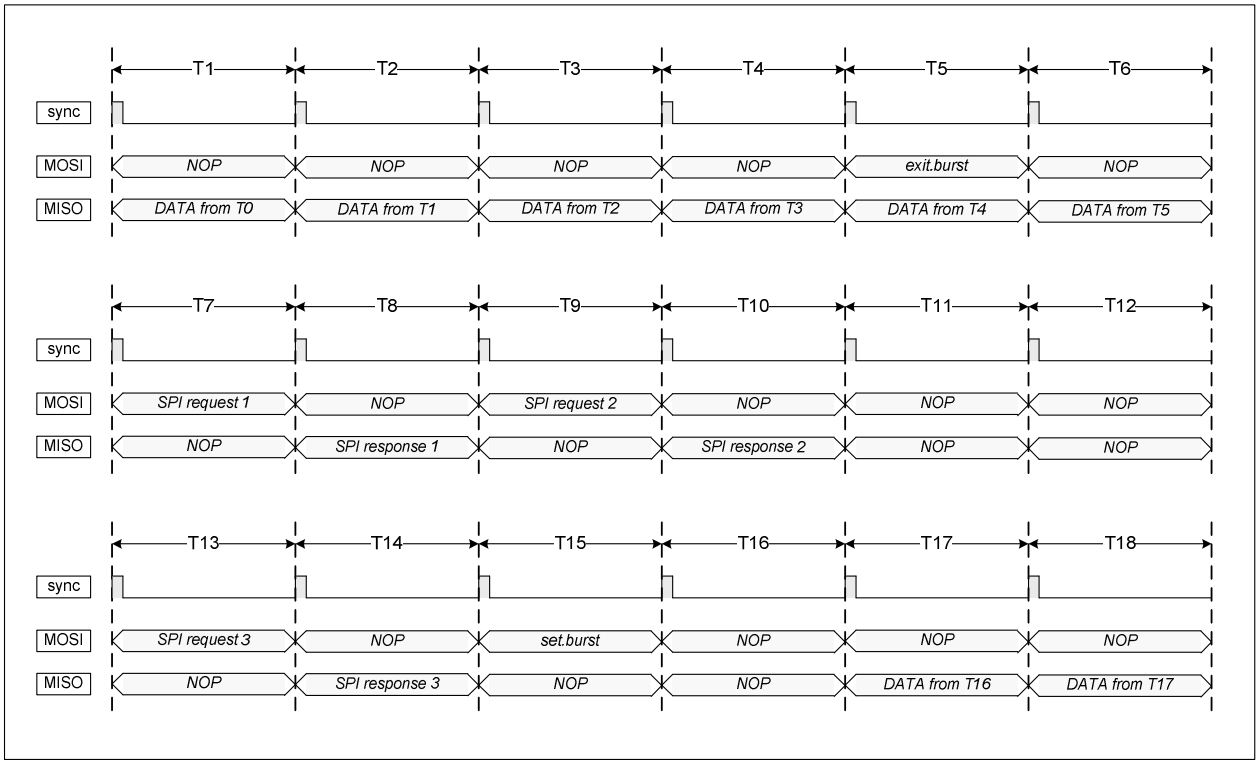


Figure 69: Transition from burst mode to R&R mode to burst mode

T1...T4	"ATIC 116" is in "burst mode"
T5	ECU sends "exit.burst"
T6	"ATIC 116" sends the last DATA telegram
T7	"ATIC 116" enters R&R mode
T7...T14	ECU sends SPI commands, each SPI command is answered by the "ATIC 116" by sending an SPI response
T15	ECU sends "set.burst"
T17	"ATIC 116" enters "burst mode" again

If an SPI command other than "exit.burst" is sent when "ATIC 116" is in burst mode, this command will be ignored. If "exit.burst" is sent in time frame "N", the next SPI command can be sent by the ECU no sooner than in time frame "N+2". In time frame "N+1", the last DATA telegram (with measurement data from time frame "N") is sent by the "ATIC 116".

4.13 SPI commands in burst and R&R mode

In the table below, codes of SPI commands available in burst mode and R&R mode are listed

Command	Request Code (4bit)	Answer Code (4bit)	Description
exit.burst	0xA		exit burst mode

Table 23: List of SPI commands available in burst mode

Command	Request Code (4bit)	Answer Code (4bit)	Description
set.counter	0x1	0x2	set low-power counters
reset.telecounter	0x3	0x4	reset telegram counter
reset.powerloss	0x5	0x6	reset power-loss bit
reset.error	0x7	0x8	reset error bits
set.burst	0x9		enter burst mode
get.error	0xB	0xC	get error bits
get.data	0xD	0xE	get data from EEPROM
set.program	0xF	0x0	enter program mode

Table 24: List of SPI commands available in R&R mode

4.14 Program mode

The program mode can be entered from R&R mode using the SPI command "set.program". This mode is used to write data to the ASIC's EPROM memory. The program mode is exited by the SPI command "esc.program". Upon this command, "ATIC 116" leaves the program mode and enters the R&R mode. In the table below, codes of SPI commands available in program mode are listed

Command	Request Code (4bit)	Answer Code (4bit)	Description
set.data	0xB	0xC	write to EEPROM
esc.program	0xE	0xF	leave program mode

Table 25: SPI commands in program mode

The basic timing pattern in the program mode is as follows: SPI request (time frame N+1) is immediately followed by the corresponding SPI response (time frame N+2). After the SPI response (time frame N+3), "ATIC 116" must be able to process the next SPI request.

The next SPI request can be sent either in the time frame immediately following the previous SPI response (N+3), or in any later time frame. This is shown in the diagram below (the optional NOP-time frames are shown grey)

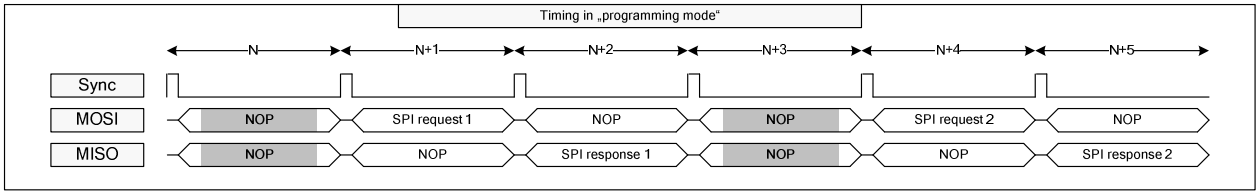


Figure 70: Timing in "programming mode"

There is one exception from the timing described above:

- writing to EEPROM using "set.data".

Writing to EEPROM

When writing to EEPROM, each pair of "SPI request" and "SPI response" must be followed by a delay of 40ms. This time is needed by the EEPROM to process the write command. This is visualized in the diagram below.

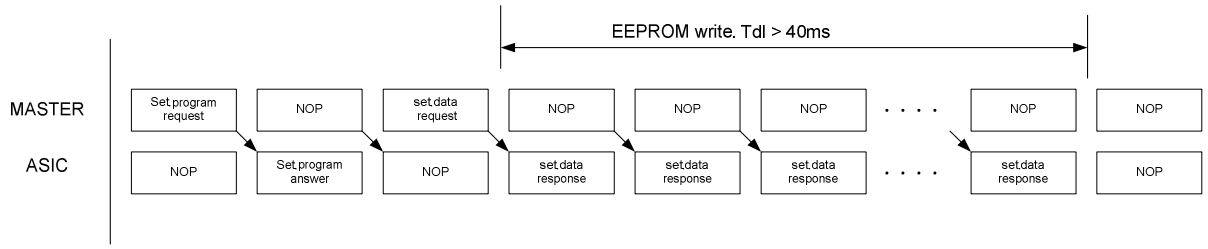


Figure 71: Timing diagram for writing into EEPROM

The procedure is the following:

1) The Master sends the set.data command

2) The ASIC receives the command and recognizes it as correct command. Then it updates the SPI shadow register with response of the set.data command

3) The Master sends NOP command and the ASIC respond with answer of set.data command

4) The ASIC starts to write into EEPROM

5) If Master send any command during the time when the ASIC performs EEPROM write, it will receive as an answer the answer to the set.data command

- because the SPI shadow register is no longer updated (because of the EEPROM writing, all interrupts are disabled), on every SYNC pulse, the ASIC updates its SPI shift register with the last answer

6) If Master continues to send NOP or some other command, as soon as the EEMPROM write is finished (interrupts are enabled), the ASIC will respond with NOP or with the answer to the last send command

NOTE:

In the Figure 71 above the NOP command during EEPROM write is used as an example; it can be any other defined command.

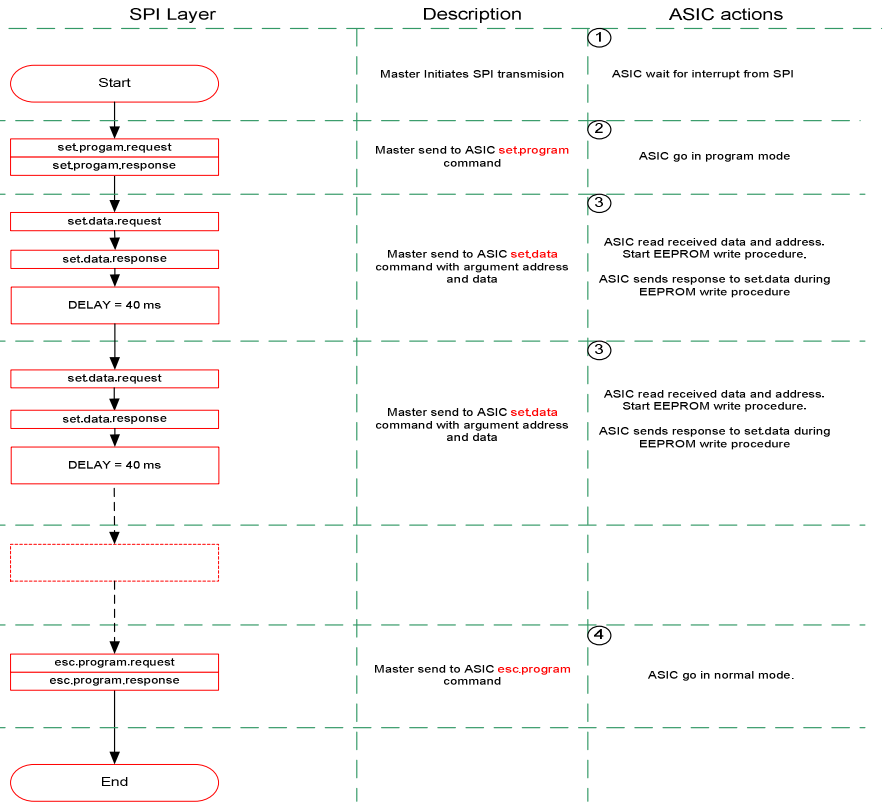


Figure 72: Flow chart for writing into EEPROM

EEPROM memory is logically divided into two areas (Melexis area and Conti area). To avoid undesired EEPROM writing both software and hardware protections are implemented.

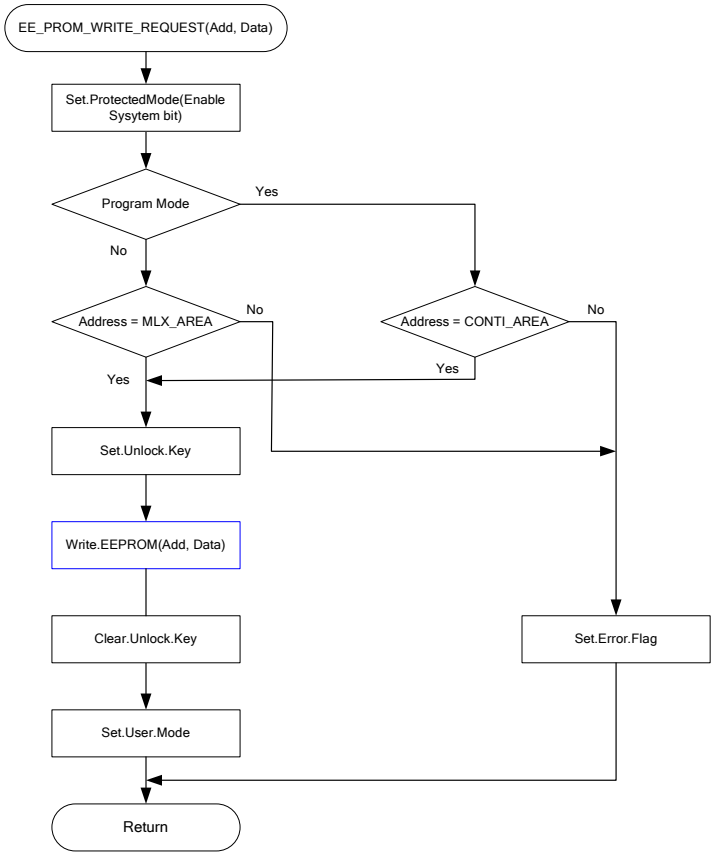


Figure 73: Flow chart for processing the SPI command "set.data"

Trying to write into protected EEPROM area will cause no effect over the "ATIC 116" (except that an appropriate error flag will be set). Hardware protections include 7bit IO and program mode bit. Software protections include System Bit, and checks with software keys in RAM.

4.15 Bits vs. SCLK timing

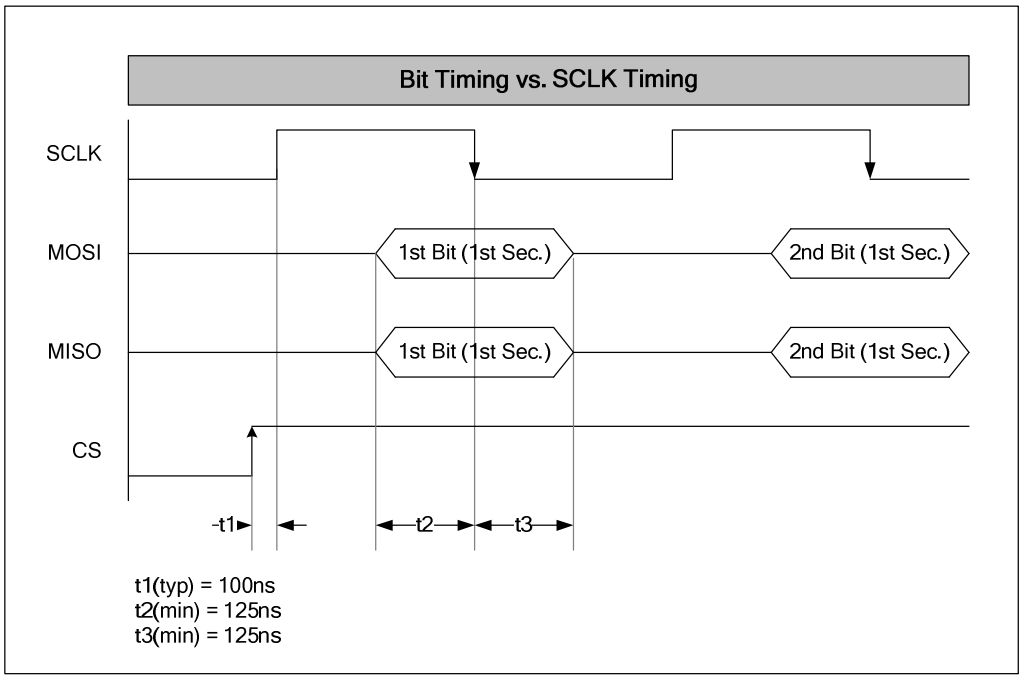


Figure 74: Bit timing vs. SCLK timing

During each SCLK cycle, one bit is transmitted from ECU to "ATIC 116" (MOSI) and one bit is transmitted from "ATIC 116" to ECU (MISO). Each bit must have a valid value (LOW or HIGH) in the direct proximity of the SCLK falling edge. This is shown in the figure above.

4.16 SPI telegrams, details

Below, the SPI telegrams for all valid SPI requests and response are shown. If certain bits in the telegram are not used, they are set by default to "0" which is indicated as "00000000". If certain bits in the telegram are used, this is indicated as "XXXXXXXX".

TeleCounter

The calculation algorithm for telegram counter depends on the mode in which the "ATIC 116" is operating:

(a) wrap-up behavior: TeleCounter will count following this sequence: 0, 1, 2, 3, 0, 1, 2, 3, 0... (or, in binary numbers, 00, 01, 10, 11, 00, 01, 10, 11, 00 ...)

(b) burst mode: TeleCounter increments by "1" with each DATA telegram sent

(c) R&R mode: If TeleCounter of "SPI request" is "n", then TeleCounter of the corresponding "SPI response" is "n+1". If n = 3 (binary 11), then n+1 = 0 (binary 0): (wrap-up behavior)

(d) R&R mode and "NOP": the algorithm for TeleCounter increment described in point (c) is valid for all SPI responses in R&R mode except NOP; the TeleCounter calculation for NOP is described in chapter about NOP.

Below, the SPI telegrams for all valid SPI requests and response are shown.

4.16.1 Burst mode

There are only two valid telegrams in burst mode:

- DATA telegram which is sent from "ATIC 116" to ECU
- "exit.burst" telegram which is sent from ECU to "ATIC 116"

	DATA telegram			
TeleCounter	*SecCode*	*angle (MSB→LSB)*		
2 bit	*2 bit*	*12 bit*		
n	**00**	**XXXXXXXXXXXX**		
TeleCounter	*SecCode*	*speed1, MSS (MSB→LSB)*		
2 bit	*2 bit*	*12 bit*		
n	**01**	**XXXXXXXXXXXX**		
TeleCounter	*SecCode*	*speed2, LSS (MSB→LSB)*	*Counter (MSB→LSB)*	
2 bit	*2 bit*	*4 bit*	*8 bit*	
n	**10**	**XXXX**	**XXXXXXXX**	
TeleCounter	*SecCode*	*PWR*	*Error / Diag*	*CRC Checksum*
2 bit	*2 bit*	*1 bit*	*3 bit*	*8 bit*
n	**11**	**X**	**XXX**	**XXXXXXXX**

MSS: most significant section

LSS: least significant section

Request	exit.burst		
TeleCounter	*SecCode*	*Command Code*	---
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**00**	**1010**	**00000000**
TeleCounter	*SecCode*	*Command Code*	---
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**01**	**1010**	**00000000**
TeleCounter	*SecCode*	*Command Code*	---
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**10**	**1010**	**00000000**
TeleCounter	*SecCode*	*Command Code*	*CRC Checksum*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**11**	**1010**	**XXXXXXXX**

4.16.2 Request & Response mode

set.counter

Request	set.counter		
TeleCounter	*SecCode*	*Command Code*	*---*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**00**	**0001**	**00000000**
TeleCounter	*SecCode*	*Command Code*	*---*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**01**	**0001**	**00000000**
TeleCounter	*SecCode*	*Command Code*	*Counter Value*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**10**	**0001**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*CRC Checksum*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**11**	**0001**	**XXXXXXXX**

Response	set.counter		
TeleCounter	*SecCode*	*Command Code*	*---*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**00**	**0010**	**00000000**
TeleCounter	*SecCode*	*Command Code*	*---*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**01**	**0010**	**00000000**
TeleCounter	*SecCode*	*Command Code*	*Counter Value (repeat from request)*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**10**	**0010**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*CRC Checksum*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**11**	**0010**	**XXXXXXXX**

reset.telecounter

Request	reset.telecounter (default: 0)		
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	00	0x3	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	01	0x3	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	10	0x3	00000000
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n	11	0x3	XXXXXXXX

Response	reset.telecounter (default: 0)		
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
0	00	0x4	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
0	01	0x4	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
0	10	0x4	00000000
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
0	11	0x4	XXXXXXXX

reset.powerloss

Request	reset.powerloss (default: 1)		
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**00**	**0x5**	**00000000**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**01**	**0x5**	**00000000**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**10**	**0x5**	**00000000**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n	**11**	**0x5**	**XXXXXXXX**

Response	reset.powerloss (default: 1)		
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n+1	**00**	**0x6**	**00000000**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n+1	**01**	**0x6**	**00000000**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n+1	**10**	**0x6**	**00000000**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n+1	**11**	**0x6**	**XXXXXXXX**

reset.error

Request	reset.error		
TeleCounter	SecCode	Command Code	errors to be reset (most significant byte)
2 bit	2 bit	4 bit	8 bit
n	**00**	**0x7**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	errors to be reset (medium significant byte)
2 bit	2 bit	4 bit	8 bit
n	**01**	**0x7**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	errors to be reset (least significant byte)
2 bit	2 bit	4 bit	8 bit
n	**10**	**0x7**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n	**11**	**0x7**	**XXXXXXXX**

Response	reset.error		
TeleCounter	SecCode	Command Code	reset errors (most significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**00**	**0x8**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	reset errors (medium significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**01**	**0x8**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	reset errors (least significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**10**	**0x8**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n+1	**11**	**0x8**	**XXXXXXXX**

NOTE: Error code explanation is given in the chapter "ATIC116 diagnosis"

set.burst

Request	set.burst		
TeleCounter	*SecCode*	*Command Code*	---
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**00**	**0x9**	**00000000**
TeleCounter	*SecCode*	*Command Code*	---
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**01**	**0x9**	**00000000**
TeleCounter	*SecCode*	*Command Code*	---
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**10**	**0x9**	**00000000**
TeleCounter	*SecCode*	*Command Code*	*CRC Checksum*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**11**	**0x9**	**XXXXXXXX**

get.error

Request	get.error		
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**00**	**0xB**	**00000000**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**01**	**0xB**	**00000000**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**10**	**0xB**	**00000000**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n	**11**	**0xB**	**XXXXXXXX**

Response	get.error		
TeleCounter	SecCode	Command Code	error code (most significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**00**	**0xC**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	error code (medium significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**01**	**0xC**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	error code (least significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**10**	**0xC**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n+1	**11**	**0xC**	**XXXXXXXX**

NOTE: Error code explanation is given in the chapter "ATIC116 diagnosis"

get.data

Request	get.data		
TeleCounter	SecCode	Command Code	EEPROM Address
2 bit	2 bit	4 bit	8 bit
n	**00**	**0xD**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**01**	**0xD**	**00000000**
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	**10**	**0xD**	**00000000**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n	**11**	**0xD**	**XXXXXXXX**

Response	get.data		
TeleCounter	SecCode	Command Code	EEPROM Address (repeat from request)
2 bit	2 bit	4 bit	8 bit
n+1	**00**	**0xE**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	Data (most significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**01**	**0xE**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	Data (least significant byte)
2 bit	2 bit	4 bit	8 bit
n+1	**10**	**0xE**	**XXXXXXXX**
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n+1	**11**	**0xE**	**XXXXXXXX**

set.program

Request	set.program		
TeleCounter	SecCode	Command Code	Program Entry Key
2 bit	2 bit	4 bit	8 bit
n	00	0xF	XXXXXXXX
TeleCounter	SecCode	Command Code	Optional: MLX Key or Conti Key
2 bit	2 bit	4 bit	8 bit (High Byte)
n	01	0xF	XXXXXXXX
TeleCounter	SecCode	Command Code	Optional: MLX Key or Conti Key
2 bit	2 bit	4 bit	8 bit (Low Byte)
n	10	0xF	XXXXXXXX
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n	11	0xF	XXXXXXXX

Response	set.program		
TeleCounter	SecCode	Command Code	Program Entry Key
2 bit	2 bit	4 bit	8 bit
n+1	00	0x0	XXXXXXXX
TeleCounter	SecCode	Command Code	Optional: MLX Key or Conti Key
2 bit	2 bit	4 bit	8 bit (High Byte)
n+1	01	0x0	XXXXXXXX
TeleCounter	SecCode	Command Code	Optional: MLX Key or Conti Key
2 bit	2 bit	4 bit	8 bit (Low Byte)
n+1	10	0x0	XXXXXXXX
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n+1	11	0x0	XXXXXXXX

4.16.3 Programming mode

set.data

Request	set.data		
TeleCounter	*SecCode*	*Command Code*	*EEPROM Address*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**00**	**0xB**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*Data (High Byta)*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**01**	**0xB**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*Data (Low Byte)*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**10**	**0xB**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*CRC Checksum*
2 bit	*2 bit*	*4 bit*	*8 bit*
n	**11**	**0xB**	**XXXXXXXX**

Response	set.data		
TeleCounter	*SecCode*	*Command Code*	*EEPROM Address*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**00**	**0xC**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*Data (High Byte)*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**01**	**0xC**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*Data (Low Byte)*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**10**	**0xC**	**XXXXXXXX**
TeleCounter	*SecCode*	*Command Code*	*CRC Checksum*
2 bit	*2 bit*	*4 bit*	*8 bit*
n+1	**11**	**0xC**	**XXXXXXXX**

esc.program

Request	esc.program		
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	00	0xE	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	01	0xE	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n	10	0xE	00000000
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n	11	0xE	XXXXXXXX

Response	esc.program		
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n+1	00	0xF	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n+1	01	0xF	00000000
TeleCounter	SecCode	Command Code	---
2 bit	2 bit	4 bit	8 bit
n+1	10	0xF	00000000
TeleCounter	SecCode	Command Code	CRC Checksum
2 bit	2 bit	4 bit	8 bit
n+1	11	0xF	XXXXXXXX

4.17 EEPROM

4.17.1 General description

EEPROM memory will be implemented in the "ATIC 116". The size of the EEPROM memory is 64*16 bits (64 words, 1 word = 2 bytes (high-byte and low-byte)). The EEPROM memory will be divided in two areas: MELEXIS area and CONTI area. The CONTI area will be further divided into a protected area, and an unprotected area. This is visualized in the diagram below:

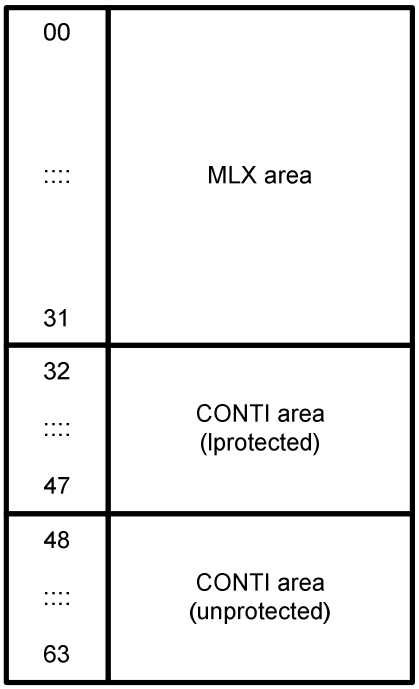


Figure 75: EEPROM overview

MELEXIS area (Words 00 ... 31)

In this area Melexis parameters are stored. The area is write-protected: only Melexis can write into this area; neither Conti nor its customers can write into this area.

CONTI protected (Words 32 ... 47)

In this area Conti parameters necessary for proper "ATIC 116" function are stored. The area is key-protected: only by sending a correct key it is possible to write into this area.

CONTI unprotected (Words 48 ... 63)

This area is used as backup to store parameters usually used by the ECU. It is possibly to freely write into this area without any limitations.

Read operation

Read operation is possible without any limitations for all three areas.

Key protection

A key is a pre-defined combination of bits; several functions can only be initiated by sending a correct key.

Program-entry key

This key is necessary to change the "ATIC 116" mode from "R&R mode" to "program mode".

Program-escape key

This key is necessary to change the "ATIC 116" mode from "program mode" to "R&R mode".

MELEXIS key

This key is necessary to write into the MELEXIS area.

CONTI key

This key is necessary to write into the CONTI lockable area.

Key name	Function	Width	Value
Program-entry key	Transition from "R&R mode" to "program mode"	8 bit	0xC9
Program-escape key	Transition from "program mode" to "R&R mode"	8 bit	0x36
MELEXIS key	Write to EEPROM MELEXIS area	16 bit	N.A.
CONTI key	Write to EEPROM CONTI lockable area	16 bit	0xACBD

Table 26: Overview of keys used for EEPROM access

Writing to MELEXIS area

This operation will be performed in the following way:

1) "ATIC 116" is in R&R mode.
2) ECU sends "set.program"; this command contains two keys: program-entry key and MELEXIS key. *)
3) ECU writes parameters into MELEXIS area using "set.data"; this command contains no keys.
4) ECU sends "esc.program"; this command contains the program-escape key.
5) "ATIC 116" goes back to R&R mode.

Writing to CONTI protected area

This operation will be performed in the following way:

6) "ATIC 116" is in R&R mode.

7) ECU sends "set.program"; this command contains two keys: program-entry key and CONTI key. *)
8) ECU writes parameters into CONTI lockable area using "set.data"; this command contains no keys.
9) ECU sends "esc.program"; this command contains the program-escape key.
10) "ATIC 116" goes back to R&R mode.

Writing to CONTI unprotected area

This operation will be performed in the following way:

11) "ATIC 116" is in R&R mode.
12) ECU sends "set.program"; this command contains one key: program-entry key.
13) ECU writes parameters into CONTI lockable area using "set.data"; this command contains no keys.
14) ECU sends "esc.program"; this command contains the program-escape key.
15) "ATIC 116" goes back to R&R mode.

EEPROM operation

The EEPROM contains several parameters which are necessary for proper function of the "ATIC 116". Upon "wake-up" (transition from low-power mode to active mode) the content of the EEPROM is read out and temporarily stored in RAM.

During operation, "ATIC 116" does not use the data stored in EEPROM; instead, it uses the mirror image of the data in RAM. In this way the access to EEPROM parameters is much faster.

**): writing to protected area using a false key will lead to ASIC hang-up. Exit is only possible by Wake-up or by reset (using pin Reset).*

EEPROM CRC

The data stored in EEPROM can get corrupted. For that reason, two CRC checksums will be used: CRC1 and CRC2. CRC1 covers the entire EEPROM area (except the addresses where CRC1 and CRC2 are stored). CRC2 covers all real-time relevant parameters (see EEPROM map below for details).

The calculation of both CRC checksums is conducted whenever the "ATIC 116" is in burst mode. It is done at regular intervals in the background loop (together with other diagnosis-related tasks) using parameters temporarily stored in RAM.

4.17.2 User-settable EEPROM parameters

There are several EEPROM parameters which can be changed by the user. Most of them are stored in the CONTI protected area. One parameter (EE_Transport_Mode) is stored in the CONTI unprotected area. There are no user-settable parameters in the MELEXIS area.

User-settable EEPROM parameters, protected area

In the table below an overview of the user-settable parameters in CONTI protected area is shown.

ADR (HEX)	No. (DEC)	Contents	Comment
2040	32	EE_EXER_SIN	
2042	33	EE_EXER_COS	
2044	34	EE_RADIUS_HIGH	
2046	35	EE_RADIUS_LOW	
2048	36	EE_K1	
204A	37	EE_K2	
204C	38	EE_TS	
204E	39	EE_ERROR_PACK	
2050	40	EE_ERROR_PACK	
2052	41	EE_CALIBMODE	bit[15]

Table 27: User settable EEPROM parameters, protected area

EE_EXER_SIN, EE_EXER_COS

These parameters contain the sensor excentricity error (described above) compensation parameters. They have to be empirically determined. To disable excentricity compensation set both parameters to zero.

EE_RADIUS_HIGH, EE_RADIUS_LOW

According to trigonometrical Pythagoras, it is sin^2 + cos^2 = 1. A similar relationship is valid for the MR sensor output signals: SIN^2 + COS^2 = RADIUS, where SIN and COS are MR sensor output signals after digitization and sensor error compensation.

The actual radius calculation is performed according to the formula given below, where ADC^2_{SIN} and ADC^2_{COS} are the digitized amplitudes of the SIN and COS signals after dynamic compensation expressed in digits (see also chapter “ATIC116 Diagnosis”, Radius evaluation)

$$RADIUS\_CALCULATED = \left(ADC^2_{SIN} + ADC^2_{COS}\right) / 2^{16}$$

Ideally, SIN_{MAX} = COS_{MAX} = RADIUS = 0x1000 = 4096 (dec). Allowing a calculated radius error of 30% yields:

radius_calculated_high = 4096 * 1.30 = 5324 (dec) = 0x14CC

radius_calculated_low = 4096 * 0.70 = 2867 (dec) = 0x0B33

The EEPROM values are then:

EE_RADIUS_HIGH = 0x14CC

EE_RADIUS_LOW = 0x0B33

EE_K1, EE_K2, EE_TS

These parameters describe the dynamic behavior of the tracking loop. The tracking loop parameters K1 and K2 can be derived from the tracking loop parameters ω and δ (as described in the chapter about tracking loop). The parameter Ts (sample time) describes the time interval at which the tracking loop is executed.

During execution of the tracking loop, K1 is multiplied with Ts. Thus -- to reduce calculation time -- the value K1*Ts instead of K1 is stored as EE_K1.

Before the tracking loop parameters K1, K2, and Ts are stored in EEPROM, they must be multiplied with appropriate scaling factors. The resulting formulas are:

$$K_1 = \omega^2$$

$$K_2 = \frac{2 \cdot \delta}{\omega}$$

$$EE\_K1 = 0.707 \cdot K_1 \cdot \frac{T_S(in\_\mu\sec)}{10^6}$$

$$EE\_K2 = K_2 \cdot 2^{16}$$

$$EE\_TS = \frac{T_S(in\_\mu\sec)}{10^6} \cdot 2^{26}$$

Example

The parameter values are assumed to be: ω = 2000, δ = 0.75, Ts = 125 µs.

The EEPROM parameters are then calculated:

$$K_1 = \omega^2 = 2000^2 = 4{,}000{,}000$$

$$K_2 = \frac{2 \cdot \delta}{\omega} = \frac{2 \cdot 0.75}{2000} = 0.00075$$

$$EE\_K1 = 0.707 \cdot 4{,}000{,}000 \cdot \frac{125}{10^6} = 353.5(dec) = 0x161$$

$$EE\_K2 = 0.00075 \cdot 2^{16} = 49.152(dec) = 0x31$$

$$EE\_TS = \frac{125}{10^6} \cdot 2^{26} = 8388.6 = 0x20C5$$

Consequently, the following values are stored in EEPROM:

EE_K1 = 0x161; EE_K2 = 0x31; EE_TS = 0x20C5

EE_ERROR_PACK

The error parameters INC, DEC, and THR – which are stored in EE_ERROR_PACK – have been discussed in chapter on "ATIC116 diagnosis".

EE_CALIBMODE

Dynamic Compensation:

There are two kinds of sensor error compensation implemented in the "ATIC 116": static compensation and dynamic compensation.

Static compensation is performed using compensation parameters obtained during calibration the "ATIC 116" after assembly; these parameters are "static" in that they are not changed during the lifetime of ATIC 116.

Dynamic compensation, on the other hand, is performed using compensation parameters continuously updated during runtime. It can be enabled or disabled using the EEPROM parameter EE_CALIBMODE:

CALIBMODE[15] = 0x1 ==> dynamic compensation is disabled

CALIBMODE[15] = 0x0 ==> dynamic compensation is enabled

Speed Filtering:

Description of Speed filtering see chapter Tracking Loop. The Speed filtering can be enabled or disabled using EEPROM parameter EE_CALIBMODE:

CALIBMODE[7] = 0 ==> speed filtering disabled

CALIBMODE[7] = 1 ==> speed filtering enabled

User-settable EEPROM parameters, unprotected area

There is just one user-settable parameter in CONTI unprotected area.

ADR (HEX)	No. (DEC)	Contents	Comment
2060	48	EE_TRANSPORT_MODE	bit[0]

Table 28: User-settable EEPROM parameters, unprotected area

Upon Wake-up = 0, the ASIC will transition from active mode to either low-power mode or to transport mode, depending on EE_TRANSPORT_MODE:

EE_TRANSPORT_MODE[0] = 0x0 ==> transition from "active mode" to "low-power mode"

EE_TRANSPORT_MODE[0] = 0x1 ==> transition from "active mode" to "transport mode"

4.17.3 EEPROM table

EEPROM map, Melexis area

ADR (HEX)	No. (DEC)	Contents	Real-Time relevant?	Default value	area
2000	0	EE_CRC_1		Computed	MLX Area
2002	1	EE_CRC_2		Computed	
2004	2	EE_T25	Yes	Trimmed	
2006	3	EE_CO2_SIN	Yes	Trimmed	
2008	4	EE_CO2_COS	Yes	Trimmed	
200A	5	EE_CO1H_SIN	Yes	Trimmed	
200C	6	EE_CO1H_COS	Yes	Trimmed	
200E	7	EE_CO1C_SIN	Yes	Trimmed	
2010	8	EE_CO1C_COS	Yes	Trimmed	
2012	9	EE_CA2_SIN	Yes	Trimmed	
2014	10	EE_CA2_COS	Yes	Trimmed	
2016	11	EE_CA1H_SIN	Yes	Trimmed	
2018	12	EE_CA1H_COS	Yes	Trimmed	
201A	13	EE_CA1C_SIN	Yes	Trimmed	
201C	14	EE_CA1C_COS	Yes	Trimmed	
201E	15	EE_ANA_LOW_PWR1		Trimmed	
2020	16	EE_ANA_LOW_PWR2		Trimmed	
2022	17	EE_ANA_HIGH_PWR1		Trimmed	
2024	18	EE_ANA_HIGH_PWR2		Trimmed	
2026	19	EE_MLX_RESERVED		Trimmed	
2028	20	EE_MLXID1		Computed	
202A	21	EE_MLXID2		Computed	
202C	22	EE_MLXID3		Computed	
202E	23	EE_MLXID4		Computed	
2030	24	EE_OSC_LO_THR		0x0074	
2032	25	EE_OSC_HI_THR		0x008C	
2034	26	MLX_FREE		NA	
2036	27	MLX_FREE		NA	
2038	28	MLX_FREE		NA	
203A	29	MLX_FREE		NA	
203C	30	MLX_FREE		NA	
203E	31	MLX_FREE		NA	

Table 29: EEPROM map, Melexis area

EEPROM map, CONTI area

ADR (HEX)	No. (DEC)	Contents	Real-Time relevant?	Default value	area
2040	32	EE_EXER_SIN	Yes	0x0000	CONTI Area lockable
2042	33	EE_EXER_COS	Yes	0x0000	
2044	34	EE_RADIUS_High		0x14CC	
2046	35	EE_RADIUS_Low		0x0B33	
2048	36	EE_K1	Yes	0x0162	
204A	37	EE_K2	Yes	0x0031	
204C	38	EE_Ts	Yes	0x20C5	
204E	39	EE_ERROR_PACK_2_1		0x2070	
2050	40	EE_ERROR_PACK_4_3		0x2025	
2052	41	EE_CALIBMODE	Yes	0x80	
2054	42	USR_lockable		0	
2056	43	USR_lockable		0	
2058	44	USR_lockable		0	
205A	45	USR_lockable		0	
205C	46	USR_lockable		0	
205E	47	USR_lockable		0	
2060	48	EE_Transport_Mode	bit[0]	0x0000	CONTI area non-lockable
2062	49	USR_non_lockable		0	
2064	50	USR_non_lockable		0	
2066	51	USR_non_lockable		0	
2068	52	USR_non_lockable		0	
206A	53	USR_non_lockable		0	
206C	54	USR_non_lockable		0	
206E	55	USR_non_lockable		0	
2070	56	USR_non_lockable		0	
2072	57	USR_non_lockable		0	
2074	58	USR_non_lockable		0	
2076	59	USR_non_lockable		0	
2078	60	USR_non_lockable		0	
207A	61	USR_non_lockable		0	
207C	62	USR_non_lockable		0	
207E	63	USR_non_lockable		0	

Table 30: EEPROM map, CONTI area

5 State Transitions

5.1 State Overview

In the above text, several state diagrams have been discussed. They are now compiled into one overview state diagram containing all major states which can be expected during "ATIC 116" calibration and operation. This diagram is shown below.

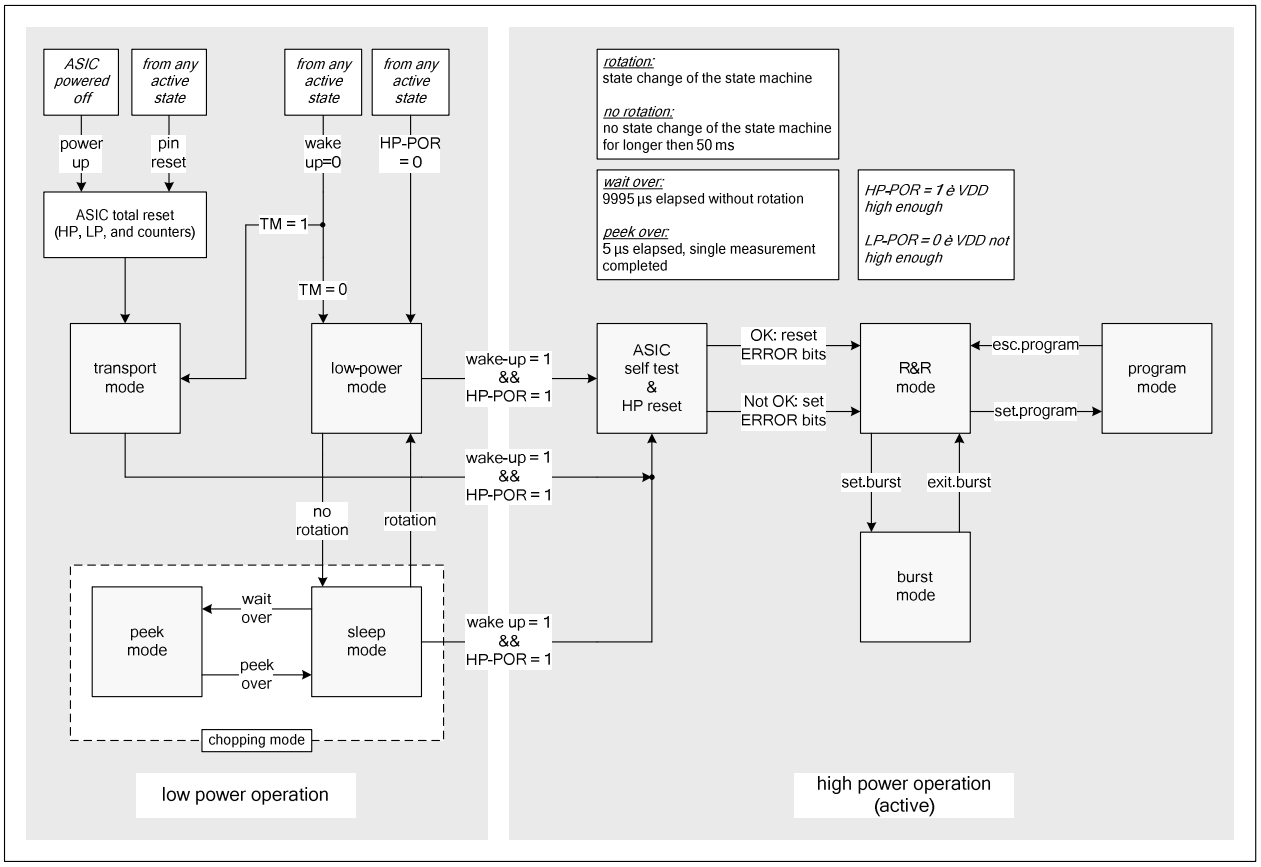


Figure 76: ATIC 116 overview of state transitions

As can be seen, all states can be divided into (1) low-power states, and (2) high-power states. Among the high-power states, several SPI states can be distinguished: (a) "R&R", (b) "burst", and (c) "program mode".

Note:

Turn counting function is ON in all low-power modes and all high-power modes. Tracking-loop calculation is ON in "burst mode"; it is OFF in all other modes.

5.2 Power-Up and Wake-Up

Power-Up

Power-Up occurs when the "ATIC 116" supply voltage is switched on. This is the case, for example, when car battery is disconnected, and then connected again.

Wake-Up

Wake-Up occurs when the "ATIC 116" transitions from any non-active mode into the active mode. It is initiated by a positive edge on the "Wake-Up" pin.

Sleep-Down

Sleep-Down occurs when the "ATIC 116" transitions from active mode into low-power mode. It is initiated by a negative edge on the "Wake-Up" pin.

5.3 Reset

Two different reset procedures are implemented in the "ATIC 116": (a) total reset and (b) HP reset.

Total reset

When "total reset" is executed then the following actions are performed:

1) HP digital is reset
2) LP digital is reset
3) Both LP rotation counters are reset

"Total reset" is executed upon:

a) Power-Up
b) Pin reset

HP reset

When "HP reset" is executed then the following actions are performed:

1) HP logic is reset
2) EEPROM parameters are loaded into RAM

"HP reset" is executed upon any transition from any non-active mode (such as chopping mode) into active mode.

5.4 State transitions in active mode

In active mode, the following transitions are possible:

(1) "R&R" to "burst mode", and "burst mode" to "R&R"

(2) "R&R" to "PROGRAM mode"

(3) "PROGRAM mode" to "R&R mode"

These transitions are shown in the figures below (note: no SPI response for set.burst and exit.burst):

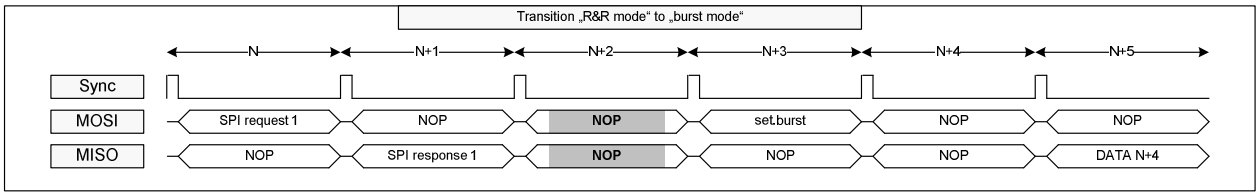


Figure 77: Transition "R&R mode" to "burst mode"

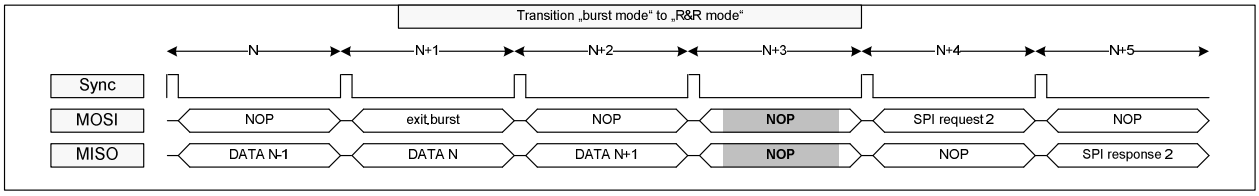


Figure 78: Transition "burst mode" to "R&R mode"

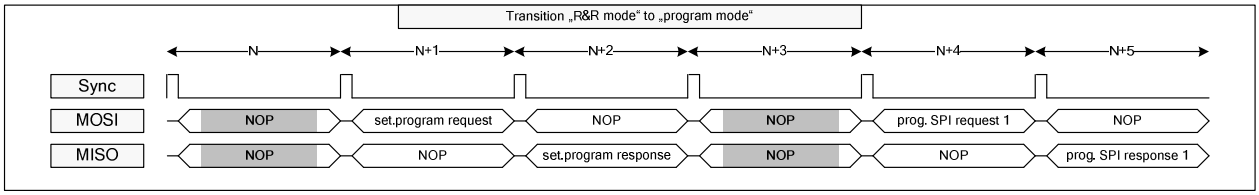


Figure 79: Transition "R&R mode" to "program mode"

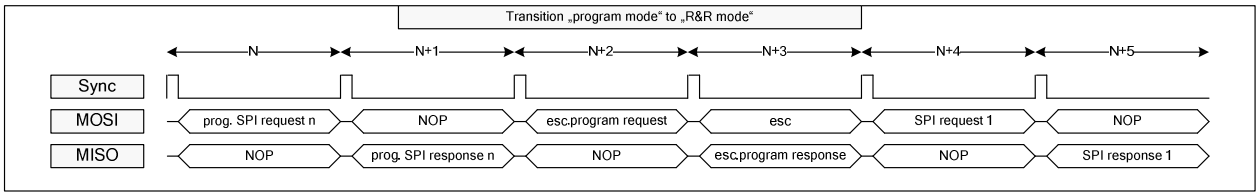


Figure 80: Transition "program mode" to "R&R mode"

Comment:

In "R&R mode" and "program mode", the communication between ECU and "ATIC 116" consists of SPI requests (sent by ECU to "ATIC 116") and SPI responses (sent by "ATIC 116" to ECU). Each ECU request is followed by the corresponding "ATIC 116" response.

The next SPI request can be sent by the ECU immediately after the "ATIC 116" response to the previous SPI request, or several "empty" telegrams or “empty” time slots after the "ATIC 116" response. These "empty" telegrams consist of NOP being transmitted on both MOSI and MISO lines and are shown in the diagrams above as grey-filled fields. During empty time slots CS and CLK may remain on static level.

5.5 State transitions between low-power modes

The two important state transitions between low-power modes are:

(1) Transition from "chopping mode" to "low-power mode"

(2) Transition from "low-power mode" to "chopping mode"

These transitions are shown in the figure below.

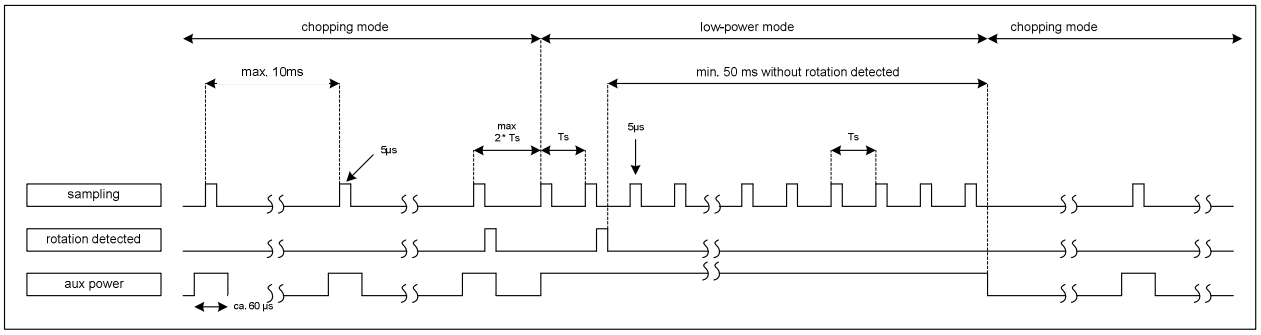


Figure 81: Transition "chopping mode" to "low-power mode" to "chopping mode"

5.6 State transitions from low-power modes to active mode

The two important state transitions from low-power modes to active mode are:

(3) Transition from "chopping mode" to "active mode"

(4) Transition from "low-power mode" to "active mode"

These transitions are shown in the figures below.

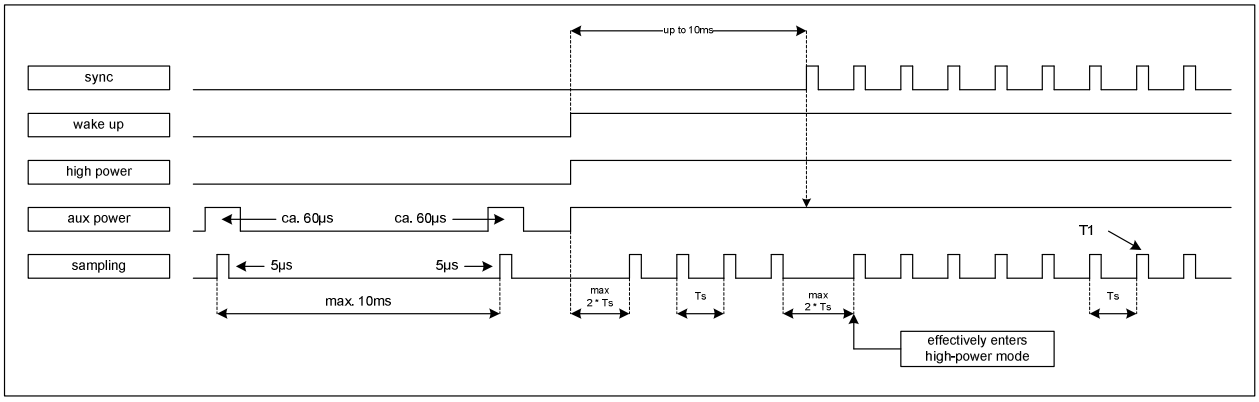


Figure 82: Transition from "chopping mode" to "active mode"

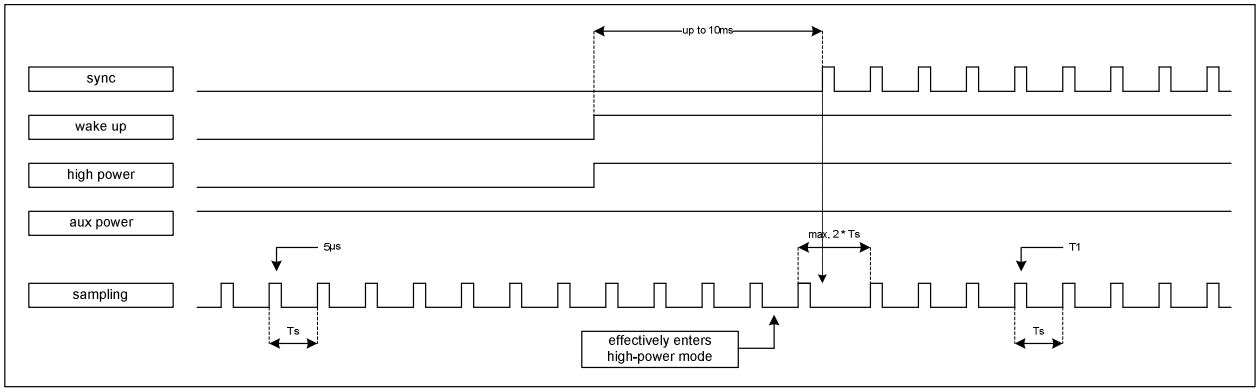


Figure 83: Transition from "low-power mode" to "active mode"

Upon entering the active mode, "ATIC 116" enters the SPI mode "R&R mode" and stays in this mode. Other SPI modes must be explicitly entered by using "set.burst" or "set.program".

It is important that no turning information is lost during the transition process. For that reason, it is necessary that the "ATIC 116" begins sampling (with sample time Ts) no later than 2*Ts after "wake-up" signal.

It is possible that the wake-up signal occurs during transition from "chopping mode" to "low-power mode" or from "low-power mode" to "chopping mode". In such case, the "wake-up" signal overrides the other transitions. However, no turning information may be lost during the transition, so it may be necessary to finish calculation tasks (like state machine calculation) already running.

5.7 State transition from active mode to low-power mode

The transition from active mode to low-power mode is shown in the figure below.

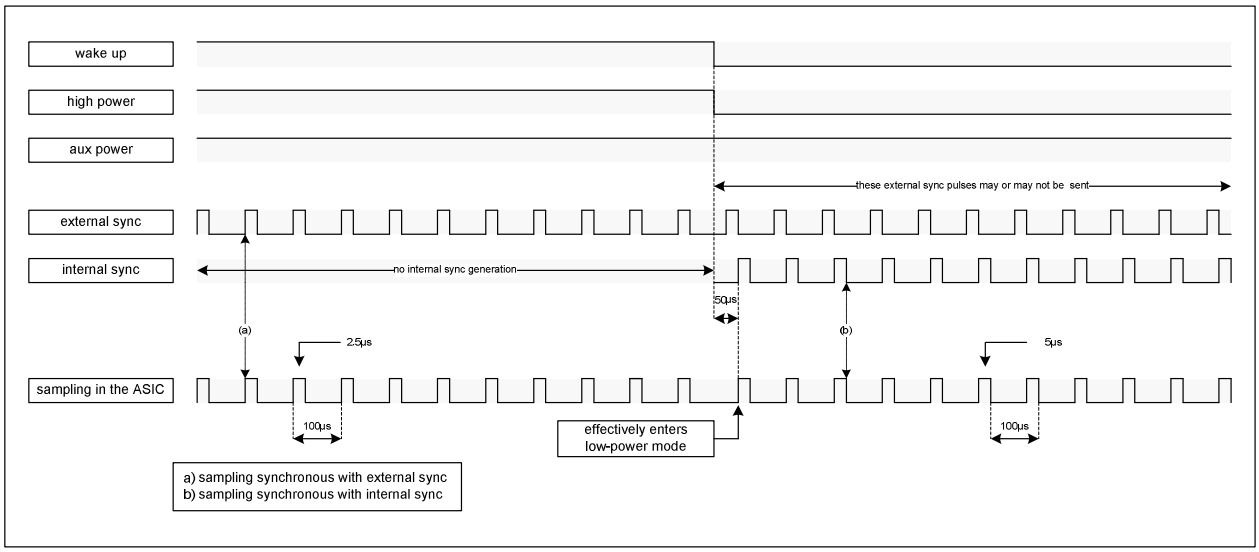


Figure 84: Transition from "active mode" to "low-power mode".

1) In "active mode" the sampling is controlled by external Sync pulse; in "low-power mode" the sampling is controlled by an internal sync pulse.
2) The transition from "active mode" to "low-power mode" is initiated by Wake-Up negative edge. No other signals are necessary for successful mode transition.
3) 50µs after Wake-Up negative edge internal sync generation is started; thus the first sampling triggered by the internal sync pulse occurs 50µs after Wake-Up negative edge.

5.8 Turn counting during state transitions

No turn-counting information may be "lost" during transition from one state to another. For that reason, it is necessary that during all transitions the sampling in the auxiliary path is continued, and that the time period between samplings is no longer than 2*Ts.

5.9 Transport mode

1) TM flag is stored in EEPROM; it can only be changed by writing to EEPROM over SPI.
2) Power-Loss flag will be set or remains set whenever TM flag is HIGH.
3) Power-Loss flag can only be reset when TM flag is LOW.

6 Electro-Magnetic Compatibility (EMC)

6.1 EMC requirements

The ATIC116 shall be qualified by the IC-supplier with integrated circuit test methods described in the general CONTINENTAL document "Electromagnetic Compatibility Requirements for Integrated Circuits" A2C00027649AAA rev. b at test level III. CONTINENTAL will perform application tests within application developments in parallel to the IC tests. In case of exceeded limits during application tests caused by the ATIC116, the supplier has to analyze and solve the root causes, supported by CONTINENTAL.

6.2 EMC requirements on IC-Level

EMC tests on IC-level

- Conducted Emission (CE), 150Ohm method on the following IC-pins:
  MR+, 3V3D, VDD, MISO
  Limit: 12-M (preliminary)
- Conducted Immunity (CI), Direct Power Injection method DPI on the following IC-pins:
  MR+, 3V3D, VDD
  DPI forward power: 30dBm
- Radiated Emission (RE), Mini-TEM-Cell method
  Limit: N (preliminary)
- Radiated Immunity (RI), Mini-TEM-Cell method
  E-field: 300V/m
- Electrostatic discharge ESD on all IC-pins (externally ESD protected, see module description)

For details on measurement methods and limits please refer to following document:
"Electromagnetic Compatibility Requirements for Integrated Circuits" A2C00027649AAA rev. b

Preparation and measurements

The following tasks are necessary to get proper EMC measurements on IC level:

- Create a detailed test plan together with CONTINENTAL
- Create a combination test board for CE, CI, RE, RI and a test board for ESD
- Create a test adaption to set the IC into operation for the tests (hardware and software)
- Do complete EMC measurements according test plan for each silicon
- Evaluation and documentation for each silicon

6.3 EMC requirements on Application Level

Slowly reduce and increase the supply voltage

Purpose :

A slow battery discharge and charge is simulated.

Test :

Laboratory setup operating mode

Apply the test voltage to all voltage inputs.

Reduce the supply voltage from 5V to 0 V.

Increase the supply voltage from 0 V to 5V.

Voltage change (0.5 ± 0.1) V per minute

Requirements :

Functional state A, within the operating voltage range.

Functional state C, outside of the operating voltage range.

Reset Behavior during Voltage Drops

Purpose :

Simulates the reset behavior of the test object during various voltage drops. This test is applied to test objects with a reset function (generally test objects with microcontroller).

Test :

Laboratory setup operating mode

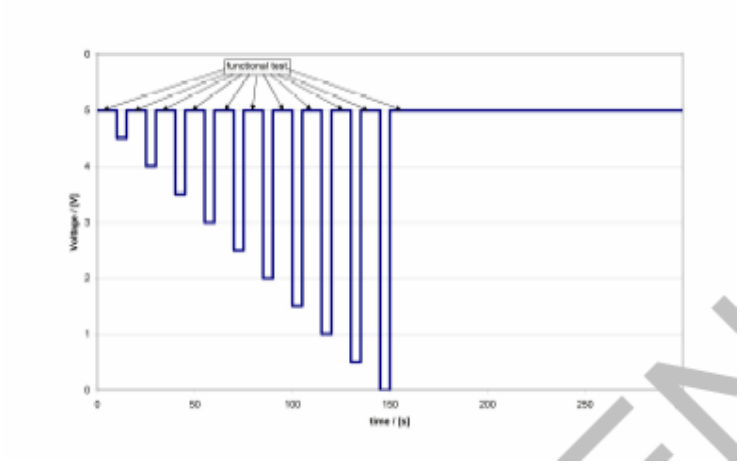
Set test implementation for 10 s U_{Bmin}

Cycle for 5 s reduction of the operating voltage of U_{Bmin} by 0.5 V, for 10 s U_{Bmin}, set and carry out a functional test.

In each cycle, the voltage will be reduced by an additional 0.5 V (see figure).

The test is complete when the voltage reaches a value of • 0.5 V. The voltage change occurs

within 100 ms.



Requirements :

Functional state A, within the operating voltage range.

Functional state C, outside of the operating voltage range.

Immunity to audio frequency magnetic field

- **Reference document**

This test procedure conforms to MIL-STD-STD 461 E standard.

- **Field of application**

This test is intended to check the immunity of equipment sensitive to magnetic fields.
Its main characteristics are as follows:
- Sinusoidal signal
- Frequency band [20 Hz - 100 kHz].
- Substitution method.
- Generation of magnetic field with sinusoidal wave form generated by current flow in a loop antenna or Helmholtz coils.
- 3 EUT and associated harness orientations.

Frequency band (Hz)	Magnetic field spectrum envelope (dBµA/m)
20 - 1000	180
1000 - 10000	180 - 40 x log (F/1000)
10000 - 100000	140
50 - 400 (*)	160

(*) this special frequency band requirement is valid only for EUT fitted on chassis of car or close to the earth ground.

7 CHANGE HISTORY

Revision	Date	Specification Changes (Page/ Chapter/ Modification)	Responsible
A	26.Nov.09	Creation	Conti

8 TECHNOLOGY INFORMATION

(To be filled out by the supplier)

This technology information is a part of the specification

General

manufacture		_____
component name		_____
component family		_____
package outline		_____
manufacture plant	(wafer)	_____
	(assembly)	_____
	(final test)	_____
CECC-Qualification		CECC- _____
free of cadmium		( ) yes ( ) no _____ppm
free of asbestos		( ) yes ( ) no _____ppm

ASIC Die

design version.	_____
semiconductor material	_____
technology	_____
backside metallisation	_____
contact metallisation	_____
surface passivation	_____
die thickness	_____
die dimension	_____

Sensor Die

design version.	_____
semiconductor material	_____
technology	_____
backside metallisation	_____
contact metallisation	_____
surface passivation	_____
die thickness	_____
die dimension	_____

Assembly

die attach method	_____
die attach material	_____
wire bond material	_____
wire bond thickness	_____
wire bond method	_____
package material	_____

Terminals

lead frame material	_____
intermediate layer	_____thickness: _____
	_____thickness: _____
	_____thickness: _____
lead finish	_____thickness: _____
surface passivation	( ) yes ( ) no

