LGDP4531

720-Channel, 262,144-Color One-Chip Driver
with RAM, Power Supply and Gate Circuits
for Amorphous TFT-LCD Panels

Rev 1.15
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Description

The LGDP4531 is a one-chip liquid crystal controller driver LSI, comprising RAM of 240 RGB x 320 dots at maximum, a source driver, a gate driver and a power supply circuit. For effective data transfer, the LGDP4531 supports high-speed 8-/9-/16-/18-bit bus interfaces as a system interface to microcomputer and high-speed RAM write mode.

As a moving picture interface, the LGDP4531 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0).

Also, the LGDP4531 incorporates step-up circuits and voltage follower circuits to generate TFT liquid crystal panel drive voltages.

The LGDP4531's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A one-chip controller driver incorporating a gate circuit and a power supply circuit for 240RGB x320 dots graphics display on an amorphous TFT panel in 262k colors
- System interface
    - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
    - Serial interface
- Interface for moving picture display
    - 6-, 16-, 18-bit bus RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
    - VSYNC interface (System interface + VSYNC)
    - FMARK interface (System interface + FMARK)
- Window address function to specify a rectangular area on the internal RAM to write data
- Writes data within a rectangular area on the internal RAM via moving picture interface
    - Reduces data transfer by specifying the area on the RAM to rewrite data
    - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
    - Resizing function (x 1/2, x 1/4)
- Abundant color display and drawing functions
    - Programmable γ -correction function for 262k-color display
    - Partial display function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
    - Deep standby function
    - 8-color display function
    - Input power supply voltages: Vcc = 2.5V ~ 3.3 V (logic regulator power supply)
        IOVcc = 1.65V ~ 3.3 V (interface I/O power supply)
        Vci = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
    - Source driver liquid crystal drive/Vcom power supply: DDVDH-GND = 4.5V ~ 6.0 V
    - Gate drive power supply: VGH-GND = 10.0V ~ 15.0 V
        VGL-GND = -4.5V ~ -12.5V
        VGH-VGL ≤ 25V
- Liquid crystal power supply startup sequence
- TFT storage capacitance: Cst only (common Vcom formula)
- 172,800-byte internal RAM
- Internal 720-channel source driver and 320-channel gate driver
- Configures a COG module with one chip by arranging gate lines on both sides

Block Diagram
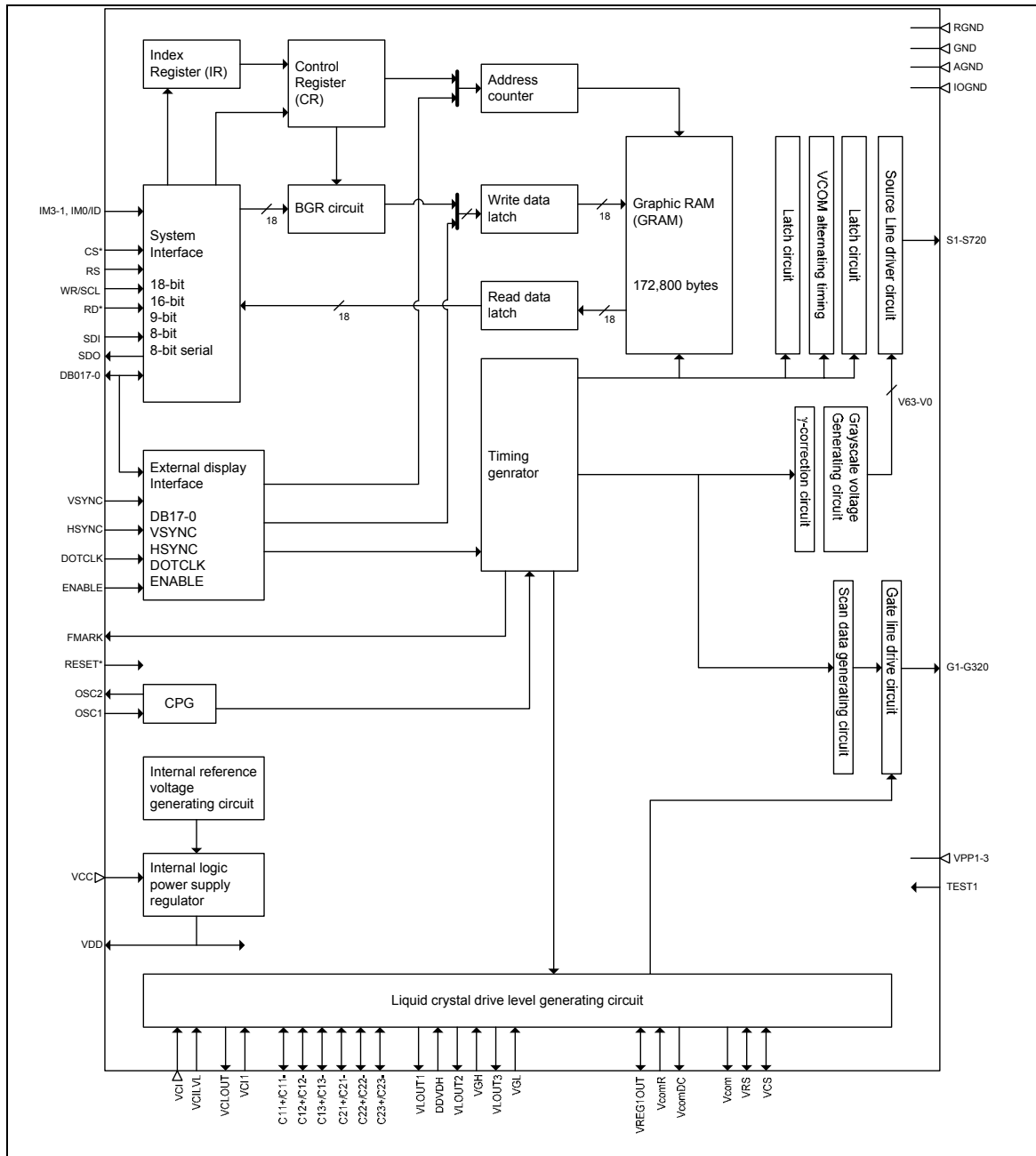
Figure 1

Pin Function

Table 1

Signal	I/O	Connected to	Function
IM3-1, IM0/ID	I	GND/ IOVcc	Select a mode to interface to an MPU. In SPI mode, the IM0 pin is used to set the ID of device code.

IM[3:0]	Interface Mode	DB Pins
000*	Setting disabled	-
0010	80-system 16-bit interface	DB[17:10], DB[8:1]
0011	80-system 8-bit interface	DB[17:10]
010*	Serial peripheral interface (SPI)	SDI, SDO
011*	Setting disabled	-
100*	Setting disabled	-
1010	80-system 18-bit interface	DB[17:0]
1011	80-system 9-bit interface	DB[17:9]
11**	Setting disabled	-

Signal	I/O	Connected to	Function
CS*	I	MPU	A chip select signal. Amplitude: IOVCC-GND. Low: LGDP4531 is selected and accessible. High: LGDP4531 is not selected and not accessible. Fix to the GND level when not in use.
RS	I	MPU	A register select signal. Amplitude: IOVCC-GND. Low: select the index/status register. High: select a control register. In SPI mode, fix to either IOVcc or GND level.
WR*/SCL	I	MPU	Outputs a write strobe signal in 80-system bus interface mode and enables an operation to write data when the signal is low. In SPI mode, a synchronizing clock signal is output.
RD*	I	MPU	Outputs a read strobe signal in 80-system bus interface mode and enables an operation to read data when the signal is low. In SPI mode, fix to either IOVcc or GND level.
SDI	I	MPU	A serial data input (SDI) pin in SPI mode. Data are input on the rising edge of the SCL signal. Fix to either IOVcc or GND level when not in use.
SDO	O	MPU	A serial data output (SDO) pin in SPI mode. Data are output on the falling edge of the SCL signal. Leave the pin open when not in use.
DB0 ~ DB17	I/O	MPU	An 18-bit parallel bidirectional data bus. Unused pins must be fixed either IOVcc or GND level.
ENABLE	I	MPU	A data enable signal in RGB interface mode. Low: Select (accessible) High: Not select (inaccessible) The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVcc or GND level when not in use.
VSYNC	I	MPU	A frame synchronizing signal. When VSPL = "0", it is active low. When VSPL = "1", it is active high. Fix to either IOVcc or GND level when not in use.

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HSYNC	I	MPU	A line synchronizing signal. When HSPL = "0", it is active low. When HSPL = "1", it is active high. Fix to either IOVcc or GND level when not in use.
DOTCLK	I	MPU	A dot clock signal. When DPL = "0", input data on the rising edge of DOTCLK. When DPL = "1", input data on the falling edge of DOTCLK. Fix to either IOVcc or GND level when not in use.
RESET*	I	MPU or External RC circuit	A reset pin. Initializes the LGDP4531 with a low input. Be sure to execute a power-on reset after supplying power.
VCMSEL	I	IOVcc or GND	If VCMSEL is set to high, VCOMH level control comes from EPROM block. If VCMSEL is set to low, VCOMH level control comes from internal registers set by MPU. Connect to GND when EPROM is not used.
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal GRAM. Leave the pin open when not in use.
OSC1 OSC2	I/O	Oscillation Resistor	Connect to an external resistor for R-C oscillation.
Vcc	I	Power supply	Power supply to internal logic regulator circuit: Vcc =2.5V ~ 3.3 V Vcc ≥ IOVcc
GND	-	Power supply	Internal logic GND : GND = 0V
RGND	-	Power supply	Internal RAM GND : RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDD	O	Stabilizing capacitor	Internal logic regulator output to be used as a power supply to internal logic. Connect a stabilizing capacitor.
IOVcc	I	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVcc = 1.65V ~ 3.3V. Vcc ≥ IOVcc. . In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent nosie.
IOGND	-	Power supply	GND for the interface pins : RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
Vci	I	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
VciOUT	O	Stabilizing capacitor, Vci1	Internal reference voltage generated between Vci and GND. The output level is set by instruction (VC).
Vci1	I/O	VciOUT or Vci	Reference voltage for the step-up circuit 1. Vci1 must be set to a level, which will generate the VLOUT1, VLOUT2 and VLOUT3 levels within the respective setting ranges.
VciLVL	I	Power supply	Reference level to generate the VciOUT level according to the step-up rate set with the VC bits. Be sure to connect VciLVL with Vci on the FPC to prevent noise.

VLOUT1	O	Stabilizing capacitor, DDVDH	Output from the step-up circuit 1, generated from Vci1. The step-up factor for the VLOUT1 level is set by instruction (BT). VLOUT1 = 4.5V ~ 6.0V
DDVDH	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and Vcom drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	O	Stabilizing capacitor, VGH	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT2 = max 15.0V
VGH	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	O	Stabilizing capacitor, VGL	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT3 = min −12.5V
VGL	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VLOUT4	O	Stabilizing capacitor, VCL	A voltage level of Vci1 x (-1) generated in the step=ip circuit 2. Connect to a stabilizing capacitor when using the VLOUT4 output.
VCL	I	VLOUT4	Power supply for operating VCOML. Vci1 is multiplied by 1 and output by internal step-up circuit 2. VCL = 0 to -3.3(V)
C11+, C11- C12+, C12-	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 1.
C13+, C13- C21+, C21- C22+, C22- C23+, C23-	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.
VREG1OUT	O	Stabilizing capacitor	Output generated from a reference voltage VciLVL by amplifying by the factor, which is set by instruction (VRH). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 3.0V ~ (DDVDH – 0.5)V
Vcom	O	TFT panel common electrode	Power supply to TFT panel's common electrode. Output AC voltage with the amplitude VCOMH and VCOML. The alternating cycle is changeable by register setting. Also Vcom output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	Output for the high level of VCOM. This output voltage is adjusted by an instruction (VCM) setting. VCOMH = 3.0 to (DDVDH -0.5) (V)
VCOML	O	Stabilizing capacitor	Output for the low level of VCOM. This output voltage is adjusted by an instruction (VDV) setting or fixed to GND by a register (VCOMG) setting. In this case, a capacitor for stabilization is not necessary. VCOML = (VCL +0.5)to 1 (V)
VcomR	I	Variable resistor or open	If a variable resistor is used to adjust VCOMH, it is attached to this pin. In this case, use an instruction (VCM) setting to stop the internal digital potentiometer circuit of VCOMH, and insert the variable resistor for use in adjustment of VCOM between VREG1OUT. Leave it open or connect to GND when not in use.
VGS	I	GND	Reference level for grayscale voltage generating circuit.

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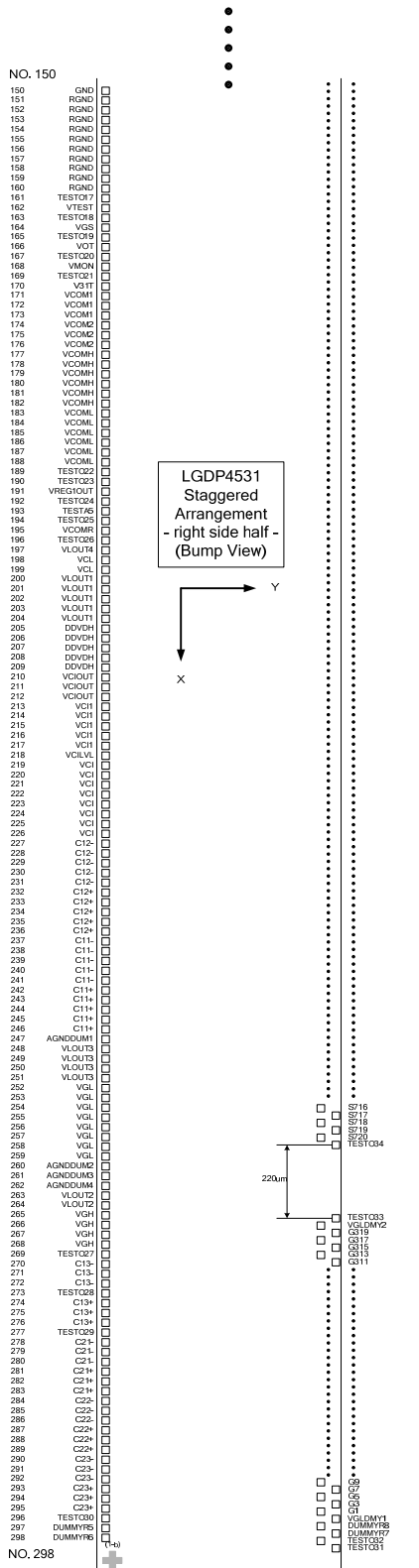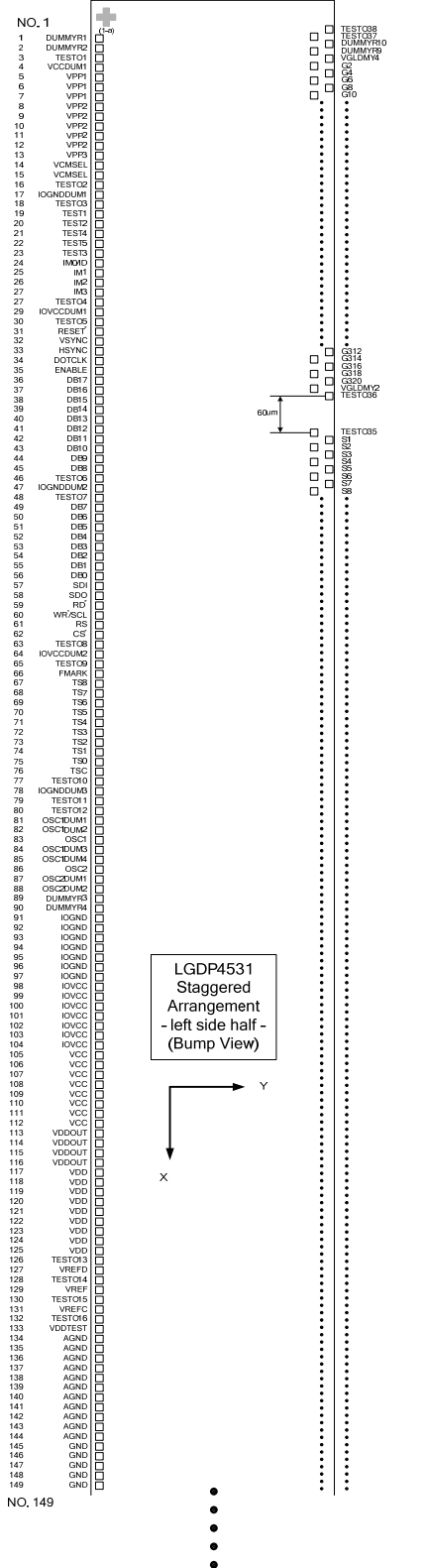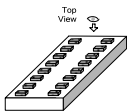|			
S1 ~ S720	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal outputs, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S720.
G1 ~ G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level
V0T,V31T	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
VTEST	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
VREFC	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
VREF	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
VDDTEST	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
VREFD	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
VMON	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
IOVCCDUM 1-2	-	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave them open.
VCCDUM1	-	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
IOGNDDUM 1-3	-	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
OSC1DUM 1-4	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
OSC2DUM 1-2	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
AGNDDUM 1-4	-	-	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
DUMMYR 1-2	-	-	Dummy pins. Connect to IOVCC, GND or open when not in use.
DUMMYR 3-4	-	-	DUMMYR3 and DUMMYR4 are short-circuited within the chip for COG contact resistance measurement.
DUMMYR 5-10	-	-	Dummy pins. Connect to IOVCC, GND or open when not in use.
TEST1	I	GND	Test pin. Connect to GND.
TEST2 - 5	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
TESTA5	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
TSC	-	-	Test pin. Connect to IOVCC, GND or open when not in use.
TS8-0	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
VPP1, VPP3	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
VPP2	I	Power supply	Power supply pin for EPROM write operation. Leave it open when EPROM is not used.
TESTO1-38	-	-	Test pins. Connect to IOVCC, GND or open when not in use.

PAD Arrangement

PAD Coordinate

Pad #	PAD Name	X	Y	Pad #	PAD Name	X	Y	Pad #	PAD Name	X	Y
1	DUMMYR1	-10395.0	-517.5	85	OSC1DUM4	-4515.0	-517.5	169	TESTO21	1365.0	-517.5
2	DUMMYR2	-10325.0	-517.5	86	OSC2	-4445.0	-517.5	170	V31T	1435.0	-517.5
3	TESTO1	-10255.0	-517.5	87	OSC2DUM1	-4375.0	-517.5	171	VCOM1	1505.0	-517.5
4	VCCDUM1	-10185.0	-517.5	88	OSC2DUM2	-4305.0	-517.5	172	VCOM1	1575.0	-517.5
5	VPP1	-10115.0	-517.5	89	DUMMYR3	-4235.0	-517.5	173	VCOM1	1645.0	-517.5
6	VPP1	-10045.0	-517.5	90	DUMMYR4	-4165.0	-517.5	174	VCOM2	1715.0	-517.5
7	VPP1	-9975.0	-517.5	91	IOGND	-4095.0	-517.5	175	VCOM2	1785.0	-517.5
8	VPP2	-9905.0	-517.5	92	IOGND	-4025.0	-517.5	176	VCOM2	1855.0	-517.5
9	VPP2	-9835.0	-517.5	93	IOGND	-3955.0	-517.5	177	VCOMH	1925.0	-517.5
10	VPP2	-9765.0	-517.5	94	IOGND	-3885.0	-517.5	178	VCOMH	1995.0	-517.5
11	VPP2	-9695.0	-517.5	95	IOGND	-3815.0	-517.5	179	VCOMH	2065.0	-517.5
12	VPP2	-9625.0	-517.5	96	IOGND	-3745.0	-517.5	180	VCOMH	2135.0	-517.5
13	VPP3	-9555.0	-517.5	97	IOGND	-3675.0	-517.5	181	VCOMH	2205.0	-517.5
14	VCMSEL	-9485.0	-517.5	98	IOVCC	-3605.0	-517.5	182	VCOMH	2275.0	-517.5
15	VCMSEL	-9415.0	-517.5	99	IOVCC	-3535.0	-517.5	183	VCOML	2345.0	-517.5
16	TESTO2	-9345.0	-517.5	100	IOVCC	-3465.0	-517.5	184	VCOML	2415.0	-517.5
17	IOGNDDUM1	-9275.0	-517.5	101	IOVCC	-3395.0	-517.5	185	VCOML	2485.0	-517.5
18	TESTO3	-9205.0	-517.5	102	IOVCC	-3325.0	-517.5	186	VCOML	2555.0	-517.5
19	TEST1	-9135.0	-517.5	103	IOVCC	-3255.0	-517.5	187	VCOML	2625.0	-517.5
20	TEST2	-9065.0	-517.5	104	IOVCC	-3185.0	-517.5	188	VCOML	2695.0	-517.5
21	TEST4	-8995.0	-517.5	105	VCC	-3115.0	-517.5	189	TESTO22	2765.0	-517.5
22	TEST5	-8925.0	-517.5	106	VCC	-3045.0	-517.5	190	TESTO23	2835.0	-517.5
23	TEST3	-8855.0	-517.5	107	VCC	-2975.0	-517.5	191	VREG1OUT	2905.0	-517.5
24	IM0/ID	-8785.0	-517.5	108	VCC	-2905.0	-517.5	192	TESTO24	2975.0	-517.5
25	IM1	-8715.0	-517.5	109	VCC	-2835.0	-517.5	193	TESTA5	3045.0	-517.5
26	IM2	-8645.0	-517.5	110	VCC	-2765.0	-517.5	194	TESTO25	3115.0	-517.5
27	IM3	-8575.0	-517.5	111	VCC	-2695.0	-517.5	195	VCOMR	3185.0	-517.5
28	TESTO4	-8505.0	-517.5	112	VCC	-2625.0	-517.5	196	TESTO26	3255.0	-517.5
29	IOVCCDUM1	-8435.0	-517.5	113	VDDOUT	-2555.0	-517.5	197	VLOUT4	3325.0	-517.5
30	TESTO5	-8365.0	-517.5	114	VDDOUT	-2485.0	-517.5	198	VCL	3395.0	-517.5
31	RESET*	-8295.0	-517.5	115	VDDOUT	-2415.0	-517.5	199	VCL	3465.0	-517.5
32	VSYNC	-8225.0	-517.5	116	VDDOUT	-2345.0	-517.5	200	VLOUT1	3535.0	-517.5
33	HSYNC	-8155.0	-517.5	117	VDD	-2275.0	-517.5	201	VLOUT1	3605.0	-517.5
34	DOTCLK	-8085.0	-517.5	118	VDD	-2205.0	-517.5	202	VLOUT1	3675.0	-517.5
35	ENABLE	-8015.0	-517.5	119	VDD	-2135.0	-517.5	203	VLOUT1	3745.0	-517.5
36	DB17	-7945.0	-517.5	120	VDD	-2065.0	-517.5	204	VLOUT1	3815.0	-517.5
37	DB16	-7875.0	-517.5	121	VDD	-1995.0	-517.5	205	DDVDH	3885.0	-517.5
38	DB15	-7805.0	-517.5	122	VDD	-1925.0	-517.5	206	DDVDH	3955.0	-517.5
39	DB14	-7735.0	-517.5	123	VDD	-1855.0	-517.5	207	DDVDH	4025.0	-517.5
40	DB13	-7665.0	-517.5	124	VDD	-1785.0	-517.5	208	DDVDH	4095.0	-517.5
41	DB12	-7595.0	-517.5	125	VDD	-1715.0	-517.5	209	DDVDH	4165.0	-517.5
42	DB11	-7525.0	-517.5	126	TESTO13	-1645.0	-517.5	210	VCIOUT	4235.0	-517.5
43	DB10	-7455.0	-517.5	127	VREFD	-1575.0	-517.5	211	VCIOUT	4305.0	-517.5
44	DB9	-7385.0	-517.5	128	TESTO14	-1505.0	-517.5	212	VCIOUT	4375.0	-517.5
45	DB8	-7315.0	-517.5	129	VREF	-1435.0	-517.5	213	VCI1	4445.0	-517.5
46	TESTO6	-7245.0	-517.5	130	TESTO15	-1365.0	-517.5	214	VCI1	4515.0	-517.5
47	IOGNDDUM2	-7175.0	-517.5	131	VREFC	-1295.0	-517.5	215	VCI1	4585.0	-517.5
48	TESTO7	-7105.0	-517.5	132	TESTO16	-1225.0	-517.5	216	VCI1	4655.0	-517.5
49	DB7	-7035.0	-517.5	133	VDDTEST	-1155.0	-517.5	217	VCI1	4725.0	-517.5
50	DB6	-6965.0	-517.5	134	AGND	-1085.0	-517.5	218	VCILVL	4795.0	-517.5
51	DB5	-6895.0	-517.5	135	AGND	-1015.0	-517.5	219	VCI	4865.0	-517.5
52	DB4	-6825.0	-517.5	136	AGND	-945.0	-517.5	220	VCI	4935.0	-517.5
53	DB3	-6755.0	-517.5	137	AGND	-875.0	-517.5	221	VCI	5005.0	-517.5
54	DB2	-6685.0	-517.5	138	AGND	-805.0	-517.5	222	VCI	5075.0	-517.5
55	DB1	-6615.0	-517.5	139	AGND	-735.0	-517.5	223	VCI	5145.0	-517.5
56	DB0	-6545.0	-517.5	140	AGND	-665.0	-517.5	224	VCI	5215.0	-517.5
57	SDO	-6475.0	-517.5	141	AGND	-595.0	-517.5	225	VCI	5285.0	-517.5
58	SDI	-6405.0	-517.5	142	AGND	-525.0	-517.5	226	VCI	5355.0	-517.5
59	RD*	-6335.0	-517.5	143	AGND	-455.0	-517.5	227	C12-	5425.0	-517.5
60	WR*/SCL	-6265.0	-517.5	144	AGND	-385.0	-517.5	228	C12-	5495.0	-517.5
61	RS	-6195.0	-517.5	145	GND	-315.0	-517.5	229	C12-	5565.0	-517.5
62	CS*	-6125.0	-517.5	146	GND	-245.0	-517.5	230	C12-	5635.0	-517.5
63	TESTO8	-6055.0	-517.5	147	GND	-175.0	-517.5	231	C12-	5705.0	-517.5
64	IOVCCDUM2	-5985.0	-517.5	148	GND	-105.0	-517.5	232	C12+	5775.0	-517.5
65	TESTO9	-5915.0	-517.5	149	GND	-35.0	-517.5	233	C12+	5845.0	-517.5
66	FMARK	-5845.0	-517.5	150	GND	35.0	-517.5	234	C12+	5915.0	-517.5
67	TS8	-5775.0	-517.5	151	RGND	105.0	-517.5	235	C12+	5985.0	-517.5
68	TS7	-5705.0	-517.5	152	RGND	175.0	-517.5	236	C12+	6055.0	-517.5
69	TS6	-5635.0	-517.5	153	RGND	245.0	-517.5	237	C11-	6125.0	-517.5
70	TS5	-5565.0	-517.5	154	RGND	315.0	-517.5	238	C11-	6195.0	-517.5
71	TS4	-5495.0	-517.5	155	RGND	385.0	-517.5	239	C11-	6265.0	-517.5
72	TS3	-5425.0	-517.5	156	RGND	455.0	-517.5	240	C11-	6335.0	-517.5
73	TS2	-5355.0	-517.5	157	RGND	525.0	-517.5	241	C11-	6405.0	-517.5
74	TS1	-5285.0	-517.5	158	RGND	595.0	-517.5	242	C11+	6475.0	-517.5
75	TS0	-5215.0	-517.5	159	RGND	665.0	-517.5	243	C11+	6545.0	-517.5
76	TSC	-5145.0	-517.5	160	RGND	735.0	-517.5	244	C11+	6615.0	-517.5
77	TESTO10	-5075.0	-517.5	161	TESTO17	805.0	-517.5	245	C11+	6685.0	-517.5
78	IOGNDDUM3	-5005.0	-517.5	162	VTEST	875.0	-517.5	246	C11+	6755.0	-517.5
79	TESTO11	-4935.0	-517.5	163	TESTO18	945.0	-517.5	247	AGNDDUM1	6825.0	-517.5
80	TESTO12	-4865.0	-517.5	164	VGS	1015.0	-517.5	248	VLOUT3	6895.0	-517.5
81	OSC1DUM1	-4795.0	-517.5	165	TESTO19	1085.0	-517.5	249	VLOUT3	6965.0	-517.5
82	OSC1DUM2	-4725.0	-517.5	166	V0T	1155.0	-517.5	250	VLOUT3	7035.0	-517.5
83	OSC1	-4655.0	-517.5	167	TESTO20	1225.0	-517.5	251	VLOUT3	7105.0	-517.5
84	OSC1DUM3	-4585.0	-517.5	168	VMON	1295.0	-517.5	252	VGL	7175.0	-517.5

LG Electronics

Pad # .	PAD Name	X	Y	Pad # .	PAD Name	X	Y	Pad # .	PAD Name	X	Y
253	VGL	7245.0	-517.5	340	G73	9850.0	386.5	427	G247	8110.0	511.5
254	VGL	7315.0	-517.5	341	G75	9830.0	511.5	428	G249	8090.0	386.5
255	VGL	7385.0	-517.5	342	G77	9810.0	386.5	429	G251	8070.0	511.5
256	VGL	7455.0	-517.5	343	G79	9790.0	511.5	430	G253	8050.0	386.5
257	VGL	7525.0	-517.5	344	G81	9770.0	386.5	431	G255	8030.0	511.5
258	VGL	7595.0	-517.5	345	G83	9750.0	511.5	432	G257	8010.0	386.5
259	VGL	7665.0	-517.5	346	G85	9730.0	386.5	433	G259	7990.0	511.5
260	AGNDDUM2	7735.0	-517.5	347	G87	9710.0	511.5	434	G261	7970.0	386.5
261	AGNDDUM3	7805.0	-517.5	348	G89	9690.0	386.5	435	G263	7950.0	511.5
262	AGNDDUM4	7875.0	-517.5	349	G91	9670.0	511.5	436	G265	7930.0	386.5
263	VLOUT2	7945.0	-517.5	350	G93	9650.0	386.5	437	G267	7910.0	511.5
264	VLOUT2	8015.0	-517.5	351	G95	9630.0	511.5	438	G269	7890.0	386.5
265	VGH	8085.0	-517.5	352	G97	9610.0	386.5	439	G271	7870.0	511.5
266	VGH	8155.0	-517.5	353	G99	9590.0	511.5	440	G273	7850.0	386.5
267	VGH	8225.0	-517.5	354	G101	9570.0	386.5	441	G275	7830.0	511.5
268	VGH	8295.0	-517.5	355	G103	9550.0	511.5	442	G277	7810.0	386.5
269	TESTO27	8365.0	-517.5	356	G105	9530.0	386.5	443	G279	7790.0	511.5
270	C13-	8435.0	-517.5	357	G107	9510.0	511.5	444	G281	7770.0	386.5
271	C13-	8505.0	-517.5	358	G109	9490.0	386.5	445	G283	7750.0	511.5
272	C13-	8575.0	-517.5	359	G111	9470.0	511.5	446	G285	7730.0	386.5
273	TESTO28	8645.0	-517.5	360	G113	9450.0	386.5	447	G287	7710.0	511.5
274	C13+	8715.0	-517.5	361	G115	9430.0	511.5	448	G289	7690.0	386.5
275	C13+	8785.0	-517.5	362	G117	9410.0	386.5	449	G291	7670.0	511.5
276	C13+	8855.0	-517.5	363	G119	9390.0	511.5	450	G293	7650.0	386.5
277	TESTO29	8925.0	-517.5	364	G121	9370.0	386.5	451	G295	7630.0	511.5
278	C21-	8995.0	-517.5	365	G123	9350.0	511.5	452	G297	7610.0	386.5
279	C21-	9065.0	-517.5	366	G125	9330.0	386.5	453	G299	7590.0	511.5
280	C21-	9135.0	-517.5	367	G127	9310.0	511.5	454	G301	7570.0	386.5
281	C21+	9205.0	-517.5	368	G129	9290.0	386.5	455	G303	7550.0	511.5
282	C21+	9275.0	-517.5	369	G131	9270.0	511.5	456	G305	7530.0	386.5
283	C21+	9345.0	-517.5	370	G133	9250.0	386.5	457	G307	7510.0	511.5
284	C22-	9415.0	-517.5	371	G135	9230.0	511.5	458	G309	7490.0	386.5
285	C22-	9485.0	-517.5	372	G137	9210.0	386.5	459	G311	7470.0	511.5
286	C22-	9555.0	-517.5	373	G139	9190.0	511.5	460	G313	7450.0	386.5
287	C22+	9625.0	-517.5	374	G141	9170.0	386.5	461	G315	7430.0	511.5
288	C22+	9695.0	-517.5	375	G143	9150.0	511.5	462	G317	7410.0	386.5
289	C22+	9765.0	-517.5	376	G145	9130.0	386.5	463	G319	7390.0	511.5
290	C23-	9835.0	-517.5	377	G147	9110.0	511.5	464	VGLDMY2	7370.0	386.5
291	C23-	9905.0	-517.5	378	G149	9090.0	386.5	465	TESTO33	7350.0	511.5
292	C23-	9975.0	-517.5	379	G151	9070.0	511.5	466	TESTO34	7130.0	511.5
293	C23+	10045.0	-517.5	380	G153	9050.0	386.5	467	S720	7110.0	386.5
294	C23+	10115.0	-517.5	381	G155	9030.0	511.5	468	S719	7090.0	511.5
295	C23+	10185.0	-517.5	382	G157	9010.0	386.5	469	S718	7070.0	386.5
296	TESTO30	10255.0	-517.5	383	G159	8990.0	511.5	470	S717	7050.0	511.5
297	DUMMYR5	10325.0	-517.5	384	G161	8970.0	386.5	471	S716	7030.0	386.5
298	DUMMYR6	10395.0	-517.5	385	G163	8950.0	511.5	472	S715	7010.0	511.5
299	TESTO31	10670.0	511.5	386	G165	8930.0	386.5	473	S714	6990.0	386.5
300	TESTO32	10650.0	386.5	387	G167	8910.0	511.5	474	S713	6970.0	511.5
301	DUMMYR7	10630.0	511.5	388	G169	8890.0	386.5	475	S712	6950.0	386.5
302	DUMMYR8	10610.0	386.5	389	G171	8870.0	511.5	476	S711	6930.0	511.5
303	VGLDMY1	10590.0	511.5	390	G173	8850.0	386.5	477	S710	6910.0	386.5
304	G1	10570.0	386.5	391	G175	8830.0	511.5	478	S709	6890.0	511.5
305	G3	10550.0	511.5	392	G177	8810.0	386.5	479	S708	6870.0	386.5
306	G5	10530.0	386.5	393	G179	8790.0	511.5	480	S707	6850.0	511.5
307	G7	10510.0	511.5	394	G181	8770.0	386.5	481	S706	6830.0	386.5
308	G9	10490.0	386.5	395	G183	8750.0	511.5	482	S705	6810.0	511.5
309	G11	10470.0	511.5	396	G185	8730.0	386.5	483	S704	6790.0	386.5
310	G13	10450.0	386.5	397	G187	8710.0	511.5	484	S703	6770.0	511.5
311	G15	10430.0	511.5	398	G189	8690.0	386.5	485	S702	6750.0	386.5
312	G17	10410.0	386.5	399	G191	8670.0	511.5	486	S701	6730.0	511.5
313	G19	10390.0	511.5	400	G193	8650.0	386.5	487	S700	6710.0	386.5
314	G21	10370.0	386.5	401	G195	8630.0	511.5	488	S699	6690.0	511.5
315	G23	10350.0	511.5	402	G197	8610.0	386.5	489	S698	6670.0	386.5
316	G25	10330.0	386.5	403	G199	8590.0	511.5	490	S697	6650.0	511.5
317	G27	10310.0	511.5	404	G201	8570.0	386.5	491	S696	6630.0	386.5
318	G29	10290.0	386.5	405	G203	8550.0	511.5	492	S695	6610.0	511.5
319	G31	10270.0	511.5	406	G205	8530.0	386.5	493	S694	6590.0	386.5
320	G33	10250.0	386.5	407	G207	8510.0	511.5	494	S693	6570.0	511.5
321	G35	10230.0	511.5	408	G209	8490.0	386.5	495	S692	6550.0	386.5
322	G37	10210.0	386.5	409	G211	8470.0	511.5	496	S691	6530.0	511.5
323	G39	10190.0	511.5	410	G213	8450.0	386.5	497	S690	6510.0	386.5
324	G41	10170.0	386.5	411	G215	8430.0	511.5	498	S689	6490.0	511.5
325	G43	10150.0	511.5	412	G217	8410.0	386.5	499	S688	6470.0	386.5
326	G45	10130.0	386.5	413	G219	8390.0	511.5	500	S687	6450.0	511.5
327	G47	10110.0	511.5	414	G221	8370.0	386.5	501	S686	6430.0	386.5
328	G49	10090.0	386.5	415	G223	8350.0	511.5	502	S685	6410.0	511.5
329	G51	10070.0	511.5	416	G225	8330.0	386.5	503	S684	6390.0	386.5
330	G53	10050.0	386.5	417	G227	8310.0	511.5	504	S683	6370.0	511.5
331	G55	10030.0	511.5	418	G229	8290.0	386.5	505	S682	6350.0	386.5
332	G57	10010.0	386.5	419	G231	8270.0	511.5	506	S681	6330.0	511.5
333	G59	9990.0	511.5	420	G233	8250.0	386.5	507	S680	6310.0	386.5
334	G61	9970.0	386.5	421	G235	8230.0	511.5	508	S679	6290.0	511.5
335	G63	9950.0	511.5	422	G237	8210.0	386.5	509	S678	6270.0	386.5
336	G65	9930.0	386.5	423	G239	8190.0	511.5	510	S677	6250.0	511.5
337	G67	9910.0	511.5	424	G241	8170.0	386.5	511	S676	6230.0	386.5
338	G69	9890.0	386.5	425	G243	8150.0	511.5	512	S675	6210.0	511.5
339	G71	9870.0	511.5	426	G245	8130.0	386.5	513	S674	6190.0	386.5

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Pad # .	PAD Name	X	Y
514	S673	6170.0	511.5
515	S672	6150.0	386.5
516	S671	6130.0	511.5
517	S670	6110.0	386.5
518	S669	6090.0	511.5
519	S668	6070.0	386.5
520	S667	6050.0	511.5
521	S666	6030.0	386.5
522	S665	6010.0	511.5
523	S664	5990.0	386.5
524	S663	5970.0	511.5
525	S662	5950.0	386.5
526	S661	5930.0	511.5
527	S660	5910.0	386.5
528	S659	5890.0	511.5
529	S658	5870.0	386.5
530	S657	5850.0	511.5
531	S656	5830.0	386.5
532	S655	5810.0	511.5
533	S654	5790.0	386.5
534	S653	5770.0	511.5
535	S652	5750.0	386.5
536	S651	5730.0	511.5
537	S650	5710.0	386.5
538	S649	5690.0	511.5
539	S648	5670.0	386.5
540	S647	5650.0	511.5
541	S646	5630.0	386.5
542	S645	5610.0	511.5
543	S644	5590.0	386.5
544	S643	5570.0	511.5
545	S642	5550.0	386.5
546	S641	5530.0	511.5
547	S640	5510.0	386.5
548	S639	5490.0	511.5
549	S638	5470.0	386.5
550	S637	5450.0	511.5
551	S636	5430.0	386.5
552	S635	5410.0	511.5
553	S634	5390.0	386.5
554	S633	5370.0	511.5
555	S632	5350.0	386.5
556	S631	5330.0	511.5
557	S630	5310.0	386.5
558	S629	5290.0	511.5
559	S628	5270.0	386.5
560	S627	5250.0	511.5
561	S626	5230.0	386.5
562	S625	5210.0	511.5
563	S624	5190.0	386.5
564	S623	5170.0	511.5
565	S622	5150.0	386.5
566	S621	5130.0	511.5
567	S620	5110.0	386.5
568	S619	5090.0	511.5
569	S618	5070.0	386.5
570	S617	5050.0	511.5
571	S616	5030.0	386.5
572	S615	5010.0	511.5
573	S614	4990.0	386.5
574	S613	4970.0	511.5
575	S612	4950.0	386.5
576	S611	4930.0	511.5
577	S610	4910.0	386.5
578	S609	4890.0	511.5
579	S608	4870.0	386.5
580	S607	4850.0	511.5
581	S606	4830.0	386.5
582	S605	4810.0	511.5
583	S604	4790.0	386.5
584	S603	4770.0	511.5
585	S602	4750.0	386.5
586	S601	4730.0	511.5
587	S600	4710.0	386.5
588	S599	4690.0	511.5
589	S598	4670.0	386.5
590	S597	4650.0	511.5
591	S596	4630.0	386.5
592	S595	4610.0	511.5
593	S594	4590.0	386.5
594	S593	4570.0	511.5
595	S592	4550.0	386.5
596	S591	4530.0	511.5
597	S590	4510.0	386.5
598	S589	4490.0	511.5
599	S588	4470.0	386.5
600	S587	4450.0	511.5

Pad # .	PAD Name	X	Y
601	S586	4430.0	386.5
602	S585	4410.0	511.5
603	S584	4390.0	386.5
604	S583	4370.0	511.5
605	S582	4350.0	386.5
606	S581	4330.0	511.5
607	S580	4310.0	386.5
608	S579	4290.0	511.5
609	S578	4270.0	386.5
610	S577	4250.0	511.5
611	S576	4230.0	386.5
612	S575	4210.0	511.5
613	S574	4190.0	386.5
614	S573	4170.0	511.5
615	S572	4150.0	386.5
616	S571	4130.0	511.5
617	S570	4110.0	386.5
618	S569	4090.0	511.5
619	S568	4070.0	386.5
620	S567	4050.0	511.5
621	S566	4030.0	386.5
622	S565	4010.0	511.5
623	S564	3990.0	386.5
624	S563	3970.0	511.5
625	S562	3950.0	386.5
626	S561	3930.0	511.5
627	S560	3910.0	386.5
628	S559	3890.0	511.5
629	S558	3870.0	386.5
630	S557	3850.0	511.5
631	S556	3830.0	386.5
632	S555	3810.0	511.5
633	S554	3790.0	386.5
634	S553	3770.0	511.5
635	S552	3750.0	386.5
636	S551	3730.0	511.5
637	S550	3710.0	386.5
638	S549	3690.0	511.5
639	S548	3670.0	386.5
640	S547	3650.0	511.5
641	S546	3630.0	386.5
642	S545	3610.0	511.5
643	S544	3590.0	386.5
644	S543	3570.0	511.5
645	S542	3550.0	386.5
646	S541	3530.0	511.5
647	S540	3510.0	386.5
648	S539	3490.0	511.5
649	S538	3470.0	386.5
650	S537	3450.0	511.5
651	S536	3430.0	386.5
652	S535	3410.0	511.5
653	S534	3390.0	386.5
654	S533	3370.0	511.5
655	S532	3350.0	386.5
656	S531	3330.0	511.5
657	S530	3310.0	386.5
658	S529	3290.0	511.5
659	S528	3270.0	386.5
660	S527	3250.0	511.5
661	S526	3230.0	386.5
662	S525	3210.0	511.5
663	S524	3190.0	386.5
664	S523	3170.0	511.5
665	S522	3150.0	386.5
666	S521	3130.0	511.5
667	S520	3110.0	386.5
668	S519	3090.0	511.5
669	S518	3070.0	386.5
670	S517	3050.0	511.5
671	S516	3030.0	386.5
672	S515	3010.0	511.5
673	S514	2990.0	386.5
674	S513	2970.0	511.5
675	S512	2950.0	386.5
676	S511	2930.0	511.5
677	S510	2910.0	386.5
678	S509	2890.0	511.5
679	S508	2870.0	386.5
680	S507	2850.0	511.5
681	S506	2830.0	386.5
682	S505	2810.0	511.5
683	S504	2790.0	386.5
684	S503	2770.0	511.5
685	S502	2750.0	386.5
686	S501	2730.0	511.5
687	S500	2710.0	386.5

Pad # .	PAD Name	X	Y
688	S499	2690.0	511.5
689	S498	2670.0	386.5
690	S497	2650.0	511.5
691	S496	2630.0	386.5
692	S495	2610.0	511.5
693	S494	2590.0	386.5
694	S493	2570.0	511.5
695	S492	2550.0	386.5
696	S491	2530.0	511.5
697	S490	2510.0	386.5
698	S489	2490.0	511.5
699	S488	2470.0	386.5
700	S487	2450.0	511.5
701	S486	2430.0	386.5
702	S485	2410.0	511.5
703	S484	2390.0	386.5
704	S483	2370.0	511.5
705	S482	2350.0	386.5
706	S481	2330.0	511.5
707	S480	2310.0	386.5
708	S479	2290.0	511.5
709	S478	2270.0	386.5
710	S477	2250.0	511.5
711	S476	2230.0	386.5
712	S475	2210.0	511.5
713	S474	2190.0	386.5
714	S473	2170.0	511.5
715	S472	2150.0	386.5
716	S471	2130.0	511.5
717	S470	2110.0	386.5
718	S469	2090.0	511.5
719	S468	2070.0	386.5
720	S467	2050.0	511.5
721	S466	2030.0	386.5
722	S465	2010.0	511.5
723	S464	1990.0	386.5
724	S463	1970.0	511.5
725	S462	1950.0	386.5
726	S461	1930.0	511.5
727	S460	1910.0	386.5
728	S459	1890.0	511.5
729	S458	1870.0	386.5
730	S457	1850.0	511.5
731	S456	1830.0	386.5
732	S455	1810.0	511.5
733	S454	1790.0	386.5
734	S453	1770.0	511.5
735	S452	1750.0	386.5
736	S451	1730.0	511.5
737	S450	1710.0	386.5
738	S449	1690.0	511.5
739	S448	1670.0	386.5
740	S447	1650.0	511.5
741	S446	1630.0	386.5
742	S445	1610.0	511.5
743	S444	1590.0	386.5
744	S443	1570.0	511.5
745	S442	1550.0	386.5
746	S441	1530.0	511.5
747	S440	1510.0	386.5
748	S439	1490.0	511.5
749	S438	1470.0	386.5
750	S437	1450.0	511.5
751	S436	1430.0	386.5
752	S435	1410.0	511.5
753	S434	1390.0	386.5
754	S433	1370.0	511.5
755	S432	1350.0	386.5
756	S431	1330.0	511.5
757	S430	1310.0	386.5
758	S429	1290.0	511.5
759	S428	1270.0	386.5
760	S427	1250.0	511.5
761	S426	1230.0	386.5
762	S425	1210.0	511.5
763	S424	1190.0	386.5
764	S423	1170.0	511.5
765	S422	1150.0	386.5
766	S421	1130.0	511.5
767	S420	1110.0	386.5
768	S419	1090.0	511.5
769	S418	1070.0	386.5
770	S417	1050.0	511.5
771	S416	1030.0	386.5
772	S415	1010.0	511.5
773	S414	990.0	386.5
774	S413	970.0	511.5

Pad #	PAD Name	X	Y
775	S412	950.0	386.5
776	S411	930.0	511.5
777	S410	910.0	386.5
778	S409	890.0	511.5
779	S408	870.0	386.5
780	S407	850.0	511.5
781	S406	830.0	386.5
782	S405	810.0	511.5
783	S404	790.0	386.5
784	S403	770.0	511.5
785	S402	750.0	386.5
786	S401	730.0	511.5
787	S400	710.0	386.5
788	S399	690.0	511.5
789	S398	670.0	386.5
790	S397	650.0	511.5
791	S396	630.0	386.5
792	S395	610.0	511.5
793	S394	590.0	386.5
794	S393	570.0	511.5
795	S392	550.0	386.5
796	S391	530.0	511.5
797	S390	510.0	386.5
798	S389	490.0	511.5
799	S388	470.0	386.5
800	S387	450.0	511.5
801	S386	430.0	386.5
802	S385	410.0	511.5
803	S384	390.0	386.5
804	S383	370.0	511.5
805	S382	350.0	386.5
806	S381	330.0	511.5
807	S380	310.0	386.5
808	S379	290.0	511.5
809	S378	270.0	386.5
810	S377	250.0	511.5
811	S376	230.0	386.5
812	S375	210.0	511.5
813	S374	190.0	386.5
814	S373	170.0	511.5
815	S372	150.0	386.5
816	S371	130.0	511.5
817	S370	110.0	386.5
818	S369	90.0	511.5
819	S368	70.0	386.5
820	S367	50.0	511.5
821	S366	30.0	386.5
822	S365	10.0	511.5
823	S364	-10.0	386.5
824	S363	-30.0	511.5
825	S362	-50.0	386.5
826	S361	-70.0	511.5
827	S360	-90.0	386.5
828	S359	-110.0	511.5
829	S358	-130.0	386.5
830	S357	-150.0	511.5
831	S356	-170.0	386.5
832	S355	-190.0	511.5
833	S354	-210.0	386.5
834	S353	-230.0	511.5
835	S352	-250.0	386.5
836	S351	-270.0	511.5
837	S350	-290.0	386.5
838	S349	-310.0	511.5
839	S348	-330.0	386.5
840	S347	-350.0	511.5
841	S346	-370.0	386.5
842	S345	-390.0	511.5
843	S344	-410.0	386.5
844	S343	-430.0	511.5
845	S342	-450.0	386.5
846	S341	-470.0	511.5
847	S340	-490.0	386.5
848	S339	-510.0	511.5
849	S338	-530.0	386.5
850	S337	-550.0	511.5
851	S336	-570.0	386.5
852	S335	-590.0	511.5
853	S334	-610.0	386.5
854	S333	-630.0	511.5
855	S332	-650.0	386.5
856	S331	-670.0	511.5
857	S330	-690.0	386.5
858	S329	-710.0	511.5
859	S328	-730.0	386.5
860	S327	-750.0	511.5
861	S326	-770.0	386.5

Pad #	PAD Name	X	Y
862	S325	-790.0	511.5
863	S324	-810.0	386.5
864	S323	-830.0	511.5
865	S322	-850.0	386.5
866	S321	-870.0	511.5
867	S320	-890.0	386.5
868	S319	-910.0	511.5
869	S318	-930.0	386.5
870	S317	-950.0	511.5
871	S316	-970.0	386.5
872	S315	-990.0	511.5
873	S314	-1010.0	386.5
874	S313	-1030.0	511.5
875	S312	-1050.0	386.5
876	S311	-1070.0	511.5
877	S310	-1090.0	386.5
878	S309	-1110.0	511.5
879	S308	-1130.0	386.5
880	S307	-1150.0	511.5
881	S306	-1170.0	386.5
882	S305	-1190.0	511.5
883	S304	-1210.0	386.5
884	S303	-1230.0	511.5
885	S302	-1250.0	386.5
886	S301	-1270.0	511.5
887	S300	-1290.0	386.5
888	S299	-1310.0	511.5
889	S298	-1330.0	386.5
890	S297	-1350.0	511.5
891	S296	-1370.0	386.5
892	S295	-1390.0	511.5
893	S294	-1410.0	386.5
894	S293	-1430.0	511.5
895	S292	-1450.0	386.5
896	S291	-1470.0	511.5
897	S290	-1490.0	386.5
898	S289	-1510.0	511.5
899	S288	-1530.0	386.5
900	S287	-1550.0	511.5
901	S286	-1570.0	386.5
902	S285	-1590.0	511.5
903	S284	-1610.0	386.5
904	S283	-1630.0	511.5
905	S282	-1650.0	386.5
906	S281	-1670.0	511.5
907	S280	-1690.0	386.5
908	S279	-1710.0	511.5
909	S278	-1730.0	386.5
910	S277	-1750.0	511.5
911	S276	-1770.0	386.5
912	S275	-1790.0	511.5
913	S274	-1810.0	386.5
914	S273	-1830.0	511.5
915	S272	-1850.0	386.5
916	S271	-1870.0	511.5
917	S270	-1890.0	386.5
918	S269	-1910.0	511.5
919	S268	-1930.0	386.5
920	S267	-1950.0	511.5
921	S266	-1970.0	386.5
922	S265	-1990.0	511.5
923	S264	-2010.0	386.5
924	S263	-2030.0	511.5
925	S262	-2050.0	386.5
926	S261	-2070.0	511.5
927	S260	-2090.0	386.5
928	S259	-2110.0	511.5
929	S258	-2130.0	386.5
930	S257	-2150.0	511.5
931	S256	-2170.0	386.5
932	S255	-2190.0	511.5
933	S254	-2210.0	386.5
934	S253	-2230.0	511.5
935	S252	-2250.0	386.5
936	S251	-2270.0	511.5
937	S250	-2290.0	386.5
938	S249	-2310.0	511.5
939	S248	-2330.0	386.5
940	S247	-2350.0	511.5
941	S246	-2370.0	386.5
942	S245	-2390.0	511.5
943	S244	-2410.0	386.5
944	S243	-2430.0	511.5
945	S242	-2450.0	386.5
946	S241	-2470.0	511.5
947	S240	-2490.0	386.5
948	S239	-2510.0	511.5

Pad #	PAD Name	X	Y
949	S238	-2530.0	386.5
950	S237	-2550.0	511.5
951	S236	-2570.0	386.5
952	S235	-2590.0	511.5
953	S234	-2610.0	386.5
954	S233	-2630.0	511.5
955	S232	-2650.0	386.5
956	S231	-2670.0	511.5
957	S230	-2690.0	386.5
958	S229	-2710.0	511.5
959	S228	-2730.0	386.5
960	S227	-2750.0	511.5
961	S226	-2770.0	386.5
962	S225	-2790.0	511.5
963	S224	-2810.0	386.5
964	S223	-2830.0	511.5
965	S222	-2850.0	386.5
966	S221	-2870.0	511.5
967	S220	-2890.0	386.5
968	S219	-2910.0	511.5
969	S218	-2930.0	386.5
970	S217	-2950.0	511.5
971	S216	-2970.0	386.5
972	S215	-2990.0	511.5
973	S214	-3010.0	386.5
974	S213	-3030.0	511.5
975	S212	-3050.0	386.5
976	S211	-3070.0	511.5
977	S210	-3090.0	386.5
978	S209	-3110.0	511.5
979	S208	-3130.0	386.5
980	S207	-3150.0	511.5
981	S206	-3170.0	386.5
982	S205	-3190.0	511.5
983	S204	-3210.0	386.5
984	S203	-3230.0	511.5
985	S202	-3250.0	386.5
986	S201	-3270.0	511.5
987	S200	-3290.0	386.5
988	S199	-3310.0	511.5
989	S198	-3330.0	386.5
990	S197	-3350.0	511.5
991	S196	-3370.0	386.5
992	S195	-3390.0	511.5
993	S194	-3410.0	386.5
994	S193	-3430.0	511.5
995	S192	-3450.0	386.5
996	S191	-3470.0	511.5
997	S190	-3490.0	386.5
998	S189	-3510.0	511.5
999	S188	-3530.0	386.5
1000	S187	-3550.0	511.5
1001	S186	-3570.0	386.5
1002	S185	-3590.0	511.5
1003	S184	-3610.0	386.5
1004	S183	-3630.0	511.5
1005	S182	-3650.0	386.5
1006	S181	-3670.0	511.5
1007	S180	-3690.0	386.5
1008	S179	-3710.0	511.5
1009	S178	-3730.0	386.5
1010	S177	-3750.0	511.5
1011	S176	-3770.0	386.5
1012	S175	-3790.0	511.5
1013	S174	-3810.0	386.5
1014	S173	-3830.0	511.5
1015	S172	-3850.0	386.5
1016	S171	-3870.0	511.5
1017	S170	-3890.0	386.5
1018	S169	-3910.0	511.5
1019	S168	-3930.0	386.5
1020	S167	-3950.0	511.5
1021	S166	-3970.0	386.5
1022	S165	-3990.0	511.5
1023	S164	-4010.0	386.5
1024	S163	-4030.0	511.5
1025	S162	-4050.0	386.5
1026	S161	-4070.0	511.5
1027	S160	-4090.0	386.5
1028	S159	-4110.0	511.5
1029	S158	-4130.0	386.5
1030	S157	-4150.0	511.5
1031	S156	-4170.0	386.5
1032	S155	-4190.0	511.5
1033	S154	-4210.0	386.5
1034	S153	-4230.0	511.5
1035	S152	-4250.0	386.5

Pad #	PAD Name	X	Y
1036	S151	-4270.0	511.5
1037	S150	-4290.0	386.5
1038	S149	-4310.0	511.5
1039	S148	-4330.0	386.5
1040	S147	-4350.0	511.5
1041	S146	-4370.0	386.5
1042	S145	-4390.0	511.5
1043	S144	-4410.0	386.5
1044	S143	-4430.0	511.5
1045	S142	-4450.0	386.5
1046	S141	-4470.0	511.5
1047	S140	-4490.0	386.5
1048	S139	-4510.0	511.5
1049	S138	-4530.0	386.5
1050	S137	-4550.0	511.5
1051	S136	-4570.0	386.5
1052	S135	-4590.0	511.5
1053	S134	-4610.0	386.5
1054	S133	-4630.0	511.5
1055	S132	-4650.0	386.5
1056	S131	-4670.0	511.5
1057	S130	-4690.0	386.5
1058	S129	-4710.0	511.5
1059	S128	-4730.0	386.5
1060	S127	-4750.0	511.5
1061	S126	-4770.0	386.5
1062	S125	-4790.0	511.5
1063	S124	-4810.0	386.5
1064	S123	-4830.0	511.5
1065	S122	-4850.0	386.5
1066	S121	-4870.0	511.5
1067	S120	-4890.0	386.5
1068	S119	-4910.0	511.5
1069	S118	-4930.0	386.5
1070	S117	-4950.0	511.5
1071	S116	-4970.0	386.5
1072	S115	-4990.0	511.5
1073	S114	-5010.0	386.5
1074	S113	-5030.0	511.5
1075	S112	-5050.0	386.5
1076	S111	-5070.0	511.5
1077	S110	-5090.0	386.5
1078	S109	-5110.0	511.5
1079	S108	-5130.0	386.5
1080	S107	-5150.0	511.5
1081	S106	-5170.0	386.5
1082	S105	-5190.0	511.5
1083	S104	-5210.0	386.5
1084	S103	-5230.0	511.5
1085	S102	-5250.0	386.5
1086	S101	-5270.0	511.5
1087	S100	-5290.0	386.5
1088	S99	-5310.0	511.5
1089	S98	-5330.0	386.5
1090	S97	-5350.0	511.5
1091	S96	-5370.0	386.5
1092	S95	-5390.0	511.5
1093	S94	-5410.0	386.5
1094	S93	-5430.0	511.5
1095	S92	-5450.0	386.5
1096	S91	-5470.0	511.5
1097	S90	-5490.0	386.5
1098	S89	-5510.0	511.5
1099	S88	-5530.0	386.5
1100	S87	-5550.0	511.5
1101	S86	-5570.0	386.5
1102	S85	-5590.0	511.5
1103	S84	-5610.0	386.5
1104	S83	-5630.0	511.5
1105	S82	-5650.0	386.5
1106	S81	-5670.0	511.5
1107	S80	-5690.0	386.5
1108	S79	-5710.0	511.5
1109	S78	-5730.0	386.5
1110	S77	-5750.0	511.5
1111	S76	-5770.0	386.5
1112	S75	-5790.0	511.5
1113	S74	-5810.0	386.5
1114	S73	-5830.0	511.5
1115	S72	-5850.0	386.5
1116	S71	-5870.0	511.5
1117	S70	-5890.0	386.5
1118	S69	-5910.0	511.5
1119	S68	-5930.0	386.5
1120	S67	-5950.0	511.5
1121	S66	-5970.0	386.5
1122	S65	-5990.0	511.5
1123	S64	-6010.0	386.5
1124	S63	-6030.0	511.5
1125	S62	-6050.0	386.5
1126	S61	-6070.0	511.5
1127	S60	-6090.0	386.5
1128	S59	-6110.0	511.5
1129	S58	-6130.0	386.5
1130	S57	-6150.0	511.5
1131	S56	-6170.0	386.5
1132	S55	-6190.0	511.5
1133	S54	-6210.0	386.5
1134	S53	-6230.0	511.5
1135	S52	-6250.0	386.5
1136	S51	-6270.0	511.5
1137	S50	-6290.0	386.5
1138	S49	-6310.0	511.5
1139	S48	-6330.0	386.5
1140	S47	-6350.0	511.5
1141	S46	-6370.0	386.5
1142	S45	-6390.0	511.5
1143	S44	-6410.0	386.5
1144	S43	-6430.0	511.5
1145	S42	-6450.0	386.5
1146	S41	-6470.0	511.5
1147	S40	-6490.0	386.5
1148	S39	-6510.0	511.5
1149	S38	-6530.0	386.5
1150	S37	-6550.0	511.5
1151	S36	-6570.0	386.5
1152	S35	-6590.0	511.5
1153	S34	-6610.0	386.5
1154	S33	-6630.0	511.5
1155	S32	-6650.0	386.5
1156	S31	-6670.0	511.5
1157	S30	-6690.0	386.5
1158	S29	-6710.0	511.5
1159	S28	-6730.0	386.5
1160	S27	-6750.0	511.5
1161	S26	-6770.0	386.5
1162	S25	-6790.0	511.5
1163	S24	-6810.0	386.5
1164	S23	-6830.0	511.5
1165	S22	-6850.0	386.5
1166	S21	-6870.0	511.5
1167	S20	-6890.0	386.5
1168	S19	-6910.0	511.5
1169	S18	-6930.0	386.5
1170	S17	-6950.0	511.5
1171	S16	-6970.0	386.5
1172	S15	-6990.0	511.5
1173	S14	-7010.0	386.5
1174	S13	-7030.0	511.5
1175	S12	-7050.0	386.5
1176	S11	-7070.0	511.5
1177	S10	-7090.0	386.5
1178	S9	-7110.0	511.5
1179	S8	-7130.0	386.5
1180	S7	-7150.0	511.5
1181	S6	-7170.0	386.5
1182	S5	-7190.0	511.5
1183	S4	-7210.0	386.5
1184	S3	-7230.0	511.5
1185	S2	-7250.0	386.5
1186	S1	-7270.0	511.5
1187	TESTO35	-7290.0	386.5
1188	TESTO36	-7350.0	511.5
1189	VGLDMY3	-7370.0	386.5
1190	G320	-7390.0	511.5
1191	G318	-7410.0	386.5
1192	G316	-7430.0	511.5
1193	G314	-7450.0	386.5
1194	G312	-7470.0	511.5
1195	G310	-7490.0	386.5
1196	G308	-7510.0	511.5
1197	G306	-7530.0	386.5
1198	G304	-7550.0	511.5
1199	G302	-7570.0	386.5
1200	G300	-7590.0	511.5
1201	G298	-7610.0	386.5
1202	G296	-7630.0	511.5
1203	G294	-7650.0	386.5
1204	G292	-7670.0	511.5
1205	G290	-7690.0	386.5
1206	G288	-7710.0	511.5
1207	G286	-7730.0	386.5
1208	G284	-7750.0	511.5
1209	G282	-7770.0	386.5
1210	G280	-7790.0	511.5
1211	G278	-7810.0	386.5
1212	G276	-7830.0	511.5
1213	G274	-7850.0	386.5
1214	G272	-7870.0	511.5
1215	G270	-7890.0	386.5
1216	G268	-7910.0	511.5
1217	G266	-7930.0	386.5
1218	G264	-7950.0	511.5
1219	G262	-7970.0	386.5
1220	G260	-7990.0	511.5
1221	G258	-8010.0	386.5
1222	G256	-8030.0	511.5
1223	G254	-8050.0	386.5
1224	G252	-8070.0	511.5
1225	G250	-8090.0	386.5
1226	G248	-8110.0	511.5
1227	G246	-8130.0	386.5
1228	G244	-8150.0	511.5
1229	G242	-8170.0	386.5
1230	G240	-8190.0	511.5
1231	G238	-8210.0	386.5
1232	G236	-8230.0	511.5
1233	G234	-8250.0	386.5
1234	G232	-8270.0	511.5
1235	G230	-8290.0	386.5
1236	G228	-8310.0	511.5
1237	G226	-8330.0	386.5
1238	G224	-8350.0	511.5
1239	G222	-8370.0	386.5
1240	G220	-8390.0	511.5
1241	G218	-8410.0	386.5
1242	G216	-8430.0	511.5
1243	G214	-8450.0	386.5
1244	G212	-8470.0	511.5
1245	G210	-8490.0	386.5
1246	G208	-8510.0	511.5
1247	G206	-8530.0	386.5
1248	G204	-8550.0	511.5
1249	G202	-8570.0	386.5
1250	G200	-8590.0	511.5
1251	G198	-8610.0	386.5
1252	G196	-8630.0	511.5
1253	G194	-8650.0	386.5
1254	G192	-8670.0	511.5
1255	G190	-8690.0	386.5
1256	G188	-8710.0	511.5
1257	G186	-8730.0	386.5
1258	G184	-8750.0	511.5
1259	G182	-8770.0	386.5
1260	G180	-8790.0	511.5
1261	G178	-8810.0	386.5
1262	G176	-8830.0	511.5
1263	G174	-8850.0	386.5
1264	G172	-8870.0	511.5
1265	G170	-8890.0	386.5
1266	G168	-8910.0	511.5
1267	G166	-8930.0	386.5
1268	G164	-8950.0	511.5
1269	G162	-8970.0	386.5
1270	G160	-8990.0	511.5
1271	G158	-9010.0	386.5
1272	G156	-9030.0	511.5
1273	G154	-9050.0	386.5
1274	G152	-9070.0	511.5
1275	G150	-9090.0	386.5
1276	G148	-9110.0	511.5
1277	G146	-9130.0	386.5
1278	G144	-9150.0	511.5
1279	G142	-9170.0	386.5
1280	G140	-9190.0	511.5
1281	G138	-9210.0	386.5
1282	G136	-9230.0	511.5
1283	G134	-9250.0	386.5
1284	G132	-9270.0	511.5
1285	G130	-9290.0	386.5
1286	G128	-9310.0	511.5
1287	G126	-9330.0	386.5
1288	G124	-9350.0	511.5
1289	G122	-9370.0	386.5
1290	G120	-9390.0	511.5
1291	G118	-9410.0	386.5
1292	G116	-9430.0	511.5
1293	G114	-9450.0	386.5
1294	G112	-9470.0	511.5
1295	G110	-9490.0	386.5
1296	G108	-9510.0	511.5

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Pad # .	PAD Name	X	Y
1297	G106	-9530.0	386.5
1298	G104	-9550.0	511.5
1299	G102	-9570.0	386.5
1300	G100	-9590.0	511.5
1301	G98	-9610.0	386.5
1302	G96	-9630.0	511.5
1303	G94	-9650.0	386.5
1304	G92	-9670.0	511.5
1305	G90	-9690.0	386.5
1306	G88	-9710.0	511.5
1307	G86	-9730.0	386.5
1308	G84	-9750.0	511.5
1309	G82	-9770.0	386.5
1310	G80	-9790.0	511.5
1311	G78	-9810.0	386.5
1312	G76	-9830.0	511.5
1313	G74	-9850.0	386.5
1314	G72	-9870.0	511.5
1315	G70	-9890.0	386.5
1316	G68	-9910.0	511.5
1317	G66	-9930.0	386.5
1318	G64	-9950.0	511.5
1319	G62	-9970.0	386.5
1320	G60	-9990.0	511.5
1321	G58	-10010.0	386.5
1322	G56	-10030.0	511.5
1323	G54	-10050.0	386.5
1324	G52	-10070.0	511.5
1325	G50	-10090.0	386.5
1326	G48	-10110.0	511.5
1327	G46	-10130.0	386.5
1328	G44	-10150.0	511.5
1329	G42	-10170.0	386.5
1330	G40	-10190.0	511.5
1331	G38	-10210.0	386.5
1332	G36	-10230.0	511.5
1333	G34	-10250.0	386.5
1334	G32	-10270.0	511.5
1335	G30	-10290.0	386.5
1336	G28	-10310.0	511.5
1337	G26	-10330.0	386.5
1338	G24	-10350.0	511.5
1339	G22	-10370.0	386.5
1340	G20	-10390.0	511.5
1341	G18	-10410.0	386.5
1342	G16	-10430.0	511.5
1343	G14	-10450.0	386.5
1344	G12	-10470.0	511.5
1345	G10	-10490.0	386.5
1346	G8	-10510.0	511.5
1347	G6	-10530.0	386.5
1348	G4	-10550.0	511.5
1349	G2	-10570.0	386.5
1350	VGLDMY4	-10590.0	511.5
1351	DUMMYR9	-10610.0	386.5
1352	DUMMYR10	-10630.0	511.5
1353	TESTO37	-10650.0	386.5
1354	TESTO38	-10670.0	511.5

Alignment mark	X	Y
1-a	-10613.0	-468.0
1-b	10613.0	-468.0

Bump Arrangement

S1 ~ S720 G1 ~ G320 DUMMYR TESTO VGLDMY (No. 299 ~ No. 1354)	20 21 100 225 25 S=2100 ² Unit:
I/O PINS (No. 1 ~ No. 298)	50 20 80 S=4000 ² Min. 70 Unit:

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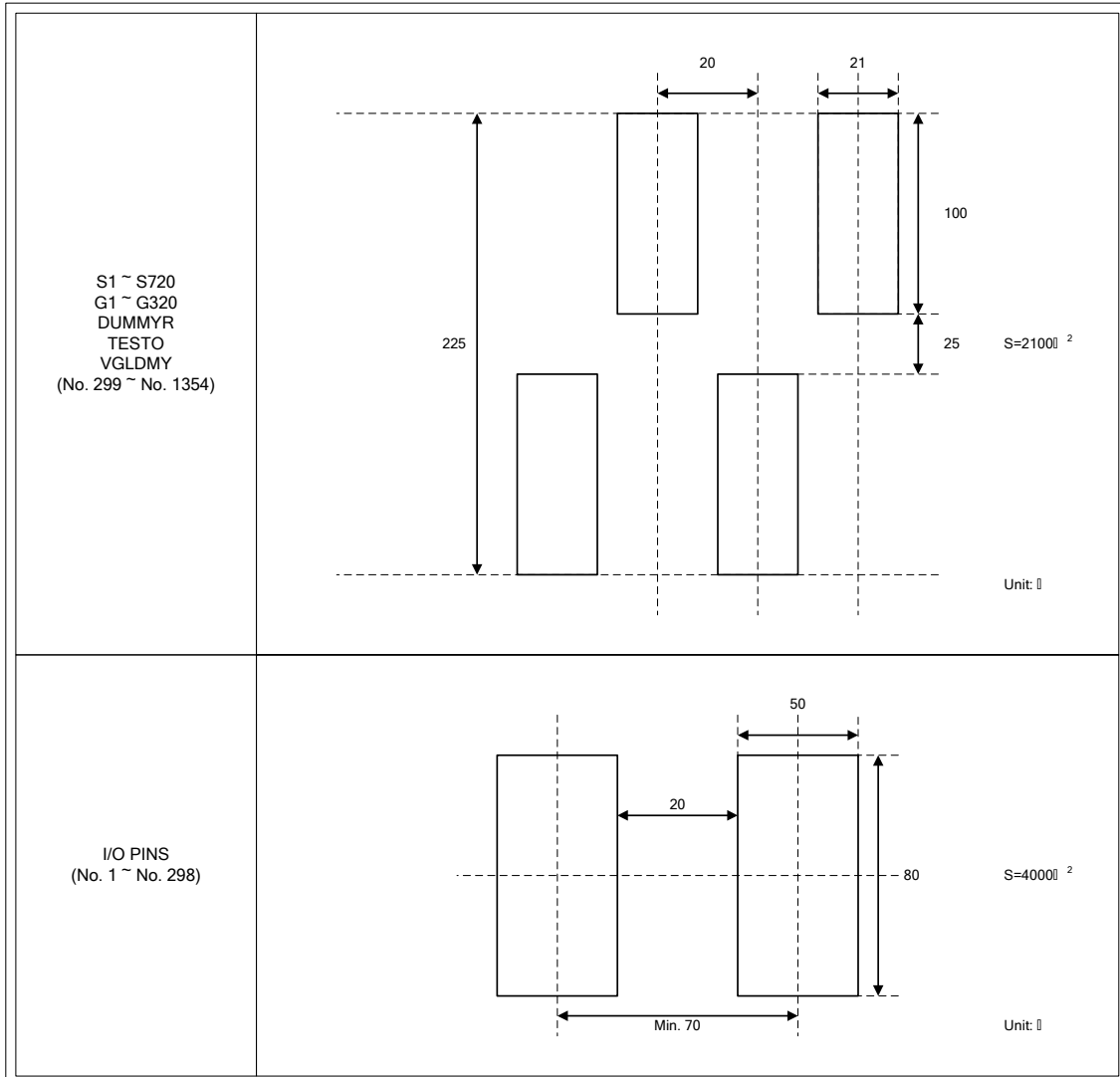
Block Function

System Interface

The LGDP4531 supports 2-system high-speed interfaces: 80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and a Serial Peripheral Interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

The LGDP4531 has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the LGDP4531 read the first data from the internal GRAM. Valid data are read out after the LGDP4531 performs the second read operation.

Instructions are written consecutively as the instruction execution time except starting oscillator takes 0 clock cycle.

Table 2 Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)

80-system I/F			Function
WR*	RD*	RS	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 3 Register Selection (Serial Peripheral Interface)

Start Byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

External Display Interface

The LGDP4531 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB[17:0]) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section.

The LGDP4531 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18bit) bytes, using 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Generator

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

The LGDP4531 generates RC oscillation with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency is changed according to the value of an external resistor. Adjust the oscillation frequency in accordance to the operating voltage or the frame frequency. An operating clock can be input externally. During standby mode, RC oscillation is halted to reduce power consumption. For details, see "Oscillator."

LCD Driver Circuit

The LCD driver circuit of the LGDP4531 consists of a 528-output source driver (S1 ~ S528) and a 240-output gate driver (G1~G240). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Drive Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

GRAM Address MAP

Table 4 GRAM address and display panel position (SS = "0", BGR = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G320	"00000"H			"00001"H			"00002"H			"00003"H			…	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			…	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			…	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			…	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			…	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			…	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			…	"006EC"H			"006ED"H			"006EE"H			"006EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			…	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G312	"00800"H			"00801"H			"00802"H			"00803"H			…	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G311	"00900"H			"00901"H			"00902"H			"00903"H			…	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G310	"00A00"H			"00A01"H			"00A02"H			"00A03"H			…	"00AEC"H			"00AED"H			"00AEE"H			"00AEF"H		
G12	G309	"00B00"H			"00B01"H			"00B02"H			"00B03"H			…	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G308	"00C00"H			"00C01"H			"00C02"H			"00C03"H			…	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G307	"00D00"H			"00D01"H			"00D02"H			"00D03"H			…	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G306	"00E00"H			"00E01"H			"00E02"H			"00E03"H			…	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G305	"00F00"H			"00F01"H			"00F02"H			"00F03"H			…	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G304	"01000"H			"01001"H			"01002"H			"01003"H			…	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G303	"01100"H			"01101"H			"01102"H			"01103"H			…	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G302	"01200"H			"01201"H			"01202"H			"01203"H			…	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G301	"01300"H			"01301"H			"1302"H			"01303"H			…	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
⋮	⋮	⋮			⋮			⋮			⋮			…	⋮			⋮			⋮			⋮		
⋮	⋮	⋮			⋮			⋮			⋮			…	⋮			⋮			⋮			⋮		
G313	G8	"13800"H			"13801"H			"13802"H			"13803"H			…	"138EC"H			"138ED"H			"138EE"H			"138EF"H		
G314	G7	"13900"H			"13901"H			"13902"H			"13903"H			…	"139EC"H			"139ED"H			"139EE"H			"139EF"H		
G315	G6	"13A00"H			"13A01"H			"13A02"H			"13A03"H			…	"13AEC"H			"13AED"H			"13AEE"H			"13AEF"H		
G316	G5	"13B00"H			"13B01"H			"13B02"H			"13B03"H			…	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			…	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			…	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			…	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			…	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

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Figure 2　GRAM data and display data: system interface (SS = "0", BGR = "0")

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80-system 9-bit interface (2 transfers, 262k colors)

	1st transfer									2nd transfer								
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (3n + 1)						S (3n + 2)						S (3n + 3)					

Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface or SPI (2 transfers, 65k colors) TRI = "0

	1st transfer								2nd transfer							
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (3n + 1)						S (3n + 2)						S (3n + 3)					

Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "0"

	1st transfer		2nd transfer								3rd transfer						
GRAM data	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (3n + 1)						S (3n + 2)						S (3n + 3)					

Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "1"

	1st transfer						2nd transfer						3rd transfer					
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (3n + 1)						S (3n + 2)						S (3n + 3)					

Note: n = lower eight bits of address (0 to 239)

Figure 3   GRAM data and display data: system interface (SS = "0", BGR = "0")

18-bit RGB interface

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0

RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Output pin	S (3n + 1)	S (3n + 2)	S (3n + 3)

Note: n = lower eight bits of address (0 to 239)

16-bit RGB interface

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13		DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1

RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Output pin	S (3n + 1)	S (3n + 2)	S (3n + 3)

Note: n = lower eight bits of address (0 to 239)

6-bit RGB interface

	1st transfer	2nd transfer	3rd transfer
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12

RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Output pin	S (3n + 1)	S (3n + 2)	S (3n + 3)

Note: n = lower eight bits of address (0 to 239)

Figure 4 GRAM data and display data: system interface (SS = "0", BGR = "0")

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Table 5 GRAM address and display panel position (SS = "1", BGR = "1")

S/G pin		S720 S719 S718	S717 S716 S715	S714 S713 S712	S711 S710 S709	…	S12 S11 S10	S9 S8 S7	S6 S5 S4	S3 S2 S1
GS=0	GS=1	DB[17:0]	DB[17:0]	DB[17:0]	DB[17:0]	…	DB[17:0]	DB[17:0]	DB[17:0]	DB[17:0]
G1	G320	"00000"H	"00001"H	"00002"H	"00003"H	…	"000EC"H	"000ED"H	"000EE"H	"000EF"H
G2	G319	"00100"H	"00101"H	"00102"H	"00103"H	…	"001EC"H	"001ED"H	"001EE"H	"001EF"H
G3	G318	"00200"H	"00201"H	"00202"H	"00203"H	…	"002EC"H	"002ED"H	"002EE"H	"002EF"H
G4	G317	"00300"H	"00301"H	"00302"H	"00303"H	…	"003EC"H	"003ED"H	"003EE"H	"003EF"H
G5	G316	"00400"H	"00401"H	"00402"H	"00403"H	…	"004EC"H	"004ED"H	"004EE"H	"004EF"H
G6	G315	"00500"H	"00501"H	"00502"H	"00503"H	…	"005EC"H	"005ED"H	"005EE"H	"005EF"H
G7	G314	"00600"H	"00601"H	"00602"H	"00603"H	…	"006EC"H	"006ED"H	"006EE"H	"006EF"H
G8	G313	"00700"H	"00701"H	"00702"H	"00703"H	…	"007EC"H	"007ED"H	"007EE"H	"007EF"H
G9	G312	"00800"H	"00801"H	"00802"H	"00803"H	…	"008EC"H	"008ED"H	"008EE"H	"008EF"H
G10	G311	"00900"H	"00901"H	"00902"H	"00903"H	…	"009EC"H	"009ED"H	"009EE"H	"009EF"H
G11	G310	"00A00"H	"00A01"H	"00A02"H	"00A03"H	…	"00AEC"H	"00AED"H	"00AEE"H	"00AEF"H
G12	G309	"00B00"H	"00B01"H	"00B02"H	"00B03"H	…	"00BEC"H	"00BED"H	"00BEE"H	"00BEF"H
G13	G308	"00C00"H	"00C01"H	"00C02"H	"00C03"H	…	"00CEC"H	"00CED"H	"00CEE"H	"00CEF"H
G14	G307	"00D00"H	"00D01"H	"00D02"H	"00D03"H	…	"00DEC"H	"00DED"H	"00DEE"H	"00DEF"H
G15	G306	"00E00"H	"00E01"H	"00E02"H	"00E03"H	…	"00EEC"H	"00EED"H	"00EEE"H	"00EEF"H
G16	G305	"00F00"H	"00F01"H	"00F02"H	"00F03"H	…	"00FEC"H	"00FED"H	"00FEE"H	"00FEF"H
G17	G304	"01000"H	"01001"H	"01002"H	"01003"H	…	"010EC"H	"010ED"H	"010EE"H	"010EF"H
G18	G303	"01100"H	"01101"H	"01102"H	"01103"H	…	"011EC"H	"011ED"H	"011EE"H	"011EF"H
G19	G302	"01200"H	"01201"H	"01202"H	"01203"H	…	"012EC"H	"012ED"H	"012EE"H	"012EF"H
G20	G301	"01300"H	"01301"H	"1302"H	"01303"H	…	"013EC"H	"013ED"H	"013EE"H	"013EF"H
⋮	⋮	⋮	⋮	⋮	⋮	…	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	…	⋮	⋮	⋮	⋮
G313	G8	"13800"H	"13801"H	"13802"H	"13803"H	…	"138EC"H	"138ED"H	"138EE"H	"138EF"H
G314	G7	"13900"H	"13901"H	"13902"H	"13903"H	…	"139EC"H	"139ED"H	"139EE"H	"139EF"H
G315	G6	"13A00"H	"13A01"H	"13A02"H	"13A03"H	…	"13AEC"H	"13AED"H	"13AEE"H	"13AEF"H
G316	G5	"13B00"H	"13B01"H	"13B02"H	"13B03"H	…	"13BEC"H	"13BED"H	"13BEE"H	"13BEF"H
G317	G4	"13C00"H	"13C01"H	"13C02"H	"13C03"H	…	"13CEC"H	"13CED"H	"13CEE"H	"13CEF"H
G318	G3	"13D00"H	"13D01"H	"13D02"H	"13D03"H	…	"13DEC"H	"13DED"H	"13DEE"H	"13DEF"H
G319	G2	"13E00"H	"13E01"H	"13E02"H	"13E03"H	…	"13EEC"H	"13EED"H	"13EEE"H	"13EEF"H
G320	G1	"13F00"H	"13F01"H	"13F02"H	"13F03"H	…	"13FEC"H	"13FED"H	"13FEE"H	"13FEF"H

80-system 18-bit interface

80-system 16-bit interface

80-system 16-bit interface MSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM = "0"

80-system 16-bit interface LSB mode (2 transfers/pixel, 262k colors) TRI = "1", DFM = "1"

Figure 5 GRAM data and display data: system interface (SS = "1", BGR = "1")

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80-system 9-bit interface (2 transfers, 262k colors)

	1st transfer								2nd transfer								
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (720 – 3n)						S (719 – 3n)						S (718 – 3n)					

Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface or SPI (2 transfers, 65k colors) TRI = "0"

	1st transfer								2nd transfer								
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (720 – 3n)						S (719 – 3n)						S (718 – 3n)					

Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "0"

	1st transfer		2nd transfer								3rd transfer							
GRAM data	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (720 – 3n)						S (719 – 3n)						S (718 – 3n)					

Note: n = lower eight bits of address (0 to 239)

80-system 8-bit interface (3 transfers/pixel, 262k colors) TRI = "1", DFM = "1"

	1st transfer						2nd transfer						3rd transfer					
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (720 – 3n)						S (719 – 3n)						S (718 – 3n)					

Note: n = lower eight bits of address (0 to 239)

Figure 6 GRAM data and display data: system interface (SS = "1", BGR = "1")

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18-bit RGB interface

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0

RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (720 – 3n)						S (719 – 3n)						S (718 – 3n)					

Note: n = lower eight bits of address (0 to 239)

16-bit RGB interface

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13		DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	

RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (720 – 3n)						S (719 – 3n)						S (718 – 3n)					

Note: n = lower eight bits of address (0 to 239)

6-bit RGB interface

	1st transfer						2nd transfer						3rd transfer					
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12

RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S (720 – 3n)						S (719 – 3n)						S (718 – 3n)					

Note: n = lower eight bits of address (0 to 239)

Figure 7 GRAM data and display data: system interface (SS = "1", BGR = "1")

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Instructions

Outline

The LGDP4531 adopts 18-bit bus architecture to interface to a high-performance microcomputer. The LGDP4531 starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the instruction register (IR) and the data register (DR). Since internal operations of the LGDP4531 are controlled by the signals sent from the microcomputer, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0) are called instructions. The LGDP4531 use the 18-bit format internally for operations involving internal GRAM access. The instructions of the LGDP4531 are categorized into the following groups.

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

Normally, the instruction for writing data to the internal GRAM is used the most often. Since the LGDP4531 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there is less load on the program in the microcomputer. Since instructions are executed in 0 cycles, it is possible to write instructions consecutively.

Instruction Data Format

Note that as the following figure shows, the assignment of 16 instruction bits(IB15-0) to the data bus differs in different interface operations. Write instruction according to the data transfer format of the interface in use.

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80-system 18-bit interface

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0

Instruction Bit (IB)	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8		IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

80-system 16-bit interface

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10		DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1

Instruction Bit (IB)	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8		IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

80-system 9-bit interface

1st transfer — 2nd transfer

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9

Instruction Bit (IB)	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8		IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

80-system 8-bit interface or SPI (2/3 transfers)

1st transfer — 2nd transfer

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10		DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10

Instruction Bit (IB)	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8		IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

Figure 8 Instruction bits

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Instruction Description

The following are detailed explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index (IR)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0		*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h - RFFh) of a control register or RAM control to be accessed using binary numbers "0000_0000" to "1111_1111". An access to the register as well as instruction bits contained in it is disabled unless its index is represented in this register.

Device code read (R00h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1		0	1	0	0	0	1	0	1	0	0	1	1	0	0	0	1

The device code "4531"H is read out when reading out this register forcibly.

Driver output control (R01h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

SS – Selects the shift direction of outputs from the source pins.

If SS = "0", the source pins output from S1 to S720.
If SS = "1", the source pins output from S720 to S1.

The combination of SS and BGR bits controls the order of assigning RGB dots to the source driver pins S1 to S720.

If SS = "0" and BGR = "0", RGB dots are assigned interchangeably from S1 to S720.
If SS = "1" and BGR = "1", RGB dots are assigned interchangeably from S720 to S1.

When changing SS or BGR bits, RAM data must be rewritten.

SM – Sets gate driver assignment in combination with the GS bit according to the LC module. See "Scan mode setting".

LCD Driving Wave Control (R02h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	BC0	EOR	0	0			NW[5:0]			

NW[5:0] – Specify n, the number of raster-rows from 1 to 64, where alternations occurs every n+1 raster-rows when C-pattern waveform is generatd(BC0=1).

EOR – When EOR=1, alternation occured by applying EOR(Exclusive OR) operatin to an odd/even frame selecting signal and n-raster-row inversion signal while a C-pattern waveform is generated(BC0=1).

This instruction is used when liquid crystal alternation drive is not available due to combination of numbers of LCD raster-rows and the value of "x n". For details, see n-raster-row Inversion Alternating Drive.

BC0 – Selects the liquid crystal drive waveform VCOM. See "Line Inversion AC Drive" for details.
        BC0 = 0: frame inversion waveform is selected.
        BC0 = 1: Line inversion waveform is selected.
In either liquid crystal drive method, the polarity inversion is halted in blank periods (back and front porch periods).

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D[1:0]		AM	0	0	0

The LGDP4531 modifies data sent from a microcomputer before writing them to the internal GRAM in order to write the GRAM data in high speed and reduce software processing load on the microcomputer. See "Graphics Operation Function" for details.

TRI – Selects the RAM data transfer mode in 80-system 8-bit/16-bit bus interface operation.
In 8-bit interface operation,
        TRI = 0: 16-bit RAM data is transferred in two transfers.
        TRI = 1: 18-bit RAM data is transferred in three transfers.
In 16-bit bus interface operation,
        TRI = 0: 16-bit RAM data is transferred in one transfer.
        TRI = 1: 18-bit RAM data is transferred in two transfers.
Make sure TRI = 0 when not using either 16-bit or 8-bit interface. Also, set TRI = 0 during read operation.

DFM – Sets the mode of transferring data to the internal RAM when TRI = "1". See the following figures for details.

Table 6

TRI	DFM	RAM write data transfer via serial peripheral interface (SPI)
0	*	SPI (2 transfers/pixel) – 65k colors available
1	0	SPI (3 transfers/pixel) – 262k colors available
1	1	Setting disabled

Table 7

TRI	DFM	RAM write data transfer via 8-bit interface
0	*	80-system 8-bit interface (2 transfers/pixel) – 65k colors

1st transfer / 2nd transfer

GRAM Data	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10
RGB Assign	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

TRI	DFM	
1	0	80-system 8-bit interface (3 transfers/pixel) – 262k colors

1st / 2nd transfer / 3rd transfer

GRAM Data	DB11	DB10	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10
RGB Assign	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

TRI	DFM	
1	1	80-system 8-bit interface (3 transfers/pixel) – 262k colors

1st transfer / 2nd transfer / 3rd transfer

GRAM Data	DB17	DB16	DB15	DB14	DB13	DB12	DB17	DB16	DB15	DB14	DB13	DB12	DB17	DB16	DB15	DB14	DB13	DB12
RGB Assign	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Table 8

TRI	DFM	RAM write data transfer via 16-bit interface
0	*	80-system 16-bit interface (1 transfers/pixel) – 65k colors

GRAM Data	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
RGB Assign	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

TRI	DFM	
1	0	80-system 16-bit interface MSB mode(2 transfers/pixel) – 262k colors available

1st transfer / 2nd

GRAM Data	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB17	DB16
RGB Assign	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

TRI	DFM	
1	1	80-system 16-bit interface LSB mode(2 transfers/pixel) – 262k colors available

1st / 2nd transfer

GRAM Data	DB2	DB1	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
RGB Assign	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR – Reverses the order of RGB dots to BGR when writing 18-bit pixel data to the internal GRAM. Note that the orders of RGB dots in both WM[17:0] and CP[17:0] bits are automatically changed upon setting BGR = "1".

ORG – Moves the origin of a window address area in combination with the ID setting. This function is enabled when writing data within the window address area.

I/D[1:0] – The address counter is automatically incremented by 1 as writing data to the internal GRAM when I/D[1:0] = "1". The address counter is automatically decremented by 1 as writing data to the internal GRAM when I/D[1:0] = "0". The increment/decrement can be set separately to each upper (AD[15:8]) / lower (AD[7:0]) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal GRAM is set with the AM bit.

AM – Sets the direction of automatically updating address for writing data to the internal RAM in the address counter (AC). When AM = "0", the address is updated in horizontal writing direction. When AM = "1", the address is updated in vertical writing direction. When a window address area is set, data are written only to the GRAM area specified with window address in the writing direction set with I/D[1:0] and AM bits.
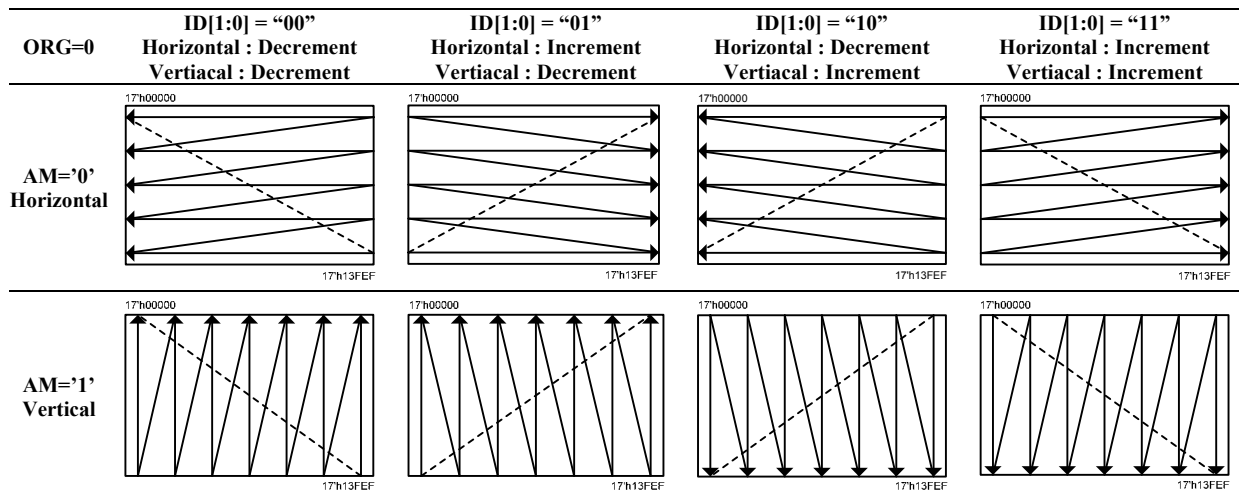
Figure 9   Automatic address update (ORG=0, AM, ID)
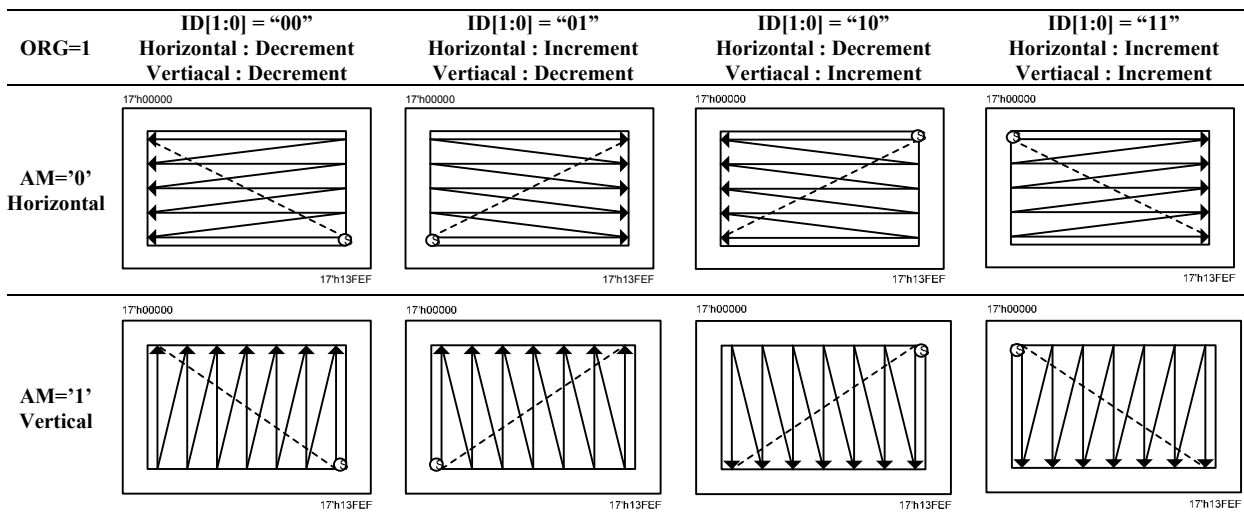
Figure 10   Automatic address update (ORG=1, AM, ID)

Resizing Control (R04h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]	

RSZ[1:0] – Sets the resizing factor. When the RSZ bits are set for resizing, the LGDP4531 writes the data of the resized image in both horizontal and vertical directions according to the resizing factor on the internal GRAM. See "Resizing fuction".

RCH[1:0] – Sets the number of pixels made as the remainder in horizontal direction as a result of resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

RCV[1:0] – Sets the number of pixels made as the remainder in vertical direction as a result of resizing a picture. By specifying the number of remainder pixels with RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

Table 9

RSZ[1:0]	Resizing scale
2'h0	No resizing (x1)
2'h1	x 1/2
2'h2	Setting disabled
2'h3	x 1/4

Table 10

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Table 11

RCV[1:0]	Number of remainder Pixels in Vertical Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

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Display Control 1 (R07h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	PTDE[1:0]		0	0	0	BASEE	0	0	GON	DTE	COL	0	D[1:0]	

D[1:0] – A graphics display appears on the screen when D[1] = "1", and is turned off upon setting D[1] = "0". When setting D[1] = "0", the graphics display data are retained in the internal GRAM and the display appears instantly on the screen upon setting D[1] to "1". When the D[1] bit is "0", i.e. while no display is shown on the screen, all source outputs are at the GND level to reduce charging/discharging current on liquid crystal cells, which is generated during liquid crystal AC drive.

When the display is turned off by setting D[1:0] = 2'h1, the LGDP4531 continues internal display operation. When the display is turned off by setting D[1:0] = 2'h0, the LGDP4531's internal display operation is halted completely. In combination with GON bit, the D[1:0] bits control ON/OFF of graphics display. For details, see "Instruction setting".

Table 12

D[1:0]	BASEE	Source Output (S1-720)	FMARK signal	Internal Operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-display	Operation	Operation
2'h3	0	Non-display	Operation	Operation
	1	Base-image display	Operation	Operation

Notes: 1. The data write operation from the microcomputer is not affected by the setting in the D[1:0] bits.
      2. The PTS bits set the source output level for "non-lit display"

COL – When COL = "1", the 8-color display mode is selected. For details, see the "8-color Display Mode" section. The 8-color display mode is not available in external interface mode.

Table 13

COL	Operating amplifier	Display color
1'h0	64	262,144
1'h1	2	8

Note: When COL=1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

GON, DTE – The combination of settings in GON and DTE bits sets the output level form gate lines(G1-G320). When GON=0, the Vcom output level becomes the GND level.

Table 14

GON	DTE	G1-G320
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

BASEE – Base image display enable bit.
        BASEE = 0 : No base image is displayed. The LGDP4531 drives liquid crystal at no-display
                level or shows only partial images on the screen.
        BASEE = 1 : A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE[1:0] – PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of
partial image 2. When PTDE[1]/[0]=0, the partial image is turned off and only base image is displayed on
the screen. When PTDE[1]/[0]= 1, the partial image is displayed on the screen. In this case, turn off the
base image by setting BASEE = 0.

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0		FP[3:0]			0	0	0	0		BP[3:0]		

FP[3:0]/BP[3:0] – Sets the blank period made at the beginning and the end of a display (front porch and
back porch, respectively). The FP[3:0] and BP[3:0] bits specify the number of lines for the front and back
porch periods, respectively. In setting, be sure:

        BP + FP ≤ 16 lines
        FP ≥ 2 lines
        BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC
signal, followed by a display operation period. After driving the number of lines set with NL bits, a front
porch period starts. After the front porch period, a blank period continues until the next input of VSYNC
signal.

Table 15

FP[3:0]/BP[3:0]	Number of lines for the front/back porches
4'h0	Setting disabled
4'h1	Setting disabled
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting disabled

Note: The output timing to the LCD is delayed by a 2-line period from the input of synchronizing signal.
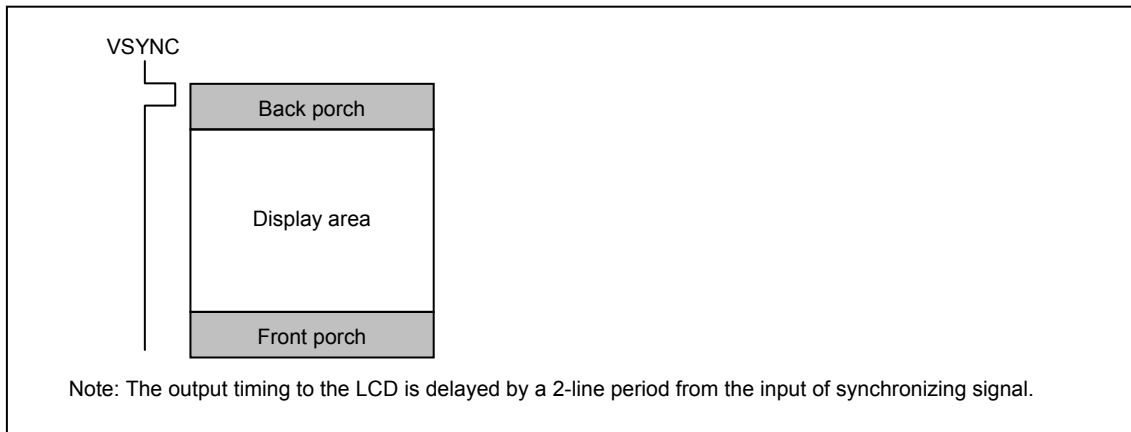
Figure 11 Back/front porches

Set the BP[3:0], FP[3:0] bits as follows in each operation mode.

Table 16

Internal clock operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS[2:0]			0	0	PTG[1:0]		ISC[3:0]			

ISC[3:0] – Set the interval of scan when PTG[1:0] sets the interval scan. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal is inverted in the same cycle as the interval scan.

Table 17

ISC[3:0]	Scan cycle	Time for interval when(fFLM)=60Hz
4'h0	Setting disabled	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTG[1:0] – Set the scan mode in non-display area, which is made between partial display periods of the first and the second images, or turning off both base and partial images(full-screen non display). The setting is commonly applied to all non-display drive period.

Table 18

PTG[1:0]	Gate drive operation In non-display area	Source output level In non-display area	Vcom output
2'h0	Normal scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h1	Setting disabled	-	-
2'h2	Interval scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h3	Setting disabled	-	-

Note: Select frame-inversion AC drive when setting interval scan.

PTS[2:0] – Set the source output in non-display drive period.

Table 19

PTS[2:0]	Source output level		Grayscale amplifier In operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3h0	V63	V0	V0 to V63	Register setting(DC0,DC1)
3h1	Setting disabled	Setting disabled	-	-
3h2	GND	GND	V0 to V63	Register setting(DC0,DC1)
3h3	Hi-Z	Hi-Z	V0 to V63	Register setting(DC0,DC1)
3'h4	V63	V0	V0 and V63	1/2 the frequency set with DC0,DC1
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0 and V63	1/2 the frequency set with DC0,DC1
3'h7	Hi-Z	Hi-Z	V0 and V63	1/2 the frequency set with DC0,DC1

Notes: 1.The gate output level in non-display drive period is controlled by the PTG setting(off-scan mode).

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI[2:0]		

FMI[2:0] – Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE – When FMARKOE=1, the LGDP4531 starts outputting FMARK signal from the FMARK pin in the output interval set with the FMI[2:0] bits. See "FMARK" for details.

Table 20

FMI[2:0]	Output interval
3'h0	1 frame
3'h1	2frame
3'h3	4 frame
3'h5	6 frame
Others settings	Setting disabled

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External Display Interface Control 1 (R0Ch)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	ENC[1:0]		0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

ENC[1:0] – Sets the RAM data write cycle in RGB interface mode.

Table 21 ENC[1:0] bits

ENC[1:0]	RAM data write cycle
2'h00	Write data to RAM every frame cycle
2'h01	Setting disabled
2'h10	Write data to RAM every 2 frame cycles
2'h11	Write data to RAM every 4 frame cycles

RM – Selects the interface to access the LGDP4531's internal GRAM. The RAM access is possible only via the interface selected with the RM bit. Set RM to "1" when writing display data via the RGB interface. The LGDP4531 allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 22 RM bit

RM	Interface for RAM access
1'h0	System interface/VSYNC interface
1'h1	RGB interface

RIM[1:0] – Selects one of the following RGB interface modes when the RGB interface mode is selected with the RM and DM bits. Make this setting before display operation via external display interface. Do not make changes to the setting during display operation.

Table 23 RIM[1:0] bits

RIM[1:0]	RGB interface mode
2'h00	18-bit RGB interface (1 transfer/pixel)
2'h01	16-bit RGB interface (1 transfer/pixel)
2'h10	6-bit RGB interface (3 transfers/pixel)
2'h11	Setting disabled

DM[1:0] – Sets the display operation mode. By setting DM[1:0] as follows, it is possible to switch between the internal clock operation mode and the external display interface mode. Do not switch between different external interface modes (RGB interface and VSYNC interface).

Table 24 DM[1:0] bits

DM[1:0]	Display operation mode
2'h00	Internal clock operation
2'h01	RGB interface
2'h10	VSYNC interface
2'h11	Setting disabled

Notes:
1. Instructions are set only via the system interface.

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2. Be sure that data transfer and dot clock input are performed in units of RGB dots in 6-bit RGB interface mode.

As the following table, the optimum interface for the state of display can be selected by setting the external display interface mode.

Table 25

Display State	Operation mode	RAM access (RM)	Display mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 01)
Rewrite still picture area while display moving pictures	RGB interface (2)	System interface (RM = 0)	RGB interface (DM = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 10)

Notes:
1. Instructions are set only via the system interface.
2. The RGB-I/F and the VSYNC-I/F are not used simultaneously.
3. Do not make changes to the RGB-I/F mode setting (RIM) while the RGB I/F is in operation.
4. See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

Internal clock operation mode

All display operations are synchronized with the signals generated from the internal operating clock in this mode. None of inputs via the external display interface are valid. The internal RAM is accessible only via the system interface.

RGB interface mode (1)

In RGB interface mode, display operations are synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clock (DOTCLK). These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels via the DB[17:0] pins. All display data are stored in the internal RAM. The combined use of the high-speed RAM write mode and the widow address function enables not only displaying data in moving picture area and data in the internal RAM in other than the moving picture area at a time but also minimizing data transfer by transferring data only when rewriting screen.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated inside the LGDP4531 by internally counting the number of line synchronizing signal clocks (HSYNC) from the falling edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring RGB data via the DB[17:0] pins.

RGB interface mode (2)

The LGDP4531 enables rewriting RAM data via the system interface while the RGB interface is selected for display operation. In this case, Be sure to write RAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE bit first and then set a new address (AD[15:0]) in the AC and the index register to R22h.

VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the frame synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal RAM at more than the minimum speed from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and method. For details, see "External Display Interface".

No external signal input except VSYNC input is accepted in VSYNC interface mode.

The timings and durations of front porch (FP), back porch (BP) periods and display duration period (NL) are automatically calculated from the falling edge of the frame synchronization signal (VSYNC) according to the instructions set in the relevant registers.

Frame Maker Position (R0Dh)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	0	FMP[8:0]								

FMP[8:0] – Sets the output position of frame cycle signal (frame maker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is output at the start of back porch period for 1H period (IOVcc-IOGND amplitude signal). FMARK can be used as a trigger signal for frame synchronous write operation. See "FMARK" for details.

Make sure 9'h000 <=FMP <= BP+NL+FP

Table 26

FMP[8:0]	FMARK output position
9'h000	0th line
9'h001	1st line
9'h002	2nd line
:	:
9'h14D	333rd line
9'h14E	334th line
9'h14F	335th line

External Display Interface Control 2 (R0Fh)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

DPL – Sets the signal polarity of DOTCLK pin.

DPL = 0 : input data on the rising edge of DOTCLK
DPL = 1 : input data on the falling edge of DOTCLK

EPL – Sets the signal polarity of ENABLE pin.

EPL = 0 : writes data DB[17:0] when ENABLE = 0 and disables data write operation when ENABLE = 1.
EPL = 1 : writes data DB[17:0] when ENABLE = 1 and disables data write operation when ENABLE = 0.

HSPL – Sets the signal polarity of HSYNC pin.
HSPL = 0 : Low active
HSPL = 1 : High active

VSPL – Sets the signal polarity of VSYNC pin.
VSPL = 0 : Low active
VSPL = 1 : High active

Power Control 1 (R10h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	SAP[2:0]			BT[3:0]				0	AP[2:0]			DK	DSTB	SLP	0

SLP – When SLP = 1, the LGDP4531 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change of GRAM data or instruction is accepted in sleep mode. The GRAM data and the instruction bits remain unchanged.

DSTB – When DSTB = 1, the LGDP4531 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and the instruction bit setting are destroyed and must be reset after exiting deep standby mode.

DK – Activates DDVDH. When DK = 0, DDVDH activates at the same timing as VGH. When DK = 1, DDVDH activates separately from VGH.

Table 27

DK	Step-up Cycle in Step-up Circuit 1
1'h0	Startup DDVDH simultaneously with VGH. Startup step-up circuit 1 (VLOUT1 output) according to AP[2:0]
1'h1	Halt step-up circuit 1 (VLOUT1). (Default)

AP[2:0] – Adjusts the constant current in the operation amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0]=3'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.
Adjust the amount of fixed current from the fixed-current source in the internal operational amplifier circuit. VGH operates when AP is not 000. Complete setting AP before setting PON = 1. (While setting PON = 1, setting of AP bit cannot be changed.) For the details of sequences, refer to Flow of "Power Supply Setting".

Table 28

AP[2:0]	LCD power supply circuits	Grayscale voltage generating circuit
3'h0	Halt operation	Halt operation
3'h1	Setting disabled	Setting disabled
3'h2	Normal operation	0.5
3'h3	Normal operation	0.75
3'h4	Normal operation	1
3'h5	Normal operation	1.25
3'h6	Normal operation	1.5
3'h7	Setting disabled	Setting disabled

Note: In this table, the constant current in operational amplifiers is shown by the ratio to the constant current when AP[1:0] is set to 2'h3.

BT[3:0] – Sets the factor used in the step-up circuits. Use an optimal step-up factor for the voltage in use. To reduce power consumption, set a smaller factor.

Table 29 Step up factor and output voltage level

BT[3:0]	DDVDH	VGH	VGL	Capacitor connection Pins
4'h0			–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h1		DDVDH x 4 [x 8]	–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
4'h2			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h3	Vci1 x 2 [x 2]		–(Vci1 + DDVDH x 2) [x –5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h4		Vci1 + DDVDH x 3 [x 7]	–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±, C23±
4'h5			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±, C23±
4'h6		DDVDH x 3 [x 6]	–(DDVDH x 2) [x –4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
4'h7			–(Vci1 + DDVDH) [x –3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
4'h8~ 4'hF	Setting disabled			

Note: 1. The step-up factor from Vci1 are shown in the brackets [ ].
   2. Connect capacitors where required when using DDVDH, VGH, VGL voltages.
   3. Set the following voltages within the respective ranges:
        DDVDH = 6.0V(max.), VGH = 15.0V (max.) and VGL = -12.5V (max.)

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SAP[2:0] – Adjust the constant current for the operational amplifer circuit in the source driver. A larger constant current stabilizes the operational ampilifer circuit, but current consumption increases. Adjust the constant current taking the display quality-current consumprion trade-off into account. During a period showing no display, set SAP = 0 to halt the operational amplifier circuit to reduce current consumption.

Table 30

SAP[2:0]	Constant current (ratio to 3)
3'h0	Halt operational amplifier
3'h1	Constant current (ratio to 3) : 0.65
3'h2	Constant current (ratio to 3) : 0.8
3'h3	Constant current (ratio to 3) : 1.00
3'h4	Constant current (ratio to 3) : 1.35
3'h5	Constant current (ratio to 3) : 1.60
3'h6	Setting disabled
3'h7	Setting disabled

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC1[2:0]			0	DC0[2:0]			0	VC[2:0]		

Table 31 Step-up frequency (Step-up Circuit 1)

DC0[2:0]	Step-up circuit 1 : step-up frequency (f_{DCDC1})
3'h0	fosc/4
3'h1	fosc/8
3'h2	fosc/16
3'h3	fosc/32
3'h4	fosc/64
3'h5	fosc/2
3'h6	Halt step-up circuit 1
3'h7	fosc/1

Note : Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.

Table 32 Step-up frequency (Step-up Circuit 2)

DC1[2:0]	Step-up circuit 2 : step-up frequency (f_{DCDC2})
3'h0	fosc/64
3'h1	fosc/128
3'h2	fosc/256
3'h3	fosc/512
3'h4	fosc/1024
3'h5	fosc/32
3'h6	Halt step-up circuit 2
3'h7	fosc/16

Note : Make sure to set DC0 and DC1 to maintain $f_{DCDC1} \geq f_{DCDC2}$.

Table 33 VciOUT output level

VC[2:0]	VciOUT (Reference Voltage) (Vci1 Voltage)
3'h0	1.00 x VciLVL
3'h1	0.92 x VciLVL
3'h2	0.90 x VciLVL
3'h3	0.87 x VciLVL
3'h4	0.85 x VciLVL
3'h5	0.83 x VciLVL
3'h6	0.73 x VciLVL
3'h7	Setting disabled

Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH[3:0]			

VRH[3:0] – Sets the factor to generate VREG1OUT from VciLVL.

Table 34 VREG1OUT

VRH[3:0]	VREG1OUT Voltage
4'h0	VciOUT x 1.27
4'h1	VciOUT x 1.32
4'h2	VciOUT x 1.37
4'h3	VciOUT x 1.42
4'h4	VciOUT x 1.47
4'h5	VciOUT x 1.52
4'h6	VciOUT x 1.57
4'h7	Setting disabled
4'h8	Setting disabled
4'h9	VciOUT x 1.62
4'hA	VciOUT x 1.67
4'hB	VciOUT x 1.72
4'hC	VciOUT x 1.77
4'hD	VciOUT x 1.82
4'hE	VciOUT x 1.87
4'hF	VciOUT x 1.92

Note: Set the VC and VRH bits to maintain the VREG1OUT voltage at (DDVDH – 0.5) V or less.

PON – Controls the operation to generate VLOUT3. In setting the PON bit, follows the power-supply startup sequence.

        PON = 0 : Halts the step-up operation to generate VLOUT3.
        PON = 1 : Starts the step-up operation to generate VLOUT3.

Power Control 4 (R13h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	VCOMG		VDV[4:0]				0			VCM[6:0]				

VCM[6:0] – Sets the VcomH level (the higher voltage of Vcom alternating drive). VCM[6:0] specifies the voltage by VREG1OUT x n, where n is a discrete number from 0.400 to 0.875. To halt internal volume and adjust VcomH with an external resistor from VcomR, set VCM[6:0] = "1111111".

Table 35

VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH
7'h00	VREG1OUT x 0.400	7'h20	VREG1OUT x 0.560	7'h40	VREG1OUT x 0.720	7'h60	VREG1OUT x 0.880
7'h01	VREG1OUT x 0.405	7'h21	VREG1OUT x 0.565	7'h41	VREG1OUT x 0.725	7'h61	VREG1OUT x 0.885
7'h02	VREG1OUT x 0.410	7'h22	VREG1OUT x 0.570	7'h42	VREG1OUT x 0.730	7'h62	VREG1OUT x 0.890
7'h03	VREG1OUT x 0.415	7'h23	VREG1OUT x 0.575	7'h43	VREG1OUT x 0.735	7'h63	VREG1OUT x 0.895
7'h04	VREG1OUT x 0.420	7'h24	VREG1OUT x 0.580	7'h44	VREG1OUT x 0.740	7'h64	VREG1OUT x 0.900
7'h05	VREG1OUT x 0.425	7'h25	VREG1OUT x 0.585	7'h45	VREG1OUT x 0.745	7'h65	VREG1OUT x 0.905
7'h06	VREG1OUT x 0.430	7'h26	VREG1OUT x 0.590	7'h46	VREG1OUT x 0.750	7'h66	VREG1OUT x 0.910
7'h07	VREG1OUT x 0.435	7'h27	VREG1OUT x 0.595	7'h47	VREG1OUT x 0.755	7'h67	VREG1OUT x 0.915
7'h08	VREG1OUT x 0.440	7'h28	VREG1OUT x 0.600	7'h48	VREG1OUT x 0.760	7'h68	VREG1OUT x 0.920
7'h09	VREG1OUT x 0.445	7'h29	VREG1OUT x 0.605	7'h49	VREG1OUT x 0.765	7'h69	VREG1OUT x 0.925
7'h0A	VREG1OUT x 0.450	7'h2A	VREG1OUT x 0.610	7'h4A	VREG1OUT x 0.770	7'h6A	VREG1OUT x 0.930
7'h0B	VREG1OUT x 0.455	7'h2B	VREG1OUT x 0.615	7'h4B	VREG1OUT x 0.775	7'h6B	VREG1OUT x 0.935
7'h0C	VREG1OUT x 0.460	7'h2C	VREG1OUT x 0.620	7'h4C	VREG1OUT x 0.780	7'h6C	VREG1OUT x 0.940
7'h0D	VREG1OUT x 0.465	7'h2D	VREG1OUT x 0.625	7'h4D	VREG1OUT x 0.785	7'h6D	VREG1OUT x 0.945
7'h0E	VREG1OUT x 0.470	7'h2E	VREG1OUT x 0.630	7'h4E	VREG1OUT x 0.790	7'h6E	VREG1OUT x 0.950
7'h0F	VREG1OUT x 0.475	7'h2F	VREG1OUT x 0.635	7'h4F	VREG1OUT x 0.795	7'h6F	VREG1OUT x 0.955
7'h10	VREG1OUT x 0.480	7'h30	VREG1OUT x 0.640	7'h50	VREG1OUT x 0.800	7'h70	VREG1OUT x 0.960
7'h11	VREG1OUT x 0.485	7'h31	VREG1OUT x 0.645	7'h51	VREG1OUT x 0.805	7'h71	VREG1OUT x 0.965
7'h12	VREG1OUT x 0.490	7'h32	VREG1OUT x 0.650	7'h52	VREG1OUT x 0.810	7'h72	VREG1OUT x 0.970
7'h13	VREG1OUT x 0.495	7'h33	VREG1OUT x 0.655	7'h53	VREG1OUT x 0.815	7'h73	VREG1OUT x 0.975
7'h14	VREG1OUT x 0.500	7'h34	VREG1OUT x 0.660	7'h54	VREG1OUT x 0.820	7'h74	VREG1OUT x 0.980
7'h15	VREG1OUT x 0.505	7'h35	VREG1OUT x 0.665	7'h55	VREG1OUT x 0.825	7'h75	Setting disabled
7'h16	VREG1OUT x 0.510	7'h36	VREG1OUT x 0.670	7'h56	VREG1OUT x 0.830	7'h76	Setting disabled
7'h17	VREG1OUT x 0.515	7'h37	VREG1OUT x 0.675	7'h57	VREG1OUT x 0.835	7'h77	Setting disabled
7'h18	VREG1OUT x 0.520	7'h38	VREG1OUT x 0.680	7'h58	VREG1OUT x 0.840	7'h78	Setting disabled
7'h19	VREG1OUT x 0.525	7'h39	VREG1OUT x 0.685	7'h59	VREG1OUT x 0.845	7'h79	Setting disabled
7'h1A	VREG1OUT x 0.530	7'h3A	VREG1OUT x 0.690	7'h5A	VREG1OUT x 0.850	7'h7A	Setting disabled
7'h1B	VREG1OUT x 0.535	7'h3B	VREG1OUT x 0.695	7'h5B	VREG1OUT x 0.855	7'h7B	Setting disabled
7'h1C	VREG1OUT x 0.540	7'h3C	VREG1OUT x 0.700	7'h5C	VREG1OUT x 0.860	7'h7C	Setting disabled
7'h1D	VREG1OUT x 0.545	7'h3D	VREG1OUT x 0.705	7'h5D	VREG1OUT x 0.865	7'h7D	Setting disabled
7'h1E	VREG1OUT x 0.550	7'h3E	VREG1OUT x 0.710	7'h5E	VREG1OUT x 0.870	7'h7E	Setting disabled
7'h1F	VREG1OUT x 0.555	7'h3F	VREG1OUT x 0.715	7'h5F	VREG1OUT x 0.875	7'h7F	Halt internal volume.

Note : Set the VcomH voltage from 2.5V to (DDVDH – 0.5) V.

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VDV[4:0] – Sets the alternating amplitudes of VCOM AC voltage. These bits amplify VCOM by from 0.6 to 1.23 times the VREG1OUT voltage. If VCOMG = 0, VDV[4:0] bits are disabled.

Table 36

VDV[4:0]	Vcom amplitude	VDV[4:0]	Vcom amplitude
5'h00	VREG1OUT x 0.60	5'h10	VREG1OUT x 1.05
5'h01	VREG1OUT x 0.63	5'h11	VREG1OUT x 1.08
5'h02	VREG1OUT x 0.66	5'h12	VREG1OUT x 1.11
5'h03	VREG1OUT x 0.69	5'h13	VREG1OUT x 1.14
5'h04	VREG1OUT x 0.72	5'h14	VREG1OUT x 1.17
5'h05	VREG1OUT x 0.75	5'h15	VREG1OUT x 1.20
5'h06	VREG1OUT x 0.78	5'h16	VREG1OUT x 1.23
5'h07	VREG1OUT x 0.81	5'h17	VREG1OUT x 1.26
5'h08	VREG1OUT x 0.84	5'h18	VREG1OUT x 1.29
5'h09	VREG1OUT x 0.87	5'h19	VREG1OUT x 1.32
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.35
5'h0B	VREG1OUT x 0.93	5'h1B	VREG1OUT x 1.38
5'h0C	VREG1OUT x 0.96	5'h1C	VREG1OUT x 1.41
5'h0D	VREG1OUT x 0.99	5'h1D	VREG1OUT x 1.44
5'h0E	VREG1OUT x 1.02	5'h1E	VREG1OUT x 1.47
5'h0F	Setting disabled	5'h1F	VREG1OUT x 1.50

Note : Set the VcomH voltage from 2.5V to (DDVDH – 0.5) V.

VCOMG – When VCOMG = 1, the LGDP4531 can output a negative voltage level for VCOML (1.0 ~ -Vci + 0.5V max). When VCOMG = 0, the LGDP4531 halts the amplifier for negative voltage to save power. When VCOMG = 0, the VDV[4:0] bits are disabled. In this case, adjust the amplitude of VCOM AV voltage with VCM[4:0] bits (VCOMH setting). Set PON = 1 before setting VCOMG = 1. When VCOMG = 1, voltage of VCOML can be set to any level, and instruction (VDV) becomes valid. VCOMG = 1 is valid when PON = 1. When COMG = 0, output of VCOML if fixed to GND level, and setting of instruction (VDV) becomes invalid. When VCOMG = 0, output of VCOML and VCL stop.

Regulator Control (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RSET			0	RI[2:0]			0	RV[2:0]			0	RCONT[2:0]		

RCONT[2:0] – These bits control the input voltage of main bias op_amp.

Table 37

RCONT[2:0]	Input voltage
3'h0	Vci x 0.25
3'h1	Setting diabled
3'h2	Open
3'h3	Vci x 0.30
3'h4	Setting disabled
3'h5	Setting disabled
3'h6	Vci x 0.20
3'h7	Setting disabled

RV[2:0] – These bits control the output voltage of internal logic regulator.

Table 38

RV [2:0]	Vdd voltage
3'h0	Vci x 0.80
3'h1	Vci x 0.75
3'h2	Vci x 0.70
3'h3	Vci x 0.65
3'h4	Vci x 0.60
3'h5	Vci x 0.55
3'h6	Vci x 0.50
3'h7	Vci x 0.45

RI[2:0] – These bits control the bias current of internal logic regulator.

Table 39

RI [2:0]	Constant current
3'h0	0.2
3'h1	0.1
3'h2	2.2
3'h3	3
3'h4	3.2
3'h5	4
3'h6	5.2
3'h7	6

Note : In this table, the constant current is shown by the ratio to the constant current when RI[2:0] is set to 3'h3.

RSET[2:0] – These bits control the main bias.

IPS Control (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IPS

IPS – This bit specify the IPS mode enable signal.

Table 40

IPS	Mode
1'h0	TN mode
1'h1	IPS mode

Table 41 In TN mode

Line	N frame		N+1 frame	
	VCOM1	**VCOM2**	**VCOM1**	**VCOM2**
1	VCOML	VCOML	VCOMH	VCOMH
2	VCOMH	VCOMH	VCOML	VCOML
3	VCOML	VCOML	VCOMH	VCOMH
4	VCOMH	VCOMH	VCOML	VCOML
…	…	…	…	…
319	VCOML	VCOML	VCOMH	VCOMH
320	VCOMH	VCOMH	VCOML	VCOML

Table 42 In IPS mode

Line	N frame		N+1 frame	
	VCOM1	**VCOM2**	**VCOM1**	**VCOM2**
1	VCOML	Hi-Z	VCOMH	Hi-Z
2	Hi-Z	VCOMH	Hi-Z	VCOML
3	VCOML	Hi-Z	VCOMH	Hi-Z
4	Hi-Z	VCOMH	Hi-Z	VCOML
…	…	…	…	…
319	VCOML	Hi-Z	VCOMH	Hi-Z
320	Hi-Z	VCOMH	Hi-Z	VCOML

RAM Address Set (Horizontal Address) (R20h)

RAM Address Set (Vertical Address) (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD[7:0]							
W	1	0	0	0	0	0	0	0	AD[16:8]								

AD[16:0] – A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as data is written to the internal GRAM in order to write data consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM='1'), the address AD[16:0] is set in the address counter every frame on the falling edge of VSYNC.

Note 2: In internal clock operation and VSYNC interface operation (RM='0'), the address AD[16:0] is set when executing the instruction.

Table 43

AD[16:0]	GRAM Data Setting
17'h00000 – 17'h000EF	Bitmap data on the first line
17'h00100 – 17'h001EF	Bitmap data on the second line
17'h00200 – 17'h002EF	Bitmap data on the third line
:	:
17'h16500 – 17'h13DEF	Bitmap data on the 318th line
17'h16600 – 17'h13EEF	Bitmap data on the 319th line
17'h16700 – 17'h13FEF	Bitmap data on the 320th line

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Write Data to RAM (R22h)

R/W	RS	The bit assignment between RAM write data WD[17:0] and DB[17:0] differs according to the selected interface.
W	1	WD[17:0]

WD[17:0] – The LGDP4531 write data to the internal GRAM by expanding into 18 bits internally. The data expansion fomat into 18 bits differs according to the interface.

The GRAM data represents the grayscale level. The LGDP4531 automatically updates the address according to AM and I/D[1:0] as it writes data in the GRAM. In standby mode, the GRAM is not accessible. The data in 16-bit format is developed into 18 bits according to the register setting (DFM) in 8-/16-bit interface operation.

Note : When writing data in the GRAM via system interface while using the RGB interface, make sure that write operation via two interface do not conflict.

Table 44 GRAM data and corresponding LCD Grayscale level (REV = 1)

GRAM data RGB	Grayscale level		GRAM data RGB	Grayscale level	
	Netative	Positive		Netative	Positive
6'h00	V63	V0	6'h20	V31	V32
6'h01	V62	V1	6'h21	V30	V33
6'h02	V61	V2	6'h22	V29	V34
6'h03	V60	V3	6'h23	V28	V35
6'h04	V59	V4	6'h24	V27	V36
6'h05	V58	V5	6'h25	V26	V37
6'h06	V57	V6	6'h26	V25	V38
6'h07	V56	V7	6'h27	V24	V39
6'h08	V55	V8	6'h28	V23	V40
6'h09	V54	V9	6'h29	V22	V41
6'h0A	V53	V10	6'h2A	V21	V42
6'h0B	V52	V11	6'h2B	V20	V43
6'h0C	V51	V12	6'h2C	V19	V44
6'h0D	V50	V13	6'h2D	V18	V45
6'h0E	V49	V14	6'h2E	V17	V46
6'h0F	V48	V15	6'h2F	V16	V47
6'h10	V47	V16	6'h30	V15	V48
6'h11	V46	V17	6'h31	V14	V49
6'h12	V45	V18	6'h32	V13	V50
6'h13	V44	V19	6'h33	V12	V51
6'h14	V43	V20	6'h34	V11	V52
6'h15	V42	V21	6'h35	V10	V53
6'h16	V41	V22	6'h36	V9	V54
6'h17	V40	V23	6'h37	V8	V55
6'h18	V39	V24	6'h38	V7	V56
6'h19	V38	V25	6'h39	V6	V57
6'h1A	V37	V26	6'h3A	V5	V58
6'h1B	V36	V27	6'h3B	V4	V59
6'h1C	V35	V28	6'h3C	V3	V60
6'h1D	V34	V29	6'h3D	V2	V61
6'h1E	V33	V30	6'h3E	V1	V62
6'h1F	V32	V31	6'h3F	V0	V63

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Table 45 GRAM data and corresponding LCD Grayscale level (REV = 0)

GRAM data RGB	Grayscale level		GRAM data RGB	Grayscale level	
	Netative	**Positive**		**Netative**	**Positive**
6'h00	V0	V63	6'h20	V32	V31
6'h01	V1	V62	6'h21	V33	V30
6'h02	V2	V61	6'h22	V34	V29
6'h03	V3	V60	6'h23	V35	V28
6'h04	V4	V59	6'h24	V36	V27
6'h05	V5	V58	6'h25	V37	V26
6'h06	V6	V57	6'h26	V38	V25
6'h07	V7	V56	6'h27	V39	V24
6'h08	V8	V55	6'h28	V40	V23
6'h09	V9	V54	6'h29	V41	V22
6'h0A	V10	V53	6'h2A	V42	V21
6'h0B	V11	V52	6'h2B	V43	V20
6'h0C	V12	V51	6'h2C	V44	V19
6'h0D	V13	V50	6'h2D	V45	V18
6'h0E	V14	V49	6'h2E	V46	V17
6'h0F	V15	V48	6'h2F	V47	V16
6'h10	V16	V47	6'h30	V48	V15
6'h11	V17	V46	6'h31	V49	V14
6'h12	V18	V45	6'h32	V50	V13
6'h13	V19	V44	6'h33	V51	V12
6'h14	V20	V43	6'h34	V52	V11
6'h15	V21	V42	6'h35	V53	V10
6'h16	V22	V41	6'h36	V54	V9
6'h17	V23	V40	6'h37	V55	V8
6'h18	V24	V39	6'h38	V56	V7
6'h19	V25	V38	6'h39	V57	V6
6'h1A	V26	V37	6'h3A	V58	V5
6'h1B	V27	V36	6'h3B	V59	V4
6'h1C	V28	V35	6'h3C	V60	V3
6'h1D	V29	V34	6'h3D	V61	V2
6'h1E	V30	V33	6'h3E	V62	V1
6'h1F	V31	V32	6'h3F	V63	V0

Read Data from RAM (R22h)

R/W	RS	The bit assignment between RAM write data RD[17:0] and DB[17:0] differs according to the selected interface.
R	1	RD[17:0]

RD[17:0] – 18-bit data read from the GRAM. The bit assignment between RD[17:0] and DB[17:0] (data on the data bus) differs according to the selected interface.

When the LGDP4531 read data from the GRAM to the microcomputer, the first word read immediately after RAM address set is taken in the intenal read-data latch and inbalid data is sent to the data bus DB[17:0]. Vaild data is sent to the data bus as the LGDP4531 reads out the second and subsequence words.

When either 8-bit or 16-bit interface is selected, the LSB of R and B dot data are not read out.

Note : This register is not available in RGB interface operation.

Figure 12

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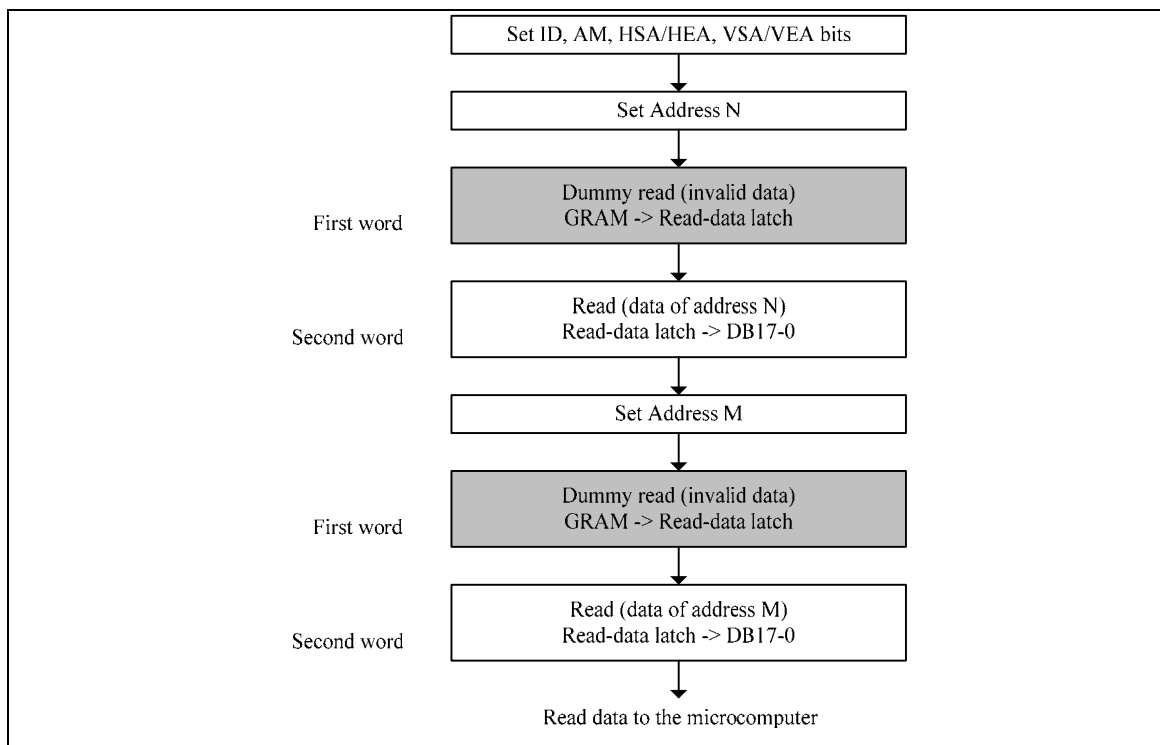
Gamma Control 1-10 (R30h to R39h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	0	VRP0[3:0]			
W	1	0	0	0	VRN1[4:0]					0	0	0	0	VRN0[3:0]			

PKP5-0[2 :0] – γ fine-adjustment register for positive polarity
PRP1-0[2 :0] – γ gradient-adjustment register for positive polarity
VRP0[3:0],VRP1[4 :0] – γ amplitude-adjustment register for positive polarity

PKN5-0[2 :0] – γ fine-adjustment register for negative polarity
PRN1-0[2 :0] – γ gradient-adjustment register for negative polarity
VRN0[3:0], VRN1[4 :0] – γ amplitude-adjustment register for negative polarity

EPROM Control Register 1 (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	POR	VPP	PPROG	PWE	PA[1:0]		0	PDIN[6:0]						

EPROM programming control. See "EPROM Control" section.

PDIN[6:0] – Data input. This corresponds to VCM[6:0] bits of R13h.

PA[1:0] – address input. This selects one of four banks of the EPROM.

Table 46

PA[1:0]	Write Data Input	Write OPT Cell
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

PWE – Write enable.

PPROG – Program mode enable.

VPP – Power switch control for the VPP pin of the embedded EPROM. When VPP = "1", the internal VPP is set to 7.2V; otherwise it is set to 1.8V.

POR – Pin for power-on rest.

EPROM Control Register 2 (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0											RA[1:0]		VCMSEL[1:0]	

EPROM programming control. See "EPROM Control" section.

VCMSEL[1:0] – With VCMSEL pin, sets VcomH level from either the register R13h or the EPROM

Table 47

VCMSEL[1:0]	VCMSEL pin	VcomH Level adjustment
00	X	VCM[6:0] of the register R13h
01	X	EPROM data selected by RA[1:0]
1X	0	VCM[6:0] of the register R13h
1X	1	EPROM data selected by RA[1:0]

RA[1:0] – Read address input. This selects one of four banks of the EPROM.

EPROM Control Register 3 (R42h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0								PDOUT[6:0]						

PDOUT[6:0] – EPROM Read Data output.

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Window Horizontal RAM Address Start/End (R50h/R51h)

Window Vertical RAM Address Start/End (R52h/R53h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	0	0				HSA[7:0]				
W	1		0	0	0	0	0	0	0	0				HEA[7:0]				
W	1		0	0	0	0	0	0	0					VSA[8:0]				
W	1		0	0	0	0	0	0	0					VEA[8:0]				

HSA[7:0]/HEA[7:0] – HSA[7:0] and HEA[7:0] represent the addresses at the start and end of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the range on the GRAM to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HSA < HEA ≤ 8'hEF.

VSA[8:0]/VEA[8:0] – VSA[8:0] and VEA[8:0] represent the addresses at the start and end of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the range on the GRAM to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.

Figure 13

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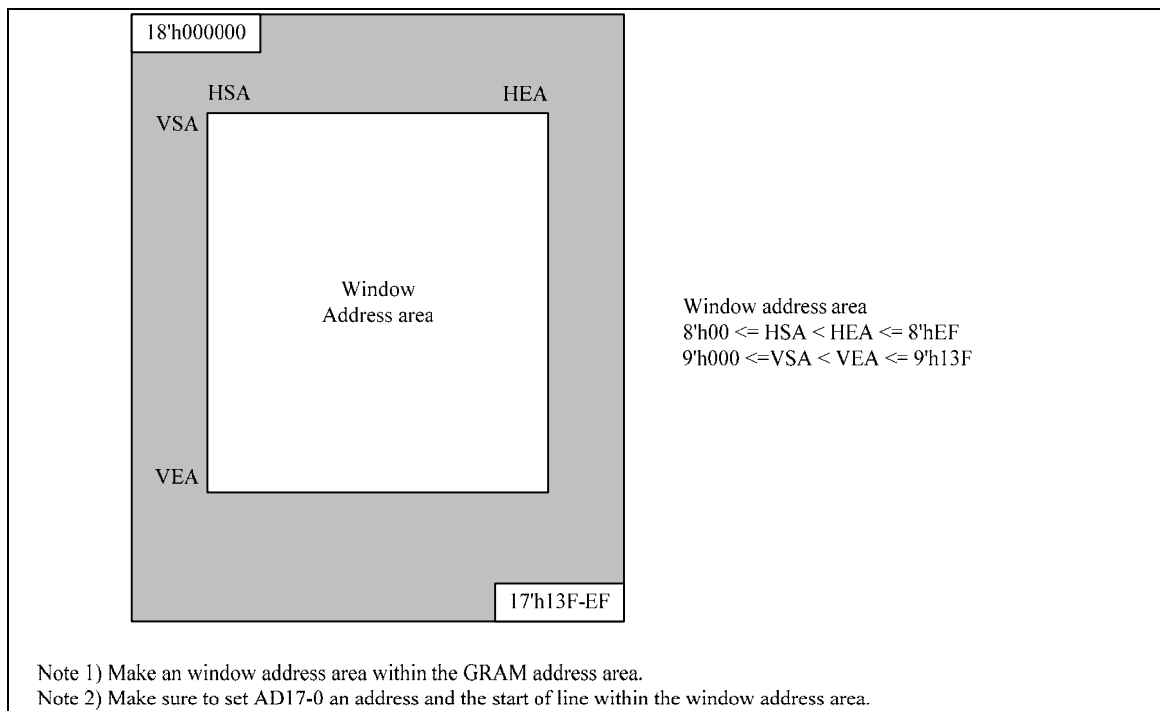
Driver Output Control (R60h)

Base Image Display Control (R61h)

Vertical Scroll Control (R6Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GS	0			NL[5:0]				0	0			SCN[5:0]			
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
W	1	0	0	0	0	0	0	0				VL[8:0]					

SCN[5:0] – Specifies the gate line where the gate driver starts scan.

NL[5:0] – Sets the number of lines to drive the LCD at an interval of 8lines. The GRAM address mapping is not affected by the number of lines set with NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 48

NL[5:0]	Number of Lines
6'h00 – 6'h1C	Setting disabled
6'h1D	240 (lines)
6'h1E	248
6'h1F	256
6'h20	264
6'h21	272
6'h22	280
6'h23	288
6'h24	296
6'h25	304
6'h26	312
6'h27	320
6'h28 – 6'h3F	Setting disabled

GS – Set the direction of scan by the gate driver. Set the GS bit in combination with SM and SS bits to optimize scan method to the LCD module.

REV – The grayscale level corresponding to the GRAM data can be reversed by setting REV = 1. This enables the LGDP4531 to display the same image form a same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by resiger setting (PTS).

Table 49

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	**Negative Polarity**
0	18'h00000 : 18'h3FFFF	V63 : V0	V0 : V63
1	18'h00000 : 18'h3FFFF	V0 : V63	V63 : V0

VLE – Vertical scroll display enable bit. When VLE = 1, the LGDP4531 starts displaying the base image from the line (of the physical display) determined by setting the VL[8:0] bits. VL[8:0] represents the number of lines shifted from the first line of the physical display (the amount of scrolling). Note that the display position of partial image is not affected by the base image scrolling.

The vertical scrolling is not available in external display inteface opration. In this case, make sure to set VLE = 0.

NDL – Sets the source output level in non-display lit driving periods. By setting the NDL bit, the non-display area can be kept lit on.

Table 50

NDL	Non-display area	
	Positive	**Negative**
0	V63	V0
1	V0	V63

VL[8:0] – Sets the amount of scrolling the base image by the number of lines. The RAM data in the start line address is displayed on the line, which is shifted from the first line of the liquid crystal panel by the number of lines set with VL[8:0]. In setting VL[8:0], make sure VL ≤ 320.

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Table 51

| SCN[5:0] | Gate line No (Scan start position) | | | |
| | SM = 0 | | SM = 1 | |
	GS = 0	GS = 1	GS = 0	GS = 1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28 – 6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

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Partial Image 1: Display Position (R80h)

RAM Address (Start/End Line Address) (R81h/R82h)

Partial Image 2: Display Position (R83h)

RAM Address (Start/End Line Address) (R84h/R85h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0				PTDP0[8:0]					
W	1	0	0	0	0	0	0	0				PTSA0[8:0]					
W	1	0	0	0	0	0	0	0				PTEA0[8:0]					
W	1	0	0	0	0	0	0	0				PTDP1[8:0]					
W	1	0	0	0	0	0	0	0				PTSA1[8:0]					
W	1	0	0	0	0	0	0	0				PTEA1[8:0]					

PTDP0[8:0] – Sets the display position of partial image 1.
PTDP1[8:0] – Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting make sure that

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display position : (PTDP0, PTEA0)
Coordinates of partial image 2 display position : (PTDP1, PTEA1)

If PTDP0 = 9'h000, the partial image 1 is displayed from the first line of the base image.

PTSA0[8:0] – Sets the start line addresses of the RAM area, respectively for the partial image 1

PTEA0[8:0] – Sets the end display position of partial image 1.

PTSA1[8:0] – Sets the start line addresses of the RAM area, respectively for the partial image 2.

PTEA1[8:0] – Sets the end display position of partial image 2.

Panel Interface Control 1 (R90h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	DIVI[1:0]		0	0	0	RTNI[4:0]				

RTNI[4:0] – Sets 1H (line) period. This setting is enabled while the LGDP4531's display operation is synchronized with internal clock.

DIVI[1:0] – Sets the division ratio of the internal clock frequency. The LGDP4531's internal operation is synchronized with the frequency divided internal clock. When changing the DIVI[1:0] bits, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame-Frequency Adjustment Function". The setting in DIVI[1:0] is disabled in RGB interface operation.

Frame Frequency Calculation

Frame frequency = fosc/(clock cycles per line x division ratio x (active line + BP + FP))

Table 52 clocks per line (internal clock operation 1 clock = 1 OSC)

RTNI[4:0]	Clock per Line
5'h00 – 5'h0F	Setting disabled
5'h10	64 clocks
5'h11	68 clocks
5'h12	72 clocks
5'h13	76 clocks
5'h14	80 clocks
5'h15	84 clocks
5'h16	88 clocks
5'h17	92 clocks
5'h18	96 clocks
5'h19	100 clocks
5'h1A	104 clocks
5'h1B	108 clocks
5'h1C	112 clocks
5'h1D	116 clocks
5'h1E	120 clocks
5'h1F	124 clocks

Table 53 Division ratio of the internal clock

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

Panel Interface Control 2 (R92h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	NOWI[2:0]			0	0	0	0	EQI2[1:0]		EQI1[1:0]	

EQI1[1:0] – Sets equalization period.

Note : when VCOML >= 0V, EQI1,EQI2 setting is diaabled.

Table 54

EQI1[1:0]	Equalization period
2'h0	0 (internal clock period [see note])
2'h1	2
2'h2	4
2'h3	6

EQI2[1:0] – Sets equalization period.

Table 55

EQI2[1:0]	Equalization period
2'h0	0 (internal clock period [see note])
2'h1	2
2'h2	4
2'h3	6

NOWI[2:0] – Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation in synchronization with internal clock.
:

Table 56

NOWI[2:0]	Non-overlap period
3'h0	0 (internal clock period [see note])
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note : The internal clock is the frequency divided clock with the division ratio set with the DIVI[1:0] bits.

Panel Interface Control 3 (R93h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	0	0	0	0	0	0	0		MCPI[2:0]	

MCPI[2:0] – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation in synchronization with internal clock.

Table 57

MCPI[2:0]	Source output position
3'h0	0 (internal clock period [see note])
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note: The internal clock is the frequency divided clock with the division ratio set with the DIVI[[1:0] bits. The source output position is measured from a reference point by the number of internal clock cycle.

Panel Interface Control 4 (R95h)

R/W	RS		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1		0	0	0	0	0	0	DIVE[1:0]		0	0			RTNE[5:0]			

RTNE[5:0] – Sets the number of internal clocks per 1H (line) period. Set the value that represents the number of DOTCLKs divided by the division ratio, which is input in a 1H period.

DIVE[1:0] – Sets DIVE, the internal division ratio of DOTCLK. The internal operation is performed according to the clocks divided by the internal division ratio DIVE.

Table 58 Division ratio of DOTCLK

DIVE[1:0]	Division Ratio	Internal operation clock unit (DOTCLK)			
		18-bit, 1 transfer RGB interface DOTCLK = 5 MHz		8-bit, 3 transfer RGB interface DOTCLK = 15 MHz	
2'h0	Setting disabled	Setting disabled	-	Setting disabled	-
2'h1	1/1	1 DOTCLKs	0.2 μs	3 DOTCLKs	0.2 μs
2'h2	1/2	2 DOTCLKs	0.4 μs	6 DOTCLKs	0.4 μs
2'h3	1/4	4 DOTCLKs	0.8 μs	12 DOTCLKs	0.8 μs

Table 59 DOTCLK per line (1H period)

RTNE[5:0]	DOTCLK per line (1H)	RTNE[5:0]	DOTCLK per line (1H)
6'h00	Setting disabled	6'h20	128 clocks
6'h01	Setting disabled	6'h21	132 clocks
6'h02	Setting disabled	6'h22	136 clocks
6'h03	Setting disabled	6'h23	140 clocks
6'h04	Setting disabled	6'h24	144 clocks
6'h05	Setting disabled	6'h25	148 clocks
6'h06	Setting disabled	6'h26	152 clocks
6'h07	Setting disabled	6'h27	156 clocks
6'h08	Setting disabled	6'h28	160 clocks
6'h09	Setting disabled	6'h29	164 clocks
6'h0A	Setting disabled	6'h2A	168 clocks
6'h0B	Setting disabled	6'h2B	172 clocks
6'h0C	Setting disabled	6'h2C	176 clocks
6'h0E	Setting disabled	6'h2E	180 clocks
6'h0E	Setting disabled	6'h2E	184 clocks
6'h0F	Setting disabled	6'h2F	188 clocks
6'h10	64 clocks	6'h30	192 clocks
6'h11	68 clocks	6'h31	196 clocks
6'h12	72 clocks	6'h32	200 clocks
6'h13	76 clocks	6'h33	204 clocks
6'h14	80 clocks	6'h34	208 clocks
6'h15	84 clocks	6'h35	212 clocks
6'h16	88 clocks	6'h36	216 clocks
6'h17	92 clocks	6'h37	220 clocks
6'h18	96 clocks	6'h38	224 clocks
6'h19	100 clocks	6'h39	228 clocks
6'h1A	104 clocks	6'h3A	232 clocks
6'h1B	108 clocks	6'h3B	236 clocks
6'h1C	112 clocks	6'h3C	240 clocks
6'h1E	116 clocks	6'h3E	244 clocks
6'h1E	120 clocks	6'h3E	248 clocks
6'h1F	124 clocks	6'h3F	252 clocks

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Panel Interface Control 5 (R97h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0		NOWE[3:0]			0	0	0	0	EQE2[1:0]		EQE1[1:0]	

EQE1[1:0] – Sets equalization period.

Note : when VCOML >= 0V, EQE1,EQE2 setting is disabled.

Table 60

EQE1[1:0]	Equalization period
2'h0	0 (internal clock period [see note])
2'h1	8
2'h2	16
2'h3	24

EQE2[1:0] – Sets equalization period.

Table 61

EQE2[1:0]	Equalization period
2'h0	0 (internal clock period [see note])
2'h1	8
2'h2	16
2'h3	24

NOWE[3:0] – Sets the non-overlap period of adjacent gate outputs. The settint is enabled in display operation via RGB interface.

Table 62

NOWE[3:0]	Non-overlap period	NOWE[3:0]	Non-overlap period
4'h0	0 (internal clock period [see note])	4'h8	32
4'h1	4	4'h9	36
4'h2	8	4'hA	40
4'h3	12	4'hB	44
4'h4	16	4'hC	48
4'h5	20	4'hD	52
4'h6	24	4'hE	56
4'h7	28	4'hF	60

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

Panel Interface Control 6 (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2:0]		

MCPE[2:0] – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation via RGB interface.

Table 63

MCPE[2:0]	Source output position
3'h0	0 (internal clock period [see note])
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

Test Register 1 (RA0h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	TDFN	0	0	0	TOSC	0	0	TVCOM[1:0]	

TVCOM[1:0] – Sets the Vcom output level for test.

Table 64

TVCOM [1:0]	Vcom Level
2'h0	modulation
2'h1	modulation
2'h2	VCOML
2'h3	VCOMH

TOSC – Sets for the oscillator test.

TDFN – Sets for the function test.

Test Register 2 (RA1h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	G_TSD[1:0]		0	0	TSHZ	TSD_EN	0	0	TSD[1:0]	

TSD[1:0] – Sets

TSD_EN – Sets

TSHZ – Sets

G_TSD – Sets

Test Register 3 (RA2h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	T8CL	0	0	0	FRC	0	0	0	0	0	HaltVreg	MultiVci	DLYEN

DLYEN – Used for Device Test.

MultiVci – Used for Device Test.

HaltVreg – Used for Device Test.

FRC – Used for FRC mode test

T8CL – Used for 8 color mode test

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Instruction List

Index	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	Start oscillation																1
01h	Driver output control 1						SM (0)		SS (0)								
02h	LCD Driving Wave Control							BC0 (0)	EOR (0)			NW[5:0] (000000)					
03h	Entry mode	TRI (0)	DFM (0)		BGR (0)					ORG (0)		ID[1:0] (11)		AM (0)			
04h	Resizing Control							RCV[1:0] (00)				RCH[1:0] (00)				RSZ[1:0] (00)	
07h	Display Control 1			PTDE[1:0] (00)					BASEE (0)			GON (0)	DTE (0)	COL (0)		D[1:0] (00)	
08h	Display Control 2					FP[3:0] (1000)								BP[3:0] (1000)			
09h	Display Control 3						PTS[2:0] (000)					PTG[1:0] (00)		ISC[3:0] (0000)			
0Ah	Display Control 4													FMARKOE (0)	FMI[2:0] (000)		
0Ch	External display Interface Control 1			ENC[1:0] (000)					RM (0)			DM[1:0] (00)				RIM[1:0] (00)	
0Dh	Frame Marker Position								FMP[8:0] (000000000)								
0Fh	External display Interface Control 2											VSPL (0)	HSPL (0)			EPL (0)	DPL (0)
10h	Power Control 1			SAP[2:0] (000)			BT[3:0] (0000)					AP[2:0] (000)	DK (1)		DSTB (0)	SLP (0)	
11h	Power Control 2					DC1[2:0] (110)						DC0[2:0] (110)		VC[2:0] (000)			
12h	Power Control 3											PON (0)	VRH[3:0] (0000)				
13h	Power Control 4			VCOMG (0)		VDV[4:0] (00000)						VCM[6:0] (0000000)					
15h	Regulator Control			RSET[2:0] (000)			RI[2:0] (000)					RV[2:0] (011)		RCONT (000)			
16h	IPS Control																IPS (0)
20h	RAM Address Set (Horizontal Address)								AD[7:0] (00000000)								
21h	RAM Address Set (Vertical Address)								AD[16:8] (000000000)								
22h	RAM Data							WD[17:0] or RD[17:0]									
30h	Gamma Control 1						PKP1[2:0] (000)							PKP0[2:0] (000)			
31h	Gamma Control 2						PKP3[2:0] (000)							PKP2[2:0] (000)			
32h	Gamma Control 3						PKP5[2:0] (000)							PKP4[2:0] (000)			
33h	Gamma Control 4						PRP1[2:0] (000)							PRP0[2:0] (000)			
34h	Gamma Control 5						PKN1[2:0] (000)							PKN0[2:0] (000)			
35h	Gamma Control 6						PKN3[2:0] (000)							PKN2[2:0] (000)			
36h	Gamma Control 7						PKN5[2:0] (000)							PKN4[2:0] (000)			
37h	Gamma Control 8						PRN1[2:0] (000)							PRN0[2:0] (000)			
38h	Gamma Control 9					VRP1[4:0]								VRP0[3:0]			
39h	Gamma Control 10					VRN1[4:0]								VRN0[3:0]			
40h	EPROM Control 1			POR (0)	VPP (0)	PPROG (0)	PWE (0)	PA[1:0] (00)				PDIN[6:0] (0000000)					
41h	EPROM Control 2											RA[1:0] (00)		VCMSEL[1:0] (00)			
42h	EPROM Control 3											PDOUT[6:0] (0000000)					
50h	Window Horizontal RAM Start Address								HSA[7:0] (00000000)								
51h	Window Horizontal RAM End Address								HEA[7:0] (11101111)								
52h	Window Vertical RAM Start Address								VSA[8:0] (000000000)								
53h	Window Vertical RAM End Address								VEA[8:0] (100111111)								

Addr	Register	Bit fields
60h	Driver Output Control 2	GS (0); NL[5:0] (000000); SCN[5:0] (000000)
61h	Base Image Display Control	NDL (0); VLE (0); REV (0)
6Ah	Vertical Scroll Control	VL[8:0] (000000000)
80h	Partial Image 1 Display Position	PTDP0[8:0] (000000000)
81h	Partial Image 1 RAM Start Line Address	PTSA0[8:0] (000000000)
82h	Partial Image 1 RAM End Line Address	PTEA0[8:0] (000000000)
83h	Partial Image 2 Display Position	PTDP1[8:0] (000000000)
84h	Partial Image 2 RAM Start Line Address	PTSA1[8:0] (000000000)
85h	Partial Image 2 RAM End Line Address	PTEA1[8:0] (000000000)
90h	Panel Interface Control 1	DIVI[1:0] (00); RTNI[4:0] (00000)
92h	Panel Interface Control 2	NOWI[2:0] (000); EQI2[1:0] (00); EQI1[1:0] (00)
93h	Panel Interface Control 3	MCPI[2:0] (000)
95h	Panel Interface Control 4	DIVE[1:0] (00); RTNE[5:0] (000000)
97h	Panel Interface Control 5	NOWE[3:0] (0000); EQE2[1:0] (00); EQE1[1:0] (00)
98h	Panel Interface Control 6	MCPE[2:0] (000)
A0h	Test register 1	TDFN (0); TOSC (0); TVCOM[1:0] (00)
A1h	Test register 2	G_TSD[1:0] (00); TSHZ (0); TSD_EN (0); TSD[1:0] (00)
A2h	Test register 3	T8CL (0); FRC (0); HaltVreg (0); MultiVci (1); DLYEN (0)

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Reset Function

The LGDP4531 is initialized with a RESET input. During a reset period, the LGDP4531 is in a busy state and neither instruction nor access to the GRAM data from the MPU is accepted. The LGDP4531's internal power supply circuit unit is initialized also with a RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, neither access to the internal GRAM nor initial setting of instruction bits is accepted.

1. Initial state of instruction bits (default)
See the instruction list. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization
The RAM data is not automatically initialized with a RESET input and must be initialized by software in a display-off period (D1-0 = "00").

3. Output pin initial state *[See note]
1. LCD driver S1~S720   : GND
          G1~G320 : VGL (= GND)
2. Vcom   : GND
3. VcomDC   : GND
4. VRS   : GND
5. VCS   : GND
6. VREG1OUT   : VGS
7. VciOUT   : Hi-z
8. VLOUT1   : Vci
9. VLOUT2   : DDVDH (= Vci)
10. VLOUT3   : GND
11. FMARK   : GND
12. Oscillator   : Oscillate
13. SDO   : GND

4. Initial state of input/output pins*[See note]
1. C11+   : Hi-z
2. C11-   : Hi-z
3. C12+   : Hi-z
4. C12-   : Hi-z
5. C13+   : Vci1
6. C13-   : GND
7. C21+   : DDVDH (= Vci)
8. C21-   : GND
9. C22+   : DDVDH (= Vci)
10. C22-   : GND
11. C23+   : DDVDH (= Vci)
12. C23-   : GND
13. VDD   : VDD

Note: The above-mentioned initial states of output and input pins are the ones when the LGDP4531's power supply circuit is connected as exemplified in "Wiring example".

5. Note on Reset function
  (1) When a RESET input is entered into the LGDP4531 while it is in deep standby mode, the LGDP4531 starts up the inside logic regulator and makes a transition to the initial state. During this period, the interface pins may be under an unstable condition. For this reason, do not enter a RESET input in deep standby mode.

  (2) When transferring instruction using either two or three transfer mode via 8-/9-/16-bit interface, make sure to execute a data transfer synchronization after executing a reset operation.

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Basic Mode operation of the LGDP4531

The basic operation modes of the LGDP4531 are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

Figure 14

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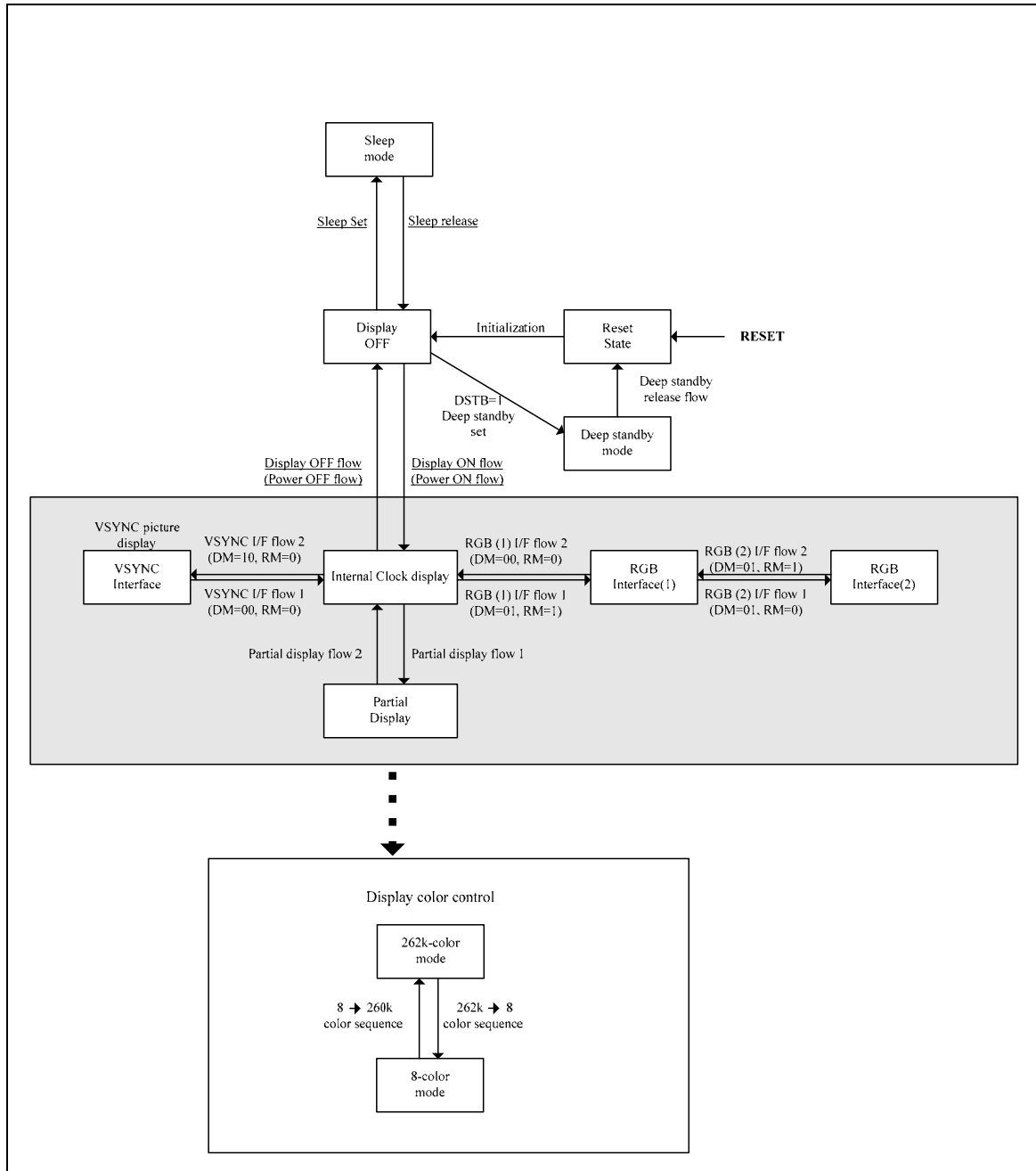
Interface and data format

The LGDP4531 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The LGDP4531 allows selecting an optimum interface according to the kind of display (moving or still picture) in order to transfer data efficiently.

As external display interface, the LGDP4531 supports RGB interface and VSYNC interface, both enabling data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the LGDP4531 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the LGDP4531's GRAM in order to minimize the data transfer by transferring data only when it is necessary to switch the moving picture frames. The window address function specifies the RAM area where data is rewritten for moving picture display and enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display using system interface by writing data to the GRAM at more than a certain speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in speed and methods of writing data to the internal RAM.

The LGDP4531 can operate in either one of the following four modes according to the state of display. The display operation mode is determined by setting the external interface control register. When switching between different modes, make sure to refer to mode switching sequence.

Table 65

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM[1:0]) while RGB interface is in operation.
4. See the "External Display Interface" section for the mode transition sequence.
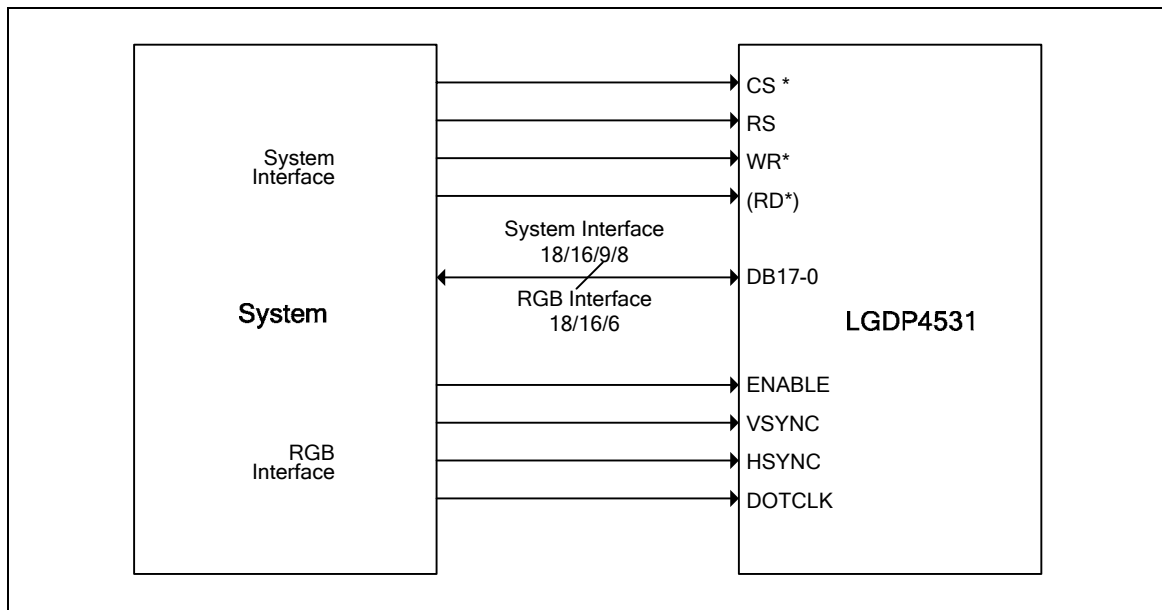
Figure 15 LGDP4531's Interface

Internal clock operation
The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. Any input via external display interface is invalid in this operation. The internal RAM is accessible only via system interface.

RGB interface operation (1)
The display operation is synchronized with the frame synchronous signal (VSYNC), the line synchronous signal (HSYNC), and the dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied throughout the display period using RGB interface.

The LGDP4531 transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function enables the LGDP4531 to display a moving picture and the data in other than the moving picture RAM area simultaneously and transferring only data to be overwritten in the moving picture RAM area when7 rewriting the moving picture RAM area. This structure can minimize the total number of data transfer.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the LGDP4531 by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with these settings.

RGB interface operation (2)
This mode enables the LGDP4531 to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first and then set a new address and the index register to R22h.

VSYNC interface operation
The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the LGDP4531 to display a moving picture using system interface by writing data to the internal RAM at more than a minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are constraints in speed and methods of writing RAM data. For

details, see the "VSYNC Interface" section. As an external input, only VSYNC signal input is valid in this mode. Any other input via external display interface is invalid.
The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) according to the register settings inside the LGDP4531.

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System Interface

The following are the kinds of system interfaces available with the LGDP4531. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 66

IM[3:0]	Interface Mode with MPU	DB pins	Colors
0000	Setting disabled	-	-
0001	Setting disabled	-	-
0010	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note 1
0011	80-system 8-bit interface	DB17-10	262,144 *see Note 2
010*	Clock synchronous serial interface	SDI,SDO	65,536
0110	Setting disabled	-	-
0111	Setting disabled	-	-
1000	Setting disabled	-	-
1001	Setting disabled	-	-
1010	80-system 18-bit interface	DB17-0	262,144
1011	80-system 9-bit interface	DB17-9	262,144
1100	Setting disabled	-	-
1101	Setting disabled	-	-
1110	Setting disabled	-	-
1111	Setting disabled	-	-

Notes: 1. 65,536 colors in 16-bit signal transfer mode.
             2. 65,536 colors in 8-bit 2-transfer mode.

80-system 18-bit Bus Interface
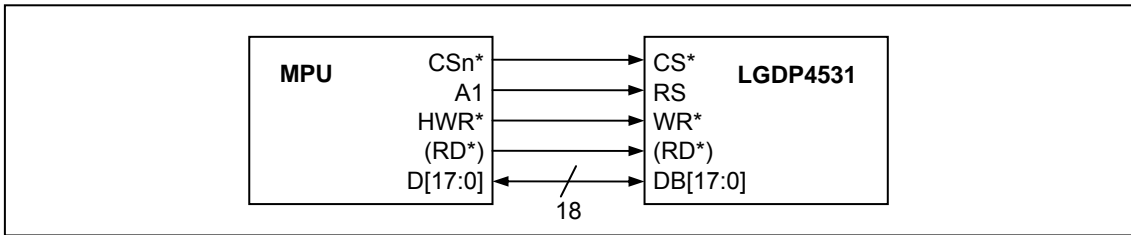
Figure 16 18-bit Interface
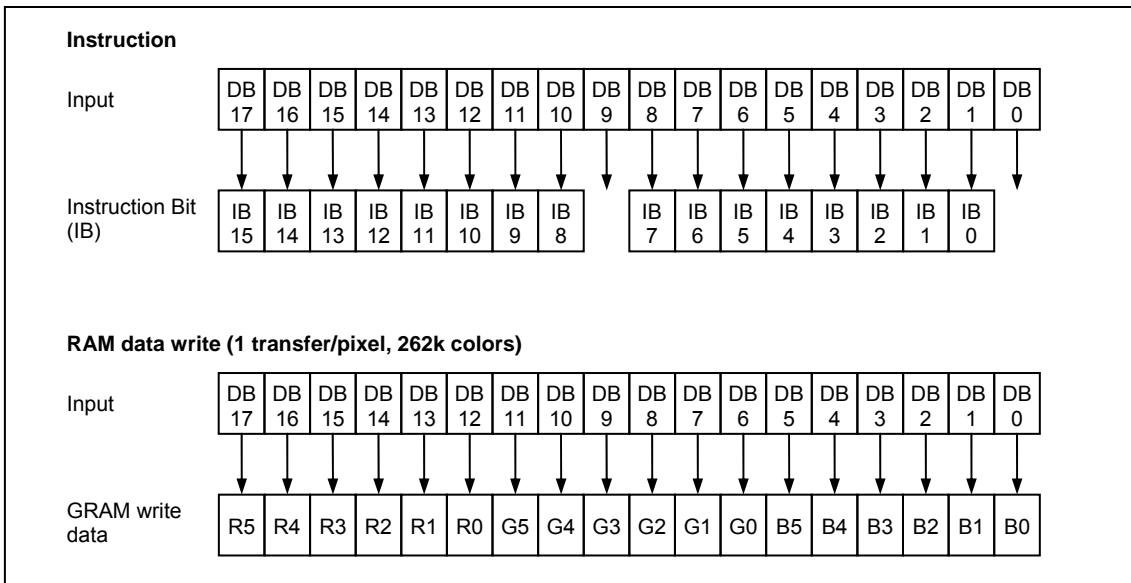
Figure 17 Data format for 18-bit interface

80-system 16-bit Bus Interface
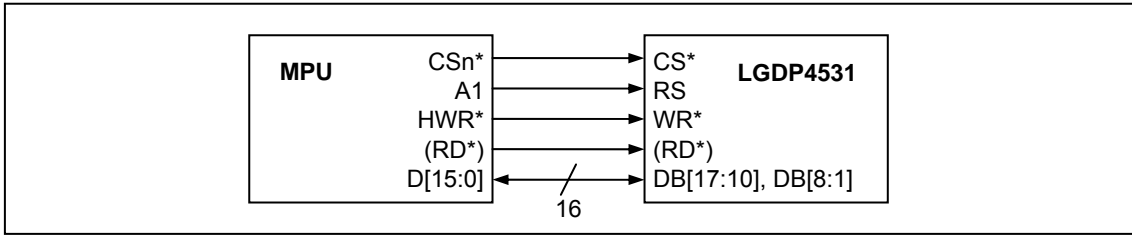
Figure 18 16-bit Interface
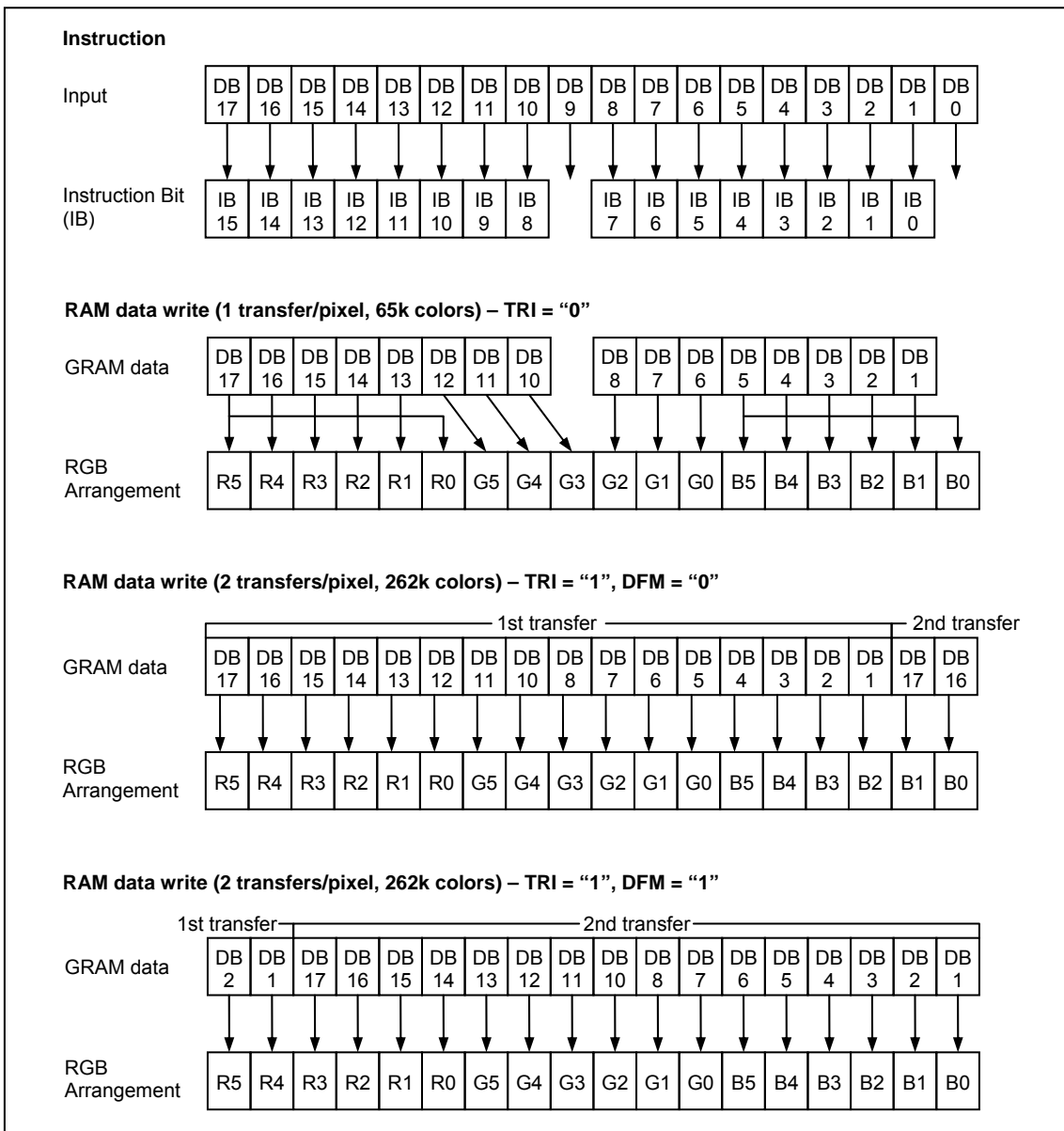
Figure 19 Data format for 16-bit interface

LG Electronics

Data Transfer Synchronous in 16-bit Bus Interface operation

The LGDP4531 supports a data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 2/16 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.
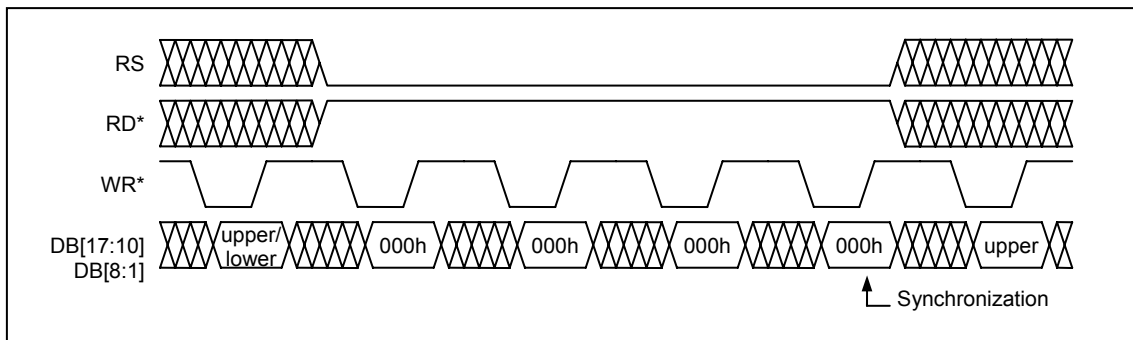
Figure 20 16-bit Data Transfer Synchronization

LG Electronics

80-system 9-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into the upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing to the index register, the upper byte (8 bits) must be written.
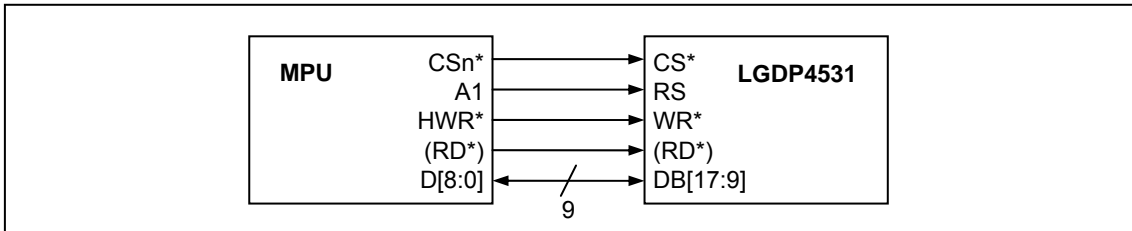
Figure 21 9-bit Interface
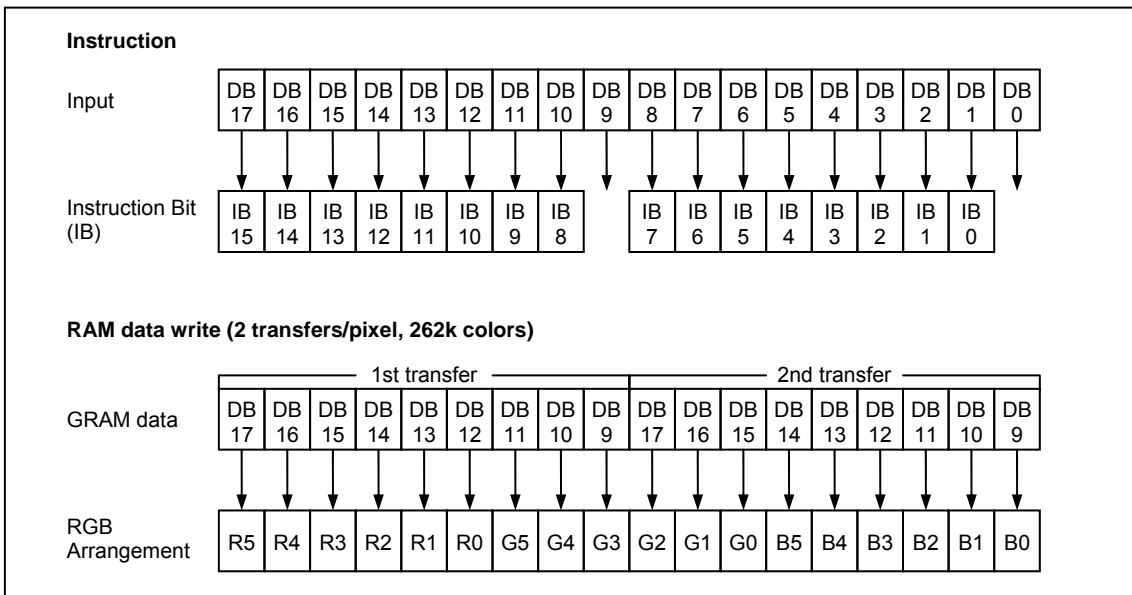
Figure 22 9-bit Interface Data Format

LG Electronics

Data Transfer Synchronous in 9-bit Bus Interface operation

The LGDP4531 supports a data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 9 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.
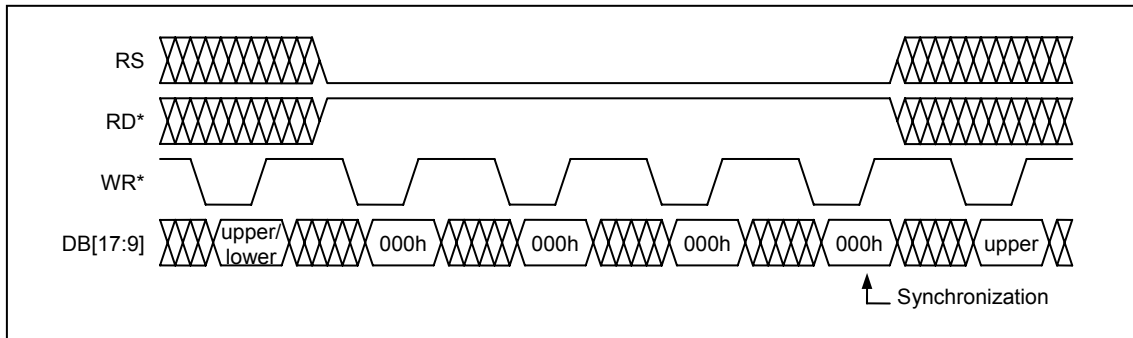
Figure 23 9-bit Data Transfer Synchronization

LG Electronics

80-system 8-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing the index register, the upper byte (8 bits) must be written.
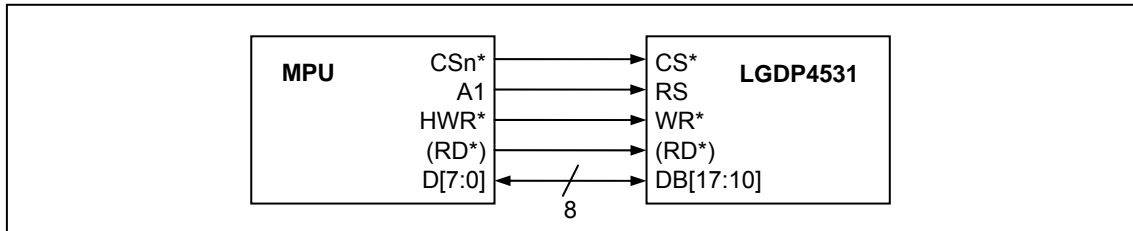
Figure 24 8-bit Interface

LG Electronics

Instruction

Input

DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0

Instruction Bit (IB)

IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8		IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

RAM data write (2 transfers/pixel, 65k colors) – TRI = "0"

GRAM data

	1st transfer									2nd transfer						
DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10		DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10

RGB Arrangement

R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

RAM data write (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"

1st transfer		2nd transfer								3rd transfer							

GRAM data

DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10

RGB Arrangement

R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

RAM data write (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "1"

	1st transfer					2nd transfer						3rd transfer					

GRAM data

DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12

RGB Arrangement

R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Figure 25 8-bit Interface Data Format

LG Electronics

Data Transfer Synchronous in 8-bit Bus Interface operation

The LGDP4531 supports a data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 8 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.
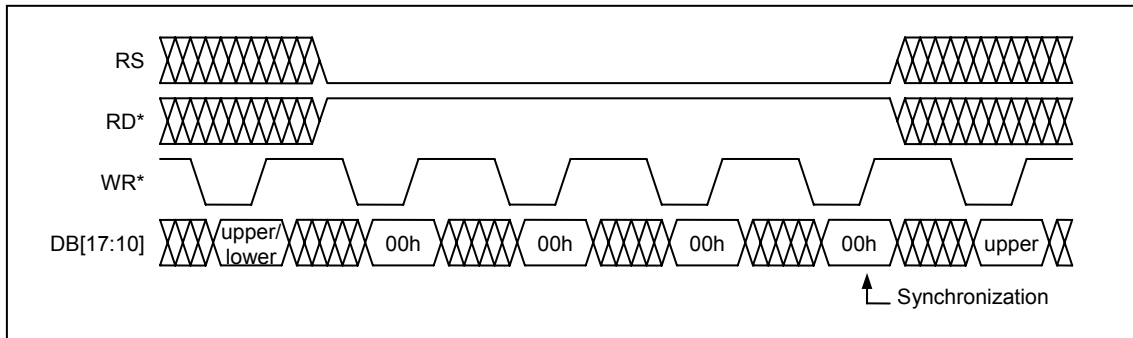
Figure 26 8-bit Data Transfer Synchronization

LG Electronics

Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the IOGND/IOVcc/IOGND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The LGDP4531 recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The LGDP4531 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4531 are compared and both 6-bit data match, and then the LGDP4531 starts taking in data. The least significant bit of the device identification code is set with the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the LGDP4531 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). The LGDP4531 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The LGDP4531 writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the LGDP4531 starts transferring or receiving data in units of bytes. The LGDP4531 executes data transfer from the MSB. The LGDP4531's instruction takes 16-bit format and they are executed inside after it is transferred in two bytes (16 bits: DB15-0) from the MSB (The LGDP4531 expands RAM write data into 18-bit format when writing them to the internal GRAM). The first byte received by the LGDP4531 following the start byte is always the upper eight bits of instruction and the second byte is the lower 8 bits of instruction.

In case of reading data from the GRAM, the LGDP4531 does not transfer valid data until first five bytes of data are read from the GRAM following the start byte. The LGDP4531 starts sending valid data as it reads the sixth and subsequent byte data.

Table 67 Start byte format

Transferred bits	1	2	3	4	5	6	7	8
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

Note: ID bit is selected by setting the IM0/ID pin.

Table 68

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

Instruction

	1st transfer								2nd transfer							
Input	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Instruction Bit (IB)	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0

RAM data write (2 transfers/pixel, 65k colors) – TRI = "0"

	1st transfer								2nd transfer							
GRAM data	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

RAM data write (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"

	1st transfer						2nd transfer						3rd transfer					
GRAM data	D23	D22	D21	D20	D19	D18	D15	D14	D13	D12	D11	D10	D7	D6	D5	D4	D3	D2
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Figure 27 Data format for SPI
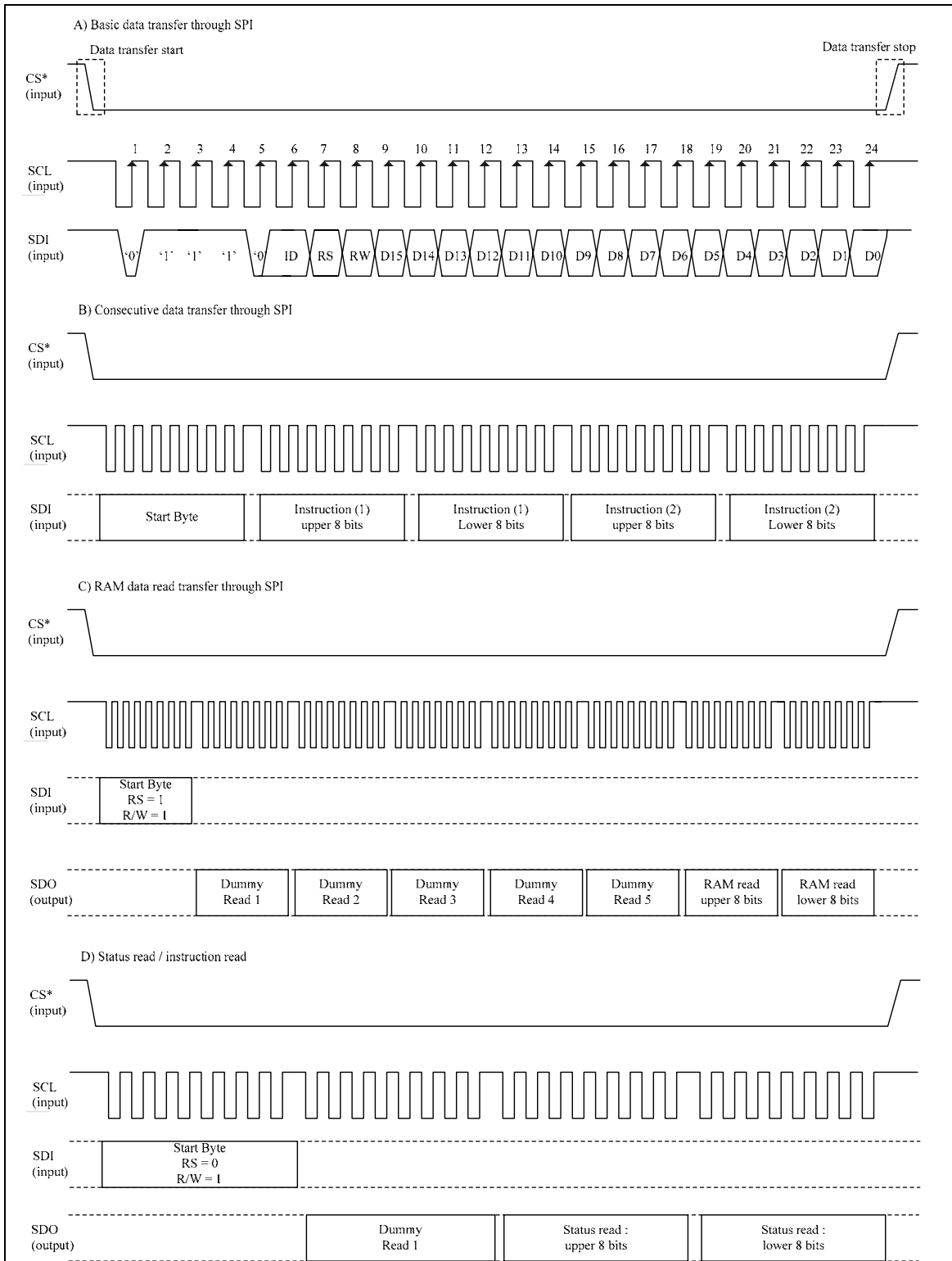
Figure 28 Data Transfer in Serial interface

VSYNC Interface

The LGDP4531 supports VSYNC interface, enabling the LGDP4531 to display a moving picture with minimum modifications to the existing system, using system interface and the frame synchronization signal (VSYNC).
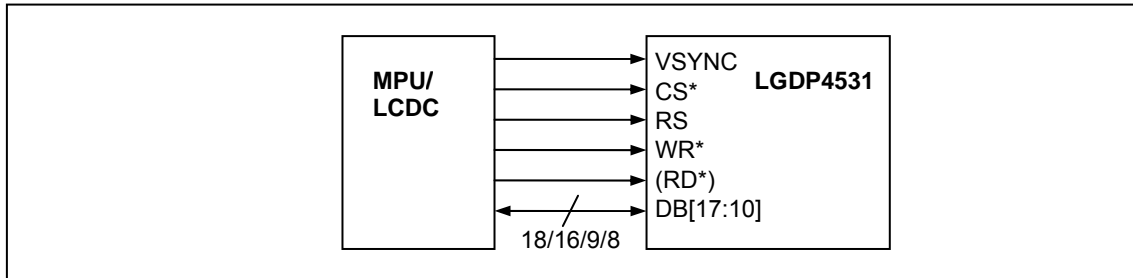
Figure 29 VSYNC Interface

The VSYNC interface is selected by setting DM[1:0] = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at a speed faster to a certain degree than the internal display operation speed, it becomes possible to rewrite data without flickering the moving picture on display and enables the LGDP4531 to display a moving picture using a system interface.

The LGDP4531 performs the display operation with the internal clock signal generated from the internal oscillator and the VSYNC signal in this mode. In VSYNC mode, the data displayed on the screen are written to the internal RAM in order to transfer only the data to be written over the moving picture RAM area and thereby minimize the total data transfer required for moving picture display.
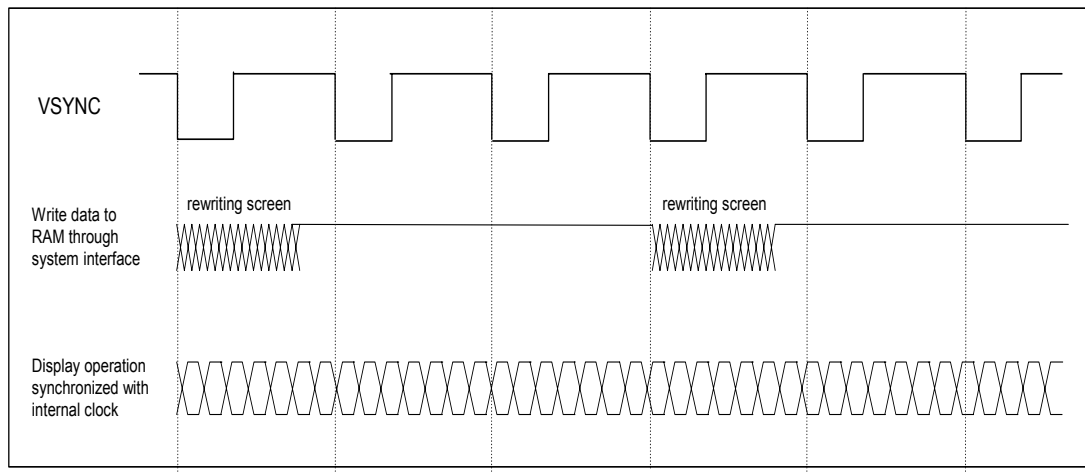
Figure 30 Moving Picture Data Transfers via VSYNC Interfce

The VSYNC interface has the minimum speed of writing data to the internal RAM via the system interface and the minimum internal clock frequency, which are calculated from the following formulae.

Internal clock frequency (fosc) [Hz]
= FrameFrequency × (DisplayLines (NL) + FrontPorch (FP) + BackPorch (BP)) × 64 clocks × variance

$$RAMWriteSpeed > \frac{240 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 64\ clocks \times \frac{1}{fosc}}$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum RAM writing speed and internal clock frequency in VSYNC interface mode is as follows.

[Example]
Display size   240 RGB × 320 lines
Lines   320 lines
Back/front porch   14/2 lines (BP = 1110/FP = 0010)
Frame frequency   60 Hz

Internal clock frequency (fosc)
= 60 Hz × (320 + 2 + 14) lines × 64 Clocks × 1.1 / 0.9 = 1.6 MHz

When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as differences in external resistors or voltage changes are not in consideration. It is necessary to allow for an enough margin if these factors must be incorporated.

Minimum speed for RAM writing
240 × 320 / {((14 + 320 - 2) lines × 64 clock) / 1.6 MHz} = 5.7 MHz

The above theoretical value is calculated on the premise that the LGDP4531 starts writing data to the internal RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line where display operation is performed and the RAM line address where data write operation is performed.

The RAM write speed of 5.7MHz or more on the falling edge of VSYNC will guarantee the completion of RAM write operation before the LGDP4531 starts displaying the RAM data on the screen, enabling rewriting the entire screen without flicker.

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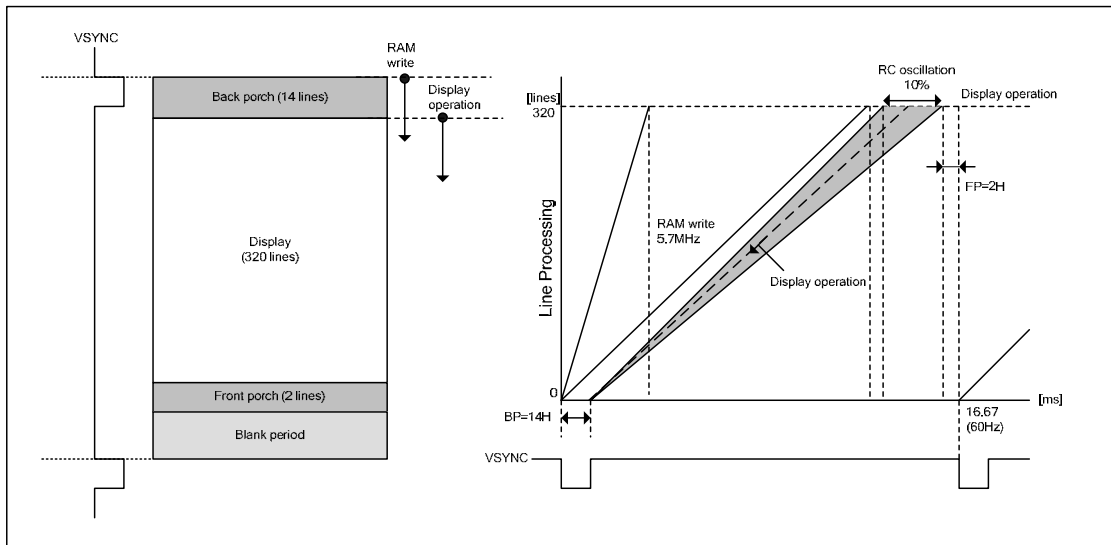
Figure 31 Write/Display Operation Timing via VSYNC Interface

Notes in using the VSYNC interface

1. The above example of calculation gives a theoretical value. In the actual setting, other possible causes of variances not counted in the above example such as differences in internal oscillators should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a RAM writing speed.

2. The above example of calculation gives a minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting a minimum RAM writing speed can have extra margins.
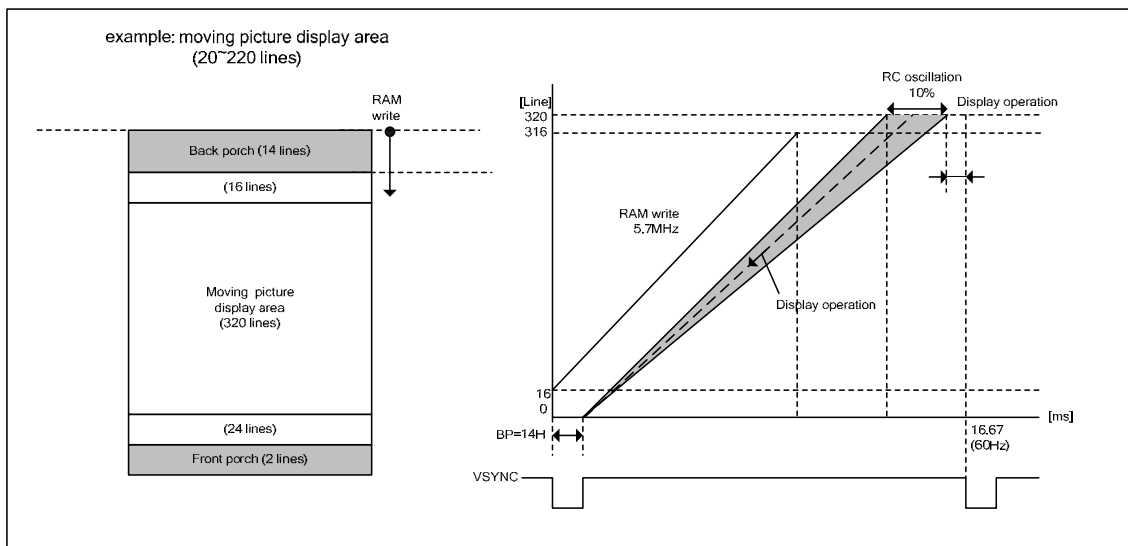
Figure 32 RAM write margin

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3. After drawing 1 frame, a front porch period continues until the next input of VSYNC is detected.

4. When switching from the internal clock operation mode (DM1-0 = "00") to the VSYNC interface mode, or the other way around, it is enabled from the next VSYNC cycle, i.e. after completing the display of the frame, which the LGDP4531 was internally processing when switching the modes.

5. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

6. In VSYNC interface mode, set the AM bit to "0" to transfer display data in the method mentioned above.
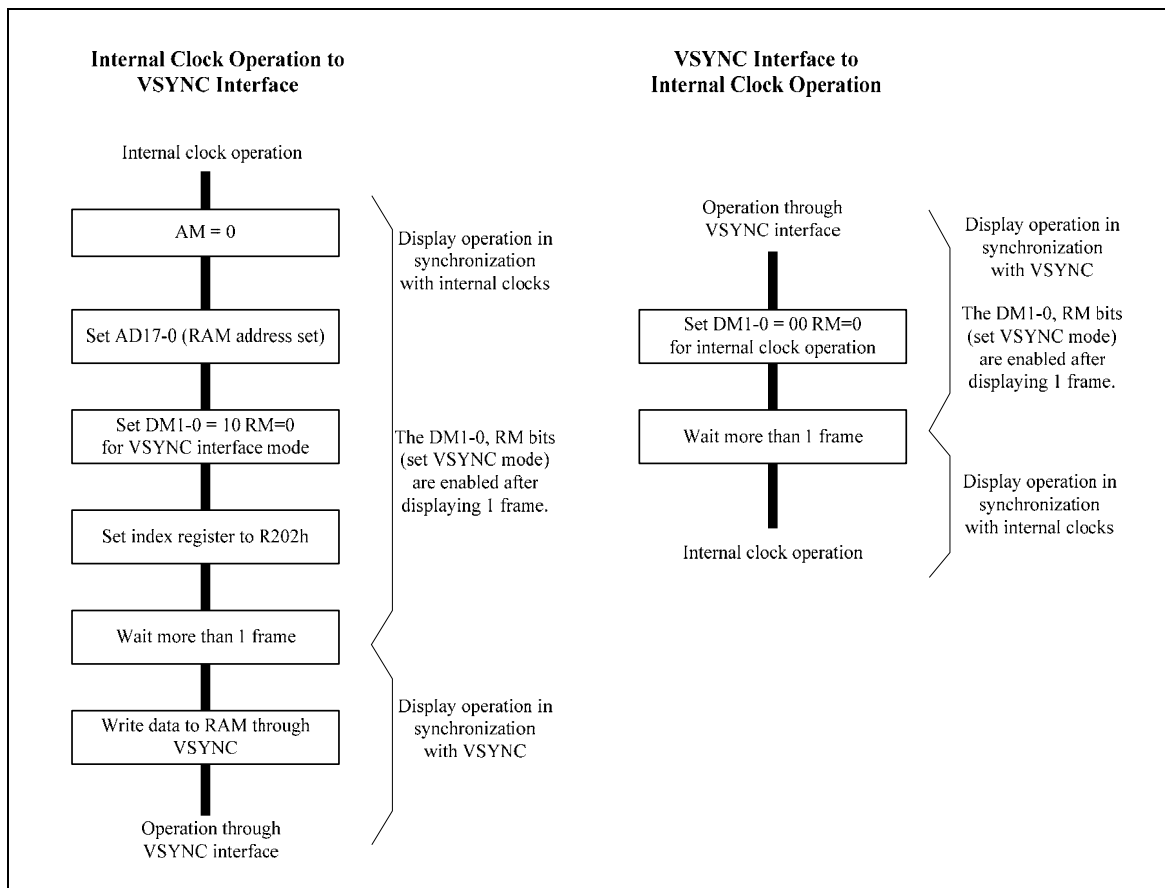
Figure 33 Sequences to Switch between VSYNC and Internal Clock Operation Modes

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External Display Interface

The following RGB interfaces are available with the LGDP4531. The interface operation is set with the RIM[1:0] bits. The RGB interface is used for RAM access.

Table 69

RIM[1:0]	RGB Interface	DB Pin
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	-

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface in combination with the window address function enables minimizing data transfer by rewriting data in high-speed with low power consumption only within the RAM area where data must be updated. In RGB interface operation, it is necessary to set back and front porch periods before and after the display period, respectively.
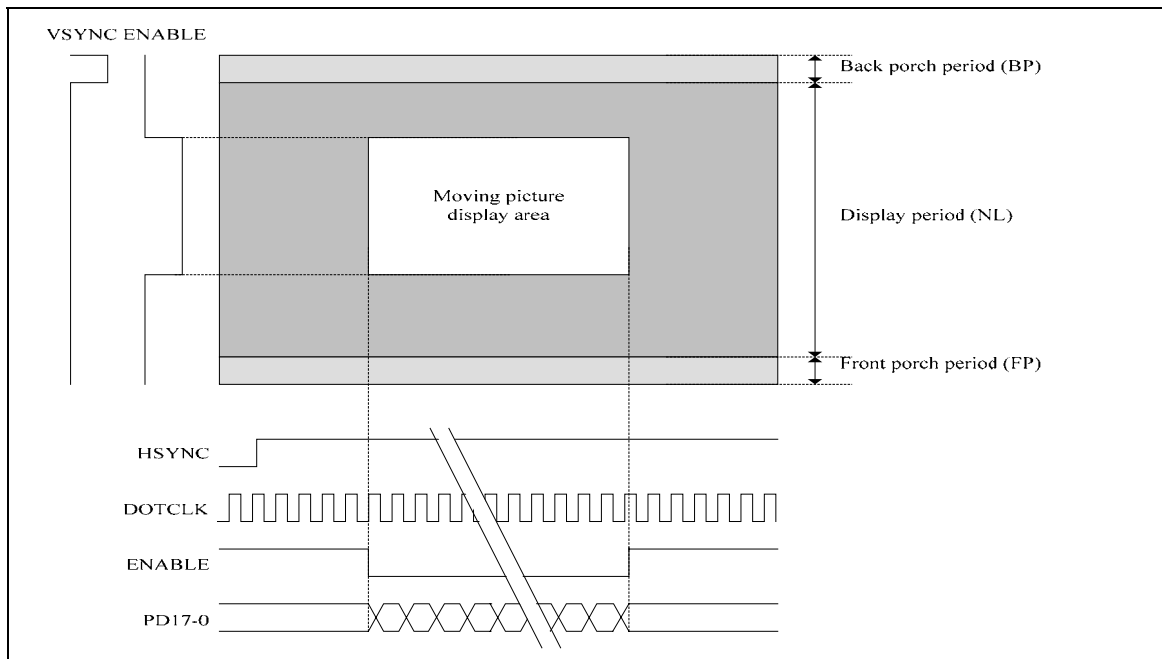
Figure 34 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals are changeable by setting the DPL, EPL, HSPL, and VSPL bits, respectively according to the system configuration.

RGB Interface Timing

The timing relationships of signals in RGB interface operation area as follows.

16-18-bit RGB Interface Timing
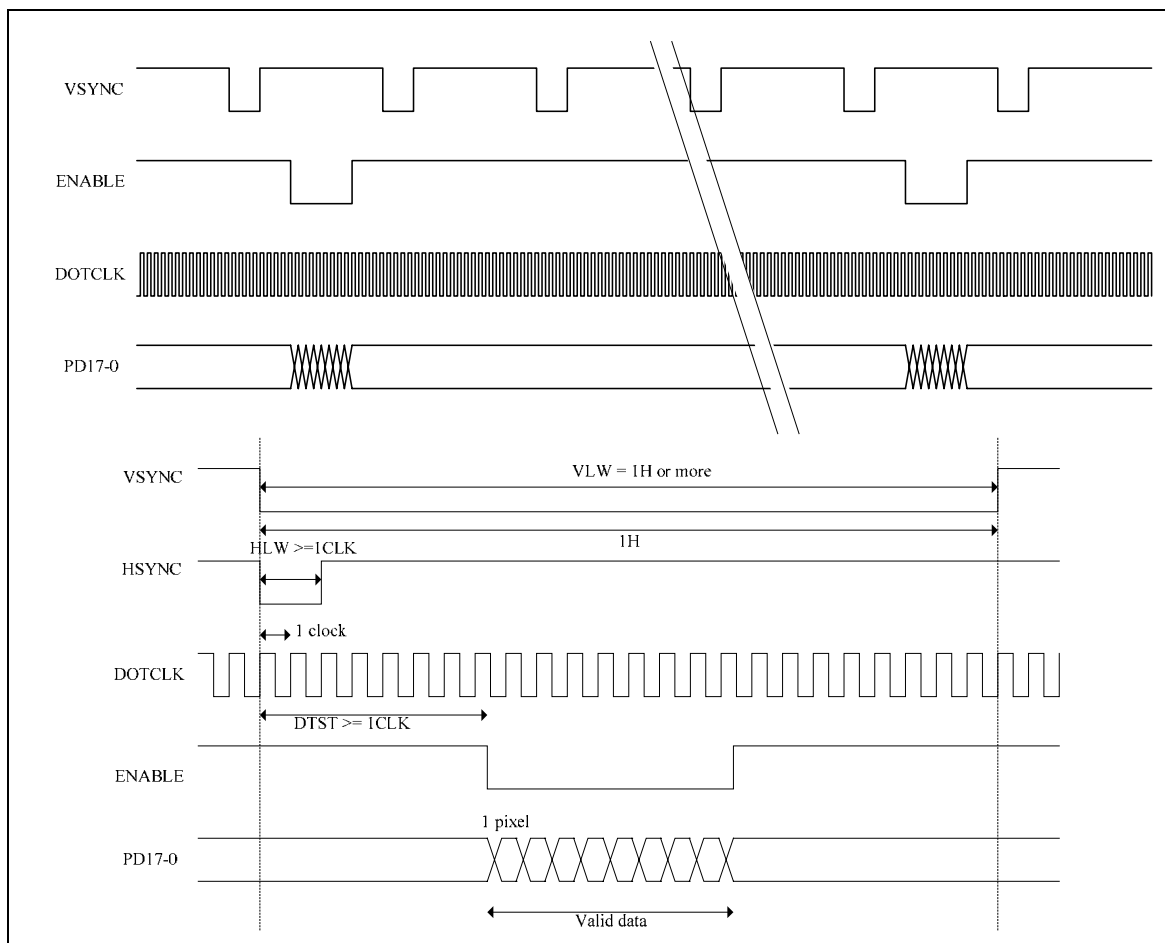
Figure 35

Notes: 1. VLW   : VSYNC Low period
             HLW   : HSYNC Low period
             DTST   : data transfer setup time

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6-bit RGB Interface Timing
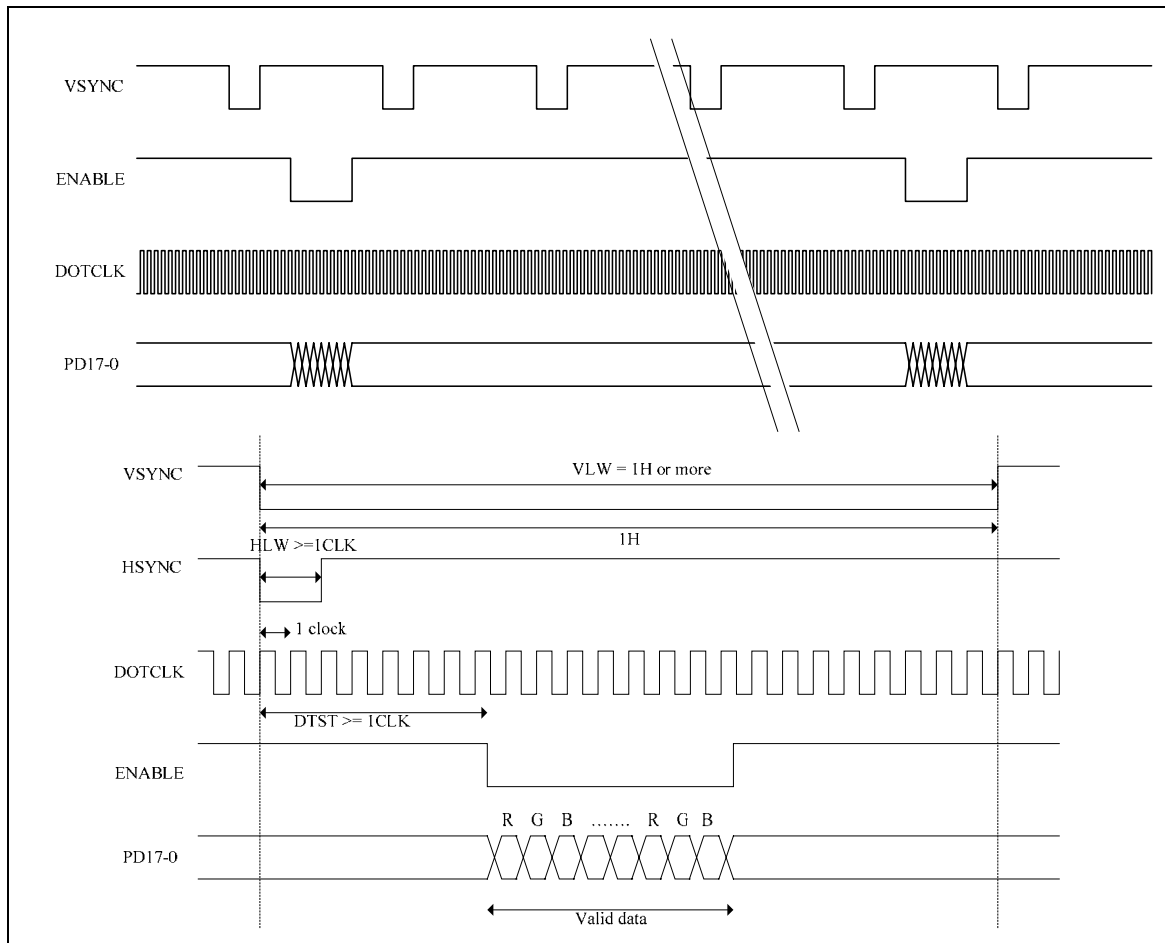
Figure 36

Notes: 1. VLW   : VSYNC Low period
         HLW   : HSYNC Low period
         DTST   : Data transfer setup time
      2. In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so
          that one pixel is transferred in units of three DOTCLKs via DB17-12 (DB5-0).

Moving Picture Display with the RGB Interface

The LGDP4531 supports RGB interfaces for displaying a moving picture and RAM for storing display
data, which provides the following advantages in displaying a moving picture.

1. The window address function can minimize data transfer by specifying a moving picture RAM area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. The data transfer is limited to a moving picture RAM area.
4. The reduction in data transfer contributes to the reduction in power consumption by the entire system
5. The combined use with system interface allows updating data in the still picture area, such as icons,
    while displaying a moving picture via RGB interface

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RAM access via system interface in RGB interface operation

The LGDP4531 allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. Then set RM = "0" to enable RAM access via system interface. When reverting to the RGB interface operation, wait for a time for a read/write bus cycle. Then, set RM = "1" and the index register to R22h to start accessing RAM via RGB interface. A conflict between RAM accesses via two different interfaces will not guarantee write operation.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.
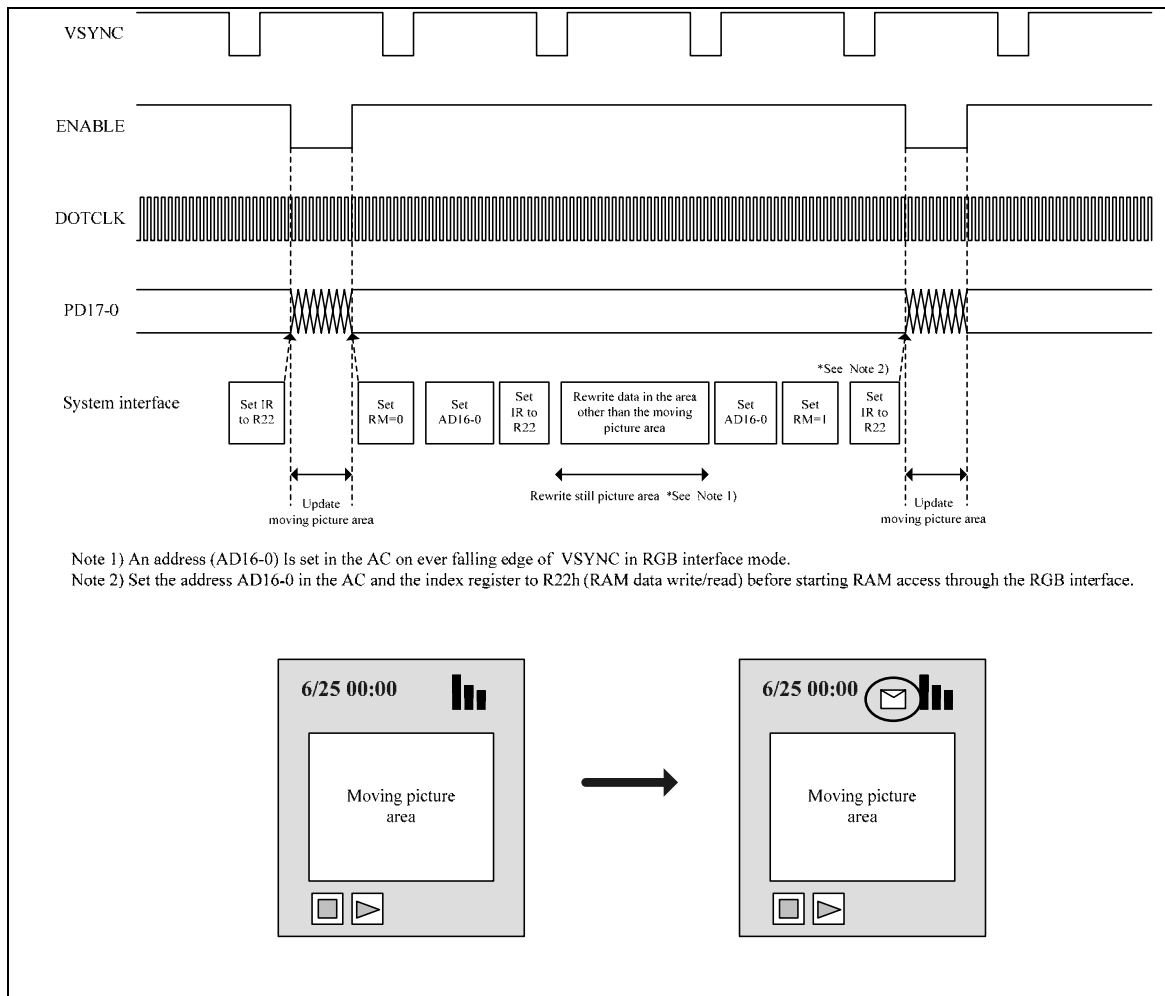
Figure 37 Updating the Still Picture Area while Displaying Moving Picture

6-bit RGB Interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus according to data enable signal (ENABLE). Unused pins DB[11:0] must be fixed at either IOVcc or IOGND level.

The instructions are set only via system interface.
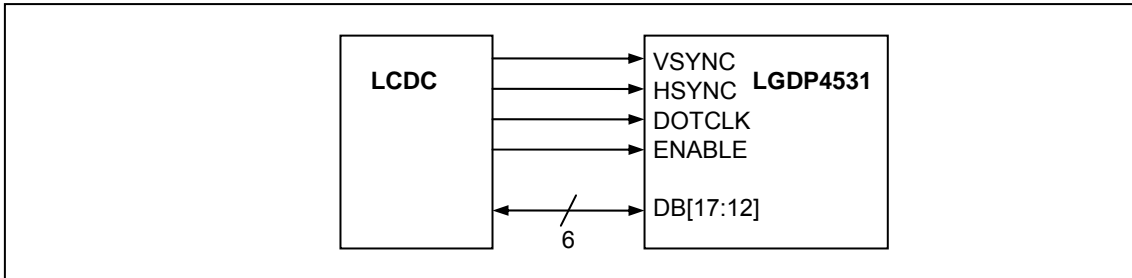
Figure 38 6-bit RGB interface
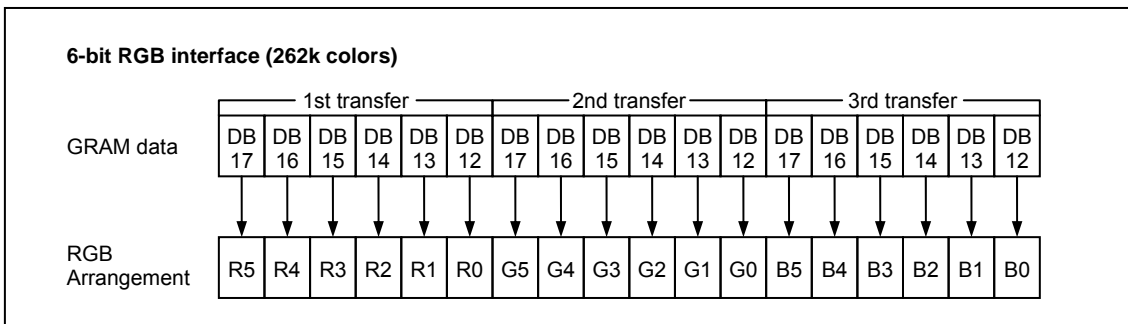
Figure 39 Data format for 6-bit interface

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Data Transfer Synchronization in 6-bit Bus Interface operation

The LGDP4531 has data transfer counters to count the first, second, and third 6-bit data transfers in 6-bit RBG interface operation. The transfer counters are always reset to the first data transfer on the falling edge of VSYNC. If there is a mismatch in the number of data transfers, the counters are reset to the first data transfer at the start of each frame (on the falling edge of VSYNC) and data transfer can be restarted in correct order from the next frame. In case of displaying a moving picture, which requires consecutive data transfer, this function can minimize the effect from the data transfer mismatch and help recover the display system to a normal state.
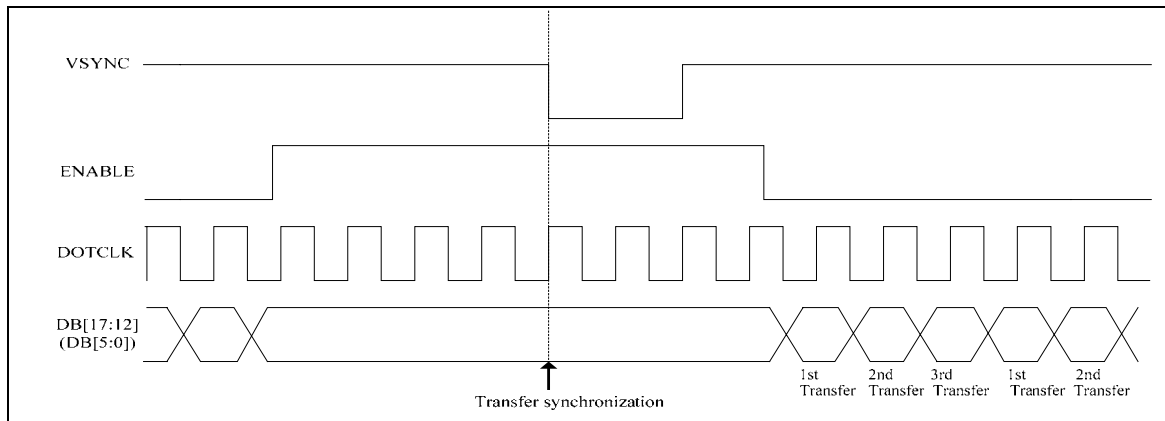
Figure 40 6-bit Transfer Synchronization

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16-bit RGB Interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus according to data enable signal (ENABLE).

The instructions are set only via system interface.
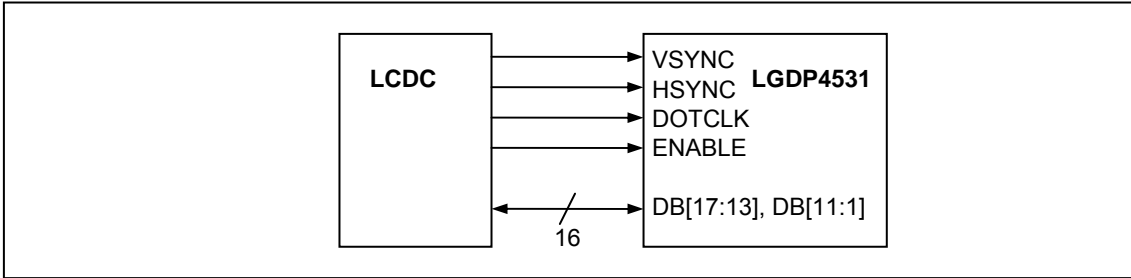
Figure 41 16-bit RGB interface
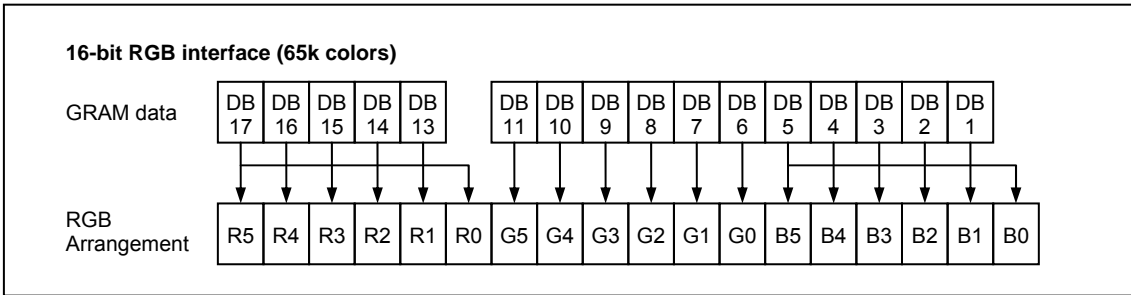
Figure 42 Data format for 16-bit interface

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18-bit RGB Interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) according to data enable signal (ENABLE).

The instructions are set only via system interface.
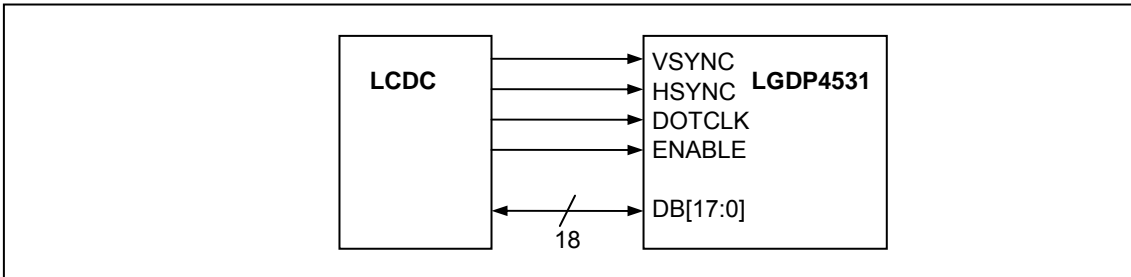
Figure 43 18-bit RGB interface
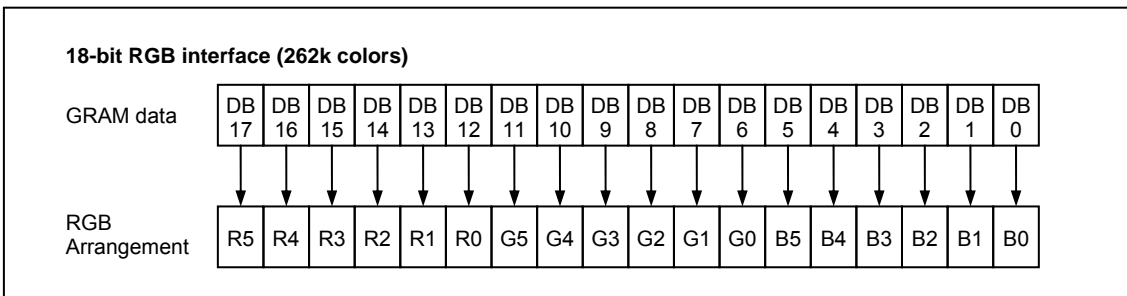
Figure 44 Data format for 18-bit interface

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Notes on Using the External Display Interface

1. The following functions are not available in external display interface operation.

Table 70 Functions Not Available in External Display Interface operation

Fucntion	External Display Interface	Internal Display Interface
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied throughout the display operation.

3. The reference clock for generating liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.

4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel.

5. In 6-bit RGB interface operation, each 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. Take this into consideration and make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE, and data transfer via DB17-12 so that data transfer is completed in units of pixels.

6. When switching between the internal operation mode and the external display interface operation, follow the sequences in Figure 43 RGB and Internal Clock Operation Mode switching sequences.

7. In RGB interface operation, a front porch period continues until the next VSYNC input is detected after the end of each frame period.

8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to the internal RAM.

9. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.
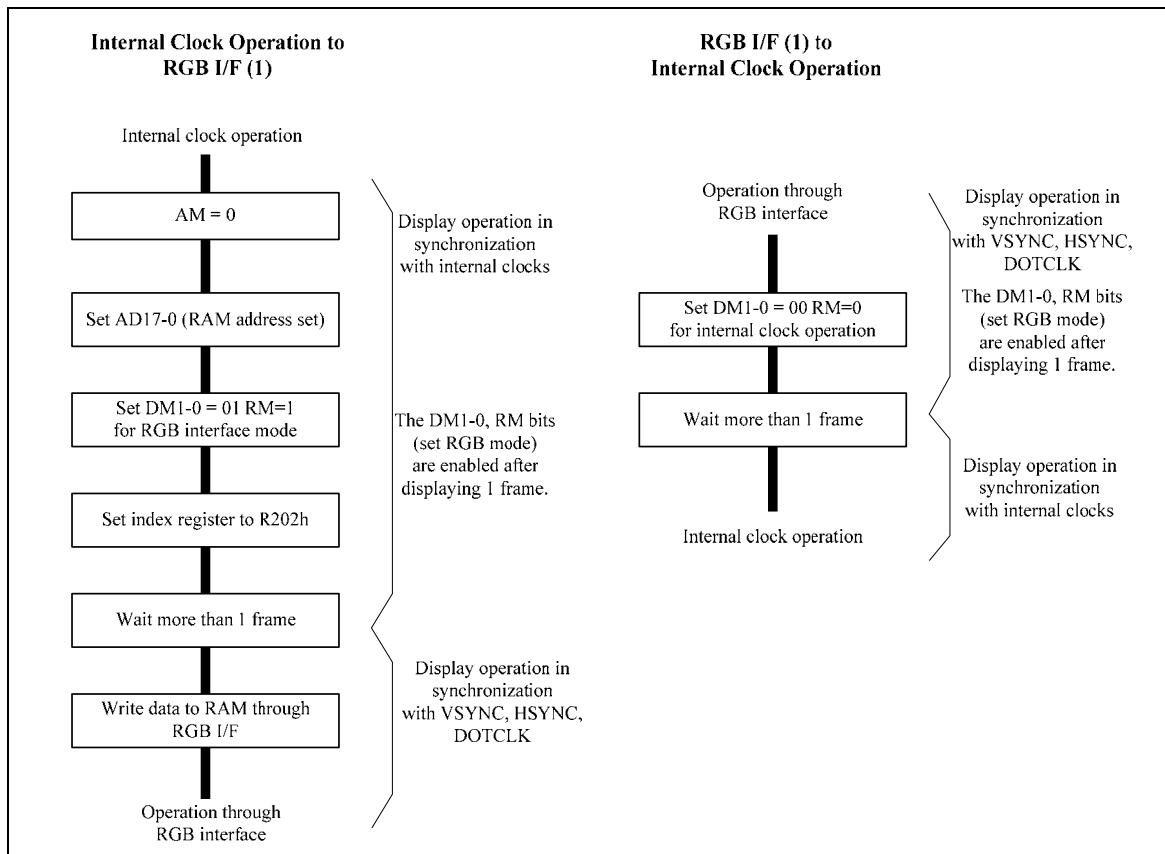
Figure 45 RGB and Internal Clock Operation Mode switching sequences

RAM Address and Display Position on the Panel

The LGDP4531 has memory to store display data of 240RGB x 320 lines. The LGDP4531 incorporates a circuit to control partial display, which enables switching driving methods for full-screen display and partial display.

The LGDP4531 allows separate settings for display control and driving position control and specifying a RAM area for each image displayed on the screen. This structure enables designing a display on the screen not constrained by the mounting position of the display panel.

The following is the sequence of settings for full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image with PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, the register setting in SS bit is required when writing RAM data.

Table 71

	Display ENABLE	Numbers of Lines	RAM area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h13F)

Notes : 1: The base image is displayed from the first line of the screen.
2: Make sure NL ≤ 320 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h13F, respectively.

Table 72

	Display ENABLE	Display position	RAM start position
Partial image 1	PTDE0	(PTDP0, PTEA0)	PTSA0
Partial image 2	PTDE1	(PTDP1, PTEA1)	PTSA1
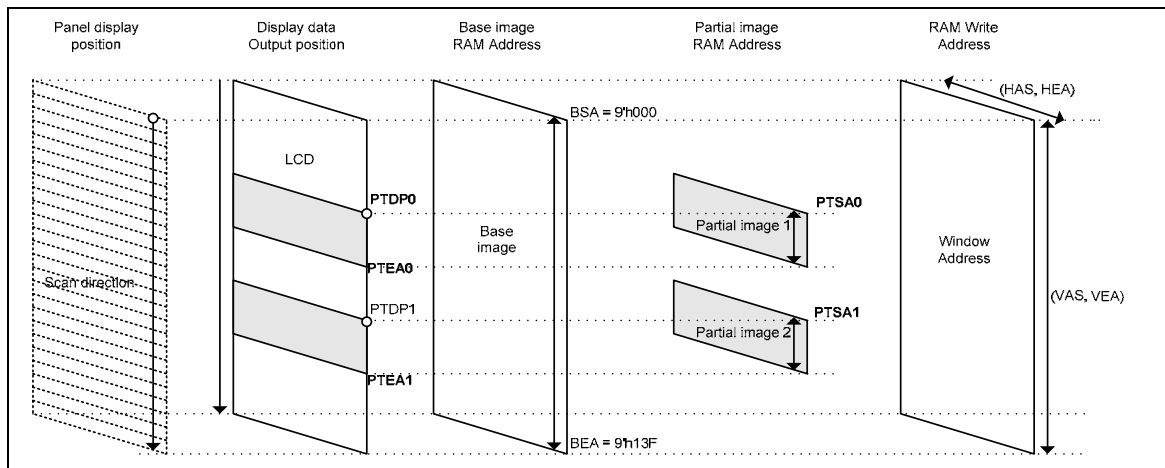
Figure 46 RAM Address, display position and drive position

Restrictions in setting display control instruction

The following are the constraints in setting coordinates of display data, display position, and partial image display.

Screen setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is within the limit: NL $\leq$ 320 lines

Base image display

1. The base image is displayed from the first line of the screen: BSA = 1_{st} line (of the display panel)

2. The base image RAM area specified with BSA, BEA must include the same or more number of lines necessary to drive the liquid crystal panel (NL setting): BEA - BSA $\geq$ NL

Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partials do not overlap each other.

$$0 \leq PTDP0 \leq PTEA0 <$$
$$PTDP1 \leq PTEA1 \leq NL$$

The following figure shows the relationship among the RAM address, display position, and driving positions of the panel.
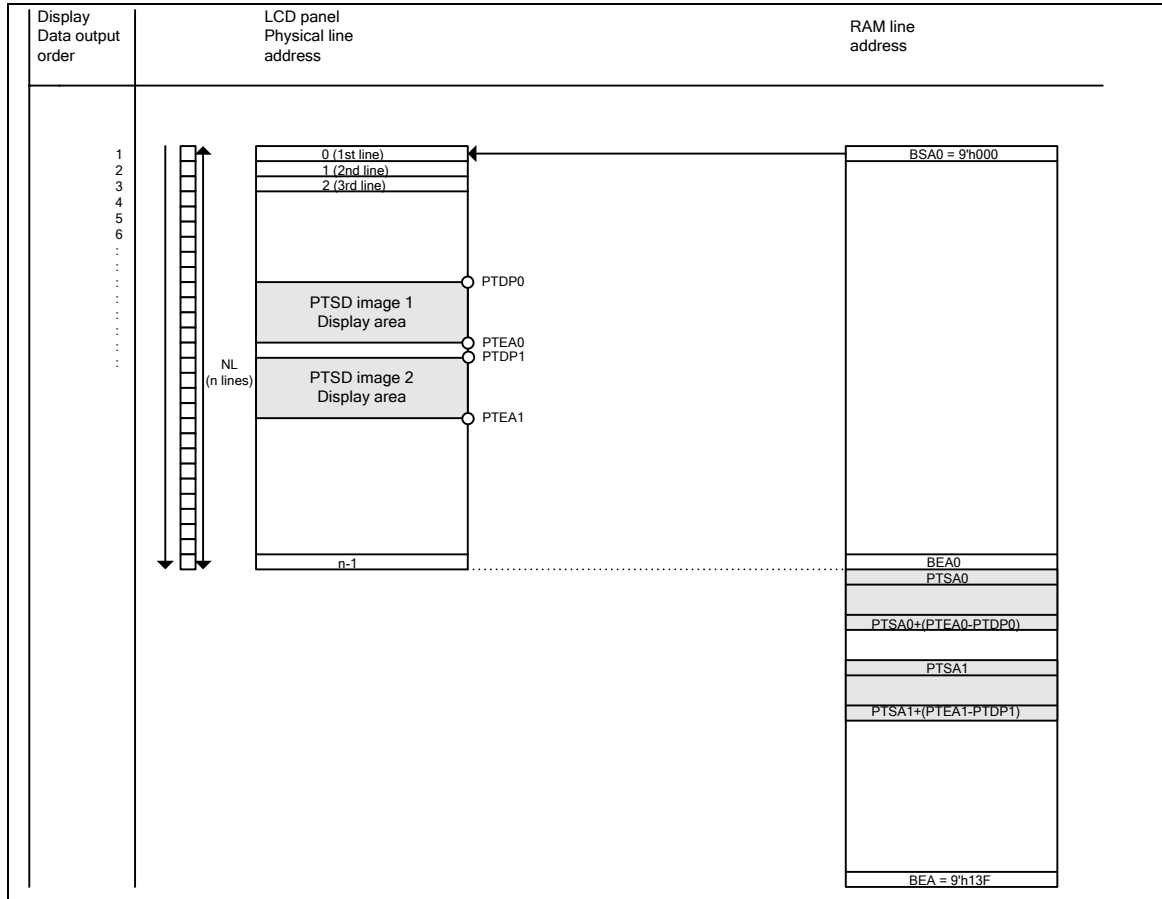
Figure 47 Display RAM Address and display position

Note: In this figure, the RAM address is defined in relation to the display position on the panel. Inside the LGDP4531, the RAM address area where the data is written is defined within a window address area on the GRAM address mapping.

Instruction setting example

The followings are the examples of settings for 240(RGB) x 320(lines) panels.

1. Full screen display (no partial)

The following is an example of setting for full screen display.

Table 73

Base image display insruction	
BASEE	1
NL[5:0]	6'h27
PTDE0	0
PTDE1	0
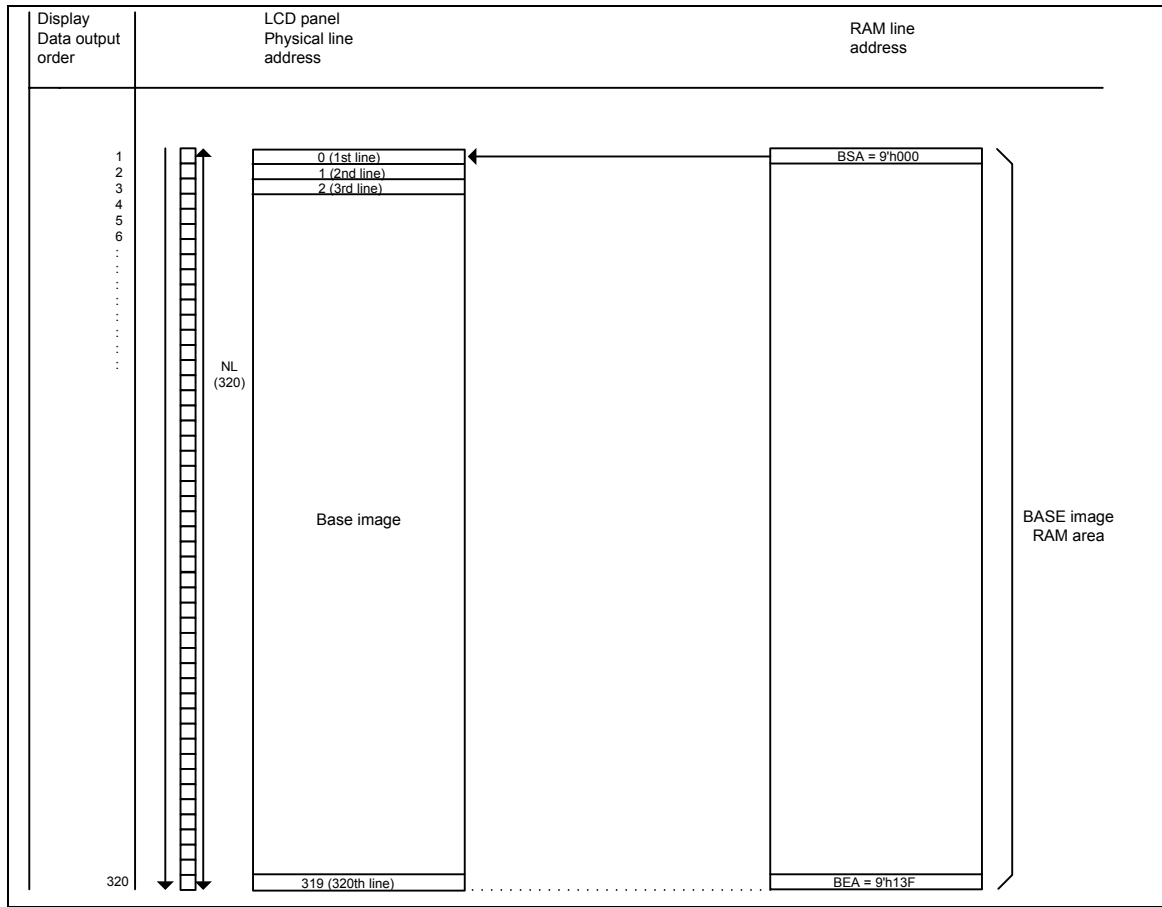
Figure 48 Full screen display (no partial)

2. Partial only

The following is an example of setting for displaying partial image 1 only and turning off the base image display. The partial image 1 is displayed at the position designated by users.

Table 74

Base image display insruction	
BASEE	0
NL[5:0]	6'h27

Partial image 1 display insruction	
PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h08F
PTDP0[8:0]	9'h080

Partial image 2 display insruction	
PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000
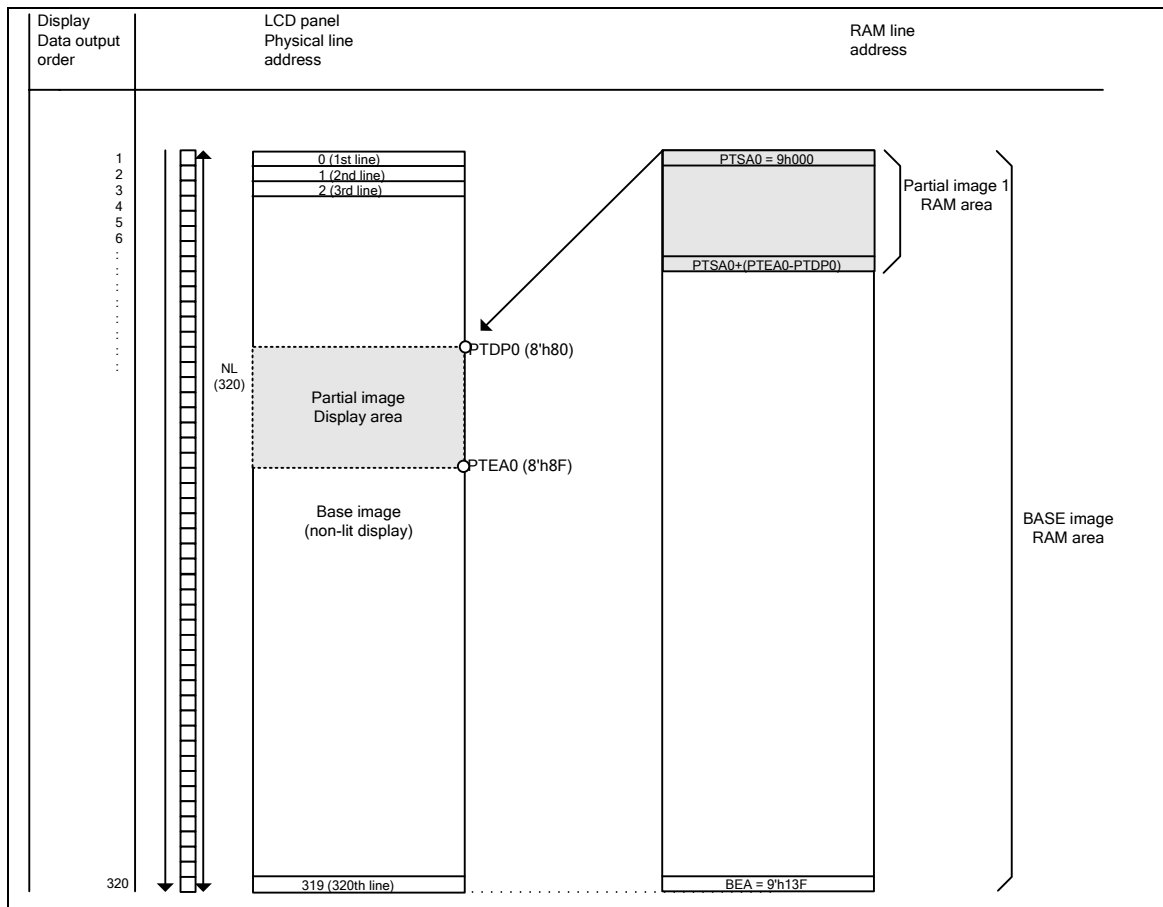
Figure 49 Partial display

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Resizing function

The LGDP4531 supports resizing function (x 1/2, x 1/4), which is executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit representing the contraction factor (x1/2 or x1/4) of the image. This function enables the LGDP4531 to write the resized image data directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system just to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The LGDP4531 processes the contraction of an image simply by selecting pixels. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.
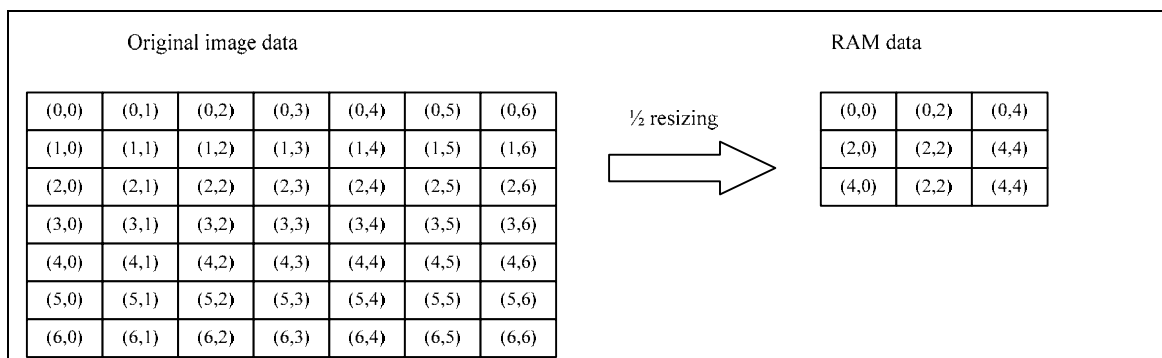
Figure 50 Data transfer in resizing

Table 75

Origianl image size (X x Y)	Resized image Size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
640x480(VGA)	320x240	160x120
352x288(CIF)	176x144	88x72
320x240(QVGA)	160x120	80x60
176x144(QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

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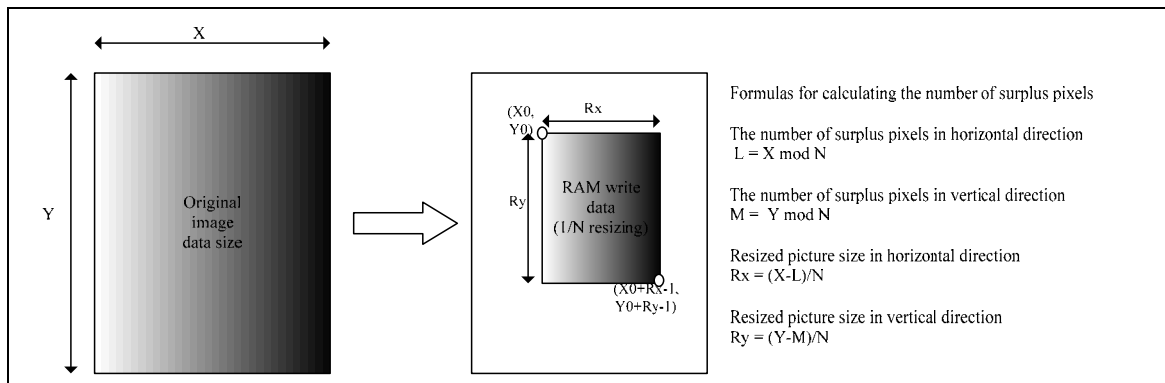
Figure 51 Resizing Setting, surplus pixel calculation

Table 76
Image (before resizing)

Number of data in horizontal direction	X
Numbef of data in vertical direction	Y
Resizing ratio	1/N

Resizing setting in the LGDP4531

Resizing setting	RSZ	N-1
Numbef of data in horizontal direction	RCH	L
Numbef of data in vertical direction	RCV	M
RAM writing start address	AD	(X0,Y0)
RAM window address	HAS	X0
	HEA	X0+Rx-1
	VSA	Y0
	VEA	Y0+Ry-1

Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if RSZ = 2'h0), set RCH = RCV = 2'h0.

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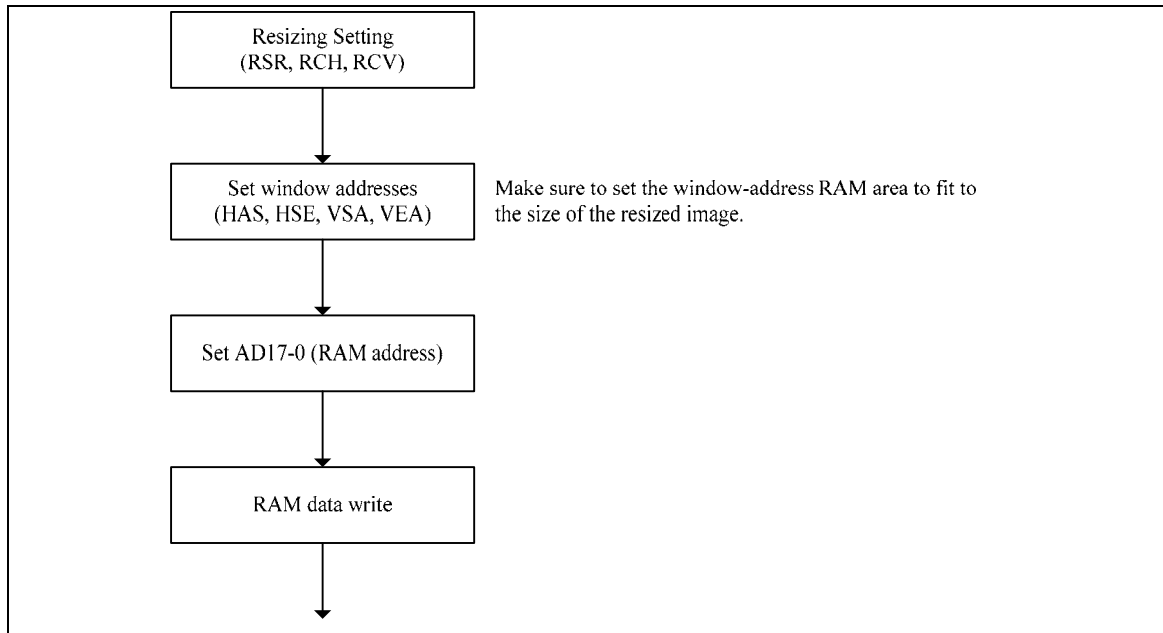
Figure 52 RAM write operation sequence in resizing

LG Electronics

FMARK function

The LGDP4531 outputs an FMARK pulse in the timing when driving the line specified with FMP[8:0] bits. The FMARK signal can be used as a trigger signal in writing display data in synchronization with display operation by detecting the address where the RAM data is read out for display operation.

The output interval of FMARK pulse can be set with the FMI[2:0] bits. Set the FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. Sets FMARKOE = 1 when outputting FMARK pulse from the FMARK pin.

Table 77

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1
9'h002	2
:	:
9'h14D	333
9'h14E	334
9'h14F	335
9'h150 ~ 1FF	Setting disabled

Table 78

FMI[2:0]	FMARK output interval
3'h0	One frame period
3'h1	2 frame periods
3'h3	4 frame periods
3'h5	6 frame periods
Other setting	Setting disabled

FMP setting example
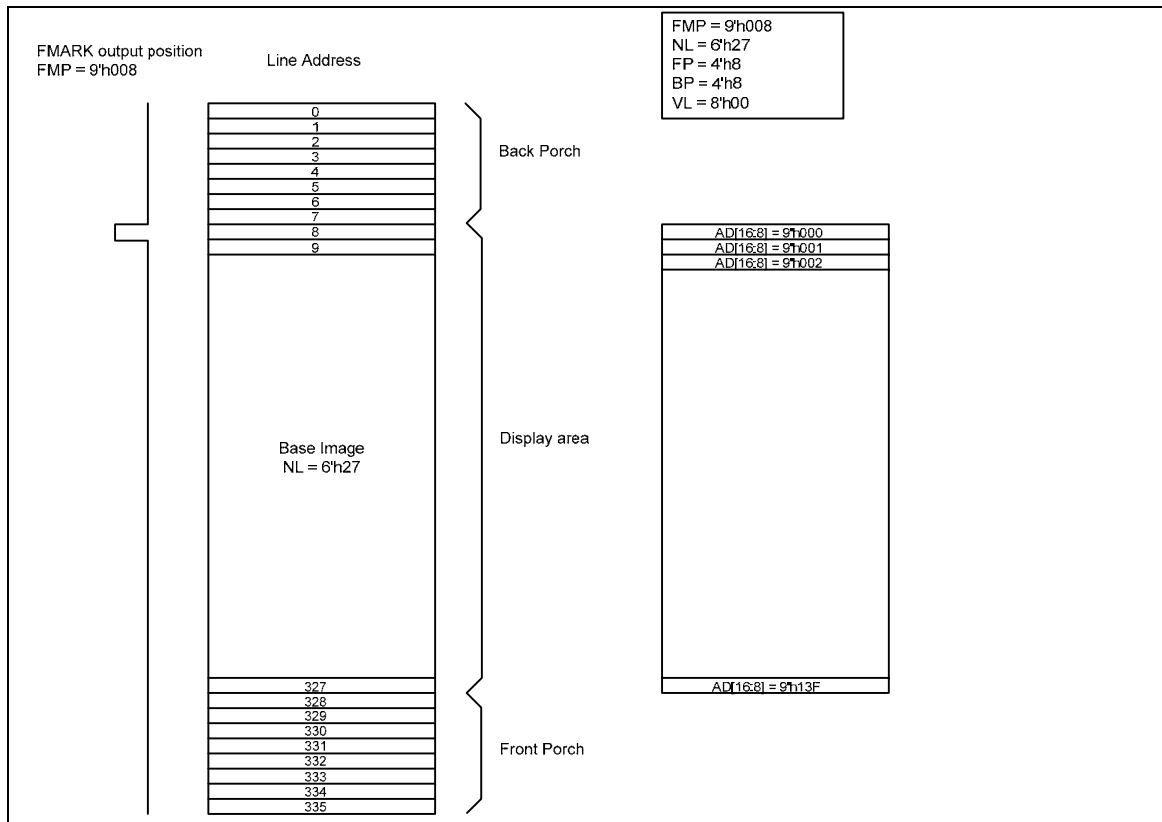
Figure 53

Display operation synchronous data transfer using FMARK

The LGDP4531 uses FMARK signal as a trigger signal to start writing data to the internal GRAM in synchronization with display scan operation.
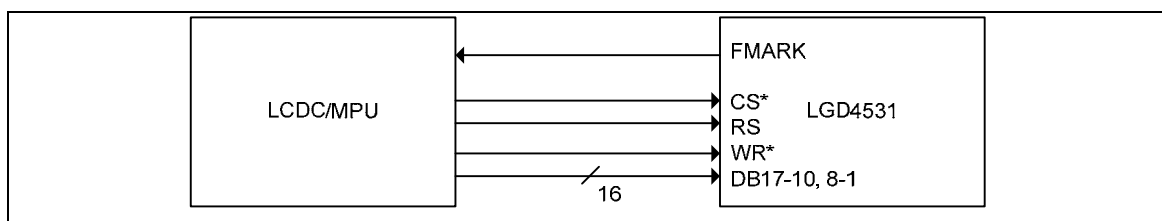
Figure 54 Display synchronous data transfer interface

The LGDP4531 writes display data to the internal GRAM at a speed faster to a certain degree than that of display operation in order to enable a moving picture display via the system interface without flicker. By writing all display data to the internal RAM, only the data tp be overwritten in the moving picture RAM area is transferred and the total data transfer for moving picture display can be minimized.

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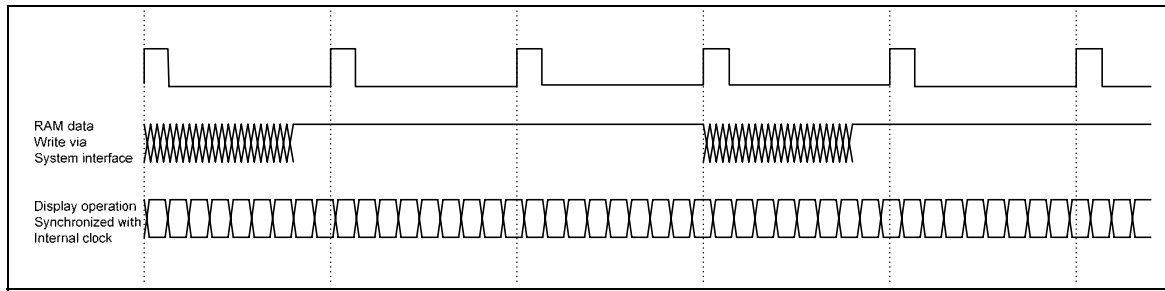
Figure 55 Moving Picture Data Transfers via FMARK function

The data transfer operation via FMARK function has a minimum RAM data rite speed an internal clock frequency, which must be more than the theoretical values chlculated from the following equations

Internal clock frequency (fosc) [Hz]
= FrameFrequency x (DisplayLines(NL) + FrontPorch(FP) + BackPorch(BP)) x 64(clocks) x variance

$$RAMWriteSpeed > \frac{240 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 64\ clocks \times \frac{1}{fosc}}$$

Note : When RAM write operation is not started right after the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

LG Electronics

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of the RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the LGDP4531 to write data including image data consecutively without taking data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]	
(Horizontal direction)	$8'h00 \leq HSA \leq HEA \leq 8'hEF$
(Vertical direction)	$9'h000 \leq VSA \leq VEA \leq 9'h13F$
[RAM Address setting range]	
(RAM address)	$HSA \leq AD7\text{-}0 \leq HEA$
	$VSA \leq AD16\text{-}8 \leq VEA$
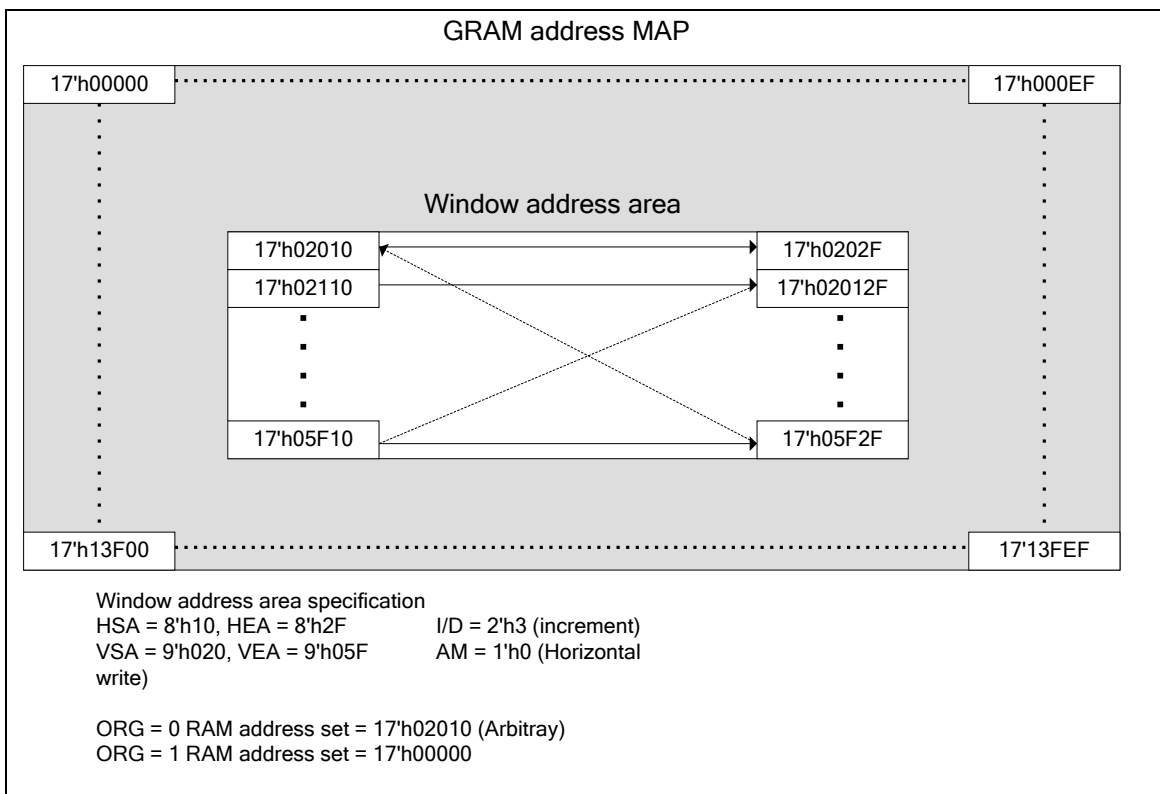
Figure 56 Automatic address update within a Window Address Area

LG Electronics

EPROM Control

LGDP4531 has an embedded EPROM which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32GCV1).
EO01X32GCV1 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32GCV1.
The pins of the embedded EPROM can be controlled using the EPROM control 1 (R60h) register as shown below.

Table 79

EO01X32GCV1	Bit fields of register R40h
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.2V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[6:0] = 0V/1.8V	PDIN[6:0] = 0/1

The RA[1:0] of register R61h selects one of four EPROM bytes.
Accessing EPROM control registers, follow the timing requirements of read and program cycles.
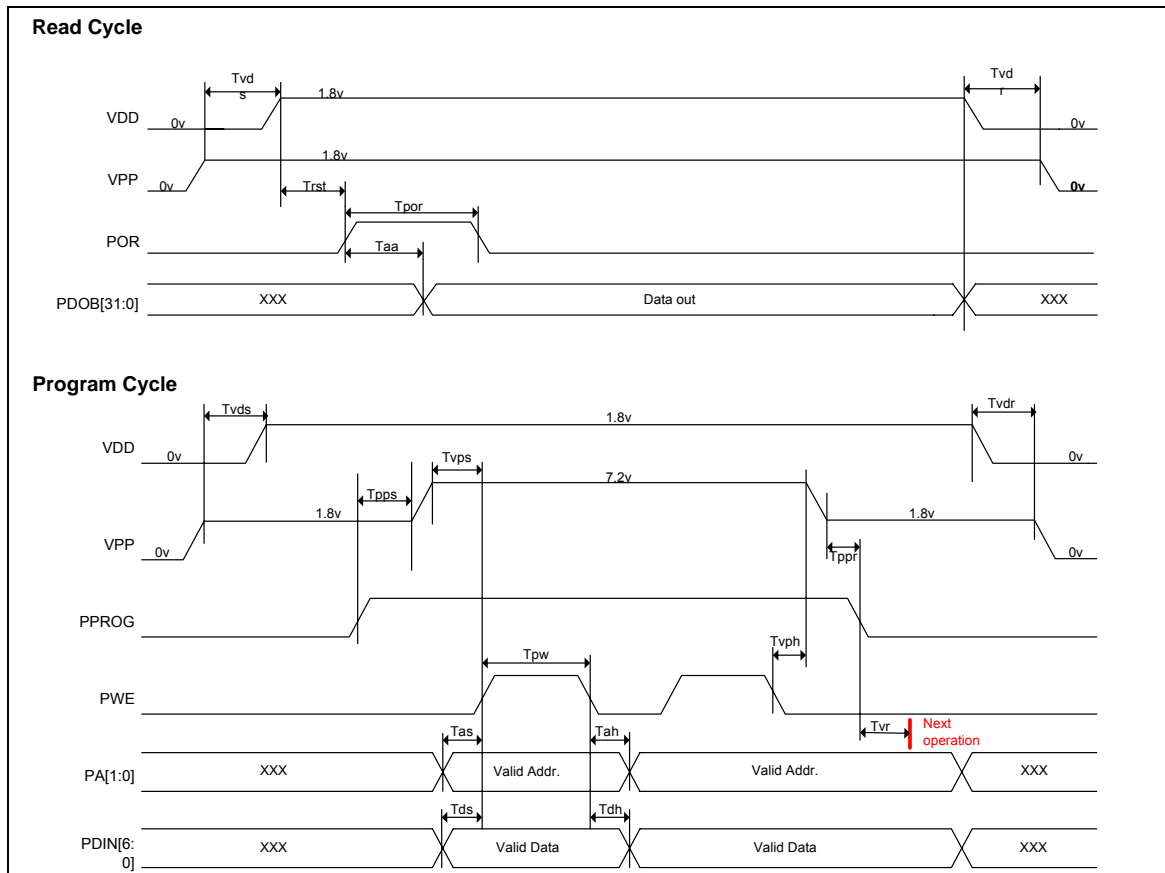
Figure 57 EPROM timings

Table 80

Parameter	Symbol	EO01X32GCV1		Unit
		Min	**Max**	
Risimg Time / Fallimg Time	T_r / T_f	-	1	ns
Data Access Time	T_{aa}	-	70	ns
Power-on Pulse Width Time	T_{por}	70	-	ns
Address / Data Setup Time	T_{as} / T_{ds}	4	-	ns
Address / Data Hold Time	T_{ah} / T_{dh}	9	-	ns
External VPP Setup Time	T_{vps}	0	-	ns
External VPP Hold Time	T_{vph}	0	-	ns
Program Recovery Time	T_{vr}	10	-	us
Program Pulse Width	T_{pw}	90	110	us
VDD Setup Time	T_{vds}	0	-	ms
VDD Recovery Time	T_{vdr}	0	-	ms
PPROG Setup Time	T_{pps}	10	-	ns
PPROG Recovery Time	T_{ppr}	10	-	ns

Notes

1. All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.

2. All program signals that align together in the timing diagrams should be derived from the rising clock edge.

3. All timing measurements are from the 50% of the input to 50% of the output.

4. All input waveforms have rising time (t_r) and falling time (t_f) of 1ns from 10% to 90% of the input waveforms.

5. For capacitive loads greater than 1pF, access time will increase by 1ns per pF of additional loading.

6. Program time means one byte program time in user mode

LG Electronics

Scan Mode Setting

The LGDP4531 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the LGDP4531 and the LCD panel.

SM	GS	Scan direction	
0	0		G1, G2, G3, G4, …, G318, G319, G320
0	1		G320, G319, G318, ···, G4, G3, G2, G1
1	0		G1, G3, G5, …, G317, G319, G2, G4, G6, …, G318, G320
1	1		G320, G318, G316, ···, G6, G4, G2, G319, G317, G315, ···, G5, G3, G1

Figure 58

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8-color Display Mode

The LGDP4531 has a function to display in eight colors, where the available grayscales are only V0 and V63, and the power supplies for other grayscales (V1 to V62) are cut off to reduce power consumption. In 8-color display mode, the γ-adjustment registers P0KP0-P0KP5, P0KN0-P0KN5, P0RP0, P0RP1, P0RN0, P0RN1, P0FP0-P0FP3, and P0FN0-P0FN3, are disabled and the power supplies for V1 to V62 are halted. The LGDP4531 does not require rewriting GRAM data by writing the MSB of each dot data to the rest to display in 8 colors.
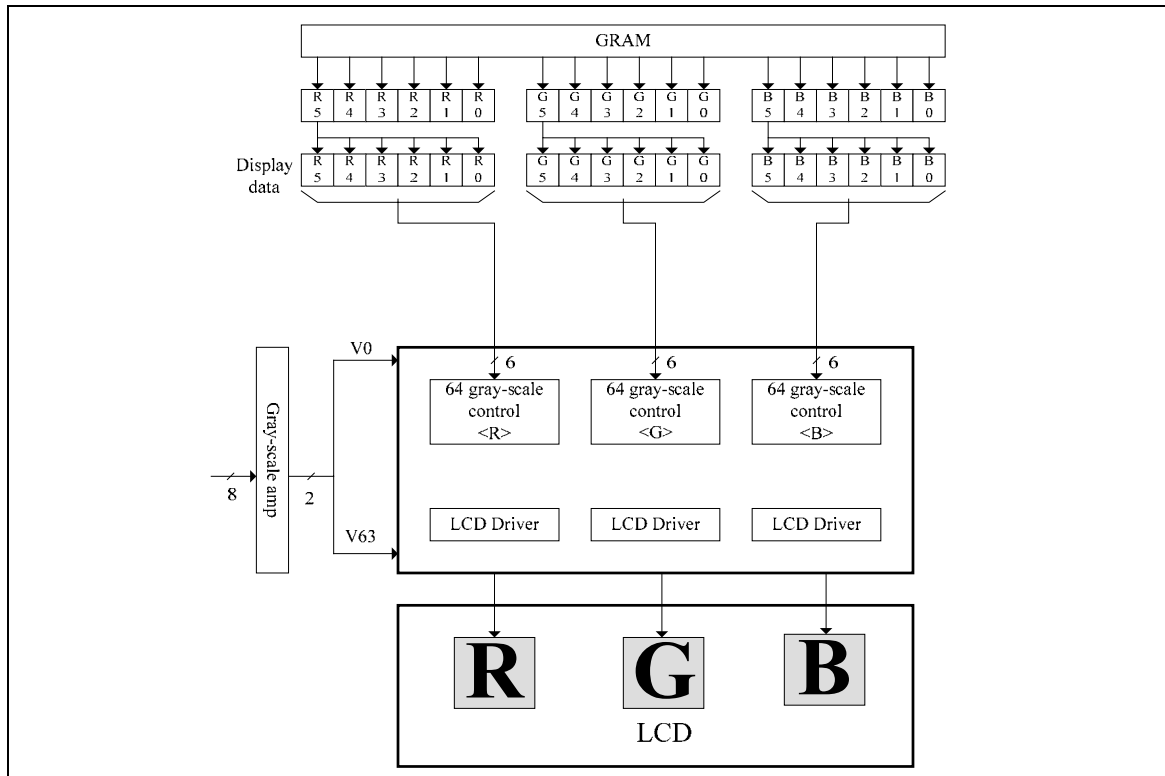
Figure 59 8-color Display mode

Line Inversion AC Drive

The LGDP4531, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.
In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells .
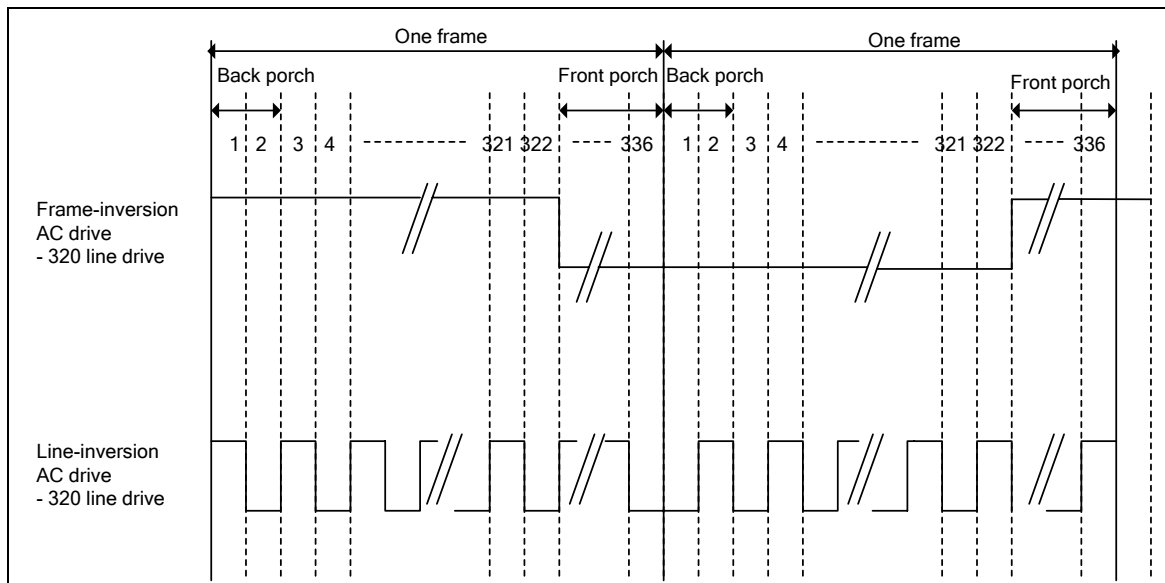
Figure 60 Example of Alternating Signals for n-line Inversion

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Frame-Frequency Adjustment Function

The LGDP4531 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting the DIVI/E, RTNI/E bits without changing the oscillation frequency.

To switch frame frequencies according to whether displaying a moving picture or displaying a still picture, set a high oscillation frequency in advance. Then, set a low frame frequency to save power consumption when displaying a still picture. When displaying a moving picture, set the frequency high.

Relationship between the liquid crystal Drive Duty and the Frame Frequency

The relationship between the liquid crystal drive duty and the frqme frequency is calaulated from the following equation. The frame frequency can be adjusted by setting the 1H period adjustment (RTNI/E) bit and the operation clock division (DIVI/E) bit.

Equlation for calculating frame frequency

$$Frame\ Frequency = \frac{Fosc}{Number\ Of\ Clocks\ Per\ Line\ x\ Division\ Ratio\ x\ (Line + FP + BP)}$$

Fosc	: RC oscillation frequency
Number of Clocks per line	: RTNI/E bit
Division Ratio	: DIVI/E bit
Line	: number of lines to drive the LCD (NL bit)
FP	: Number of lines for front porch
BP	: Number of lines for back porch

Example of Calculation : when maximum frame frequency = 60Hz

Number of lines : 320 lines
1H period : 64 Clock cycles (RTNI/E[4:0] = "10000")
Division ratio of operating clock : 1/1
Front porch : 2 lines
Back porch : 14 lines

Fosc = 60 (Hz) x 64 (clocks) x 1/1 x (320 + 2 + 14) (Lines) = 1. 29(MHz)

In this case, the RC oscillation frequency is to set to 1.29MHz. Adjust the value of the external resistor coneected to the RC oscillator so that RC oscillation frequency becomes 1.29MHz.

Partial Display Function

The partial display function allows the LGDP4531 to drive linies selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven with non-display level to reduce power consumption.

The power saving effect can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

Figure 61

LG Electronics
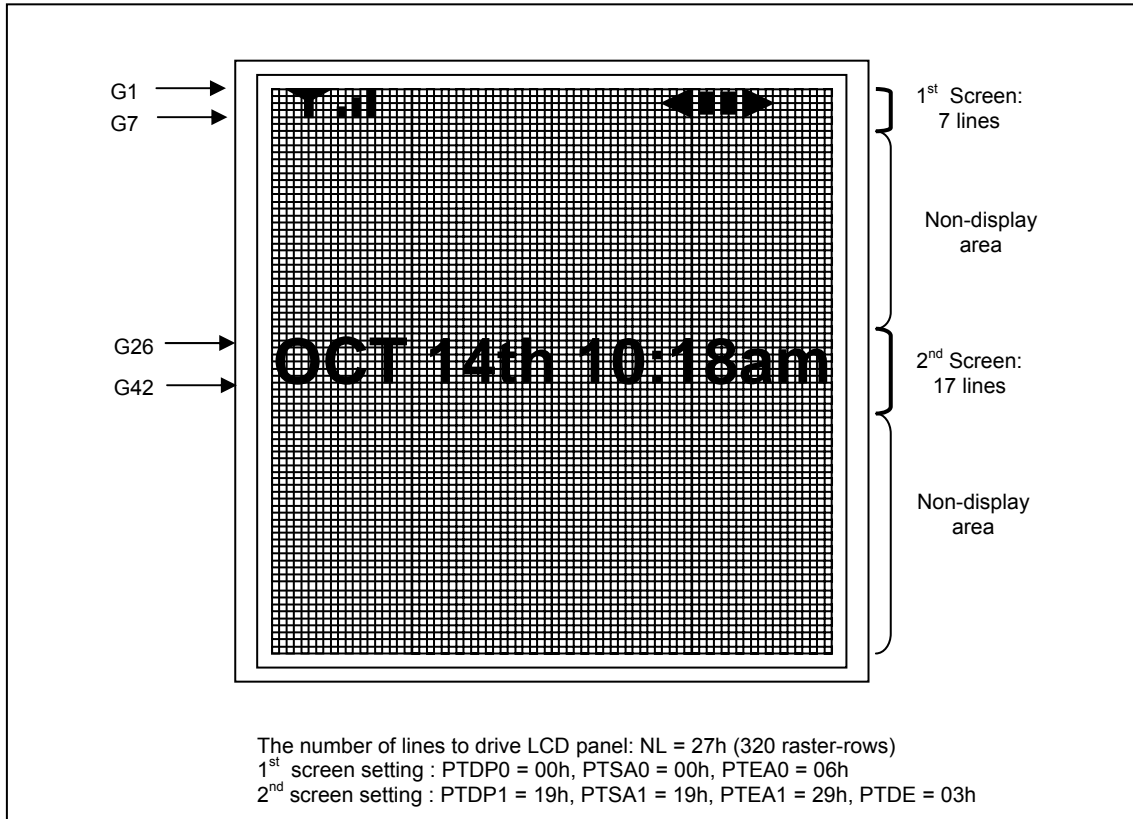
Liquid crystal panel interface timing

The relationships between RGB interface signals and liquid crustal panel control signals in interhal operation and RGB interface operations are as follows.

Internal clock operation
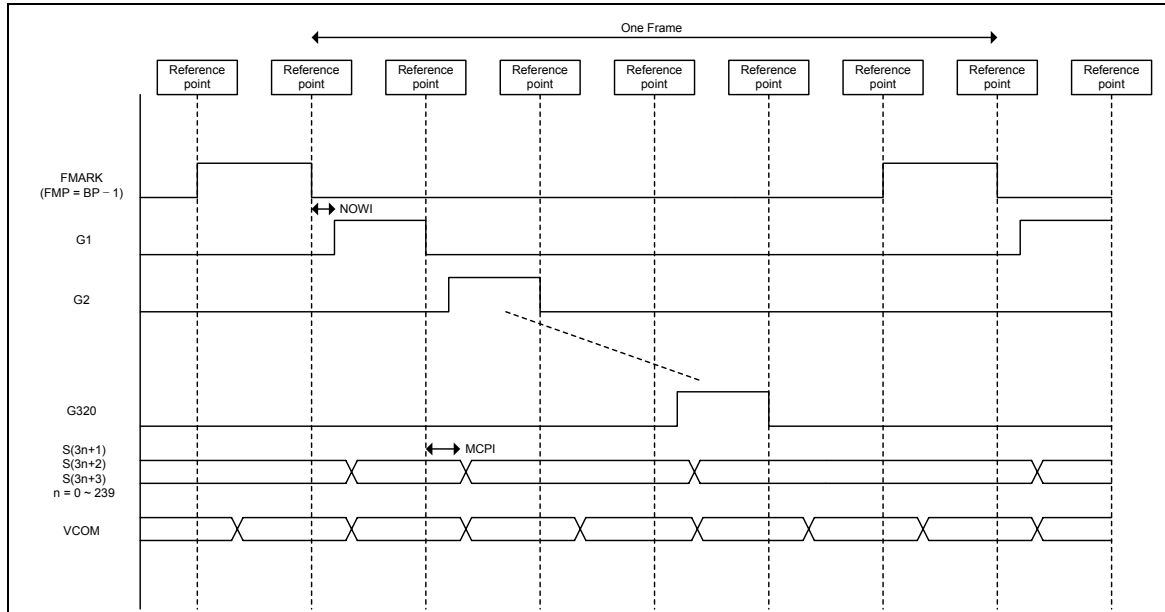
Figure 62

RGB Interface operation

Figure 63

LG LG Electronics
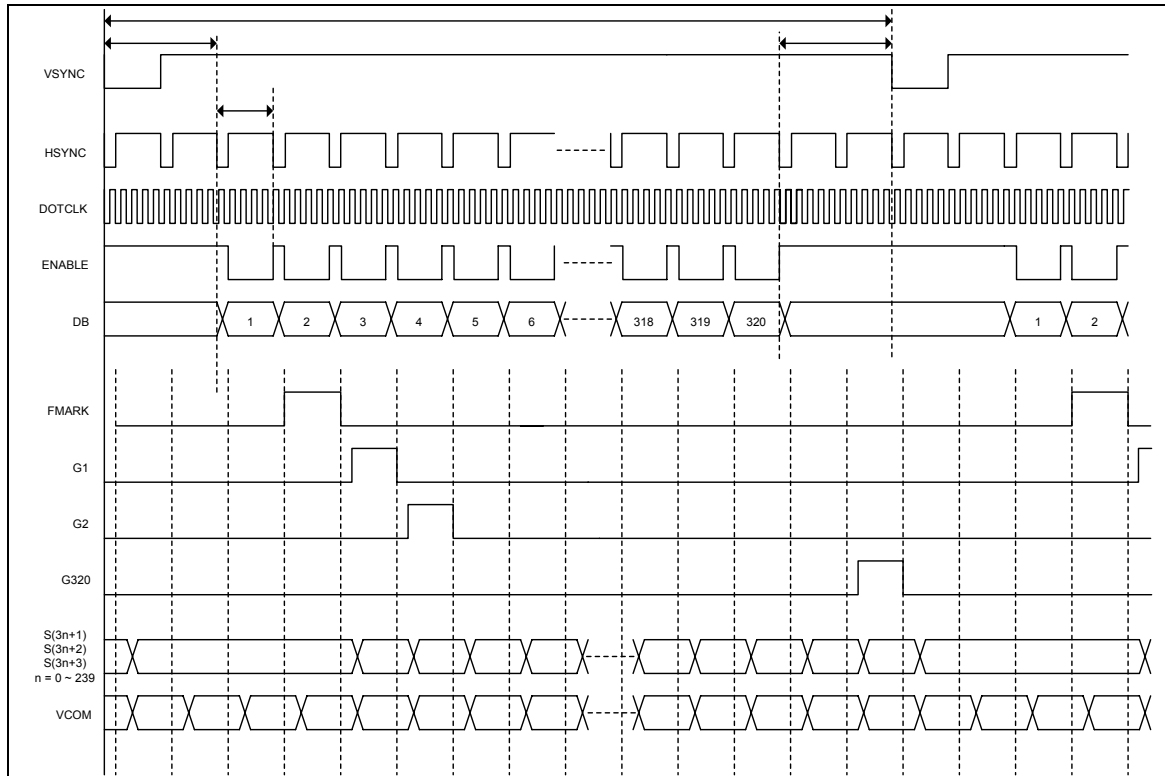
Oscillator

The LGDP4531 generates oscillation with the LGDP4531's internal RC oscillators by placing an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency varies due to resistance value of external resistor, wiring distance, and operating supply voltage. For example, placing an Rf resistor of a larger resistance value, or lowering the supply voltage level brings down the oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between resistance value of Rf resistor and oscillation frequency.
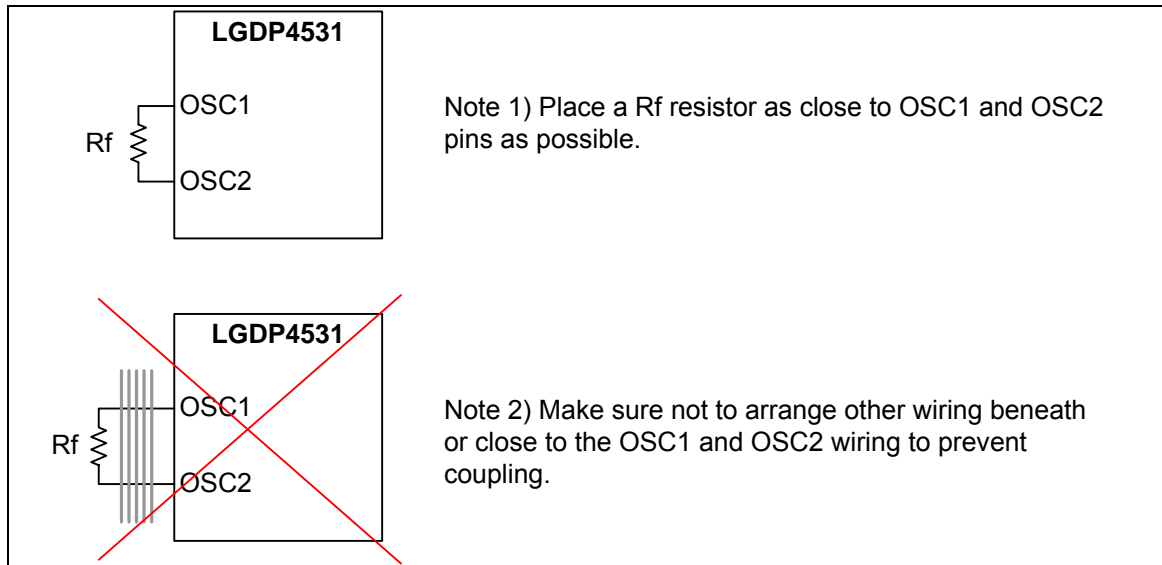
Figure 64

γ-Correction Function

The LGDP4531 has the γ-correction function to display in 262,144 colors simultaneously. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LGDP4531 available with liquid crystal panels of various characteristics.
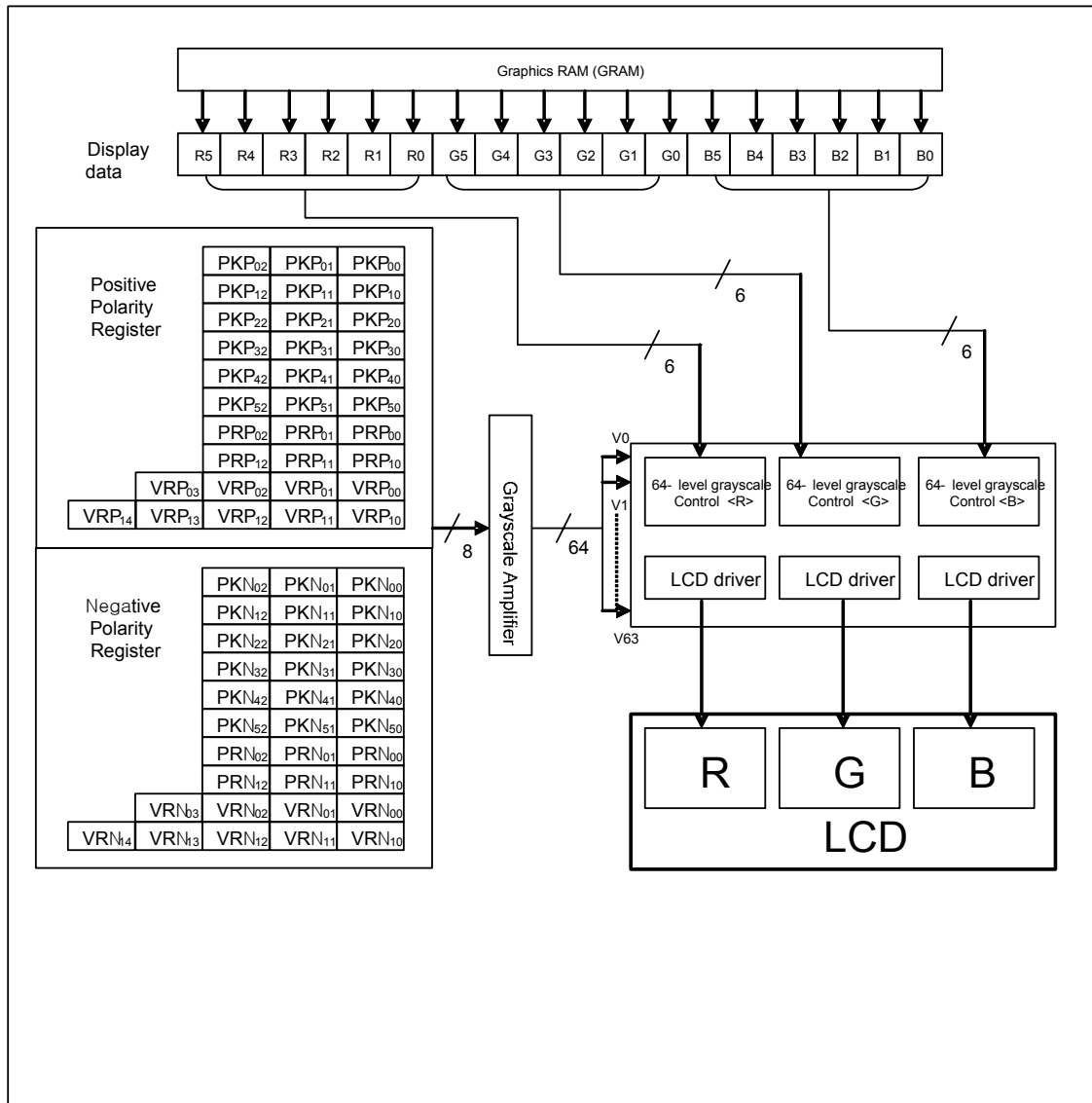
Figure 65 Grayscale control

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Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LGDP4531.
To generate 64 grayscale voltages (V0 to V63), the LGDP4531 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.
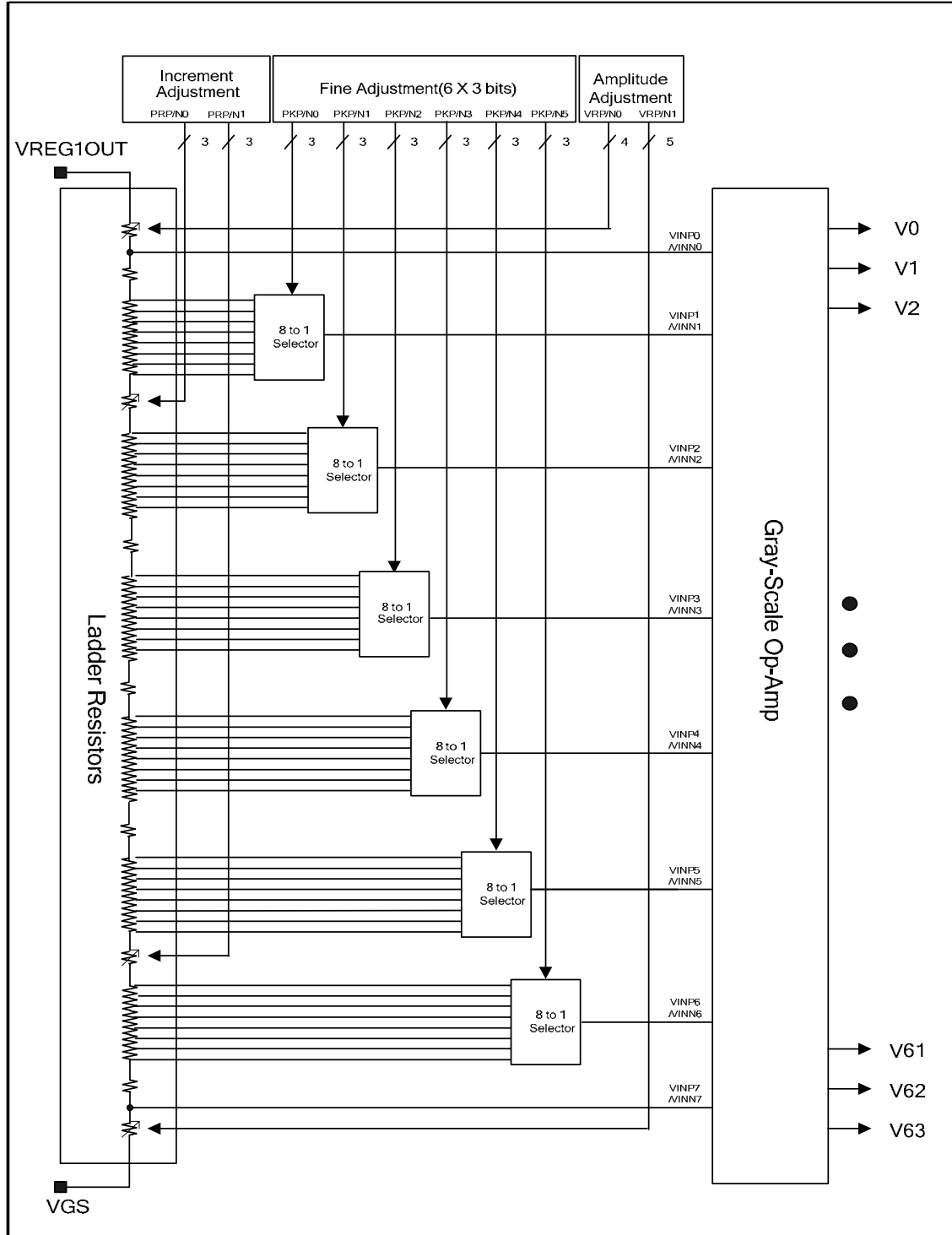
Figure 66 Grayscale amplifier unit

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Figure 67 Ladder resistor units and 8-to-1 selectors (IPS=0)

LG Electronics
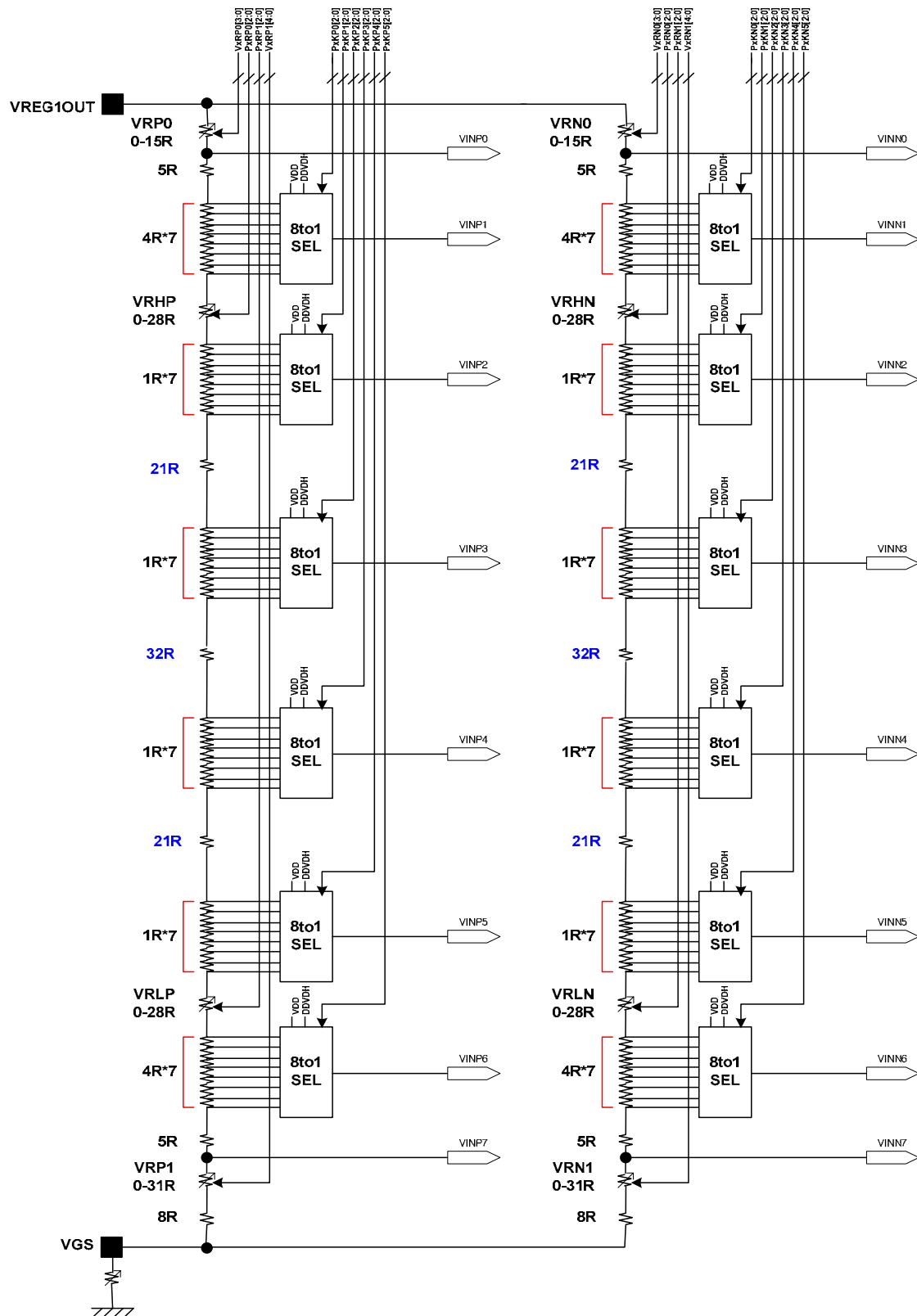
Figure 68 Ladder resistor units and 8-to-1 selectors (IPS=1)

γ-Correction Register

The γ-correction registers of the LGDP4531 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for γ-characteristics of a liquid crystal panel. These γ-correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.
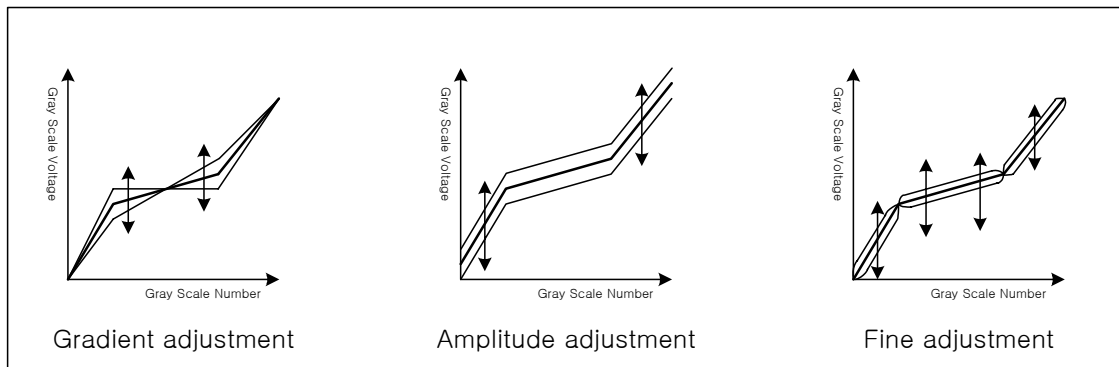
Figure 69

1. Gradient adjustment registers
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers
The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers
The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

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Table 81 List of registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder Resistors and 8-to-1 Selector

Block Configuration

The reference voltage generating unit as illustrated in page 3-4 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LGDP4531 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 82 Gradient adjustment

Register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)
3'h0	0R
3'h1	4R
3'h2	8R
3'h3	12R
3'h4	16R
3'h5	20R
3'h6	24R
3'h7	28R

Table 83 Amplitude adjustment(1)

Register VRP(N)0[3:0]	Resistance VRP(N)0
4'h0	0R
4'h1	1R
4'h2	2R
:	:
4'h12	12R
4'h13	13R
4'h14	14R
4'h15	15R

Table 84 Amplitude adjustment(2)

Register VRP(N)1[4:0]	Resistance VRP(N)1
5'h0	0R
5'h1	1R
5'h2	2R
:	:
5'h28	28R
5'h29	29R
5'h30	30R
5'h31	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

Table 85 Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N3	VINP(N)4	VINP(N)5	VINP(N)6
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

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The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

Table 86 Formula for calculating voltage (IPS=0)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV*(VRP0+5R)/SUMRP	PKP0= 3'h0	VINP1
KVP2	VREG1OUT - ΔV*(VRP0+9R)/SUMRP	PKP0= 3'h1	
KVP3	VREG1OUT - ΔV*(VRP0+13R)/SUMRP	PKP0= 3'h2	
KVP4	VREG1OUT - ΔV*(VRP0+17R)/SUMRP	PKP0= 3'h3	
KVP5	VREG1OUT - ΔV*(VRP0+21R)/SUMRP	PKP0= 3'h4	
KVP6	VREG1OUT - ΔV*(VRP0+25R)/SUMRP	PKP0= 3'h5	
KVP7	VREG1OUT - ΔV*(VRP0+29R)/SUMRP	PKP0= 3'h6	
KVP8	VREG1OUT - ΔV*(VRP0+33R)/SUMRP	PKP0= 3'h7	
KVP9	VREG1OUT - ΔV*(VRP0+33R+VRHP)/SUMRP	PKP1= 3'h0	VINP2
KVP10	VREG1OUT - ΔV*(VRP0+34R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	VREG1OUT - ΔV*(VRP0+35R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	VREG1OUT - ΔV*(VRP0+36R+VRHP)/SUMRP	PKP1= 3'h3	
KVP13	VREG1OUT - ΔV*(VRP0+37R+VRHP)/SUMRP	PKP1= 3'h4	
KVP14	VREG1OUT - ΔV*(VRP0+38R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	VREG1OUT - ΔV*(VRP0+39R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	VREG1OUT - ΔV*(VRP0+40R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	VREG1OUT - ΔV*(VRP0+45R+VRHP)/SUMRP	PKP2= 3'h0	VINP3
KVP18	VREG1OUT - ΔV*(VRP0+46R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	VREG1OUT - ΔV*(VRP0+47R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	VREG1OUT - ΔV*(VRP0+48R+VRHP)/SUMRP	PKP2= 3'h3	
KVP21	VREG1OUT - ΔV*(VRP0+49R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	VREG1OUT - ΔV*(VRP0+50R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	VREG1OUT - ΔV*(VRP0+51R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	VREG1OUT - ΔV*(VRP0+52R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	VREG1OUT - ΔV*(VRP0+68R+VRHP)/SUMRP	PKP3= 3'h0	VINP4
KVP26	VREG1OUT - ΔV*(VRP0+69R+VRHP)/SUMRP	PKP3= 3'h1	
KVP27	VREG1OUT - ΔV*(VRP0+70R+VRHP)/SUMRP	PKP3= 3'h2	
KVP28	VREG1OUT - ΔV*(VRP0+71R+VRHP)/SUMRP	PKP3= 3'h3	
KVP29	VREG1OUT - ΔV*(VRP0+72R+VRHP)/SUMRP	PKP3= 3'h4	
KVP30	VREG1OUT - ΔV*(VRP0+73R+VRHP)/SUMRP	PKP3= 3'h5	
KVP31	VREG1OUT - ΔV*(VRP0+74R+VRHP)/SUMRP	PKP3= 3'h6	
KVP32	VREG1OUT - ΔV*(VRP0+75R+VRHP)/SUMRP	PKP3= 3'h7	
KVP33	VREG1OUT - ΔV*(VRP0+80R+VRHP)/SUMRP	PKP4= 3'h0	VINP5
KVP34	VREG1OUT - ΔV*(VRP0+81R+VRHP)/SUMRP	PKP4= 3'h1	
KVP35	VREG1OUT - ΔV*(VRP0+82R+VRHP)/SUMRP	PKP4= 3'h2	
KVP36	VREG1OUT - ΔV*(VRP0+83R+VRHP)/SUMRP	PKP4= 3'h3	
KVP37	VREG1OUT - ΔV*(VRP0+84R+VRHP)/SUMRP	PKP4= 3'h4	
KVP38	VREG1OUT - ΔV*(VRP0+85R+VRHP)/SUMRP	PKP4= 3'h5	
KVP39	VREG1OUT - ΔV*(VRP0+86R+VRHP)/SUMRP	PKP4= 3'h6	
KVP40	VREG1OUT - ΔV*(VRP0+87R+VRHP)/SUMRP	PKP4= 3'h7	
KVP41	VREG1OUT - ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP5= 3'h0	VINP6
KVP42	VREG1OUT - ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	VREG1OUT - ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	VREG1OUT - ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP5= 3'h3	
KVP45	VREG1OUT - ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP5= 3'h4	
KVP46	VREG1OUT - ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP5= 3'h5	
KVP47	VREG1OUT - ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP5= 3'h6	
KVP48	VREG1OUT - ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP5= 3'h7	
KVP49	VREG1OUT - ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors =128R+VRHP+VRLP+VRP0+VRP1

ΔV : Difference in electrical potential between VREG1OUT and VGS

Table 87 Formula for calculating voltage (IPS=1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV*(VRP0+5R)/SUMRP	PKP0= 3'h0	
KVP2	VREG1OUT - ΔV*(VRP0+9R)/SUMRP	PKP0= 3'h1	
KVP3	VREG1OUT - ΔV*(VRP0+13R)/SUMRP	PKP0= 3'h2	
KVP4	VREG1OUT - ΔV*(VRP0+17R)/SUMRP	PKP0= 3'h3	VINP1
KVP5	VREG1OUT - ΔV*(VRP0+21R)/SUMRP	PKP0= 3'h4	
KVP6	VREG1OUT - ΔV*(VRP0+25R)/SUMRP	PKP0= 3'h5	
KVP7	VREG1OUT - ΔV*(VRP0+29R)/SUMRP	PKP0= 3'h6	
KVP8	VREG1OUT - ΔV*(VRP0+33R)/SUMRP	PKP0= 3'h7	
KVP9	VREG1OUT - ΔV*(VRP0+33R+VRHP)/SUMRP	PKP1= 3'h0	
KVP10	VREG1OUT - ΔV*(VRP0+34R+VRHP)/SUMRP	PKP1= 3'h1	
KVP11	VREG1OUT - ΔV*(VRP0+35R+VRHP)/SUMRP	PKP1= 3'h2	
KVP12	VREG1OUT - ΔV*(VRP0+36R+VRHP)/SUMRP	PKP1= 3'h3	VINP2
KVP13	VREG1OUT - ΔV*(VRP0+37R+VRHP)/SUMRP	PKP1= 3'h4	
KVP14	VREG1OUT - ΔV*(VRP0+38R+VRHP)/SUMRP	PKP1= 3'h5	
KVP15	VREG1OUT - ΔV*(VRP0+39R+VRHP)/SUMRP	PKP1= 3'h6	
KVP16	VREG1OUT - ΔV*(VRP0+40R+VRHP)/SUMRP	PKP1= 3'h7	
KVP17	VREG1OUT - ΔV*(VRP0+61R+VRHP)/SUMRP	PKP2= 3'h0	
KVP18	VREG1OUT - ΔV*(VRP0+62R+VRHP)/SUMRP	PKP2= 3'h1	
KVP19	VREG1OUT - ΔV*(VRP0+63R+VRHP)/SUMRP	PKP2= 3'h2	
KVP20	VREG1OUT - ΔV*(VRP0+64R+VRHP)/SUMRP	PKP2= 3'h3	VINP3
KVP21	VREG1OUT - ΔV*(VRP0+65R+VRHP)/SUMRP	PKP2= 3'h4	
KVP22	VREG1OUT - ΔV*(VRP0+66R+VRHP)/SUMRP	PKP2= 3'h5	
KVP23	VREG1OUT - ΔV*(VRP0+67R+VRHP)/SUMRP	PKP2= 3'h6	
KVP24	VREG1OUT - ΔV*(VRP0+68R+VRHP)/SUMRP	PKP2= 3'h7	
KVP25	VREG1OUT - ΔV*(VRP0+100R+VRHP)/SUMRP	PKP3= 3'h0	
KVP26	VREG1OUT - ΔV*(VRP0+101R+VRHP)/SUMRP	PKP3= 3'h1	
KVP27	VREG1OUT - ΔV*(VRP0+102R+VRHP)/SUMRP	PKP3= 3'h2	
KVP28	VREG1OUT - ΔV*(VRP0+103R+VRHP)/SUMRP	PKP3= 3'h3	VINP4
KVP29	VREG1OUT - ΔV*(VRP0+104R+VRHP)/SUMRP	PKP3= 3'h4	
KVP30	VREG1OUT - ΔV*(VRP0+105R+VRHP)/SUMRP	PKP3= 3'h5	
KVP31	VREG1OUT - ΔV*(VRP0+106R+VRHP)/SUMRP	PKP3= 3'h6	
KVP32	VREG1OUT - ΔV*(VRP0+107R+VRHP)/SUMRP	PKP3= 3'h7	
KVP33	VREG1OUT - ΔV*(VRP0+128R+VRHP)/SUMRP	PKP4= 3'h0	
KVP34	VREG1OUT - ΔV*(VRP0+129R+VRHP)/SUMRP	PKP4= 3'h1	
KVP35	VREG1OUT - ΔV*(VRP0+130R+VRHP)/SUMRP	PKP4= 3'h2	
KVP36	VREG1OUT - ΔV*(VRP0+131R+VRHP)/SUMRP	PKP4= 3'h3	VINP5
KVP37	VREG1OUT - ΔV*(VRP0+132R+VRHP)/SUMRP	PKP4= 3'h4	
KVP38	VREG1OUT - ΔV*(VRP0+133R+VRHP)/SUMRP	PKP4= 3'h5	
KVP39	VREG1OUT - ΔV*(VRP0+134R+VRHP)/SUMRP	PKP4= 3'h6	
KVP40	VREG1OUT - ΔV*(VRP0+135R+VRHP)/SUMRP	PKP4= 3'h7	
KVP41	VREG1OUT - ΔV*(VRP0+135R+VRHP+VRLP)/SUMRP	PKP5= 3'h0	
KVP42	VREG1OUT - ΔV*(VRP0+139R+VRHP+VRLP)/SUMRP	PKP5= 3'h1	
KVP43	VREG1OUT - ΔV*(VRP0+143R+VRHP+VRLP)/SUMRP	PKP5= 3'h2	
KVP44	VREG1OUT - ΔV*(VRP0+147R+VRHP+VRLP)/SUMRP	PKP5= 3'h3	VINP6
KVP45	VREG1OUT - ΔV*(VRP0+151R+VRHP+VRLP)/SUMRP	PKP5= 3'h4	
KVP46	VREG1OUT - ΔV*(VRP0+155R+VRHP+VRLP)/SUMRP	PKP5= 3'h5	
KVP47	VREG1OUT - ΔV*(VRP0+159R+VRHP+VRLP)/SUMRP	PKP5= 3'h6	
KVP48	VREG1OUT - ΔV*(VRP0+163R+VRHP+VRLP)/SUMRP	PKP5= 3'h7	
KVP49	VREG1OUT - ΔV*(VRP0+168R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors =176R+VRHP+VRLP+VRP0+VRP1

ΔV : Difference in electrical potential between VREG1OUT and VGS

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Table 88 Formula for calculating voltage

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	VINP4+(VINP3-VINP4)*(11/23)
V1	VINP1	V33	VINP4+(VINP3-VINP4)*(10/23)
V2	VINP2+(VINP1-VINP2)*(30/48)	V34	VINP4+(VINP3-VINP4)*(9/23)
V3	VINP2+(VINP1-VINP2)*(23/48)	V35	VINP4+(VINP3-VINP4)*(8/23)
V4	VINP2+(VINP1-VINP2)*(16/48)	V36	VINP4+(VINP3-VINP4)*(7/23)
V5	VINP2+(VINP1-VINP2)*(12/48)	V37	VINP4+(VINP3-VINP4)*(6/23)
V6	VINP2+(VINP1-VINP2)*(8/48)	V38	VINP4+(VINP3-VINP4)*(5/23)
V7	VINP2+(VINP1-VINP2)*(4/48)	V39	VINP4+(VINP3-VINP4)*(4/23)
V8	VINP2	V40	VINP4+(VINP3-VINP4)*(3/23)
V9	VINP3+(VINP2-VINP3)*(22/24)	V41	VINP4+(VINP3-VINP4)*(2/23)
V10	VINP3+(VINP2-VINP3)*(20/24)	V42	VINP4+(VINP3-VINP4)*(1/23)
V11	VINP3+(VINP2-VINP3)*(18/24)	V43	VINP4
V12	VINP3+(VINP2-VINP3)*(16/24)	V44	VINP5+(VINP4-VINP5)*(22/24)
V13	VINP3+(VINP2-VINP3)*(14/24)	V45	VINP5+(VINP4-VINP5)*(20/24)
V14	VINP3+(VINP2-VINP3)*(12/24)	V46	VINP5+(VINP4-VINP5)*(18/24)
V15	VINP3+(VINP2-VINP3)*(10/24)	V47	VINP5+(VINP4-VINP5)*(16/24)
V16	VINP3+(VINP2-VINP3)*(8/24)	V48	VINP5+(VINP4-VINP5)*(14/24)
V17	VINP3+(VINP2-VINP3)*(6/24)	V49	VINP5+(VINP4-VINP5)*(12/24)
V18	VINP3+(VINP2-VINP3)*(4/24)	V50	VINP5+(VINP4-VINP5)*(10/24)
V19	VINP3+(VINP2-VINP3)*(2/24)	V51	VINP5+(VINP4-VINP5)*(8/24)
V20	VINP3	V52	VINP5+(VINP4-VINP5)*(6/24)
V21	VINP4+(VINP3-VINP4)*(22/23)	V53	VINP5+(VINP4-VINP5)*(4/24)
V22	VINP4+(VINP3-VINP4)*(21/23)	V54	VINP5+(VINP4-VINP5)*(2/24)
V23	VINP4+(VINP3-VINP4)*(20/23)	V55	VINP5
V24	VINP4+(VINP3-VINP4)*(19/23)	V56	VINP6+(VINP5-VINP6)*(44/48)
V25	VINP4+(VINP3-VINP4)*(18/23)	V57	VINP6+(VINP5-VINP6)*(40/48)
V26	VINP4+(VINP3-VINP4)*(17/23)	V58	VINP6+(VINP5-VINP6)*(36/48)
V27	VINP4+(VINP3-VINP4)*(16/23)	V59	VINP6+(VINP5-VINP6)*(32/48)
V28	VINP4+(VINP3-VINP4)*(15/23)	V60	VINP6+(VINP5-VINP6)*(25/48)
V29	VINP4+(VINP3-VINP4)*(14/23)	V61	VINP6+(VINP5-VINP6)*(18/48)
V30	VINP4+(VINP3-VINP4)*(13/23)	V62	VINP6
V31	VINP4+(VINP3-VINP4)*(12/23)	V63	VINP7

Note: Make sure DDVDH-V0 > 0.5V

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Relationship between RAM Data and Voltage Output Levels
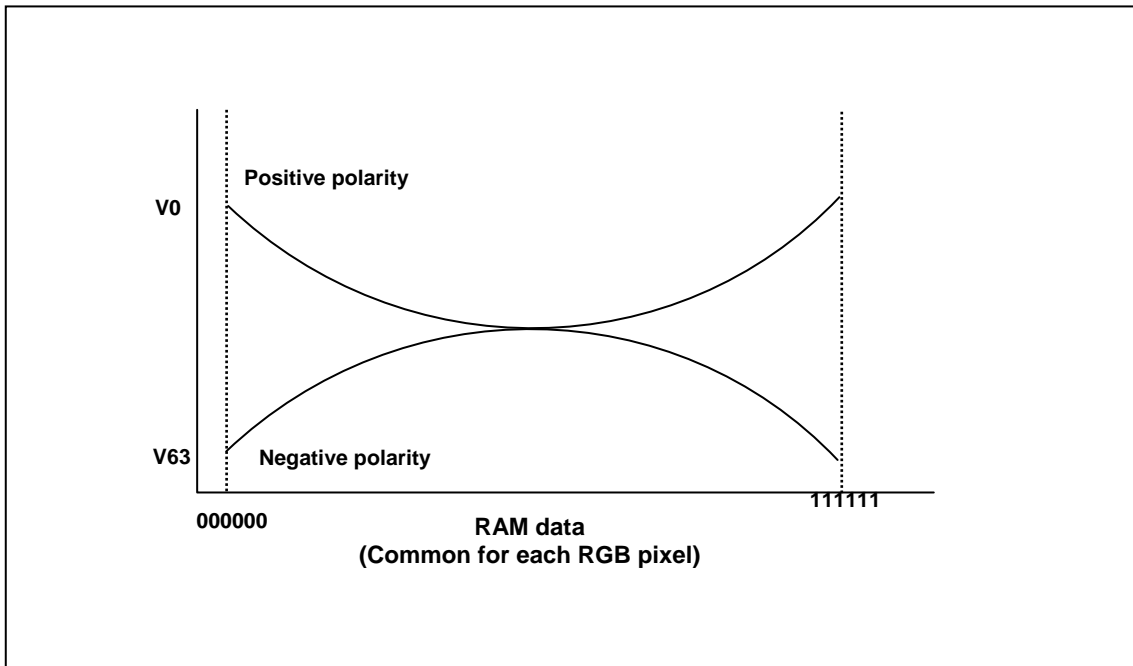The relationship between RAM data and source output voltage levels is as follows..

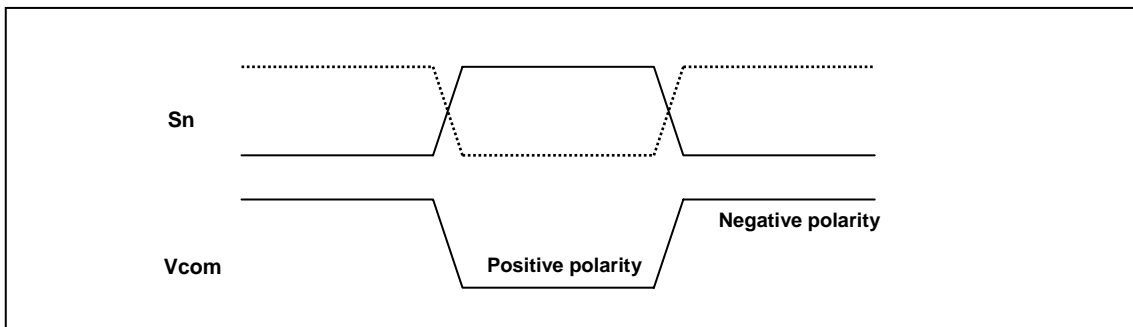
Figure 70 RAM data and the output voltage (REV = "1")

Figure 71 Source output and Vcom

Power-supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the LGDP4531.

Power supply circuit connection example 1 (Vci1 = VciOUT)

In the following example, the VciOUT level is adjusted internally with the VciOUT output circuit.

Figure 72

Note: The wiring resistance between the schottky diode and GND/VGL must be 10Ohm or less.

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Power supply circuit connection example2 (Vci1 = Vci direct input)

In the following example, the electrical Vci is directly applied to Vci1. In this case, the VciOUT level cannot be adjusted internally but step-up operation becomes more effective
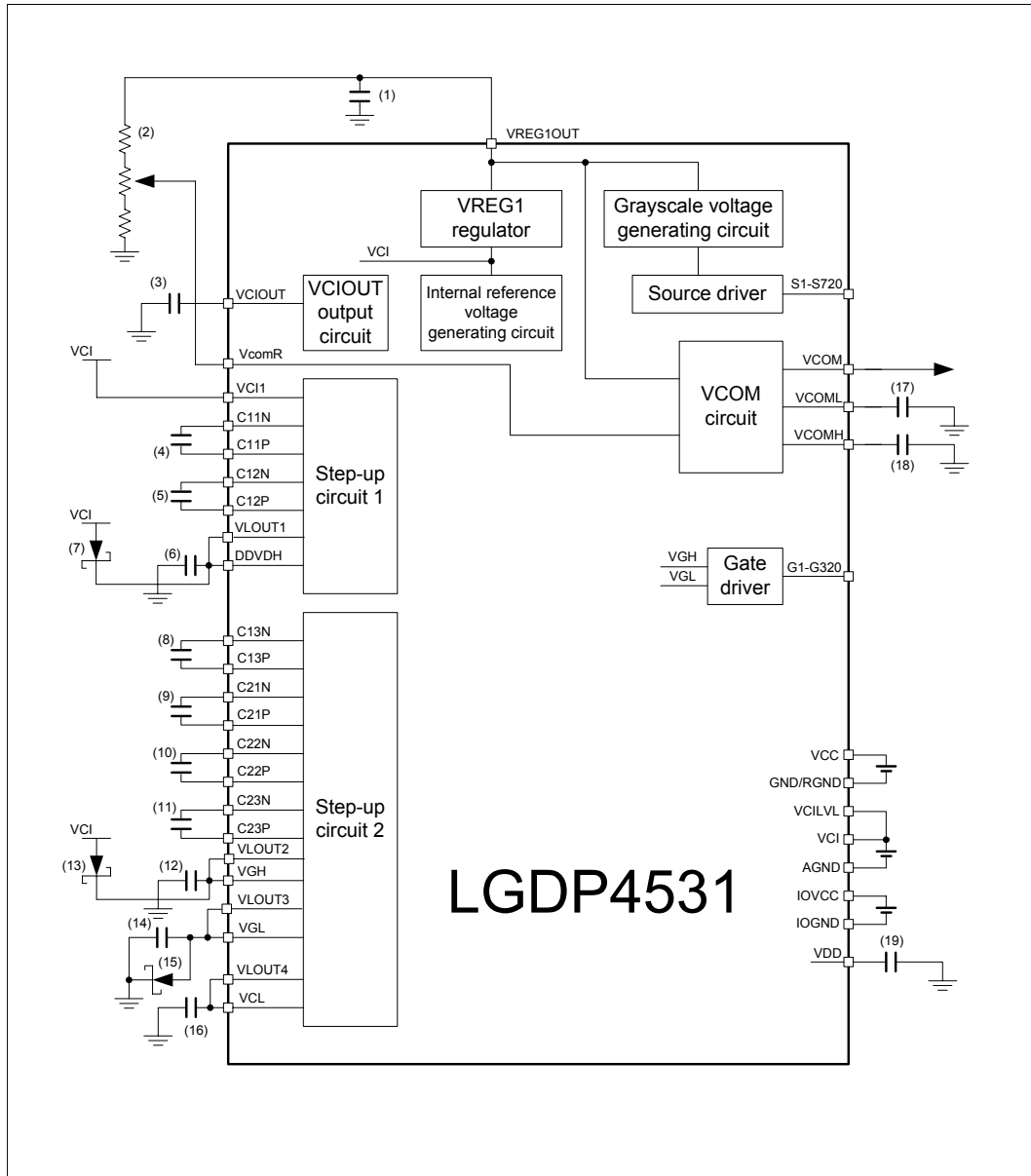
Figure 73

Note: 1. The wiring resistance between the schottky diode and GND/VGL must be 10Ohm or less.
2. When directly applying the Vci level to Vci1, set VC=3'h0.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the LGDP4531 are as follows.

Table 89 Capacitor

Capacitance	Voltage proof	Pin Connection
1uF (B characteristics)	6V	(1)VREG1OUT, (3)VciOUT, (4) C11N/P, (5) C12N/P, (8) C13N/P, (16) VLOUT4, (17) VCOML, (18) VCOMH, (19) VDD
	10V	(6) VLOUT1, (9) C21N/P, (10) C22N/P, (11) C23N/P
	25V	(12) VLOUT2, (14) VLOUT3

Notes: 1. Check with the LC module.
   2. The numbers in the parentheses corresponds to the numbers of the elements in Figure 72, Figure 73.

Table 90 Schottky Diode

Specification	Pin Connection
VF<0.4 V/20 mA@25℃, VR $\geq$ 30V	(7) Vci-DDVDH (15) GND-VGL (13) Vci-VGH

Table 91 Variable Resistor

Specification	Pin Connection
>200kΩ	(2) VcomR

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Voltage Setting Pattern Diagram

The pattern diagram of voltage setting and waveforms of the liquid crystal application voltages are as follows.
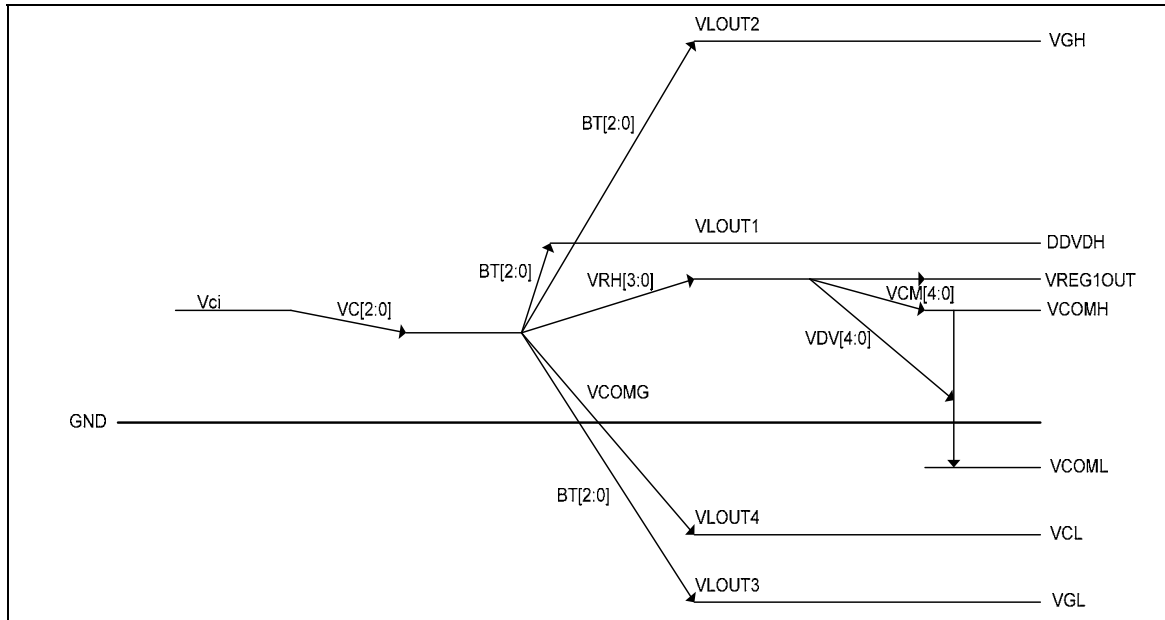
Figure 74 Pattern Diagram for Voltage Setting

Note   Output voltages of DDVDH, VGH, VGL, and VCL drop from setting voltage(idea voltage) depending on the current consumption at output. (DDVDH – VREG1OUT) > 0.5V and (VCOML – VGL) > 0.5V are the relation to the actual voltage. When using the voltage in the large current consumption at the fast VCOM2 cycle(such as line-by-line inversion), check the voltage value

Power Supply Instruction Setting

The following are the sequences for setting power supply ON/OFF. Make power supply ON/OFF settings according to the following sequences in Display ON/OFF, Standby set/exit, Sleep set/exit sequences.

Figure 75

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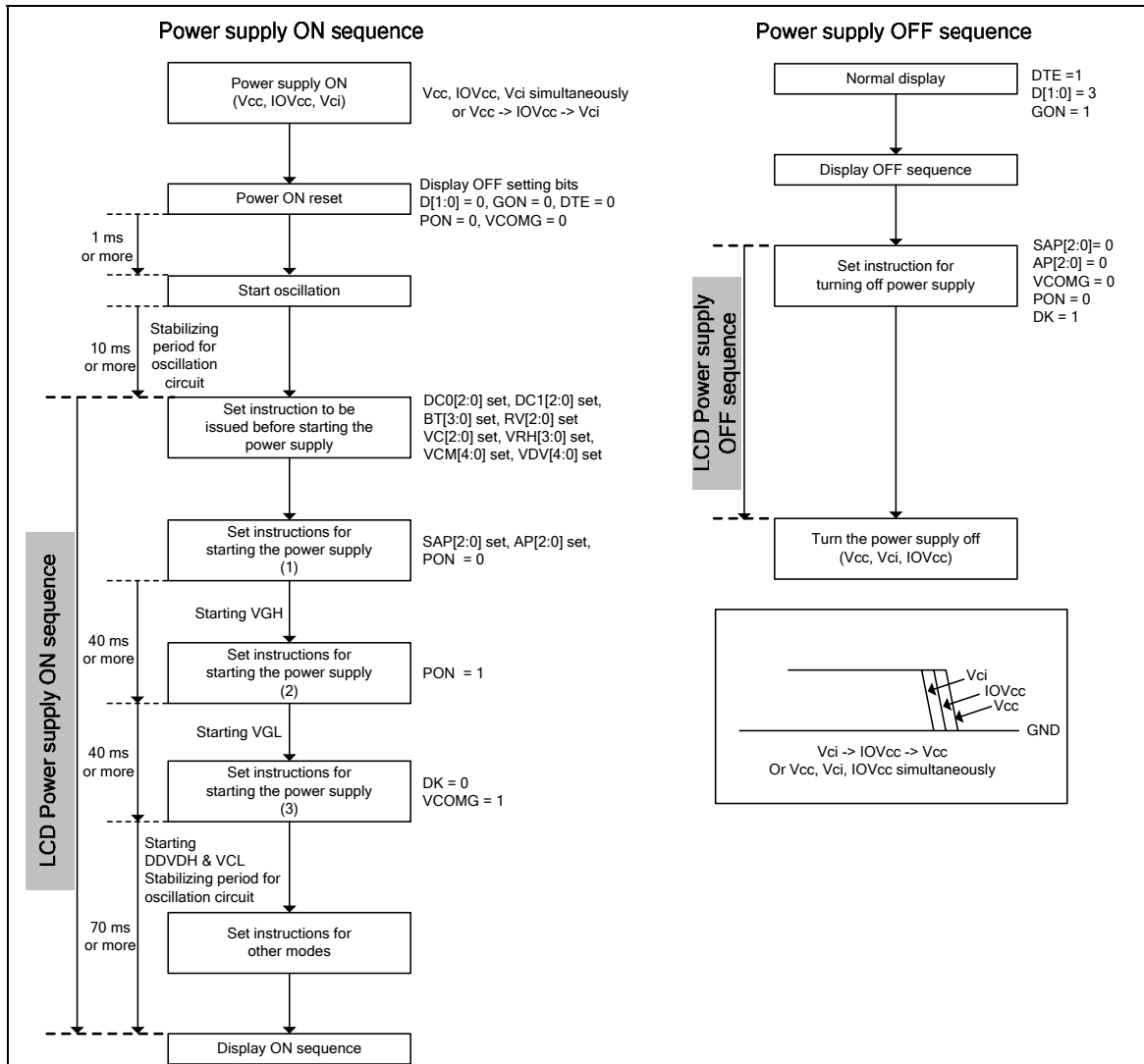
Instruction Setting

The following are the sequences for various instruction settings with the LGDP4531. When making the following instruction settings, follow the respective sequences below.
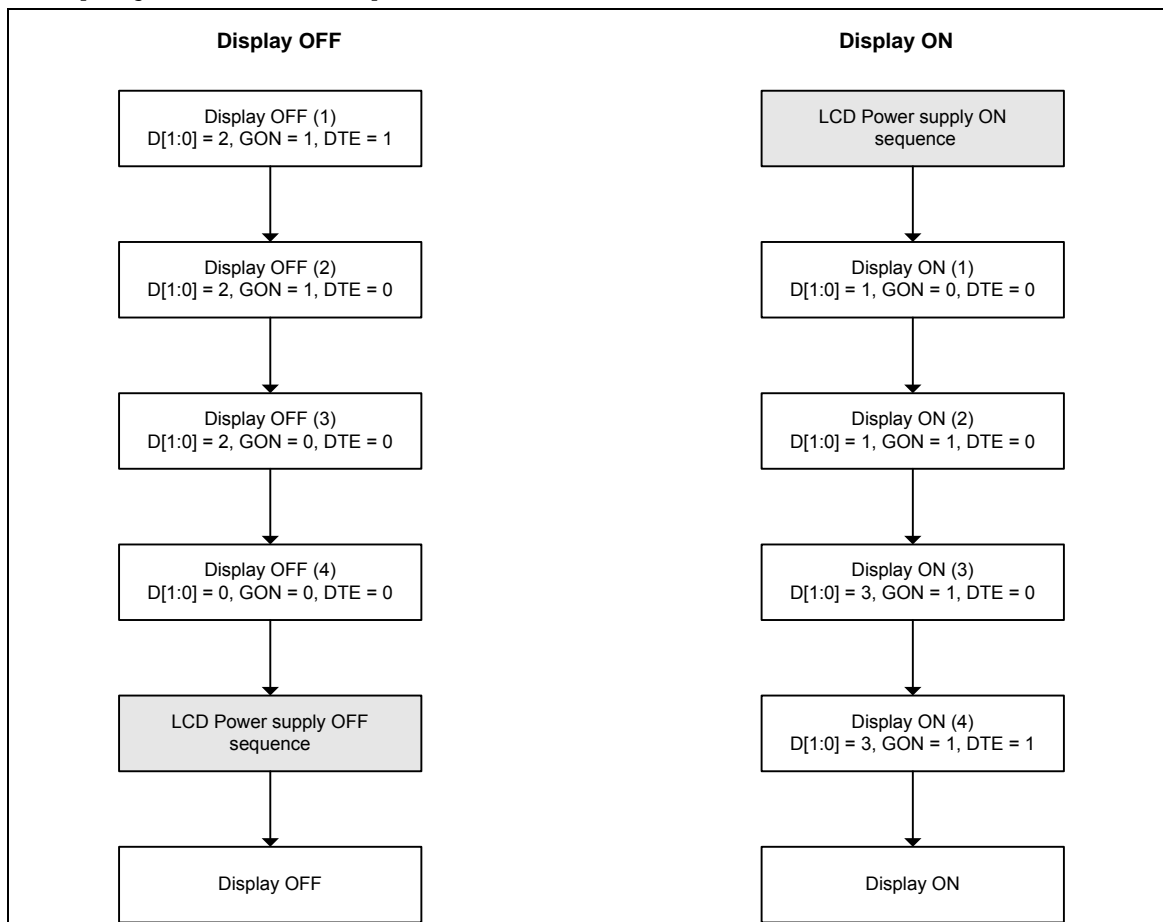
Display ON/OFF sequence

Display OFF	Display ON
Display OFF (1) D[1:0] = 2, GON = 1, DTE = 1	LCD Power supply ON sequence
Display OFF (2) D[1:0] = 2, GON = 1, DTE = 0	Display ON (1) D[1:0] = 1, GON = 0, DTE = 0
Display OFF (3) D[1:0] = 2, GON = 0, DTE = 0	Display ON (2) D[1:0] = 1, GON = 1, DTE = 0
Display OFF (4) D[1:0] = 0, GON = 0, DTE = 0	Display ON (3) D[1:0] = 3, GON = 1, DTE = 0
LCD Power supply OFF sequence	Display ON (4) D[1:0] = 3, GON = 1, DTE = 1
Display OFF	Display ON

Figure 76

Sleep mode SET/EXIT sequences

Sleep mode

Display OFF sequence

Set Sleep mode

Sleep set (SLP = 1)

Sleep release (SLP = 0)

Exit Sleep mode

Display ON sequence

Figure 77

LG Electronics
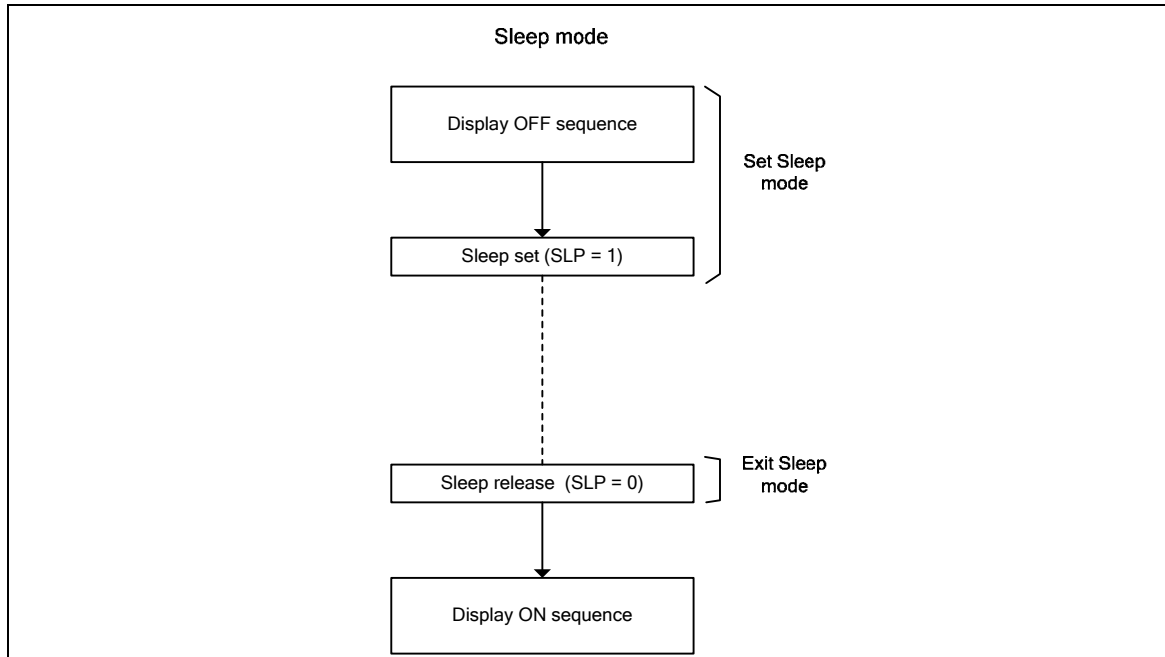
Deep standby mode IN/EXIT sequences
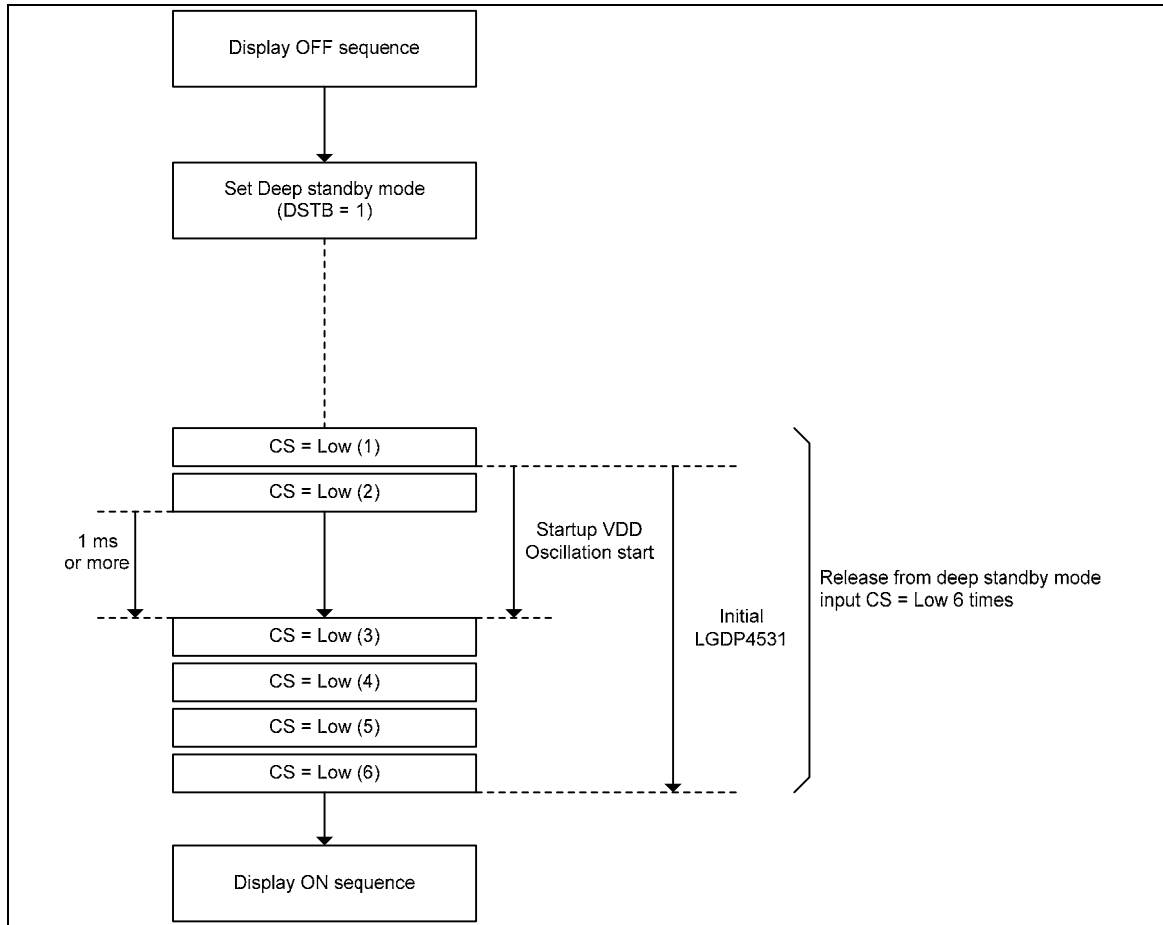
Figure 78

8-color mode setting

Figure 79

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Parital Display setting

Partial display setting sequence

Full-screen display

Partial display setting
R80h : PTDP0
R81h : PTSA0
R82h : PTEA0
R83h : PTDP1
R84h : PTSA1
R85h : PTEA1

Base image display OFF
Partial display ON
R07h : BASEE =0 , PTDE = 1

8 color display, low power
Consumption settings

R07h : COL = 1 ,
R09h : PTS

Set as required

Partial display

Base image display ON
Partial display OFF
R07h : BASEE =1 , PTDE = 0

Full-screen display

Figure 80

Absolute Maximum Ratings

Table 92

Item	Symbol	Unit	value	Notes
Power supply voltage (1)	Vcc, IOVcc	V	-0.3 ~ +4.5	1, 2
Power supply voltage (2)	Vci – AGND	V	-0.3 ~ +4.5	1, 3
Power supply voltage (3)	DDVDH – AGND	V	-0.3 ~ +8.0	1, 4
Power supply voltage (4)	AGND – VCL	V	-0.3 ~ +4.5	1
Power supply voltage (5)	DDVDH –VCL	V	-0.3 ~ +8.0	1, 5
Power supply voltage (6)	VGH – AGND	V	-0.3 ~ +18	1, 6
Power supply voltage (7)	AGND – VGL	V	-0.3 ~ +18	1, 7
Input voltage	Vt	V	-0.3~IOVcc+0.3	1
Operating temperature	Topr	˚C	-40 ~ +85	1, 8
Storage temperature	Tstg	˚C	-55 ~ +125	1

Note 1) If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.
Note 2) Make sure (High) Vcc $\geq$ GND (Low), (High) IOVcc $\geq$ GND (Low).
Note 3) Make sure (High) Vci $\geq$ GND (Low).
Note 4) Make sure (High) DDVDH $\geq$ AGND (Low).
Note 5) Make sure (High) DDVDH $\geq$ VCL (Low).
Note 6) Make sure (High) VGH $\geq$ AGND (Low).
Note 7) Make sure (High) AGND $\geq$ VGL (Low).
Note 8) The DC/AC characteristics of die and wafer products is guaranteed at 85 ℃.

Electrical Characteristics

DC Characteristics

Table 93

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Notes
Input high-level voltage	V_{IH}	V	IOVcc $= 1.65 \sim 3.3$V	0.8IOVcc		IOVcc	2,3
Input low-level voltage	V_{IL}	V	IOVcc $= 1.65 \sim 3.3$V	0		0.2IOVcc	2,3
Output high-level voltage (1) (DB17-0, SDO, FMARK)	V_{OH1}	V	IOVcc $= 1.65 \sim 3.3$V $I_{OH} = 0.1$mA	0.8IOVcc			2
Output lowlevel voltage (1) (DB17-0, SDO, FMARK)	V_{OL1}	V	IOVcc $= 1.65\sim 3.3$V $I_{OL} = 0.1$mA			0.2IOVcc	2
I/O leakage current	I_{Ii}	μA	Vin $= 0 \sim$ IOVcc	-1		1	4
Current consumption : Deep standby mode	I_{ST}	μA	IOVcc $=$ Vcc $=$ Vci $=$ 2.8V , Ta $\approx 25°$C		1	10	5

80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 94 See Figure 83 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time	Write	t_{CYCW}	ns	50		
	Read	t_{CYCW}	ns	250		
Write "Low" level pulse width Read "Low" level pulse width	Write	PW_{LW}	ns	25		
	Read	PW_{LR}	ns	150		
Write "High" level pulse width Read "High" level pulse width	Write	PW_{HW}	ns	25		
	Read	PW_{HR}	ns	100		
Write/Read rise/fall time		t_{WRr} , t_{WRf}	ns			25
Setup time	Write (RS to CS*/ WR*)	t_{AS}	ns	0		
	Read (RS to CS*/ RD*)			10		
Address hold time		t_{AH}	ns	2		
Write data setup time		t_{DSW}	ns	25		
Write data hold time		t_{H}	ns	5		
Read data delay time		t_{DDR}	ns			200
Read data hold time		t_{DHR}	ns	5		

80-System Bus Interface Timing Characteristics (8/9-Bit Bus)

Table 95 See Figure 83 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item			Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time		Write	t_{CYCW}	ns	40		
		Read	t_{CYCW}	ns	250		
Write "Low" level pulse width		Write	PW_{LW}	ns	20		
Read "Low" level pulse width		Read	PW_{LR}	ns	150		
Write "High" level pulse width		Write	PW_{HW}	ns	25		
Read "High" level pulse width		Read	PW_{HR}	ns	100		
Write/Read rise/fall time			t_{WRr} , t_{WRf}	ns			25
Setup time	Write (RS to CS*/ WR*)		t_{AS}	ns	0		
	Read (RS to CS*/ RD*)				10		
Address hold time			t_{AH}	ns	2		
Write data setup time			t_{DSW}	ns	25		
Write data hold time			t_{H}	ns	5		
Read data delay time			t_{DDR}	ns			200
Read data hold time			t_{DHR}	ns	5		

Serial Peripheral Interface Timing Characteristics

Table 96 See Figure 84 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	50		
	Read (transmitted)	t_{SCYC}	ns	250		
Serial clock "High" level pulse width	Write (received)	t_{SCH}	ns	25		
	Read (transmitted)	t_{SCH}	ns	150		
Serial clock "Low" level pulse width	Write (received)	t_{SCL}	ns	25		
	Read (transmitted)	t_{SCL}	ns	100		
Serial clock rise/fall time		t_{scr} , t_{scf}	ns			20
Chip select setup time		t_{CSU}	ns	20		
Chip select hold time		t_{CH}	ns	60		
Serial input data setup time		t_{SISU}	ns	30		
Serial input data hold time		t_{SIH}	ns	30		
Serial output data delay time		t_{SOD}	ns			130
Serial output data hold time		t_{SOH}	ns	5		

RGB Interface Timing Characteristics

Table 97 See Figure 85 (18/16-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	ns	0		
ENABLE setup time	tENS	ns	10		
ENABLE hold time	tENH	ns	20		
DOTCLK "Low" level pulse width	PWDL	ns	25		
DOTCLK "High" level pulse width	PWDH	ns	25		
DOTCLK cycle time	tCYCD	ns	50		
Data setup time	tPDS	ns	10		
Data hold time	tPDH	ns	25		
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns			25

Reset Timing Characteristics

Table 98 See Figure 86 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset "Low" level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	us	-	-	10

LCD Driver Output Characteristics

Table 99 See Figure 87

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Driver output delay time	t_{DD}	us	Vcc=3.0V, DDVDH=5.5V, VREG1OUT=5.0V, RC oscillation: fosc =2.5MHz (driving 320 lines), Ta=25°C REV=0, SAP=010, AP=010, VRNx=5h'0, VRPx=5h'0, PKPx=3h'0, PKNx=3h'0, PRPx=3h'0, PRNx=3h'0, All pins undergo same changes from a same gray level. Time to reach ±35mV during VCOM polarity inversion. Load resistance R=10kΩ, Load capacitance C=20pF	-	T.B.D	-

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
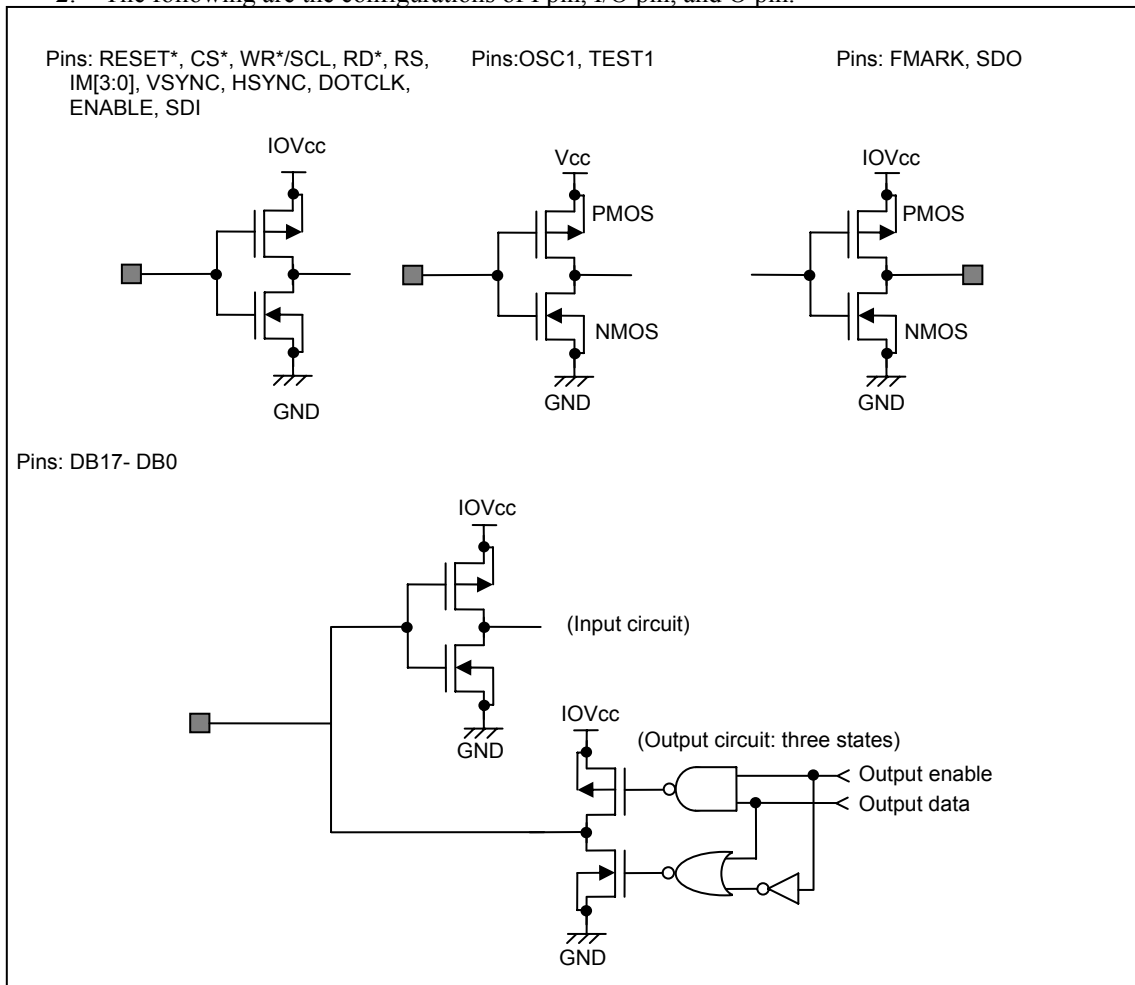2. The following are the configurations of I pin, I/O pin, and O pin.

Figure 81

3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the IOVcc level.
4. This excludes currents though the output drive MOS.
5. This excludes currents flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CS* pin is set to "High" or "Low".
6. This is the case when an external oscillation resistor Rf is used.
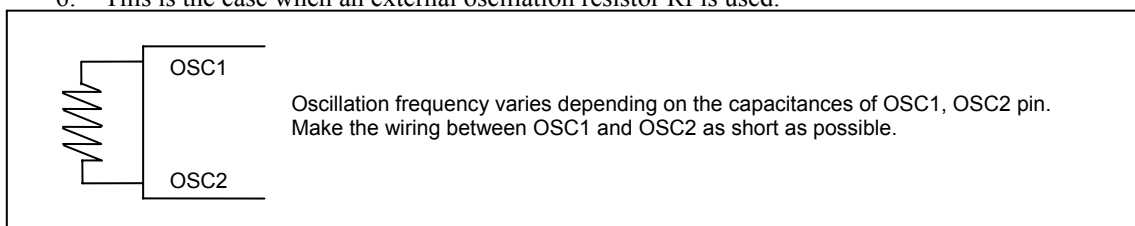
Figure 82

Table 100 RC Oscillation Frequency, Ta=25°C

Oscillation Resistance (kΩ)	RC Oscillation Frequency : fosc (MHz)		
	@ VCI = 2.8V , R15h=16'h0230		
	Min.	Typ.	Max.
5.1	5.9	6.9	8.0
5.6	5.6	6.6	7.6
6.8	5.0	5.9	6.8
8.2	4.4	5.2	6.0
10	3.9	4.6	5.2
12	3.4	4.0	4.6
15	2.8	3.3	3.8
18	2.4	2.9	3.3
22	2.1	2.4	2.8
27	1.7	2.0	2.3
33	1.5	1.7	2.0
39	1.2	1.5	1.7
47	1.0	1.2	1.4

Timing characteristic diagram

Note 1) PWLW and PWLR are defined by the overlap period when CS* is "Low" and WR* or RD* is "Low".
Note 2) Unused DB pins must be fixed at "IOVCC" or "GND".
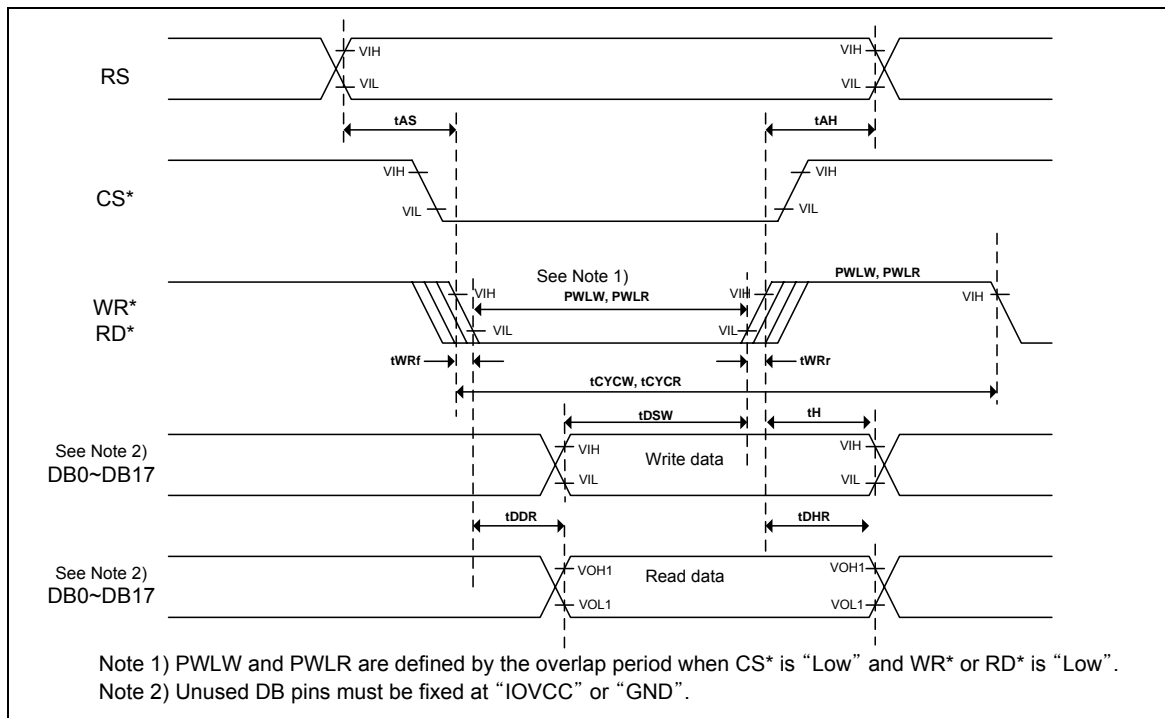
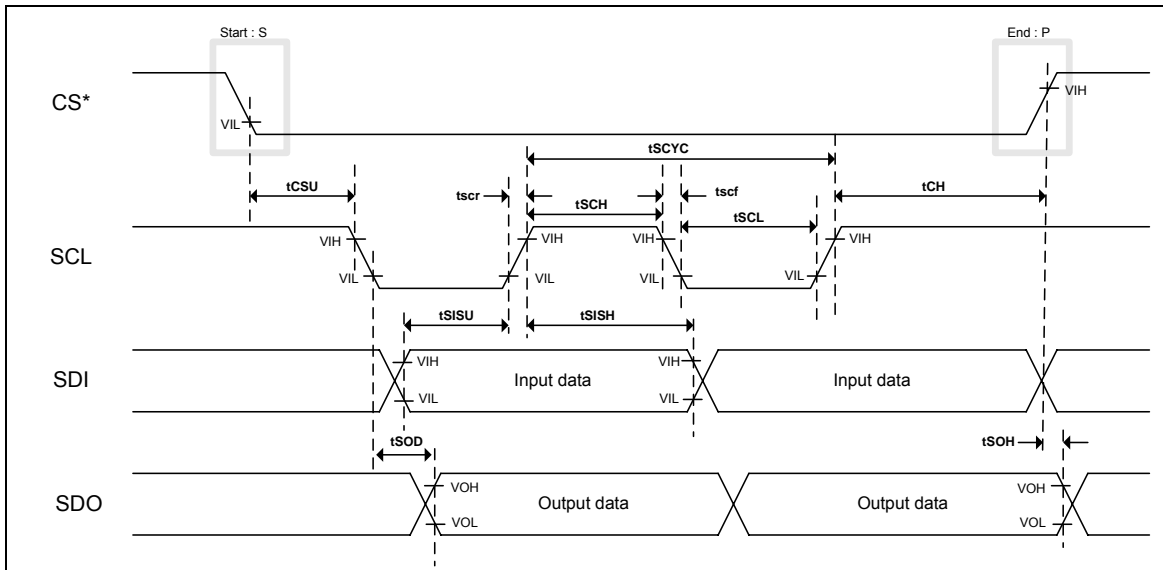**Figure 83 80-system bus interface operation**

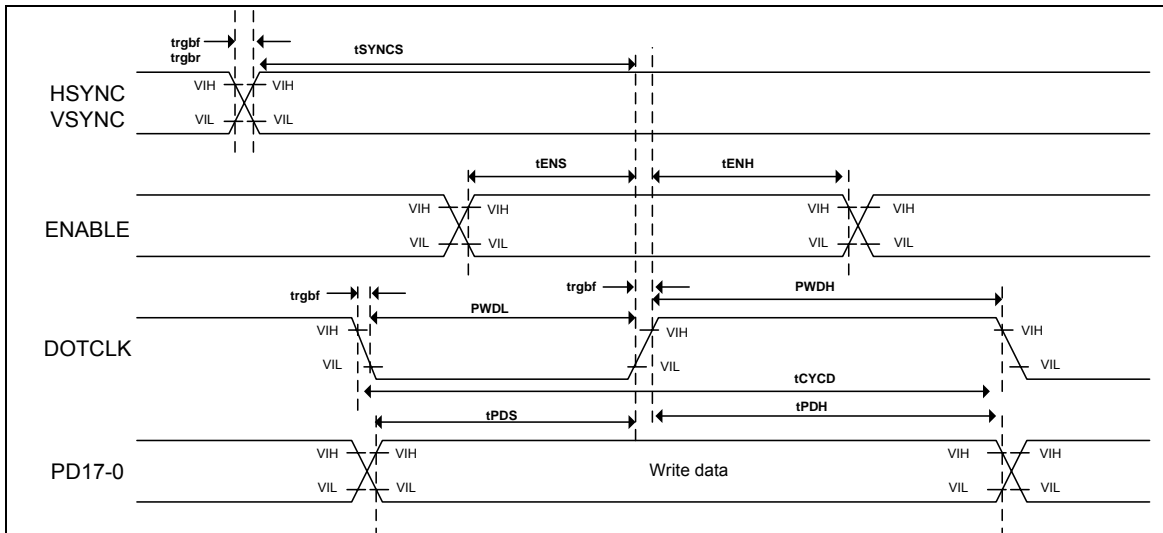**Figure 84 Serial Peripheral interface operation**

Figure 85 RGB interface operation

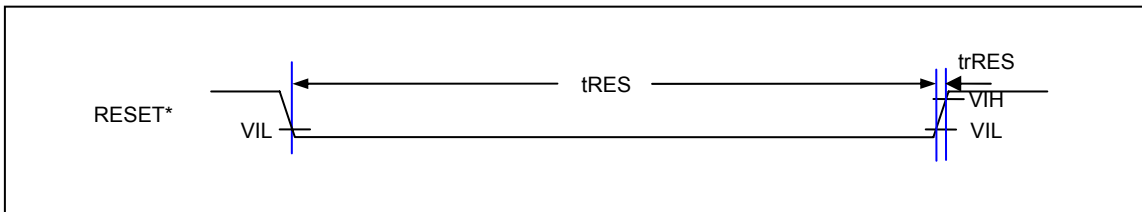**Figure 86 Reset operation**
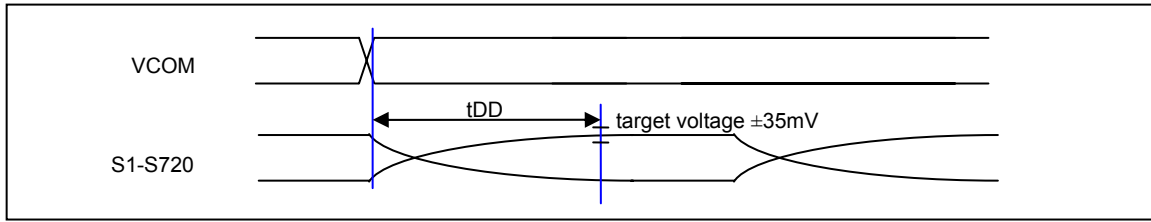
Figure 87 LCD driver outputs

Revision History

Rev.	Date	Revision Description	Revised by
1.13	2007.04.28	p.150 Added RC-oscillation Frequecny : Table 100	D.H. Kim
1.14	2007.06.15	p.22~27 Modified system interface : Figure 2, 3, 4, 6	S.H. Koh
1.14	2007.06.15	p.33, 84 65k colors → 262k colors (3-transfers mode) : Table 7, Figure 25	S.H. Koh
1.14	2007.06.15	p.119 Corrected alternating signal for frame inversion : Figure 60	S.H. Koh
1.15	2007.07.03	p.7 Added descriptions of RS & FMARK pins when not in use : Table 1	S.M. Kim
1.15	2007.07.03	p.126 PRP/N0 → PRP/N1 : Figure 66	D.H. Kim
1.15	2007.07.03	p.11 Revised the Pad Arrangement	D.H. Kim
1.15	2007.07.03	p.142 Erased the "wait clock" on sleep mode sequence : Figure 77	D.H. Kim

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