

# LGDP4535

## 720-Channel, 262,144-Color One-Chip Driver with RAM, Power Supply and Gate Circuits for Amorphous TFT-LCD Panels

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## Description

The LGDP4535 is a one-chip liquid crystal controller driver LSI, comprising RAM of 240 RGB x 320 dots at maximum, a source driver, a gate driver and a power supply circuit. For effective data transfer, the LGDP4535 supports high-speed 8-/9-/16-/18-bit bus interfaces as a system interface to microcomputer and high-speed RAM write mode.

As a moving picture interface, the LGDP4535 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0).

Also, the LGDP4535 incorporates step-up circuits and voltage follower circuits to generate TFT liquid crystal panel drive voltages.

The LGDP4535's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

## Features

- A one-chip controller driver incorporating a gate circuit and a power supply circuit for 240RGB x320 dots graphics display on an amorphous TFT panel in 262k colors
- System interface
  - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
  - Serial interface
- Interface for moving picture display
  - 6-, 16-, 18-bit bus RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  - VSYNC interface (System interface + VSYNC)
  - FMARK interface (System interface + FMARK)
- Window address function to specify a rectangular area on the internal RAM to write data
- Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
  - Resizing function (x 1/2, x 1/4)
- Abundant color display and drawing functions
  - Programmable  $\gamma$ -correction function for 262k-color display
  - Partial display function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Standby, Deep standby, sleep function
  - 8-color display function
  - Input power supply voltages:  $V_{cc} = 2.5V \sim 3.3V$  (logic regulator power supply)  
 $IOV_{cc} = 1.65V \sim 3.3V$  (interface I/O power supply)  
 $V_{ci} = 2.5V \sim 3.3V$  (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/Vcom power supply:  $DDVDH-GND = 4.5V \sim 6.0V$
  - Gate drive power supply:  $VGH-GND = 10.0V \sim 15.0V$   
 $VGL-GND = -4.5V \sim -12.5V$   
 $VGH-VGL \leq 25V$
  - Vcom drive power supply:  $VCOMH = VCI \sim (DDVDH-0.5)V$   
 $VCOML = (VCL+0.5)V \sim 0V$   
 $VCOMH-VCOML$  amplitude = 6.0V (Max.)
- Liquid crystal power supply startup sequence
- TFT storage capacitance: Cst only (common Vcom formula)
- 172,800-byte internal RAM
- Internal 720-channel source driver and 320-channel gate driver
- Configures a COG module with one chip by arranging gate lines on both sides

## Block Diagram

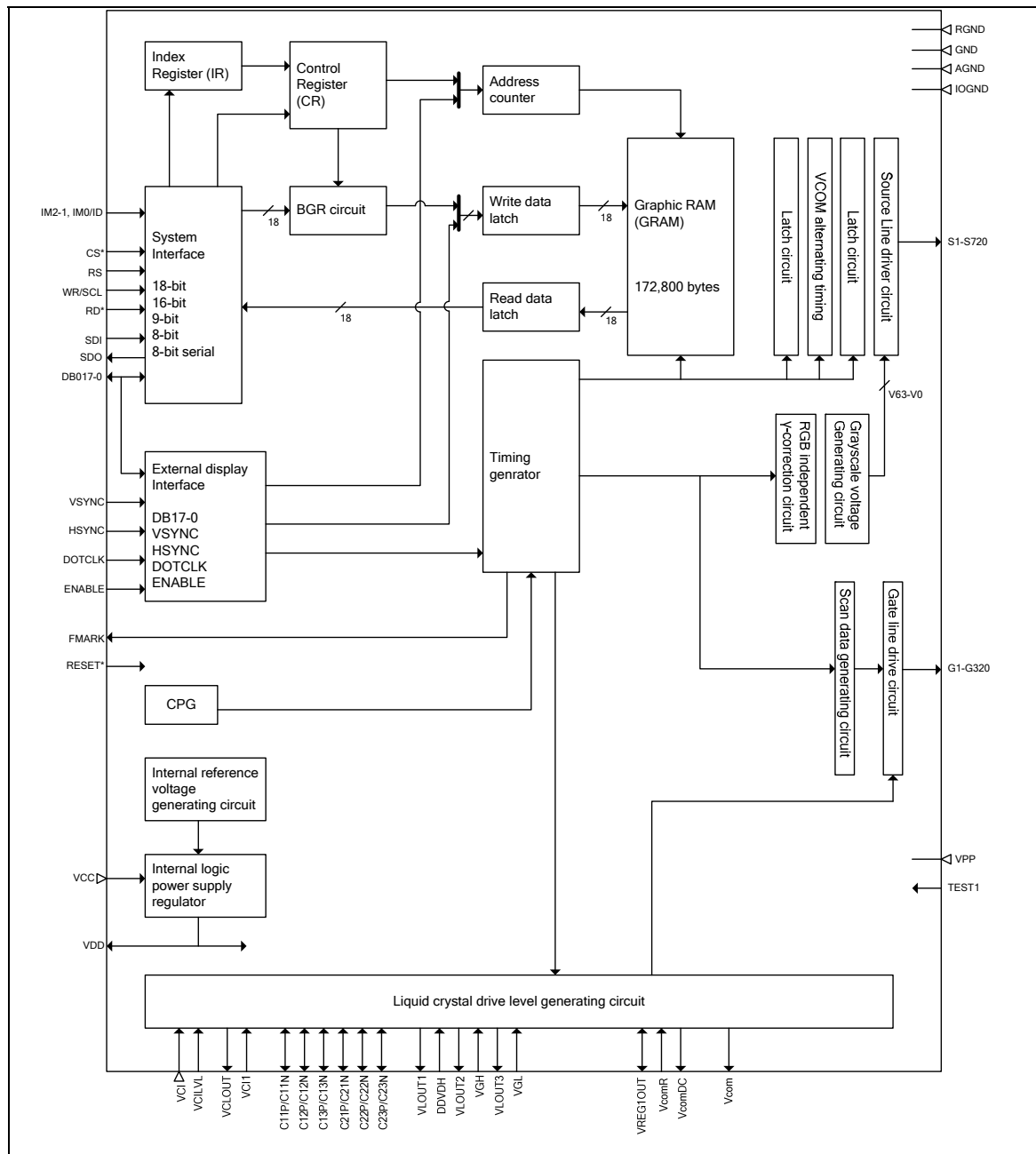


Figure 1

## Pin Function

**Table 1 Interface Pins**

Signal	I/O	Connected to	Function		
IM2-1, IM0/ID	I	GND/IOVCC	Select a mode to interface to an MPU. In SPI mode, the IM0 pin is used to set the ID of device code.		
			IM[3:0]	Interface Mode	DB Pins
			000*	Setting disabled	-
			0010	80-system 16-bit interface	DB[17:10], DB[8:1]
			0011	80-system 8-bit interface	DB[17:10]
			010*	Serial peripheral interface (SPI)	SDI, SDO
			011*	Setting disabled	-
			100*	Setting disabled	-
			1010	80-system 18-bit interface	DB[17:0]
			1011	80-system 9-bit interface	DB[17:9]
11**	Setting disabled	-			
CS*	I	MPU	A chip select signal. Amplitude: IOVCC-GND. Low: LGDP4535 is selected and accessible. High: LGDP4535 is not selected and not accessible. Fix to the IOVCC level when not in use.		
RS	I	MPU	A register select signal. Amplitude: IOVCC-GND. Low: select the index/status register. High: select a control register. In SPI mode, fix to either IOVCC or GND level.		
WR*/SCL	I	MPU	Outputs a write strobe signal in 80-system bus interface mode and enables an operation to write data when the signal is low. In SPI mode, a synchronizing clock signal is output.		
RD*	I	MPU	Outputs a read strobe signal in 80-system bus interface mode and enables an operation to read data when the signal is low. In SPI mode, fix to either IOVCC or GND level.		
SDI	I	MPU	A serial data input (SDI) pin in SPI mode. Data are input on the rising edge of the SCL signal. Fix to either IOVCC or GND level when not in use.		
SDO	O	MPU	A serial data output (SDO) pin in SPI mode. Data are output on the falling edge of the SCL signal. Leave open when not in use.		
DB0 ~ DB17	I/O	MPU	An 18-bit parallel bidirectional data bus. Unused pins must be fixed either IOVCC or GND level.		
ENABLE	I	MPU	A data enable signal in RGB interface mode. Low: Select (accessible) High: Not select (inaccessible) The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVCC or GND level when not in use.		
VSYNC	I	MPU	A frame synchronizing signal. When VSPL = “0”, it is active low. When VSPL = “1”, it is active high. Fix to either IOVCC or GND level when not in use.		

HSYNC	I	MPU	A line synchronizing signal. When HSPL = "0", it is active low. When HSPL = "1", it is active high. Fix to either IOVCC or GND level when not in use.
DOTCLK	I	MPU	A dot clock signal. When DPL = "0", input data on the rising edge of DOTCLK. When DPL = "1", input data on the falling edge of DOTCLK. Fix to either IOVCC or GND level when not in use.
RESET*	I	MPU or External RC circuit	A reset pin. Initializes the LGDP4535 with a low input. Be sure to execute a power-on reset after supplying power.
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal GRAM. Leave open when not in use.

**Table 2 Power Supply Pins**

Signal	I/O	Connected to	Function
VCC	-	Power supply	Power supply to internal logic regulator circuit: $V_{cc} = 2.5V \sim 3.3V$ , $V_{cc} \geq IOV_{cc}$
VCI	-	Power supply	Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
VCILVL	-	Power supply	VCILVL must be at the same electrical potential as VCI. Be sure to connect VCILVL with VCI on the FPC to prevent noise.
IOVCC	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. $IOV_{cc} = 1.65V \sim 3.3V$ . $V_{cc} \geq IOV_{cc}$ . In case of COG, connect to VCC on the FPC if $IOV_{cc} = V_{cc}$ to prevent noise.
VDD VDDOUT	O	Stabilizing capacitor	Internal logic regulator output to be used as a power supply to internal logic. Connect a stabilizing capacitor.
GND	-	Power supply	Internal logic GND : $GND = 0V$
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): $AGND = 0V$ . In case of COG, connect to GND on the FPC to prevent noise.
VPP2	-	Power supply	Power supply pin for EPROM write operation. Connect to GND or open when EPROM is not used.

**Table 3 Step-Up Circuit**

Signal	I/O	Connected to	Function
VCIOUT	O	Stabilizing capacitor, Vci1	Internal reference voltage generated between Vci and GND. The output level is set by instruction (VC).



VCI1	I	VciOUT or Vci	Reference voltage for the step-up circuit 1. Vci1 must be set to a level, which will generate the VLOUT1, VLOUT2 and VLOUT3 levels within the respective setting ranges.
VLOUT1	O	Stabilizing capacitor, DDVDH	Output from the step-up circuit 1, generated from Vci1. The step-up factor for the VLOUT1 level is set by instruction (BT). VLOUT1 = 4.5V ~ 6.0V
DDVDH	I	VLOUT1	Power supply for the source driver liquid crystal drive unit and Vcom drive. Connect to VLOUT1. DDVDH = 4.5V ~ 6.0V
VLOUT2	O	Stabilizing capacitor, VGH	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT2 = max 15.0V
VGH	I	VLOUT2	Liquid crystal drive power supply. Connect to VLOUT2.
VLOUT3	O	Stabilizing capacitor, VGL	Output from the step-up circuit 2, generated from Vci1 and DDVDH. The step-up factor for VLOUT2 is set by instruction (BT). VLOUT3 = min -12.5V
VGL	I	VLOUT3	Liquid crystal drive power supply. Connect to VLOUT3.
VLOUT4	O	Stabilizing capacitor, VCL	A voltage level of Vci1 x (-1) generated in the step-up circuit 2. Connect to a stabilizing capacitor when using the VLOUT4 output.
VCL	I	VLOUT4	Power supply for operating VCOML. Vci1 is multiplied by 1 and output by internal step-up circuit 2. VCL = 0 to -3.3(V)
C11P, C11N C12P, C12N	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 1.
C13P, C13N C21P, C21N C22P, C22N	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 2. Connect capacitors where they are required according to the step-up factor.

**Table 4 LCD Drive**

Signal	I/O	Connected to	Function
VREG1OUT	O	Stabilizing capacitor	Output generated from a reference voltage VciLVL by amplifying by the factor, which is set by instruction (VRH). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 3.0V ~ (DDVDH - 0.5)V
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. Output AC voltage with the amplitude VCOMH and VCOML. The alternating cycle is changeable by register setting. Also Vcom output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	Output for the high level of VCOM. This output voltage is adjusted by an instruction (VCM) setting. VCOMH = 3.0 to (DDVDH - 0.5) (V)
VCOML	O	Stabilizing capacitor	Output for the low level of VCOM. This output voltage is adjusted by an instruction (VDV) setting or fixed to GND by a register (VCOMG) setting. In this case, a capacitor for stabilization is not necessary. VCOML = (VCL + 0.5) to 1 (V)

VCOMR	I	Variable resistor or open	If a variable resistor is used to adjust VCOMH, it is attached to this pin. In this case, use an instruction (VCM) setting to stop the internal digital potentiometer circuit of VCOMH, and insert the variable resistor for use in adjustment of VCOM between VREG1OUT. Leave it open or connect to GND when not in use.
VGS	I	GND	Reference level for grayscale voltage generating circuit.
S1 ~ S720	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal outputs, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S720.
G1 ~ G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level

**Table 5 Others (Test, Dummy Pins)**

Signal	I/O	Connected to	Function
TEST1	I	GND	Test pin. Connect to GND.
TEST2-5	-	-	Test pins. Connect to IOVCC, GND or open when not in use.
TESTO1-14	-	-	Test pins. Connect to GND or open when not in use.
VTEST	-	-	Test pin. Connect to GND or open when not in use.
VREFC	-	-	Test pin. Connect to GND or open when not in use.
VREFD	-	-	Test pin. Connect to GND or open when not in use.
VREF	-	-	Test pin. Connect to GND or open when not in use.
VDDTEST	-	-	Test pin. Connect to GND or open when not in use.
VMON	-	-	Test pin. Connect to GND or open when not in use.
VCIR	-	-	Test pin. Connect to GND or open when not in use.
TSC	-	-	Test pin. Connect to GND or open when not in use.
TS0-8	-	-	Test pin. Connect to GND or open when not in use.
TEVCI2	-	-	Test pin. Connect to GND or open when not in use.
IOVCCDUM1	-	-	Output the IOVCC voltage level. These pins are internally shorted to IOVCC. Use it to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave open.
GNDDUM1-6	-	-	Output the GND voltage level. These pins are internally shorted to GND. Use it to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave open.
AGNDDUM1-7	-	-	Output the GND voltage level. These pins are internally shorted to GND.
VGLDMY1-4	-	-	Output the VGL voltage level. These pins are internally shorted to VGL. Use it to fix the unused gate lines at VGL level.

DUMMYR 1-6	-	-	Short-circuited within the chip for COG contact resistance measurement. DUMMYR pins are short-circuited as below. DUMMYR1 and DUMMYR6 DUMMYR2 and DUMMYR5 DUMMYR3 and DUMMYR4
VPP1	-	-	Test pin. Connect to GND or open when not in use.
VPP3A, 3B, 3C	-	-	Test pins. Connect to GND or open when not in use.

# PAD Arrangement

- Chip size : 18800um x 710um
- Chip thickness : 350um
- PAD Coordination : PAD center
- Coordination origin : Chip center

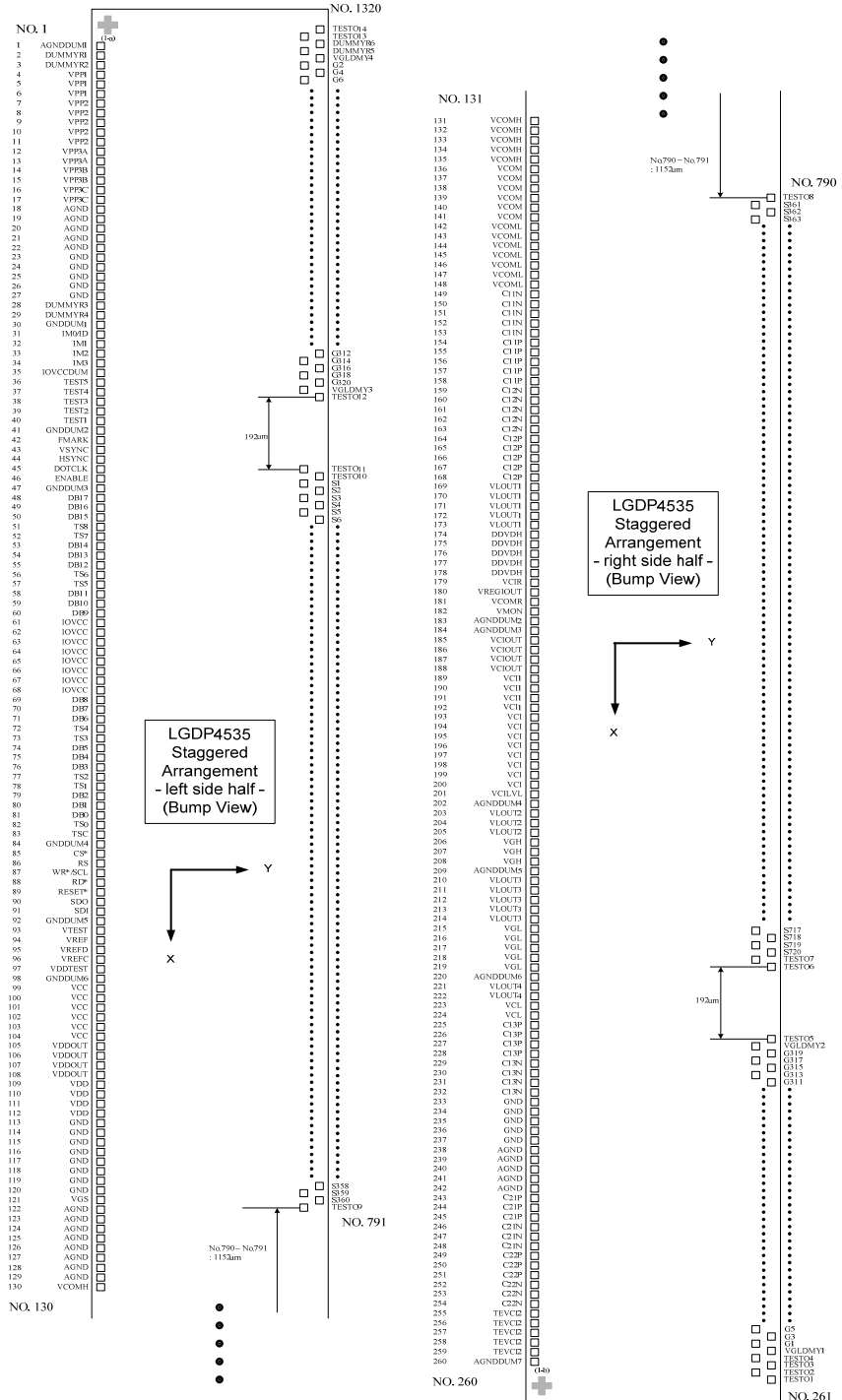
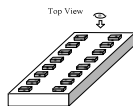
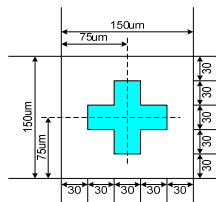
- Au BUMP size
- (1) 50.00um x 80.00um
- No.1 ~ No.260

- (2) 16.00um x 94.00um
- No.261 ~ No.1320

- Au BUMP pitch : see PAD coordination Table
- Au BUMP height : 15um(typ.)
- No. in the figure corresponds to No. in the PAD coordination Table

- Alignment mark

Alignment mark	X	Y
1-a	-9266	-251
1-b	9266	-251



## PAD Coordinate

PAD NO.	PAD NAME	X	Y
1	AGNDDUM1	-9065	-281
2	DUMMYR1	-8995	-281
3	DUMMYR2	-8925	-281
4	VPP1	-8855	-281
5	VPP1	-8785	-281
6	VPP1	-8715	-281
7	VPP2	-8645	-281
8	VPP2	-8575	-281
9	VPP2	-8505	-281
10	VPP2	-8435	-281
11	VPP2	-8365	-281
12	VPP3A	-8295	-281
13	VPP3A	-8225	-281
14	VPP3B	-8155	-281
15	VPP3B	-8085	-281
16	VPP3C	-8015	-281
17	VPP3C	-7945	-281
18	AGND	-7875	-281
19	AGND	-7805	-281
20	AGND	-7735	-281
21	AGND	-7665	-281
22	AGND	-7595	-281
23	GND	-7525	-281
24	GND	-7455	-281
25	GND	-7385	-281
26	GND	-7315	-281
27	GND	-7245	-281
28	DUMMYR3	-7175	-281
29	DUMMYR4	-7105	-281
30	GNDDUM1	-7035	-281
31	IM0/ID	-6965	-281
32	IM1	-6895	-281
33	IM2	-6825	-281
34	IM3	-6755	-281
35	IOVCCDUM	-6685	-281
36	TEST5	-6615	-281
37	TEST4	-6545	-281
38	TEST3	-6475	-281
39	TEST2	-6405	-281
40	TEST1	-6335	-281
41	GNDDUM2	-6265	-281
42	FMARK	-6195	-281
43	VSYNC	-6125	-281
44	HSYNC	-6055	-281
45	DOTCLK	-5985	-281
46	ENABLE	-5915	-281
47	GNDDUM3	-5845	-281
48	DB17	-5775	-281
49	DB16	-5705	-281
50	DB15	-5635	-281

PAD NO.	PAD NAME	X	Y
51	TS8	-5565	-281
52	TS7	-5495	-281
53	DB14	-5425	-281
54	DB13	-5355	-281
55	DB12	-5285	-281
56	TS6	-5215	-281
57	TS5	-5145	-281
58	DB11	-5075	-281
59	DB10	-5005	-281
60	DB9	-4935	-281
61	IOVCC	-4865	-281
62	IOVCC	-4795	-281
63	IOVCC	-4725	-281
64	IOVCC	-4655	-281
65	IOVCC	-4585	-281
66	IOVCC	-4515	-281
67	IOVCC	-4445	-281
68	IOVCC	-4375	-281
69	DB8	-4305	-281
70	DB7	-4235	-281
71	DB6	-4165	-281
72	TS4	-4095	-281
73	TS3	-4025	-281
74	DB5	-3955	-281
75	DB4	-3885	-281
76	DB3	-3815	-281
77	TS2	-3745	-281
78	TS1	-3675	-281
79	DB2	-3605	-281
80	DB1	-3535	-281
81	DB0	-3465	-281
82	TS0	-3395	-281
83	TSC	-3325	-281
84	GNDDUM4	-3255	-281
85	CS*	-3185	-281
86	RS	-3115	-281
87	WR*/SCL	-3045	-281
88	RD*	-2975	-281
89	RESET*	-2905	-281
90	SDO	-2835	-281
91	SDI	-2765	-281
92	GNDDUM5	-2695	-281
93	VTEST	-2625	-281
94	VREF	-2555	-281
95	VREFD	-2485	-281
96	VREFC	-2415	-281
97	VDDTEST	-2345	-281
98	GNDDUM6	-2275	-281
99	VCC	-2205	-281
100	VCC	-2135	-281

PAD NO.	PAD NAME	X	Y
101	VCC	-2065	-281
102	VCC	-1995	-281
103	VCC	-1925	-281
104	VCC	-1855	-281
105	VDDOUT	-1785	-281
106	VDDOUT	-1715	-281
107	VDDOUT	-1645	-281
108	VDDOUT	-1575	-281
109	VDD	-1505	-281
110	VDD	-1435	-281
111	VDD	-1365	-281
112	VDD	-1295	-281
113	GND	-1225	-281
114	GND	-1155	-281
115	GND	-1085	-281
116	GND	-1015	-281
117	GND	-945	-281
118	GND	-875	-281
119	GND	-805	-281
120	GND	-735	-281
121	VGS	-665	-281
122	AGND	-595	-281
123	AGND	-525	-281
124	AGND	-455	-281
125	AGND	-385	-281
126	AGND	-315	-281
127	AGND	-245	-281
128	AGND	-175	-281
129	AGND	-105	-281
130	VCOMH	-35	-281
131	VCOMH	35	-281
132	VCOMH	105	-281
133	VCOMH	175	-281
134	VCOMH	245	-281
135	VCOMH	315	-281
136	VCOM	385	-281
137	VCOM	455	-281
138	VCOM	525	-281
139	VCOM	595	-281
140	VCOM	665	-281
141	VCOM	735	-281
142	VCOML	805	-281
143	VCOML	875	-281
144	VCOML	945	-281
145	VCOML	1015	-281
146	VCOML	1085	-281
147	VCOML	1155	-281
148	VCOML	1225	-281
149	C11N	1295	-281
150	C11N	1365	-281

PAD NO.	PAD NAME	X	Y
151	C11N	1435	-281
152	C11N	1505	-281
153	C11N	1575	-281
154	C11P	1645	-281
155	C11P	1715	-281
156	C11P	1785	-281
157	C11P	1855	-281
158	C11P	1925	-281
159	C12N	1995	-281
160	C12N	2065	-281
161	C12N	2135	-281
162	C12N	2205	-281
163	C12N	2275	-281
164	C12P	2345	-281
165	C12P	2415	-281
166	C12P	2485	-281
167	C12P	2555	-281
168	C12P	2625	-281
169	VLOUT1	2695	-281
170	VLOUT1	2765	-281
171	VLOUT1	2835	-281
172	VLOUT1	2905	-281
173	VLOUT1	2975	-281
174	DDVDH	3045	-281
175	DDVDH	3115	-281
176	DDVDH	3185	-281
177	DDVDH	3255	-281
178	DDVDH	3325	-281
179	VCIR	3395	-281
180	VREG1OUT	3465	-281
181	VCOMR	3535	-281
182	VMON	3605	-281
183	AGNDDUM2	3675	-281
184	AGNDDUM3	3745	-281
185	VCIOUT	3815	-281
186	VCIOUT	3885	-281
187	VCIOUT	3955	-281
188	VCIOUT	4025	-281
189	VCI1	4095	-281
190	VCI1	4165	-281
191	VCI1	4235	-281
192	VCI1	4305	-281
193	VCI	4375	-281
194	VCI	4445	-281
195	VCI	4515	-281
196	VCI	4585	-281
197	VCI	4655	-281
198	VCI	4725	-281
199	VCI	4795	-281
200	VCI	4865	-281

PAD NO.	PAD NAME	X	Y
201	VCILVL	4935	-281
202	AGNDDUM4	5005	-281
203	VLOUT2	5075	-281
204	VLOUT2	5145	-281
205	VLOUT2	5215	-281
206	VGH	5285	-281
207	VGH	5355	-281
208	VGH	5425	-281
209	AGNDDUM5	5495	-281
210	VLOUT3	5565	-281
211	VLOUT3	5635	-281
212	VLOUT3	5705	-281
213	VLOUT3	5775	-281
214	VLOUT3	5845	-281
215	VGL	5915	-281
216	VGL	5985	-281
217	VGL	6055	-281
218	VGL	6125	-281
219	VGL	6195	-281
220	AGNDDUM6	6265	-281
221	VLOUT4	6335	-281
222	VLOUT4	6405	-281
223	VCL	6475	-281
224	VCL	6545	-281
225	C13P	6615	-281
226	C13P	6685	-281
227	C13P	6755	-281
228	C13P	6825	-281
229	C13N	6895	-281
230	C13N	6965	-281
231	C13N	7035	-281
232	C13N	7105	-281
233	GND	7175	-281
234	GND	7245	-281
235	GND	7315	-281
236	GND	7385	-281
237	GND	7455	-281
238	AGND	7525	-281
239	AGND	7595	-281
240	AGND	7665	-281
241	AGND	7735	-281
242	AGND	7805	-281
243	C21P	7875	-281
244	C21P	7945	-281
245	C21P	8015	-281
246	C21N	8085	-281
247	C21N	8155	-281
248	C21N	8225	-281
249	C22P	8295	-281
250	C22P	8365	-281

PAD NO.	PAD NAME	X	Y
251	C22P	8435	-281
252	C22N	8505	-281
253	C22N	8575	-281
254	C22N	8645	-281
255	TEVCI2	8715	-281
256	TEVCI2	8785	-281
257	TEVCI2	8855	-281
258	TEVCI2	8925	-281
259	TEVCI2	8995	-281
260	AGNDDUM7	9065	-281
261	TESTO1	9216	279
262	TESTO2	9200	166
263	TESTO3	9184	279
264	TESTO4	9168	166
265	VGLDMY1	9152	279
266	G1	9136	166
267	G3	9120	279
268	G5	9104	166
269	G7	9088	279
270	G9	9072	166
271	G11	9056	279
272	G13	9040	166
273	G15	9024	279
274	G17	9008	166
275	G19	8992	279
276	G21	8976	166
277	G23	8960	279
278	G25	8944	166
279	G27	8928	279
280	G29	8912	166
281	G31	8896	279
282	G33	8880	166
283	G35	8864	279
284	G37	8848	166
285	G39	8832	279
286	G41	8816	166
287	G43	8800	279
288	G45	8784	166
289	G47	8768	279
290	G49	8752	166
291	G51	8736	279
292	G53	8720	166
293	G55	8704	279
294	G57	8688	166
295	G59	8672	279
296	G61	8656	166
297	G63	8640	279
298	G65	8624	166
299	G67	8608	279
300	G69	8592	166

PAD NO.	PAD NAME	X	Y
301	G71	8576	279
302	G73	8560	166
303	G75	8544	279
304	G77	8528	166
305	G79	8512	279
306	G81	8496	166
307	G83	8480	279
308	G85	8464	166
309	G87	8448	279
310	G89	8432	166
311	G91	8416	279
312	G93	8400	166
313	G95	8384	279
314	G97	8368	166
315	G99	8352	279
316	G101	8336	166
317	G103	8320	279
318	G105	8304	166
319	G107	8288	279
320	G109	8272	166
321	G111	8256	279
322	G113	8240	166
323	G115	8224	279
324	G117	8208	166
325	G119	8192	279
326	G121	8176	166
327	G123	8160	279
328	G125	8144	166
329	G127	8128	279
330	G129	8112	166
331	G131	8096	279
332	G133	8080	166
333	G135	8064	279
334	G137	8048	166
335	G139	8032	279
336	G141	8016	166
337	G143	8000	279
338	G145	7984	166
339	G147	7968	279
340	G149	7952	166
341	G151	7936	279
342	G153	7920	166
343	G155	7904	279
344	G157	7888	166
345	G159	7872	279
346	G161	7856	166
347	G163	7840	279
348	G165	7824	166
349	G167	7808	279
350	G169	7792	166

PAD NO.	PAD NAME	X	Y
351	G171	7776	279
352	G173	7760	166
353	G175	7744	279
354	G177	7728	166
355	G179	7712	279
356	G181	7696	166
357	G183	7680	279
358	G185	7664	166
359	G187	7648	279
360	G189	7632	166
361	G191	7616	279
362	G193	7600	166
363	G195	7584	279
364	G197	7568	166
365	G199	7552	279
366	G201	7536	166
367	G203	7520	279
368	G205	7504	166
369	G207	7488	279
370	G209	7472	166
371	G211	7456	279
372	G213	7440	166
373	G215	7424	279
374	G217	7408	166
375	G219	7392	279
376	G221	7376	166
377	G223	7360	279
378	G225	7344	166
379	G227	7328	279
380	G229	7312	166
381	G231	7296	279
382	G233	7280	166
383	G235	7264	279
384	G237	7248	166
385	G239	7232	279
386	G241	7216	166
387	G243	7200	279
388	G245	7184	166
389	G247	7168	279
390	G249	7152	166
391	G251	7136	279
392	G253	7120	166
393	G255	7104	279
394	G257	7088	166
395	G259	7072	279
396	G261	7056	166
397	G263	7040	279
398	G265	7024	166
399	G267	7008	279
400	G269	6992	166



PAD NO.	PAD NAME	X	Y
401	G271	6976	279
402	G273	6960	166
403	G275	6944	279
404	G277	6928	166
405	G279	6912	279
406	G281	6896	166
407	G283	6880	279
408	G285	6864	166
409	G287	6848	279
410	G289	6832	166
411	G291	6816	279
412	G293	6800	166
413	G295	6784	279
414	G297	6768	166
415	G299	6752	279
416	G301	6736	166
417	G303	6720	279
418	G305	6704	166
419	G307	6688	279
420	G309	6672	166
421	G311	6656	279
422	G313	6640	166
423	G315	6624	279
424	G317	6608	166
425	G319	6592	279
426	VGLDMY2	6576	166
427	TESTO5	6560	279
428	TESTO6	6368	279
429	TESTO7	6352	166
430	S720	6336	279
431	S719	6320	166
432	S718	6304	279
433	S717	6288	166
434	S716	6272	279
435	S715	6256	166
436	S714	6240	279
437	S713	6224	166
438	S712	6208	279
439	S711	6192	166
440	S710	6176	279
441	S709	6160	166
442	S708	6144	279
443	S707	6128	166
444	S706	6112	279
445	S705	6096	166
446	S704	6080	279
447	S703	6064	166
448	S702	6048	279
449	S701	6032	166
450	S700	6016	279

PAD NO.	PAD NAME	X	Y
451	S699	6000	166
452	S698	5984	279
453	S697	5968	166
454	S696	5952	279
455	S695	5936	166
456	S694	5920	279
457	S693	5904	166
458	S692	5888	279
459	S691	5872	166
460	S690	5856	279
461	S689	5840	166
462	S688	5824	279
463	S687	5808	166
464	S686	5792	279
465	S685	5776	166
466	S684	5760	279
467	S683	5744	166
468	S682	5728	279
469	S681	5712	166
470	S680	5696	279
471	S679	5680	166
472	S678	5664	279
473	S677	5648	166
474	S676	5632	279
475	S675	5616	166
476	S674	5600	279
477	S673	5584	166
478	S672	5568	279
479	S671	5552	166
480	S670	5536	279
481	S669	5520	166
482	S668	5504	279
483	S667	5488	166
484	S666	5472	279
485	S665	5456	166
486	S664	5440	279
487	S663	5424	166
488	S662	5408	279
489	S661	5392	166
490	S660	5376	279
491	S659	5360	166
492	S658	5344	279
493	S657	5328	166
494	S656	5312	279
495	S655	5296	166
496	S654	5280	279
497	S653	5264	166
498	S652	5248	279
499	S651	5232	166
500	S650	5216	279

PAD NO.	PAD NAME	X	Y
501	S649	5200	166
502	S648	5184	279
503	S647	5168	166
504	S646	5152	279
505	S645	5136	166
506	S644	5120	279
507	S643	5104	166
508	S642	5088	279
509	S641	5072	166
510	S640	5056	279
511	S639	5040	166
512	S638	5024	279
513	S637	5008	166
514	S636	4992	279
515	S635	4976	166
516	S634	4960	279
517	S633	4944	166
518	S632	4928	279
519	S631	4912	166
520	S630	4896	279
521	S629	4880	166
522	S628	4864	279
523	S627	4848	166
524	S626	4832	279
525	S625	4816	166
526	S624	4800	279
527	S623	4784	166
528	S622	4768	279
529	S621	4752	166
530	S620	4736	279
531	S619	4720	166
532	S618	4704	279
533	S617	4688	166
534	S616	4672	279
535	S615	4656	166
536	S614	4640	279
537	S613	4624	166
538	S612	4608	279
539	S611	4592	166
540	S610	4576	279
541	S609	4560	166
542	S608	4544	279
543	S607	4528	166
544	S606	4512	279
545	S605	4496	166
546	S604	4480	279
547	S603	4464	166
548	S602	4448	279
549	S601	4432	166
550	S600	4416	279

PAD NO.	PAD NAME	X	Y
551	S599	4400	166
552	S598	4384	279
553	S597	4368	166
554	S596	4352	279
555	S595	4336	166
556	S594	4320	279
557	S593	4304	166
558	S592	4288	279
559	S591	4272	166
560	S590	4256	279
561	S589	4240	166
562	S588	4224	279
563	S587	4208	166
564	S586	4192	279
565	S585	4176	166
566	S584	4160	279
567	S583	4144	166
568	S582	4128	279
569	S581	4112	166
570	S580	4096	279
571	S579	4080	166
572	S578	4064	279
573	S577	4048	166
574	S576	4032	279
575	S575	4016	166
576	S574	4000	279
577	S573	3984	166
578	S572	3968	279
579	S571	3952	166
580	S570	3936	279
581	S569	3920	166
582	S568	3904	279
583	S567	3888	166
584	S566	3872	279
585	S565	3856	166
586	S564	3840	279
587	S563	3824	166
588	S562	3808	279
589	S561	3792	166
590	S560	3776	279
591	S559	3760	166
592	S558	3744	279
593	S557	3728	166
594	S556	3712	279
595	S555	3696	166
596	S554	3680	279
597	S553	3664	166
598	S552	3648	279
599	S551	3632	166
600	S550	3616	279

PAD NO.	PAD NAME	X	Y
601	S549	3600	166
602	S548	3584	279
603	S547	3568	166
604	S546	3552	279
605	S545	3536	166
606	S544	3520	279
607	S543	3504	166
608	S542	3488	279
609	S541	3472	166
610	S540	3456	279
611	S539	3440	166
612	S538	3424	279
613	S537	3408	166
614	S536	3392	279
615	S535	3376	166
616	S534	3360	279
617	S533	3344	166
618	S532	3328	279
619	S531	3312	166
620	S530	3296	279
621	S529	3280	166
622	S528	3264	279
623	S527	3248	166
624	S526	3232	279
625	S525	3216	166
626	S524	3200	279
627	S523	3184	166
628	S522	3168	279
629	S521	3152	166
630	S520	3136	279
631	S519	3120	166
632	S518	3104	279
633	S517	3088	166
634	S516	3072	279
635	S515	3056	166
636	S514	3040	279
637	S513	3024	166
638	S512	3008	279
639	S511	2992	166
640	S510	2976	279
641	S509	2960	166
642	S508	2944	279
643	S507	2928	166
644	S506	2912	279
645	S505	2896	166
646	S504	2880	279
647	S503	2864	166
648	S502	2848	279
649	S501	2832	166
650	S500	2816	279

PAD NO.	PAD NAME	X	Y
651	S499	2800	166
652	S498	2784	279
653	S497	2768	166
654	S496	2752	279
655	S495	2736	166
656	S494	2720	279
657	S493	2704	166
658	S492	2688	279
659	S491	2672	166
660	S490	2656	279
661	S489	2640	166
662	S488	2624	279
663	S487	2608	166
664	S486	2592	279
665	S485	2576	166
666	S484	2560	279
667	S483	2544	166
668	S482	2528	279
669	S481	2512	166
670	S480	2496	279
671	S479	2480	166
672	S478	2464	279
673	S477	2448	166
674	S476	2432	279
675	S475	2416	166
676	S474	2400	279
677	S473	2384	166
678	S472	2368	279
679	S471	2352	166
680	S470	2336	279
681	S469	2320	166
682	S468	2304	279
683	S467	2288	166
684	S466	2272	279
685	S465	2256	166
686	S464	2240	279
687	S463	2224	166
688	S462	2208	279
689	S461	2192	166
690	S460	2176	279
691	S459	2160	166
692	S458	2144	279
693	S457	2128	166
694	S456	2112	279
695	S455	2096	166
696	S454	2080	279
697	S453	2064	166
698	S452	2048	279
699	S451	2032	166
700	S450	2016	279

PAD NO.	PAD NAME	X	Y
701	S449	2000	166
702	S448	1984	279
703	S447	1968	166
704	S446	1952	279
705	S445	1936	166
706	S444	1920	279
707	S443	1904	166
708	S442	1888	279
709	S441	1872	166
710	S440	1856	279
711	S439	1840	166
712	S438	1824	279
713	S437	1808	166
714	S436	1792	279
715	S435	1776	166
716	S434	1760	279
717	S433	1744	166
718	S432	1728	279
719	S431	1712	166
720	S430	1696	279
721	S429	1680	166
722	S428	1664	279
723	S427	1648	166
724	S426	1632	279
725	S425	1616	166
726	S424	1600	279
727	S423	1584	166
728	S422	1568	279
729	S421	1552	166
730	S420	1536	279
731	S419	1520	166
732	S418	1504	279
733	S417	1488	166
734	S416	1472	279
735	S415	1456	166
736	S414	1440	279
737	S413	1424	166
738	S412	1408	279
739	S411	1392	166
740	S410	1376	279
741	S409	1360	166
742	S408	1344	279
743	S407	1328	166
744	S406	1312	279
745	S405	1296	166
746	S404	1280	279
747	S403	1264	166
748	S402	1248	279
749	S401	1232	166
750	S400	1216	279

PAD NO.	PAD NAME	X	Y
751	S399	1200	166
752	S398	1184	279
753	S397	1168	166
754	S396	1152	279
755	S395	1136	166
756	S394	1120	279
757	S393	1104	166
758	S392	1088	279
759	S391	1072	166
760	S390	1056	279
761	S389	1040	166
762	S388	1024	279
763	S387	1008	166
764	S386	992	279
765	S385	976	166
766	S384	960	279
767	S383	944	166
768	S382	928	279
769	S381	912	166
770	S380	896	279
771	S379	880	166
772	S378	864	279
773	S377	848	166
774	S376	832	279
775	S375	816	166
776	S374	800	279
777	S373	784	166
778	S372	768	279
779	S371	752	166
780	S370	736	279
781	S369	720	166
782	S368	704	279
783	S367	688	166
784	S366	672	279
785	S365	656	166
786	S364	640	279
787	S363	624	166
788	S362	608	279
789	S361	592	166
790	TESTO8	576	279
791	TESTO9	-576	166
792	S360	-592	279
793	S359	-608	166
794	S358	-624	279
795	S357	-640	166
796	S356	-656	279
797	S355	-672	166
798	S354	-688	279
799	S353	-704	166
800	S352	-720	279

PAD NO.	PAD NAME	X	Y
801	S351	-736	166
802	S350	-752	279
803	S349	-768	166
804	S348	-784	279
805	S347	-800	166
806	S346	-816	279
807	S345	-832	166
808	S344	-848	279
809	S343	-864	166
810	S342	-880	279
811	S341	-896	166
812	S340	-912	279
813	S339	-928	166
814	S338	-944	279
815	S337	-960	166
816	S336	-976	279
817	S335	-992	166
818	S334	-1008	279
819	S333	-1024	166
820	S332	-1040	279
821	S331	-1056	166
822	S330	-1072	279
823	S329	-1088	166
824	S328	-1104	279
825	S327	-1120	166
826	S326	-1136	279
827	S325	-1152	166
828	S324	-1168	279
829	S323	-1184	166
830	S322	-1200	279
831	S321	-1216	166
832	S320	-1232	279
833	S319	-1248	166
834	S318	-1264	279
835	S317	-1280	166
836	S316	-1296	279
837	S315	-1312	166
838	S314	-1328	279
839	S313	-1344	166
840	S312	-1360	279
841	S311	-1376	166
842	S310	-1392	279
843	S309	-1408	166
844	S308	-1424	279
845	S307	-1440	166
846	S306	-1456	279
847	S305	-1472	166
848	S304	-1488	279
849	S303	-1504	166
850	S302	-1520	279

PAD NO.	PAD NAME	X	Y
851	S301	-1536	166
852	S300	-1552	279
853	S299	-1568	166
854	S298	-1584	279
855	S297	-1600	166
856	S296	-1616	279
857	S295	-1632	166
858	S294	-1648	279
859	S293	-1664	166
860	S292	-1680	279
861	S291	-1696	166
862	S290	-1712	279
863	S289	-1728	166
864	S288	-1744	279
865	S287	-1760	166
866	S286	-1776	279
867	S285	-1792	166
868	S284	-1808	279
869	S283	-1824	166
870	S282	-1840	279
871	S281	-1856	166
872	S280	-1872	279
873	S279	-1888	166
874	S278	-1904	279
875	S277	-1920	166
876	S276	-1936	279
877	S275	-1952	166
878	S274	-1968	279
879	S273	-1984	166
880	S272	-2000	279
881	S271	-2016	166
882	S270	-2032	279
883	S269	-2048	166
884	S268	-2064	279
885	S267	-2080	166
886	S266	-2096	279
887	S265	-2112	166
888	S264	-2128	279
889	S263	-2144	166
890	S262	-2160	279
891	S261	-2176	166
892	S260	-2192	279
893	S259	-2208	166
894	S258	-2224	279
895	S257	-2240	166
896	S256	-2256	279
897	S255	-2272	166
898	S254	-2288	279
899	S253	-2304	166
900	S252	-2320	279

PAD NO.	PAD NAME	X	Y
901	S251	-2336	166
902	S250	-2352	279
903	S249	-2368	166
904	S248	-2384	279
905	S247	-2400	166
906	S246	-2416	279
907	S245	-2432	166
908	S244	-2448	279
909	S243	-2464	166
910	S242	-2480	279
911	S241	-2496	166
912	S240	-2512	279
913	S239	-2528	166
914	S238	-2544	279
915	S237	-2560	166
916	S236	-2576	279
917	S235	-2592	166
918	S234	-2608	279
919	S233	-2624	166
920	S232	-2640	279
921	S231	-2656	166
922	S230	-2672	279
923	S229	-2688	166
924	S228	-2704	279
925	S227	-2720	166
926	S226	-2736	279
927	S225	-2752	166
928	S224	-2768	279
929	S223	-2784	166
930	S222	-2800	279
931	S221	-2816	166
932	S220	-2832	279
933	S219	-2848	166
934	S218	-2864	279
935	S217	-2880	166
936	S216	-2896	279
937	S215	-2912	166
938	S214	-2928	279
939	S213	-2944	166
940	S212	-2960	279
941	S211	-2976	166
942	S210	-2992	279
943	S209	-3008	166
944	S208	-3024	279
945	S207	-3040	166
946	S206	-3056	279
947	S205	-3072	166
948	S204	-3088	279
949	S203	-3104	166
950	S202	-3120	279

PAD NO.	PAD NAME	X	Y
951	S201	-3136	166
952	S200	-3152	279
953	S199	-3168	166
954	S198	-3184	279
955	S197	-3200	166
956	S196	-3216	279
957	S195	-3232	166
958	S194	-3248	279
959	S193	-3264	166
960	S192	-3280	279
961	S191	-3296	166
962	S190	-3312	279
963	S189	-3328	166
964	S188	-3344	279
965	S187	-3360	166
966	S186	-3376	279
967	S185	-3392	166
968	S184	-3408	279
969	S183	-3424	166
970	S182	-3440	279
971	S181	-3456	166
972	S180	-3472	279
973	S179	-3488	166
974	S178	-3504	279
975	S177	-3520	166
976	S176	-3536	279
977	S175	-3552	166
978	S174	-3568	279
979	S173	-3584	166
980	S172	-3600	279
981	S171	-3616	166
982	S170	-3632	279
983	S169	-3648	166
984	S168	-3664	279
985	S167	-3680	166
986	S166	-3696	279
987	S165	-3712	166
988	S164	-3728	279
989	S163	-3744	166
990	S162	-3760	279
991	S161	-3776	166
992	S160	-3792	279
993	S159	-3808	166
994	S158	-3824	279
995	S157	-3840	166
996	S156	-3856	279
997	S155	-3872	166
998	S154	-3888	279
999	S153	-3904	166
1000	S152	-3920	279

PAD NO.	PAD NAME	X	Y
1001	S151	-3936	166
1002	S150	-3952	279
1003	S149	-3968	166
1004	S148	-3984	279
1005	S147	-4000	166
1006	S146	-4016	279
1007	S145	-4032	166
1008	S144	-4048	279
1009	S143	-4064	166
1010	S142	-4080	279
1011	S141	-4096	166
1012	S140	-4112	279
1013	S139	-4128	166
1014	S138	-4144	279
1015	S137	-4160	166
1016	S136	-4176	279
1017	S135	-4192	166
1018	S134	-4208	279
1019	S133	-4224	166
1020	S132	-4240	279
1021	S131	-4256	166
1022	S130	-4272	279
1023	S129	-4288	166
1024	S128	-4304	279
1025	S127	-4320	166
1026	S126	-4336	279
1027	S125	-4352	166
1028	S124	-4368	279
1029	S123	-4384	166
1030	S122	-4400	279
1031	S121	-4416	166
1032	S120	-4432	279
1033	S119	-4448	166
1034	S118	-4464	279
1035	S117	-4480	166
1036	S116	-4496	279
1037	S115	-4512	166
1038	S114	-4528	279
1039	S113	-4544	166
1040	S112	-4560	279
1041	S111	-4576	166
1042	S110	-4592	279
1043	S109	-4608	166
1044	S108	-4624	279
1045	S107	-4640	166
1046	S106	-4656	279
1047	S105	-4672	166
1048	S104	-4688	279
1049	S103	-4704	166
1050	S102	-4720	279

PAD NO.	PAD NAME	X	Y
1051	S101	-4736	166
1052	S100	-4752	279
1053	S99	-4768	166
1054	S98	-4784	279
1055	S97	-4800	166
1056	S96	-4816	279
1057	S95	-4832	166
1058	S94	-4848	279
1059	S93	-4864	166
1060	S92	-4880	279
1061	S91	-4896	166
1062	S90	-4912	279
1063	S89	-4928	166
1064	S88	-4944	279
1065	S87	-4960	166
1066	S86	-4976	279
1067	S85	-4992	166
1068	S84	-5008	279
1069	S83	-5024	166
1070	S82	-5040	279
1071	S81	-5056	166
1072	S80	-5072	279
1073	S79	-5088	166
1074	S78	-5104	279
1075	S77	-5120	166
1076	S76	-5136	279
1077	S75	-5152	166
1078	S74	-5168	279
1079	S73	-5184	166
1080	S72	-5200	279
1081	S71	-5216	166
1082	S70	-5232	279
1083	S69	-5248	166
1084	S68	-5264	279
1085	S67	-5280	166
1086	S66	-5296	279
1087	S65	-5312	166
1088	S64	-5328	279
1089	S63	-5344	166
1090	S62	-5360	279
1091	S61	-5376	166
1092	S60	-5392	279
1093	S59	-5408	166
1094	S58	-5424	279
1095	S57	-5440	166
1096	S56	-5456	279
1097	S55	-5472	166
1098	S54	-5488	279
1099	S53	-5504	166
1100	S52	-5520	279

PAD NO.	PAD NAME	X	Y
1101	S51	-5536	166
1102	S50	-5552	279
1103	S49	-5568	166
1104	S48	-5584	279
1105	S47	-5600	166
1106	S46	-5616	279
1107	S45	-5632	166
1108	S44	-5648	279
1109	S43	-5664	166
1110	S42	-5680	279
1111	S41	-5696	166
1112	S40	-5712	279
1113	S39	-5728	166
1114	S38	-5744	279
1115	S37	-5760	166
1116	S36	-5776	279
1117	S35	-5792	166
1118	S34	-5808	279
1119	S33	-5824	166
1120	S32	-5840	279
1121	S31	-5856	166
1122	S30	-5872	279
1123	S29	-5888	166
1124	S28	-5904	279
1125	S27	-5920	166
1126	S26	-5936	279
1127	S25	-5952	166
1128	S24	-5968	279
1129	S23	-5984	166
1130	S22	-6000	279
1131	S21	-6016	166
1132	S20	-6032	279
1133	S19	-6048	166
1134	S18	-6064	279
1135	S17	-6080	166
1136	S16	-6096	279
1137	S15	-6112	166
1138	S14	-6128	279
1139	S13	-6144	166
1140	S12	-6160	279
1141	S11	-6176	166
1142	S10	-6192	279
1143	S9	-6208	166
1144	S8	-6224	279
1145	S7	-6240	166
1146	S6	-6256	279
1147	S5	-6272	166
1148	S4	-6288	279
1149	S3	-6304	166
1150	S2	-6320	279

PAD NO.	PAD NAME	X	Y
1151	S1	-6336	166
1152	TESTO10	-6352	279
1153	TESTO11	-6368	166
1154	TESTO12	-6560	279
1155	VGLDMY3	-6576	166
1156	G320	-6592	279
1157	G318	-6608	166
1158	G316	-6624	279
1159	G314	-6640	166
1160	G312	-6656	279
1161	G310	-6672	166
1162	G308	-6688	279
1163	G306	-6704	166
1164	G304	-6720	279
1165	G302	-6736	166
1166	G300	-6752	279
1167	G298	-6768	166
1168	G296	-6784	279
1169	G294	-6800	166
1170	G292	-6816	279
1171	G290	-6832	166
1172	G288	-6848	279
1173	G286	-6864	166
1174	G284	-6880	279
1175	G282	-6896	166
1176	G280	-6912	279
1177	G278	-6928	166
1178	G276	-6944	279
1179	G274	-6960	166
1180	G272	-6976	279
1181	G270	-6992	166
1182	G268	-7008	279
1183	G266	-7024	166
1184	G264	-7040	279
1185	G262	-7056	166
1186	G260	-7072	279
1187	G258	-7088	166
1188	G256	-7104	279
1189	G254	-7120	166
1190	G252	-7136	279
1191	G250	-7152	166
1192	G248	-7168	279
1193	G246	-7184	166
1194	G244	-7200	279
1195	G242	-7216	166
1196	G240	-7232	279
1197	G238	-7248	166
1198	G236	-7264	279
1199	G234	-7280	166
1200	G232	-7296	279



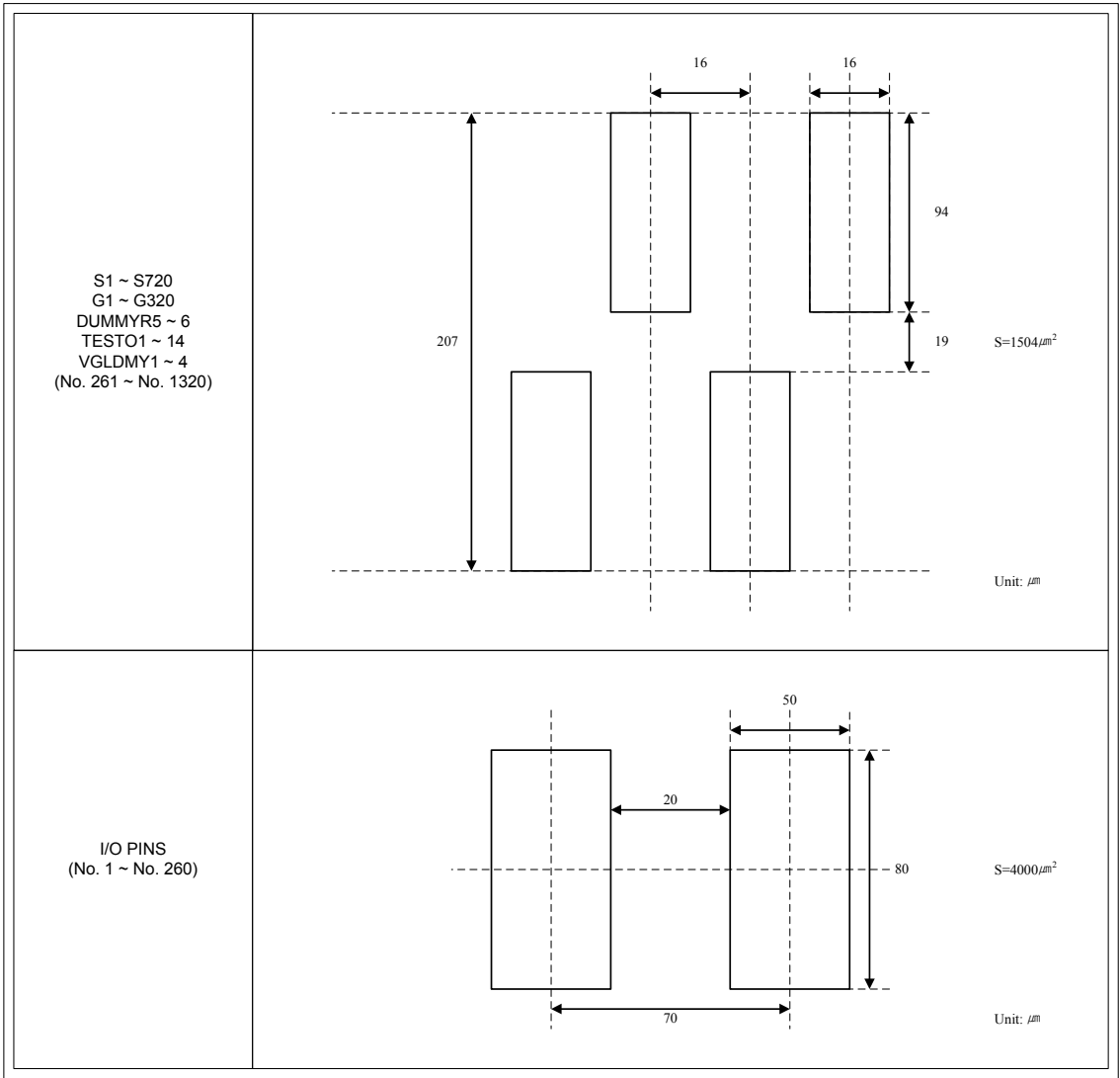
PAD NO.	PAD NAME	X	Y
1201	G230	-7312	166
1202	G228	-7328	279
1203	G226	-7344	166
1204	G224	-7360	279
1205	G222	-7376	166
1206	G220	-7392	279
1207	G218	-7408	166
1208	G216	-7424	279
1209	G214	-7440	166
1210	G212	-7456	279
1211	G210	-7472	166
1212	G208	-7488	279
1213	G206	-7504	166
1214	G204	-7520	279
1215	G202	-7536	166
1216	G200	-7552	279
1217	G198	-7568	166
1218	G196	-7584	279
1219	G194	-7600	166
1220	G192	-7616	279
1221	G190	-7632	166
1222	G188	-7648	279
1223	G186	-7664	166
1224	G184	-7680	279
1225	G182	-7696	166
1226	G180	-7712	279
1227	G178	-7728	166
1228	G176	-7744	279
1229	G174	-7760	166
1230	G172	-7776	279
1231	G170	-7792	166
1232	G168	-7808	279
1233	G166	-7824	166
1234	G164	-7840	279
1235	G162	-7856	166
1236	G160	-7872	279
1237	G158	-7888	166
1238	G156	-7904	279
1239	G154	-7920	166
1240	G152	-7936	279
1241	G150	-7952	166
1242	G148	-7968	279
1243	G146	-7984	166
1244	G144	-8000	279
1245	G142	-8016	166
1246	G140	-8032	279
1247	G138	-8048	166
1248	G136	-8064	279
1249	G134	-8080	166
1250	G132	-8096	279

PAD NO.	PAD NAME	X	Y
1251	G130	-8112	166
1252	G128	-8128	279
1253	G126	-8144	166
1254	G124	-8160	279
1255	G122	-8176	166
1256	G120	-8192	279
1257	G118	-8208	166
1258	G116	-8224	279
1259	G114	-8240	166
1260	G112	-8256	279
1261	G110	-8272	166
1262	G108	-8288	279
1263	G106	-8304	166
1264	G104	-8320	279
1265	G102	-8336	166
1266	G100	-8352	279
1267	G98	-8368	166
1268	G96	-8384	279
1269	G94	-8400	166
1270	G92	-8416	279
1271	G90	-8432	166
1272	G88	-8448	279
1273	G86	-8464	166
1274	G84	-8480	279
1275	G82	-8496	166
1276	G80	-8512	279
1277	G78	-8528	166
1278	G76	-8544	279
1279	G74	-8560	166
1280	G72	-8576	279
1281	G70	-8592	166
1282	G68	-8608	279
1283	G66	-8624	166
1284	G64	-8640	279
1285	G62	-8656	166
1286	G60	-8672	279
1287	G58	-8688	166
1288	G56	-8704	279
1289	G54	-8720	166
1290	G52	-8736	279
1291	G50	-8752	166
1292	G48	-8768	279
1293	G46	-8784	166
1294	G44	-8800	279
1295	G42	-8816	166
1296	G40	-8832	279
1297	G38	-8848	166
1298	G36	-8864	279
1299	G34	-8880	166
1300	G32	-8896	279

PAD NO.	PAD NAME	X	Y
1301	G30	-8912	166
1302	G28	-8928	279
1303	G26	-8944	166
1304	G24	-8960	279
1305	G22	-8976	166
1306	G20	-8992	279
1307	G18	-9008	166
1308	G16	-9024	279
1309	G14	-9040	166
1310	G12	-9056	279
1311	G10	-9072	166
1312	G8	-9088	279
1313	G6	-9104	166
1314	G4	-9120	279
1315	G2	-9136	166
1316	VGLDUMMY4	-9152	279
1317	DUMMYR5	-9168	166
1318	DUMMYR6	-9184	279
1319	TESTO13	-9200	166
1320	TESTO14	-9216	279

Alignment mark	X	Y
1-a	-9266	-251
1-b	9266	-251

Bump Arrangement



## Block Function

### System Interface

The LGDP4535 supports 2-system high-speed interfaces: 80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and a Serial Peripheral Interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

The LGDP4535 has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the LGDP4535 read the first data from the internal GRAM. Valid data are read out after the LGDP4535 performs the second read operation.

Instructions are written consecutively as the instruction execution time except starting oscillator takes 0 clock cycle.

**Table 6 Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)**

80-system I/F			Function
WR*	RD*	RS	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

**Table 7 Register Selection (Serial Peripheral Interface)**

Start Byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

### External Display Interface

The LGDP4535 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB[17:0]) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section.

The LGDP4535 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

### **Address Counter (AC)**

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

### **Graphics RAM (GRAM)**

GRAM is graphics RAM storing bit-pattern data of 172,800 (240 x 320x 18bit) bytes, using 18 bits per pixel.

### **Grayscale Voltage Generating Circuit**

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the  $\gamma$ -correction register to display in 262,144 colors. For details, see the “ $\gamma$ -Correction Register” section.

### **Timing Generator**

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

### **Oscillator (OSC)**

LGDP4535 generates RC oscillation with an internal oscillation resistor. The frame rate is adjusted by the register setting.

### **LCD Driver Circuit**

The LCD driver circuit of the LGDP4535 consists of a 720-output source driver (S1 ~ S720) and a 240-output gate driver (G1~G320). Display pattern data are latched when the 720th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

### **LCD Drive Power Supply Circuit**

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

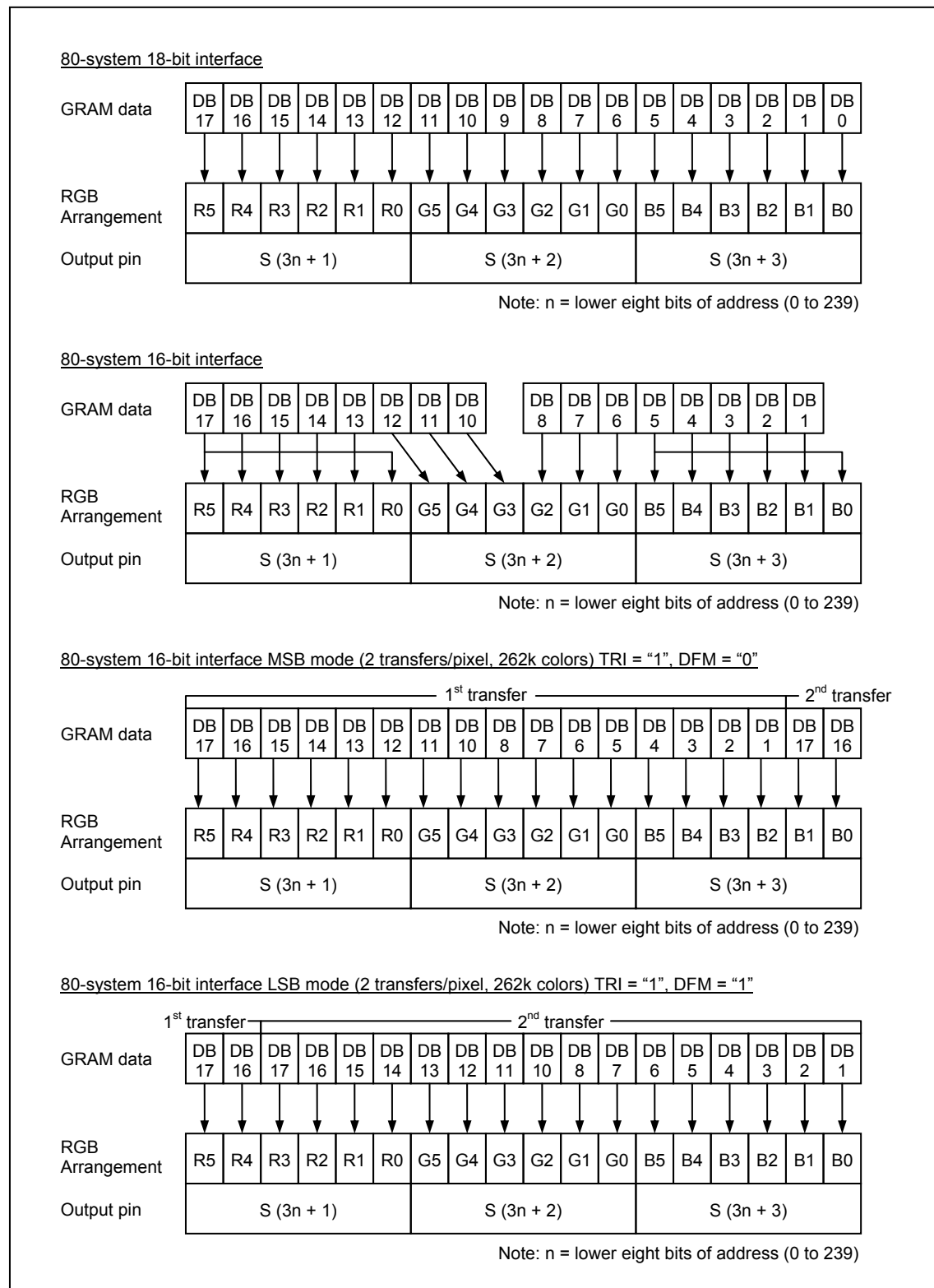
### **Internal logic power supply regulator**

The internal logic power supply regulator generates internal logic power supply VDD.

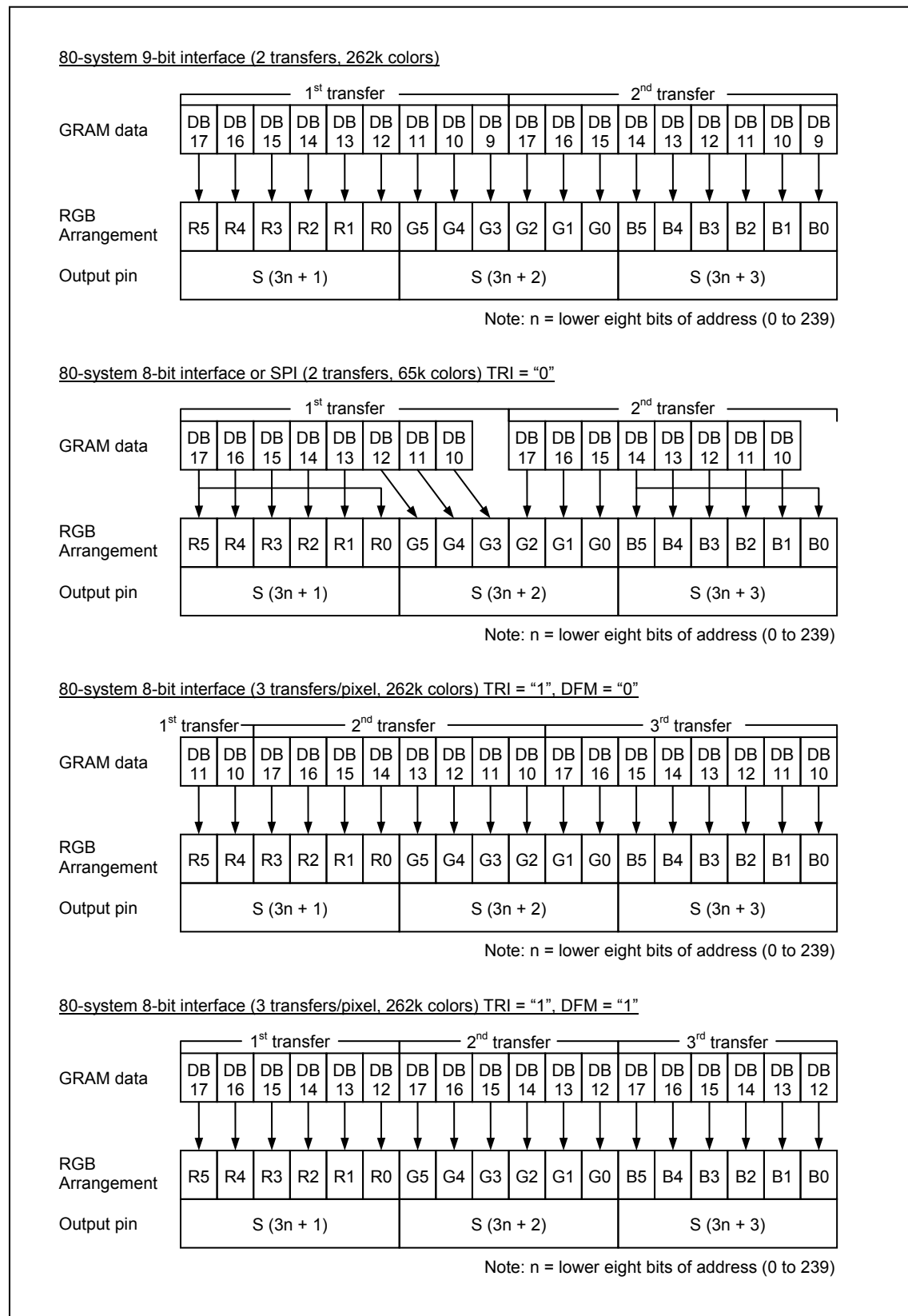
## GRAM Address MAP

Table 8 GRAM address and display panel position (SS = “0”, BGR = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	...	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB[17:0]				DB[17:0]				DB[17:0]				...	DB[17:0]				DB[17:0]				DB[17:0]			
G1	G320	“00000”H				“00001”H				“00002”H				...	“000EC”H				“000ED”H				“000EE”H			
G2	G319	“00100”H				“00101”H				“00102”H				...	“001EC”H				“001ED”H				“001EE”H			
G3	G318	“00200”H				“00201”H				“00202”H				...	“002EC”H				“002ED”H				“002EE”H			
G4	G317	“00300”H				“00301”H				“00302”H				...	“003EC”H				“003ED”H				“003EE”H			
G5	G316	“00400”H				“00401”H				“00402”H				...	“004EC”H				“004ED”H				“004EE”H			
G6	G315	“00500”H				“00501”H				“00502”H				...	“005EC”H				“005ED”H				“005EE”H			
G7	G314	“00600”H				“00601”H				“00602”H				...	“006EC”H				“006ED”H				“006EE”H			
G8	G313	“00700”H				“00701”H				“00702”H				...	“007EC”H				“007ED”H				“007EE”H			
G9	G312	“00800”H				“00801”H				“00802”H				...	“008EC”H				“008ED”H				“008EE”H			
G10	G311	“00900”H				“00901”H				“00902”H				...	“009EC”H				“009ED”H				“009EE”H			
G11	G310	“00A00”H				“00A01”H				“00A02”H				...	“00AEC”H				“00AED”H				“00AEE”H			
G12	G309	“00B00”H				“00B01”H				“00B02”H				...	“00BEC”H				“00BED”H				“00BEE”H			
G13	G308	“00C00”H				“00C01”H				“00C02”H				...	“00CEC”H				“00CED”H				“00CEE”H			
G14	G307	“00D00”H				“00D01”H				“00D02”H				...	“00DEC”H				“00DED”H				“00DEE”H			
G15	G306	“00E00”H				“00E01”H				“00E02”H				...	“00EEC”H				“00EED”H				“00EEE”H			
G16	G305	“00F00”H				“00F01”H				“00F02”H				...	“00FEC”H				“00FED”H				“00FEE”H			
G17	G304	“01000”H				“01001”H				“01002”H				...	“010EC”H				“010ED”H				“010EE”H			
G18	G303	“01100”H				“01101”H				“01102”H				...	“011EC”H				“011ED”H				“011EE”H			
G19	G302	“01200”H				“01201”H				“01202”H				...	“012EC”H				“012ED”H				“012EE”H			
G20	G301	“01300”H				“01301”H				“1302”H				...	“013EC”H				“013ED”H				“013EE”H			
:	:	:				:				:				...	:				:				:			
:	:	:				:				:				...	:				:				:			
G313	G8	“13800”H				“13801”H				“13802”H				...	“138EC”H				“138ED”H				“138EE”H			
G314	G7	“13900”H				“13901”H				“13902”H				...	“139EC”H				“139ED”H				“139EE”H			
G315	G6	“13A00”H				“13A01”H				“13A02”H				...	“13AEC”H				“13AED”H				“13AEE”H			
G316	G5	“13B00”H				“13B01”H				“13B02”H				...	“13BEC”H				“13BED”H				“13BEE”H			
G317	G4	“13C00”H				“13C01”H				“13C02”H				...	“13CEC”H				“13CED”H				“13CEE”H			
G318	G3	“13D00”H				“13D01”H				“13D02”H				...	“13DEC”H				“13DED”H				“13DEE”H			
G319	G2	“13E00”H				“13E01”H				“13E02”H				...	“13EEC”H				“13EED”H				“13EEE”H			
G320	G1	“13F00”H				“13F01”H				“13F02”H				...	“13FEC”H				“13FED”H				“13FEE”H			

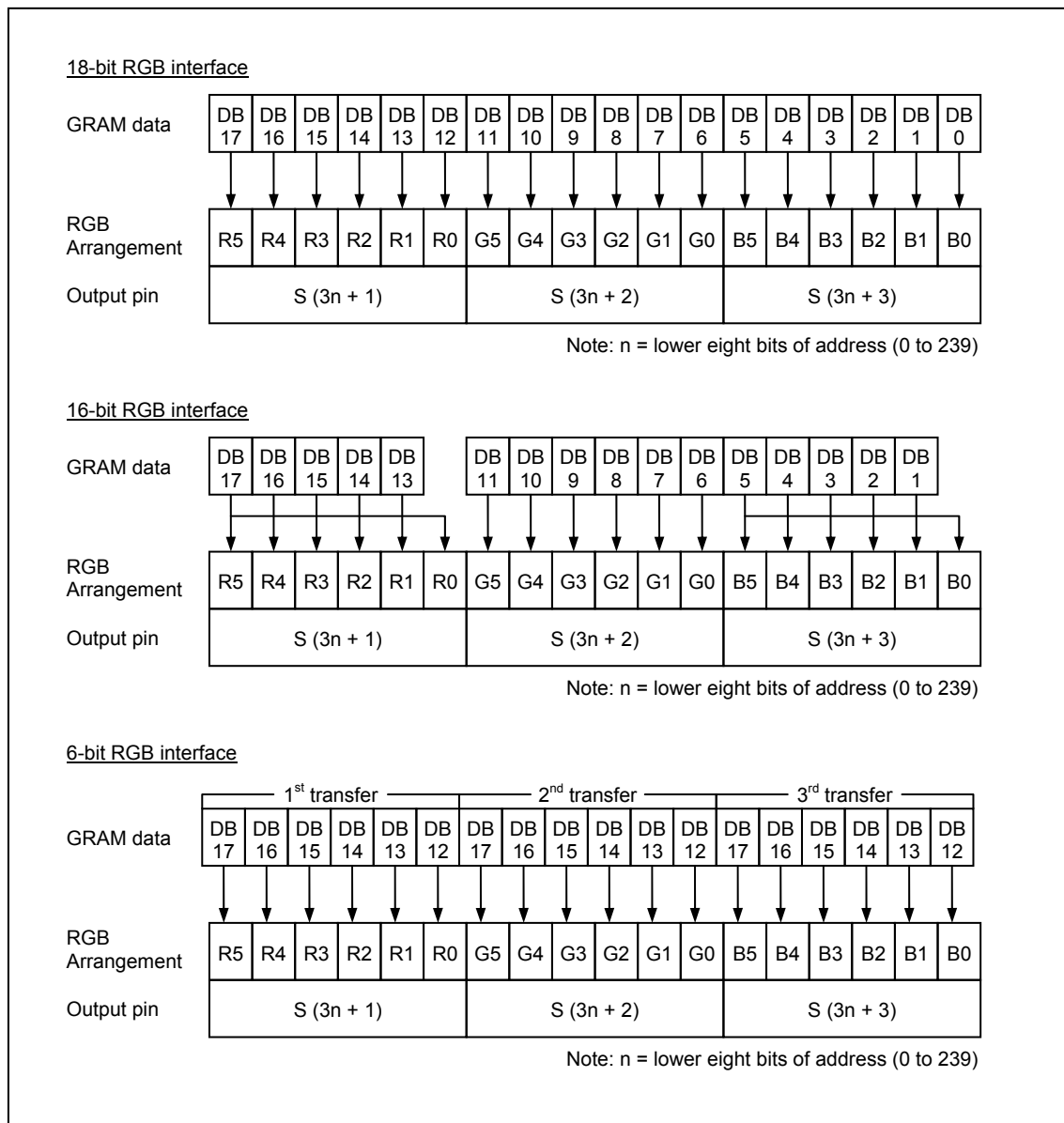


**Figure 2 GRAM data and display data: system interface (SS = "0", BGR = "0")**



**Figure 3 GRAM data and isplay data: system interface (SS = "0", BGR = "0")**

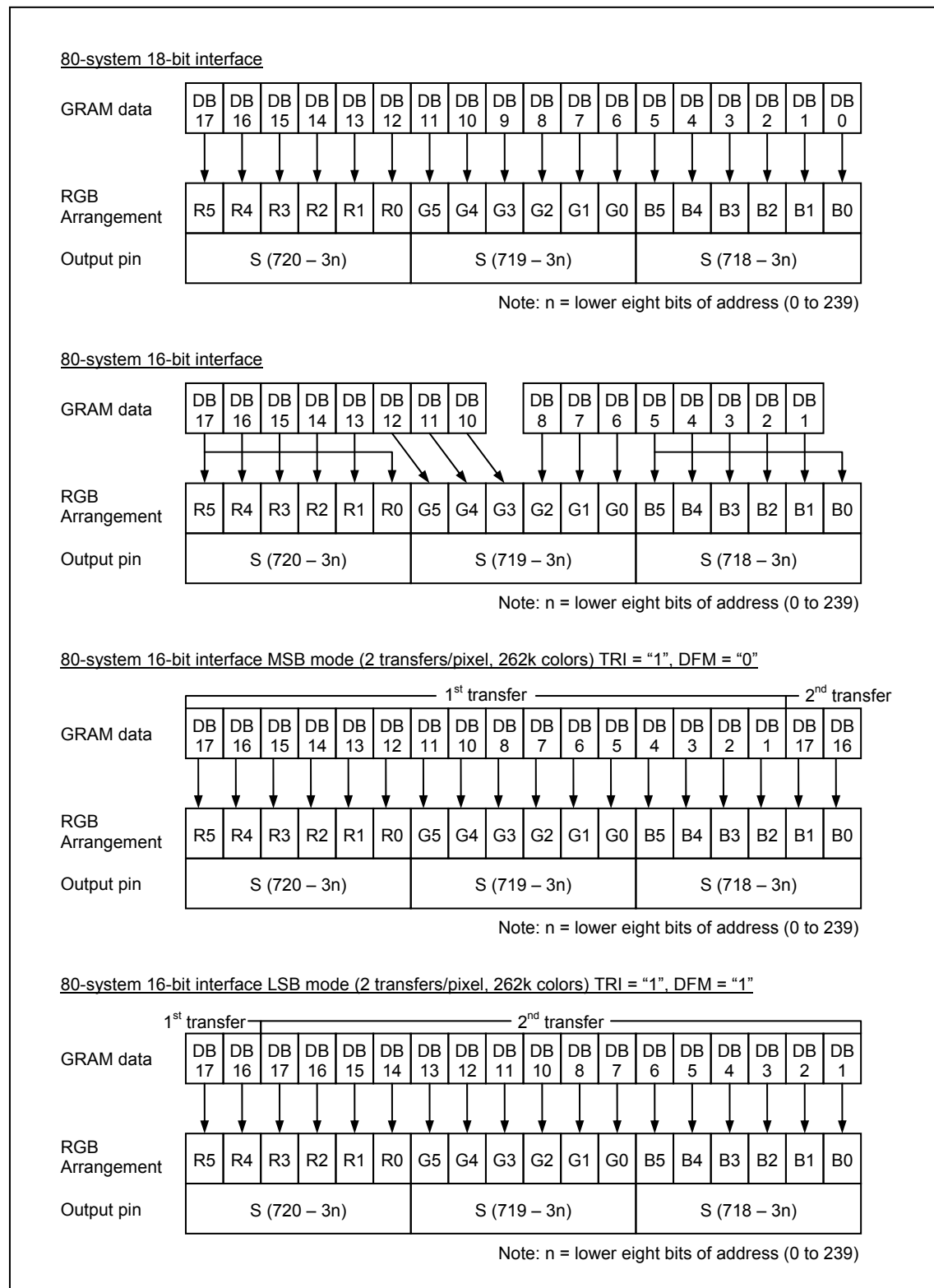




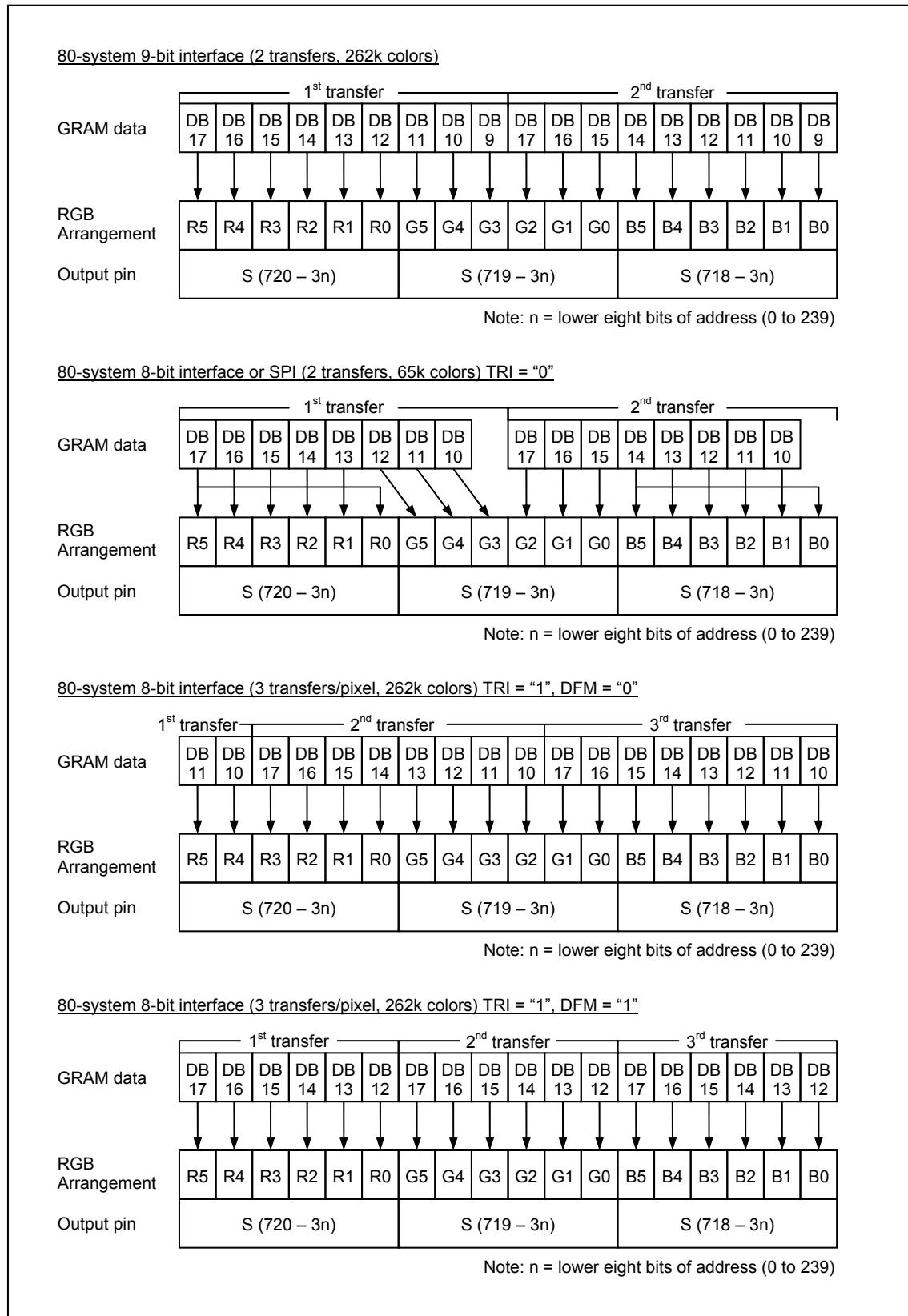
**Figure 4 GRAM data and display data: system interface (SS = “0”, BGR = “0”)**

**Table 9 GRAM address and display panel position (SS = “1”, BGR = “1”)**

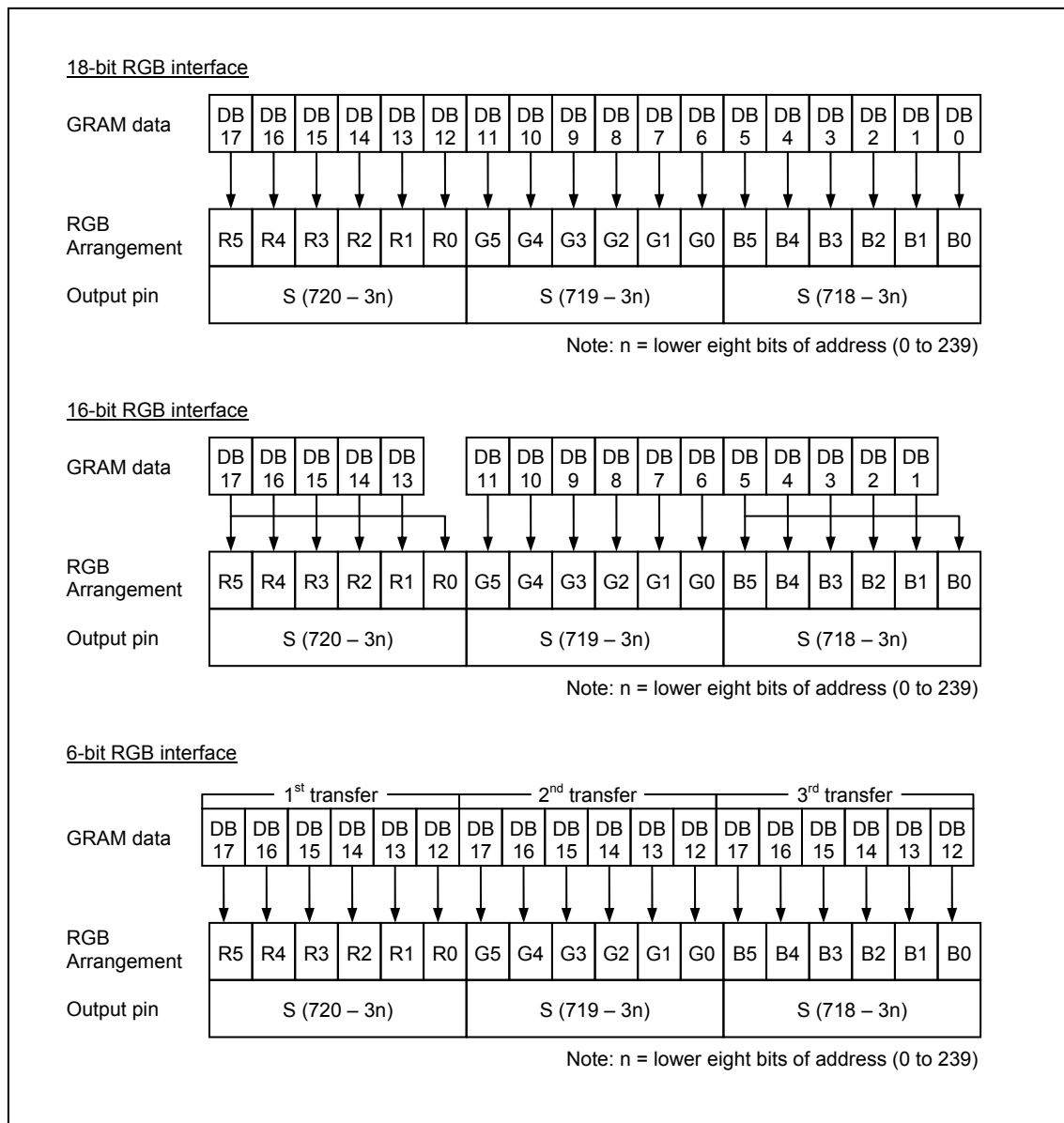
S/G pin		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	⋮	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			...	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G320	"00000"H			"00001"H			"00002"H			"00003"H			...	"000EC"H			"000ED"H			"000EE"H			"000EF"H		
G2	G319	"00100"H			"00101"H			"00102"H			"00103"H			...	"001EC"H			"001ED"H			"001EE"H			"001EF"H		
G3	G318	"00200"H			"00201"H			"00202"H			"00203"H			...	"002EC"H			"002ED"H			"002EE"H			"002EF"H		
G4	G317	"00300"H			"00301"H			"00302"H			"00303"H			...	"003EC"H			"003ED"H			"003EE"H			"003EF"H		
G5	G316	"00400"H			"00401"H			"00402"H			"00403"H			...	"004EC"H			"004ED"H			"004EE"H			"004EF"H		
G6	G315	"00500"H			"00501"H			"00502"H			"00503"H			...	"005EC"H			"005ED"H			"005EE"H			"005EF"H		
G7	G314	"00600"H			"00601"H			"00602"H			"00603"H			...	"006EC"H			"006ED"H			"006EE"H			"006EF"H		
G8	G313	"00700"H			"00701"H			"00702"H			"00703"H			...	"007EC"H			"007ED"H			"007EE"H			"007EF"H		
G9	G312	"00800"H			"00801"H			"00802"H			"00803"H			...	"008EC"H			"008ED"H			"008EE"H			"008EF"H		
G10	G311	"00900"H			"00901"H			"00902"H			"00903"H			...	"009EC"H			"009ED"H			"009EE"H			"009EF"H		
G11	G310	"00A00"H			"00A01"H			"00A02"H			"00A03"H			...	"00AEC"H			"00AED"H			"00AEE"H			"00AEF"H		
G12	G309	"00B00"H			"00B01"H			"00B02"H			"00B03"H			...	"00BEC"H			"00BED"H			"00BEE"H			"00BEF"H		
G13	G308	"00C00"H			"00C01"H			"00C02"H			"00C03"H			...	"00CEC"H			"00CED"H			"00CEE"H			"00CEF"H		
G14	G307	"00D00"H			"00D01"H			"00D02"H			"00D03"H			...	"00DEC"H			"00DED"H			"00DEE"H			"00DEF"H		
G15	G306	"00E00"H			"00E01"H			"00E02"H			"00E03"H			...	"00EEC"H			"00EED"H			"00EEE"H			"00EEF"H		
G16	G305	"00F00"H			"00F01"H			"00F02"H			"00F03"H			...	"00FEC"H			"00FED"H			"00FEE"H			"00FEF"H		
G17	G304	"01000"H			"01001"H			"01002"H			"01003"H			...	"010EC"H			"010ED"H			"010EE"H			"010EF"H		
G18	G303	"01100"H			"01101"H			"01102"H			"01103"H			...	"011EC"H			"011ED"H			"011EE"H			"011EF"H		
G19	G302	"01200"H			"01201"H			"01202"H			"01203"H			...	"012EC"H			"012ED"H			"012EE"H			"012EF"H		
G20	G301	"01300"H			"01301"H			"1302"H			"01303"H			...	"013EC"H			"013ED"H			"013EE"H			"013EF"H		
:	:	:	:	:	:	:	:	:	:	:	:	:	:	...	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	...	:	:	:	:	:	:	:	:	:	:	:	
G313	G8	"13800"H			"13801"H			"13802"H			"13803"H			...	"138EC"H			"138ED"H			"138EE"H			"138EF"H		
G314	G7	"13900"H			"13901"H			"13902"H			"13903"H			...	"139EC"H			"139ED"H			"139EE"H			"139EF"H		
G315	G6	"13A00"H			"13A01"H			"13A02"H			"13A03"H			...	"13AEC"H			"13AED"H			"13AEE"H			"13AEF"H		
G316	G5	"13B00"H			"13B01"H			"13B02"H			"13B03"H			...	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			...	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			...	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			...	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			...	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		



**Figure 5 GRAM data and display data: system interface (SS = "1", BGR = "1")**



**Figure 6 GRAM data and display data: system interface (SS = "1", BGR = "1")**



**Figure 7 GRAM data and display data: system interface (SS = “1”, BGR = “1”)**

## Instructions

### Outline

The LGDP4535 adopts 18-bit bus architecture to interface to a high-performance microcomputer. The LGDP4535 starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the instruction register (IR) and the data register (DR). Since internal operations of the LGDP4535 are controlled by the signals sent from the microcomputer, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 to IB0) are called instructions. The LGDP4535 use the 18-bit format internally for operations involving internal GRAM access. The instructions of the LGDP4535 are categorized into the following groups.

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale  $\gamma$ -correction

Normally, the instruction for writing data to the internal GRAM is used the most often. Since the LGDP4535 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there is less load on the program in the microcomputer. Since instructions are executed in 0 cycles, it is possible to write instructions consecutively.

### Instruction Data Format

Note that as the following figure shows, the assignment of 16 instruction bits (IB15-0) to the data bus differs in different interface operations. Write instruction according to the data transfer format of the interface in use.

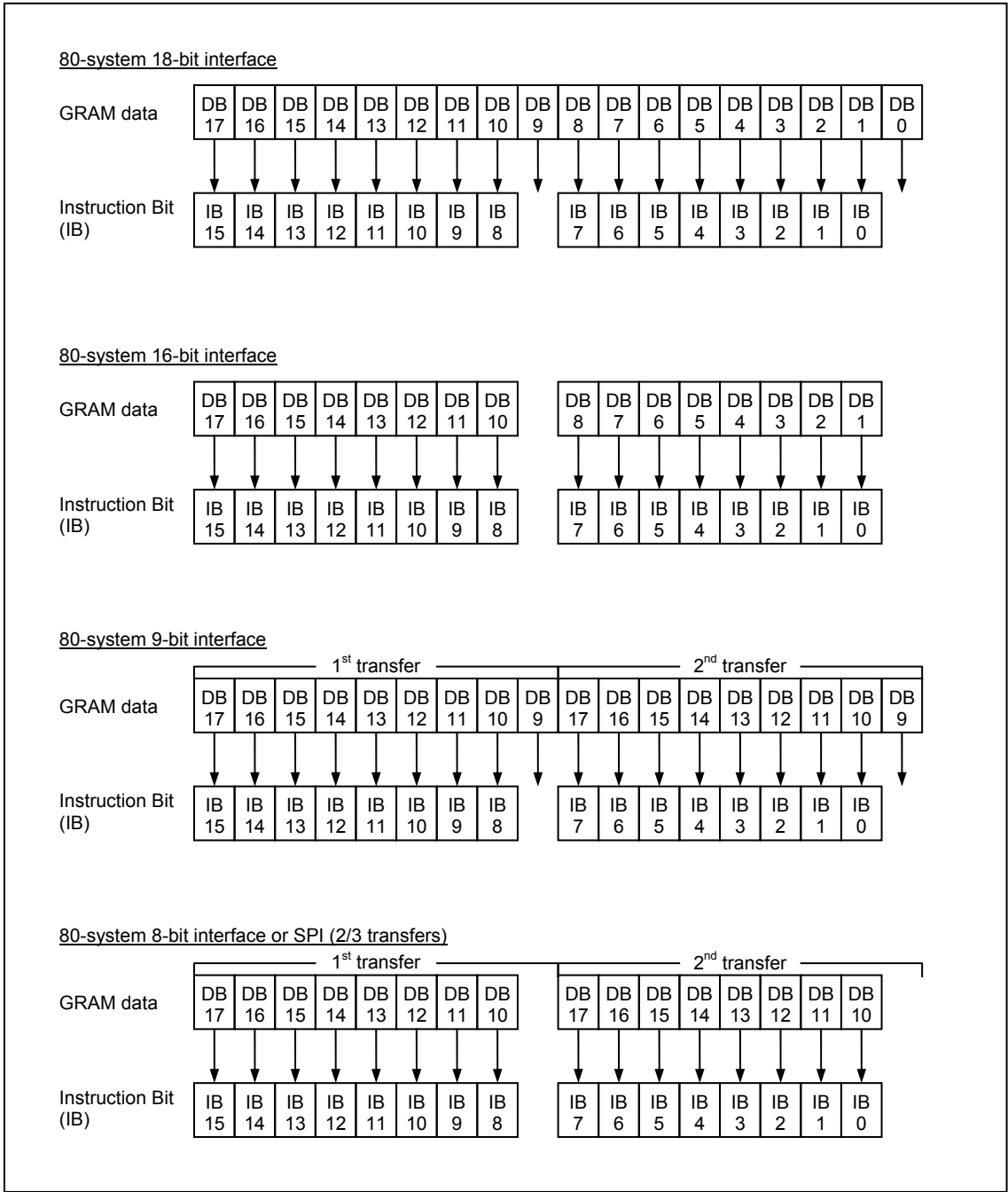


Figure 8 Instruction bits

## Instruction Description

The following are detailed explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

### Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h - RFFh) of a control register or RAM control to be accessed using binary numbers “0000\_0000” to “1111\_1111”. An access to the register as well as instruction bits contained in it is disabled unless its index is represented in this register.

### Device code read (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1

The device code “4535”H is read out when reading out this register forcibly.

### Driver output control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

**SS** – Selects the shift direction of outputs from the source pins.

If SS = “0”, the source pins output from S1 to S720.

If SS = “1”, the source pins output from S720 to S1.

The combination of SS and BGR bits controls the order of assigning RGB dots to the source driver pins S1 to S720.

If SS = “0” and BGR = “0”, RGB dots are assigned interchangeably from S1 to S720.

If SS = “1” and BGR = “1”, RGB dots are assigned interchangeably from S720 to S1.

When changing SS or BGR bits, RAM data must be rewritten.

**SM** – Sets gate driver assignment in combination with the GS bit according to the LC module. See “Scan mode setting”.

### LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	BC0	EOR	0	0	NW[5:0]					

**NW[5:0]** – Specify n, the number of raster-rows from 1 to 64, where alternations occurs every n+1 raster-rows when C-pattern waveform is generated(BC0=1).

**EOR** – When EOR=1, alternation occurred by applying EOR(Exclusive OR) operatin to an odd/even frame selecting signal and n-raster-row inversion signal while a C-patten waveform is generated(BC0=1).



This instruction is used when liquid crystal alternation drive is not available due to combination of numbers of LCD raster-rows and the value of “x n”. For details, see n-raster-row Inversion Alternating Drive.

**BC0** – Selects the liquid crystal drive waveform VCOM. See “Line Inversion AC Drive” for details.

BC0 = 0: frame inversion waveform is selected.

BC0 = 1: Line inversion waveform is selected.

In either liquid crystal drive method, the polarity inversion is halted in blank periods (back and front porch periods).

## Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D[1:0]	AM	0	EPF[1:0]		

The LGDP4535 modifies data sent from a microcomputer before writing them to the internal GRAM in order to write the GRAM data in high speed and reduce software processing load on the microcomputer. See “Graphics Operation Function” for details.

**TRI** – Selects the RAM data transfer mode in 80-system 8-bit/16-bit bus interface operation.

In 8-bit interface operation,

TRI = 0: 16-bit RAM data is transferred in two transfers.

TRI = 1: 18-bit RAM data is transferred in three transfers.

In 16-bit bus interface operation,

TRI = 0: 16-bit RAM data is transferred in one transfer.

TRI = 1: 18-bit RAM data is transferred in two transfers.

Make sure TRI = 0 when not using either 16-bit or 8-bit interface. Also, set TRI = 0 during read operation.

**DFM** – Sets the mode of transferring data to the internal RAM when TRI = “1”. See the following figures for details.

**Table 10**

TRI	DFM	RAM write data transfer via serial peripheral interface (SPI)
0	*	<p><u>SPI (2 transfers/pixel) – 65k colors available</u></p>
1	0	<p><u>SPI (3 transfers/pixel) – 262k colors available</u></p>
1	1	Setting disabled

Table 11

TRI	DFM	RAM write data transfer via 8-bit interface
0	*	<p><u>80-system 8-bit interface (2 transfers/pixel) – 65k colors</u></p>
1	0	<p><u>80-system 8-bit interface (3 transfers/pixel) – 262k colors</u></p>
1	1	<p><u>80-system 8-bit interface (3 transfers/pixel) – 262k colors</u></p>

Table 12

TRI	DFM	RAM write data transfer via 16-bit interface
0	*	<p><u>80-system 16-bit interface (1 transfers/pixel) – 65k colors</u></p>
1	0	<p><u>80-system 16-bit interface MSB mode(2 transfers/pixel) – 262k colors available</u></p>
1	1	<p><u>80-system 16-bit interface LSB mode(2 transfers/pixel) – 262k colors available</u></p>

**BGR** – Reverses the order of RGB dots to BGR when writing 18-bit pixel data to the internal GRAM.

BGR = 0 : Write source data in order of R-G-B.

BGR = 1 : Change the order with B-G-R.

**ORG** – Moves the origin of a window address area in combination with the ID setting. This function is enabled when writing data within the window address area.

**I/D[1:0]** – The address counter is automatically incremented by 1 as writing data to the internal GRAM when I/D[1:0] = “1”. The address counter is automatically decremented by 1 as writing data to the internal GRAM when I/D[1:0] = “0”. The increment/decrement can be set separately to each upper (AD[15:8]) / lower (AD[7:0]) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal GRAM is set with the AM bit.

**AM** – Sets the direction of automatically updating address for writing data to the internal RAM in the address counter (AC). When AM = “0”, the address is updated in horizontal writing direction. When AM = “1”, the address is updated in vertical writing direction. When a window address area is set, data are written only to the GRAM area specified with window address in the writing direction set with I/D[1:0] and AM bits.

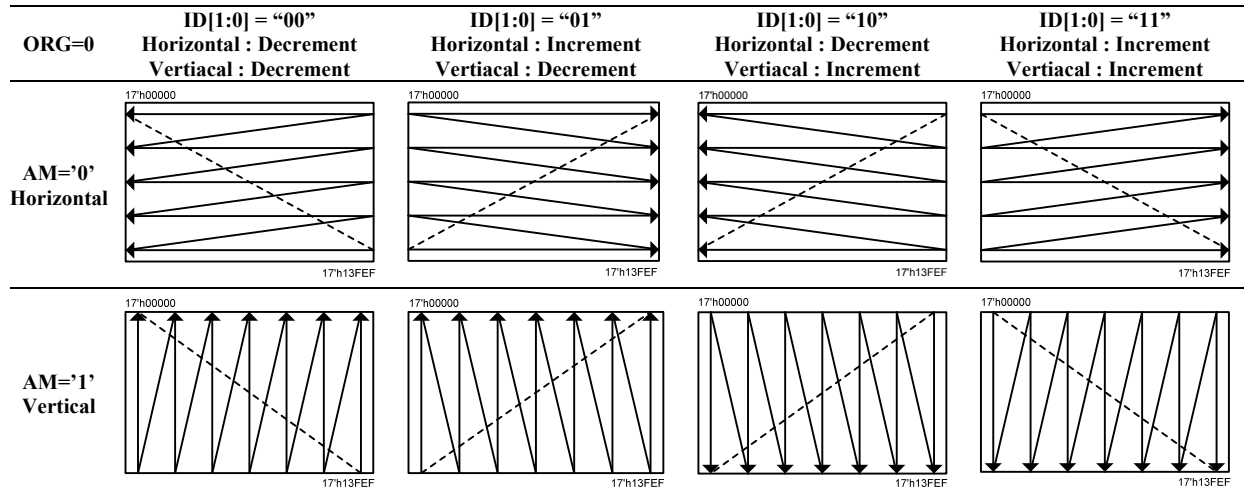


Figure 9 Automatic address update (ORG=0, AM, ID)

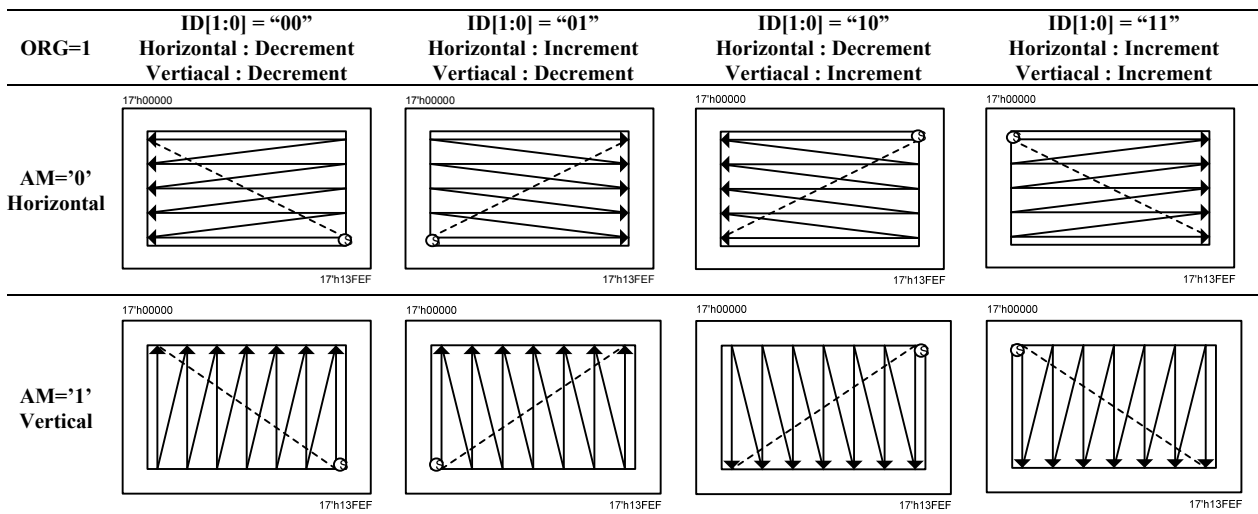


Figure 10 Automatic address update (ORG=1, AM, ID)

**EPF[1:0]** – Set the data format when 16bpp(R,G and B) to 18bpp(r, g and b) is stored in internal RAM.

EPF settings are effective when :

1. 80-system 16-bit interface, TRI = 0
2. 80-system 8-bit interface, TRI = 0
3. Clock synchronous serial interface

**Table 13**

EPF	Expand 16bpp(R,G,B) to 18bpp(r,g,b)
2'h0	Same vaule as MSB is inputted to LSB of R and B $r[5:0] = \{R[4:0], R[4]\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], B[4]\}$
2'h1	“0” is inputted to LSB of r and b $r[5:0] = \{R[4:0], 1'b0\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 1'b0\}$ Except. $R[4:0], B[4:0] = 5'h1F \rightarrow r,b[5:0] = 6'h3F$ $G[5:0] = 6'h3F \rightarrow g[5:0] = 6'h3F$
2'h2	“1” is inputted to LSB of r and b $r[5:0] = \{R[4:0], 1'b1\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 1'b1\}$ Except. $R[4:0], B[4:0] = 5'h00 \rightarrow r,b[5:0] = 6'h00$ $G[5:0] = 6'h00 \rightarrow g[5:0] = 6'h00$
2'h3	Setting disabled

## Resizing Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV[1:0]	0	0	RCH[1:0]	0	0	0	0	RSZ[1:0]	

**RSZ[1:0]** – Sets the resizing factor. When the RSZ bits are set for resizing, the LGDP4535 writes the data of the resized image in both horizontal and vertical directions according to the resizing factor on the internal GRAM. See “Resizing fuction”.

**RCH[1:0]** – Sets the number of pixels made as the remainder in horizontal direction as a result of resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

**RCV[1:0]** – Sets the number of pixels made as the remainder in vertical direction as a result of resizing a picture. By specifying the number of remainder pixels with RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ=2'h0) or there are no remainder pixels.

**Table 14**

RSZ[1:0]	Resizing scale
2'h0	No resizing ( x1)
2'h1	x 1/2
2'h2	Setting disabled
2'h3	x 1/4

**Table 15**

RCH[1:0]	Number of remainder Pixels in Horizontal Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

**Table 16**

RCV[1:0]	Number of remainder Pixels in Vertical Direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

## Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE[1:0]	0	0	0	BASEE	0	0	GON	DTE	COL	0		D[1:0]	

**D[1:0]** – A graphics display appears on the screen when D[1] = “1”, and is turned off upon setting D[1] = “0”. When setting D[1] = “0”, the graphics display data are retained in the internal GRAM and the display appears instantly on the screen upon setting D[1] to “1”. When the D[1] bit is “0”, i.e. while no display is shown on the screen, all source outputs are at the GND level to reduce charging/discharging current on liquid crystal cells, which is generated during liquid crystal AC drive.

When the display is turned off by setting D[1:0] = 2'h1, the LGDP4535 continues internal display operation. When the display is turned off by setting D[1:0] = 2'h0, the LGDP4535's internal display operation is halted completely. In combination with GON bit, the D[1:0] bits control ON/OFF of graphics display. For details, see “Instruction setting”.

**Table 17**

D[1:0]	BASEE	Source Output (S1-720)	FMARK signal	Internal Operation
2'h0	*	GND	Halt	Halt
2'h1	*	GND	Operation	Operation
2'h2	*	Non-display	Operation	Operation
2'h3	0	Non-display	Operation	Operation
	1	Base-image display	Operation	Operation

Notes: 1. The data write operation from the microcomputer is not affected by the setting in the D[1:0] bits.

## 2. The PTS bits set the source output level for “non-lit display”

**COL** – When COL = “1”, the 8-color display mode is selected. For details, see the “8-color Display Mode” section. The 8-color display mode is not available in external interface mode.

**Table 18**

COL	Operating amplifier	Display color
1'h0	64	262,144
1'h1	2	8

Note: When COL=1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

**GON, DTE** – The combination of settings in GON and DTE bits sets the output level form gate lines(G1-G320). When GON=0, the Vcom output level becomes the GND level.

**Table 19**

GON	DTE	G1-G320
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

**BASEE** – Base image display enable bit.

BASEE = 0 : No base image is displayed. The LGDP4535 drives liquid crystal at no-display level or shows only partial images on the screen.

BASEE = 1 : A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

**PTDE[1:0]** – PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of partial image 2. When PTDE[1]/[0]=0, the partial image is turned off and only base image is displayed on the screen. When PTDE[1]/[0]= 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

## Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	FP[7:0]								BP[7:0]							

**FP[7:0]/BP[7:0]** – Sets the blank period made at the beginning and the end of a display (front porch and back porch, respectively). The FP[7:0] and BP[7:0] bits specify the number of lines for the front and back porch periods, respectively. In setting, be sure:

FP ≥ 2 lines

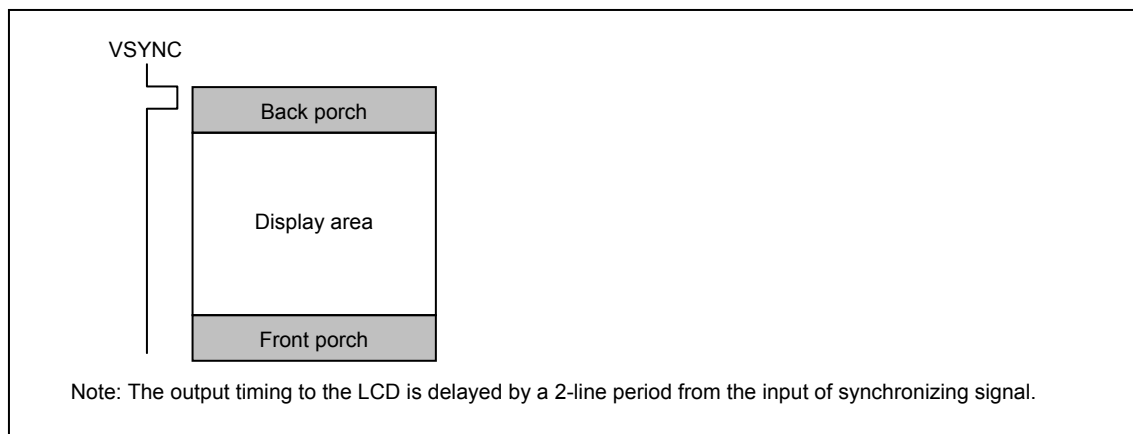
BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front

porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal.

**Table 20**

FP[7:0]/BP[7:0]	Number of lines for the front/back porches
8'h00	Setting disabled
8'h01	Setting disabled
8'h02	2 lines
8'h03	3 lines
8'h04	4 lines
8'h05	5 lines
8'h06	6 lines
8'h07	7 lines
8'h08	8 lines
8'h09	9 lines
8'h0A	10 lines
8'h0B	11 lines
:	:
8'hED	253 lines
8'hFE	254 lines
8'hFF	255 lines



**Figure 11 Back/front porches**

Set the BP[7:0], FP[7:0] bits as follows in each operation mode.

**Table 21**

<b>Internal clock operation</b>	BP $\geq$ 2 lines	FP $\geq$ 2 lines
<b>RGB interface</b>	BP $\geq$ 2 lines	FP $\geq$ 2 lines
<b>VSYNC interface</b>	BP $\geq$ 2 lines	FP $\geq$ 2 lines

### Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS[2:0]	0	0	0	0	PTG[1:0]			ISC[3:0]		

**ISC[3:0]** – Set the interval of scan when PTG[1:0] sets the interval scan. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal is inverted in the same cycle as the interval scan.

Table 22

ISC[3:0]	Scan cycle	Time for interval when(fFLM)=60Hz
4'h0	Setting disabled	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

**PTG[1:0]** – Set the scan mode in non-display area, which is made between partial display periods of the first and the second images, or turning off both base and partial images(full-screen non display). The setting is commonly applied to all non-display drive period.

Table 23

PTG[1:0]	Gate drive operation In non-display area	Source output level In non-display area	Vcom output
2'h0	Normal scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h1	Setting disabled	-	-
2'h2	Interval scan	PTS[2:0] setting	VcomH/VcomL amplitude
2'h3	Setting disabled	-	-

Note: Select frame-inversion AC drive when setting interval scan.

**PTS[2:0]** – Set the source output in non-display drive period.

Table 24

PTS[2:0]	Source output level		Grayscale amplifier In operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3h0	V63	V0	V0 to V63	Register setting(DC0,DC1)
3h1	Setting disabled	Setting disabled	-	-
3h2	GND	GND	V0 to V63	Register setting(DC0,DC1)
3h3	Hi-Z	Hi-Z	V0 to V63	Register setting(DC0,DC1)
3'h4	V63	V0	V0 and V63	1/2 the frequency set with DC0,DC1
3'h5	Setting disabled	Setting disabled	-	-



3'h6	GND	GND	V0 and V63	1/2 the frequency set with DC0,DC1
3'h7	Hi-Z	Hi-Z	V0 and V63	1/2 the frequency set with DC0,DC1

Notes: 1. The gate output level in non-display drive period is controlled by the PTG setting(off-scan mode).

### Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE		FMI[2:0]	

**FMI[2:0]** – Set the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

**FMARKOE** – When FMARKOE=1, the LGDP4535 starts outputting FMARK signal from the FMARK pin in the output interval set with the FMI[2:0] bits. See “FMARK” for details.

**Table 25**

FMI[2:0]	Output interval
3'h0	1 frame
3'h1	2 frame
3'h3	4 frame
3'h5	6 frame
Others settings	Setting disabled

### External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	ENC[2:0]			0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

**ENC[2:0]** – Sets the RAM data write cycle in RGB interface mode.

**Table 26 ENC[2:0] bits**

ENC[2:0]	RAM data write cycle (frame periods)
3'h0	1 frame
3'h1	
3'h2	
3'h3	

**RM** – Selects the interface to access the LGDP4535's internal GRAM. The RAM access is possible only via the interface selected with the RM bit. Set RM to “1” when writing display data via the RGB interface. The LGDP4535 allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = “0” even while display operations are performed via the RGB interface.

**Table 27 RM bit**

RM	Interface for RAM access
1'h0	System interface/VSYNC interface
1'h1	RGB interface

**RIM[1:0]** – Selects one of the following RGB interface modes when the RGB interface mode is selected with the RM and DM bits. Make this setting before display operation via external display interface. Do not make changes to the setting during display operation.

**Table 28 RIM[1:0] bits**

<b>RIM[1:0]</b>	<b>RGB interface mode</b>
2'h00	18-bit RGB interface (1 transfer/pixel)
2'h01	16-bit RGB interface (1 transfer/pixel)
2'h10	6-bit RGB interface (3 transfers/pixel)
2'h11	Setting disabled

**DM[1:0]** – Sets the display operation mode. By setting DM[1:0] as follows, it is possible to switch between the internal clock operation mode and the external display interface mode. Do not switch between different external interface modes (RGB interface and VSYNC interface).

**Table 29 DM[1:0] bits**

<b>DM[1:0]</b>	<b>Display operation mode</b>
2'h00	Internal clock operation
2'h01	RGB interface
2'h10	VSYNC interface
2'h11	Setting disabled

**Notes:**

1. Instructions are set only via the system interface.
2. Be sure that data transfer and dot clock input are performed in units of RGB dots in 6-bit RGB interface mode.

As the following table, the optimum interface for the state of display can be selected by setting the external display interface mode.

**Table 30**

<b>Display State</b>	<b>Operation mode</b>	<b>RAM access (RM)</b>	<b>Display mode (DM)</b>
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 01)
Rewrite still picture area while display moving pictures	RGB interface (2)	System interface (RM = 0)	RGB interface (DM = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 10)

**Notes:**

1. Instructions are set only via the system interface.
2. The RGB-I/F and the VSYNC-I/F are not used simultaneously.
3. Do not make changes to the RGB-I/F mode setting (RIM) while the RGB I/F is in operation.
4. See the “External Display Interface” section for the flowcharts to follow when switching from one mode to another.

## Internal clock operation mode

All display operations are synchronized with the signals generated from the internal operating clock in this mode. None of inputs via the external display interface are valid. The internal RAM is accessible only via the system interface.

## RGB interface mode (1)

In RGB interface mode, display operations are synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clock (DOTCLK). These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels via the DB[17:0] pins. All display data are stored in the internal RAM. The combined use of the high-speed RAM write mode and the widow address function enables not only displaying data in moving picture area and data in the internal RAM in other than the moving picture area at a time but also minimizing data transfer by transferring data only when rewriting screen.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated inside the LGDP4535 by internally counting the number of line synchronizing signal clocks (HSYNC) from the falling edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring RGB data via the DB[17:0] pins.

## RGB interface mode (2)

The LGDP4535 enables rewriting RAM data via the system interface while the RGB interface is selected for display operation. In this case, Be sure to write RAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE bit first and then set a new address (AD[15:0]) in the AC and the index register to R22h.

## VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the frame synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal RAM at more than the minimum speed from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and method. For details, see “External Display Interface”.

No external signal input except VSYNC input is accepted in VSYNC interface mode.

The timings and durations of front porch (FP), back porch (BP) periods and display duration period (NL) are automatically calculated from the falling edge of the frame synchronization signal (VSYNC) according to the instructions set in the relevant registers.

## Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	FMP[9:0]									

**FMP[9:0]** – Sets the output position of frame cycle signal (frame marker). When FMP[9:0] = 10'h000, a high-active pulse FMARK is output at the start of back porch period for 1H period (IOVcc-IOGND amplitude signal). FMARK can be used as a trigger signal for frame synchronous write operation. See “FMARK” for details.

Make sure  $10'h000 \leq \text{FMP} \leq \text{BP} + \text{NL} + \text{FP}$

**Table 31**

<b>FMP[9:0]</b>	<b>FMARK output position</b>
10'h000	0 <sup>th</sup> line
10'h001	1 <sup>st</sup> line
10'h002	2 <sup>nd</sup> line
:	:
10'h2AC	684 <sup>rd</sup> line
10'h2AD	685 <sup>th</sup> line
10'h2AE	686 <sup>th</sup> line
10'h2AF	687 <sup>th</sup> line

### External Display Interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

**DPL** – Sets the signal polarity of DOTCLK pin.

DPL = 0 : input data on the rising edge of DOTCLK  
DPL = 1 : input data on the falling edge of DOTCLK

**EPL** – Sets the signal polarity of ENABLE pin.

EPL = 0 : writes data DB[17:0] when ENABLE = 0 and disables data write operation when ENABLE = 1.  
EPL = 1 : writes data DB[17:0] when ENABLE = 1 and disables data write operation when ENABLE = 0.

**HSPL** – Sets the signal polarity of HSYNC pin.

HSPL = 0 : Low active

HSPL = 1 : High active

**VSPL** – Sets the signal polarity of VSYNC pin.

VSPL = 0 : Low active

VSPL = 1 : High active

### Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP[2:0]				BT[2:0]		0	AP[2:0]			DK	DSTB	SLP	STB	

**STB** – When STB = “1”, the LGDP4535 enters the standby mode. In standby mode, the display operation completely halts, and the internal operation, including internal RC oscillation and reception of external clock pulses, completely halts. Only instructions to release the LGDP4535 from the standby mode (STB = “0”) and to start oscillators are accepted during the standby mode. To set the standby mode, follow the sequence of standby mode setting.

**SLP** – When SLP = 1, the LGDP4535 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change of GRAM data or instruction is accepted in sleep mode. The GRAM data and the instruction bits remain unchanged.

**DSTB** – When DSTB = 1, the LGDP4535 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and the instruction bit setting are destroyed and must be reset after exiting deep standby mode.

**DK** – Activates DDVDH. When DK = 0, DDVDH activates at the same timing as VGH. When DK = 1, DDVDH activates separately from VGH.

**Table 32**

<b>DK</b>	<b>Step-up Cycle in Step-up Circuit 1</b>
1'h0	Startup DDVDH simultaneously with VGH. Startup step-up circuit 1 (VLOUT1 output) according to AP[2:0]
1'h1	Halt step-up circuit 1 (VLOUT1). (Default)

**AP[2:0]** – Adjusts the constant current in the operation amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0]=3'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Adjust the amount of fixed current from the fixed-current source in the internal operational amplifier circuit. VGH operates when AP is not 000. Complete setting AP before setting PON = 1. (While setting PON = 1, setting of AP bit cannot be changed.) For the details of sequences, refer to Flow of “Power Supply Setting”.

**Table 33**

<b>AP[2:0]</b>	<b>LCD power supply circuits</b>	<b>Grayscale voltage generating circuit</b>
3'h0	Halt operation	Halt operation
3'h1	Setting disabled	Setting disabled
3'h2	Normal operation	0.5
3'h3	Normal operation	0.75
3'h4	Normal operation	1
3'h5	Normal operation	1.25
3'h6	Normal operation	1.5
3'h7	Setting disabled	Setting disabled

Note: In this table, the constant current in operational amplifiers is shown by the ratio to the constant current when AP[1:0] is set to 2'h3.

**BT[2:0]** – Sets the factor used in the step-up circuits. Use an optimal step-up factor for the voltage in use. To reduce power consumption, set a smaller factor.

**Table 34 Step up factor and output voltage level**

BT[2:0]	DDVDH	VGH	VGL	Capacitor connection Pins
3'h0			$-(V_{ci1} + DDVDH \times 2)$ [x -5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
3'h1		DDVDH x 3 [x 6]	$-(DDVDH \times 2)$ [x -4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
3'h2			$-(V_{ci1} + DDVDH)$ [x -3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
3'h3	Vci1 x 2 [x 2]		$-(V_{ci1} + DDVDH \times 2)$ [x -5]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
3'h4		Vci1 + DDVDH x 2 [x 5]	$-(DDVDH \times 2)$ [x -4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
3'h5			$-(V_{ci1} + DDVDH)$ [x -3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±
3'h6		DDVDH x 2 [x 4]	$-(DDVDH \times 2)$ [x -4]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C21±, C22±
3'h7			$-(V_{ci1} + DDVDH)$ [x -3]	VLOUT1, VLOUT2, VLOUT3, C11±, C12±, C13±, C21±, C22±

Note: 1. The step-up factor from Vci1 are shown in the brackets [ ].  
 2. Connect capacitors where required when using DDVDH, VGH, VGL voltages.  
 3. Set the following voltages within the respective ranges:  
 DDVDH = 6.0V(max.), VGH = 15.0V (max.) and VGL = -12.5V (max.)

**SAP[2:0]** – Adjust the constant current for the operational amplifier circuit in the source driver. A larger constant current stabilizes the operational amplifier circuit, but current consumption increases. Adjust the constant current taking the display quality-current consumption trade-off into account. During a period showing no display, set SAP = 0 to halt the operational amplifier circuit to reduce current consumption.

**Table 35**

SAP[2:0]	Constant current (ratio to 3)
3'h0	Halt operational amplifier
3'h1	Constant current (ratio to 3) : 0.65
3'h2	Constant current (ratio to 3) : 0.8
3'h3	Constant current (ratio to 3) : 1.00
3'h4	Constant current (ratio to 3) : 1.35
3'h5	Constant current (ratio to 3) : 1.60
3'h6	Setting disabled
3'h7	Setting disabled

## Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC1[2:0]		0	DC0[2:0]		0	VC[2:0]				

**Table 36 Step-up frequency (Step-up Circuit 1)**

DC0[2:0]	Step-up circuit 1 : step-up frequency ( $f_{\text{DCDC1}}$ )
3'h0	$f_{\text{osc}}/16$
3'h1	$f_{\text{osc}}/32$
3'h2	$f_{\text{osc}}/64$
3'h3	$f_{\text{osc}}/128$
3'h4	$f_{\text{osc}}/256$
3'h5	$f_{\text{osc}}/8$
3'h6	Halt step-up circuit 1
3'h7	$f_{\text{osc}}/4$

Note : Make sure to set DC0 and DC1 to maintain  $f_{\text{DCDC1}} \geq f_{\text{DCDC2}}$ .

**Table 37 Step-up frequency (Step-up Circuit 2)**

DC1[2:0]	Step-up circuit 2 : step-up frequency ( $f_{\text{DCDC2}}$ )
3'h0	$f_{\text{osc}}/128$
3'h1	$f_{\text{osc}}/256$
3'h2	$f_{\text{osc}}/512$
3'h3	$f_{\text{osc}}/1024$
3'h4	$f_{\text{osc}}/2048$
3'h5	$f_{\text{osc}}/64$
3'h6	Halt step-up circuit 2
3'h7	$f_{\text{osc}}/32$

Note : Make sure to set DC0 and DC1 to maintain  $f_{\text{DCDC1}} \geq f_{\text{DCDC2}}$ .

**Table 38 VciOUT output level**

VC[2:0]	VciOUT (Reference Voltage) (VciLVL Voltage)
3'h0	$1.00 \times \text{VciLVL}$
3'h1	$0.92 \times \text{VciLVL}$
3'h2	$0.90 \times \text{VciLVL}$
3'h3	$0.87 \times \text{VciLVL}$
3'h4	$0.85 \times \text{VciLVL}$
3'h5	$0.83 \times \text{VciLVL}$
3'h6	$0.73 \times \text{VciLVL}$
3'h7	Setting disabled

### Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH[3:0]			

**VRH[3:0]** – Sets the factor to generate VREG1OUT from VciLVL.

**Table 39 VREG1OUT**

VRH[3:0]	VREG1OUT Voltage
4'h0	VciOUT x 1.27
4'h1	VciOUT x 1.32
4'h2	VciOUT x 1.37
4'h3	VciOUT x 1.42
4'h4	VciOUT x 1.47
4'h5	VciOUT x 1.52
4'h6	VciOUT x 1.57
4'h7	Setting disabled
4'h8	Setting disabled
4'h9	VciOUT x 1.62
4'hA	VciOUT x 1.67
4'hB	VciOUT x 1.72
4'hC	VciOUT x 1.77
4'hD	VciOUT x 1.82
4'hE	VciOUT x 1.87
4'hF	VciOUT x 1.92

Note: Set the VC and VRH bits to maintain the VREG1OUT voltage at (DDVDH – 0.5) V or less.

**PON** – Controls the operation to generate VLOUT3. In setting the PON bit, follows the power-supply startup sequence.

PON = 0 : Halts the step-up operation to generate VLOUT3.

PON = 1 : Starts the step-up operation to generate VLOUT3.

### Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV[4:0]				0	VCM[6:0]							

**VCM[6:0]** – Sets the VcomH level (the higher voltage of Vcom alternating drive). VCM[6:0] specifies the voltage by VREG1OUT x n, where n is a discrete number from 0.400 to 0.875. To halt internal volume and adjust VcomH with an external resistor from VcomR, set VCM[6:0] = “111111”.



**Table 40**

VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH
7'h00	VREG1OUT x 0.400	7'h20	VREG1OUT x 0.560	7'h40	VREG1OUT x 0.720	7'h60	VREG1OUT x 0.880
7'h01	VREG1OUT x 0.405	7'h21	VREG1OUT x 0.565	7'h41	VREG1OUT x 0.725	7'h61	VREG1OUT x 0.885
7'h02	VREG1OUT x 0.410	7'h22	VREG1OUT x 0.570	7'h42	VREG1OUT x 0.730	7'h62	VREG1OUT x 0.890
7'h03	VREG1OUT x 0.415	7'h23	VREG1OUT x 0.575	7'h43	VREG1OUT x 0.735	7'h63	VREG1OUT x 0.895
7'h04	VREG1OUT x 0.420	7'h24	VREG1OUT x 0.580	7'h44	VREG1OUT x 0.740	7'h64	VREG1OUT x 0.900
7'h05	VREG1OUT x 0.425	7'h25	VREG1OUT x 0.585	7'h45	VREG1OUT x 0.745	7'h65	VREG1OUT x 0.905
7'h06	VREG1OUT x 0.430	7'h26	VREG1OUT x 0.590	7'h46	VREG1OUT x 0.750	7'h66	VREG1OUT x 0.910
7'h07	VREG1OUT x 0.435	7'h27	VREG1OUT x 0.595	7'h47	VREG1OUT x 0.755	7'h67	VREG1OUT x 0.915
7'h08	VREG1OUT x 0.440	7'h28	VREG1OUT x 0.600	7'h48	VREG1OUT x 0.760	7'h68	VREG1OUT x 0.920
7'h09	VREG1OUT x 0.445	7'h29	VREG1OUT x 0.605	7'h49	VREG1OUT x 0.765	7'h69	VREG1OUT x 0.925
7'h0A	VREG1OUT x 0.450	7'h2A	VREG1OUT x 0.610	7'h4A	VREG1OUT x 0.770	7'h6A	VREG1OUT x 0.930
7'h0B	VREG1OUT x 0.455	7'h2B	VREG1OUT x 0.615	7'h4B	VREG1OUT x 0.775	7'h6B	VREG1OUT x 0.935
7'h0C	VREG1OUT x 0.460	7'h2C	VREG1OUT x 0.620	7'h4C	VREG1OUT x 0.780	7'h6C	VREG1OUT x 0.940
7'h0D	VREG1OUT x 0.465	7'h2D	VREG1OUT x 0.625	7'h4D	VREG1OUT x 0.785	7'h6D	VREG1OUT x 0.945
7'h0E	VREG1OUT x 0.470	7'h2E	VREG1OUT x 0.630	7'h4E	VREG1OUT x 0.790	7'h6E	VREG1OUT x 0.950
7'h0F	VREG1OUT x 0.475	7'h2F	VREG1OUT x 0.635	7'h4F	VREG1OUT x 0.795	7'h6F	VREG1OUT x 0.955
7'h10	VREG1OUT x 0.480	7'h30	VREG1OUT x 0.640	7'h50	VREG1OUT x 0.800	7'h70	VREG1OUT x 0.960
7'h11	VREG1OUT x 0.485	7'h31	VREG1OUT x 0.645	7'h51	VREG1OUT x 0.805	7'h71	VREG1OUT x 0.965
7'h12	VREG1OUT x 0.490	7'h32	VREG1OUT x 0.650	7'h52	VREG1OUT x 0.810	7'h72	VREG1OUT x 0.970
7'h13	VREG1OUT x 0.495	7'h33	VREG1OUT x 0.655	7'h53	VREG1OUT x 0.815	7'h73	VREG1OUT x 0.975
7'h14	VREG1OUT x 0.500	7'h34	VREG1OUT x 0.660	7'h54	VREG1OUT x 0.820	7'h74	VREG1OUT x 0.980
7'h15	VREG1OUT x 0.505	7'h35	VREG1OUT x 0.665	7'h55	VREG1OUT x 0.825	7'h75	Setting disabled
7'h16	VREG1OUT x 0.510	7'h36	VREG1OUT x 0.670	7'h56	VREG1OUT x 0.830	7'h76	Setting disabled
7'h17	VREG1OUT x 0.515	7'h37	VREG1OUT x 0.675	7'h57	VREG1OUT x 0.835	7'h77	Setting disabled
7'h18	VREG1OUT x 0.520	7'h38	VREG1OUT x 0.680	7'h58	VREG1OUT x 0.840	7'h78	Setting disabled
7'h19	VREG1OUT x 0.525	7'h39	VREG1OUT x 0.685	7'h59	VREG1OUT x 0.845	7'h79	Setting disabled
7'h1A	VREG1OUT x 0.530	7'h3A	VREG1OUT x 0.690	7'h5A	VREG1OUT x 0.850	7'h7A	Setting disabled
7'h1B	VREG1OUT x 0.535	7'h3B	VREG1OUT x 0.695	7'h5B	VREG1OUT x 0.855	7'h7B	Setting disabled
7'h1C	VREG1OUT x 0.540	7'h3C	VREG1OUT x 0.700	7'h5C	VREG1OUT x 0.860	7'h7C	Setting disabled
7'h1D	VREG1OUT x 0.545	7'h3D	VREG1OUT x 0.705	7'h5D	VREG1OUT x 0.865	7'h7D	Setting disabled
7'h1E	VREG1OUT x 0.550	7'h3E	VREG1OUT x 0.710	7'h5E	VREG1OUT x 0.870	7'h7E	Setting disabled
7'h1F	VREG1OUT x 0.555	7'h3F	VREG1OUT x 0.715	7'h5F	VREG1OUT x 0.875	7'h7F	Halt internal volume.

Note : Set the VcomH voltage from VCI to (DDVDH – 0.5 )V

**VDV[4:0]** – Sets the alternating amplitudes of VCOM AC voltage. These bits amplify VCOM by from 0.6 to 1.23 times the VREG1OUT voltage. If VCOMG = 0, VDV[4:0] bits are disabled.

**Table 41**

VDV[4:0]	Vcom amplitude	VDV[4:0]	Vcom amplitude
5'h00	VREG1OUT x 0.60	5'h10	VREG1OUT x 1.05
5'h01	VREG1OUT x 0.63	5'h11	VREG1OUT x 1.08
5'h02	VREG1OUT x 0.66	5'h12	VREG1OUT x 1.11
5'h03	VREG1OUT x 0.69	5'h13	VREG1OUT x 1.14
5'h04	VREG1OUT x 0.72	5'h14	VREG1OUT x 1.17
5'h05	VREG1OUT x 0.75	5'h15	VREG1OUT x 1.20
5'h06	VREG1OUT x 0.78	5'h16	VREG1OUT x 1.23
5'h07	VREG1OUT x 0.81	5'h17	VREG1OUT x 1.26
5'h08	VREG1OUT x 0.84	5'h18	VREG1OUT x 1.29
5'h09	VREG1OUT x 0.87	5'h19	VREG1OUT x 1.32
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.35
5'h0B	VREG1OUT x 0.93	5'h1B	VREG1OUT x 1.38
5'h0C	VREG1OUT x 0.96	5'h1C	VREG1OUT x 1.41
5'h0D	VREG1OUT x 0.99	5'h1D	VREG1OUT x 1.44
5'h0E	VREG1OUT x 1.02	5'h1E	VREG1OUT x 1.47
5'h0F	Setting disabled	5'h1F	VREG1OUT x 1.50

Note : Set the VcomL voltage from (VCL + 0.5)V to 0V

**VCOMG** – When VCOMG = 1, the LGDP4535 can output a negative voltage level for VCOML (0V ~ - (VCL + 0.5V) Max. ). When VCOMG = 0, the output of VCOML is fixed to GND level, and setting of the VDV[4:0] bits become invalid. And LGDP4535 halts the amplifier for negative voltage to save power. In this case, adjust the amplitude of (VCOMH-VCOML) voltage only with VCM[6:0] bits. VCOMG = 1 is valid only when PON = 1. So set PON = 1 ahead, before setting VCOMG = 1. In addition, set CMFPD = 1 ahead, before setting VCOMG = 0 on the frame inversion driving mode.

## Regulator Control (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	RSET			0	RI[2:0]		0	RV[2:0]			0	RCONT[2:0]			

**RCONT[2:0]** – These bits control the input voltage of main bias op\_amp.

**Table 42**

RCONT[2:0]	Input voltage
3'h0	Vci x 0.25
3'h1	Setting disabled
3'h2	Open
3'h3	Vci x 0.30
3'h4	Setting disabled
3'h5	Setting disabled
3'h6	Vci x 0.20
3'h7	Setting disabled

**RV[2:0]** – These bits control the output voltage of internal logic regulator.

**Table 43**

<b>RV [2:0]</b>	<b>Vdd voltage</b>
3'h0	Vci x 0.80
3'h1	Vci x 0.75
3'h2	Vci x 0.70
3'h3	Vci x 0.65
3'h4	Vci x 0.60
3'h5	Vci x 0.55
3'h6	Vci x 0.50
3'h7	Vci x 0.45

**RI[2:0]** – These bits control the bias current of internal logic regulator.

**Table 44**

<b>RI [2:0]</b>	<b>Constant current</b>
3'h0	0.2
3'h1	0.1
3'h2	2.2
3'h3	3
3'h4	3.2
3'h5	4
3'h6	5.2
3'h7	6

Note : In this table, the constant current is shown by the ratio to the constant current when RI[2:0] is set to 3'h3.

**RSET[2:0]** – These bits control the main bias.

## **Gamma Select Control (R16h)**

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	EN_MA	0	0	0	PS

**PS** – This bit specify the VA mode enable signal.

**Table 45**

<b>PS</b>	<b>Mode</b>
1'h0	TN mode
1'h1	VA mode

**EN\_MA** – This bit specify the PFN0-5/PFP0-1/PMN/PMP registers Manual setting enable signal

**Table 46**

		<b>EN_MA</b>	<b>PS</b>
Auto	TN mode	0	0
	VA mode	0	1
Manual	User setting	1	x

## ***Vcom Control (R17h)***

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	LSZ[2:0]		0	HSZ[2:0]			0	0	0	CMFPD	

**LSZ[2:0]** – This register controls VcomL amplifier to reduce cross-talk in frame inversion.

**HSZ[2:0]** – This register controls VcomH amplifier to reduce cross-talk in frame inversion.

**CMFPD** – Enable bit to use LSZ[2:0], HSZ[2:0] registers.

CMFPD = 0 : Enable LSZ[2:0], HSZ[2:0] registers, and set for frame inversion.

CMFPD = 1 : Disable LSZ[2:0], HSZ[2:0] registers, and set for line inversion.

## RAM Address Set (Horizontal Address) (R20h)

## RAM Address Set (Vertical Address) (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD[7:0]							
W	1	0	0	0	0	0	0	0	AD[16:8]								

**AD[16:0]** – A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as data is written to the internal GRAM in order to write data consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM='1'), the address AD[16:0] is set in the address counter every frame on the falling edge of VSYNC.

Note 2: In internal clock operation and VSYNC interface operation (RM='0'), the address AD[16:0] is set when executing the instruction.

**Table 47**

AD[16:0]	GRAM Data Setting
17'h00000 – 17'h000EF	Bitmap data on the first line
17'h00100 – 17'h001EF	Bitmap data on the second line
17'h00200 – 17'h002EF	Bitmap data on the third line
:	:
17'h16500 – 17'h13DEF	Bitmap data on the 318 <sup>th</sup> line
17'h16600 – 17'h13EEF	Bitmap data on the 319 <sup>th</sup> line
17'h16700 – 17'h13FEF	Bitmap data on the 320 <sup>th</sup> line

## Write Data to RAM (R22h)

R/W	RS	The bit assignment between RAM write data WD[17:0] and DB[17:0] differs according to the selected interface.
W	1	WD[17:0]

**WD[17:0]** – The LGDP4535 write data to the internal GRAM by expanding into 18 bits internally. The data expansion format into 18 bits differs according to the interface.

The GRAM data represents the grayscale level. The LGDP4535 automatically updates the address according to AM and I/D[1:0] as it writes data in the GRAM. In standby mode, the GRAM is not accessible. The data in 16-bit format is developed into 18 bits according to the register setting (DFM) in 8-/16-bit interface operation.

Note : When writing data in the GRAM via system interface while using the RGB interface, make sure that write operation via two interface do not conflict.

**Table 48 GRAM data and corresponding LCD**

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h00	V63	V0
6'h01	V62	V1
6'h02	V61	V2
6'h03	V60	V3
6'h04	V59	V4
6'h05	V58	V5
6'h06	V57	V6
6'h07	V56	V7
6'h08	V55	V8
6'h09	V54	V9
6'h0A	V53	V10
6'h0B	V52	V11
6'h0C	V51	V12
6'h0D	V50	V13
6'h0E	V49	V14
6'h0F	V48	V15
6'h10	V47	V16
6'h11	V46	V17
6'h12	V45	V18
6'h13	V44	V19
6'h14	V43	V20
6'h15	V42	V21
6'h16	V41	V22
6'h17	V40	V23
6'h18	V39	V24
6'h19	V38	V25
6'h1A	V37	V26
6'h1B	V36	V27
6'h1C	V35	V28
6'h1D	V34	V29
6'h1E	V33	V30
6'h1F	V32	V31

**Grayscale level (REV = 1)**

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h20	V31	V32
6'h21	V30	V33
6'h22	V29	V34
6'h23	V28	V35
6'h24	V27	V36
6'h25	V26	V37
6'h26	V25	V38
6'h27	V24	V39
6'h28	V23	V40
6'h29	V22	V41
6'h2A	V21	V42
6'h2B	V20	V43
6'h2C	V19	V44
6'h2D	V18	V45
6'h2E	V17	V46
6'h2F	V16	V47
6'h30	V15	V48
6'h31	V14	V49
6'h32	V13	V50
6'h33	V12	V51
6'h34	V11	V52
6'h35	V10	V53
6'h36	V9	V54
6'h37	V8	V55
6'h38	V7	V56
6'h39	V6	V57
6'h3A	V5	V58
6'h3B	V4	V59
6'h3C	V3	V60
6'h3D	V2	V61
6'h3E	V1	V62
6'h3F	V0	V63

**Table 49 GRAM data and corresponding LCD**

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h00	V0	V63
6'h01	V1	V62
6'h02	V2	V61
6'h03	V3	V60
6'h04	V4	V59
6'h05	V5	V58
6'h06	V6	V57
6'h07	V7	V56
6'h08	V8	V55
6'h09	V9	V54
6'h0A	V10	V53
6'h0B	V11	V52
6'h0C	V12	V51
6'h0D	V13	V50
6'h0E	V14	V49
6'h0F	V15	V48
6'h10	V16	V47
6'h11	V17	V46
6'h12	V18	V45
6'h13	V19	V44
6'h14	V20	V43
6'h15	V21	V42
6'h16	V22	V41
6'h17	V23	V40
6'h18	V24	V39
6'h19	V25	V38
6'h1A	V26	V37
6'h1B	V27	V36
6'h1C	V28	V35
6'h1D	V29	V34
6'h1E	V30	V33
6'h1F	V31	V32

**Grayscale level (REV = 0)**

GRAM data RGB	Grayscale level	
	Netative	Positive
6'h20	V32	V31
6'h21	V33	V30
6'h22	V34	V29
6'h23	V35	V28
6'h24	V36	V27
6'h25	V37	V26
6'h26	V38	V25
6'h27	V39	V24
6'h28	V40	V23
6'h29	V41	V22
6'h2A	V42	V21
6'h2B	V43	V20
6'h2C	V44	V19
6'h2D	V45	V18
6'h2E	V46	V17
6'h2F	V47	V16
6'h30	V48	V15
6'h31	V49	V14
6'h32	V50	V13
6'h33	V51	V12
6'h34	V52	V11
6'h35	V53	V10
6'h36	V54	V9
6'h37	V55	V8
6'h38	V56	V7
6'h39	V57	V6
6'h3A	V58	V5
6'h3B	V59	V4
6'h3C	V60	V3
6'h3D	V61	V2
6'h3E	V62	V1
6'h3F	V63	V0

Read Data from RAM (R22h)

R/W	RS	The bit assignment between RAM write data RD[17:0] and DB[17:0] differs according to the selected interface.
R	1	RD[17:0]

**RD[17:0]** – 18-bit data read from the GRAM. The bit assignment between RD[17:0] and DB[17:0] (data on the data bus) differs according to the selected interface.

When the LGDP4535 read data from the GRAM to the microcomputer, the first word read immediately after RAM address set is taken in the intenal read-data latch and inbalid data is sent to the data bus DB[17:0]. Vaild data is sent to the data bus as the LGDP4535 reads out the second and subsequence words.

When either 8-bit or 16-bit interface is selected, the LSB of R and B dot data are not read out.

Note : This register is not available in RGB interface operation.

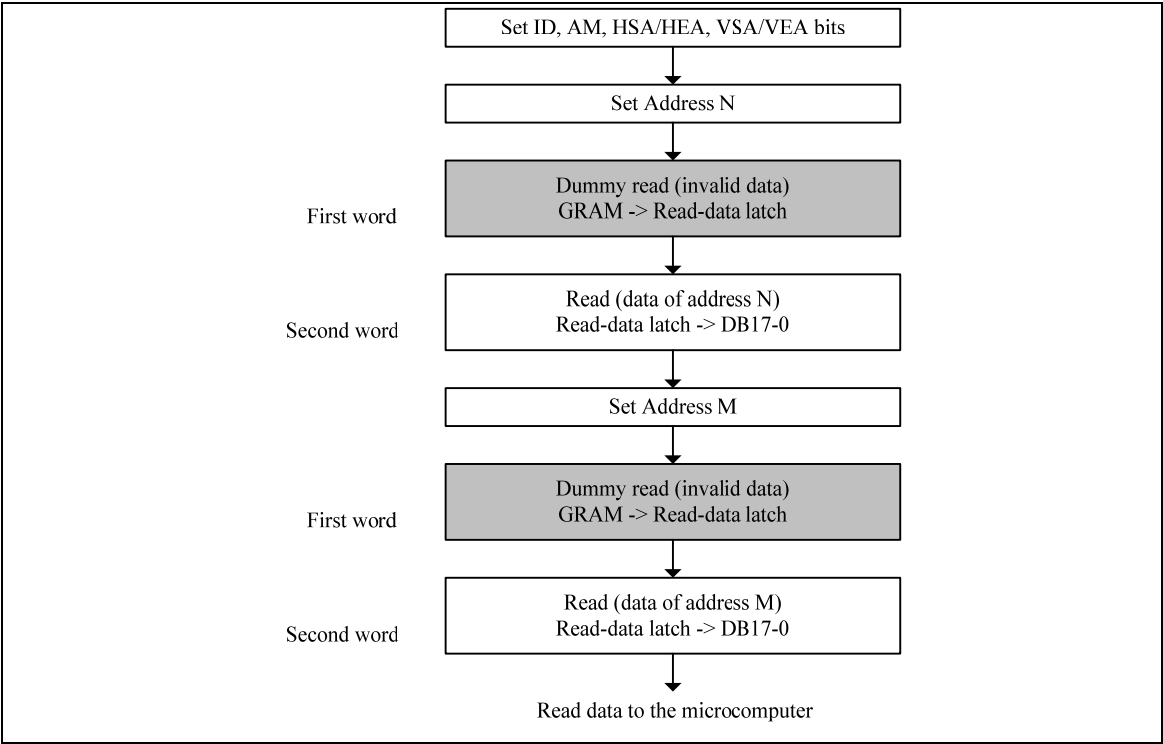


Figure 12



### Gamma Control 1-16 (R30h to R3Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]				0	0	0	VRP0[4:0]					
W	1	0	0	0	VRN1[4:0]				0	0	0	VRN0[4:0]					
W	1						PFP1[2:0]								PFP0[2:0]		
W	1						PFP3[2:0]								PFP2[2:0]		
W	1						PFN1[2:0]								PFN0[2:0]		
W	1						PFN3[2:0]								PFN2[2:0]		
W	1														PMP[2:0]		
W	1														PMN[2:0]		

**PKP5-0[2 :0]** –  $\gamma$  fine-adjustment register for positive polarity

**PRP1-0[2 :0]** –  $\gamma$  gradient-adjustment register for positive polarity

**VRP0[3:0], VRP1[4 :0]** –  $\gamma$  amplitude-adjustment register for positive polarity

**PKN5-0[2 :0]** –  $\gamma$  fine-adjustment register for negative polarity

**PRN1-0[2 :0]** –  $\gamma$  gradient-adjustment register for negative polarity

**VRN0[3:0], VRN1[4 :0]** –  $\gamma$  amplitude-adjustment register for negative polarity

**PFP3-0[2:0]** –  $\gamma$  fine adjustment register bits for positive polarity

**PFN3-0[2:0]** –  $\gamma$  fine adjustment register bits for negative polarity

**PMP[2:0]** –  $\gamma$  fine adjustment register bits for positive polarity

**PMN[2:0]** –  $\gamma$  fine adjustment register bits for negative polarity

For details, see “ $\gamma$ -Correction Function” section

## EPROM Control Register 1 (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	PTM[1:0]	POR	VPP	PPROG	PWE	PA[1:0]	PDIN[7:0]									

EPROM programming control. See “EPROM Control” section.

**PDIN[7:0]** – Data input. This corresponds to VCM[6:0] bits of R13h.

**PA[1:0]** – address input. This selects one of four banks of the EPROM.

**Table 50**

PA[1:0]	Write Data Input	Write OPT Cell
2'h0	PDIN[6:0]	Cell[6:0]
2'h1	PDIN[6:0]	Cell[14:8]
2'h2	PDIN[6:0]	Cell[22:16]
2'h3	PDIN[6:0]	Cell[30:24]

**PWE** – Write enable.

**PPROG** – Program mode enable.

**VPP** – Power switch control for the VPP pin of the embedded EPROM. When VPP = “1”, the internal VPP is set to 7.2V; otherwise it is set to 1.8V.

**POR** – Pin for power-on rest.

**PTM[1:0]** – Pins for enabling test mode

## EPROM Control Register 2 (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0										AUTOWR	RA[1:0]	VCMSSEL[1:0]		

EPROM programming control. See “EPROM Control” section.

**VCMSSEL[1:0]** – With VCMSEL pin, sets VcomH level from either the register R13h or the EPROM

**Table 51**

VCMSSEL[1:0]	VcomH Level adjustment
00	VCM[6:0] of the register R13h
01	EPROM data at first if EPROM has data. Otherwise, VCM[6:0] of the register R13h
1x	EPROM data selected by RA[1:0]

**RA[1:0]** – Read address input. This selects one of four banks of the EPROM.

**AUTOWR** – Select the methoe of write operation  
 If AUTOWR=’1’, write address is PA.  
 Else AUTOWR=’0’, write address is auto select address.

### EPROM Control Register 3 (R42h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0														PDOUT[7:0]

PDOUT[7:0] – EPROM Read Data output.

### Window Horizontal RAM Address Start/End (R50h/R51h)

### Window Vertical RAM Address Start/End (R52h/R53h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0								HSA[7:0]
W	1	0	0	0	0	0	0	0	0								HEA[7:0]
W	1	0	0	0	0	0	0	0									VSA[8:0]
W	1	0	0	0	0	0	0	0									VEA[8:0]

**HSA[7:0]/HEA[7:0]** – HSA[7:0] and HEA[7:0] represent the addresses at the start and end of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the range on the GRAM to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that  $8'h00 \leq HSA < HEA \leq 8'hEF$ .

**VSA[8:0]/VEA[8:0]** – VSA[8:0] and VEA[8:0] represent the addresses at the start and end of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the range on the GRAM to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that  $9'h000 \leq VSA < VEA \leq 9'h1AF$ .

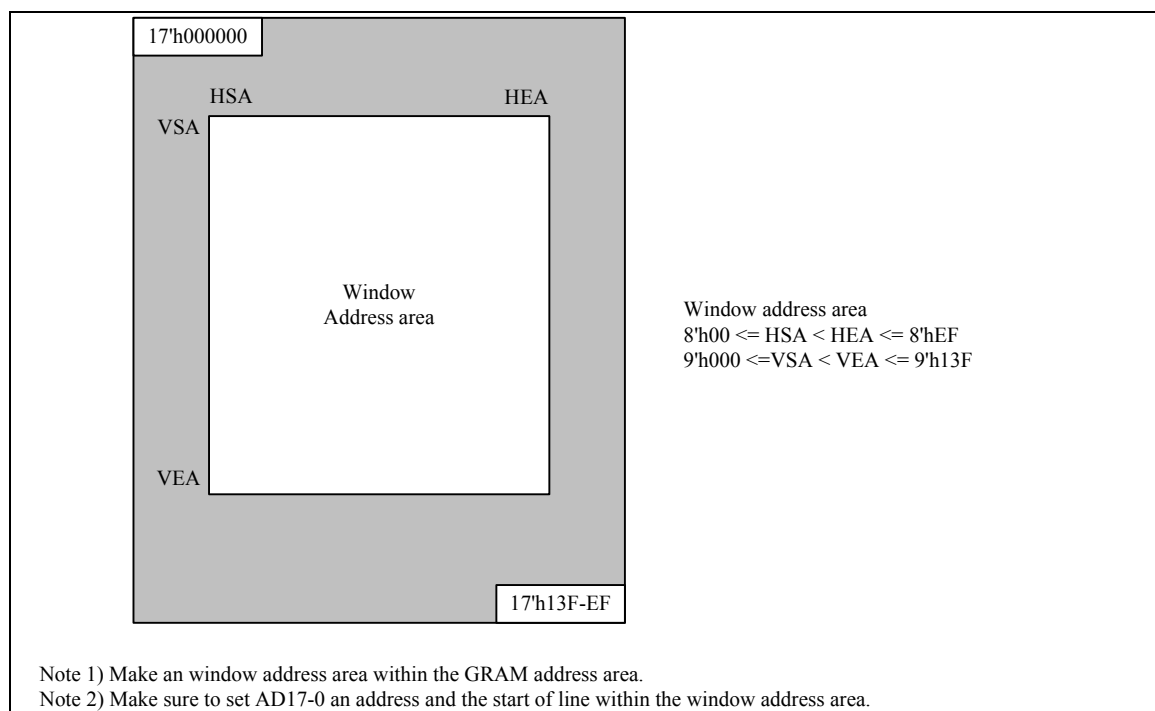


Figure 13

**Driver Output Control (R60h)****Base Image Display Control (R61h)****Vertical Scroll Control (R6Ah)**

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	GS	0	NL[5:0]						0	0	SCN[5:0]					
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
W	1	0	0	0	0	0	0	0	VL[8:0]								

**SCN[5:0]** – Specifies the gate line where the gate driver starts scan.

**NL[5:0]** – Sets the number of lines to drive the LCD at an interval of 8lines. The GRAM address mapping is not affected by the number of lines set with NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

**Table 52**

NL[5:0]	Number of Lines	NL[5:0]	Number of Lines
6'h00	8	6'h15	176
6'h01	16	6'h16	184
6'h02	24	6'h17	192
6'h03	32	6'h18	200
6'h04	40	6'h19	208
6'h05	48	6'h1A	216
6'h06	56	6'h1B	224
6'h07	64	6'h1C	232
6'h08	72	6'h1D	240
6'h09	80	6'h1E	248
6'h0A	88	6'h1F	256
6'h0B	96	6'h20	264
6'h0C	104	6'h21	272
6'h0D	112	6'h22	280
6'h0E	120	6'h23	288
6'h0F	128	6'h24	296
6'h10	136	6'h25	304
6'h11	144	6'h26	312
6'h12	152	6'h27	320
6'h13	160	6'h28 – 6'h3F	Setting disabled
6'h14	168		

**GS** – Set the direction of scan by the gate driver. Set the GS bit in combination with SM and SS bits to optimize scan method to the LCD module.

**REV** – The grayscale level corresponding to the GRAM data can be reversed by setting REV = 1. This enables the LGDP4535 to display the same image form a same set of data whether the liquid crystal panel

is normally black or white. The source output level during front, back porch periods and blank periods is determined by resiger setting (PTS).

**Table 53**

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

**VLE** – Vertical scroll display enable bit. When  $VLE = 1$ , the LGDP4535 starts displaying the base image from the line (of the physical display) determined by setting the VL[8:0] bits. VL[8:0] represents the number of lines shifted from the first line of the physical display ( the amount of scrolling). Note that the display position of partial image is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set  $VLE = 0$ .

**NDL** – Sets the source output level in non-display lit driving periods. By setting the NDL bit, the non-display area can be kept lit on.

**Table 54**

NDL	Non-display area	
	Positive	Negative
0	V63	V0
1	V0	V63

**VL[8:0]** – Sets the amount of scrolling the base image by the number of lines. The RAM data in the start line address is displayed on the line, which is shifted from the first line of the liquid crystal panel by the number of lines set with VL[8:0]. In setting VL[8:0], make sure  $VL \leq 320$ .

**Table 55**

SCN[5:0]	Gate line No (Scan start position)			
	SM = 0		SM = 1	
	GS = 0	GS = 1	GS = 0	GS = 1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28 – 6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

## Software Reset (R70h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST

**SRST** – When SRST = 1, software is reset.

When SRST = 0, software reset is canceled.

## I/F Endian Control (R71h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCREV[1:0]	

**TCREV[1:0]** – Controls the endian setting (big/little endian: the order of receiving data) when transferring one-pixel data via i80 interface in multiple times. When setting a new value to TCREV[1:0], the order is changed from when the next instruction is executed.

**Table 56**

TCREV[1:0]	2 Transfers / Pixel	3 Transfers / Pixel
2'h0	Upper to lower(1 <sup>st</sup> to 2 <sup>nd</sup> )	Upper to lower(1 <sup>st</sup> , 2 <sup>nd</sup> , 3 <sup>rd</sup> )
2'h1	Setting disabled	Setting disabled
2'h2	Setting disabled	Setting disabled
2'h3	Lower to upper(2 <sup>nd</sup> to 1 <sup>st</sup> )	Lower to upper(3 <sup>rd</sup> , 2 <sup>nd</sup> , 1 <sup>st</sup> )

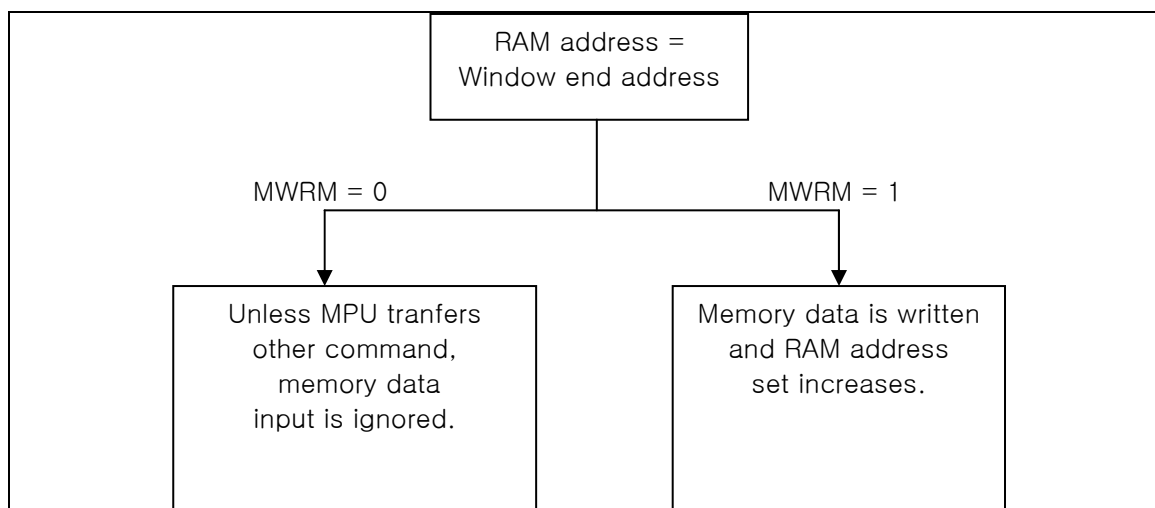
- Notes :
1. In read operation, the data is transferred from upper bits to lower bits (big endian) regardless of TCREV[1:0] setting.
  2. Make sure to set TCREV[1:0] when executing reset or exiting from shutdown mode.

## Memory Write Control (R72h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MWRM

**MWRM** – Set Memory Write Mode.

RAM horizontal address = end address, RAM vertical address = end address



## ***Partial Image 1: Display Position (R80h)***

### ***RAM Address (Start/End Line Address) (R81h/R82h)***

## ***Partial Image 2: Display Position (R83h)***

### ***RAM Address (Start/End Line Address) (R84h/R85h)***

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	PTDP0[8:0]								
W	1	0	0	0	0	0	0	0	PTSA0[8:0]								
W	1	0	0	0	0	0	0	0	PTEA0[8:0]								
W	1	0	0	0	0	0	0	0	PTDP1[8:0]								
W	1	0	0	0	0	0	0	0	PTSA1[8:0]								
W	1	0	0	0	0	0	0	0	PTEA1[8:0]								

**PTDP0[8:0]** – Sets the display position of partial image 1.

**PTDP1[8:0]** – Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting make sure that

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display position : (PTDP0, PTEA0)

Coordinates of partial image 2 display position : (PTDP1, PTEA1)

If PTDP0 = 9'h000, the partial image 1 is displayed from the first line of the base image.

**PTSA0[8:0]** – Sets the start line addresses of the RAM area, respectively for the partial image 1

**PTEA0[8:0]** – Sets the end display position of partial image 1.

**PTSA1[8:0]** – Sets the start line addresses of the RAM area, respectively for the partial image 2.

**PTEA1[8:0]** – Sets the end display position of partial image 2.

## ***Panel Interface Control 1 (R90h)***

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI[1:0]		RTNI[7:0]							

**RTNI[7:0]** – Sets 1H (line) period. This setting is enabled while the LGDP4535's display operation is synchronized with internal clock. RTNI[7:0] should be greater than or equal to 60 (= 3Ch).



**DIVI[1:0]** – Sets the division ratio of the internal clock frequency. The LGDP4535's internal operation is synchronized with the frequency divided internal clock. When changing the DIVI[1:0] bits, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see “Frame-Frequency Adjustment Function”. The setting in DIVI[1:0] is disabled in RGB interface operation.

### Frame Frequency Calculation

$$\text{Frame frequency} = \text{fosc} / (\text{clock cycles per line} \times \text{division ratio} \times (\text{active line} + \text{BP} + \text{FP}))$$

**Table 57 clocks per line (internal clock operation 1 clock = 1 OSC)**

RTNI[7:0]	Clock per Line
8'h00 – 8'h3B	Setting disabled
8'h3C	60 clocks
8'h3E	62 clocks
8'h40	64 clocks
8'h42	66 clocks
.....	
8'hFC	252 clocks
8'hFE	254 clocks

**Table 58 Division ratio of the internal clock**

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

## Panel Interface Control 2 (R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOWI[2:0]	0	0	0	0	0	0	EQI2[1:0]	EQI1[1:0]		

**EQI1[1:0]** – Sets equalization period.

*Note : when VCOML >= 0V, EQI1, EQI2 setting is disabled.*

**Table 59**

EQI1[1:0]	Equalization period
2'h0	0 (internal clock period <sup>see note</sup> )
2'h1	2
2'h2	4
2'h3	6

**EQI2[1:0]** – Sets equalization period.

**Table 60**

<b>EQI2[1:0]</b>	<b>Equalization period</b>
2'h0	0 (internal clock period <sup>see note</sup> )
2'h1	2
2'h2	4
2'h3	6

**NOWI[2:0]** – Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation in synchronization with internal clock.

**Table 61**

<b>NOWI[2:0]</b>	<b>Non-overlap period</b>
3'h0	0 (internal clock period <sup>see note</sup> )
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note : The internal clock is the frequency divided clock with the division ratio set with the DIVI[1:0] bits.

### **Panel Interface Control 3 (R93h)**

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SEI[2:0]	0	0	0	0	0	0	0	0	0	0

**MCPI[2:0]** – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation in synchronization with internal clock.

**Table 62**

<b>MCPI[2:0]</b>	<b>Source output position</b>
3'h0	0 (internal clock period <sup>see note</sup> )
3'h1	4
3'h2	8
3'h3	12
3'h4	16
3'h5	20
3'h6	24
3'h7	28

Note: The internal clock is the frequency divided clock with the division ratio set with the DIVI[[1:0] bits. The source output position is measured from a reference point by the number of internal clock cycle.

**SEI[2:0]** – Sets Source equalization period.

**Table 63**

SEQI[2:0]	Source equalization period
3'h0	0 (internal clock period <sup>see note</sup> )
3'h1	2
3'h2	4
3'h3	6
3'h4	8
3'h5	10
3'h6	12
3'h7	14

## Panel Interface Control 4 (R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE[1:0]	RTNE[7:0]								

**RTNE[7:0]** – Sets the number of internal clocks per 1H (line) period. Set the value that represents the number of DOTCLKs divided by the division ratio, which is input in a 1H period. RTNE[7:0] should be greater than or equal to 60 (= 3Ch).

**DIVE[1:0]** – Sets DIVE, the internal division ratio of DOTCLK. The internal operation is performed according to the clocks divided by the internal division ratio DIVE.

**Table 64 Division ratio of DOTCLK**

DIVE[1:0]	Division Ratio	Internal operation clock unit (DOTCLK)			
		18-bit, 1 transfer RGB interface DOTCLK = 5 MHz		8-bit, 3 transfer RGB interface DOTCLK = 15 MHz	
2'h0	Setting disabled	Setting disabled	-	Setting disabled	-
2'h1	1/1	1 DOTCLKs	0.2 $\mu$ s	3 DOTCLKs	0.2 $\mu$ s
2'h2	1/2	2 DOTCLKs	0.4 $\mu$ s	6 DOTCLKs	0.4 $\mu$ s
2'h3	1/4	4 DOTCLKs	0.8 $\mu$ s	12 DOTCLKs	0.8 $\mu$ s

**Table 65 DOTCLK per line (1H period)**

RTNE[7:0]	DOTCLK per line (1H)
8'h00 – 8'h3B	Setting disabled
8'h3C	60 clocks
8'h3E	62 clocks
8'h40	64 clocks
8'h42	66 clocks
.....	
8'hFC	252 clocks
8'hFE	254 clocks

## Panel Interface Control 5 (R97h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	NOWE[3:0]				0	0	0	0	EQE2[1:0]		EQE1[1:0]	

**EQE1[1:0]** – Sets equalization period.

*Note : when VCOML >= 0V, EQE1, EQE2 setting is disabled.*

**Table 66**

EQE1[1:0]	Equalization period
2'h0	0 (internal clock period <sup>see note</sup> )
2'h1	2
2'h2	4
2'h3	6

**EQE2[1:0]** – Sets equalization period.

**Table 67**

EQE2[1:0]	Equalization period
2'h0	0 (internal clock period <sup>see note</sup> )
2'h1	2
2'h2	4
2'h3	6

**NOWE[3:0]** – Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

**Table 68**

NOWE[3:0]	Non-overlap period	NOWE[3:0]	Non-overlap period
4'h0	0 (internal clock period <sup>see note</sup> )	4'h8	32
4'h1	4	4'h9	36
4'h2	8	4'hA	40
4'h3	12	4'hB	44
4'h4	16	4'hC	48
4'h5	20	4'hD	52
4'h6	24	4'hE	56
4'h7	28	4'hF	60

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

## Panel Interface Control 6 (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	MCPE[2:0]		

**MCPE[2:0]** – Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation via RGB interface.

**Table 69**

MCPE[2:0]	Source output position	MCPE[2:0]	Source output position
5'h00	0 (internal clock period <sup>see note</sup> )	5'h10	16
5'h01	4	5'h11	20
5'h02	8	5'h12	24
5'h03	12	5'h13	28

Note : 1 clock = (Number of data transfers / pixel) x DIVE (division ratio) [DOTCLK].

**SEQE[2:0]** – Sets Source equalization period.

**Table 70**

SEQE[2:0]	Source equalization period	SEQE[2:0]	Source equalization period
5'h00	0 (internal clock period <sup>see note</sup> )	5'h10	8
5'h01	2	5'h11	10
5'h02	4	5'h12	12
5'h03	6	5'h13	14

## Frame Rate Control (R9Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	OHZ	0	0	0	FRS[4:0]				

**FRS[4:0]** – Set the frame rate when the internal resistor is used for oscillator circuit.

Sets the source output timing by the number of internal clock from a reference point. The setting is enabled in display operation via RGB interface.

**Table 71**

FRS[4:0]	Vcom amplitude	FRS[4:0]	Vcom amplitude
5'h00	x 0.13	5'h10	x 1.69
5'h01	x 0.26	5'h11	x 1.80
5'h02	x 0.31	5'h12	x 1.83
5'h03	x 0.43	5'h13	x 1.94
5'h04	x 0.47	5'h14	x 1.97
5'h05	x 0.60	5'h15	x 2.08
5'h06	x 0.64	5'h16	x 2.10
5'h07	x 0.76	5'h17	x 2.20
5'h08	x 0.84	5'h18	x 2.28
5'h09	x 0.96	5'h19	x 2.37
5'h0A	x 1.00 ( default )	5'h1A	x 2.42
5'h0B	x 1.11	5'h1B	x 2.50
5'h0C	x 1.15	5'h1C	x 2.54
5'h0D	x 1.27	5'h1D	x 2.64
5'h0E	x 1.30	5'h1E	x 2.66
5'h0F	x 1.41	5'h1F	x 2.75

Note : When the default OSC frequency( FRS[4:0]=5'h0A ) is 2MHz and the register setting is FRS[4:0]=5'h11 , then OSC frequency = 2MHz x 1.80 = 3.6 MHz

**OHZ** – Set the test mode

OHZ = 0 – FMARK pin is normal output..

OHZ = 1 – FMARK pin is clock input for test.

## Test Register 1 (RA0h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	TDLY[1:0]	0	0	0	TDFN	0	0	TFOSC	TOSC	0	0	TVCOM[1:0]		

**TVCOM[1:0]** – Sets the Vcom output level for test.

**Table 72**

TVCOM [1:0]	Vcom Level
2'h0	modulation
2'h1	modulation
2'h2	VCOML
2'h3	VCOMH

**TOSC** – Sets for the oscillator test.

**TFOSC** – Sets for the oscillator delay test.

**TDFN** – Sets for the function test.

**TMEM** – Sets for the memory test.

**TDLY[1:0]** – Sets for the delay time test.

## Test Register 2 (RA1h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	REGULPD	0	0	0	TSAP	0	0	TSHZ	TPATE	0	TPAT[2:0]		

**TSHZ** – Sets

**TSAP** – Sets

**REGULPD** – Sets

**TPATE** – Sets

**TPAT[2:0]** – Sets

## Test Register 3 (RA2h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	T8CL	0	0	0		0	0	0	TVON	0	HaltVreg	MultiVci	

**MultiVci** – Used for Device Test.

**HaltVreg** – Used for Device Test.

**TVON** – Used for Device Test.

**T8CL** – Used for 8 color mode test

### Test Register 4 (RA3h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	RDSM[1:0]	0	0	0	WRPW[1:0]	

**WRPW[1:0]** – Used for memory write pulse width test.

**RDSM[1:0]** – Used for memory read sensing margin test.

### Test Register 5 (RA4h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	S_HIZ	0	0	0	SBC

**SBC** – Source Bias controlUsed for memory write pulse width test.

**S\_HIZ** – stepup2 .

### Test Register 6 (RA5h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OV

**OV** – Set data overwrite enable.

OV = 1 : data overwrite disable

OV = 0 : data overwrite enable.

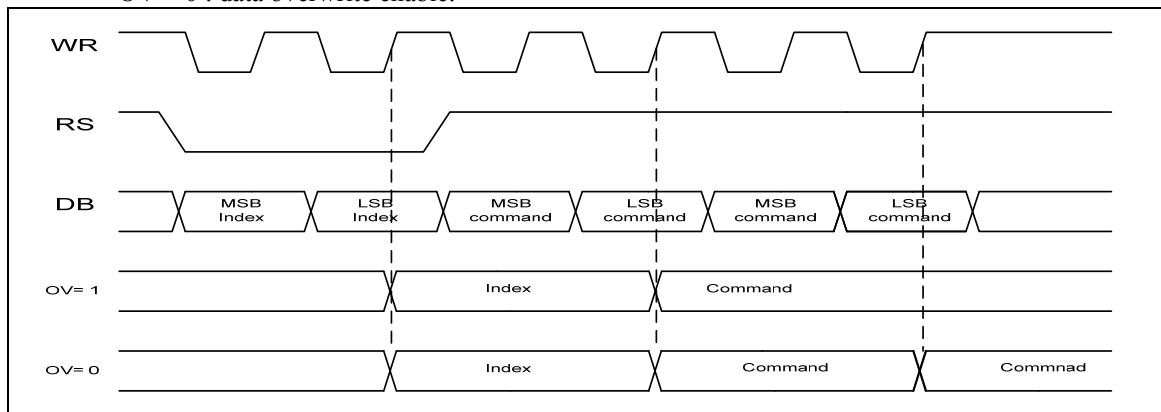


Figure 14

# Instruction List

Index	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	Start oscillation																1
01h	Driver output control 1						SM (0)		SS (0)								
02h	LCD Driving Wave Control							BC0 (0)	EOR (0)			NW[5:0] (000000)					
03h	Entry mode	TRI (0)	DFM (0)		BGR (0)					ORG (0)		ID[1:0] (11)	AM (0)			EPF[1:0] (00)	
04h	Resizing Control							RCV[1:0] (00)				RCH[1:0] (00)				RSZ[1:0] (00)	
07h	Display Control 1			PTDE[1:0] (00)				BASEE (0)				GON (0)	DTE (0)	COL (0)		D[1:0] (00)	
08h	Display Control 2	FP[3:0] (00001000)								BP[7:0] (00001000)							
09h	Display Control 3							PTS[2:0] (000)				PTG[1:0] (00)		ISC[3:0] (0000)			
0Ah	Display Control 4												FMARKOE (0)		FMI[2:0] (000)		
0Ch	External display Interface Control 1			ENC[1:0] (000)				RM (0)				DM[1:0] (00)				RIM[1:0] (00)	
0Dh	Frame Marker Position							FMP[9:0] (0000000000)									
0Fh	External display Interface Control 2											VSPL (0)	HSPL (0)			EPL (0)	DPL (0)
10h	Power Control 1			SAP[2:0] (000)				BT[2:0 ] (0000)				AP[2:0] (000)		DK (1)	DSTB (0)	SLP (0)	STB (0)
11h	Power Control 2							DCI[2:0] (110)				DCO[2:0] (110)				VC[2:0] (000)	
12h	Power Control 3												PON (0)		VRH[3:0] (0000)		
13h	Power Control 4			VCOMG (0)			VDV[4:0] (00000)					VCM[6:0] (00000000)					
15h	Regulator Control			RSET[2:0] (010)				RI[2:0] (000)				RV[2:0] (011)				RCONT (000)	
16h	Gamma Select Control												EN_MA (0)				PS (0)
17h	Vcom Control							LSZ[2:0] (000)				HSZ[2:0] (000)					CMFPD (1)
20h	RAM Address Set (Horizontal Address)											AD[7:0] (00000000)					
21h	RAM Address Set (Vertical Address)											AD[16:8] (000000000)					
22h	RAM Data	WD[17:0] or RD[17:0]															
30h	Gamma Control 1							PKP1[2:0] (000)								PKP0[2:0] (000)	
31h	Gamma Control 2							PKP3[2:0] (000)								PKP2[2:0] (000)	
32h	Gamma Control 3							PKP5[2:0] (000)								PKP4[2:0] (000)	
33h	Gamma Control 4							PRP1[2:0] (000)								PRP0[2:0] (000)	
34h	Gamma Control 5							PKN1[2:0] (000)								PKN0[2:0] (000)	
35h	Gamma Control 6							PKN3[2:0] (000)								PKN2[2:0] (000)	
36h	Gamma Control 7							PKN5[2:0] (000)								PKN4[2:0] (000)	
37h	Gamma Control 8							PRN1[2:0] (000)								PRN0[2:0] (000)	
38h	Gamma Control 9						VRP1[4:0] (00000)							VRP0[4:0] (00000)			
39h	Gamma Control 10						VRN1[4:0] (00000)							VRN0[4:0] (00000)			
3Ah	Gamma Control 11						PFP1[2:0] (001)									PFP0[2:0] (001)	
3Bh	Gamma Control 12						PFP3[2:0] (001)									PFP2[2:0] (001)	
3Ch	Gamma Control 13						PFN1[2:0] (001)									PFN0[2:0] (001)	
3Dh	Gamma Control 14						PFN3[2:0] (001)									PFN2[2:0] (001)	
3Eh	Gamma Control 15															PMP[2:0] (001)	



3Fh	Gamma Control 16															PMN[2:0] (001)
40h	EPROM Control 1	PTM[1:0] (00)		POR (0)	VPP (0)	PPROG (0)	PWE (0)	PA[1:0] (00)		PDIN[7:0] (00000000)						
41h	EPROM Control 2												AUTOWR (0)	RA[1:0] (00)		VCMSEL[1:0] (00)
42h	EPROM Control 3									PDOUT[7:0] (11111111)						
50h	Window Horizontal RAM Start Address									HSA[7:0] (00000000)						
51h	Window Horizontal RAM End Address									HEA[7:0] (11101111)						
52h	Window Vertical RAM Start Address								VSA[8:0] (00000000)							
53h	Window Vertical RAM End Address								VEA[8:0] (11010111)							
60h	Driver Output Control 2	GS (0)	NL[5:0] (000000)								SCN[5:0] (000000)					
61h	Base Image Display Control													NDL (0)	VLE (0)	REV (0)
6Ah	Vertical Scroll Control		VL[8:0] (000000000)													
70h	Software Reset															SRST (0)
71h	I/F Endian Control															TCREV[1:0] (00)
72h	Memory Write Control															MWRM (0)
80h	Partial Image 1 Display Position								PTDP0[8:0] (000000000)							
81h	Partial Image 1 RAM Start Line Address								PTSA0[8:0] (000000000)							
82h	Partial Image 1 RAM End Line Address								PTEA0[8:0] (000000000)							
83h	Partial Image 2 Display Position								PTDP1[8:0] (000000000)							
84h	Partial Image 2 RAM Start Line Address								PTSA1[8:0] (000000000)							
85h	Partial Image 2 RAM End Line Address								PTEA1[8:0] (000000000)							
90h	Panel Interface Control 1						DIVI[1:0] (00)		RTNI[7:0] (01011010)							
92h	Panel Interface Control 2					NOWI[2:0] (000)							EQI2[1:0] (00)		EQI1[1:0] (00)	
93h	Panel Interface Control 3					SEQI[2:0] (000)							MCP1[2:0] (000)			
95h	Panel Interface Control 4						DIVE[1:0] (00)		RTNE[7:0] (01011010)							
97h	Panel Interface Control 5					NOWE[3:0] (0000)							EQE2[1:0] (00)		EQE1[1:0] (00)	
98h	Panel Interface Control 6					SEQE[2:0] (000)							MCPE[2:0] (000)			
9Ah	Frame Rate and Color Control							OHZ (0)				FRS[4:0] (01000)				
A0h	Test register 1			TDLY (00)				TDFN (0)			TFOSC (0)	TOSC (0)			TVCOM[1:0] (00)	
A1h	Test register 2			REGULP D (0)				TSAP (0)			TSHZ (0)	TPATE (0)		TPAT[2:0] (000)		
A2h	Test register 3			T8CL (0)								TVON (0)		HaltVreg (0)	MultiVci (1)	
A3h	Test register 4										RDSM (00)				WRPW (00)	
A4h	Test register 5											S_HIZ (0)				SBC (0)
A5h	Test register 6															OV (0)

## Reset Function

The LGDP4535 is initialized with a RESET input. During a reset period, the LGDP4535 is in a busy state and neither instruction nor access to the GRAM data from the MPU is accepted. The LGDP4535's internal power supply circuit unit is initialized also with a RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 1 ms). During this period, neither access to the internal GRAM nor initial setting of instruction bits is accepted.

### 1. Initial state of instruction bits (default)

See the instruction list. The default value is shown in the parenthesis of each instruction bit cell.

### 2. RAM Data initialization

The RAM data is not automatically initialized with a RESET input and must be initialized by software in a display-off period (D1-0 = "00").

### 3. Output pin initial state \*See note

1. LCD driver S1~S720	: GND
G1~G320	: VGL (= GND)
2. Vcom	: GND
3. VcomR	: Hi-Z
4. VcomH	: Hi-Z
5. VcomL	: GND
6. VREG1OUT	: Hi-Z
7. VciOUT	: Vci
8. VLOUT1	: Vci
9. VLOUT2	: DDVDH (= Vci)
10. VLOUT3	: GND
11. VLOUT4	: GND
12. VDD	: VDD
13. FMARK	: GND
14. SDO	: GND
15. Oscillator	: Oscillate

### 4. Initial state of input/output pins \*See note

1. C11+	: Vci1
2. C11-	: GND
3. C12+	: Vci1
4. C12-	: GND
5. C13+	: Vci1
6. C13-	: GND
7. C21+	: DDVDH (= Vci)
8. C21-	: GND
9. C22+	: DDVDH (= Vci)
10. C22-	: GND

Note: The above-mentioned initial states of output and input pins are the ones when the LGDP4535's power supply circuit is connected as exemplified in "Wiring example".

**5. Note on Reset function**

- (1) When a RESET input is entered into the LGDP4535 while it is in deep standby mode, the LGDP4535 starts up the inside logic regulator and makes a transition to the initial state. During this period, the interface pins may be under an unstable condition. For this reason, do not enter a RESET input in deep standby mode.
- (2) When transferring instruction using either two or three transfer mode via 8-/9-/16-bit interface, make sure to execute a data transfer synchronization after executing a reset operation.

## Basic Mode operation of the LGDP4535

The basic operation modes of the LGDP4535 are shown in the following diagram. When making a transition from one mode to another, refer to instruction setting sequence.

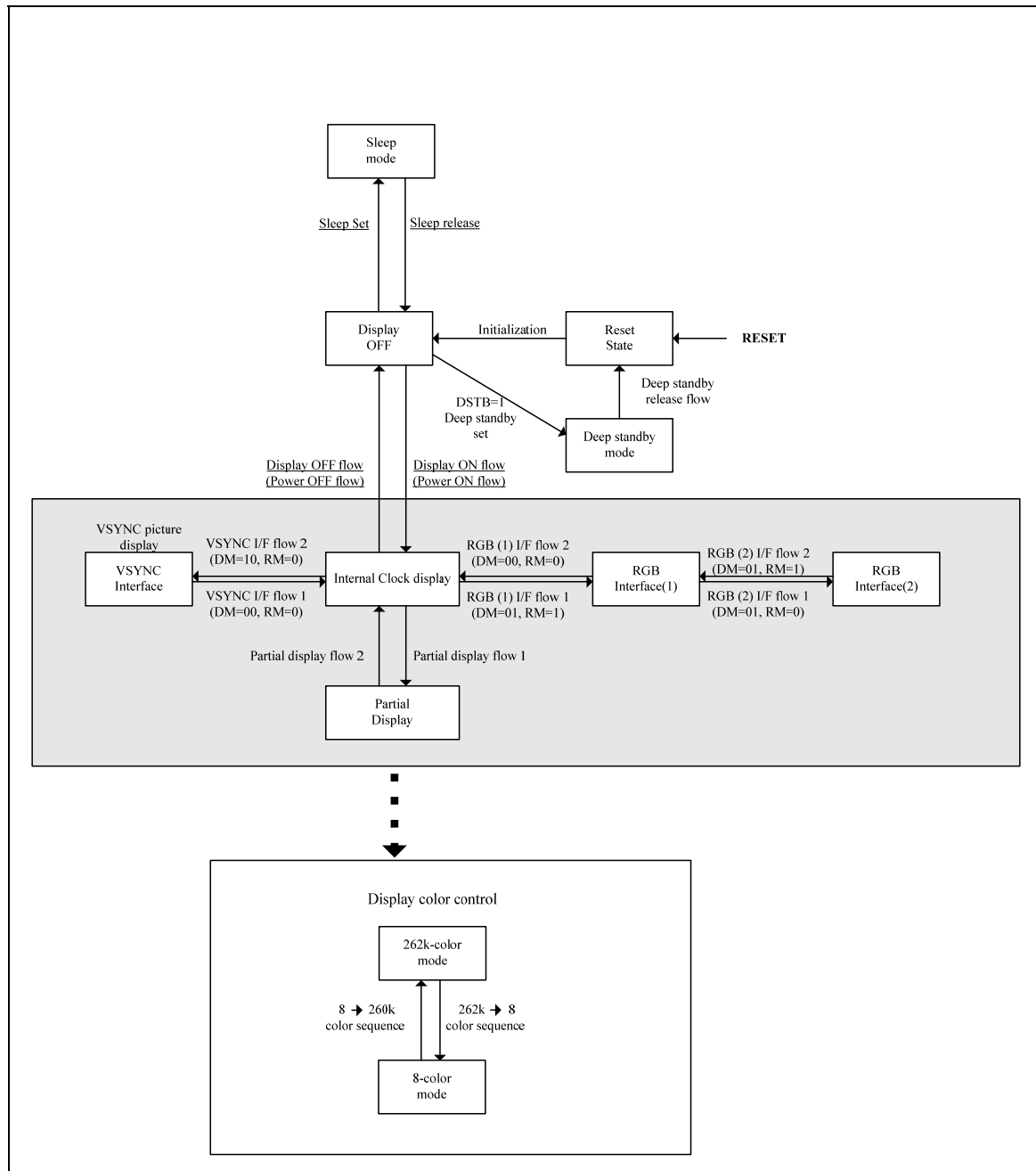


Figure 15

## Interface and data format

The LGDP4535 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The LGDP4535 allows selecting an optimum interface according to the kind of display (moving or still picture) in order to transfer data efficiently.

As external display interface, the LGDP4535 supports RGB interface and VSYNC interface, both enabling data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the LGDP4535 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the LGDP4535's GRAM in order to minimize the data transfer by transferring data only when it is necessary to switch the moving picture frames. The window address function specifies the RAM area where data is rewritten for moving picture display and enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

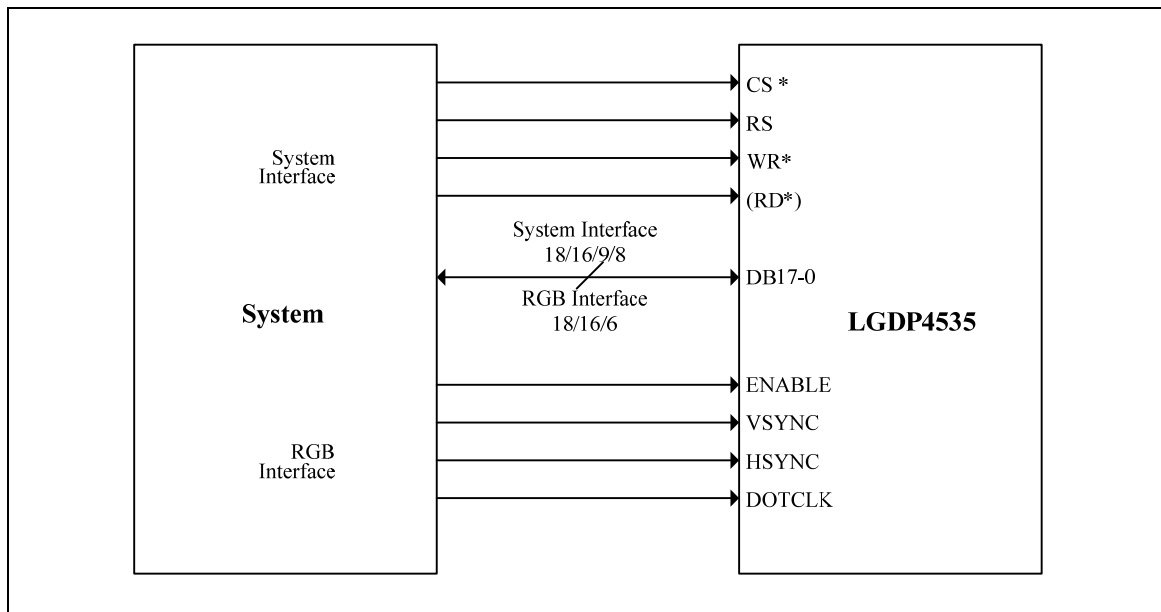
In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display using system interface by writing data to the GRAM at more than a certain speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in speed and methods of writing data to the internal RAM.

The LGDP4535 can operate in either one of the following four modes according to the state of display. The display operation mode is determined by setting the external interface control register. When switching between different modes, make sure to refer to mode switching sequence.

**Table 73**

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM[1:0] = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM[1:0] = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM[1:0] = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM[1:0] = 10)

- Notes:
1. Instructions are set only via system interface.
  2. The RGB and VSYNC interfaces cannot be used simultaneously.
  3. Do not make changes to the RGB interface operation setting (RIM[1:0]) while RGB interface is in operation.
  4. See the "External Display Interface" section for the mode transition sequence.



**Figure 16 LGDP4535's Interface**

#### Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. Any input via external display interface is invalid in this operation. The internal RAM is accessible only via system interface.

#### RGB interface operation (1)

The display operation is synchronized with the frame synchronous signal (VSYNC), the line synchronous signal (HSYNC), and the dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied throughout the display period using RGB interface.

The LGDP4535 transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function enables the LGDP4535 to display a moving picture and the data in other than the moving picture RAM area simultaneously and transferring only data to be overwritten in the moving picture RAM area when rewriting the moving picture RAM area. This structure can minimize the total number of data transfer. The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the LGDP4535 by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with these settings.

#### RGB interface operation (2)

This mode enables the LGDP4535 to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first and then set a new address and the index register to R22h.

#### VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the LGDP4535 to display a moving picture using system interface by writing data to the internal RAM at more than a minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are constraints in speed and methods of writing RAM data. For details, see the "VSYNC Interface" section. As an external input, only VSYNC signal input is valid in this mode. Any other input via external display interface is invalid.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) according to the register settings inside the LGDP4535.

## System Interface

The following are the kinds of system interfaces available with the LGDP4535. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

**Table 74**

IM[3:0]	Interface Mode with MPU	DB pins	Colors
0000	Setting disabled	-	-
0001	Setting disabled	-	-
0010	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note 1
0011	80-system 8-bit interface	DB17-10	262,144 *see Note 2
010*	Clock synchronous serial interface	SDI,SDO	65,536
0110	Setting disabled	-	-
0111	Setting disabled	-	-
1000	Setting disabled	-	-
1001	Setting disabled	-	-
1010	80-system 18-bit interface	DB17-0	262,144
1011	80-system 9-bit interface	DB17-9	262,144
1100	Setting disabled	-	-
1101	Setting disabled	-	-
1110	Setting disabled	-	-
1111	Setting disabled	-	-

Notes: 1. 65,536 colors in 16-bit signal transfer mode.  
2. 65,536 colors in 8-bit 2-transfer mode.

80-system 18-bit Bus Interface

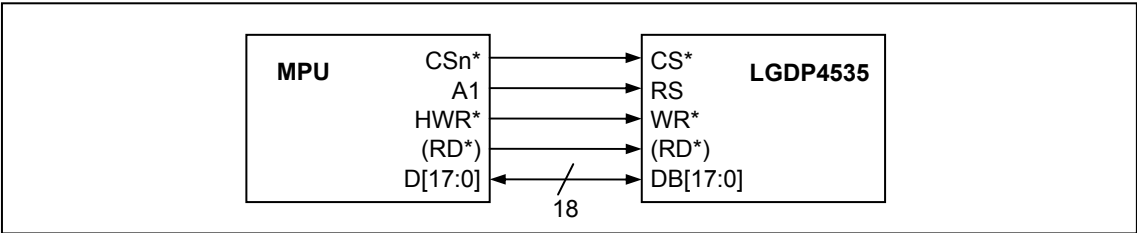


Figure 17 18-bit Interface

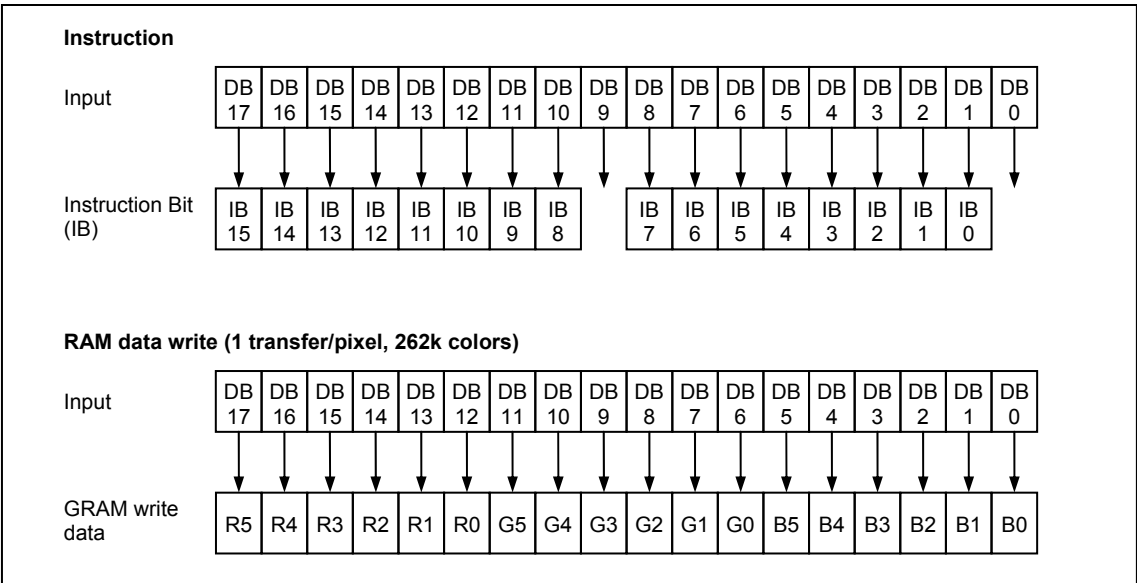


Figure 18 Data format for 18-bit interface



## 80-system 16-bit Bus Interface

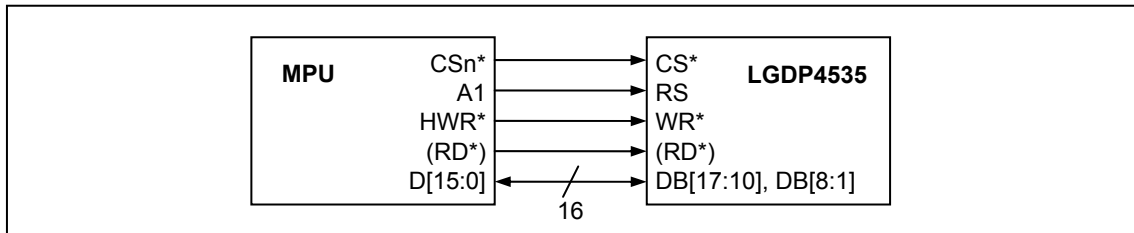


Figure 19 16-bit Interface

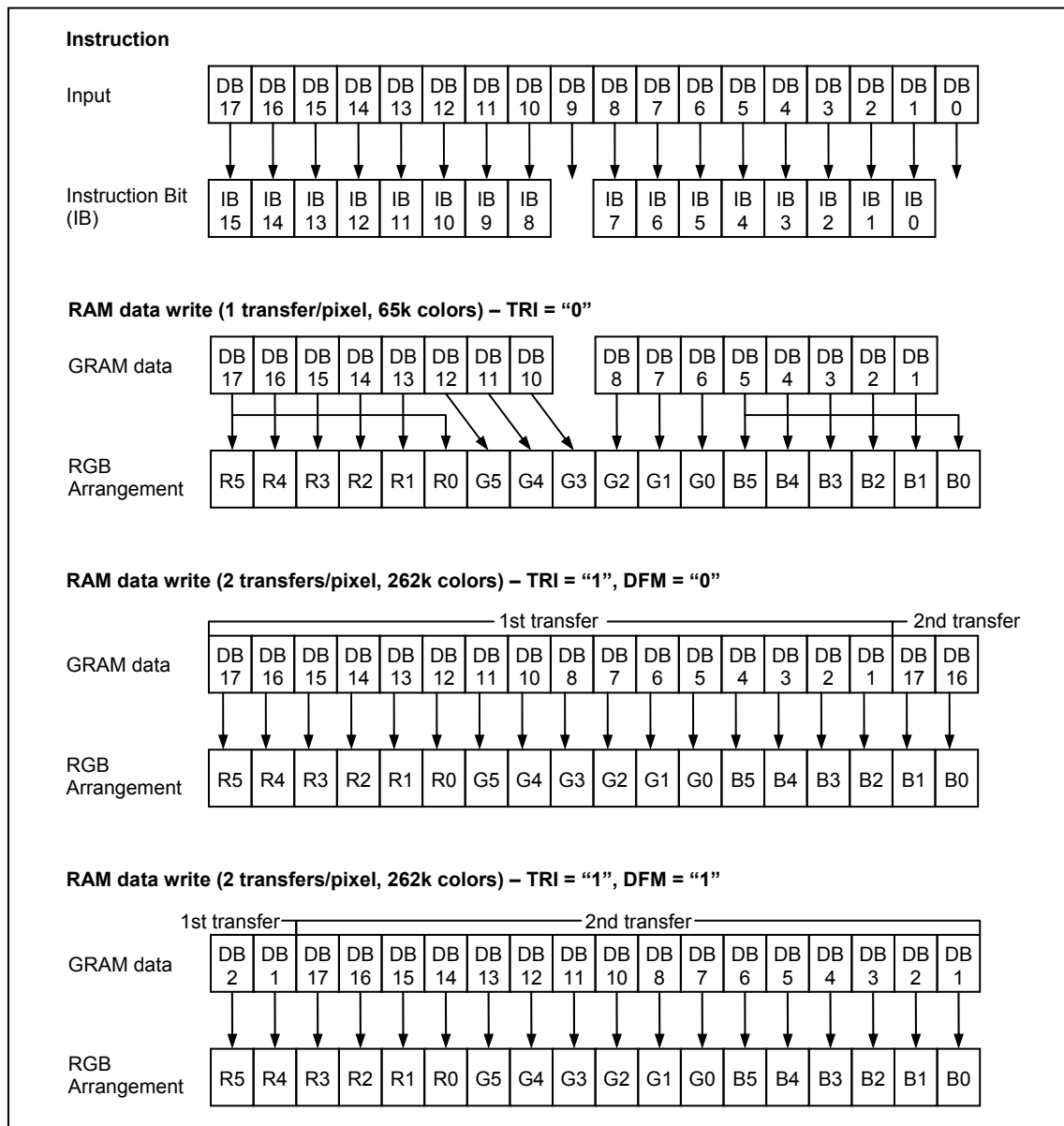
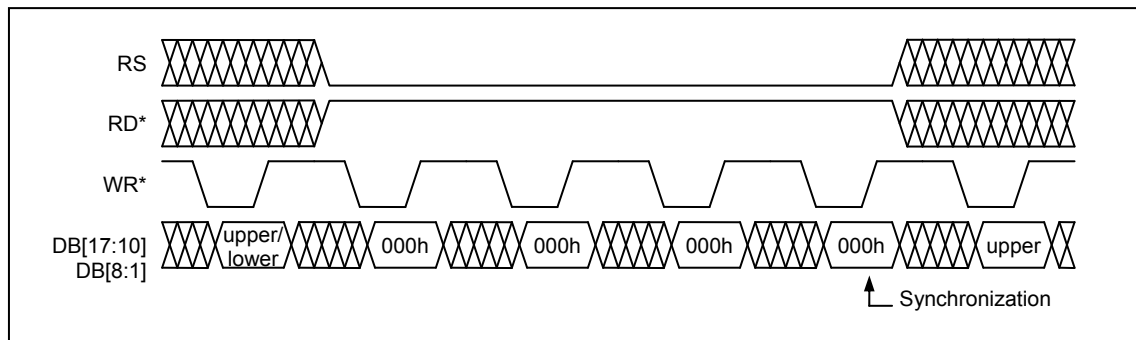


Figure 20 Data format for 16-bit interface

## Data Transfer Synchronous in 16-bit Bus Interface operation

The LGDP4535 supports a data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 2/16 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.



**Figure 21 16-bit Data Transfer Synchronization**

80-system 9-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into the upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing to the index register, the upper byte (8 bits) must be written.

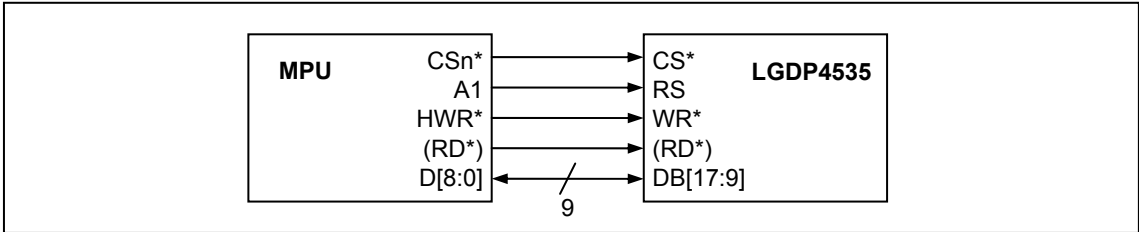


Figure 22 9-bit Inteface

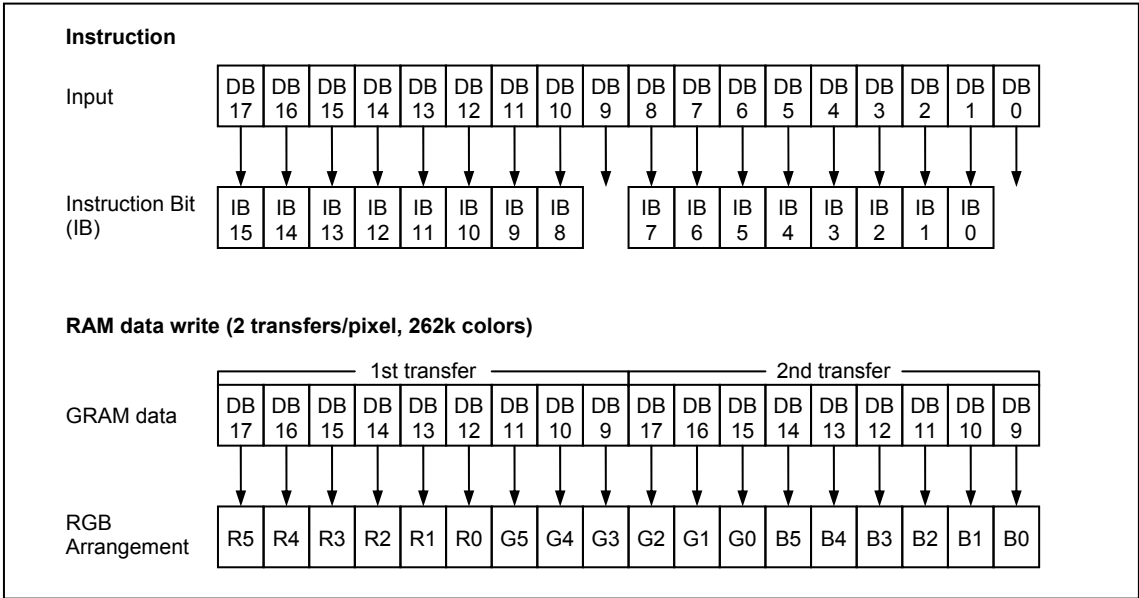


Figure 23 9-bit Inteface Data Format

## Data Transfer Synchronous in 9-bit Bus Interface operation

The LGDP4535 supports a data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 9 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.

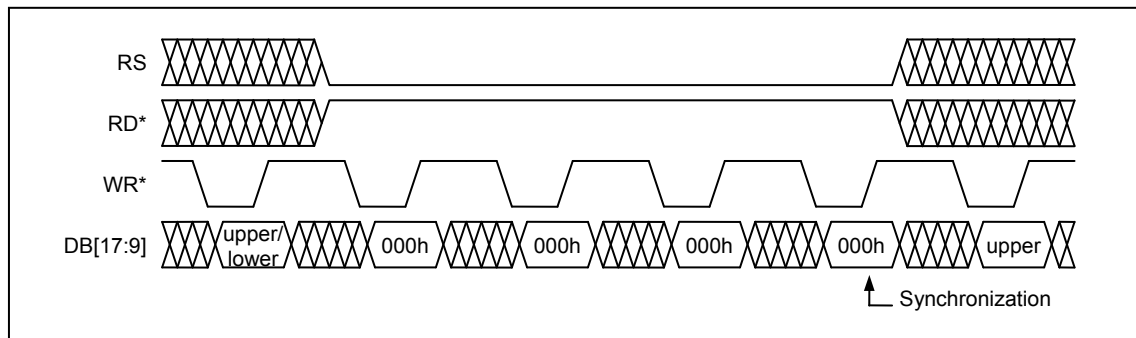


Figure 24 9-bit Data Transfer Synchronization

## 80-system 8-bit Bus Interface

When transferring a 16-bit instruction, it is divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into the upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either the IOVcc or IOGND level. When writing the index register, the upper byte (8 bits) must be written.

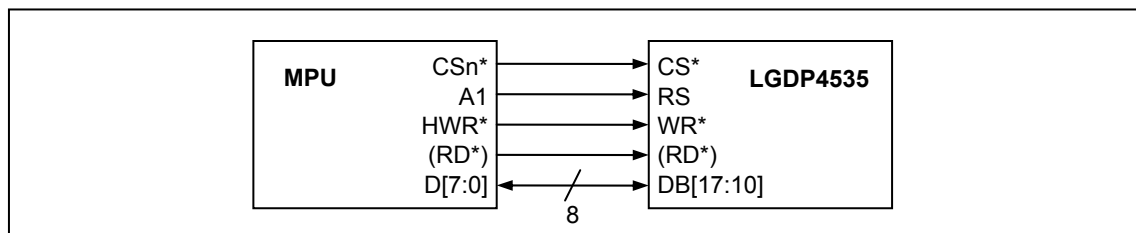


Figure 25 8-bit Interface

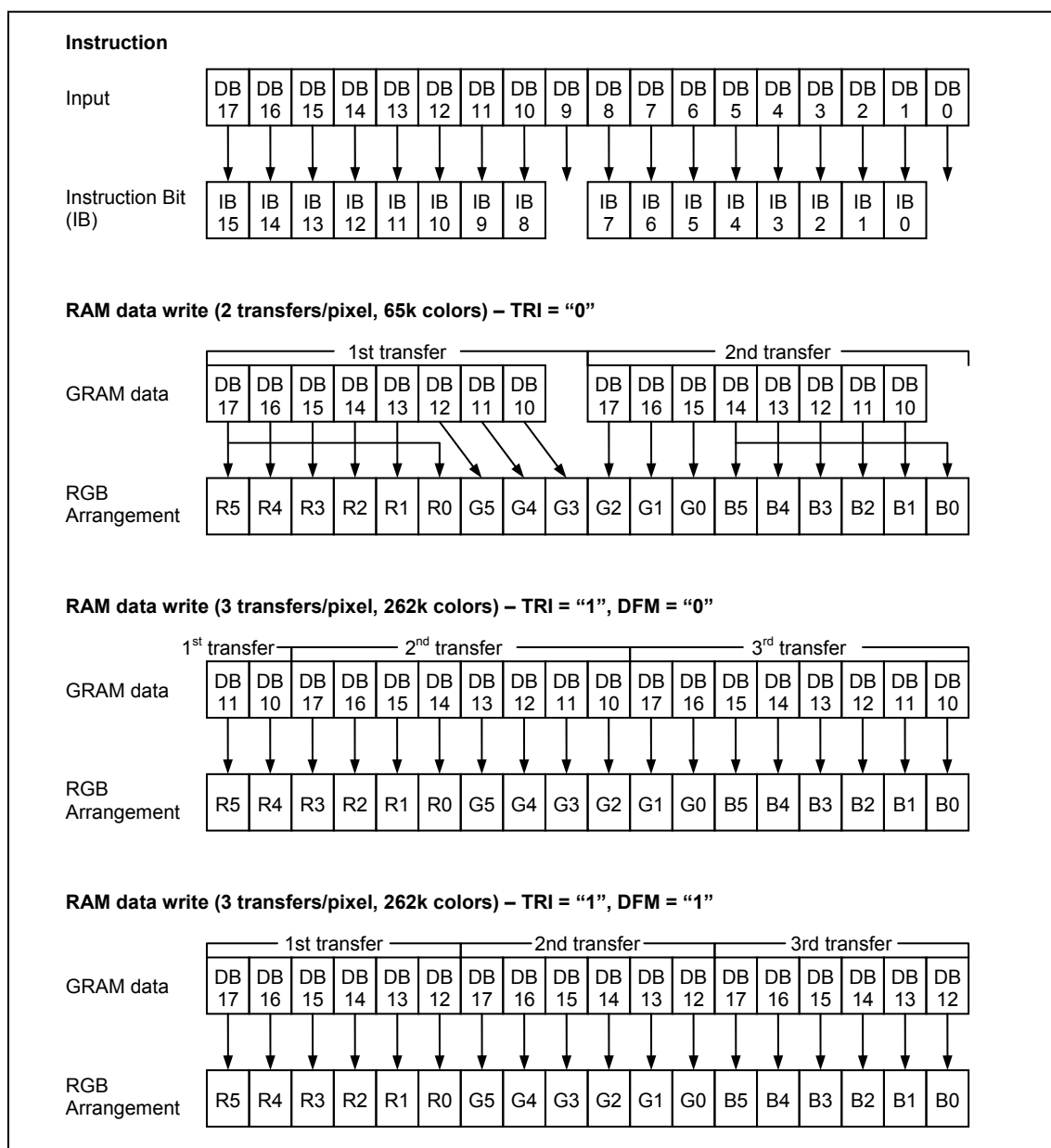
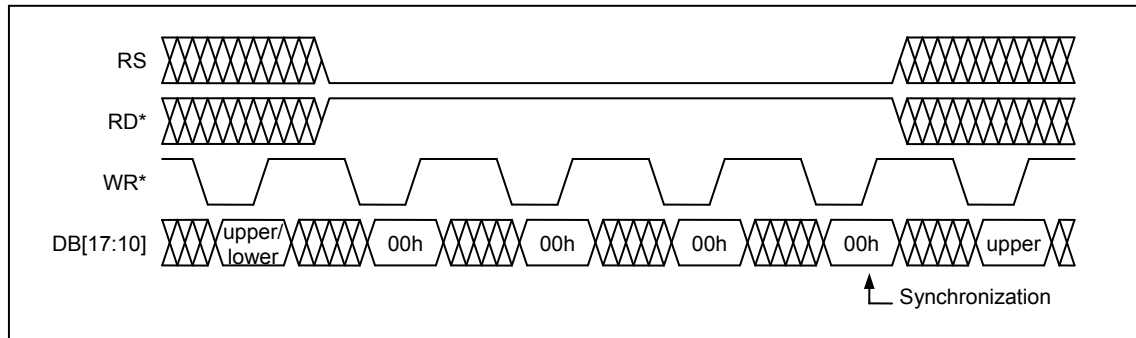


Figure 26 8-bit Interface Data Format

## Data Transfer Synchronous in 8-bit Bus Interface operation

The LGDP4535 supports a data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters to restart data transfers from the upper 8 bits. By executing synchronization periodically, the system can recover from a runaway operation.

Make sure to execute a transfer synchronization after a reset operation before transferring instruction.



**Figure 27 8-bit Data Transfer Synchronization**

## Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the IOGND/IOVcc/IOGND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The LGDP4535 recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The LGDP4535 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4535 are compared and both 6-bit data match, and then the LGDP4535 starts taking in data. The least significant bit of the device identification code is set with the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the LGDP4535 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, an index register write operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). The LGDP4535 receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The LGDP4535 writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the LGDP4535 starts transferring or receiving data in units of bytes. The LGDP4535 executes data transfer from the MSB. The LGDP4535's instruction takes 16-bit format and they are executed inside after it is transferred in two bytes (16 bits: DB15-0) from the MSB (The LGDP4535 expands RAM write data into 18-bit format when writing them to the internal GRAM). The first byte received by the LGDP4535 following the start byte is always the upper eight bits of instruction and the second byte is the lower 8 bits of instruction.

In case of reading data from the GRAM, the LGDP4535 does not transfer valid data until first five bytes of data are read from the GRAM following the start byte. The LGDP4535 starts sending valid data as it reads the sixth and subsequent byte data.

**Table 75 Start byte format**

Transferred bits	1	2	3	4	5	6	7	8
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

**Note:** ID bit is selected by setting the IM0/ID pin.

**Table 76**

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

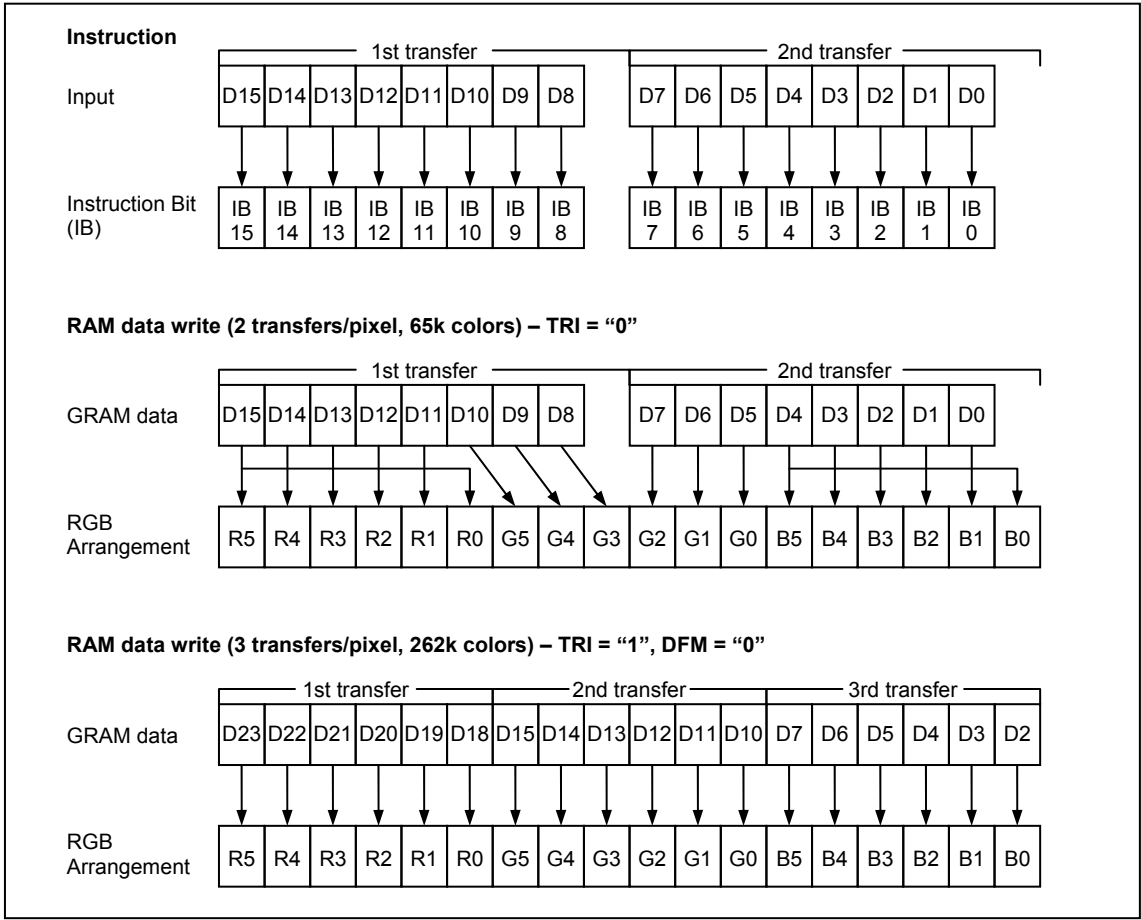
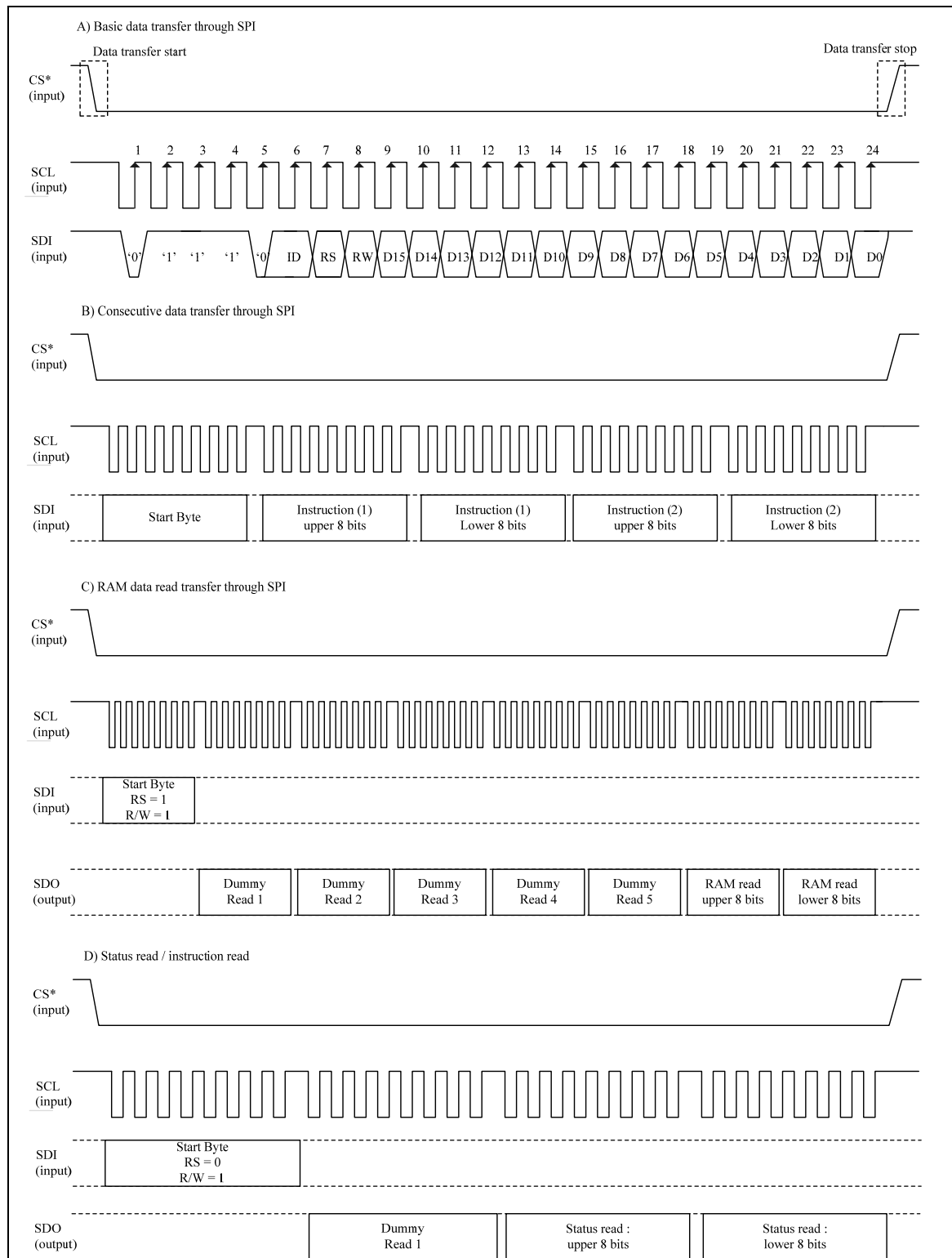


Figure 28 Data format for SPI

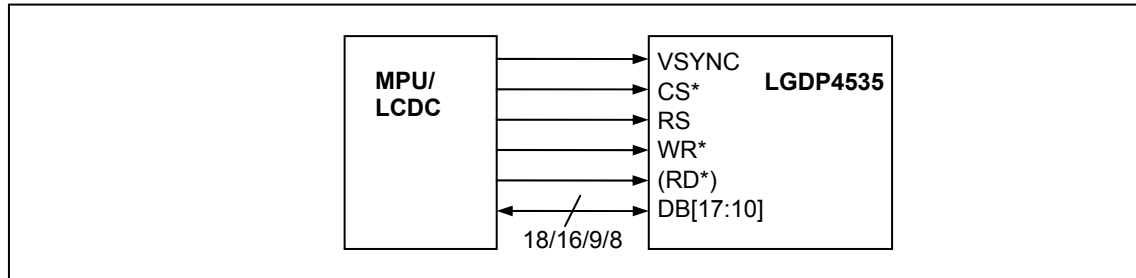




**Figure 29 Data Transfer in Serial interface**

## VSYNC Interface

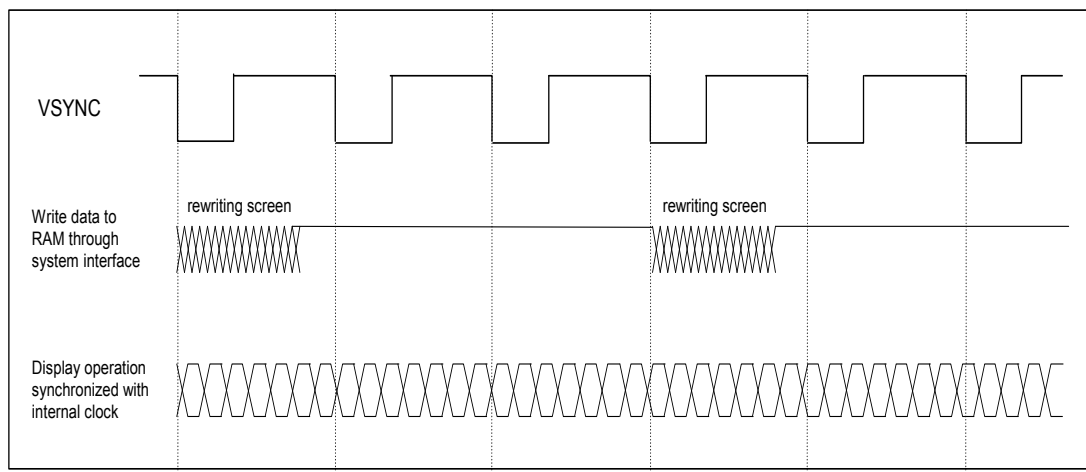
The LGDP4535 supports VSYNC interface, enabling the LGDP4535 to display a moving picture with minimum modifications to the existing system, using system interface and the frame synchronization signal (VSYNC).



**Figure 30 VSYNC Interface**

The VSYNC interface is selected by setting DM[1:0] = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at a speed faster to a certain degree than the internal display operation speed, it becomes possible to rewrite data without flickering the moving picture on display and enables the LGDP4535 to display a moving picture using a system interface.

The LGDP4535 performs the display operation with the internal clock signal generated from the internal oscillator and the VSYNC signal in this mode. In VSYNC mode, the data displayed on the screen are written to the internal RAM in order to transfer only the data to be written over the moving picture RAM area and thereby minimize the total data transfer required for moving picture display.



**Figure 31 Moving Picture Data Transfers via VSYNC Interface**

The VSYNC interface has the minimum speed of writing data to the internal RAM via the system interface and the minimum internal clock frequency, which are calculated from the following formulae.

$$\text{Internal clock frequency (fosc) [Hz]} \\ = \text{FrameFrequency} \times (\text{DisplayLines (NL)} + \text{FrontPorch (FP)} + \text{BackPorch (BP)}) \times 60 \text{ clocks} \times \text{variance}$$

$$\text{RAMWriteSpeed} > \frac{240 \times \text{DisplayLines (NL)}}{(\text{BackPorch (BP)} + \text{DisplayLines (NL)} - \text{margins}) \times 60 \text{ clocks} \times \frac{1}{fosc}}$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum RAM writing speed and internal clock frequency in VSYNC interface mode is as follows.

**[Example]**

Display size	240 RGB × 320 lines
Lines	320 lines
Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	70 Hz

**Internal clock frequency (fosc)**

$$= 70 \text{ Hz} \times (320 + 2 + 14) \text{ lines} \times 60 \text{ Clocks} \times 1.1 / 0.9 = 1.72 \text{ MHz}$$

When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

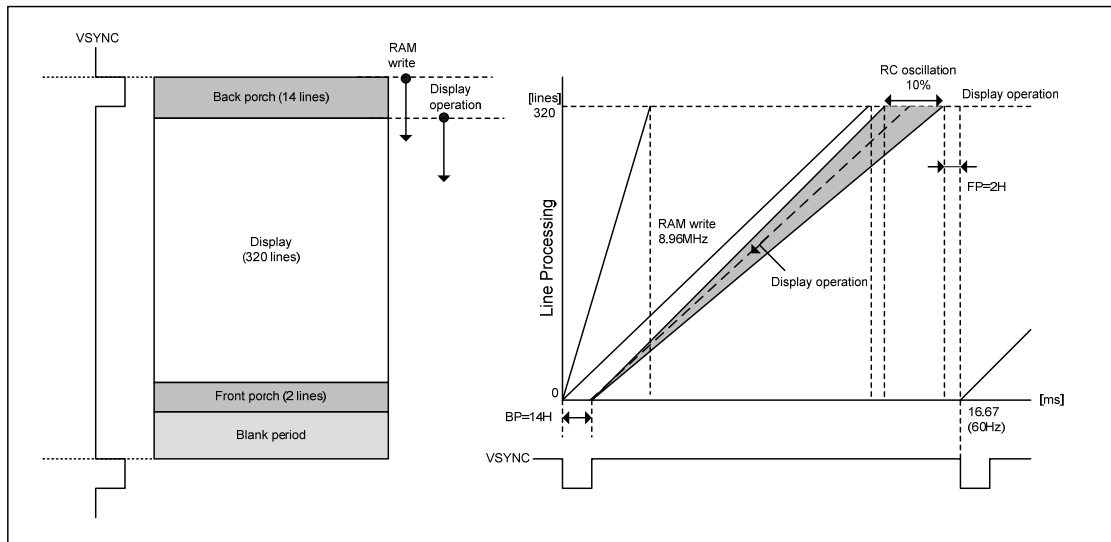
In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as differences in external resistors or voltage changes are not in consideration. It is necessary to allow for an enough margin if these factors must be incorporated.

**Minimum speed for RAM writing**

$$240 \times 320 / \{((14 + 320 - 2) \text{ lines} \times 60 \text{ clock}) / 1.72 \text{ MHz}\} = 6.63 \text{ MHz}$$

The above theoretical value is calculated on the premise that the LGDP4535 starts writing data to the internal RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line where display operation is performed and the RAM line address where data write operation is performed.

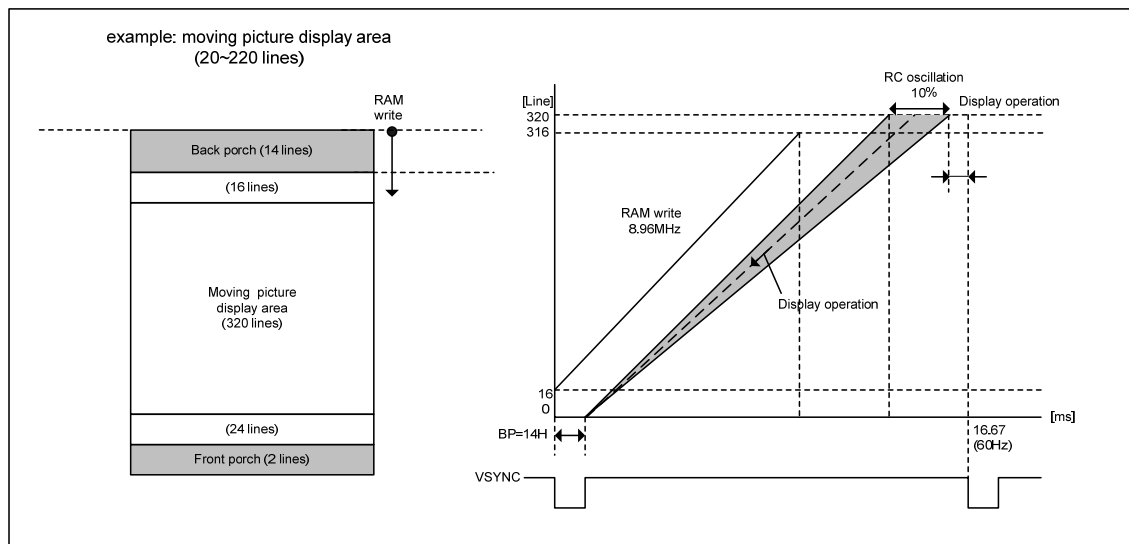
The RAM write speed of 6.63MHz or more on the falling edge of VSYNC will guarantee the completion of RAM write operation before the LGDP4535 starts displaying the RAM data on the screen, enabling rewriting the entire screen without flicker.



**Figure 32 Write/Display Operation Timing via VSYNC Interface**

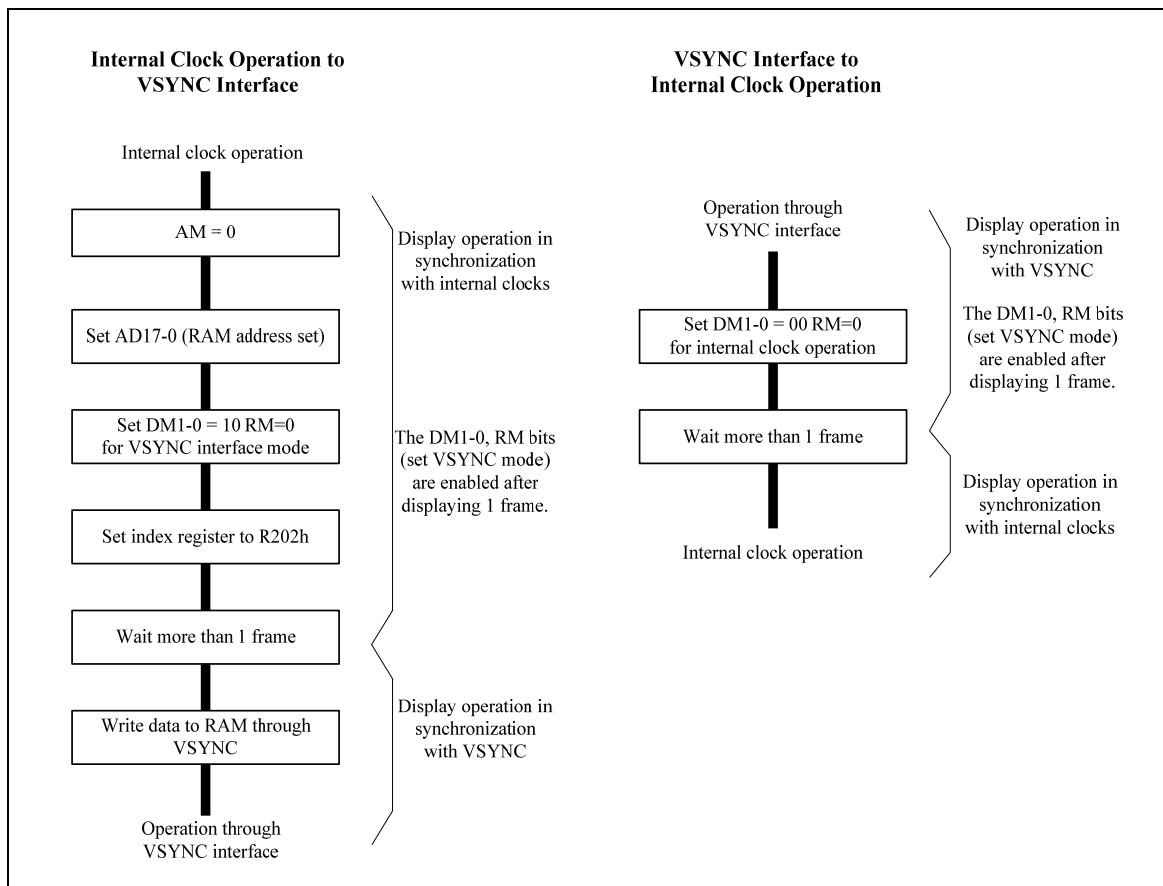
### Notes in using the VSYNC interface

1. The above example of calculation gives a theoretical value. In the actual setting, other possible causes of variances not counted in the above example such as differences in internal oscillators should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a RAM writing speed.
2. The above example of calculation gives a minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting a minimum RAM writing speed can have extra margins.



**Figure 33 RAM write margin**

3. After drawing 1 frame, a front porch period continues until the next input of VSYNC is detected.
4. When switching from the internal clock operation mode (DM1-0 = "00") to the VSYNC interface mode, or the other way around, it is enabled from the next VSYNC cycle, i.e. after completing the display of the frame, which the LGDP4535 was internally processing when switching the modes.
5. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.
6. In VSYNC interface mode, set the AM bit to "0" to transfer display data in the method mentioned above.



**Figure 34 Sequences to Switch between VSYNC and Internal Clock Operation Modes**

## External Display Interface

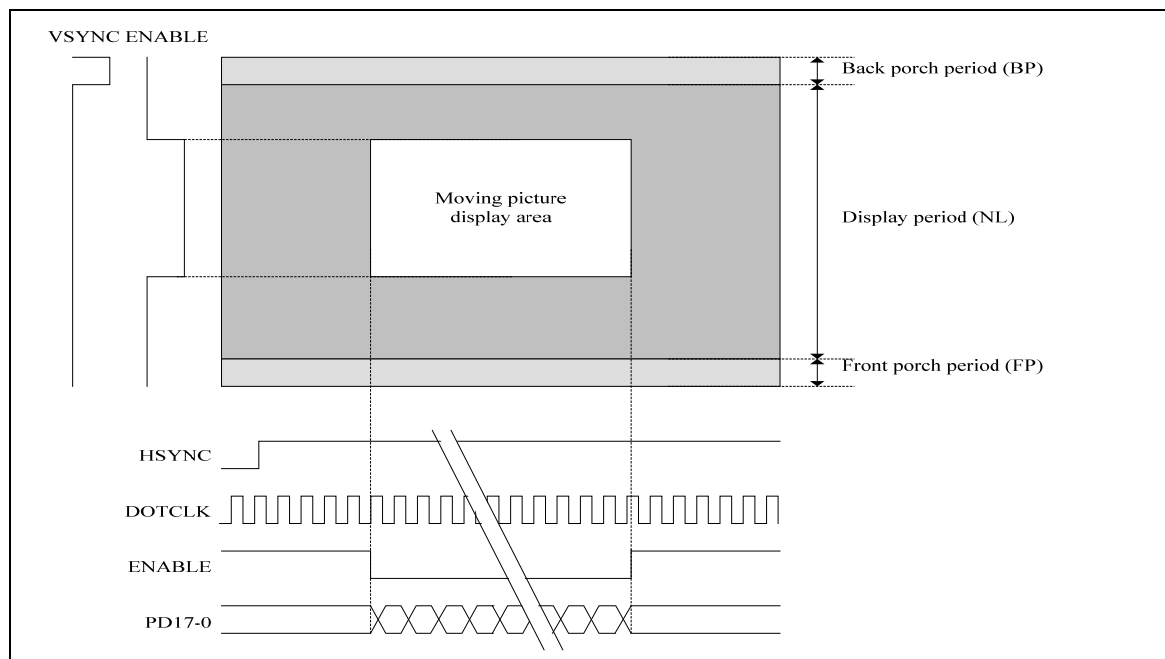
The following RGB interfaces are available with the LGDP4535. The interface operation is set with the RIM[1:0] bits. The RGB interface is used for RAM access.

**Table 77**

RIM[1:0]	RGB Interface	DB Pin
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	-

### RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface in combination with the window address function enables minimizing data transfer by rewriting data in high-speed with low power consumption only within the RAM area where data must be updated. In RGB interface operation, it is necessary to set back and front porch periods before and after the display period, respectively.



**Figure 35 Display Operation via RGB Interface**

## Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals are changeable by setting the DPL, EPL, HSPL, and VSPL bits, respectively according to the system configuration.

## RGB Interface Timing

The timing relationships of signals in RGB interface operation area as follows.

### 16-18-bit RGB Interface Timing

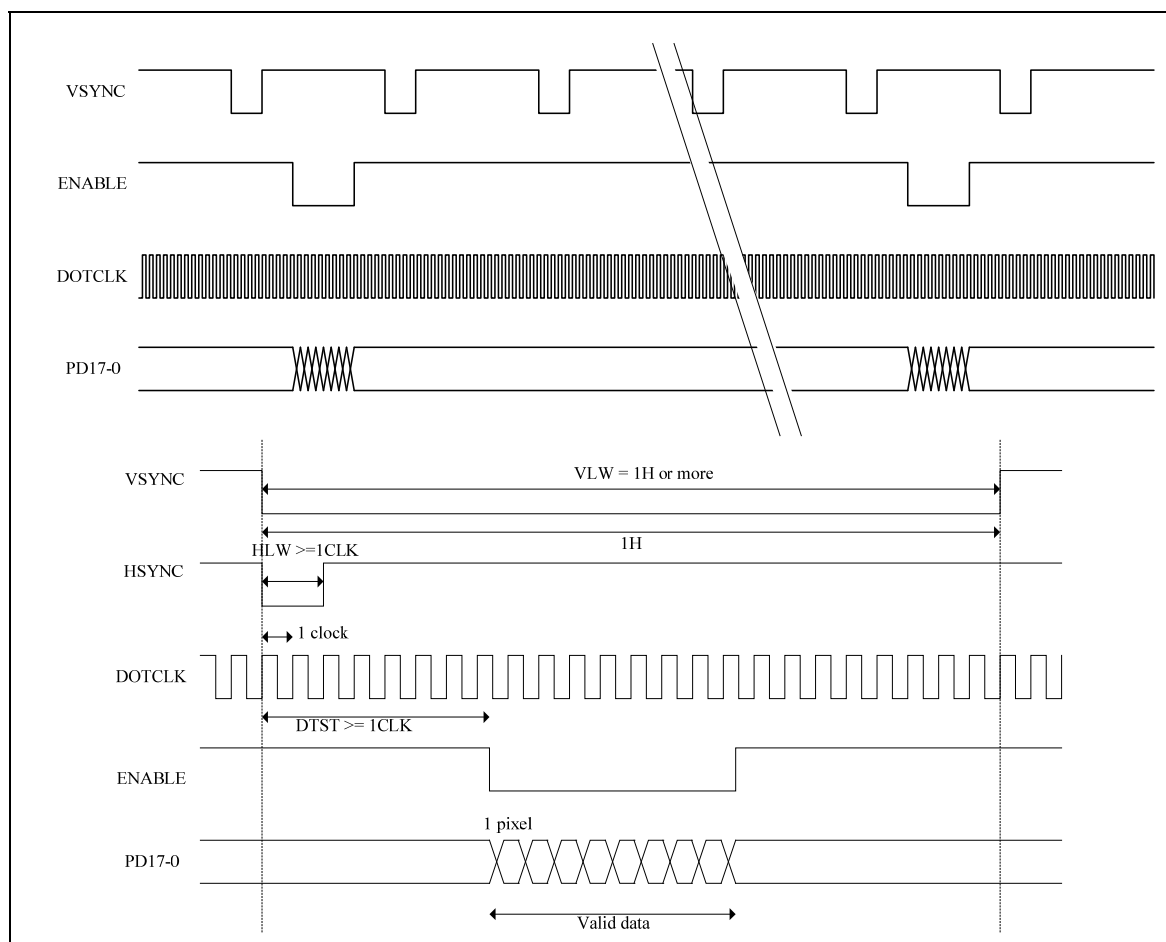
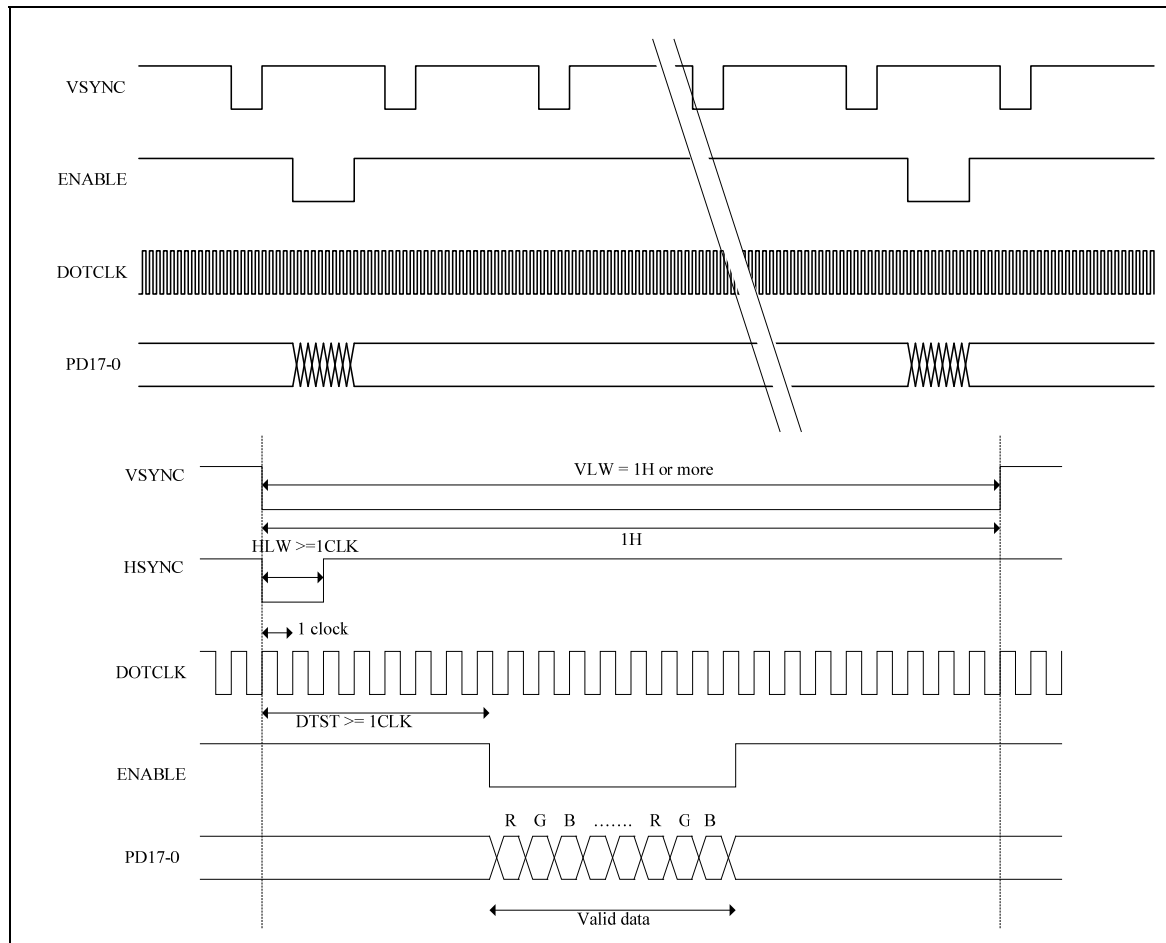


Figure 36

Notes: 1. VLW : VSYNC Low period  
 HLW : HSYNC Low period  
 DTST : data transfer setup time

## 6-bit RGB Interface Timing



**Figure 37**

- Notes: 1. VLW : VSYNC Low period  
 HLW : HSYNC Low period  
 DTST : Data transfer setup time
2. In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so that one pixel is transferred in units of three DOTCLKs via DB17-12 (DB5-0).

## Moving Picture Display with the RGB Interface

The LGDP4535 supports RGB interfaces for displaying a moving picture and RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function can minimize data transfer by specifying a moving picture RAM area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. The data transfer is limited to a moving picture RAM area.
4. The reduction in data transfer contributes to the reduction in power consumption by the entire system
5. The combined use with system interface allows updating data in the still picture area, such as icons, while displaying a moving picture via RGB interface



## RAM access via system interface in RGB interface operation

The LGDP4535 allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the RAM via system interface, set ENABLE “High” to stop writing data via RGB interface. Then set RM = “0” to enable RAM access via system interface. When reverting to the RGB interface operation, wait for a time for a read/write bus cycle. Then, set RM = “1” and the index register to R22h to start accessing RAM via RGB interface. A conflict between RAM accesses via two different interfaces will not guarantee write operation.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

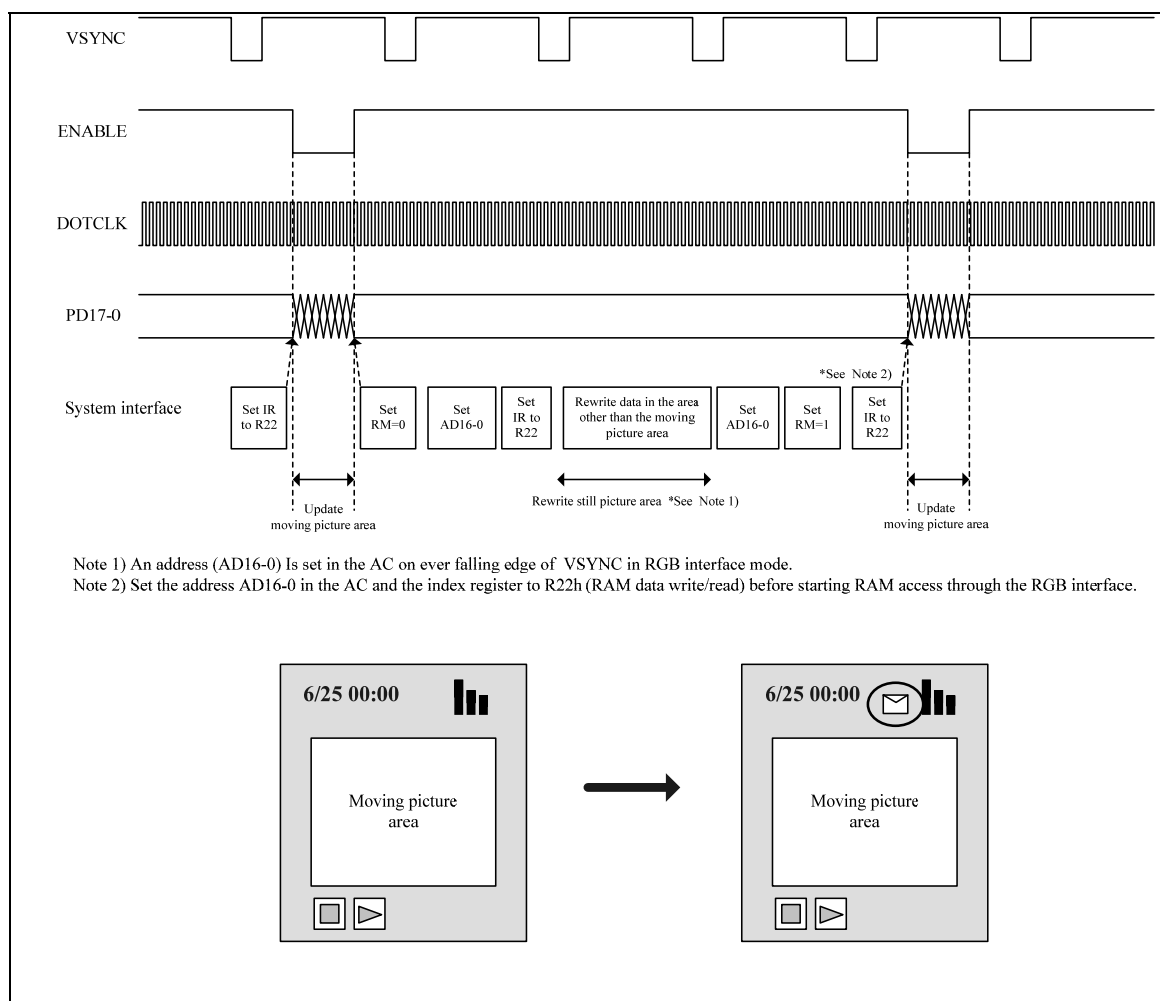


Figure 38 Updating the Still Picture Area while Displaying Moving Picture

6-bit RGB Interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus according to data enable signal (ENABLE). Unused pins DB[11:0] must be fixed at either IOVcc or IOGND level.

The instructions are set only via system interface.

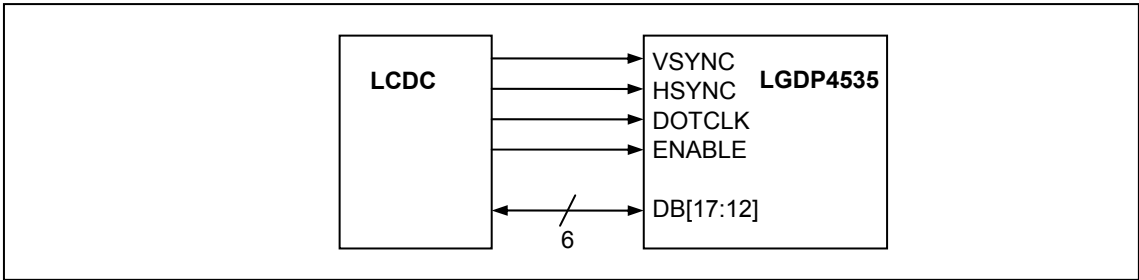


Figure 39 6-bit RGB interface

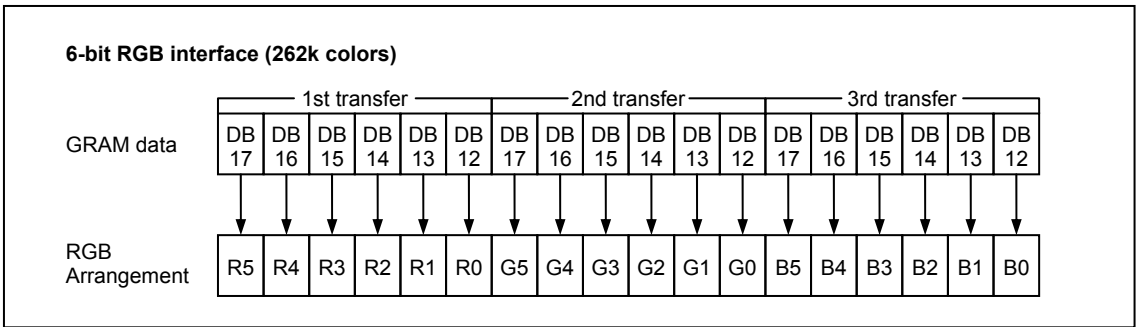
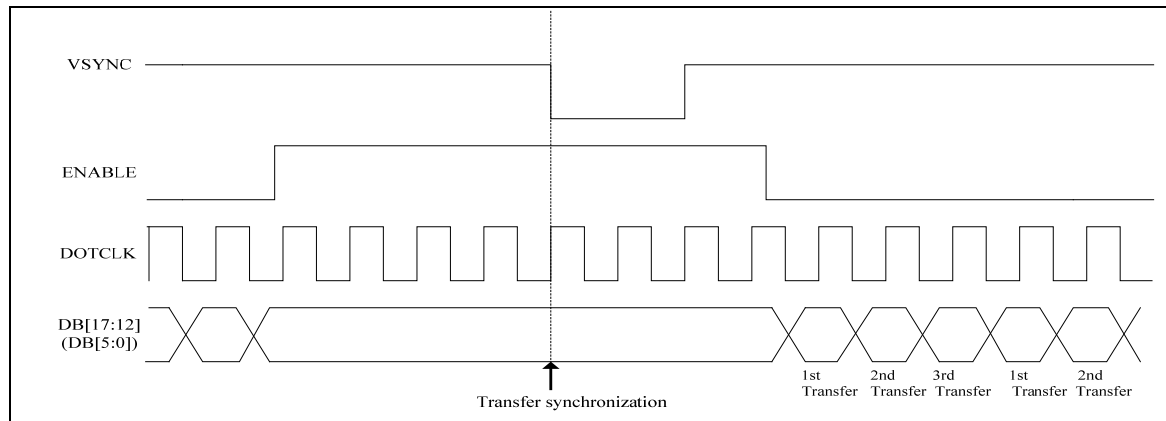


Figure 40 Data format for 6-bit interface

## Data Transfer Synchronization in 6-bit Bus Interface operation

The LGDP4535 has data transfer counters to count the first, second, and third 6-bit data transfers in 6-bit RGB interface operation. The transfer counters are always reset to the first data transfer on the falling edge of VSYNC. If there is a mismatch in the number of data transfers, the counters are reset to the first data transfer at the start of each frame (on the falling edge of VSYNC) and data transfer can be restarted in correct order from the next frame. In case of displaying a moving picture, which requires consecutive data transfer, this function can minimize the effect from the data transfer mismatch and help recover the display system to a normal state.



**Figure 41 6-bit Transfer Synchronization**

16-bit RGB Interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus according to data enable signal (ENABLE).

The instructions are set only via system interface.

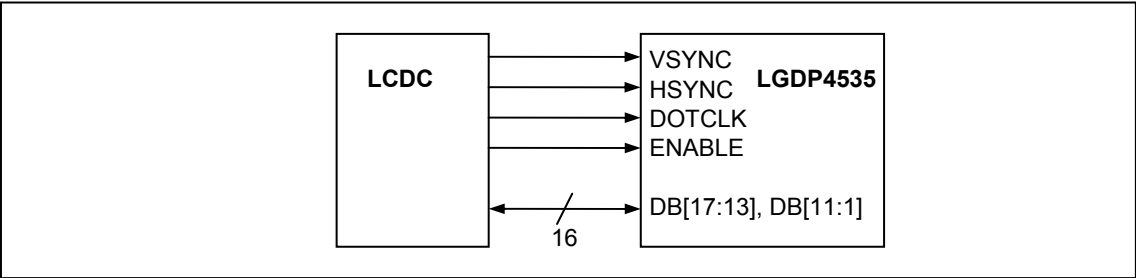


Figure 42 16-bit RGB interface

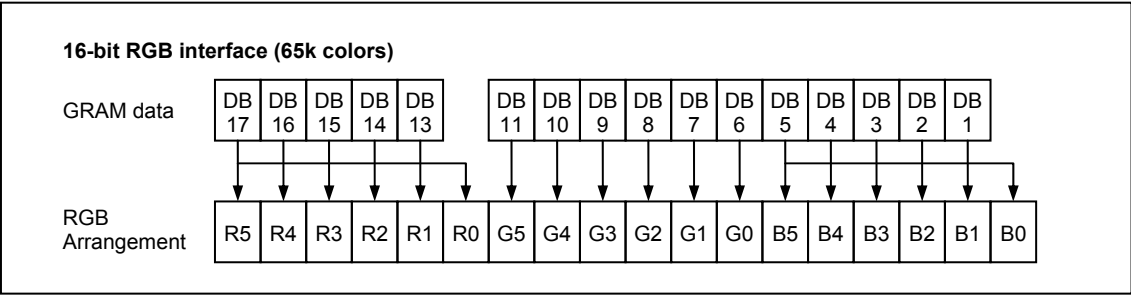


Figure 43 Data format for 16-bit interface

18-bit RGB Interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) according to data enable signal (ENABLE).

The instructions are set only via system interface.

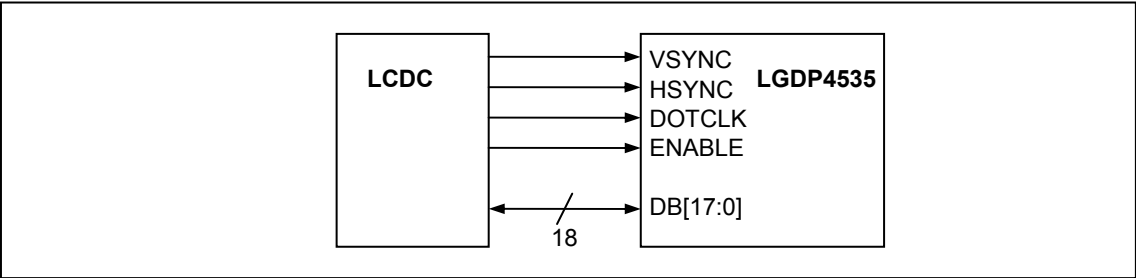


Figure 44 18-bit RGB interface

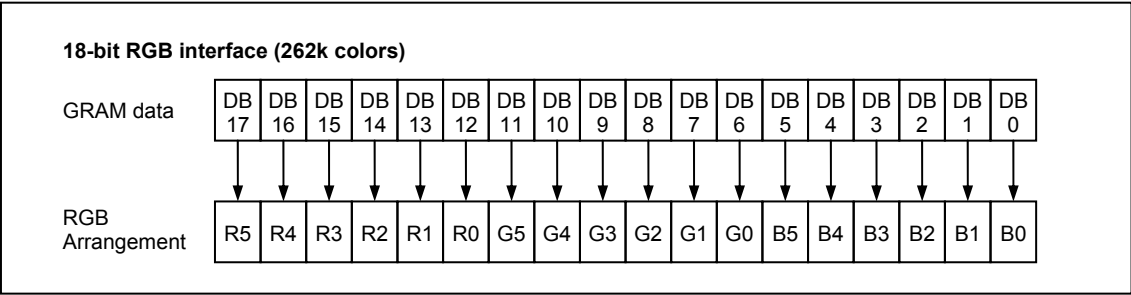


Figure 45 Data format for 18-bit interface

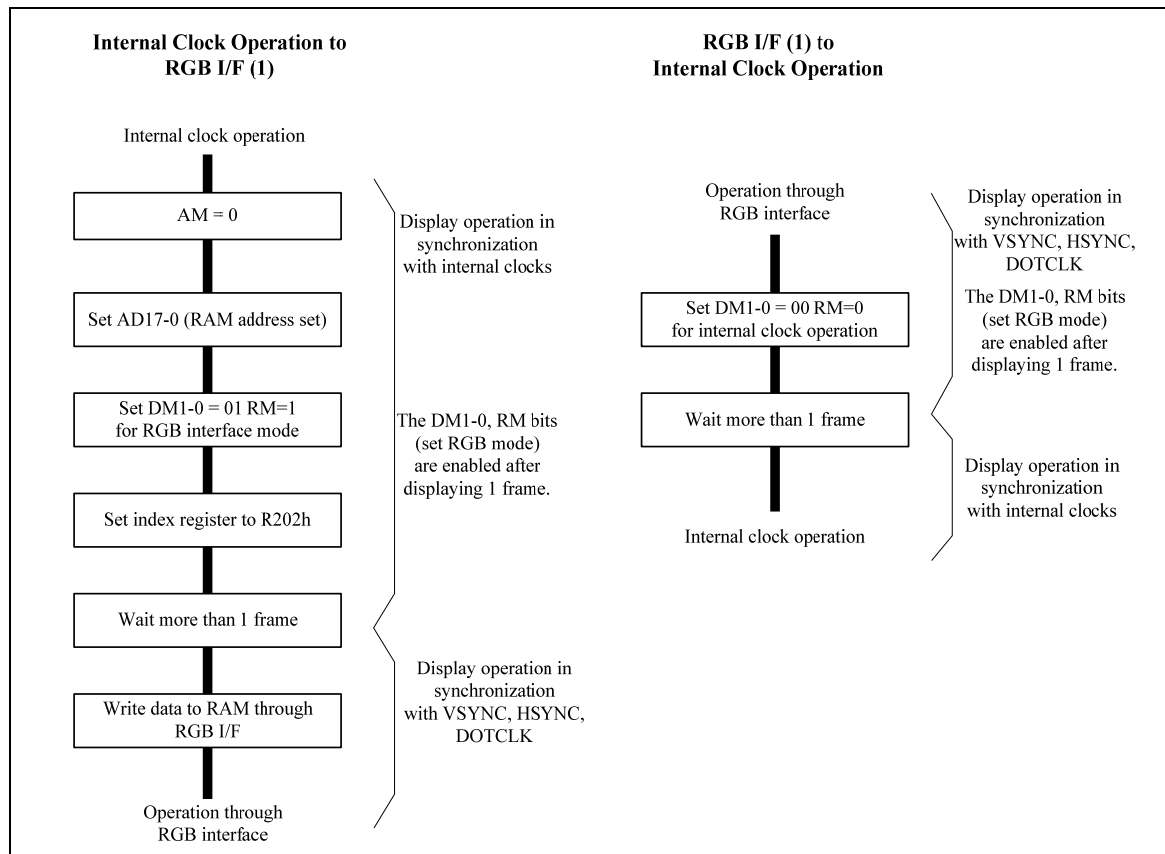
## Notes on Using the External Display Interface

1. The following functions are not available in external display interface operation.

**Table 78 Functions Not Available in External Display Interface operation**

Fucntion	External Display Interface	Internal Display Interface
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied throughout the display operation.
3. The reference clock for generating liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.
4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel.
5. In 6-bit RGB interface operation, each 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. Take this into consideration and make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE, and data transfer via DB17-12 so that data transfer is completed in units of pixels.
6. When switching between the internal operation mode and the external display interface operation, follow the sequences in Figure 46 RGB and Internal Clock Operation Mode switching sequences.
7. In RGB interface operation, a front porch period continues until the next VSYNC input is detected after the end of each frame period.
8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to the internal RAM.
9. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.



**Figure 46 RGB and Internal Clock Operation Mode switching sequences**

## RAM Address and Display Position on the Panel

The LGDP4535 has memory to store display data of 240RGB x 320 lines. The LGDP4535 incorporates a circuit to control partial display, which enables switching driving methods for full-screen display and partial display.

The LGDP4535 allows separate settings for display control and driving position control and specifying a RAM area for each image displayed on the screen. This structure enables designing a display on the screen not constrained by the mounting position of the display panel.

The following is the sequence of settings for full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image with PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, the register setting in SS bit is required when writing RAM data.

**Table 79**

	Display ENABLE	Numbers of Lines	RAM area
<b>Base image</b>	BASEE	NL	(BSA, BEA) = (9'h000, 9'h13F)

Notes : 1: The base image is displayed from the first line of the screen.  
 2: Make sure  $NL \leq 320$  (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h13F, respectively.

**Table 80**

	Display ENABLE	Display position	RAM start position
<b>Partial image 1</b>	PTDE0	(PTDP0, PTEA0)	PTSA0
<b>Partial image 2</b>	PTDE1	(PTDP1, PTEA1)	PTSA1



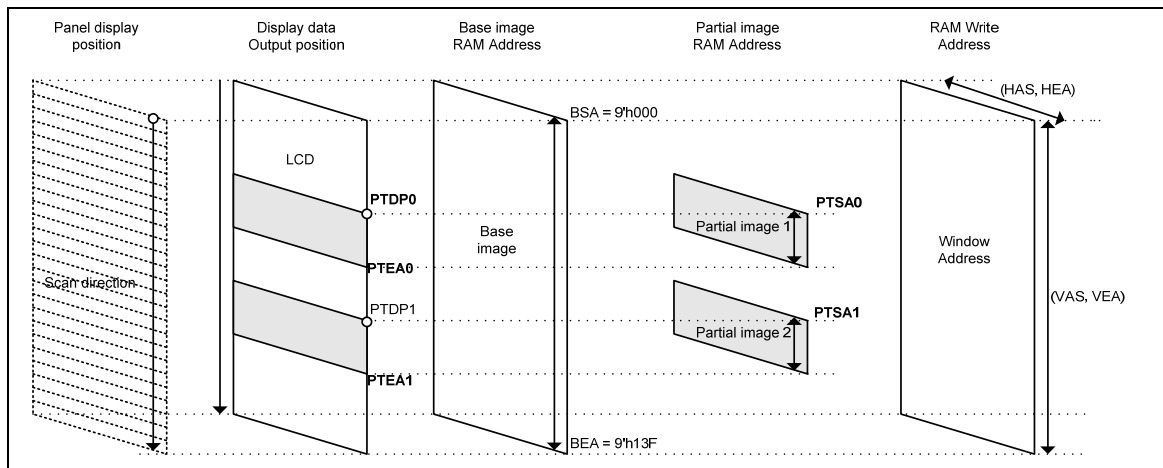


Figure 47 RAM Address, display position and drive position

## Restrictions in setting display control instruction

The following are the constraints in setting coordinates of display data, display position, and partial image display.

### Screen setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is within the limit:  $NL \leq 320$  lines

#### Base image display

1. The base image is displayed from the first line of the screen:  $BSA = 1_{st} \text{ line (of the display panel)}$
2. The base image RAM area specified with BSA, BEA must include the same or more number of lines necessary to drive the liquid crystal panel (NL setting):  $BEA - BSA \geq NL$

#### Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partials do not overlap each other.

$$0 \leq PTDP0 \leq PTEA0 < \\ PTDP1 \leq PTEA1 \leq NL$$

The following figure shows the relationship among the RAM address, display position, and driving positions of the panel.

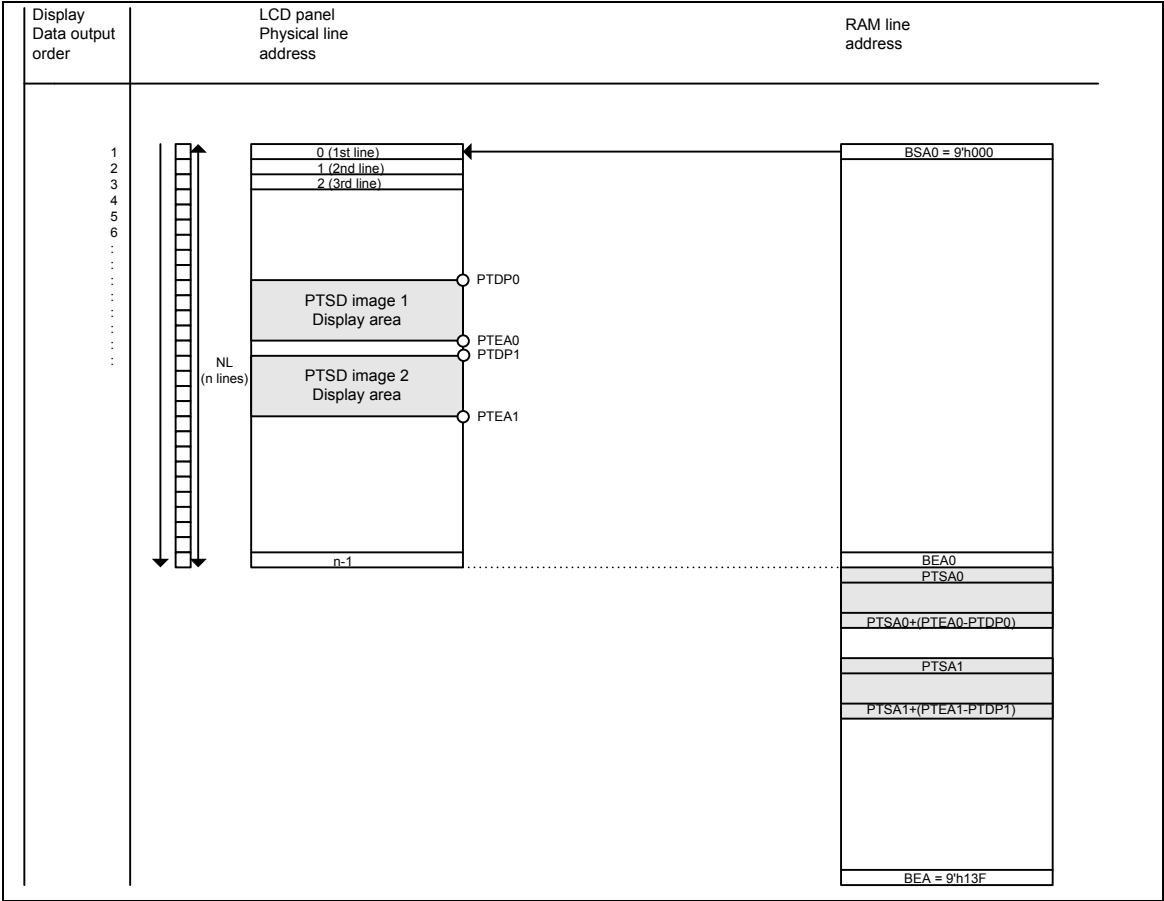


Figure 48 Display RAM Address and display position

Note: In this figure, the RAM address is defined in relation to the display position on the panel. Inside the LGDP4535, the RAM address area where the data is written is defined within a window address area on the GRAM address mapping.

Instruction setting example

The followings are the examples of settings for 240(RGB) x 320(lines) panels.

1. Full screen display (no partial)

The following is an example of setting for full screen display.

Table 81

Base image display insruction

BASEE	1
NL[5:0]	6'h27
PTDE0	0
PTDE1	0

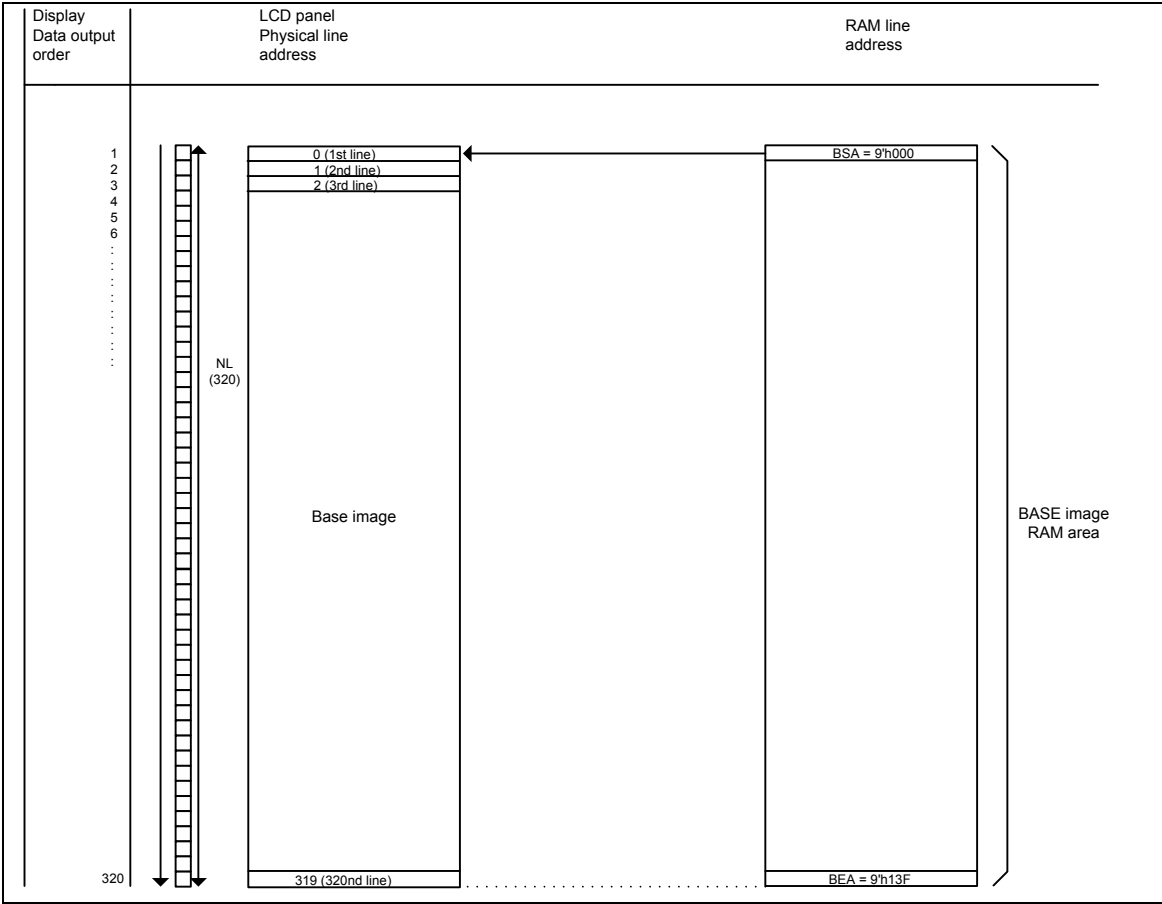


Figure 49 Full screen display (no partial)

2. Partial only

The following is an example of setting for displaying partial image 1 only and turning off the base image display. The partial image 1 is displayed at the position designated by users.

Table 82

Base image display insruction

BASEE	0
NL[5:0]	6'h27

Partial image 1 display insruction

PTDE0	1
PTSA0[8:0]	9'h000
PTEA0[8:0]	9'h08F
PTDP0[8:0]	9'h080

Partial image 2 display insruction

PTDE1	0
PTSA1[8:0]	9'h000
PTEA1[8:0]	9'h000
PTDP1[8:0]	9'h000

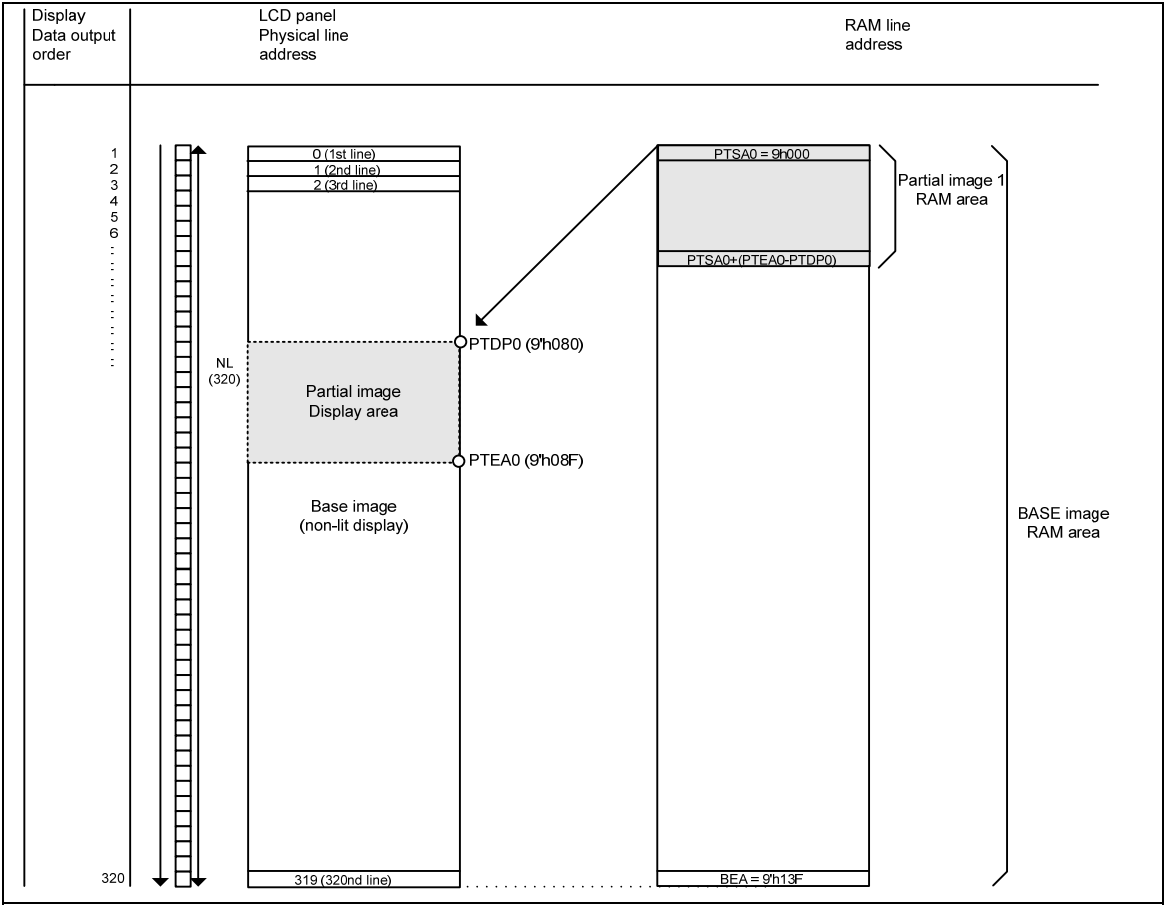


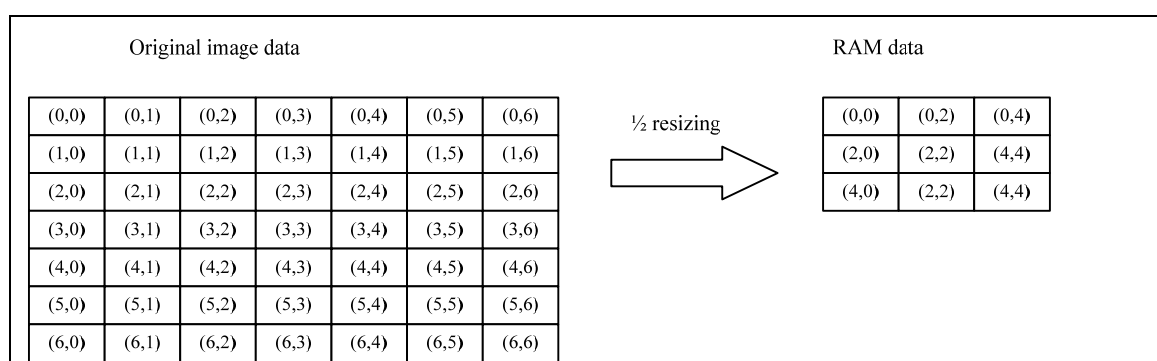
Figure 50 Partial display

## Resizing function

The LGDP4535 supports resizing function ( $\times 1/2$ ,  $\times 1/4$ ), which is executed when writing image data. The resizing function is enabled by setting a window address area and the RSZ bit representing the contraction factor ( $\times 1/2$  or  $\times 1/4$ ) of the image. This function enables the LGDP4535 to write the resized image data directly to the internal RAM, while allowing the system to transfer the original-sized image data.

The resizing function allows the system just to transfer data as usual even when resizing of the image is required. This feature makes a resized image easily available with various applications such as camera display, sub panel display, thumbnail display and so on.

The LGDP4535 processes the contraction of an image simply by selecting pixels. For this reason, the resized image may appear distorted when compared with the original image. Check the resized image before use.



**Figure 51 Data transfer in resizing**

**Table 83**

Original image size (X x Y)	Resized image Size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
640x480(VGA)	320x240	160x120
352x288(CIF)	176x144	88x72
320x240(QVGA)	160x120	80x60
176x144(QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

## Resizing setting

The RSZ bit sets the resizing (contraction) factor of an image. When setting the RAM area using the window address function, the window address area must be just the size of the resized picture. If resizing creates surplus pixels, which are calculated from the following equations, set them with the RCV, RCH bits before writing data to the internal RAM.

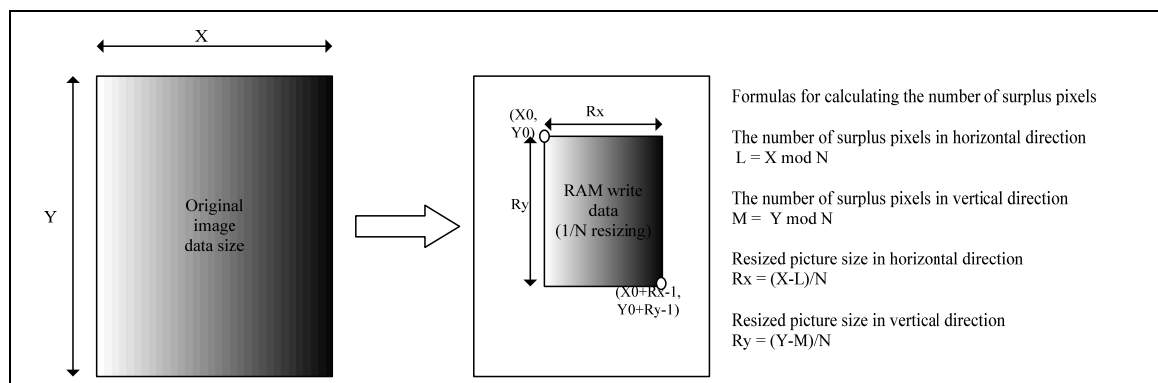


Figure 52 Resizing Setting, surplus pixel calculation

Table 84

### Image (before resizing)

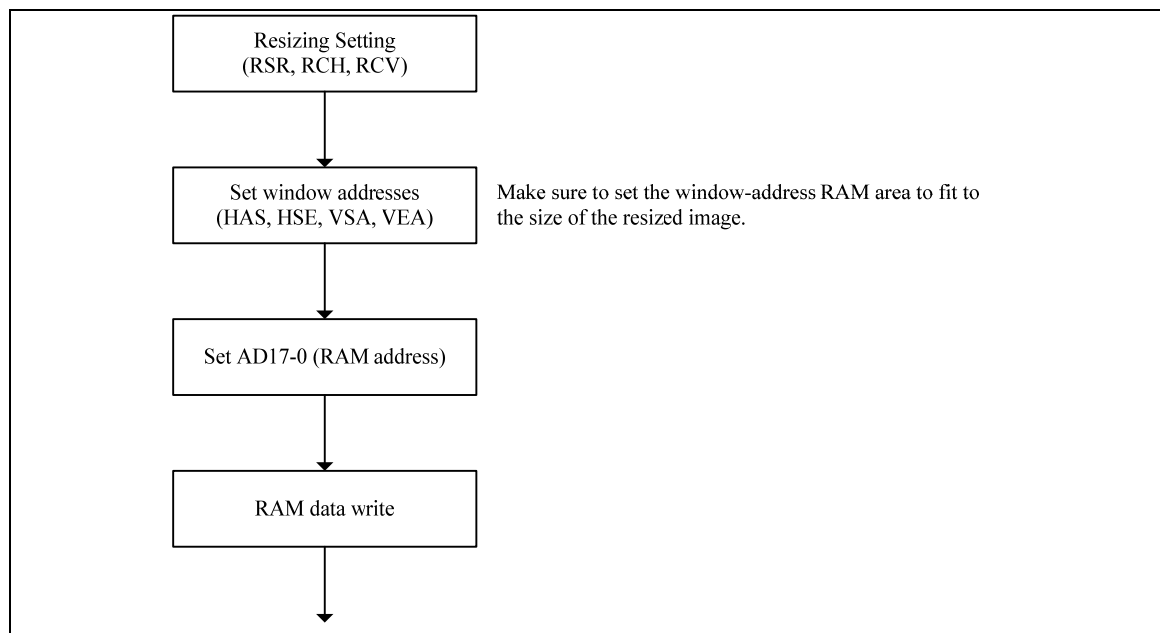
Number of data in horizontal direction	$X$
Numbef of data in vertical direction	$Y$
Resizing ratio	$1/N$

### Resizing setting in the LGDP4535

Resizing setting	RSZ	$N-1$
Numbef of data in horizontal direction	RCH	$L$
Numbef of data in vertical direction	RCV	$M$
RAM writing start address	AD	$(X0, Y0)$
RAM window address	HAS	$X0$
	HEA	$X0 + R_x - 1$
	VSA	$Y0$
	VEA	$Y0 + R_y - 1$

## Notes to Resizing function

1. Set the resizing instruction bits (RSZ, RCV, and RCH) before writing data to the internal RAM.
2. When writing data to the internal RAM using resizing function, make sure to start writing data from the first address of the window address area in units of lines.
3. Set the window address area in the internal RAM to fit the size of the resized image.
4. Set AD16-0 before start transferring and writing data to the internal RAM.
5. Set the RCH, RCV bits only when using resizing function and there are remainder pixels. Otherwise (if  $RSZ = 2'h0$ ), set  $RCH = RCV = 2'h0$ .



**Figure 53 RAM write operation sequence in resizing**

## FMARK function

The LGDP4535 outputs an FMARK pulse in the timing when driving the line specified with FMP[9:0] bits. The FMARK signal can be used as a trigger signal in writing display data in synchronization with display operation by detecting the address where the RAM data is read out for display operation.

The output interval of FMARK pulse can be set with the FMI[2:0] bits. Set the FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. Sets FMARKOE = 1 when outputting FMARK pulse from the FMARK pin.

**Table 85**

FMP[9:0]	FMARK output position
10'h000	0
10'h001	1
10'h002	2
:	:
10'h2AD	685
10'h2AE	686
10'h2AF	687
10'h2B0 ~ 3FF	Setting disabled

**Table 86**

FMI[2:0]	FMARK output interval
3'h0	One frame period
3'h1	2 frame periods
3'h3	4 frame periods
3'h5	6 frame periods
Other setting	Setting disabled



## FMP setting example

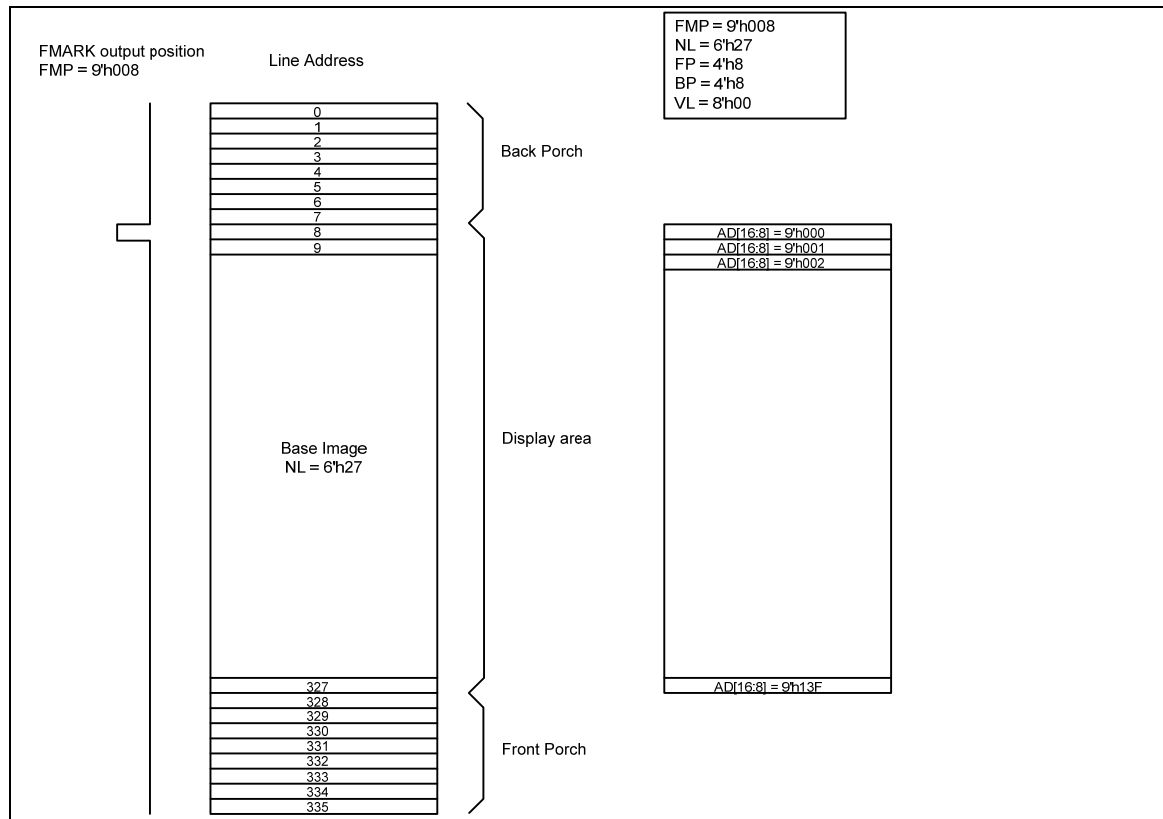


Figure 54

## Display operation synchronous data transfer using FMARK

The LGDP4535 uses FMARK signal as a trigger signal to start writing data to the internal GRAM in synchronization with display scan operation.

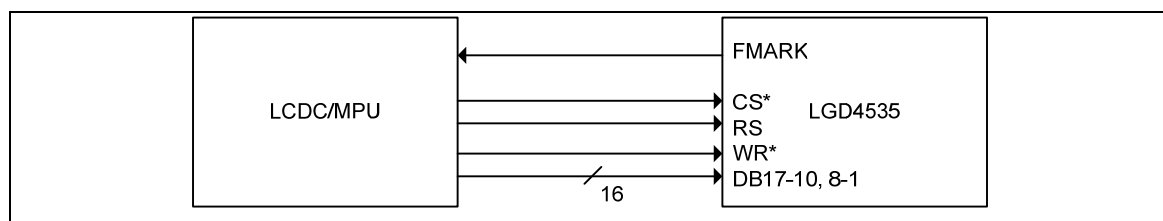
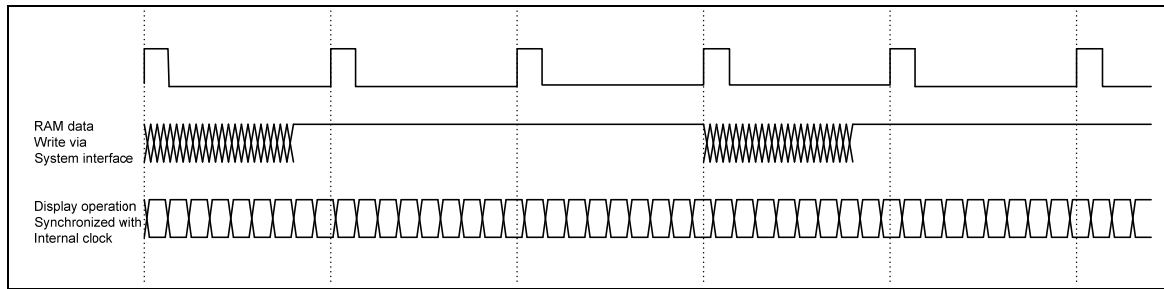


Figure 55 Display synchronous data transfer interface

The LGDP4535 writes display data to the internal GRAM at a speed faster to a certain degree than that of display operation in order to enable a moving picture display via the system interface without flicker. By writing all display data to the internal RAM, only the data to be overwritten in the moving picture RAM area is transferred and the total data transfer for moving picture display can be minimized.



**Figure 56 Moving Picture Data Transfers via FMARK function**

The data transfer operation via FMARK function has a minimum RAM data write speed an internal clock frequency, which must be more than the theoretical values calculated from the following equations

*Internal clock frequency (fosc) [Hz]*

$$= \text{FrameFrequency} \times (\text{DisplayLines(NL)} + \text{FrontPorch(FP)} + \text{BackPorch(BP)}) \times 64(\text{clocks}) \times \text{variance}$$

$$\text{RAMWriteSpeed} > \frac{240 \times \text{DisplayLines (NL)}}{(\text{BackPorch (BP)} + \text{DisplayLines (NL)} - \text{margins}) \times 64 \text{ clocks} \times \frac{1}{f_{osc}}}$$

Note : When RAM write operation is not started right after the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account.

## Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of the RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the LGDP4535 to write data including image data consecutively without taking data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]	
(Horizontal direction)	$8'h00 \leq HSA \leq HEA \leq 8'hEF$
(Vertical direction)	$9'h000 \leq VSA \leq VEA \leq 9'h13F$
[RAM Address setting range]	
(RAM address)	$HSA \leq AD7-0 \leq HEA$
	$VSA \leq AD16-8 \leq VEA$

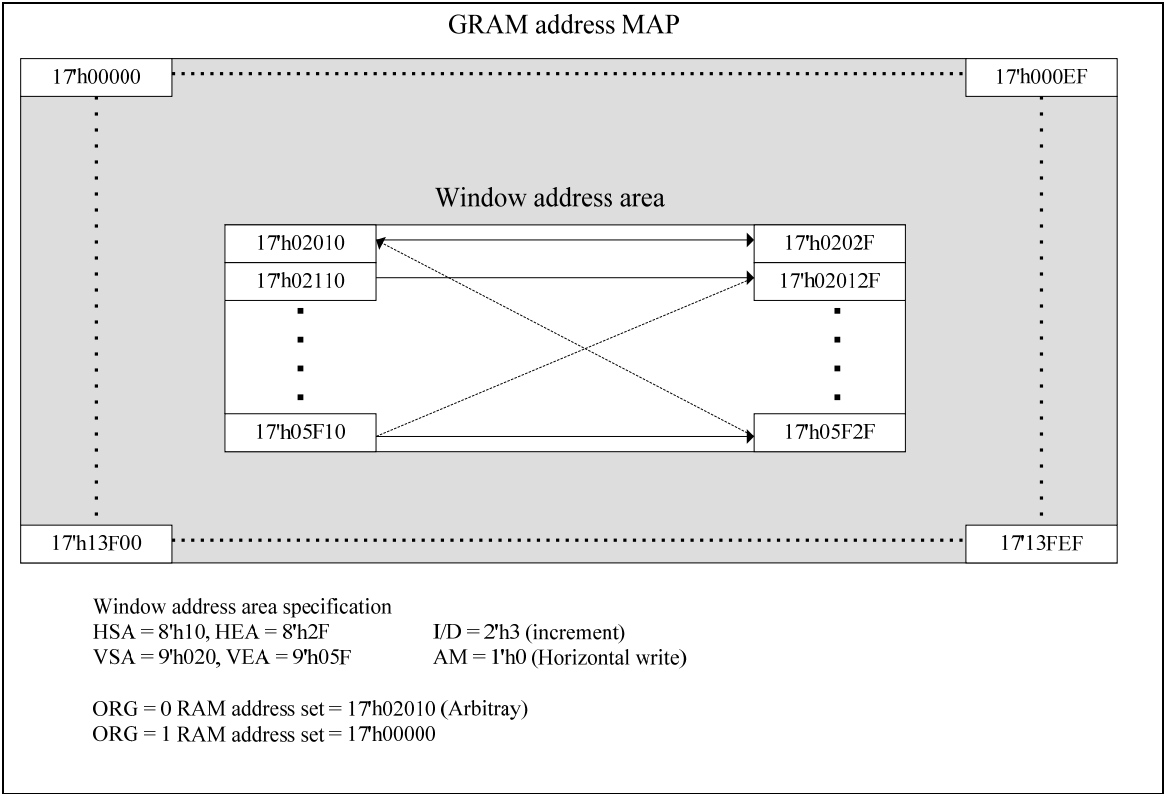


Figure 57 Automatic address update within a Window Address Area

## EPROM Control

LGDP4535 has an embedded EPROM which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32KCV6).

EO01X32KCV6 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32KCV6.

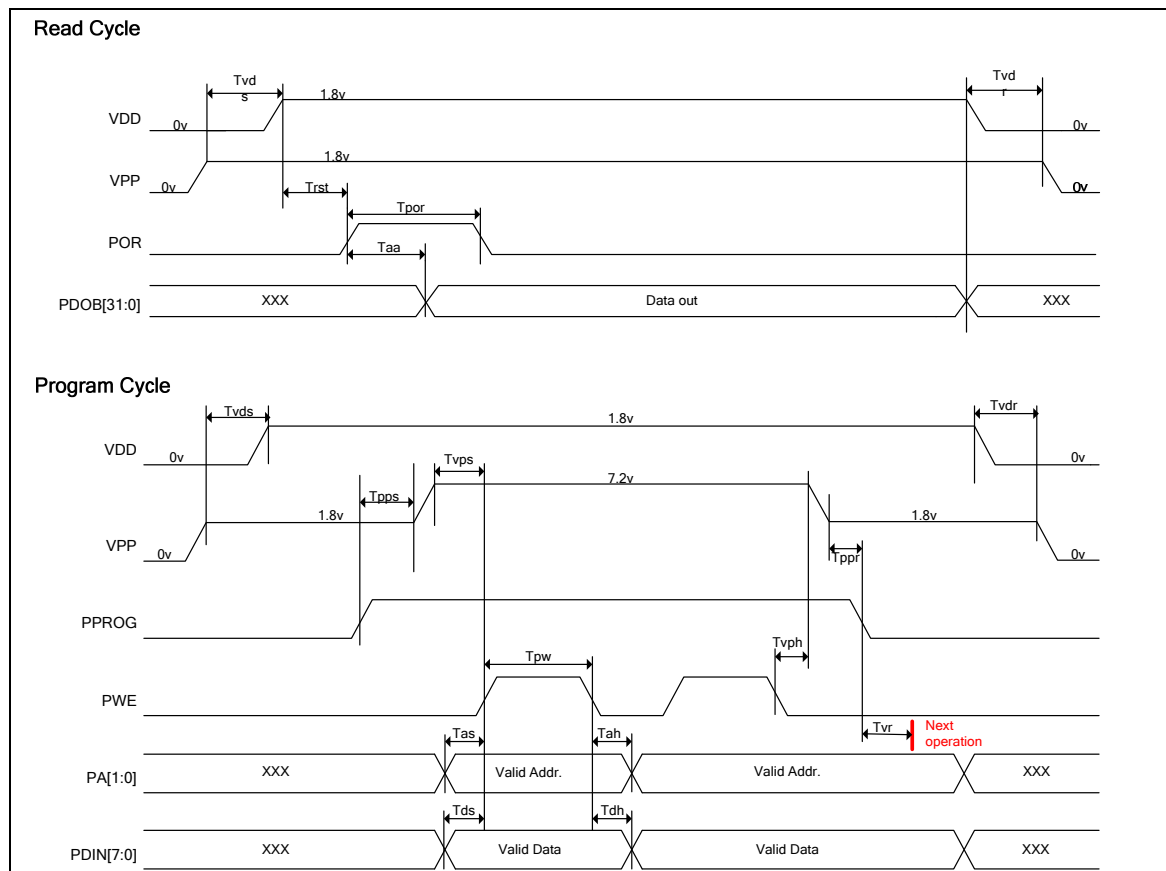
The pins of the embedded EPROM can be controlled using the EPROM control 1 (R60h) register as shown below.

**Table 87**

EO01X32KCV6	Bit fields of register R40h
PTM = 0V/1.8V	PTM[1:0] = 00/11
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.2V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[7:0] = 0V/1.8V	PDIN[7:0] = 0/1

The RA[1:0] of register R41h selects one of four EPROM bytes.

Accessing EPROM control registers, follow the timing requirements of read and program cycles.



**Figure 58 EPROM timings**

**Table 88**

Parameter	Symbol	EO01X32KCV6		Unit
		Min	Max	
Rising Time / Falling Time	$T_r / T_f$	-	1	ns
Data Access Time	$T_{aa}$	-	70	ns
Power-on Pulse Width Time	$T_{por}$	200	-	ns
Address / Data Setup Time	$T_{as} / T_{ds}$	4	-	ns
Address / Data Hold Time	$T_{ah} / T_{dh}$	9	-	ns
External VPP Setup Time	$T_{vps}$	0	-	ns
External VPP Hold Time	$T_{vph}$	0	-	ns
Program Recovery Time	$T_{vr}$	10	-	us
Program Pulse Width	$T_{pw}$	300	350	us
VDD Setup Time	$T_{vds}$	0	-	ms
VDD Recovery Time	$T_{vdr}$	0	-	ms
PPROG Setup Time	$T_{pps}$	10	-	ns
PPROG Recovery Time	$T_{ppr}$	10	-	ns
Power on Read Time	$T_{rst}$	20	-	ns

## Notes

1. All electrical and timing parameters listed above are based on SPICE (or equivalent) simulations and subject to changes after silicon verification.
2. All program signals that align together in the timing diagrams should be derived from the rising clock edge.
3. All timing measurements are from the 50% of the input to 50% of the output.
4. All input waveforms have rising time ( $t_r$ ) and falling time ( $t_f$ ) of 1ns from 10% to 90% of the input waveforms.
5. For capacitive loads greater than 1pF, access time will increase by 1ns per pF of additional loading.
6. Program time means one byte program time in user mode

## Scan Mode Setting

The LGDP4535 allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the LGDP4535 and the LCD panel.

SM	GS	Scan direction	
0	0		G1, G2, G3, G4, ..., G318, G319, G320
0	1		G320, G319, G318, ..., G4, G3, G2, G1
1	0		G1, G3, G5, ..., G317, G319, G2, G4, G6, ..., G318, G320
1	1		G320, G318, G316, ..., G6, G4, G2, G319, G317, G315, ..., G5, G3, G1

Figure 59

## Line Inversion AC Drive

The LGDP4535, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.

In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.

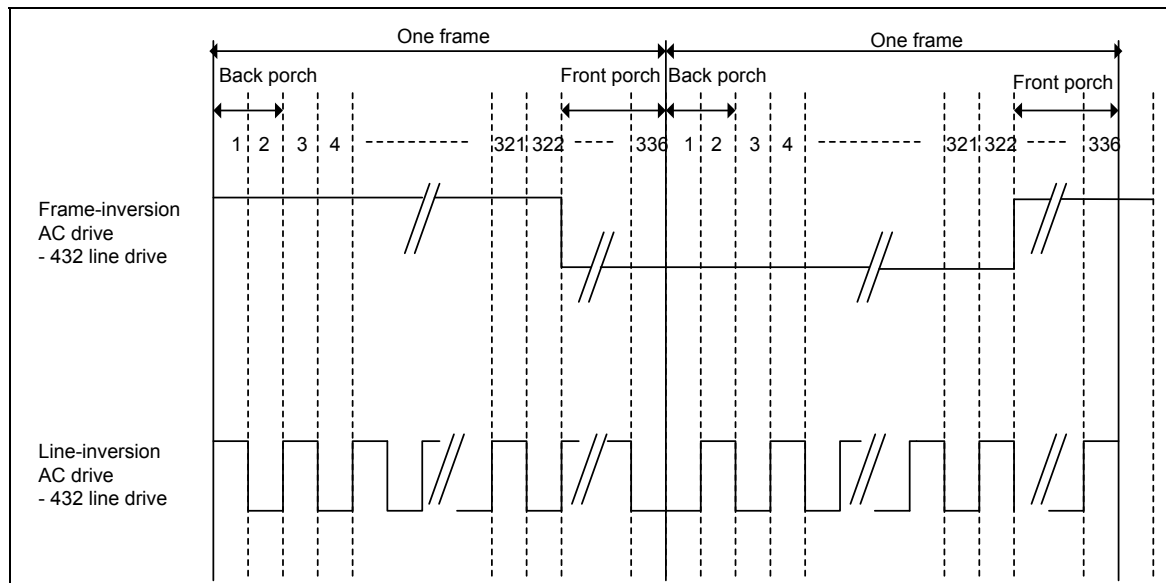


Figure 60 Example of Alternating Signals for n-line Inversion

## Frame-Frequency Adjustment Function

The LGDP4535 supports a function to adjust frame frequency. The frame frequency for driving the LCD can be adjusted by setting the DIVI/E, RTNI/E bits without changing the oscillation frequency.

To switch frame frequencies according to whether displaying a moving picture or displaying a still picture, set a high oscillation frequency in advance. Then, set a low frame frequency to save power consumption when displaying a still picture. When displaying a moving picture, set the frequency high.

### ***Relationship between the liquid crystal Drive Duty and the Frame Frequency***

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be adjusted by setting the 1H period adjustment (RTNI/E) bit and the operation clock division (DIVI/E) bit.

*Equation for calculating frame frequency*

$$\text{Frame Frequency} = \frac{F_{osc}}{\text{Number Of Clocks Per Line} \times \text{Division Ratio} \times (\text{Line} + \text{FP} + \text{BP})}$$

Fosc	: RC oscillation frequency
Number of Clocks per line	: RTNI/E bit
Division Ratio	: DIVI/E bit
Line	: number of lines to drive the LCD (NL bit)
FP	: Number of lines for front porch
BP	: Number of lines for back porch

#### **Example of Calculation : when maximum frame frequency = 70Hz**

Number of lines : 320 lines  
 1H period : 60 Clock cycles (RTNI/E[7:0] = "00111100")  
 Division ratio of operating clock : 1/1  
 Front porch : 2 lines  
 Back porch : 14 lines

$$F_{osc} = 70 \text{ (Hz)} \times 60 \text{ (clocks)} \times 1/1 \times (320 + 2 + 14) \text{ (Lines)} = 1.41 \text{ (MHz)}$$

In this case, the RC oscillation frequency is to set to 1.41MHz. Adjust the value of the external resistor connected to the RC oscillator so that RC oscillation frequency becomes 1.41MHz.



## Partial Display Function

The partial display function allows the LGDP4535 to drive lines selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven with non-display level to reduce power consumption.

The power saving effect can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

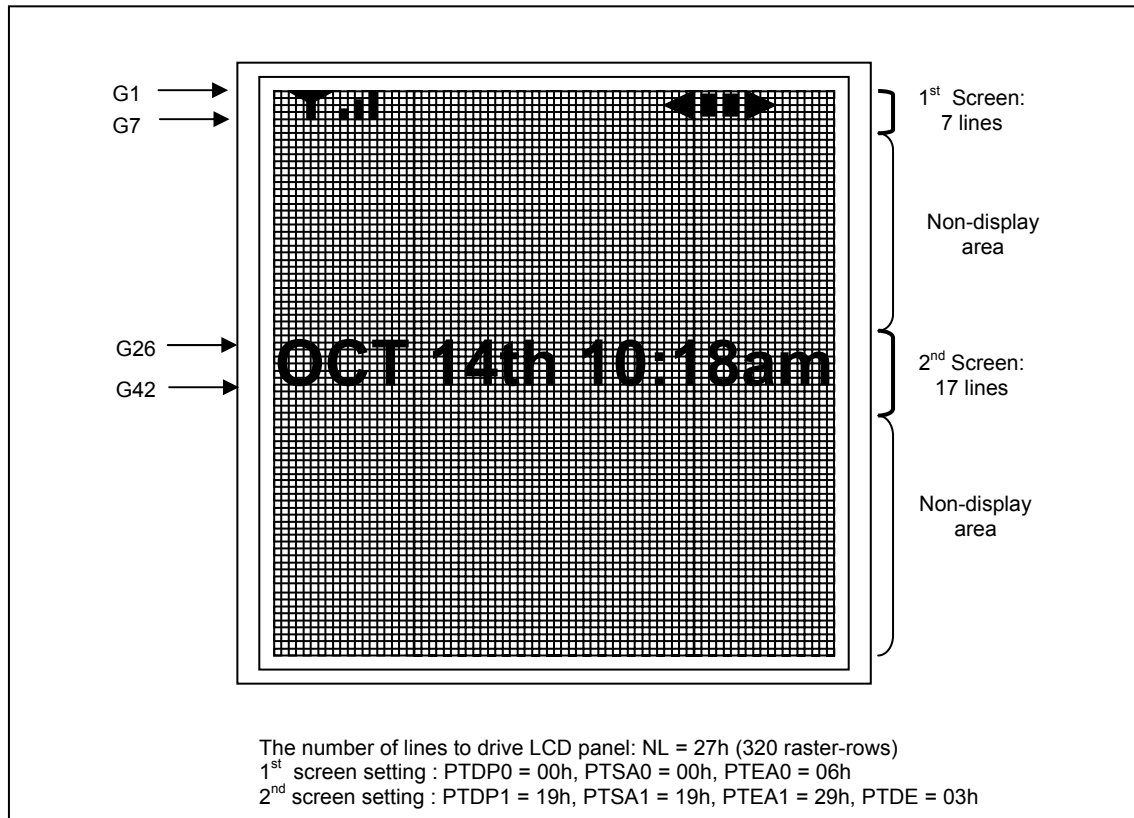


Figure 61

# Liquid crystal panel interface timing

The relationships between RGB interface signals and liquid crystal panel control signals in interhal operation and RGB interface operations are as follows.

## Internal clock operation

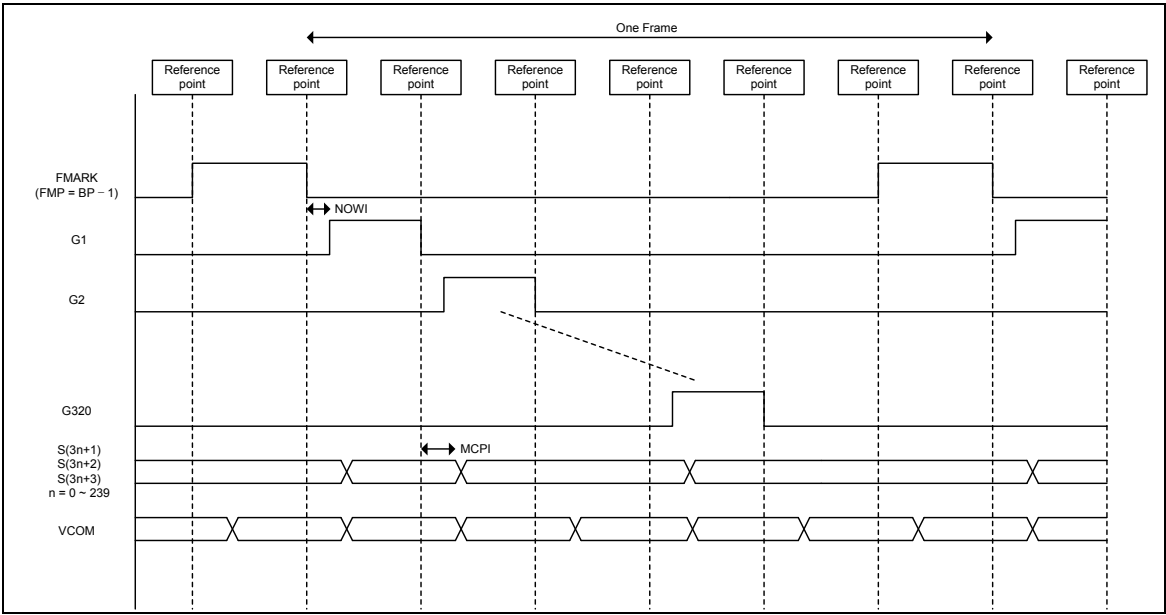


Figure 62

RGB Interface operation

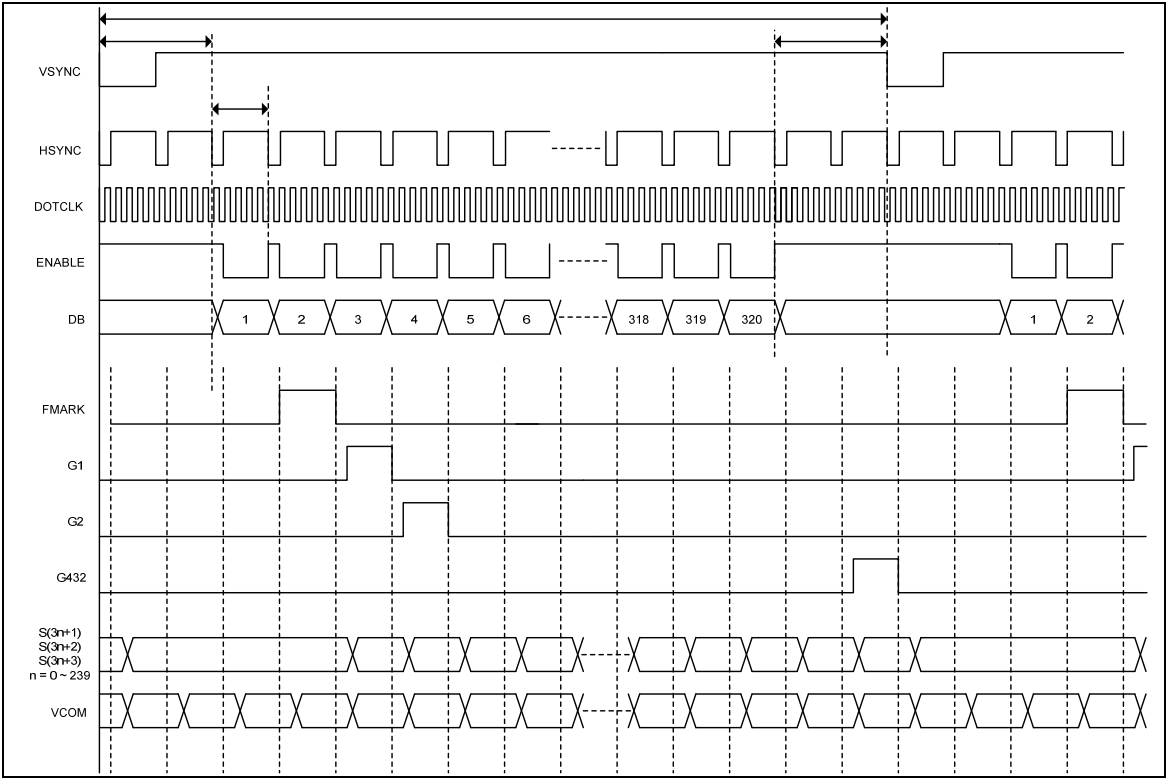


Figure 63

## $\gamma$ -Correction Function

The LGDP4535 has the  $\gamma$ -correction function to display in 262,144 colors simultaneously. The  $\gamma$ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LGDP4535 available with liquid crystal panels of various characteristics.

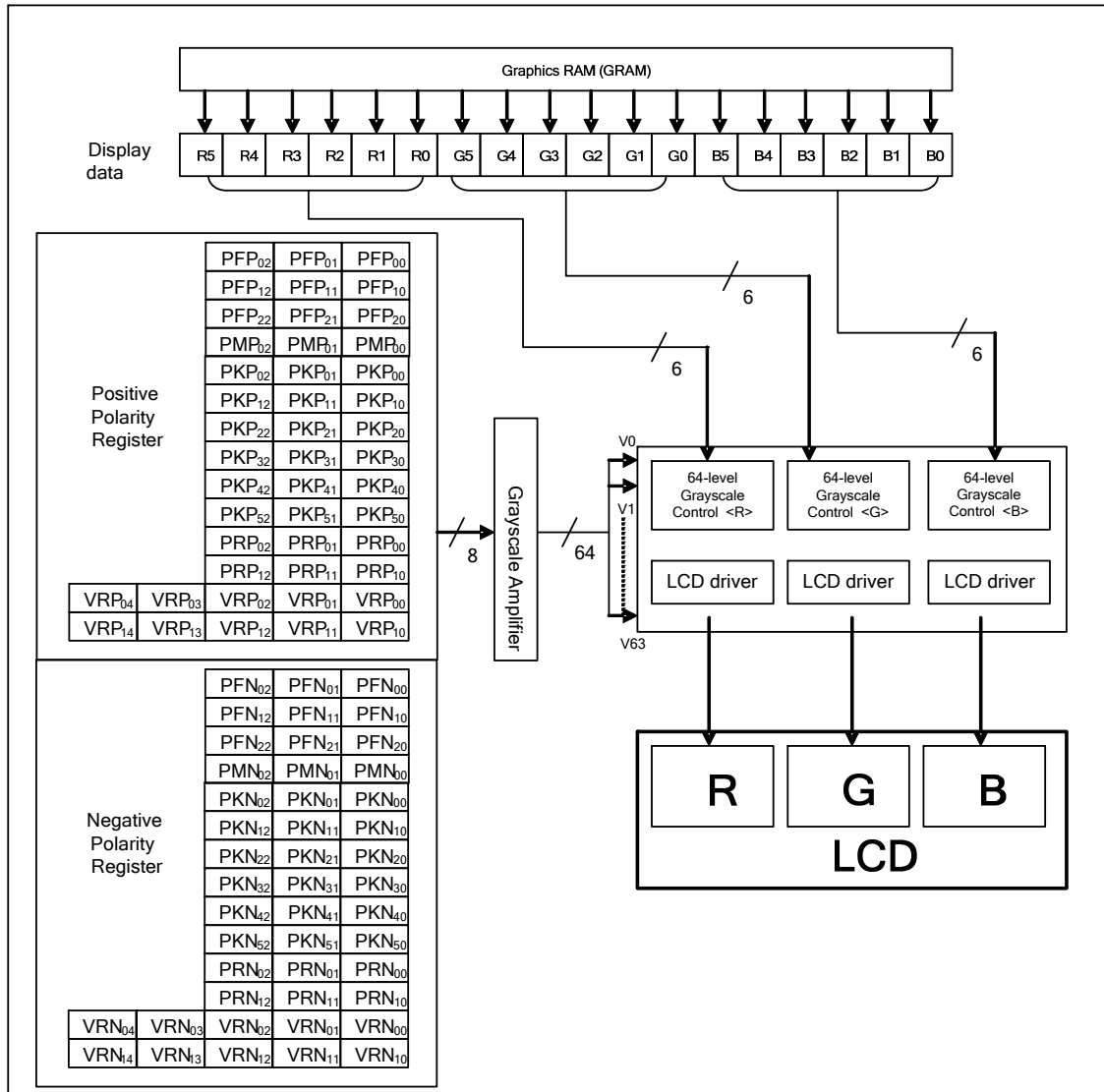


Figure 64 Grayscale control

## Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LGDP4535.

To generate 64 grayscale voltages (V0 to V63), the LGDP4535 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

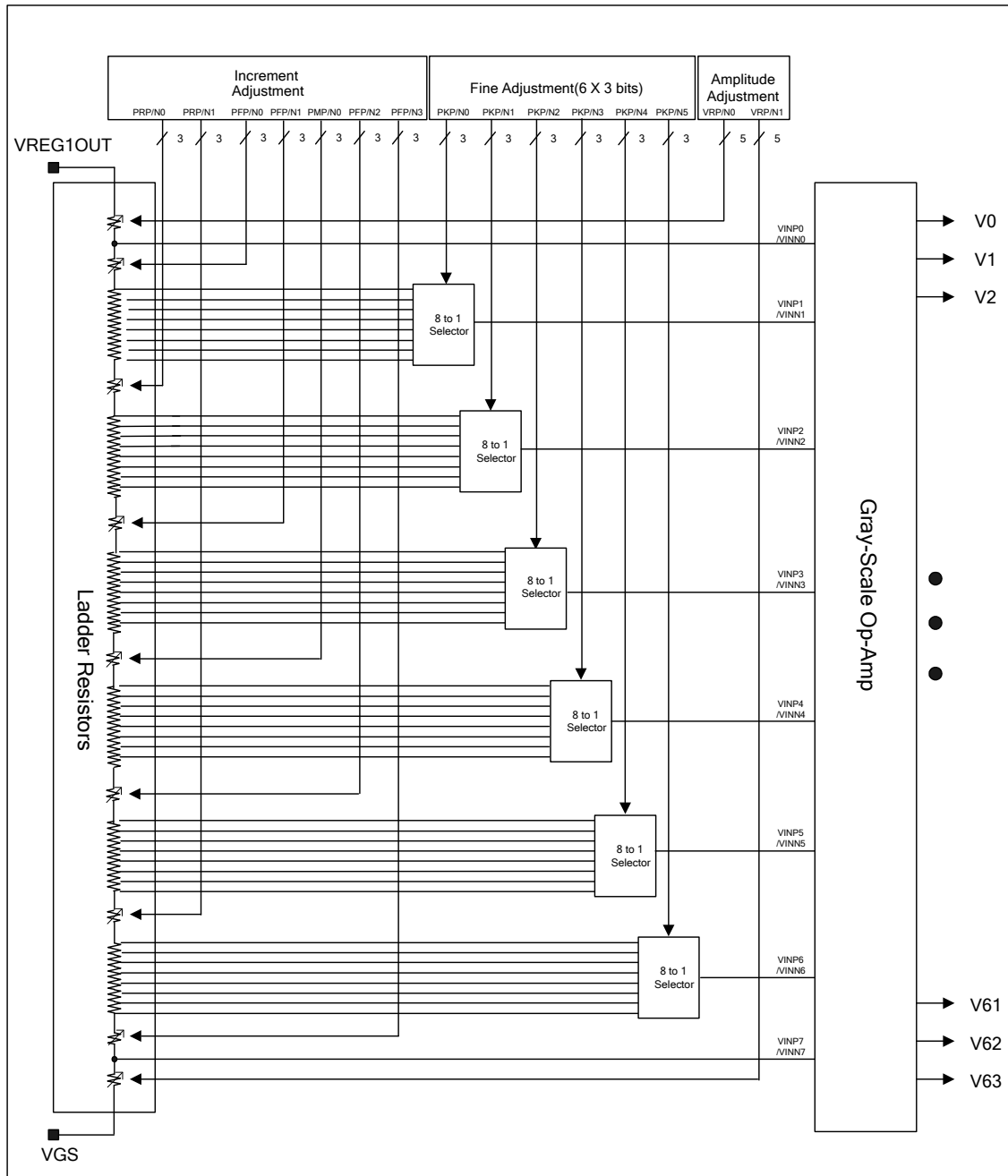


Figure 65 Grayscale amplifier unit

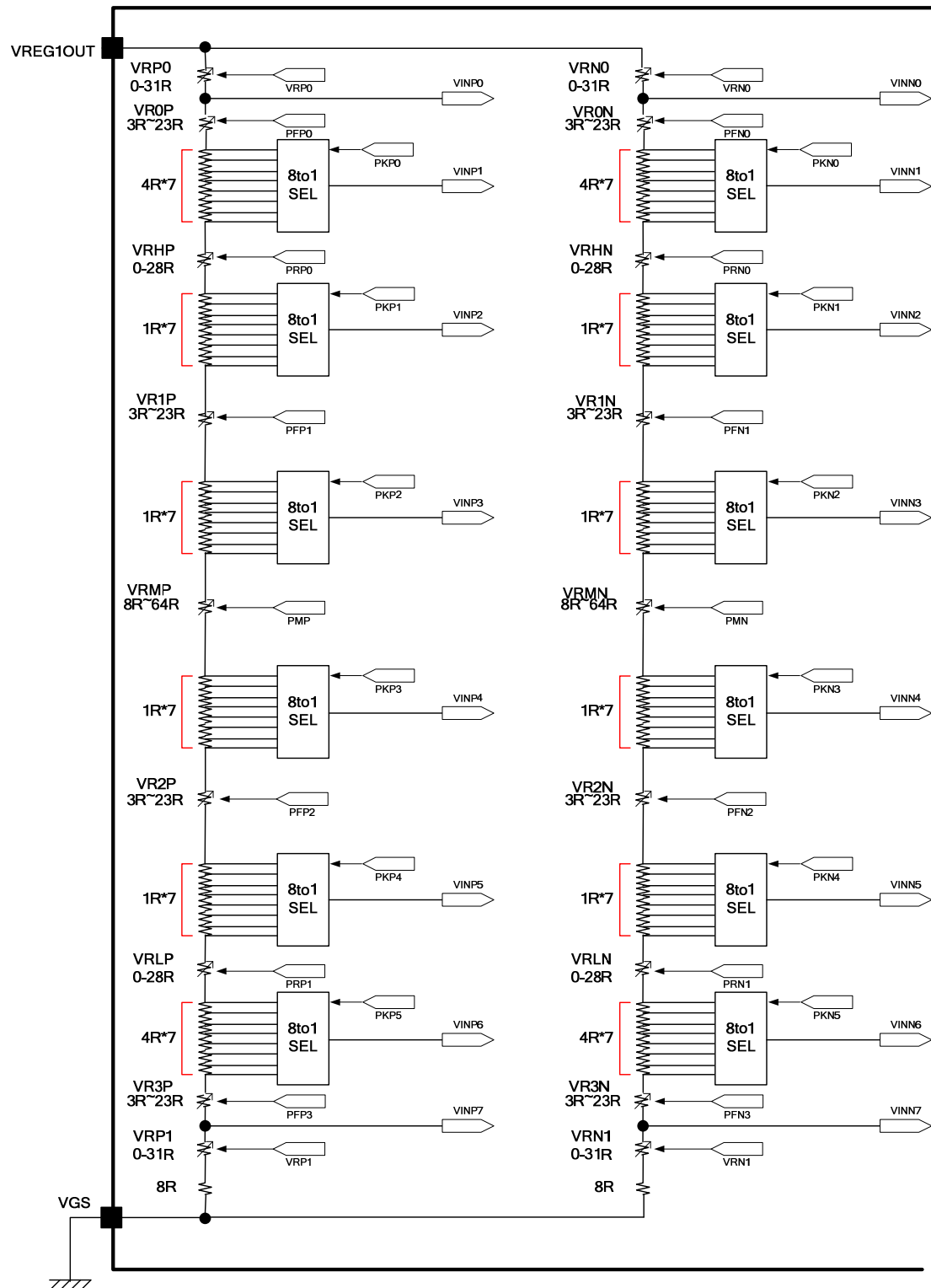
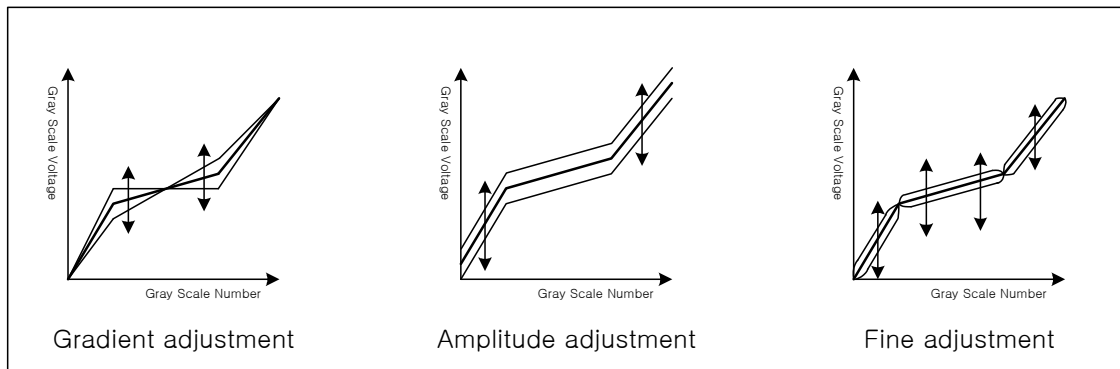


Figure 66 Ladder resistor units and 8-to-1 selectors

## ***$\gamma$ -Correction Register***

The  $\gamma$ -correction registers of the LGDP4535 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for  $\gamma$ -characteristics of a liquid crystal panel. These  $\gamma$ -correction register settings and the reference levels of the 64 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.



**Figure 67**

### **1. Gradient adjustment registers**

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

### **2. Amplitude adjustment registers**

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

### **3. Fine adjustment registers**

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

**Table 89 List of registers**

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
	PFP0[2:0]	PFN0[2:0]	Variable resistor VR0P(N)
	PFP1[2:0]	PFN1[2:0]	Variable resistor VR1P(N)
	PFP2[2:0]	PFN2[2:0]	Variable resistor VR2P(N)
	PFP3[2:0]	PFN3[2:0]	Variable resistor VR3P(N)
	PMP[2:0]	PMN[2:0]	Variable resistor VRMP(N)
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector ( voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector ( voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector ( voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector ( voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector ( voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector ( voltage level of grayscale 62)

## Ladder Resistors and 8-to-1 Selector

### Block Configuration

The reference voltage generating unit as illustrated in figure 66 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the  $\gamma$ -correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

### Variable Resistors

The LGDP4535 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)/VR0~4P(N)/VRMP(N)) and amplitude adjustment (VRP(N)0~1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

**Table 90 Gradient adjustment**

Contents of register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)	Contents of register PFP(N)0/1/2/3[2:0]	Resistance VR0/1P(N) VR2/3P(N)	Contents of register PMP(N)[2:0]	Resistance VRMP(N)
000	0R	000	3R	000	8R
001	4R	001	5R	001	16R
010	8R	010	9R	010	24R
011	12R	011	11R	011	32R
100	16R	100	15R	100	40R
101	20R	101	17R	101	48R
110	24R	110	21R	110	56R
111	28R	111	23R	111	64R



**Table 91 Amplitude adjustment**

Contents of register VRP(N)0[4:0]	Resistance VRP(N)0 VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

## 8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N)6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

**Table 92 Fine adjustment registers and selected voltage**

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
3'h0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
3'h1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
3'h2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3'h3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
3'h4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
3'h5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
3'h6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
3'h7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formula.

**Table 93 Formula for calculating voltage (1)**

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	$VREG1OUT - \Delta V * VRP0 / SUMRP$	-	VINP0
KVP1	$VREG1OUT - \Delta V * (VRP0 + VR0P + 0R) / SUMRP$	PKP0= 3'h0	VINP1
KVP2	$VREG1OUT - \Delta V * (VRP0 + VR0P + 4R) / SUMRP$	PKP0= 3'h1	
KVP3	$VREG1OUT - \Delta V * (VRP0 + VR0P + 8R) / SUMRP$	PKP0= 3'h2	
KVP4	$VREG1OUT - \Delta V * (VRP0 + VR0P + 12R) / SUMRP$	PKP0= 3'h3	
KVP5	$VREG1OUT - \Delta V * (VRP0 + VR0P + 16R) / SUMRP$	PKP0= 3'h4	
KVP6	$VREG1OUT - \Delta V * (VRP0 + VR0P + 20R) / SUMRP$	PKP0= 3'h5	
KVP7	$VREG1OUT - \Delta V * (VRP0 + VR0P + 24R) / SUMRP$	PKP0= 3'h6	
KVP8	$VREG1OUT - \Delta V * (VRP0 + VR0P + 28R) / SUMRP$	PKP0= 3'h7	VINP2
KVP9	$VREG1OUT - \Delta V * (VRP0 + VR0P + 28R + VRHP) / SUMRP$	PKP1= 3'h0	
KVP10	$VREG1OUT - \Delta V * (VRP0 + VR0P + 29R + VRHP) / SUMRP$	PKP1= 3'h1	
KVP11	$VREG1OUT - \Delta V * (VRP0 + VR0P + 30R + VRHP) / SUMRP$	PKP1= 3'h2	
KVP12	$VREG1OUT - \Delta V * (VRP0 + VR0P + 31R + VRHP) / SUMRP$	PKP1= 3'h3	
KVP13	$VREG1OUT - \Delta V * (VRP0 + VR0P + 32R + VRHP) / SUMRP$	PKP1= 3'h4	
KVP14	$VREG1OUT - \Delta V * (VRP0 + VR0P + 33R + VRHP) / SUMRP$	PKP1= 3'h5	
KVP15	$VREG1OUT - \Delta V * (VRP0 + VR0P + 34R + VRHP) / SUMRP$	PKP1= 3'h6	VINP3
KVP16	$VREG1OUT - \Delta V * (VRP0 + VR0P + 35R + VRHP) / SUMRP$	PKP1= 3'h7	
KVP17	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 35R + VRHP) / SUMRP$	PKP2= 3'h0	
KVP18	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 36R + VRHP) / SUMRP$	PKP2= 3'h1	
KVP19	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 37R + VRHP) / SUMRP$	PKP2= 3'h2	
KVP20	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 38R + VRHP) / SUMRP$	PKP2= 3'h3	
KVP21	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 39R + VRHP) / SUMRP$	PKP2= 3'h4	
KVP22	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 40R + VRHP) / SUMRP$	PKP2= 3'h5	VINP4
KVP23	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 41R + VRHP) / SUMRP$	PKP2= 3'h6	
KVP24	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 42R + VRHP) / SUMRP$	PKP2= 3'h7	
KVP25	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 42R + VRHP + VRMP) / SUMRP$	PKP3= 3'h0	
KVP26	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 43R + VRHP + VRMP) / SUMRP$	PKP3= 3'h1	
KVP27	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 44R + VRHP + VRMP) / SUMRP$	PKP3= 3'h2	
KVP28	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 45R + VRHP + VRMP) / SUMRP$	PKP3= 3'h3	
KVP29	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 46R + VRHP + VRMP) / SUMRP$	PKP3= 3'h4	VINP5
KVP30	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 47R + VRHP + VRMP) / SUMRP$	PKP3= 3'h5	
KVP31	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 48R + VRHP + VRMP) / SUMRP$	PKP3= 3'h6	
KVP32	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1P + 49R + VRHP + VRMP) / SUMRP$	PKP3= 3'h7	
KVP33	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 49R + VRHP + VRMP) / SUMRP$	PKP4= 3'h0	
KVP34	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 50R + VRHP + VRMP) / SUMRP$	PKP4= 3'h1	
KVP35	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 51R + VRHP + VRMP) / SUMRP$	PKP4= 3'h2	
KVP36	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 52R + VRHP + VRMP) / SUMRP$	PKP4= 3'h3	VINP6
KVP37	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 53R + VRHP + VRMP) / SUMRP$	PKP4= 3'h4	
KVP38	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 54R + VRHP + VRMP) / SUMRP$	PKP4= 3'h5	
KVP39	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 55R + VRHP + VRMP) / SUMRP$	PKP4= 3'h6	
KVP40	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 56R + VRHP + VRMP) / SUMRP$	PKP4= 3'h7	
KVP41	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 56R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h0	
KVP42	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 60R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h1	
KVP43	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 64R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h2	
KVP44	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 68R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h3	
KVP45	$VREG1OUT - \Delta V * (VRP0 + VR0 / 1/2P + 72R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h4	

KVP46	$VREG1OUT - \Delta V \cdot (VRP0 + VR0/1/2P + 76R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h5	
KVP47	$VREG1OUT - \Delta V \cdot (VRP0 + VR0/1/2P + 80R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h6	
KVP48	$VREG1OUT - \Delta V \cdot (VRP0 + VR0/1/2P + 84R + VRHP + VRMP + VRLP) / SUMRP$	PKP5= 3'h7	
KVP49	$VREG1OUT - \Delta V \cdot (VRP0 + VR0/1/2/3P + 84R + VRHP + VRMP + VRLP) / SUMRP$	-	VINP7

SUMRP: Sum of positive ladder resistors =  $92R + VRHP + VRLP + VRP0 + VRP1 + VR0P + VR1P + VR2P + VR3P + VRMP$

$\Delta V$  : Difference in electrical potential between VREG1OUT and VGS

**Table 94 Formula for calculating voltage (2)**

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	$VINP4 + (VINP3 - VINP4) \cdot (11/23)$
V1	VINP1	V33	$VINP4 + (VINP3 - VINP4) \cdot (10/23)$
V2	$VINP2 + (VINP1 - VINP2) \cdot (30/48)$	V34	$VINP4 + (VINP3 - VINP4) \cdot (9/23)$
V3	$VINP2 + (VINP1 - VINP2) \cdot (23/48)$	V35	$VINP4 + (VINP3 - VINP4) \cdot (8/23)$
V4	$VINP2 + (VINP1 - VINP2) \cdot (16/48)$	V36	$VINP4 + (VINP3 - VINP4) \cdot (7/23)$
V5	$VINP2 + (VINP1 - VINP2) \cdot (12/48)$	V37	$VINP4 + (VINP3 - VINP4) \cdot (6/23)$
V6	$VINP2 + (VINP1 - VINP2) \cdot (8/48)$	V38	$VINP4 + (VINP3 - VINP4) \cdot (5/23)$
V7	$VINP2 + (VINP1 - VINP2) \cdot (4/48)$	V39	$VINP4 + (VINP3 - VINP4) \cdot (4/23)$
V8	VINP2	V40	$VINP4 + (VINP3 - VINP4) \cdot (3/23)$
V9	$VINP3 + (VINP2 - VINP3) \cdot (22/24)$	V41	$VINP4 + (VINP3 - VINP4) \cdot (2/23)$
V10	$VINP3 + (VINP2 - VINP3) \cdot (20/24)$	V42	$VINP4 + (VINP3 - VINP4) \cdot (1/23)$
V11	$VINP3 + (VINP2 - VINP3) \cdot (18/24)$	V43	VINP4
V12	$VINP3 + (VINP2 - VINP3) \cdot (16/24)$	V44	$VINP5 + (VINP4 - VINP5) \cdot (22/24)$
V13	$VINP3 + (VINP2 - VINP3) \cdot (14/24)$	V45	$VINP5 + (VINP4 - VINP5) \cdot (20/24)$
V14	$VINP3 + (VINP2 - VINP3) \cdot (12/24)$	V46	$VINP5 + (VINP4 - VINP5) \cdot (18/24)$
V15	$VINP3 + (VINP2 - VINP3) \cdot (10/24)$	V47	$VINP5 + (VINP4 - VINP5) \cdot (16/24)$
V16	$VINP3 + (VINP2 - VINP3) \cdot (8/24)$	V48	$VINP5 + (VINP4 - VINP5) \cdot (14/24)$
V17	$VINP3 + (VINP2 - VINP3) \cdot (6/24)$	V49	$VINP5 + (VINP4 - VINP5) \cdot (12/24)$
V18	$VINP3 + (VINP2 - VINP3) \cdot (4/24)$	V50	$VINP5 + (VINP4 - VINP5) \cdot (10/24)$
V19	$VINP3 + (VINP2 - VINP3) \cdot (2/24)$	V51	$VINP5 + (VINP4 - VINP5) \cdot (8/24)$
V20	VINP3	V52	$VINP5 + (VINP4 - VINP5) \cdot (6/24)$
V21	$VINP4 + (VINP3 - VINP4) \cdot (22/23)$	V53	$VINP5 + (VINP4 - VINP5) \cdot (4/24)$
V22	$VINP4 + (VINP3 - VINP4) \cdot (21/23)$	V54	$VINP5 + (VINP4 - VINP5) \cdot (2/24)$
V23	$VINP4 + (VINP3 - VINP4) \cdot (20/23)$	V55	VINP5
V24	$VINP4 + (VINP3 - VINP4) \cdot (19/23)$	V56	$VINP6 + (VINP5 - VINP6) \cdot (44/48)$
V25	$VINP4 + (VINP3 - VINP4) \cdot (18/23)$	V57	$VINP6 + (VINP5 - VINP6) \cdot (40/48)$
V26	$VINP4 + (VINP3 - VINP4) \cdot (17/23)$	V58	$VINP6 + (VINP5 - VINP6) \cdot (36/48)$
V27	$VINP4 + (VINP3 - VINP4) \cdot (16/23)$	V59	$VINP6 + (VINP5 - VINP6) \cdot (32/48)$
V28	$VINP4 + (VINP3 - VINP4) \cdot (15/23)$	V60	$VINP6 + (VINP5 - VINP6) \cdot (25/48)$
V29	$VINP4 + (VINP3 - VINP4) \cdot (14/23)$	V61	$VINP6 + (VINP5 - VINP6) \cdot (18/48)$
V30	$VINP4 + (VINP3 - VINP4) \cdot (13/23)$	V62	VINP6
V31	$VINP4 + (VINP3 - VINP4) \cdot (12/23)$	V63	VINP7

Note: Make sure DDVDH-V0 > 0.5V

Relationship between RAM Data and Voltage Output Levels  
The relationship between RAM data and source output voltage levels is as follows..

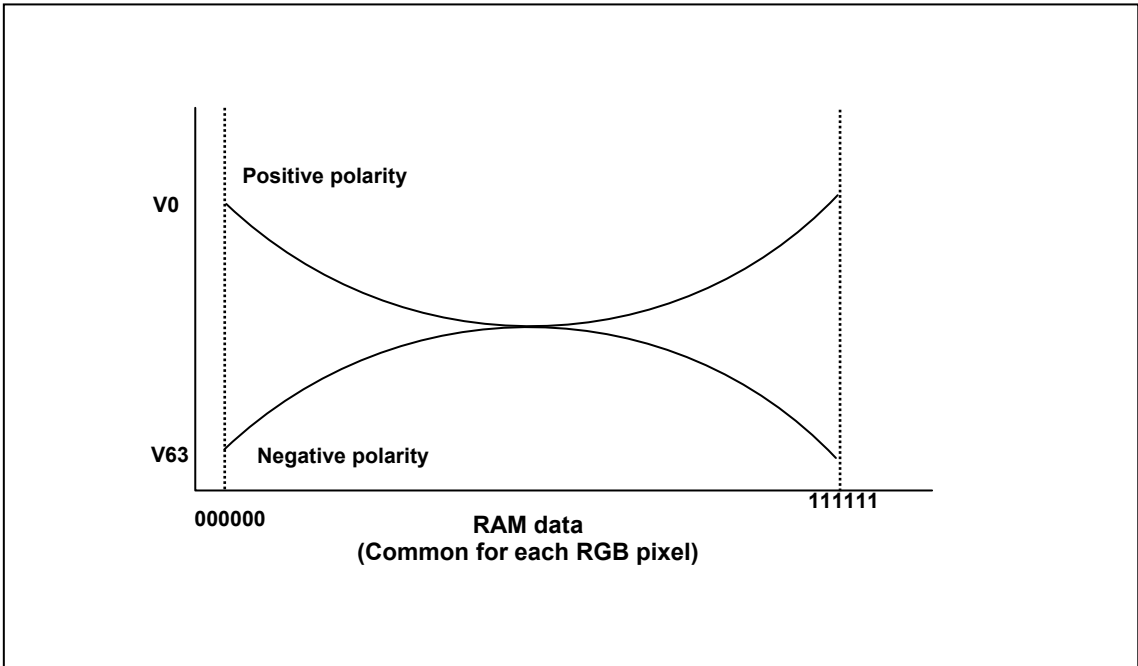


Figure 68 RAM data and the output voltage (REV = “1”)

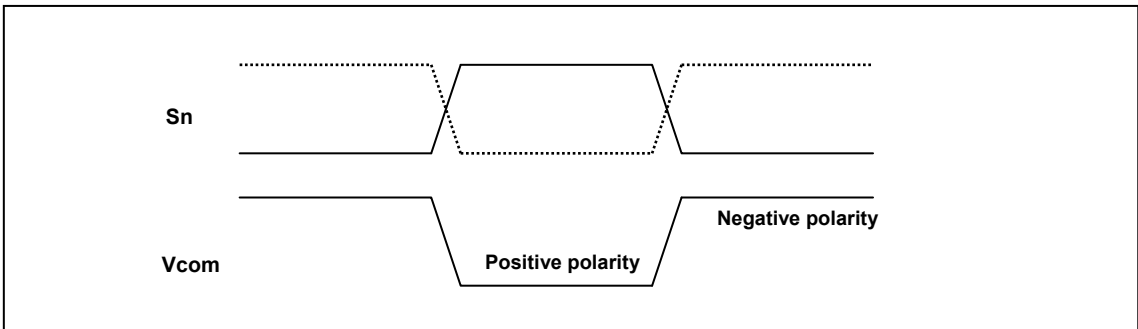


Figure 69 Source output and Vcom

## 8-Color Display Mode

The LGDP4535 has a function to display in 8colors. In 8-color mode, available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1 to V62) are halted to reduce power consumption.

In 8-color display mode, the MSBs of the respective dot data (R5, G5, B5) are written to the rest of the dot data in order to display in 8 colors without rewriting the RAM data.

The  $\gamma$ - correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.

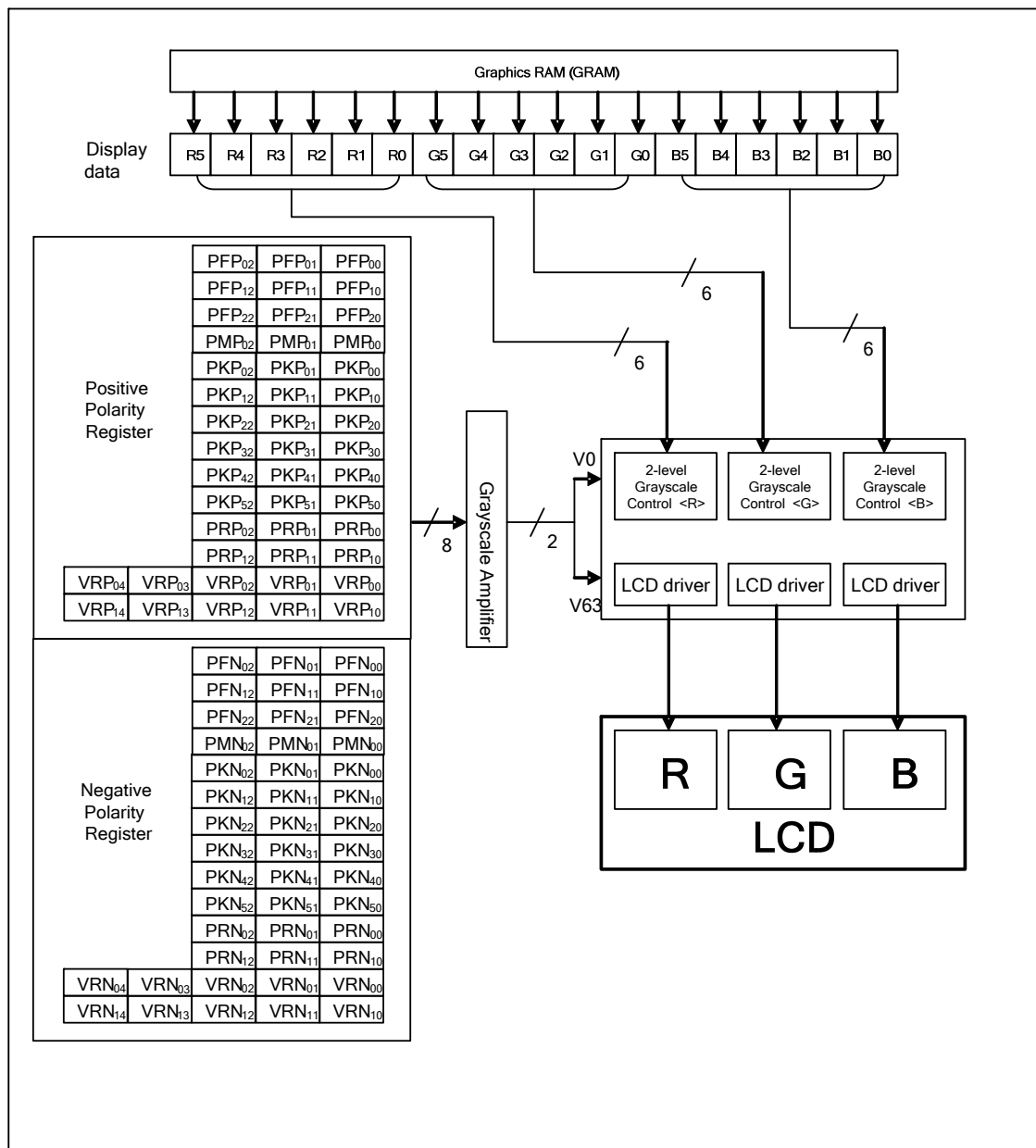


Figure 70 8-color display mode

To switch between the 262,144-color mode and 8-color mode, follow the sequence below.

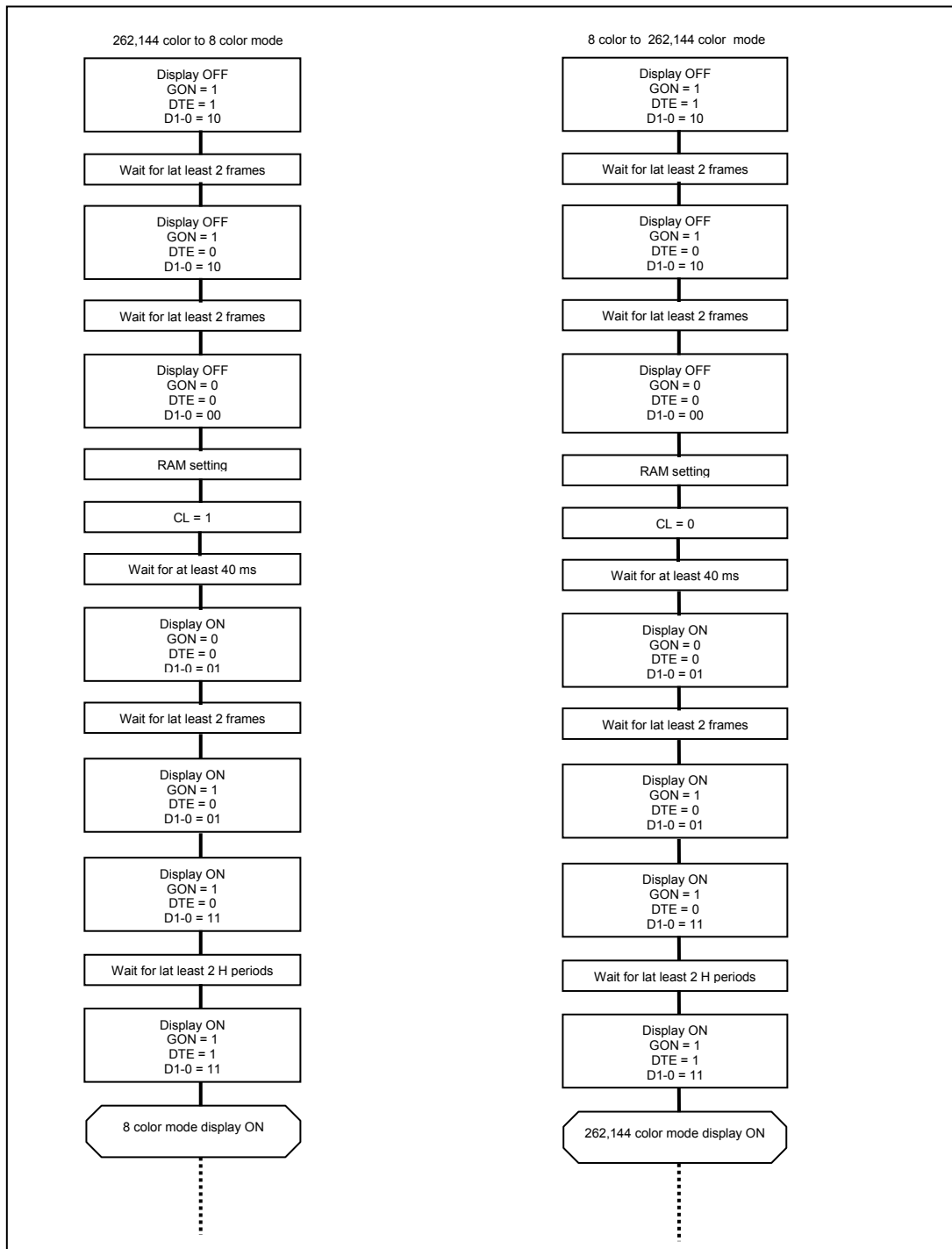


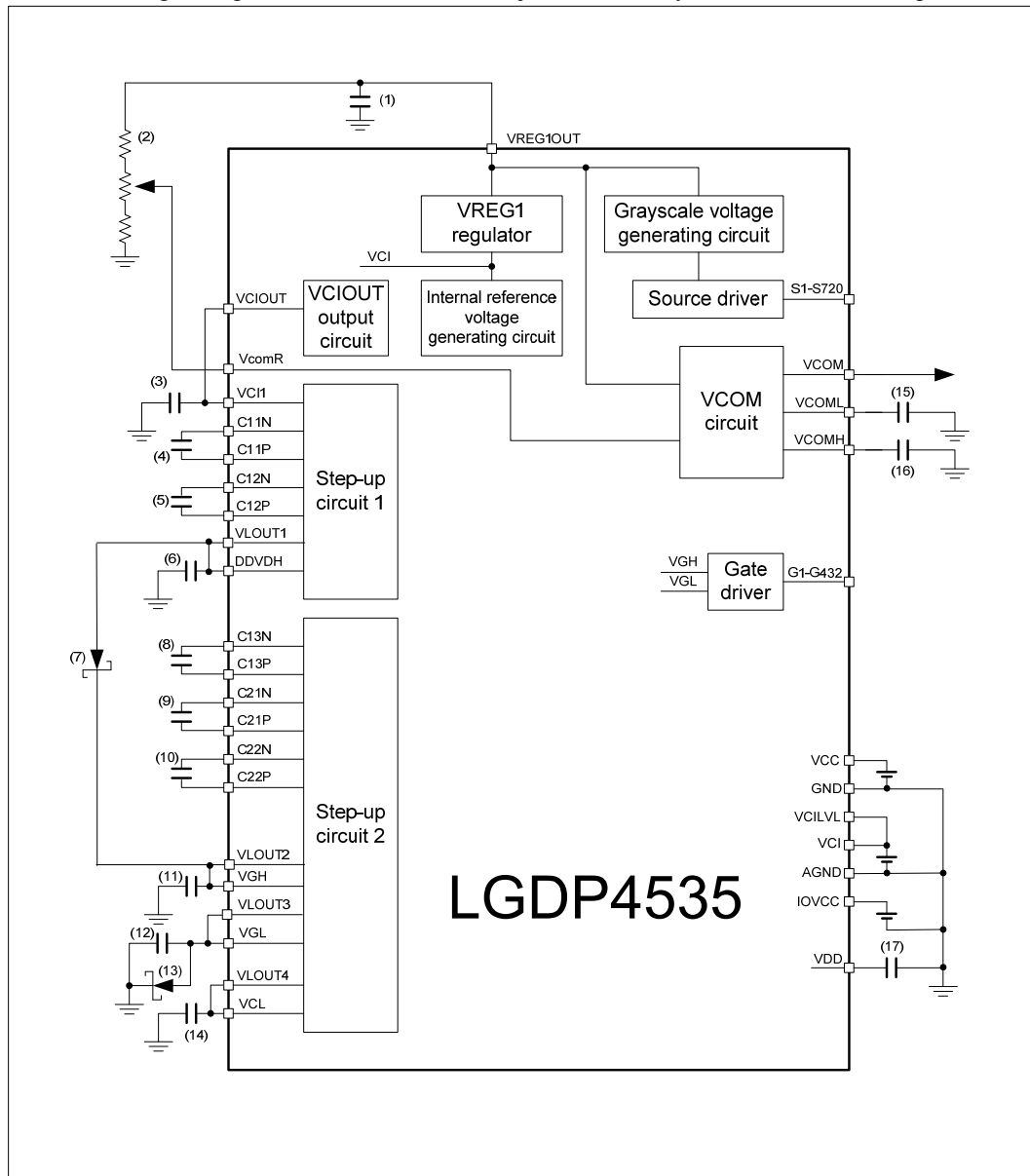
Figure 71

## Power-supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the LGDP4535.

### Power supply circuit connection example 1 ( $V_{ci1} = V_{ciOUT}$ )

In the following example, the VciOUT level is adjusted internally with the VciOUT output circuit.

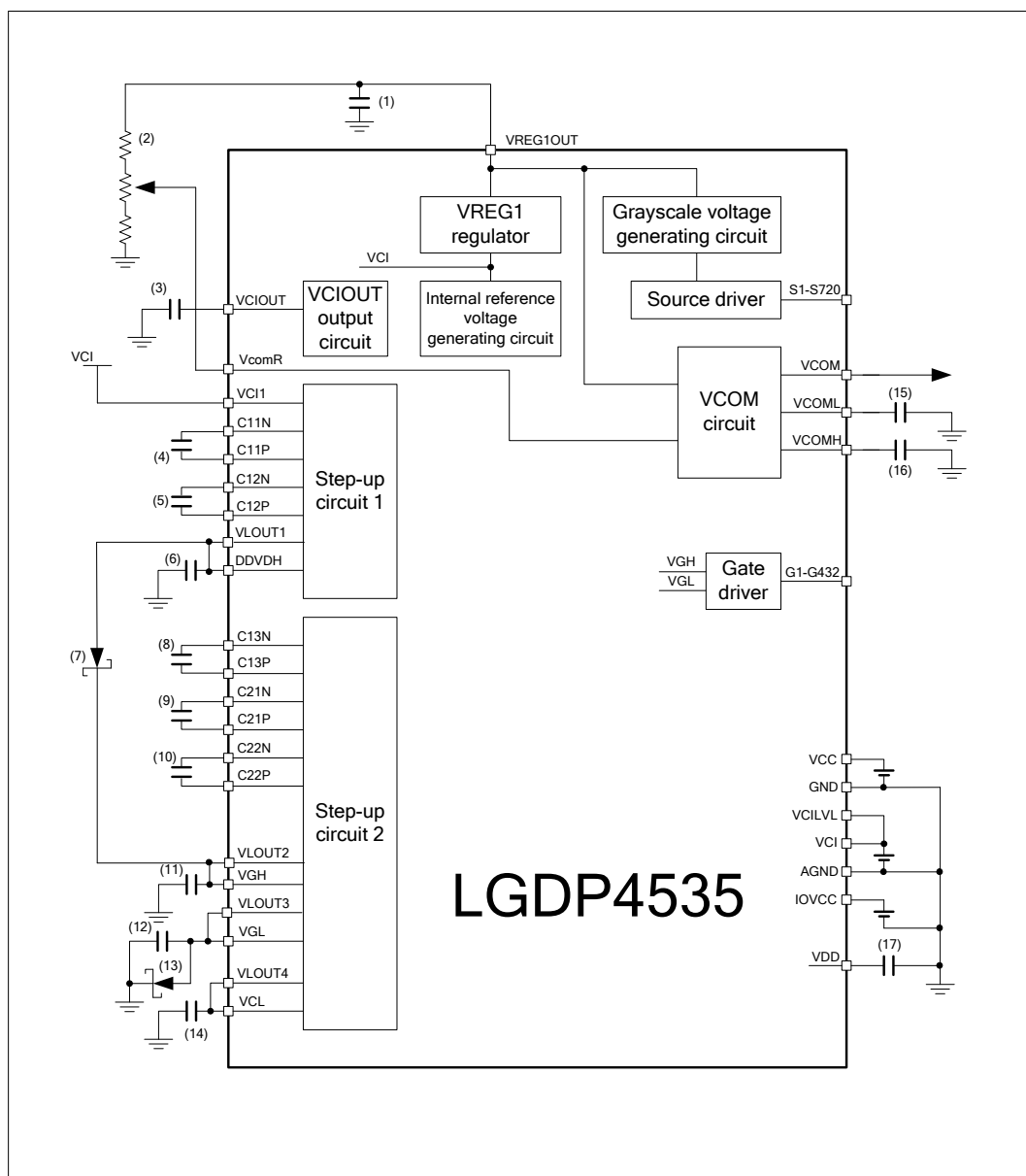


**Figure 72**

Note: The wiring resistance between the schottky diode and GND/VGL must be 10-Ohm or less.

**Power supply circuit connection example2 ( $V_{ci1} = V_{ci}$  direct input)**

In the following example, the electrical Vci is directly applied to Vci1. In this case, the VciOUT level cannot be adjusted internally but step-up operation becomes more effective



**Figure 73**

Note: 1. The wiring resistance between the schottky diode and GND/VGL must be 10-Ohm or less.

2. When directly applying the  $V_{ci}$  level to  $V_{ci1}$ , set  $VC=3'h0$ .



## Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the LGDP4535 are as follows.

**Table 95 Capacitor**

Capacitance	Voltage proof	Pin Connection
1 $\mu$ F (B characteristics)	6V	(1)VREG1OUT, (3)VciOUT, (4) C11N/P, (5) C12N/P, (8) C13N/P, (14) VLOUT4, (15) VCOML, (16) VCOMH, (17) VDD
	10V	(6) VLOUT1, (9) C21N/P, (10) C22N/P
	25V	(11) VLOUT2, (12) VLOUT3

Notes: 1. Check with the LC module.

2. The numbers in the parentheses corresponds to the numbers of the elements in Figure 72, Figure 73.

**Table 96 Schottky Diode**

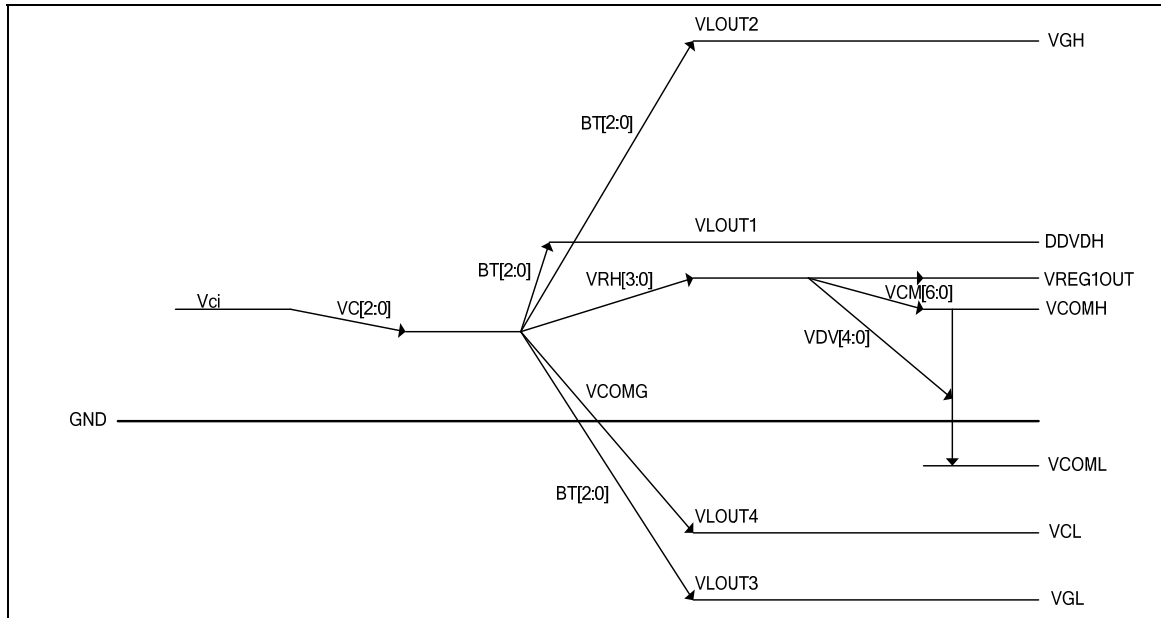
Specification	Pin Connection
$V_F < 0.4 \text{ V}/20 \text{ mA}@25^\circ\text{C}$ , $V_R \geq 30\text{V}$	(7) DDVDH-VGH (13) GND-VGL

**Table 97 Variable Resistor**

Specification	Pin Connection
$>200\text{k}\Omega$	(2) VcomR

## Voltage Setting Pattern Diagram

The pattern diagram of voltage setting and waveforms of the liquid crystal application voltages are as follows.



**Figure 74 Pattern Diagram for Voltage Setting**

**Note** Output voltages of DDVDH, VGH, VGL, and VCL drop from setting voltage(idea voltage) depending on the current consumption at output.  $(DDVDH - VREG1OUT) > 0.5V$  and  $(VCOML - VGL) > 0.5V$  are the relation to the actual voltage. When using the voltage in the large current consumption at the fast VCOM2 cycle( such as line-by-line inversion), check the voltage value

## Power Supply Instruction Setting

The followings are the sequences for setting power supply ON/OFF. Make power supply ON/OFF settings according to the following sequences in Display ON/OFF, Standby set/exit, Sleep set/exit sequences.

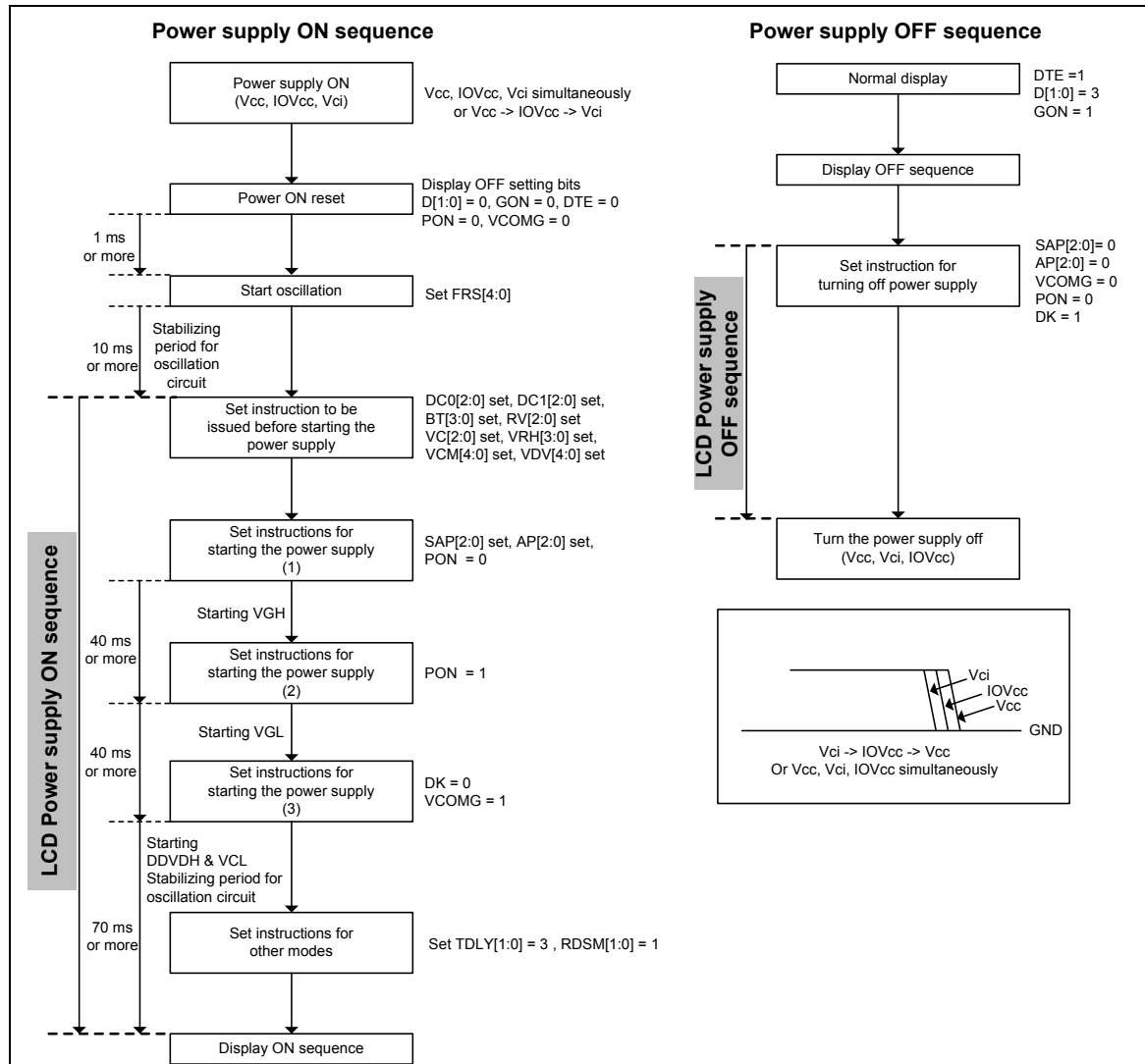


Figure 75

## Instruction Setting

The following are the sequences for various instruction settings with the LGDP4535. When making the following instruction settings, follow the respective sequences below.

### Display ON/OFF sequence

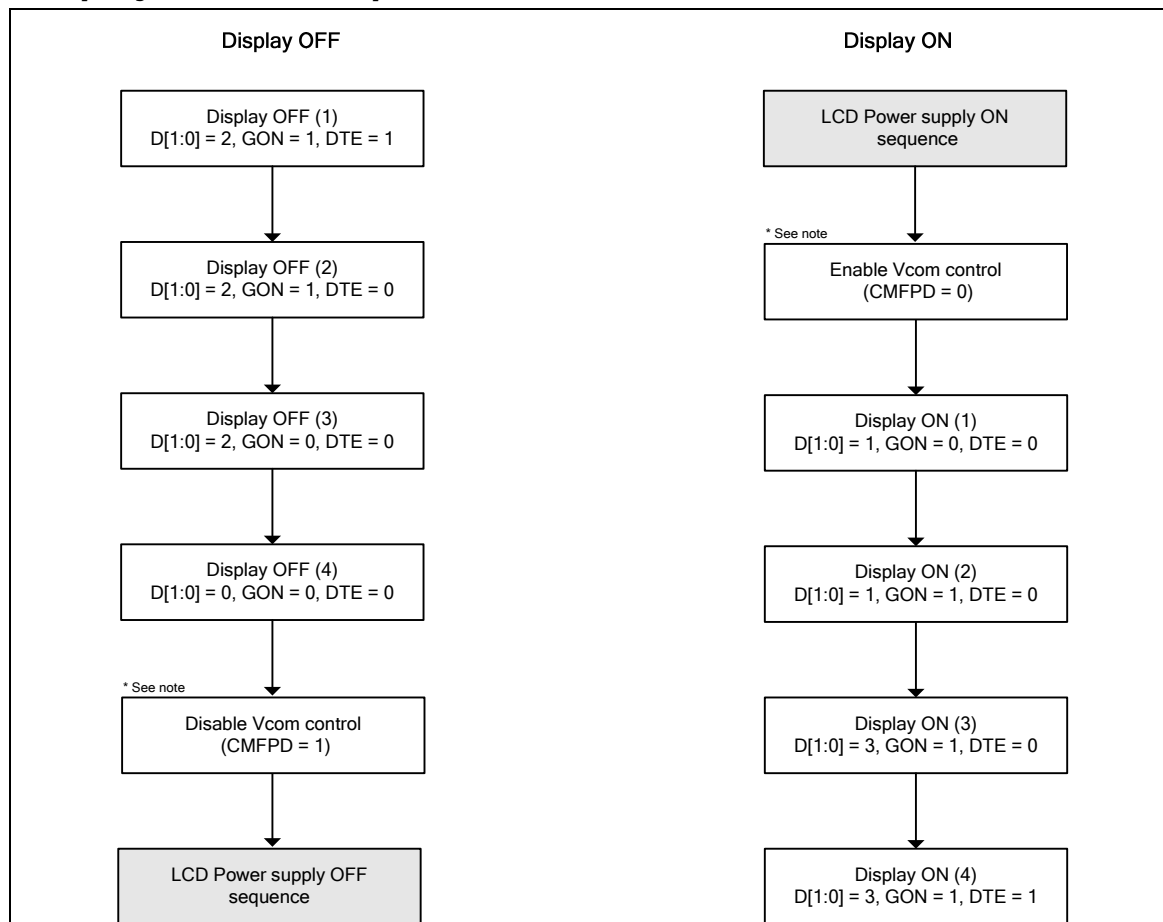
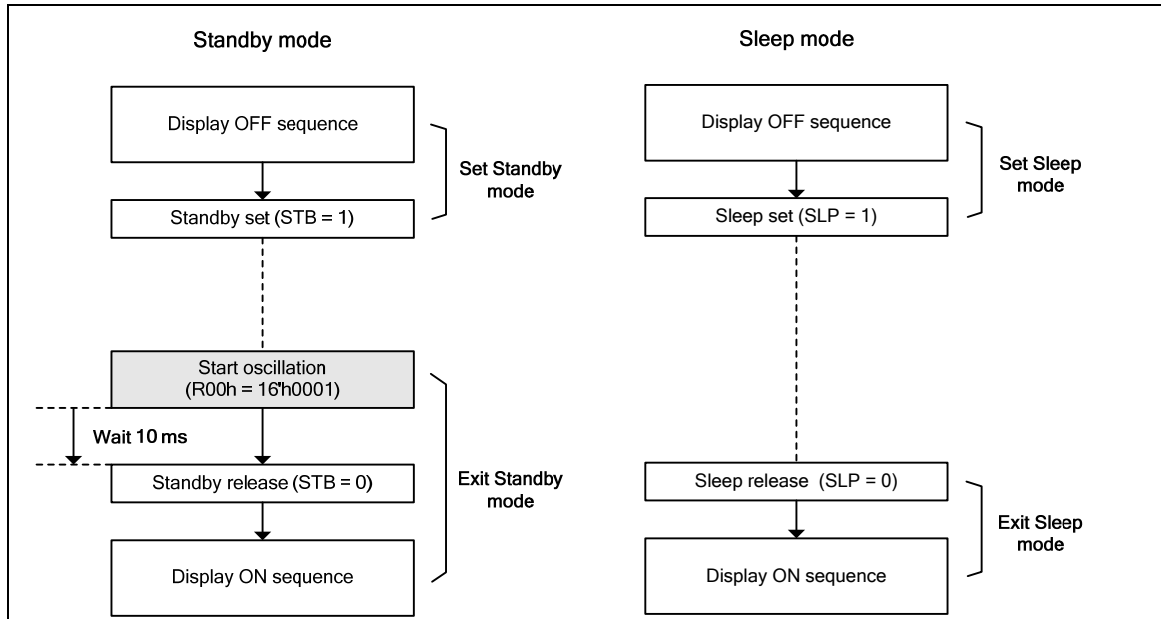


Figure 76

Note : When a line-inversion driving is set, exclude “Vcom feedback control ON/OFF” steps.

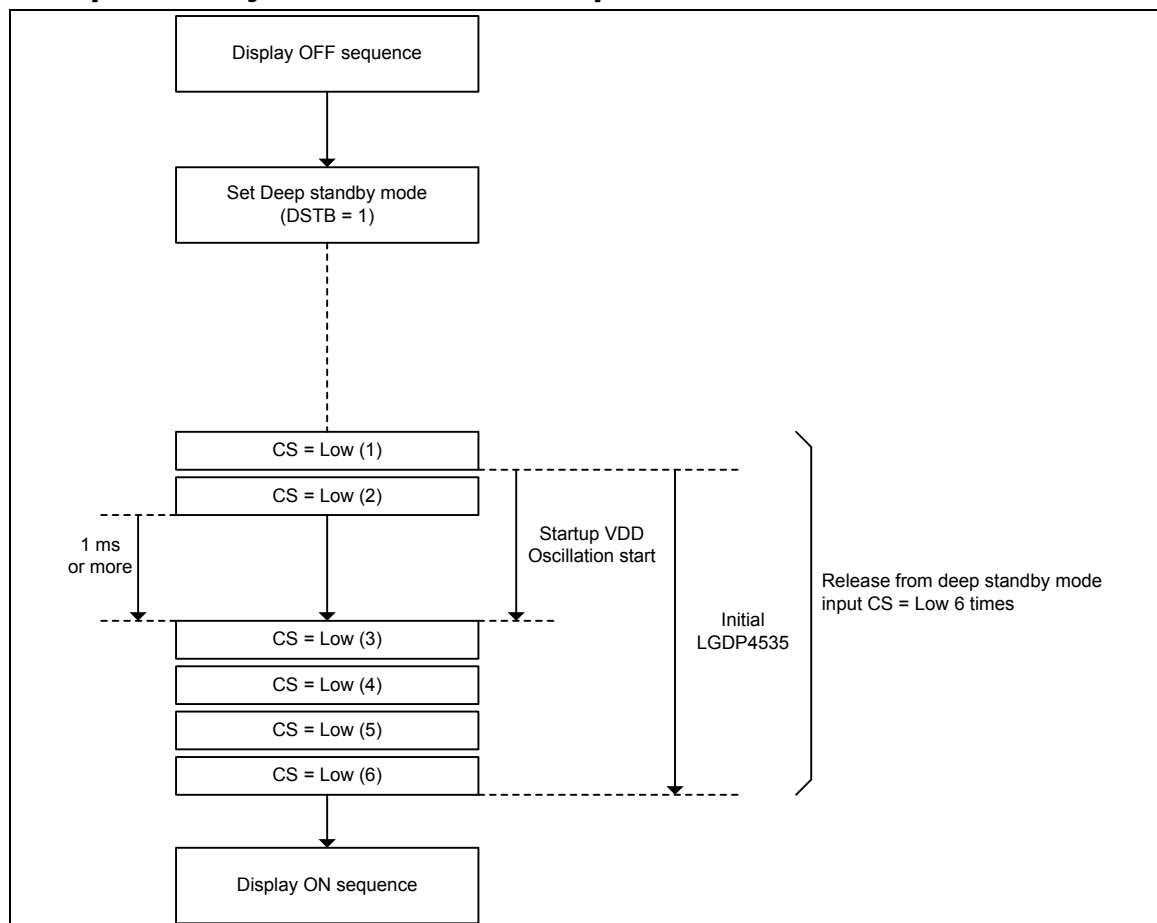
## Standby / Sleep mode SET/EXIT sequences



**Figure 77**

Note : "Display ON/OFF" sequences include "LCD Power Supply ON/OFF" sequences respectively.  
See "Display ON/OFF sequence" section.

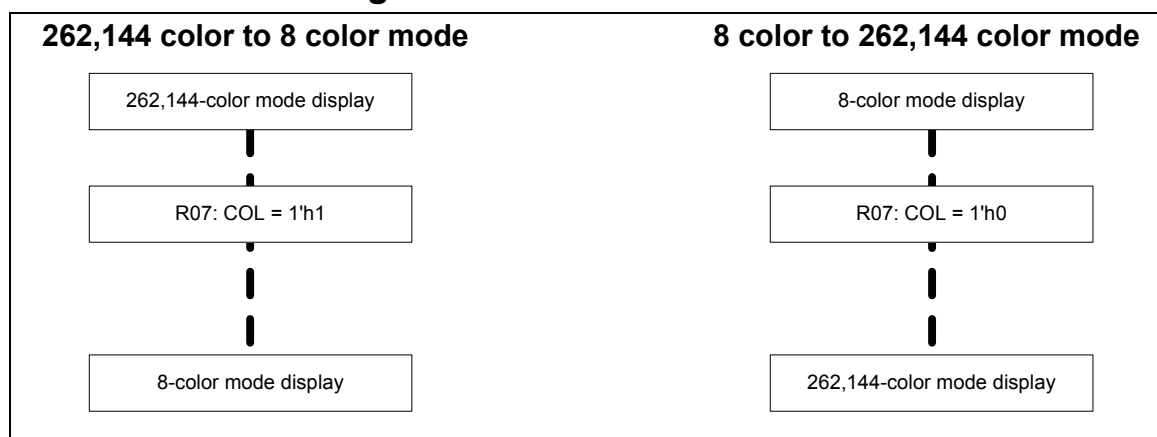
## Deep standby mode IN/EXIT sequences



**Figure 78**

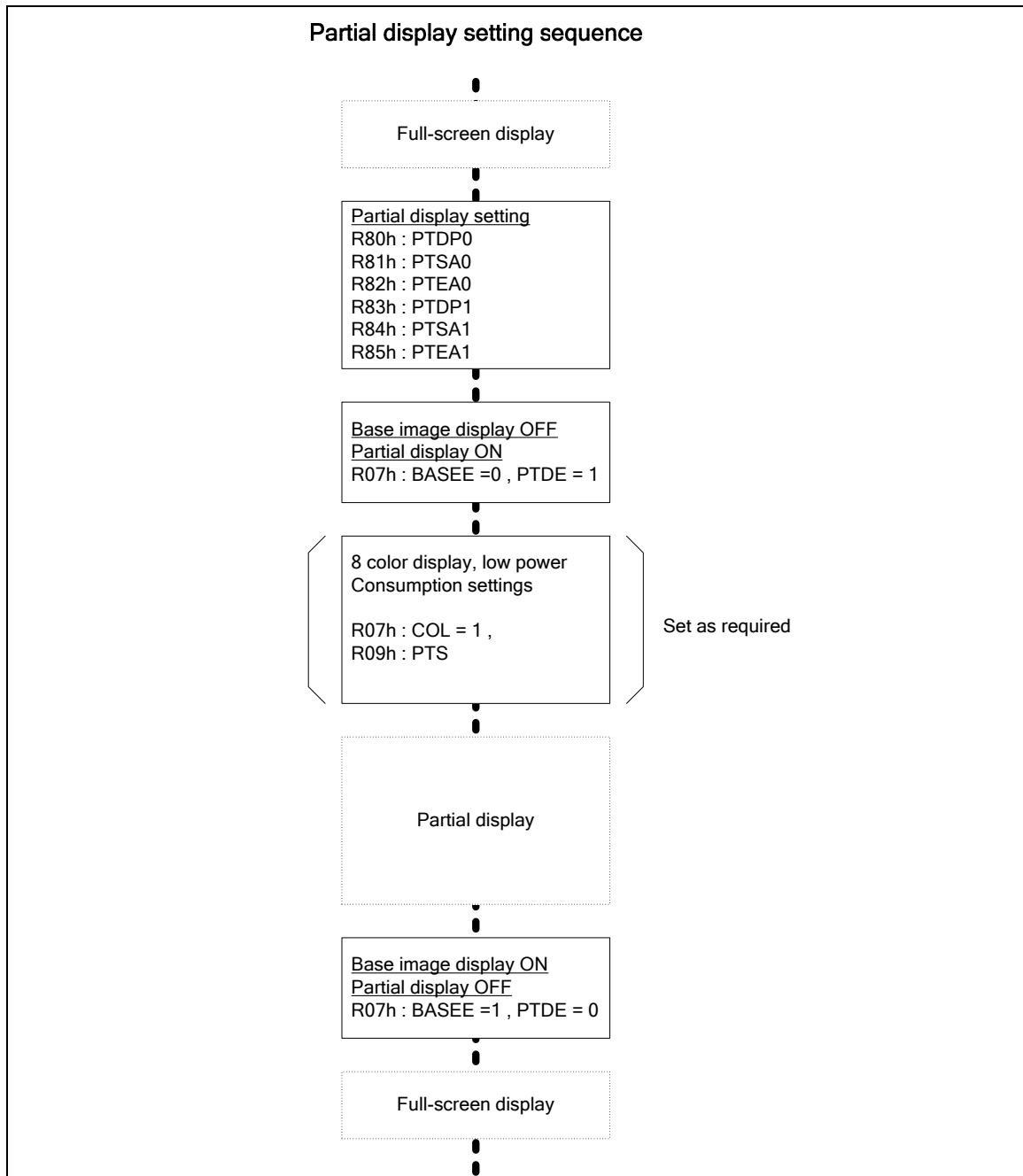
Note : “Display ON/OFF” sequences include “LCD Power Supply ON/OFF” sequences respectively.  
See “Display ON/OFF sequence” section.

## 8-color mode setting



**Figure 79**

## Parital Display setting



## Absolute Maximum Ratings

**Table 98**

Item	Symbol	Unit	value	Notes
Power supply voltage (1)	Vcc, IOVcc	V	-0.3 ~ +4.5	1, 2
Power supply voltage (2)	Vci – AGND	V	-0.3 ~ +4.5	1, 3
Power supply voltage (3)	DDVDH – AGND	V	-0.3 ~ +8.0	1, 4
Power supply voltage (4)	AGND – VCL	V	-0.3 ~ +4.5	1
Power supply voltage (5)	DDVDH – VCL	V	-0.3 ~ +8.0	1, 5
Power supply voltage (6)	VGH – AGND	V	-0.3 ~ +18	1, 6
Power supply voltage (7)	AGND – VGL	V	-0.3 ~ +18	1, 7
Input voltage	Vt	V	-0.3~IOVcc+0.3	1
Operating temperature	Topr	°C	-40 ~ +85	1, 8
Storage temperature	Tstg	°C	-55 ~ +125	1

Note 1) If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.

Note 2) Make sure (High) Vcc ≥ GND (Low), (High) IOVcc ≥ GND (Low).

Note 3) Make sure (High) Vci ≥ GND (Low).

Note 4) Make sure (High) DDVDH ≥ AGND (Low).

Note 5) Make sure (High) DDVDH ≥ VCL (Low).

Note 6) Make sure (High) VGH ≥ AGND (Low).

Note 7) Make sure (High) AGND ≥ VGL (Low).

Note 8) The DC/AC characteristics of die and wafer products is guaranteed at 85 °C.



## Electrical Characteristics

### DC Characteristics

Table 99

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.	Notes
Input high-level voltage	$V_{IH}$	V	$IOV_{CC} = 1.65 \sim 3.3V$	$0.8IOV_{CC}$		$IOV_{CC}$	2,3
Input low-level voltage	$V_{IL}$	V	$IOV_{CC} = 1.65 \sim 3.3V$	0		$0.2IOV_{CC}$	2,3
Output high-level voltage (1) (DB17-0, SDO, FMARK)	$V_{OH1}$	V	$IOV_{CC} = 1.65 \sim 3.3V$ $I_{OH} = 0.1mA$	$0.8IOV_{CC}$			2
Output lowlevel voltage (1) (DB17-0, SDO, FMARK)	$V_{OL1}$	V	$IOV_{CC} = 1.65 \sim 3.3V$ $I_{OL} = 0.1mA$			$0.2IOV_{CC}$	2
I/O leakage current	$I_{II}$	$\mu A$	$V_{in} = 0 \sim IOV_{CC}$	-1		1	4
Current consumption : Deep standby mode	$I_{ST}$	$\mu A$	$IOV_{CC} = V_{CC} = V_{CI} = 2.8V$ , $T_a \approx 25^\circ C$		1	10	5

### 80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 100 See Figure 82 (Condition:  $IOV_{CC} = 1.65$  to  $3.30V$ ,  $V_{CC} = V_{CI} = 2.50$  to  $3.30V$ )

Item		Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time	Write	$t_{CYCW}$	ns	T.B.D.	-	-
	Read	$t_{CYCW}$	ns	T.B.D.	-	-
Write "Low" level pulse width	Write	$PW_{LW}$	ns	T.B.D.	-	-
Read "Low" level pulse width	Read	$PW_{LR}$	ns	T.B.D.	-	-
Write "High" level pulse width	Write	$PW_{HW}$	ns	T.B.D.	-	-
Read "High" level pulse width	Read	$PW_{HR}$	ns	T.B.D.	-	-
Write/Read rise/fall time		$t_{WRr}$ , $t_{WRf}$	ns		-	T.B.D.
Setup time	Write (RS to CS*/ WR*)	$t_{AS}$	ns	T.B.D.	-	-
	Read (RS to CS*/ RD*)			T.B.D.	-	-
Address hold time		$t_{AH}$	ns	T.B.D.	-	-
Write data setup time		$t_{DSW}$	ns	T.B.D.	-	-
Write data hold time		$t_H$	ns	T.B.D.	-	-
Read data delay time		$t_{DDR}$	ns	-	-	T.B.D.
Read data hold time		$t_{DHR}$	ns	T.B.D.	-	-

## 80-System Bus Interface Timing Characteristics (8/9-Bit Bus)

**Table 101** See Figure 82 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Bus Cycle time	Write	$t_{CYCW}$	ns	T.B.D.	-	-
	Read	$t_{CYCW}$	ns	T.B.D.	-	-
Write “Low” level pulse width	Write	$PW_{LW}$	ns	T.B.D.	-	-
Read “Low” level pulse width	Read	$PW_{LR}$	ns	T.B.D.	-	-
Write “High” level pulse width	Write	$PW_{HW}$	ns	T.B.D.	-	-
Read “High” level pulse width	Read	$PW_{HR}$	ns	T.B.D.	-	-
Write/Read rise/fall time		$t_{WRr}, t_{WRf}$	ns	-	-	T.B.D.
Setup time	Write (RS to CS*/ WR*)	$t_{AS}$	ns	T.B.D.	-	-
	Read (RS to CS*/ RD*)			T.B.D.	-	-
Address hold time		$t_{AH}$	ns	T.B.D.	-	-
Write data setup time		$t_{DSW}$	ns	T.B.D.	-	-
Write data hold time		$t_H$	ns	T.B.D.	-	-
Read data delay time		$t_{DDR}$	ns	-	-	T.B.D.
Read data hold time		$t_{DHR}$	ns	T.B.D.	-	-

## Serial Peripheral Interface Timing Characteristics

**Table 102** See Figure 83 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item		Symbol	Unit	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	$t_{SCYC}$	ns	T.B.D.	-	-
	Read (transmitted)	$t_{SCYC}$	ns	T.B.D.	-	-
Serial clock “High” level pulse width	Write (received)	$t_{SCH}$	ns	T.B.D.	-	-
	Read (transmitted)	$t_{SCH}$	ns	T.B.D.	-	-
Serial clock “Low” level pulse width	Write (received)	$t_{SCL}$	ns	T.B.D.	-	-
	Read (transmitted)	$t_{SCL}$	ns	T.B.D.	-	-
Serial clock rise/fall time		$t_{ser}, t_{scf}$	ns	-	-	T.B.D.
Chip select setup time		$t_{CSU}$	ns	T.B.D.	-	-
Chip select hold time		$t_{CH}$	ns	T.B.D.	-	-
Serial input data setup time		$t_{SISU}$	ns	T.B.D.	-	-
Serial input data hold time		$t_{SIH}$	ns	T.B.D.	-	-
Serial output data delay time		$t_{SOD}$	ns	-	-	T.B.D.
Serial output data hold time		$t_{SOH}$	ns	T.B.D.	-	-

## RGB Interface Timing Characteristics

**Table 103** See Figure 84 (18/16-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	ns	T.B.D.	-	-
ENABLE setup time	tENS	ns	T.B.D.	-	-
ENABLE hold time	tENH	ns	T.B.D.	-	-
DOTCLK "Low" level pulse width	PWDL	ns	T.B.D.	-	-
DOTCLK "High" level pulse width	PWDH	ns	T.B.D.	-	-
DOTCLK cycle time	tCYCD	ns	T.B.D.	-	-
Data setup time	tPDS	ns	T.B.D.	-	-
Data hold time	tPDH	ns	T.B.D.	-	-
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	-	-	25

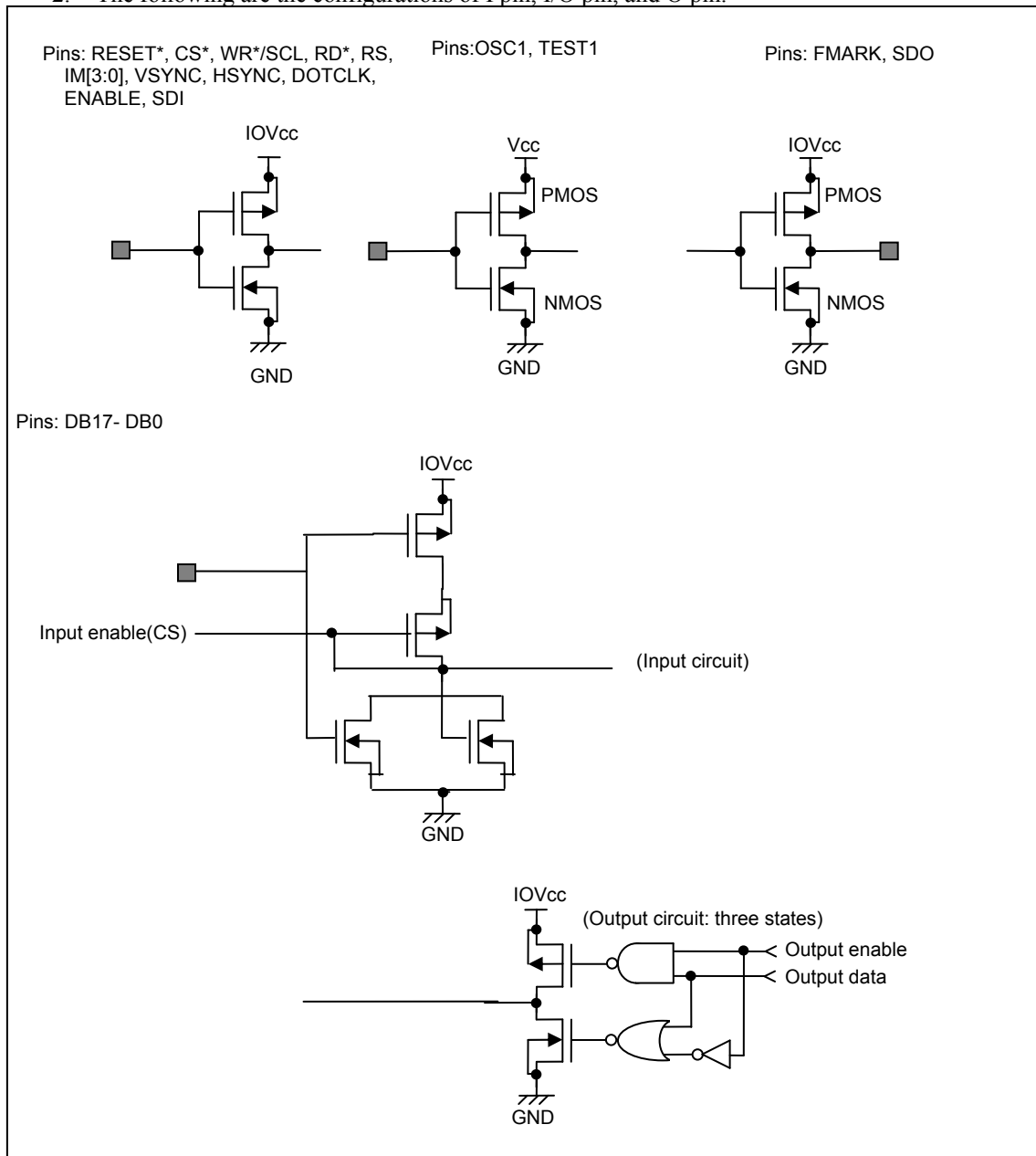
## Reset Timing Characteristics

**Table 104** See Figure 85 (Condition: IOVcc = 1.65 to 3.30V, Vcc = Vci = 2.50 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset "Low" level width	t <sub>RES</sub>	ms	T.B.D.	-	-
Reset rise time	t <sub>rRES</sub>	us	-	-	T.B.D.

## Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the configurations of I pin, I/O pin, and O pin.



**Figure 81**

3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the IOVcc level.
4. This excludes currents though the output drive MOS.
5. This excludes currents flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CS\* pin is set to "High" or "Low".

## Timing characteristic diagram

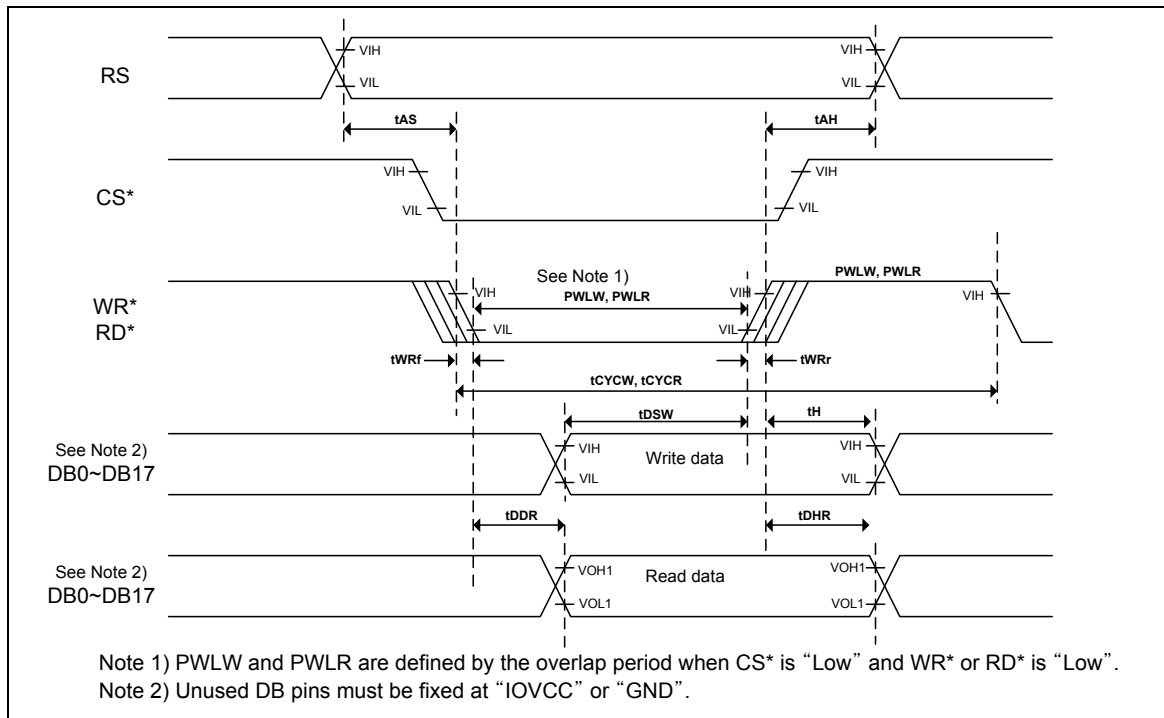


Figure 82 80-system bus interface operation

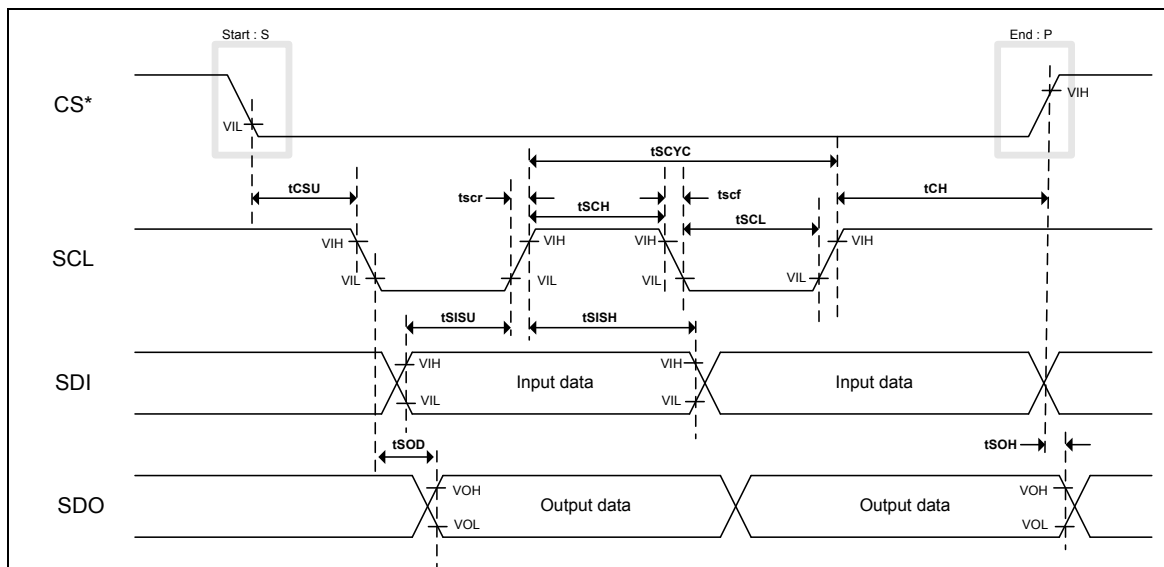


Figure 83 Serial Peripheral Interface operation

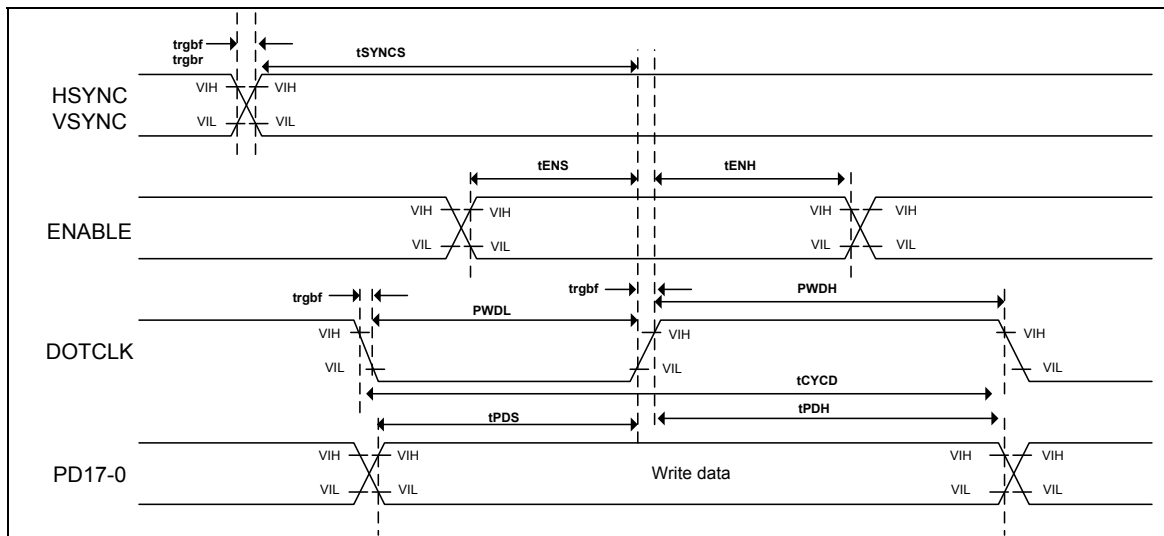


Figure 84 RGB interface operation

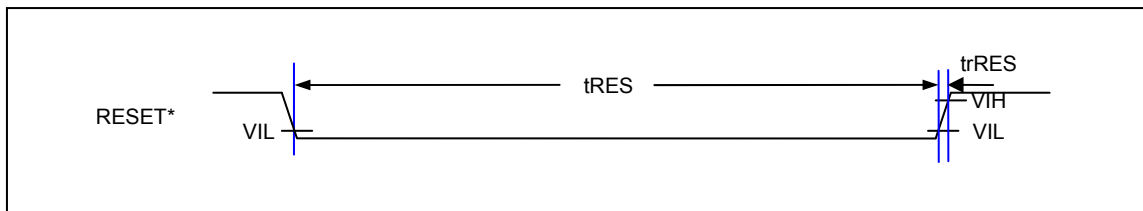


Figure 85 Reset operation

### Revision History

Rev.	Date	Revision Description	Revised by
0.0	2007.12.03	Preliminary release	S.H. Koh
0.1	2007.12.05	Remove separate gamma	S.H. Koh
0.11	2007.12.28	p.54 Revised Step-up output voltage setting : Table	Y. Kim
0.12	2008.02.26	p.58 Corrected the voltage range of VcomL	D.H. Kim
0.12	2008.02.26	p.82 Revised the initial states on Reset Function	C.S. Park
0.12	2008.02.26	p.143~145 Erased the C23N / C23P capacitors Removed a schottky diode (VCI-VGH), and then placed the other (DDVDH-VGH)	C.S. Park
0.12	2008.02.26	p.58 Revised the description of VCOMG register	D.H. Kim
0.12	2008.02.26	p.147 Added other register settings ( TDLY[1:0]=2'h3 , RDSM[1:0]=2'h1 ) on the " Power Supply ON sequence "	C.S. Park