Technical Report

LGDP4535 Application Notes

240 x 320 Resolution and 260K color Single Chip Solution

LG Electronics
System IC Team
LDI Circuit Design Gr.

GS Gangnam Tower
In SEOUL

2008 MAR 10

Version 2.0

INDEX

LGDP4535

1. LG Display 2.8” QVGA Panel

1) Application Circuit

2) Initial code

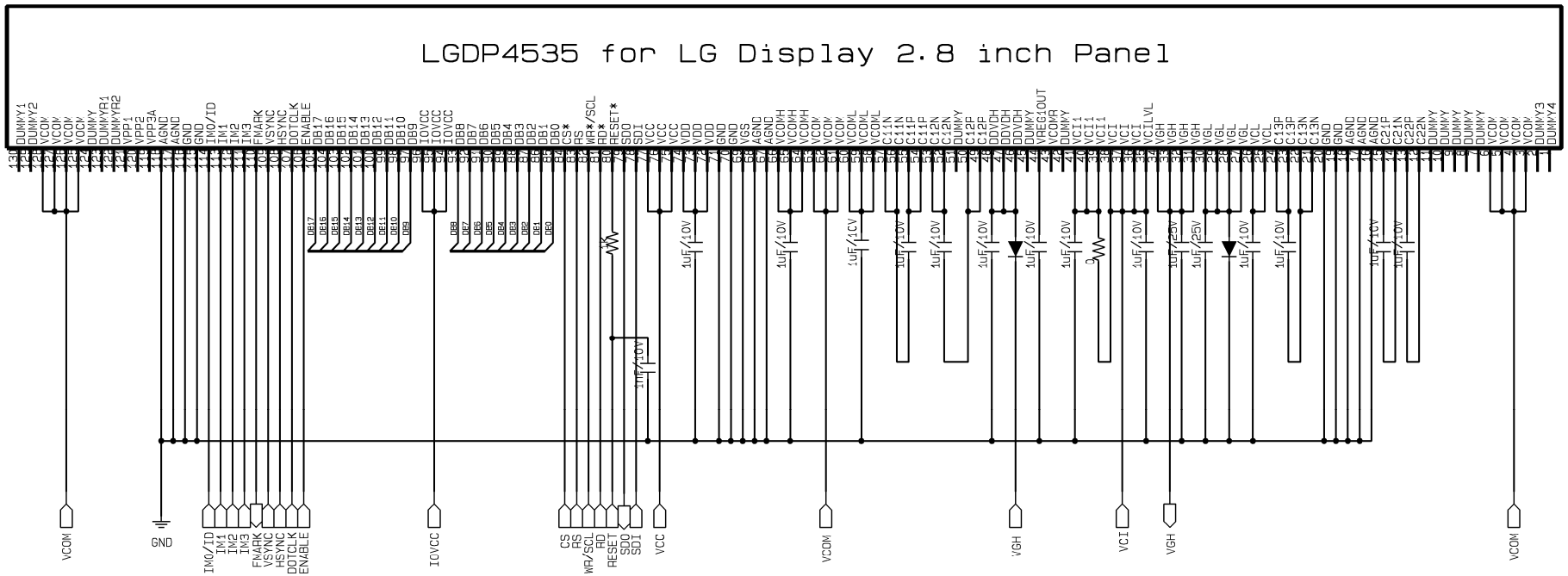
2. HYDIS 2.8” QVGA Panel

1) Application Circuit

2) Initial code

◈ LG Display 2.8” Application Circuit

LGDP4535



IM3	IM2	IM1	IM0	80-System interface Mode
1	0	1	0	18-bit Interface
0	0	1	0	16-bit Interface
1	0	1	1	9-bit Interface
0	0	1	1	8-bit Interface
0	1	0	ID	Serial Peripheral Interface(SPI)

Note :

1) When the RGB interface is not used, please shorted the VSYNC, HSYNC, DOTCLK and ENABLE to GND.
2) When the SPI interface is not used, the SDI is shorted to GND and let SDO as open.
3) All the VCOM pins must be shorted together.
4) The Resistor (Between VCI(#38) and VCI1(#39)) : open(no use) or 0 ohm.

DIMENSIONAL	TOLERANCE
ANGULAR	0

UNLESS OTHERWISE SPECIFIED

C	B	A	NO	PART NO	DESCRIPTION	MATERIAL	COLOR FINISH	NOTE
QUANTITY								

THIRD ANGLE PRO | SCALE | UNIT mm | DRAWN J.K. LEE | CHECKED | APPROVED | DATE 2008-02-27 | ISSUE

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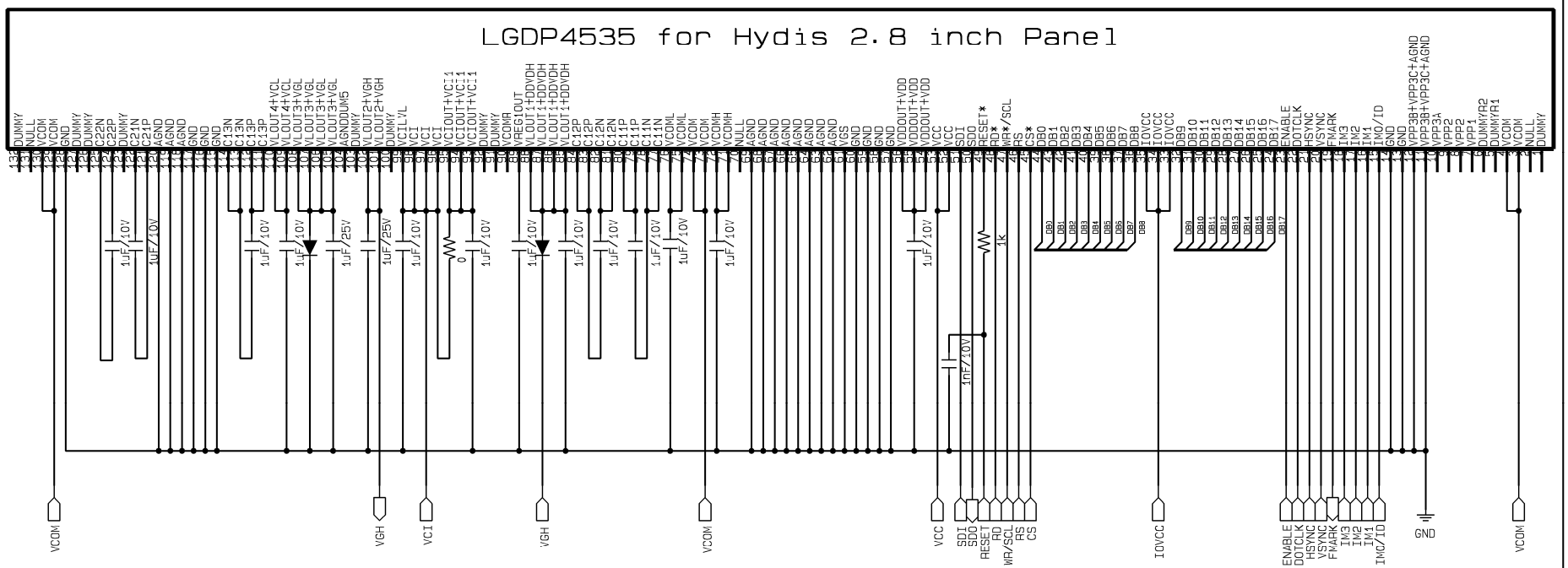
LGDP4535 Application Circuit – LG Display 2.8 inch

◈ Hydis 2.8" Application Circuit



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1	0	1	0	18-bit Interface
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Note :

1) When the RGB interface is not used, please shorted the VSYNC, HSYNC, DOTCLK and ENABLE to GND.
2) When the SPI interface is not used, the SDI is shorted to GND and let SDO as open.
3) All the VCOM pins must be shorted together.
4) The Resistor (Between VCI(#95) and VCIOUT+VCI1(#96)) : open(no use) or 0 ohm.

DIMENSIONAL	TOLERANCE
ANGULAR	0

UNLESS OTHERWISE SPECIFIED

NO	PART NO	DESCRIPTION	MATERIAL	COLOR FINISH	NOTE
QUANTITY					

THIRD ANGLE PRO | SCALE | UNIT mm | DRAWN J.K. LEE | CHECKED | APPROVED | DATE 2008-02-27

LG Electronics Inc. | ISSUE | LGDP4535 Application Circuit - Hydis 2.8 inch

2008-03-10

Gamma Setting – LGDP4535 / LG Display 2.8-inch QVGA module

Initial Code – LGDP4535 / LG Display 2.8"

* Condition

1. VCI = VCC = IOVCC = 2.8V
2. R90 [DIVI] = "01" => 1/2 division

Initialization			
Reg (Hex)	Data (Hex)	Delay (ms)	
0X15	0X0030		Power ON sequence
0x9A	0X0010		
0X11	0X0020		
0X10	0X3428		
0X12	0X0002		
0X13	0X1038		
DELAY		40	
0X12	0X0012		
DELAY		40	
0X10	0X3420		
0X13	0X3038		
DELAY		70	
0X30	0X0000		Display Mode & Gamma settings
0X31	0X0402		
0X32	0X0307		
0X33	0X0304		
0X34	0X0004		
0X35	0X0401		
0X36	0X0707		
0X37	0X0305		
0X38	0X0610		
0X39	0X0610		
0X01	0X0100		
0X02	0X0300		
0X03	0X1030		
0X08	0X0808		
0X0A	0X0008		
0X60	0X2700		
0X61	0X0001		
0X90	0X013E		
0X92	0X0100		
0X93	0X0100		
0XA0	0X3000		
0XA3	0X0010		
0X07	0X0001		Display ON sequence
0X07	0X0021		
0X07	0X0023		
0X07	0X0033		
0X07	0X0133		

SLEEP ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0032	
DELAY		20
0X07	0X0022	
DELAY		20
0X07	0X0002	
DELAY		20
0x07	0X0000	
DELAY		10
0X17	0X0001	
0x13	0X0000	
0X12	0X0000	
0X10	0X0008	
DELAY		10
0X10	0X000A	

↔

SLEEP EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
0X10	0X0008	
↓		
Power ON sequence		
↓		
Display ON sequence		

STAND-BY ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0032	
DELAY		20
0X07	0X0022	
DELAY		20
0X07	0X0002	
DELAY		20
0x07	0X0000	
DELAY		10
0X17	0X0001	
0x13	0X0000	
0X12	0X0000	
0X10	0X0008	
DELAY		10
0X10	0X0009	

↔

STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
0X00	0X0001	
0X10	0X0008	
DELAY		10
↓		
Power ON sequence		
↓		
Display ON sequence		

DEEP STAND-BY ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0032	
DELAY		20
0X07	0X0022	
DELAY		20
0X07	0X0002	
DELAY		20
0x07	0X0000	
DELAY		10
0X17	0X0001	
0x13	0X0000	
0X12	0X0000	
0X10	0X0008	
DELAY		10
0X10	0X000C	

↔

DEEP STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
2 times CS pin toggle		
DELAY		1
4 times CS pin toggle		
Initialization		

or

↔

STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
H/W Reset		
Initialization		

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2008-03-10

Gamma Setting – LGDP4535 / Hydis 2.8-inch QVGA module

Initial Code – LGDP4535 / Hydis 2.8"

* Condition

1. VCI = VCC = IOVCC = 2.8V
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Initialization			
Reg (Hex)	Data (Hex)	Delay (ms)	
0X15	0X0030		Power ON sequence
0x9A	0X0010		
0X11	0X0020		
0X10	0X3428		
0X12	0X0004		
0X13	0X1050		
DELAY		40	
0X12	0X0014		
DELAY		40	
0X10	0X3420		
0X13	0X3050		
DELAY		70	
0X30	0X0003		Display Mode & Gamma settings
0X31	0X0305		
0X32	0X0004		
0X33	0X0304		
0X34	0X0004		
0X35	0X0303		
0X36	0X0606		
0X37	0X0403		
0X38	0X050F		
0X39	0X0510		
0X01	0X0100		
0X02	0X0300		
0X03	0X1030		
0X08	0X0808		
0X0A	0X0008		
0X60	0X2700		
0X61	0X0001		
0X90	0X013E		
0X92	0X010F		
0X93	0X0001		
0XA0	0X3000		
0XA3	0X0010		
0X07	0X0001		Display ON sequence
0X07	0X0021		
0X07	0X0023		
0X07	0X0033		
0X07	0X0133		

SLEEP ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0032	
DELAY		20
0X07	0X0022	
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0x07	0X0000	
DELAY		10
0X17	0X0001	
0x13	0X0000	
0X12	0X0000	
0X10	0X0008	
DELAY		10
0X10	0X000A	

↔

SLEEP EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
0X10	0X0008	
↓		
Power ON sequence		
↓		
Display ON sequence		

STAND-BY ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0032	
DELAY		20
0X07	0X0022	
DELAY		20
0X07	0X0002	
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0X17	0X0001	
0x13	0X0000	
0X12	0X0000	
0X10	0X0008	
DELAY		10
0X10	0X0009	

↔

STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
0X00	0X0001	
0X10	0X0008	
DELAY		10
↓		
Power ON sequence		
↓		
Display ON sequence		

DEEP STAND-BY ON		
Reg (Hex)	Data (Hex)	Delay (ms)
0X07	0X0032	
DELAY		20
0X07	0X0022	
DELAY		20
0X07	0X0002	
DELAY		20
0x07	0X0000	
DELAY		10
0X17	0X0001	
0x13	0X0000	
0X12	0X0000	
0X10	0X0008	
DELAY		10
0X10	0X000C	

↔

DEEP STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
2 times CS pin toggle		
DELAY		1
4 times CS pin toggle		
Initialization		

or

↔

STAND-BY EXIT		
Reg (Hex)	Data (Hex)	Delay (ms)
H/W Reset		
Initialization		

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