

R61505V

262,144-color, 240RGB x 320 dot graphics liquid crystal controller driver for Amorphous-Silicon TFT Panel

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Description	6
Features	7
Power supply specifications	8
<i>Differences between R61505U and R61505V</i>	10
Block Diagram	13
Block Function	14
1. System Interface	14
2. External Display Interface (RGB, VSYNC interfaces)	15
3. Address Counter (AC)	16
4. Graphics RAM (GRAM)	16
5. Grayscale Voltage Generating Circuit	16
6. Liquid crystal drive power supply circuit	16
7. Timing Generator	16
8. Oscillator (OSC)	16
9. Liquid crystal driver Circuit	16
10. Internal logic power supply regulator	17
Pin Function	18
PAD Arrangement	24
PAD Coordinates	26
Bump Arrangement	40
Wiring Example & Recommended Wiring Resistance	41
GRAM Address Map	42
Instruction	44
Outline	44
Instruction Data Format	44
Index (IR)	45

Display Control	45
Device Code Read (R00h).....	45
Driver Output Control (R01h).....	46
LCD Driving Wave Control (R02h).....	47
Entry Mode (R03h).....	48
Display Control 1 (R07h).....	51
Display Control 2 (R08h).....	52
Display Control 3 (R09h).....	54
Display Control 4 (R0Ah).....	56
External Display Interface Control 1 (R0Ch).....	57
Frame Marker Position (R0Dh).....	59
VCOM Low Power Control (R0Eh).....	60
External Display Interface Control 2 (R0Fh).....	61
Power Control	62
Power Control 1 (R10h).....	62
Power Control 2 (R11h).....	64
Power Control 3 (R12h).....	67
Power Control 4 (R13h).....	69
RAM Access Control	70
RAM Address Set (Horizontal Address) (R20h) RAM Address Set (Vertical Address) (R21h).....	70
GRAM Data Write (R22h).....	71
GRAM Data Read (R22h).....	72
NVM(NON-VOLATILE MEMORY) Write Control	73
NVM Data Read 1 (R28), NVM Data Read 2 (R29h), NVM Data Read 3 (R2Ah).....	73
γControl	75
γ Control 1 ~ 10 (R30h ~ R39h).....	75
Window Address Control	77
Window Horizontal RAM Address (Start Address) (R50h).....	77
Window Horizontal RAM Address (End Address) (R51h).....	77
Window Vertical RAM Address (Start Address) (R52h).....	77
Window Vertical RAM Address (End Address) (R53h).....	77
Base Image Display Control	79
Driver Output Control (R60h).....	79
Base Image Display Control (R61h).....	79
Vertical Scroll Control (R6Ah).....	79
Partial Display Control Instruction	82
Partial Image Display Position (R80h).....	82
Partial Image RAM Address (Start Line Address) (R81h).....	82
Partial Image RAM Address (End Line Address) (R82h).....	82
Panel Interface Control	83
Panel Interface Control 1(R90h).....	83
Panel Interface Control 1-1 (R91h).....	85
Panel Interface Control 2(R92h).....	86
Panel Interface Control 3(R93h).....	87
Panel Interface Control 4 (R94h).....	88
Panel Interface Control 5 (R95h).....	89
Panel Interface Control 5-1 (R96h).....	91
Panel Interface Control 6 (R97h).....	92

<i>Panel Interface Control 7 (R98h)</i>	93
<i>Panel Interface Control 8 (R99h)</i>	94
<i>Panel Interface Control 9 (R9Ch)</i>	95
<i>NVM (NON-VOLATILE MEMORY) Control</i>	96
<i>NVM Control 1 (RA0h), NVM Control 2 (RA1h)</i>	96
<i>NVM Control 3 (RA3h), NVM Control 4 (RA4h)</i>	97
Instruction List	98
Reset Function	99
Basic Operation	100
Interface and Data Format	101
System Interface	104
<i>80-system 18-bit Bus Interface</i>	<i>105</i>
<i>80-system 16-bit Bus Interface</i>	<i>106</i>
<i>Data Transfer Synchronization in 16-bit Bus Interface operation</i>	<i>108</i>
<i>80-system 9-bit Bus Interface</i>	<i>109</i>
<i>Data Transfer Synchronization in 9-bit Bus Interface operation</i>	<i>110</i>
<i>80-system 8-bit Bus Interface</i>	<i>111</i>
<i>Data Transfer Synchronization in 8-bit Bus Interface operation</i>	<i>113</i>
<i>Serial Interface</i>	<i>114</i>
VSYNC Interface	117
<i>Notes to VSYNC Interface operation</i>	<i>119</i>
FMARK Interface	121
<i>FMP setting example</i>	<i>124</i>
External Display Interface	125
<i>RGB Interface</i>	<i>126</i>
<i>Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals</i>	<i>126</i>
<i>RGB Interface Timing</i>	<i>127</i>
<i>Setting Example of Display Control Clock in RGB Interface Operation</i>	<i>128</i>
<i>RGB Interface Timing</i>	<i>129</i>
<i>16-/18-bit RGB Interface Timing</i>	<i>129</i>
<i>RAM access via system interface in RGB interface operation</i>	<i>130</i>
<i>18-bit RGB interface</i>	<i>133</i>
<i>Notes to RGB interface operation</i>	<i>134</i>
RAM Address and Display Position on the Panel	135
<i>Restrictions in setting display control instruction</i>	<i>136</i>
<i>Instruction setting example</i>	<i>138</i>
Window Address Function	140

Scan Mode Setting	141
8-color Display Mode	142
Line Inversion AC Drive	143
<i>Alternating Timing</i>	144
Frame-Frequency Adjustment Function	145
<i>Relationship between liquid crystal drive duty and frame frequency</i>	145
Partial Display Function	146
Liquid Crystal Panel Interface Timing	147
<i>Internal clock operation</i>	147
<i>RGB interface operation</i>	148
γ Correction Function.....	149
<i>γCorrection Function</i>	149
<i>γCorrection Circuit</i>	149
<i>γCorrection Registers</i>	150
<i>Reference level adjustment registers</i>	150
<i>Interpolation Registers</i>	152
Power-supply Generating Circuit	156
<i>Power supply circuit connection example 1</i>	156
<i>Power supply circuit connection example 2 (VCI voltage is directly applied to VCII pin)</i>	157
Specifications of Power-supply Circuit External Elements	158
Voltage Setting Pattern Diagram	159
VCOMH Voltage Adjustment Sequence	160
NVM Control Sequence.....	162
<i>R61505U Compatible Sequence</i>	166
<i>R61505V Setting Sequence</i>	168
Instruction Setting Sequence.....	170
<i>R61505U Compatible Sequence</i>	170
<i>R61505V Setting Sequence</i>	171
<i>Other Mode Transition Setting Sequences</i>	172
<i>Deep Standby Mode IN/EXIT Sequences</i>	172
<i>8-color Mode Setting</i>	175
<i>Partial Display Setting</i>	175
Absolute Maximum Ratings	176
Electrical Characteristics	177

<i>DC Characteristics</i>	177
<i>AC Characteristics</i>	181
<i>Clock Characteristics</i>	181
<i>80-System Bus Interface Timing Characteristics (18-/ 16-bit Interface)</i>	181
<i>80-System Bus Interface Timing Characteristics (9-/ 8-bit Interface)</i>	182
<i>Clock-synchronized Serial Interface Timing Characteristics</i>	183
<i>Reset Timing Characteristics</i>	183
<i>RGB Interface Timing Characteristics</i>	184
<i>LCD Driver Output Characteristics</i>	185
<i>Notes on Electrical Characteristics</i>	186
<i>Test Circuits</i>	188
<i>Timing Characteristics</i>	189
<i>80-System Bus Interface</i>	189
<i>Clock Synchronous Serial Interface</i>	190
<i>Reset Operation</i>	191
<i>RGB Interface</i>	192
<i>LCD Driver Output and VCOM Output</i>	192
 Revision Record	 194

Description

The R61505V is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising RAM for a maximum 240 RGB x 320 dot graphics display, source driver, gate driver and power supply circuit. For efficient data transfer, the R61505V supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to the host processor. The R61505V supports also RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE and DB17-0) to display moving images.

The power supply circuit incorporates step-up circuits and voltage follower circuits to voltage levels to drive TFT liquid crystal panel.

The R61505V's power management functions i.e. 8-color display, the deep standby mode and so on make this LSI an ideal driver for the medium or small sized portable devices with color display systems such as digital cellular phones or small PDAs, where long battery life is a major concern.

Features

- A single-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 240RGB x 320dots graphics display on amorphous TFT panel in 262k colors
- System interface
 - High-speed interfaces via 8-, 9-, 16-, 18-bit parallel ports
 - Clock synchronous serial interface
- Moving picture display interface ^{Note}
 - 16-/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
 - VSYNC interface (System interface + VSYNC)
 - FMARK interface (System interface + FMARK)
- Window address function to specify a rectangular area in the internal RAM to write data
- Write data within a rectangular area in the internal RAM via moving picture interface
- Reduce data transfer by specifying the area in the RAM to rewrite data
- Enable displaying the data in the still picture RAM area with a moving picture simultaneously
- Abundant color display and drawing functions
 - Programmable γ -correction function for 262k-color display
 - Partial display function
- Low -power consumption architecture (enables to supply power directly to interface I/O)
 - Deep standby function
 - 8-color display function
 - Input power supply voltages: IOVCC (power supply for interface I/O)
VCC (power supply for logic regulator)
VCI (power supply for liquid crystal analog circuit)
- Incorporates a liquid crystal drive power supply circuit
 - Source driver liquid crystal drive/VCOM power supply: DDVDH, VREG1OUT, VCL, VCI
 - Gate drive power supply: VGH, VGL
 - VCOM drive (VCOM power supply): VCOMH
VCOML
- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common VCOM formula)
- 172,800-byte internal RAM
- Internal 720-channel source driver and 320-channel gate driver
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal NVM: User identification code, 4 bits, VCOM level adjustment, 7 bits x 2 sets. Deleting data is guaranteed up to 5 times.
- Internal reference voltage to generate VREG1OUT

Note: Patent of moving picture display interface is granted.

United States Patent No. 7,176,870

Japanese Patent No. 3,826,159

Korean Patent No. 747,636

Power supply specifications

Table 1

No.	Item	R61505V	
1	TFT data lines	720	
2	TFT gate lines	320	
3	TFT display storage capacitance	Cst only (Common VCOM formula)	
4	Liquid crystal drive output	S1~S720	Grayscale levels V0 ~ V63
		G1~320	VGH-VGL
		VCOM	VCOMH=3.0 ~ (DDVDH-0.5)V VCOML=(VCL+0.5) ~ 0V Amplitude between VCOMH and VCOML=max. 6V Change VCOMH with either electronic volume or from VCOMR Change VCOMH-VCOML amplitude with electronic volume
5	Input voltage	IOVCC (interface voltage)	1.65V ~ 3.3V Power supply to IM0-3, RESETX, DB17-0, RDX, SDI, SDO, WRX/SCL, RS, CSX, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK Connect to VCC and VCI on the FPC when the electrical potentials are the same.
		VCC (logic regulator power supply)	2.5V ~ 3.3V Connect to IOVCC and VCI on the FPC when the electrical potentials are the same.
		VCI (liquid crystal drive power supply voltage)	2.5V ~ 3.3V Connect to IOVCC and VCC on the FPC when the electrical potentials are the same.
		VPP1, 2, 3A, 3B, 3C (Power supply for the NVM)	(Write) VPP1: $9.2 \pm 0.3V$ VPP2: $9.2 \pm 0.3V$ VPP3A, 3B, 3C: Fix to GND
			(Erase) VPP1: $9.2 \pm 0.3V$ VPP2: $9.2 \pm 0.3V$ VPP3A : $-9.2 \pm 0.3V$ VPP3B, 3C: Fix to GND
6	Liquid crystal drive voltages	DDVDH	4.5V ~ 6.0V
		VGH	10.0V ~ 18.0V
		VGL	-4.5V ~ -13.5V
		VGH-VGL	Max. 28.0V
		VCL	-1.9V ~ -3.0V
		VCI-VCL	Max. 6.0V

7	Internal step-up circuits	DDVDH	VCI1 x 2
		VGH	VCI1 x 5, x 6
		VGL	VCI1 x -3, x -4, x -5
		VCL	VCI1 x -1

Differences between R61505U and R61505V

Table 2 Functions

	R61505U	R61505V
FRC	32 grayscales, with FRC	64 grayscales, without FRC
RGB I/F	6/16/18 bits	16/18 bits
High speed write	Supported	Not supported
Resizing	Supported	Not supported
Partial display	2 images	1 image
Sequencer	Semi-automatic	Automatic
γ correction	84 bits	100 bits
VCM	5 bits	7 bits
NVM erase function	Not supported	Supported
DDVDH level	VCI1 x 2, x 3	VCI1 x 2
VGH level	VCI1 x 6, x 7, x 8	VCI1 x 5, x 6
Serial interface	2 chip address	1 chip address only

Table 3 Voltage

	R61505U	R61505V
VGH	10.0 ~ 20.0V	10.0 ~ 18.0V

C23 is omitted.

Table 4 Notations

R61505U	R61505V
CS*	CSX
WR*	WRX
RESET*	RESETX
RD*	RDX

Table 5 Registers

Address	Register Name	Contents of changes	
R00h	Device Code Read	Changed	1505 → B505 (to identify the differences between the R61505U and R61505V)
R02h	EOR	Deleted	The R61505V does not support the function.
R03h	HMW	Deleted	The R61505V does not support the function.
R04h	RCV [1:0]	Deleted	The R61505V does not support the function.
	RCH [1:0]	Deleted	The R61505V does not support the function.
	RCZ [1:0]	Deleted	The R61505V does not support the function.
R07h	VON	Deleted	Power supply sequence of the R61505V is automated.
	GON	Deleted	Power supply sequence of the R61505V is automated.
	DTE	Deleted	Power supply sequence of the R61505V is automated.
	D [1:0]	Deleted	Power supply sequence of the R61505V is automated.
R08h	FP[7:0] BP[7:0]	Specification changed	Number of bits is increased from 4 to 8 to enable wider front and back porch periods.
R09h	PTG	Specification changed	Simplified
R10h	APE	Deleted	Power supply sequence of the R61505V has been automated.
	SAP [1:0]	Deleted	Grayscale output method changed.
	AP [1:0]	Specification changed	Setting changed.
	BT[2:0]	Specification changed	Step-up factors changed.
R11h	DC0 [2:0]	Specification changed	Specification of step-up clock frequency for Step-up circuit 1 changed.
	DC1 [2:0]	Specification changed	Specification of step-up clock frequency for Step-up circuit 2 changed.
	VC [2:0]	Specification changed	Specification of VCI voltage changed.
R12h	VRH [4:0]	Specification changed	Factors changed.
	PON, PSON	Specification changed	Sequence changed.
	VREG1R	Deleted	The R61505V internally generates VREG1OUT from VCIR.
	VCMR	Specification changed	Internal electronic volume is selected as default in the R61505V.
R13h	VDV [4:0]	Specification changed	Factors changed.
R17h	PSE	Deleted	Power supply sequence of the R61505V is automated.
R19h	TBT	Deleted	Power supply sequence of the R61505V is automated.
R0Eh	VEM [1:0]	Specification changed	The R61505V is capable of equalizing both VCOMH and VCOML.

R28h	UID [3:0]	Specification changed	Default value changed.
R29h	VCM1 [6:0]	Specification changed	Number of VCM1 bit and default value are changed. The R61505V is capable of finer voltage level setting.
R2Ah	VCM2 [6:0]	Specification changed	Number of VCM2 bit and default value are changed. The R61505V is capable of finer voltage level setting.
	VCMSEL	Specification changed	New specification of NVM (130nm)
R30~39h	γ Control	Specification changed	Control method changed.
R60h	SCN [5:0]	Specification changed	Setting changed.
R83h	PTDP1	Deleted	The R61505V does not support the function.
R84h	PTSA1	Deleted	The R61505V does not support the function.
R85h	PTEA1	Deleted	The R61505V does not support the function.
R93h	MCPI [2:0]	Specification changed	Sets VCOM alternating position. (The R61505V is capable of controlling source output position and VCOM alternating position separately.)
R94h	SDTI [2:0]	Added	Sets source output alternating position. (The R61505V is capable of controlling source output position and VCOM alternating position separately.)
R97h	NOWE[2:0]	Specification changed	Specification of non-overlap period changed.
R98h	MCPE [2:0]	Specification changed	Sets VCOM alternating position. (The R61505V is capable of controlling source output position and VCOM alternating position separately.)
R99h	SDTE [2:0]	Added	Sets source output alternating position. (The R61505V is capable of controlling source output position and VCOM alternating position separately.)
RA0h	NVAD [1:0]	Added	New specification of NVM (130nm)
	EAD[1:0]	Deleted	The R61505V does not support the function.
RA1h	NVDAT [15:0]	Added	New specification of NVM (130nm)
	ED[7:0]	Deleted	The R61505V does not support the function.
RA3h	NVVREF	Added	New specification of NVM (130nm)

Block Diagram

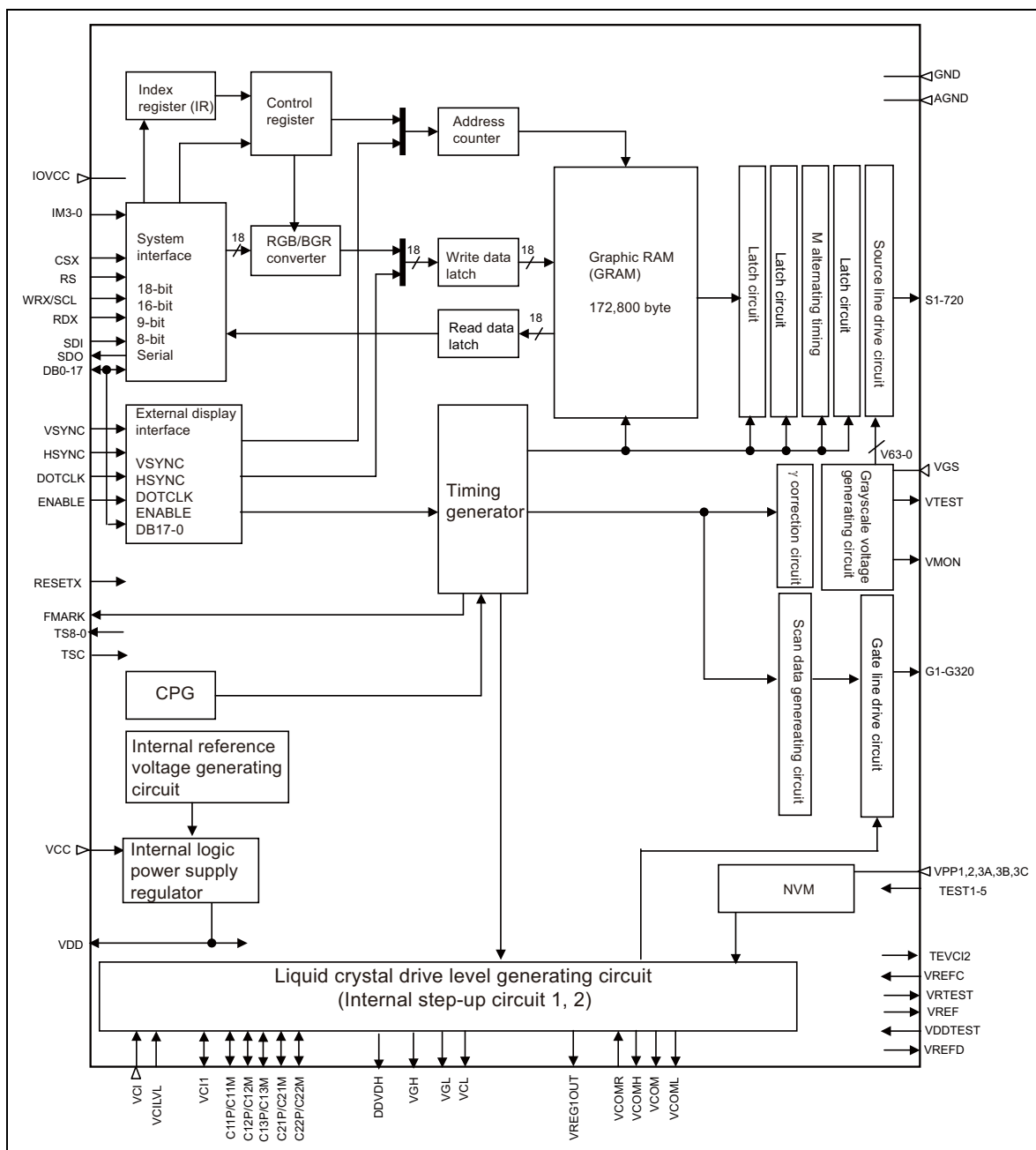


Figure 1

Block Function

1. System Interface

The R61505V supports 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The R61505V has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control register and internal GRAM. The WDR is the register to temporarily store data to be written to control register and internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the HOST PROCESSOR to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the R61505V performs the first read operation from the internal GRAM. Valid data is read out when the R61505V performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 6 Register Selection (80-system 8/9/16/18-bit Parallel Interface)

WRX	RDX	RS	Function
0	1	0	Write index to IR
1	0	0	Setting disabled
0	1	1	Write to control register or internal GRAM via WDR
1	0	1	Read from internal GRAM and register via RDR

Table 7 Register Selection (Clock synchronous serial interface)

Start byte		
RW	RS	Function
0	0	Write index to IR
1	0	Setting disabled
0	1	Write to control register or internal GRAM via WDR
1	1	Read from internal GRAM and register via RDR

Table 8

IM3	IM2	IM1	IM0	System interface	DB pins	RAM write data	Instruction write transfer
0	0	0	0	Setting disabled	-	-	-
0	0	0	1	Setting disabled	-	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
0	0	1	1	80-system 8-bit interface	DB17-10	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	0	0	Clock synchronous serial interface	(SDI, SDO)	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	0	1	Setting disabled	-	-	-
0	1	1	0	Setting disabled	-	-	-
0	1	1	1	Setting disabled	-	-	-
1	0	0	0	Setting disabled	-	-	-
1	0	0	1	Setting disabled	-	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
1	0	1	1	80-system 9-bit interface	DB17-9	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	1	0	0	Setting disabled	-	-	-
1	1	0	1	Setting disabled	-	-	-
1	1	1	0	Setting disabled	-	-	-
1	1	1	1	Setting disabled	-	-	-

2. External Display Interface (RGB, VSYNC interfaces)

The R61505V supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal GRAM via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal RAM. For details, see the “VSYNC interface” section.

The R61505V allows switching interface by instruction according to the display, i.e. still and/or moving picture(s) in order to transfer data only when the data is updated and thereby reduce the data transfer and power consumption for moving picture display.

3. Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register to set a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As the R61505V writes data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only within the rectangular area specified in the GRAM.

4. Graphics RAM (GRAM)

GRAM is graphics RAM, which can store bit-pattern data of 172,800 (240RGB x 320 (dots) x 18(bits)) bytes at maximum, using 18 bits per pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltages according to the grayscale data in the γ -correction registers to enable 262k-color display. For details, see the γ -Correction Register section.

6. Liquid crystal drive power supply circuit

The liquid crystal drive power supply circuit generates DDVDH, VGH, VGL and VCOM levels to drive liquid crystal.

7. Timing Generator

The timing generator generates a timing signal for the operation of internal circuit such as the internal GRAM. The timing signal for display operation such as RAM read operation and the timing signal for internal operation such as RAM access from the HOST PROCESSOR are generated separately in order to avoid mutual interference.

8. Oscillator (OSC)

Internal oscillator generates clock signal used to operate the R61505V.

The R61505V generates the Internal oscillation clock using internal oscillator. Adjusting the frequency by external resistance is impossible. Adjust the oscillation frequency and line numbers by Frame-Frequency Adjustment Function. During the deep standby mode, Internal oscillation halts to reduce power consumption. See "Oscillator" for details.

9. Liquid crystal driver Circuit

The liquid crystal driver circuit of the R61505V consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be

changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

10. Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

Pin Function

Table 9 Interface

Signal	I/O	Connect to	Function	When not in use																																																																																																																						
IM3-0	I	GND or IOVCC	Select a mode to interface to host processor. (Amplitude: IOVCC ~ GND)	-																																																																																																																						
			IM3		IM2	IM1	IM0	Interface Mode	DB Pin	Colors	0	0	0	0	Setting disabled	-	-	0	0	0	1	Setting disabled	-	-	0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 see Note 1	0	0	1	1	80-system 8-bit interface	DB17-10	262,144 see Note 2	0	1	0	0	Clock synchronous serial interface	-	65,536	0	1	0	1	Setting disabled			0	1	1	0	Setting disabled	-	-	0	1	1	1	Setting disabled	-	-	1	0	0	0	Setting disabled	-	-	1	0	0	1	Setting disabled	-	-	1	0	1	0	80-system 18-bit interface	DB17-0	262,144	1	0	1	1	80-system 9-bit interface	DB17-9	262,144	1	1	0	0	Setting disabled	-	-	1	1	0	1	Setting disabled	-	-	1	1	1	0	Setting disabled	-	-	1	1	1	1	Setting disabled	-	-
			IM3		IM2	IM1	IM0	Interface Mode	DB Pin	Colors																																																																																																																
			0		0	0	0	Setting disabled	-	-																																																																																																																
			0		0	0	1	Setting disabled	-	-																																																																																																																
			0		0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 see Note 1																																																																																																																
			0		0	1	1	80-system 8-bit interface	DB17-10	262,144 see Note 2																																																																																																																
			0		1	0	0	Clock synchronous serial interface	-	65,536																																																																																																																
			0		1	0	1	Setting disabled																																																																																																																		
			0		1	1	0	Setting disabled	-	-																																																																																																																
			0		1	1	1	Setting disabled	-	-																																																																																																																
			1		0	0	0	Setting disabled	-	-																																																																																																																
			1		0	0	1	Setting disabled	-	-																																																																																																																
			1		0	1	0	80-system 18-bit interface	DB17-0	262,144																																																																																																																
			1		0	1	1	80-system 9-bit interface	DB17-9	262,144																																																																																																																
			1		1	0	0	Setting disabled	-	-																																																																																																																
			1		1	0	1	Setting disabled	-	-																																																																																																																
			1		1	1	0	Setting disabled	-	-																																																																																																																
			1		1	1	1	Setting disabled	-	-																																																																																																																
			Notes: 1. 65,536 colors in one transfer mode 2. 65,536 colors in two transfers mode																																																																																																																							
CSX	I	Host processor	Chip select signal. Amplitude: IOVCC-GND Low: the R61505V is selected and accessible High: the R61505V is not selected and not accessible.	IOVCC																																																																																																																						
RS	I	Host processor	Register select signal. Amplitude: IOVCC-GND Low: select Index register High: select control register	IOVCC																																																																																																																						
WRX/SCL	I	Host processor	Write strobe signal in 80-system bus interface operation and enables write operation when WRX is low. Synchronous clock signal (SCL) in serial interface operation. Amplitude: IOVCC-GND	IOVCC																																																																																																																						
RDX	I	Host processor	Read strobe signal in 80-system bus interface operation and enables read operation when RDX is low. Amplitude: IOVCC-GND	IOVCC																																																																																																																						
SDI	I	Host processor	Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal. Amplitude: IOVCC-GND	GND or IOVCC																																																																																																																						
SDO	O	Host processor	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. Amplitude: IOVCC-GND	Open																																																																																																																						

Signal	I/O	Connect to	Function	When not in use
DB0-DB17	I/O	Host processor	18-bit parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVCC-GND). 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation (Amplitude: IOVCC-GND). 16-bit I/F: DB17-DB13 and DB11-1 are used. 18-bit I/F: DB17-DB0 are used.	GND or IOVCC
ENABLE	I	Host processor	Data enable signal for RGB interface operation. (Amplitude: IOVCC-GND). Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit. (Amplitude: IOVCC-GND) .	GND or IOVCC
VSYNC	I	Host processor	Frame synchronous signal for RGB interface operation. Low active. (Amplitude: IOVCC-GND).	GND or IOVCC
HSYNC	I	Host processor	Line synchronous signal for RGB interface operation. Low active. (Amplitude: IOVCC-GND).	GND or IOVCC
DOTCLK	I	Host processor	Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. (Amplitude: IOVCC-GND).	GND or IOVCC
FMARK	O	Host processor	Frame head pulse signal, which is used when writing data to the internal RAM. (Amplitude: IOVCC-GND).	Open

Table 10 Reset, Internal oscillation

Signal	I/O	Connect to	Function	When not in use
RESETX	I	Host processor or external circuit	Reset signal. The R61505V is initialized when this signal is at low level. Make sure to execute a power-on reset when turning on power supply (Amplitude: IOVCC-GND).	-

Table 11 Power supply

Signal	I/O	Connect to	Function	When not in use
VCC	-	Power supply	Power supply to internal logic regulator circuit.	-
GND	-	Power supply	Internal logic GND.	-
VDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.	-
IOVCC	-	Power supply	Power supply to the interface pins: RESETX, CSX, WRX, RDX, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.	-
AGND	-	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit). In case of COG, connect to GND on the FPC to prevent noise.	-
VCI	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply VCI.	-
VCILVL	I	Reference power supply	VCILVL must be at the same electrical potential as VCI. Connect to external power supply. In case of COG, connect to VCI on the FPC to prevent noise.	-
VPP1	I	Power supply or open	Internal NVM power supply. See "NVM Control Sequence" for voltages applied to VPP1, 2 and 3A pins.	Open
VPP2	I	Power supply or open		Open
VPP3A	I	Power supply or open		AGND

Table 12 Step-up circuit

Signal	I/O	Connect to	Function	When not in use
VCI1	I/O	Stabilizing capacitor	Reference voltage of step-up circuit 1. Define the voltage so that DDVDH, VGH and VGL do not exceed the ratings.	-
DDVDH	O	Stabilizing capacitor	Power supply for the source driver liquid crystal drive unit and VCOM drive which is generated from VCI1 and output from internal step-up circuit 1. The step-up factor is 2. Make sure to connect to stabilizing capacitor.	-
VGH	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply which is generated from VCI1 and DDVDH and output from internal step-up circuit 2. The step-up factor is set by BT bit. Make sure to connect to stabilizing capacitor.	-
VGL	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply which is generated from VCI1 and DDVDH and output from internal step-up circuit 2. The step-up factor is set by BT bit. Make sure to connect to stabilizing capacitor.	-
VCL	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor.	-
C11P, C11M C12P, C12M	I/ O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C13P, C13M, C21P, C21M, C22P, C22M	I/ O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-

Table 13 LCD drive

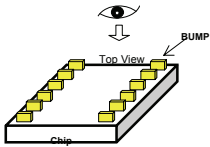
Signal	I/O	Connect to	Function	When not in use
VREG1 OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCILVL or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for (1) source driver grayscale reference voltage, (2) VCOMH level reference voltage, and (3) VCOM amplitude reference voltage. Make sure to connect to a stabilizing capacitor when in use.	-
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.	-
VCOMH	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by either external resistor (VCOMR) or electronic volume. Make sure to connect to stabilizing capacitor.	-
VCOML	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). Make sure to connect to stabilizing capacitor.	-
VCOMR	I	Variable resistor or open	Connect a variable resistor when adjusting the VCOMH level between VREG1OUT and GND.	Open
VGS	I	GND	Reference level for the grayscale voltage generating circuit.	-
S1~S720	O	LCD	Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S720.	-
G1~G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level	-

Table 14 Others (test and dummy pins)

Signal	I/O	Connect to	Function	When not in use
VTEST	O	Open	Test pin. Leave open.	Open
VREFC	I	GND	Test pin. Make sure to fix to the GND level.	-
VREFD	O	Open	Test pin. Leave open.	Open
VREF	O	Open	Test pin. Leave open.	Open
VDDTEST	I	GND	Test pin. Make sure to fix to the GND level.	-
VMON	O	Open	Test pin. Leave open.	Open
VCIR	O	Open	Test pin. Leave open.	Open
GNDDUM 1-6, AGNDDUM 1-7, IOVCCDUM	O	-	Connect unused interface and test pins to these pins on the glass to fix voltage levels. Leave open when not used.	Open
DUMMYR 1-6	-	-	Short-circuited within the chip for COG contact resistance measurement. DUMMYR pins are short-circuited as below: DUMMYR1 and DUMMYR6 DUMMYR2 and DUMMYR5 DUMMYR3 and DUMMYR4	Open
VGLDMY 1-4	O	Unused gate lines	Connect unused gate lines to fix the level at VGL.	Open
TESTO 1-14	O	-	Dummy pads. Leave open.	Open
TEST 1~5	I	GND	Test pin. Connect to GND.	GND
TSC	I	GND	Test pin. Connect to GND.	GND
TS0-8	O	Open	Test pin. Leave open.	Open
VPP3B, VPP3C	I	AGND	Test pin. Connect to AGND.	AGND
TEVC12	O	Open	Test pin. Leave open.	Open

Patents of dummy pins used to fix pin to VCC or GND are granted as below:

PATENT ISSUED: United States Patent No. 6,323,930 No. 6,924,868
Korean Patent No. 401,270
Taiwanese Patent No. 175,413
Japanese Patent No. 3,980,066



No.	Pin Name
1	AGNDUM1
2	DUMMYR1
3	DUMMYR2
4	VPP1
5	VPP1
6	VPP1
7	VPP2
8	VPP2
9	VPP2
10	VPP2
11	VPP2
12	VPP2A
13	VPP2B
14	VPP2B
15	VPP2B
16	VPP2C
17	VPP2C
18	AGND
19	AGND
20	AGND
21	AGND
22	AGND
23	GND
24	GND
25	GND
26	GND
27	GND
28	DUMMYR3
29	DUMMYR4
30	AGNDUM1
31	BM1
32	BM1
33	BM2
34	BM2
35	IOVCCDUM
36	TEST3
37	TEST4
38	TEST3
39	TEST2
40	TEST1
41	AGNDUM2
42	FMARK
43	VSINCO
44	VSINCO
45	DOTCLK
46	ENABLE
47	AGNDUM2
48	DB17
49	DB16
50	DB15
51	TS8
52	TS7
53	DB14
54	DB13
55	DB12
56	TS6
57	TS5
58	DB11
59	DB10
60	DB9
61	IOVCC
62	IOVCC
63	IOVCC
64	IOVCC
65	IOVCC
66	IOVCC
67	IOVCC
68	IOVCC
69	DB8
70	DB7
71	DB6
72	TS4
73	TS3
74	DB5
75	DB4
76	DB3
77	TS2
78	TS1
79	DB2
80	DB1
81	DB0
82	TS0
83	TS0
84	AGNDUM3
85	CSX
86	RS
87	WRX/SQL
88	RDY
89	RESETX
90	SDO
91	SDI
92	AGNDUM4
93	VTEST
94	VREF
95	VREFD
96	VREFC
97	VDDTEST
98	AGNDUM5
99	VCC
100	VCC
101	VCC
102	VCC
103	VCC
104	VCC
105	VCC
106	VCC
107	VCC
108	VCC
109	VCC
110	VCC
111	VCC
112	VCC
113	GND
114	GND
115	GND
116	GND
117	GND
118	GND
119	GND
120	GND
121	VGS
122	AGND
123	AGND
124	AGND
125	AGND
126	AGND
127	AGND
128	AGND
129	AGND
130	VCOMH
131	VCOMH
132	VCOMH
133	VCOMH
134	VCOMH
135	VCOMH
136	VCOM
137	VCOM
138	VCOM
139	VCOM
140	VCOM
141	VCOM
142	VCOML
143	VCOML
144	VCOML
145	VCOML
146	VCOML
147	VCOML
148	VCOML
149	C11M
150	C11M
151	C11M
152	C11M
153	C11M
154	C11P
155	C11P
156	C11P
157	C11P
158	C11P
159	C12M
160	C12M
161	C12M
162	C12M
163	C12M
164	C12P
165	C12P
166	C12P
167	C12P
168	C12P
169	DOVDH
170	DOVDH
171	DOVDH
172	DOVDH
173	DOVDH
174	DOVDH
175	DOVDH
176	DOVDH
177	DOVDH
178	DOVDH
179	VQIR
180	VREG1OUT
181	VCOMR
182	VMON
183	AGNDUM6
184	AGNDUM6
185	VCI1
186	VCI1
187	VCI1
188	VCI1
189	VCI1
190	VCI1
191	VCI1
192	VCI1
193	VCI1
194	VCI1
195	VCI1
196	VCI1
197	VCI1
198	VCI1
199	VCI1
200	VCI1
201	VGLVL
202	AGNDUM7
203	VGH
204	VGH
205	VGH
206	VGH
207	VGH
208	VGH
209	AGNDUM8
210	VGL
211	VGL
212	VGL
213	VGL
214	VGL
215	VGL
216	VGL
217	VGL
218	VGL
219	VGL
220	AGNDUM9
221	VGL
222	VGL
223	VGL
224	VGL
225	C13P
226	C13P
227	C13P
228	C13P
229	C13M
230	C13M
231	C13M
232	C13M
233	GND
234	GND
235	GND
236	GND
237	GND
238	AGND
239	AGND
240	AGND
241	AGND
242	AGND
243	C21P
244	C21P
245	C21P
246	C21M
247	C21M
248	C21M
249	C22P
250	C22P
251	C22P
252	C22M
253	C22M
254	C22M
255	TEVC2
256	TEVC2
257	TEVC2
258	TEVC2
259	TEVC2
260	AGNDUM10

(Rev.0.20)

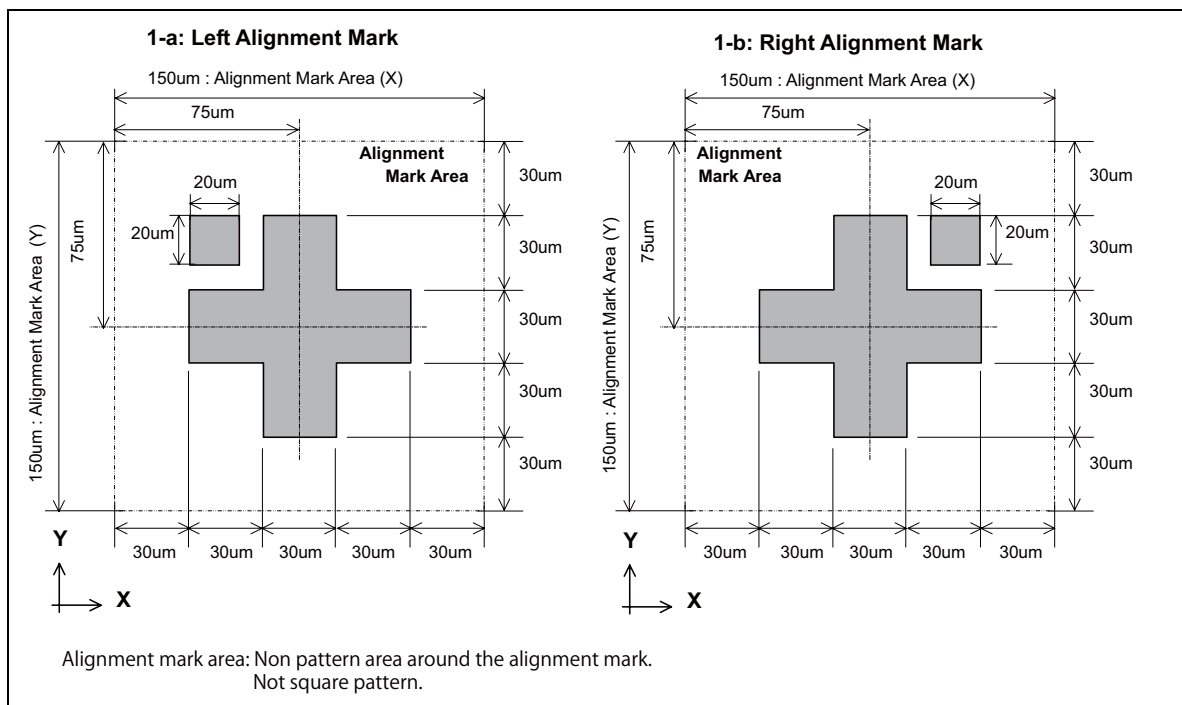
Rev	Date	Changes
0.00	2007.9.14	First issue
0.10	2007.9.20	Pin name changed, VCC2 -> TEVC2
0.20	2008.2.5	Pin name changed, BM1, BM2 -> BM0

Pin Name
TEST014
TEST013
DUMMYR8
DUMMYR9
VGLDUMY4
G2
G4
G6
G8
G316
G318
G320
VGLDUMY3
TEST012
TEST011
TEST010
S1
S2
S3
S4
S358
S359
S360
TEST09
S361
S362
S363
TEST08
S717
S718
S719
S720
TEST07
TEST06
TEST05
VGLDUMY2
G319
G317
G315
G7
G5
G3
G1
VGLDUMY1
TEST04
TEST03
TEST02
TEST01

- Chip size: 18.80mm x 0.77mm
- Chip thickness: 280μm (typ.)
- Pad coordinates: Pad center
- Pad coordinates: Chip center
- Au bump size:
 1. 50μm x 80μm (I/O)
 2. 16μm x 94μm (Output to liquid crystal)
- Au bump pitch: See “Bump Arrangement”
- Au bump height: 12 μm

Table 15 Alignment Mark

Alignment Mark shape		X	Y
Type A	(1-a)	-9266	-251
	(1-b)	9266	-251

**Figure 2 Alignment Mark**

Rev	Date	Contents of modification
0	2007.9.14	First issue
0.1	2007.9.20	Change the pin name (VCI2 → TEVCI2).
1.0	2007.10.20	Fix coordinates.
1.1	2008. 2. 5.	Pin name changed. IM0/ID → IM0

pad No	pad name	X	Y	pad No	pad name	X	Y
1	AGNDDUM1	-9065	-281	51	TS8	-5565	-281
2	DUMMYR1	-8995	-281	52	TS7	-5495	-281
3	DUMMYR2	-8925	-281	53	DB14	-5425	-281
4	VPP1	-8855	-281	54	DB13	-5355	-281
5	VPP1	-8785	-281	55	DB12	-5285	-281
6	VPP1	-8715	-281	56	TS6	-5215	-281
7	VPP2	-8645	-281	57	TS5	-5145	-281
8	VPP2	-8575	-281	58	DB11	-5075	-281
9	VPP2	-8505	-281	59	DB10	-5005	-281
10	VPP2	-8435	-281	60	DB9	-4935	-281
11	VPP2	-8365	-281	61	IOVCC	-4865	-281
12	VPP3A	-8295	-281	62	IOVCC	-4795	-281
13	VPP3A	-8225	-281	63	IOVCC	-4725	-281
14	VPP3B	-8155	-281	64	IOVCC	-4655	-281
15	VPP3B	-8085	-281	65	IOVCC	-4585	-281
16	VPP3C	-8015	-281	66	IOVCC	-4515	-281
17	VPP3C	-7945	-281	67	IOVCC	-4445	-281
18	AGND	-7875	-281	68	IOVCC	-4375	-281
19	AGND	-7805	-281	69	DB8	-4305	-281
20	AGND	-7735	-281	70	DB7	-4235	-281
21	AGND	-7665	-281	71	DB6	-4165	-281
22	AGND	-7595	-281	72	TS4	-4095	-281
23	GND	-7525	-281	73	TS3	-4025	-281
24	GND	-7455	-281	74	DB5	-3955	-281
25	GND	-7385	-281	75	DB4	-3885	-281
26	GND	-7315	-281	76	DB3	-3815	-281
27	GND	-7245	-281	77	TS2	-3745	-281
28	DUMMYR3	-7175	-281	78	TS1	-3675	-281
29	DUMMYR4	-7105	-281	79	DB2	-3605	-281
30	GNDDUM1	-7035	-281	80	DB1	-3535	-281
31	IM0	-6965	-281	81	DB0	-3465	-281
32	IM1	-6895	-281	82	TS0	-3395	-281
33	IM2	-6825	-281	83	TSC	-3325	-281
34	IM3	-6755	-281	84	GNDDUM4	-3255	-281
35	IOVCCDUM	-6685	-281	85	CSX	-3185	-281
36	TEST5	-6615	-281	86	RS	-3115	-281
37	TEST4	-6545	-281	87	WRX/SCL	-3045	-281
38	TEST3	-6475	-281	88	RDX	-2975	-281
39	TEST2	-6405	-281	89	RESETX	-2905	-281
40	TEST1	-6335	-281	90	SDO	-2835	-281
41	GNDDUM2	-6265	-281	91	SDI	-2765	-281
42	FMARK	-6195	-281	92	GNDDUM5	-2695	-281
43	VSYNC	-6125	-281	93	VTEST	-2625	-281
44	HSYNC	-6055	-281	94	VREF	-2555	-281
45	DOTCLK	-5985	-281	95	VREFD	-2485	-281
46	ENABLE	-5915	-281	96	VREFC	-2415	-281
47	GNDDUM3	-5845	-281	97	VDDTEST	-2345	-281
48	DB17	-5775	-281	98	GNDDUM6	-2275	-281
49	DB16	-5705	-281	99	VCC	-2205	-281
50	DB15	-5635	-281	100	VCC	-2135	-281

pad No	pad name	X	Y	pad No	pad name	X	Y
101	VCC	-2065	-281	151	C11M	1435	-281
102	VCC	-1995	-281	152	C11M	1505	-281
103	VCC	-1925	-281	153	C11M	1575	-281
104	VCC	-1855	-281	154	C11P	1645	-281
105	VDD	-1785	-281	155	C11P	1715	-281
106	VDD	-1715	-281	156	C11P	1785	-281
107	VDD	-1645	-281	157	C11P	1855	-281
108	VDD	-1575	-281	158	C11P	1925	-281
109	VDD	-1505	-281	159	C12M	1995	-281
110	VDD	-1435	-281	160	C12M	2065	-281
111	VDD	-1365	-281	161	C12M	2135	-281
112	VDD	-1295	-281	162	C12M	2205	-281
113	GND	-1225	-281	163	C12M	2275	-281
114	GND	-1155	-281	164	C12P	2345	-281
115	GND	-1085	-281	165	C12P	2415	-281
116	GND	-1015	-281	166	C12P	2485	-281
117	GND	-945	-281	167	C12P	2555	-281
118	GND	-875	-281	168	C12P	2625	-281
119	GND	-805	-281	169	DDVDH	2695	-281
120	GND	-735	-281	170	DDVDH	2765	-281
121	VGS	-665	-281	171	DDVDH	2835	-281
122	AGND	-595	-281	172	DDVDH	2905	-281
123	AGND	-525	-281	173	DDVDH	2975	-281
124	AGND	-455	-281	174	DDVDH	3045	-281
125	AGND	-385	-281	175	DDVDH	3115	-281
126	AGND	-315	-281	176	DDVDH	3185	-281
127	AGND	-245	-281	177	DDVDH	3255	-281
128	AGND	-175	-281	178	DDVDH	3325	-281
129	AGND	-105	-281	179	VCIR	3395	-281
130	VCOMH	-35	-281	180	VREG1OUT	3465	-281
131	VCOMH	35	-281	181	VCOMR	3535	-281
132	VCOMH	105	-281	182	VMON	3605	-281
133	VCOMH	175	-281	183	AGNDDUM2	3675	-281
134	VCOMH	245	-281	184	AGNDDUM3	3745	-281
135	VCOMH	315	-281	185	VCI1	3815	-281
136	VCOM	385	-281	186	VCI1	3885	-281
137	VCOM	455	-281	187	VCI1	3955	-281
138	VCOM	525	-281	188	VCI1	4025	-281
139	VCOM	595	-281	189	VCI1	4095	-281
140	VCOM	665	-281	190	VCI1	4165	-281
141	VCOM	735	-281	191	VCI1	4235	-281
142	VCOML	805	-281	192	VCI1	4305	-281
143	VCOML	875	-281	193	VCI	4375	-281
144	VCOML	945	-281	194	VCI	4445	-281
145	VCOML	1015	-281	195	VCI	4515	-281
146	VCOML	1085	-281	196	VCI	4585	-281
147	VCOML	1155	-281	197	VCI	4655	-281
148	VCOML	1225	-281	198	VCI	4725	-281
149	C11M	1295	-281	199	VCI	4795	-281
150	C11M	1365	-281	200	VCI	4865	-281

pad No	pad name	X	Y	pad No	pad name	X	Y
201	VCILVL	4935	-281	251	C22P	8435	-281
202	AGNDDUM4	5005	-281	252	C22M	8505	-281
203	VGH	5075	-281	253	C22M	8575	-281
204	VGH	5145	-281	254	C22M	8645	-281
205	VGH	5215	-281	255	TEVCI2	8715	-281
206	VGH	5285	-281	256	TEVCI2	8785	-281
207	VGH	5355	-281	257	TEVCI2	8855	-281
208	VGH	5425	-281	258	TEVCI2	8925	-281
209	AGNDDUM5	5495	-281	259	TEVCI2	8995	-281
210	VGL	5565	-281	260	AGNDDUM7	9065	-281
211	VGL	5635	-281	261	TESTO1	9216	279
212	VGL	5705	-281	262	TESTO2	9200	166
213	VGL	5775	-281	263	TESTO3	9184	279
214	VGL	5845	-281	264	TESTO4	9168	166
215	VGL	5915	-281	265	VGLDMY1	9152	279
216	VGL	5985	-281	266	G1	9136	166
217	VGL	6055	-281	267	G3	9120	279
218	VGL	6125	-281	268	G5	9104	166
219	VGL	6195	-281	269	G7	9088	279
220	AGNDDUM6	6265	-281	270	G9	9072	166
221	VCL	6335	-281	271	G11	9056	279
222	VCL	6405	-281	272	G13	9040	166
223	VCL	6475	-281	273	G15	9024	279
224	VCL	6545	-281	274	G17	9008	166
225	C13P	6615	-281	275	G19	8992	279
226	C13P	6685	-281	276	G21	8976	166
227	C13P	6755	-281	277	G23	8960	279
228	C13P	6825	-281	278	G25	8944	166
229	C13M	6895	-281	279	G27	8928	279
230	C13M	6965	-281	280	G29	8912	166
231	C13M	7035	-281	281	G31	8896	279
232	C13M	7105	-281	282	G33	8880	166
233	GND	7175	-281	283	G35	8864	279
234	GND	7245	-281	284	G37	8848	166
235	GND	7315	-281	285	G39	8832	279
236	GND	7385	-281	286	G41	8816	166
237	GND	7455	-281	287	G43	8800	279
238	AGND	7525	-281	288	G45	8784	166
239	AGND	7595	-281	289	G47	8768	279
240	AGND	7665	-281	290	G49	8752	166
241	AGND	7735	-281	291	G51	8736	279
242	AGND	7805	-281	292	G53	8720	166
243	C21P	7875	-281	293	G55	8704	279
244	C21P	7945	-281	294	G57	8688	166
245	C21P	8015	-281	295	G59	8672	279
246	C21M	8085	-281	296	G61	8656	166
247	C21M	8155	-281	297	G63	8640	279
248	C21M	8225	-281	298	G65	8624	166
249	C22P	8295	-281	299	G67	8608	279
250	C22P	8365	-281	300	G69	8592	166

pad No	pad name	X	Y	pad No	pad name	X	Y
301	G71	8576	279	351	G171	7776	279
302	G73	8560	166	352	G173	7760	166
303	G75	8544	279	353	G175	7744	279
304	G77	8528	166	354	G177	7728	166
305	G79	8512	279	355	G179	7712	279
306	G81	8496	166	356	G181	7696	166
307	G83	8480	279	357	G183	7680	279
308	G85	8464	166	358	G185	7664	166
309	G87	8448	279	359	G187	7648	279
310	G89	8432	166	360	G189	7632	166
311	G91	8416	279	361	G191	7616	279
312	G93	8400	166	362	G193	7600	166
313	G95	8384	279	363	G195	7584	279
314	G97	8368	166	364	G197	7568	166
315	G99	8352	279	365	G199	7552	279
316	G101	8336	166	366	G201	7536	166
317	G103	8320	279	367	G203	7520	279
318	G105	8304	166	368	G205	7504	166
319	G107	8288	279	369	G207	7488	279
320	G109	8272	166	370	G209	7472	166
321	G111	8256	279	371	G211	7456	279
322	G113	8240	166	372	G213	7440	166
323	G115	8224	279	373	G215	7424	279
324	G117	8208	166	374	G217	7408	166
325	G119	8192	279	375	G219	7392	279
326	G121	8176	166	376	G221	7376	166
327	G123	8160	279	377	G223	7360	279
328	G125	8144	166	378	G225	7344	166
329	G127	8128	279	379	G227	7328	279
330	G129	8112	166	380	G229	7312	166
331	G131	8096	279	381	G231	7296	279
332	G133	8080	166	382	G233	7280	166
333	G135	8064	279	383	G235	7264	279
334	G137	8048	166	384	G237	7248	166
335	G139	8032	279	385	G239	7232	279
336	G141	8016	166	386	G241	7216	166
337	G143	8000	279	387	G243	7200	279
338	G145	7984	166	388	G245	7184	166
339	G147	7968	279	389	G247	7168	279
340	G149	7952	166	390	G249	7152	166
341	G151	7936	279	391	G251	7136	279
342	G153	7920	166	392	G253	7120	166
343	G155	7904	279	393	G255	7104	279
344	G157	7888	166	394	G257	7088	166
345	G159	7872	279	395	G259	7072	279
346	G161	7856	166	396	G261	7056	166
347	G163	7840	279	397	G263	7040	279
348	G165	7824	166	398	G265	7024	166
349	G167	7808	279	399	G267	7008	279
350	G169	7792	166	400	G269	6992	166

pad No	pad name	X	Y	pad No	pad name	X	Y
401	G271	6976	279	451	S699	6000	166
402	G273	6960	166	452	S698	5984	279
403	G275	6944	279	453	S697	5968	166
404	G277	6928	166	454	S696	5952	279
405	G279	6912	279	455	S695	5936	166
406	G281	6896	166	456	S694	5920	279
407	G283	6880	279	457	S693	5904	166
408	G285	6864	166	458	S692	5888	279
409	G287	6848	279	459	S691	5872	166
410	G289	6832	166	460	S690	5856	279
411	G291	6816	279	461	S689	5840	166
412	G293	6800	166	462	S688	5824	279
413	G295	6784	279	463	S687	5808	166
414	G297	6768	166	464	S686	5792	279
415	G299	6752	279	465	S685	5776	166
416	G301	6736	166	466	S684	5760	279
417	G303	6720	279	467	S683	5744	166
418	G305	6704	166	468	S682	5728	279
419	G307	6688	279	469	S681	5712	166
420	G309	6672	166	470	S680	5696	279
421	G311	6656	279	471	S679	5680	166
422	G313	6640	166	472	S678	5664	279
423	G315	6624	279	473	S677	5648	166
424	G317	6608	166	474	S676	5632	279
425	G319	6592	279	475	S675	5616	166
426	VGLDMY2	6576	166	476	S674	5600	279
427	TESTO5	6560	279	477	S673	5584	166
428	TESTO6	6368	279	478	S672	5568	279
429	TESTO7	6352	166	479	S671	5552	166
430	S720	6336	279	480	S670	5536	279
431	S719	6320	166	481	S669	5520	166
432	S718	6304	279	482	S668	5504	279
433	S717	6288	166	483	S667	5488	166
434	S716	6272	279	484	S666	5472	279
435	S715	6256	166	485	S665	5456	166
436	S714	6240	279	486	S664	5440	279
437	S713	6224	166	487	S663	5424	166
438	S712	6208	279	488	S662	5408	279
439	S711	6192	166	489	S661	5392	166
440	S710	6176	279	490	S660	5376	279
441	S709	6160	166	491	S659	5360	166
442	S708	6144	279	492	S658	5344	279
443	S707	6128	166	493	S657	5328	166
444	S706	6112	279	494	S656	5312	279
445	S705	6096	166	495	S655	5296	166
446	S704	6080	279	496	S654	5280	279
447	S703	6064	166	497	S653	5264	166
448	S702	6048	279	498	S652	5248	279
449	S701	6032	166	499	S651	5232	166
450	S700	6016	279	500	S650	5216	279

pad No	pad name	X	Y	pad No	pad name	X	Y
501	S649	5200	166	551	S599	4400	166
502	S648	5184	279	552	S598	4384	279
503	S647	5168	166	553	S597	4368	166
504	S646	5152	279	554	S596	4352	279
505	S645	5136	166	555	S595	4336	166
506	S644	5120	279	556	S594	4320	279
507	S643	5104	166	557	S593	4304	166
508	S642	5088	279	558	S592	4288	279
509	S641	5072	166	559	S591	4272	166
510	S640	5056	279	560	S590	4256	279
511	S639	5040	166	561	S589	4240	166
512	S638	5024	279	562	S588	4224	279
513	S637	5008	166	563	S587	4208	166
514	S636	4992	279	564	S586	4192	279
515	S635	4976	166	565	S585	4176	166
516	S634	4960	279	566	S584	4160	279
517	S633	4944	166	567	S583	4144	166
518	S632	4928	279	568	S582	4128	279
519	S631	4912	166	569	S581	4112	166
520	S630	4896	279	570	S580	4096	279
521	S629	4880	166	571	S579	4080	166
522	S628	4864	279	572	S578	4064	279
523	S627	4848	166	573	S577	4048	166
524	S626	4832	279	574	S576	4032	279
525	S625	4816	166	575	S575	4016	166
526	S624	4800	279	576	S574	4000	279
527	S623	4784	166	577	S573	3984	166
528	S622	4768	279	578	S572	3968	279
529	S621	4752	166	579	S571	3952	166
530	S620	4736	279	580	S570	3936	279
531	S619	4720	166	581	S569	3920	166
532	S618	4704	279	582	S568	3904	279
533	S617	4688	166	583	S567	3888	166
534	S616	4672	279	584	S566	3872	279
535	S615	4656	166	585	S565	3856	166
536	S614	4640	279	586	S564	3840	279
537	S613	4624	166	587	S563	3824	166
538	S612	4608	279	588	S562	3808	279
539	S611	4592	166	589	S561	3792	166
540	S610	4576	279	590	S560	3776	279
541	S609	4560	166	591	S559	3760	166
542	S608	4544	279	592	S558	3744	279
543	S607	4528	166	593	S557	3728	166
544	S606	4512	279	594	S556	3712	279
545	S605	4496	166	595	S555	3696	166
546	S604	4480	279	596	S554	3680	279
547	S603	4464	166	597	S553	3664	166
548	S602	4448	279	598	S552	3648	279
549	S601	4432	166	599	S551	3632	166
550	S600	4416	279	600	S550	3616	279

pad No	pad name	X	Y	pad No	pad name	X	Y
601	S549	3600	166	651	S499	2800	166
602	S548	3584	279	652	S498	2784	279
603	S547	3568	166	653	S497	2768	166
604	S546	3552	279	654	S496	2752	279
605	S545	3536	166	655	S495	2736	166
606	S544	3520	279	656	S494	2720	279
607	S543	3504	166	657	S493	2704	166
608	S542	3488	279	658	S492	2688	279
609	S541	3472	166	659	S491	2672	166
610	S540	3456	279	660	S490	2656	279
611	S539	3440	166	661	S489	2640	166
612	S538	3424	279	662	S488	2624	279
613	S537	3408	166	663	S487	2608	166
614	S536	3392	279	664	S486	2592	279
615	S535	3376	166	665	S485	2576	166
616	S534	3360	279	666	S484	2560	279
617	S533	3344	166	667	S483	2544	166
618	S532	3328	279	668	S482	2528	279
619	S531	3312	166	669	S481	2512	166
620	S530	3296	279	670	S480	2496	279
621	S529	3280	166	671	S479	2480	166
622	S528	3264	279	672	S478	2464	279
623	S527	3248	166	673	S477	2448	166
624	S526	3232	279	674	S476	2432	279
625	S525	3216	166	675	S475	2416	166
626	S524	3200	279	676	S474	2400	279
627	S523	3184	166	677	S473	2384	166
628	S522	3168	279	678	S472	2368	279
629	S521	3152	166	679	S471	2352	166
630	S520	3136	279	680	S470	2336	279
631	S519	3120	166	681	S469	2320	166
632	S518	3104	279	682	S468	2304	279
633	S517	3088	166	683	S467	2288	166
634	S516	3072	279	684	S466	2272	279
635	S515	3056	166	685	S465	2256	166
636	S514	3040	279	686	S464	2240	279
637	S513	3024	166	687	S463	2224	166
638	S512	3008	279	688	S462	2208	279
639	S511	2992	166	689	S461	2192	166
640	S510	2976	279	690	S460	2176	279
641	S509	2960	166	691	S459	2160	166
642	S508	2944	279	692	S458	2144	279
643	S507	2928	166	693	S457	2128	166
644	S506	2912	279	694	S456	2112	279
645	S505	2896	166	695	S455	2096	166
646	S504	2880	279	696	S454	2080	279
647	S503	2864	166	697	S453	2064	166
648	S502	2848	279	698	S452	2048	279
649	S501	2832	166	699	S451	2032	166
650	S500	2816	279	700	S450	2016	279

pad No	pad name	X	Y	pad No	pad name	X	Y
701	S449	2000	166	751	S399	1200	166
702	S448	1984	279	752	S398	1184	279
703	S447	1968	166	753	S397	1168	166
704	S446	1952	279	754	S396	1152	279
705	S445	1936	166	755	S395	1136	166
706	S444	1920	279	756	S394	1120	279
707	S443	1904	166	757	S393	1104	166
708	S442	1888	279	758	S392	1088	279
709	S441	1872	166	759	S391	1072	166
710	S440	1856	279	760	S390	1056	279
711	S439	1840	166	761	S389	1040	166
712	S438	1824	279	762	S388	1024	279
713	S437	1808	166	763	S387	1008	166
714	S436	1792	279	764	S386	992	279
715	S435	1776	166	765	S385	976	166
716	S434	1760	279	766	S384	960	279
717	S433	1744	166	767	S383	944	166
718	S432	1728	279	768	S382	928	279
719	S431	1712	166	769	S381	912	166
720	S430	1696	279	770	S380	896	279
721	S429	1680	166	771	S379	880	166
722	S428	1664	279	772	S378	864	279
723	S427	1648	166	773	S377	848	166
724	S426	1632	279	774	S376	832	279
725	S425	1616	166	775	S375	816	166
726	S424	1600	279	776	S374	800	279
727	S423	1584	166	777	S373	784	166
728	S422	1568	279	778	S372	768	279
729	S421	1552	166	779	S371	752	166
730	S420	1536	279	780	S370	736	279
731	S419	1520	166	781	S369	720	166
732	S418	1504	279	782	S368	704	279
733	S417	1488	166	783	S367	688	166
734	S416	1472	279	784	S366	672	279
735	S415	1456	166	785	S365	656	166
736	S414	1440	279	786	S364	640	279
737	S413	1424	166	787	S363	624	166
738	S412	1408	279	788	S362	608	279
739	S411	1392	166	789	S361	592	166
740	S410	1376	279	790	TEST08	576	279
741	S409	1360	166	791	TEST09	-576	166
742	S408	1344	279	792	S360	-592	279
743	S407	1328	166	793	S359	-608	166
744	S406	1312	279	794	S358	-624	279
745	S405	1296	166	795	S357	-640	166
746	S404	1280	279	796	S356	-656	279
747	S403	1264	166	797	S355	-672	166
748	S402	1248	279	798	S354	-688	279
749	S401	1232	166	799	S353	-704	166
750	S400	1216	279	800	S352	-720	279

pad No	pad name	X	Y	pad No	pad name	X	Y
801	S351	-736	166	851	S301	-1536	166
802	S350	-752	279	852	S300	-1552	279
803	S349	-768	166	853	S299	-1568	166
804	S348	-784	279	854	S298	-1584	279
805	S347	-800	166	855	S297	-1600	166
806	S346	-816	279	856	S296	-1616	279
807	S345	-832	166	857	S295	-1632	166
808	S344	-848	279	858	S294	-1648	279
809	S343	-864	166	859	S293	-1664	166
810	S342	-880	279	860	S292	-1680	279
811	S341	-896	166	861	S291	-1696	166
812	S340	-912	279	862	S290	-1712	279
813	S339	-928	166	863	S289	-1728	166
814	S338	-944	279	864	S288	-1744	279
815	S337	-960	166	865	S287	-1760	166
816	S336	-976	279	866	S286	-1776	279
817	S335	-992	166	867	S285	-1792	166
818	S334	-1008	279	868	S284	-1808	279
819	S333	-1024	166	869	S283	-1824	166
820	S332	-1040	279	870	S282	-1840	279
821	S331	-1056	166	871	S281	-1856	166
822	S330	-1072	279	872	S280	-1872	279
823	S329	-1088	166	873	S279	-1888	166
824	S328	-1104	279	874	S278	-1904	279
825	S327	-1120	166	875	S277	-1920	166
826	S326	-1136	279	876	S276	-1936	279
827	S325	-1152	166	877	S275	-1952	166
828	S324	-1168	279	878	S274	-1968	279
829	S323	-1184	166	879	S273	-1984	166
830	S322	-1200	279	880	S272	-2000	279
831	S321	-1216	166	881	S271	-2016	166
832	S320	-1232	279	882	S270	-2032	279
833	S319	-1248	166	883	S269	-2048	166
834	S318	-1264	279	884	S268	-2064	279
835	S317	-1280	166	885	S267	-2080	166
836	S316	-1296	279	886	S266	-2096	279
837	S315	-1312	166	887	S265	-2112	166
838	S314	-1328	279	888	S264	-2128	279
839	S313	-1344	166	889	S263	-2144	166
840	S312	-1360	279	890	S262	-2160	279
841	S311	-1376	166	891	S261	-2176	166
842	S310	-1392	279	892	S260	-2192	279
843	S309	-1408	166	893	S259	-2208	166
844	S308	-1424	279	894	S258	-2224	279
845	S307	-1440	166	895	S257	-2240	166
846	S306	-1456	279	896	S256	-2256	279
847	S305	-1472	166	897	S255	-2272	166
848	S304	-1488	279	898	S254	-2288	279
849	S303	-1504	166	899	S253	-2304	166
850	S302	-1520	279	900	S252	-2320	279

pad No	pad name	X	Y	pad No	pad name	X	Y
901	S251	-2336	166	951	S201	-3136	166
902	S250	-2352	279	952	S200	-3152	279
903	S249	-2368	166	953	S199	-3168	166
904	S248	-2384	279	954	S198	-3184	279
905	S247	-2400	166	955	S197	-3200	166
906	S246	-2416	279	956	S196	-3216	279
907	S245	-2432	166	957	S195	-3232	166
908	S244	-2448	279	958	S194	-3248	279
909	S243	-2464	166	959	S193	-3264	166
910	S242	-2480	279	960	S192	-3280	279
911	S241	-2496	166	961	S191	-3296	166
912	S240	-2512	279	962	S190	-3312	279
913	S239	-2528	166	963	S189	-3328	166
914	S238	-2544	279	964	S188	-3344	279
915	S237	-2560	166	965	S187	-3360	166
916	S236	-2576	279	966	S186	-3376	279
917	S235	-2592	166	967	S185	-3392	166
918	S234	-2608	279	968	S184	-3408	279
919	S233	-2624	166	969	S183	-3424	166
920	S232	-2640	279	970	S182	-3440	279
921	S231	-2656	166	971	S181	-3456	166
922	S230	-2672	279	972	S180	-3472	279
923	S229	-2688	166	973	S179	-3488	166
924	S228	-2704	279	974	S178	-3504	279
925	S227	-2720	166	975	S177	-3520	166
926	S226	-2736	279	976	S176	-3536	279
927	S225	-2752	166	977	S175	-3552	166
928	S224	-2768	279	978	S174	-3568	279
929	S223	-2784	166	979	S173	-3584	166
930	S222	-2800	279	980	S172	-3600	279
931	S221	-2816	166	981	S171	-3616	166
932	S220	-2832	279	982	S170	-3632	279
933	S219	-2848	166	983	S169	-3648	166
934	S218	-2864	279	984	S168	-3664	279
935	S217	-2880	166	985	S167	-3680	166
936	S216	-2896	279	986	S166	-3696	279
937	S215	-2912	166	987	S165	-3712	166
938	S214	-2928	279	988	S164	-3728	279
939	S213	-2944	166	989	S163	-3744	166
940	S212	-2960	279	990	S162	-3760	279
941	S211	-2976	166	991	S161	-3776	166
942	S210	-2992	279	992	S160	-3792	279
943	S209	-3008	166	993	S159	-3808	166
944	S208	-3024	279	994	S158	-3824	279
945	S207	-3040	166	995	S157	-3840	166
946	S206	-3056	279	996	S156	-3856	279
947	S205	-3072	166	997	S155	-3872	166
948	S204	-3088	279	998	S154	-3888	279
949	S203	-3104	166	999	S153	-3904	166
950	S202	-3120	279	1000	S152	-3920	279

pad No	pad name	X	Y	pad No	pad name	X	Y
1001	S151	-3936	166	1051	S101	-4736	166
1002	S150	-3952	279	1052	S100	-4752	279
1003	S149	-3968	166	1053	S99	-4768	166
1004	S148	-3984	279	1054	S98	-4784	279
1005	S147	-4000	166	1055	S97	-4800	166
1006	S146	-4016	279	1056	S96	-4816	279
1007	S145	-4032	166	1057	S95	-4832	166
1008	S144	-4048	279	1058	S94	-4848	279
1009	S143	-4064	166	1059	S93	-4864	166
1010	S142	-4080	279	1060	S92	-4880	279
1011	S141	-4096	166	1061	S91	-4896	166
1012	S140	-4112	279	1062	S90	-4912	279
1013	S139	-4128	166	1063	S89	-4928	166
1014	S138	-4144	279	1064	S88	-4944	279
1015	S137	-4160	166	1065	S87	-4960	166
1016	S136	-4176	279	1066	S86	-4976	279
1017	S135	-4192	166	1067	S85	-4992	166
1018	S134	-4208	279	1068	S84	-5008	279
1019	S133	-4224	166	1069	S83	-5024	166
1020	S132	-4240	279	1070	S82	-5040	279
1021	S131	-4256	166	1071	S81	-5056	166
1022	S130	-4272	279	1072	S80	-5072	279
1023	S129	-4288	166	1073	S79	-5088	166
1024	S128	-4304	279	1074	S78	-5104	279
1025	S127	-4320	166	1075	S77	-5120	166
1026	S126	-4336	279	1076	S76	-5136	279
1027	S125	-4352	166	1077	S75	-5152	166
1028	S124	-4368	279	1078	S74	-5168	279
1029	S123	-4384	166	1079	S73	-5184	166
1030	S122	-4400	279	1080	S72	-5200	279
1031	S121	-4416	166	1081	S71	-5216	166
1032	S120	-4432	279	1082	S70	-5232	279
1033	S119	-4448	166	1083	S69	-5248	166
1034	S118	-4464	279	1084	S68	-5264	279
1035	S117	-4480	166	1085	S67	-5280	166
1036	S116	-4496	279	1086	S66	-5296	279
1037	S115	-4512	166	1087	S65	-5312	166
1038	S114	-4528	279	1088	S64	-5328	279
1039	S113	-4544	166	1089	S63	-5344	166
1040	S112	-4560	279	1090	S62	-5360	279
1041	S111	-4576	166	1091	S61	-5376	166
1042	S110	-4592	279	1092	S60	-5392	279
1043	S109	-4608	166	1093	S59	-5408	166
1044	S108	-4624	279	1094	S58	-5424	279
1045	S107	-4640	166	1095	S57	-5440	166
1046	S106	-4656	279	1096	S56	-5456	279
1047	S105	-4672	166	1097	S55	-5472	166
1048	S104	-4688	279	1098	S54	-5488	279
1049	S103	-4704	166	1099	S53	-5504	166
1050	S102	-4720	279	1100	S52	-5520	279

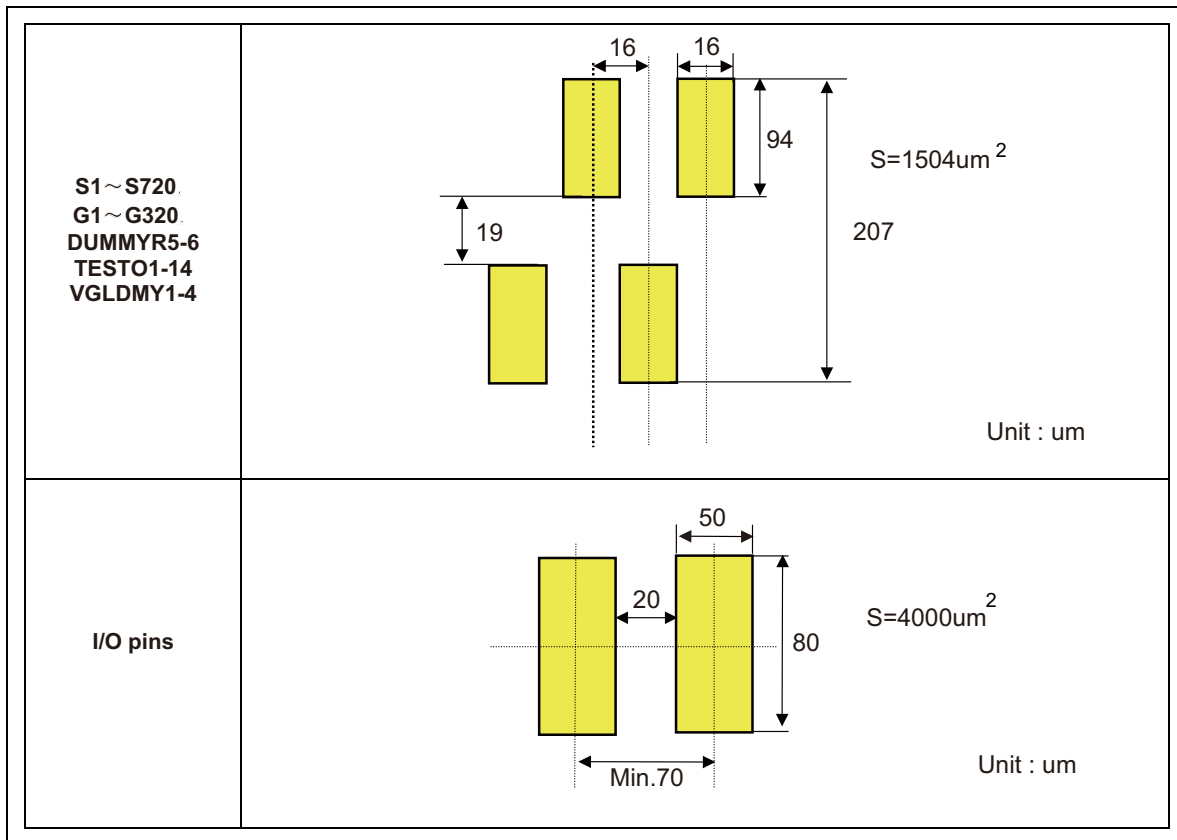
pad No	pad name	X	Y	pad No	pad name	X	Y
1101	S51	-5536	166	1151	S1	-6336	166
1102	S50	-5552	279	1152	TESTO10	-6352	279
1103	S49	-5568	166	1153	TESTO11	-6368	166
1104	S48	-5584	279	1154	TESTO12	-6560	279
1105	S47	-5600	166	1155	VGLDMY3	-6576	166
1106	S46	-5616	279	1156	G320	-6592	279
1107	S45	-5632	166	1157	G318	-6608	166
1108	S44	-5648	279	1158	G316	-6624	279
1109	S43	-5664	166	1159	G314	-6640	166
1110	S42	-5680	279	1160	G312	-6656	279
1111	S41	-5696	166	1161	G310	-6672	166
1112	S40	-5712	279	1162	G308	-6688	279
1113	S39	-5728	166	1163	G306	-6704	166
1114	S38	-5744	279	1164	G304	-6720	279
1115	S37	-5760	166	1165	G302	-6736	166
1116	S36	-5776	279	1166	G300	-6752	279
1117	S35	-5792	166	1167	G298	-6768	166
1118	S34	-5808	279	1168	G296	-6784	279
1119	S33	-5824	166	1169	G294	-6800	166
1120	S32	-5840	279	1170	G292	-6816	279
1121	S31	-5856	166	1171	G290	-6832	166
1122	S30	-5872	279	1172	G288	-6848	279
1123	S29	-5888	166	1173	G286	-6864	166
1124	S28	-5904	279	1174	G284	-6880	279
1125	S27	-5920	166	1175	G282	-6896	166
1126	S26	-5936	279	1176	G280	-6912	279
1127	S25	-5952	166	1177	G278	-6928	166
1128	S24	-5968	279	1178	G276	-6944	279
1129	S23	-5984	166	1179	G274	-6960	166
1130	S22	-6000	279	1180	G272	-6976	279
1131	S21	-6016	166	1181	G270	-6992	166
1132	S20	-6032	279	1182	G268	-7008	279
1133	S19	-6048	166	1183	G266	-7024	166
1134	S18	-6064	279	1184	G264	-7040	279
1135	S17	-6080	166	1185	G262	-7056	166
1136	S16	-6096	279	1186	G260	-7072	279
1137	S15	-6112	166	1187	G258	-7088	166
1138	S14	-6128	279	1188	G256	-7104	279
1139	S13	-6144	166	1189	G254	-7120	166
1140	S12	-6160	279	1190	G252	-7136	279
1141	S11	-6176	166	1191	G250	-7152	166
1142	S10	-6192	279	1192	G248	-7168	279
1143	S9	-6208	166	1193	G246	-7184	166
1144	S8	-6224	279	1194	G244	-7200	279
1145	S7	-6240	166	1195	G242	-7216	166
1146	S6	-6256	279	1196	G240	-7232	279
1147	S5	-6272	166	1197	G238	-7248	166
1148	S4	-6288	279	1198	G236	-7264	279
1149	S3	-6304	166	1199	G234	-7280	166
1150	S2	-6320	279	1200	G232	-7296	279

pad No	pad name	X	Y	pad No	pad name	X	Y
1201	G230	-7312	166	1251	G130	-8112	166
1202	G228	-7328	279	1252	G128	-8128	279
1203	G226	-7344	166	1253	G126	-8144	166
1204	G224	-7360	279	1254	G124	-8160	279
1205	G222	-7376	166	1255	G122	-8176	166
1206	G220	-7392	279	1256	G120	-8192	279
1207	G218	-7408	166	1257	G118	-8208	166
1208	G216	-7424	279	1258	G116	-8224	279
1209	G214	-7440	166	1259	G114	-8240	166
1210	G212	-7456	279	1260	G112	-8256	279
1211	G210	-7472	166	1261	G110	-8272	166
1212	G208	-7488	279	1262	G108	-8288	279
1213	G206	-7504	166	1263	G106	-8304	166
1214	G204	-7520	279	1264	G104	-8320	279
1215	G202	-7536	166	1265	G102	-8336	166
1216	G200	-7552	279	1266	G100	-8352	279
1217	G198	-7568	166	1267	G98	-8368	166
1218	G196	-7584	279	1268	G96	-8384	279
1219	G194	-7600	166	1269	G94	-8400	166
1220	G192	-7616	279	1270	G92	-8416	279
1221	G190	-7632	166	1271	G90	-8432	166
1222	G188	-7648	279	1272	G88	-8448	279
1223	G186	-7664	166	1273	G86	-8464	166
1224	G184	-7680	279	1274	G84	-8480	279
1225	G182	-7696	166	1275	G82	-8496	166
1226	G180	-7712	279	1276	G80	-8512	279
1227	G178	-7728	166	1277	G78	-8528	166
1228	G176	-7744	279	1278	G76	-8544	279
1229	G174	-7760	166	1279	G74	-8560	166
1230	G172	-7776	279	1280	G72	-8576	279
1231	G170	-7792	166	1281	G70	-8592	166
1232	G168	-7808	279	1282	G68	-8608	279
1233	G166	-7824	166	1283	G66	-8624	166
1234	G164	-7840	279	1284	G64	-8640	279
1235	G162	-7856	166	1285	G62	-8656	166
1236	G160	-7872	279	1286	G60	-8672	279
1237	G158	-7888	166	1287	G58	-8688	166
1238	G156	-7904	279	1288	G56	-8704	279
1239	G154	-7920	166	1289	G54	-8720	166
1240	G152	-7936	279	1290	G52	-8736	279
1241	G150	-7952	166	1291	G50	-8752	166
1242	G148	-7968	279	1292	G48	-8768	279
1243	G146	-7984	166	1293	G46	-8784	166
1244	G144	-8000	279	1294	G44	-8800	279
1245	G142	-8016	166	1295	G42	-8816	166
1246	G140	-8032	279	1296	G40	-8832	279
1247	G138	-8048	166	1297	G38	-8848	166
1248	G136	-8064	279	1298	G36	-8864	279
1249	G134	-8080	166	1299	G34	-8880	166
1250	G132	-8096	279	1300	G32	-8896	279

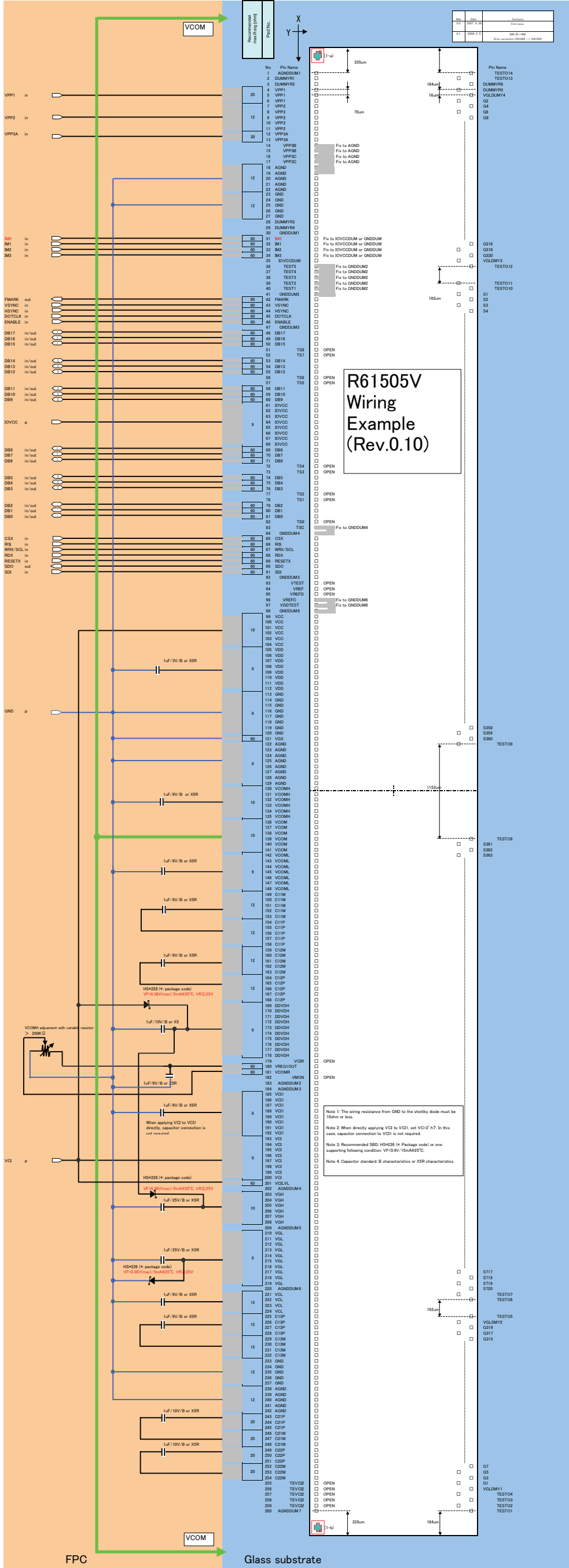
R61505V PAD Coordinates (No.14) (Unit: μ m)

2008.2.5 rev1.1

pad No	pad name	X	Y
1301	G30	-8912	166
1302	G28	-8928	279
1303	G26	-8944	166
1304	G24	-8960	279
1305	G22	-8976	166
1306	G20	-8992	279
1307	G18	-9008	166
1308	G16	-9024	279
1309	G14	-9040	166
1310	G12	-9056	279
1311	G10	-9072	166
1312	G8	-9088	279
1313	G6	-9104	166
1314	G4	-9120	279
1315	G2	-9136	166
1316	VGLDUMY4	-9152	279
1317	DUMMYR5	-9168	166
1318	DUMMYR6	-9184	279
1319	TESTO13	-9200	166
1320	TESTO14	-9216	279

Bump Arrangement**Figure 3**

R61505V Wiring Example & Recommended Wiring Resistance



GRAM Address Map

Table 16 GRAM address and display position on the panel (SS = 0, BGR = 0)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			h002EC			h002ED			h002EE			h002EF		
G4	G317	h00300			h00301			h00302			h00303			h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:			:	:			:			:			:		
G305	G16	h13000			h13001			h13002			h13003			h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			h13FEC			h13FED			h13FEE			h13FEF		

Table 17 GRAM address and display position on the panel (SS = 1, BGR = 1)

S/G pin		S720	S719	S718	S717	S716	S715	S714	S713	S712	S711	S710	S709	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			h002EC			h002ED			h002EE			h002EF		
G4	G317	h00300			h00301			h00302			h00303			h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:			:	:			:			:			:		
G305	G16	h13000			h13001			h13002			h13003			h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			h13FEC			h13FED			h13FEE			h13FEF		

Instruction

Outline

The R61505V adopts 18-bit bus architecture in order to interface to high-performance host processor in high speed. The R61505V starts internal processing after storing 16-/8-/1-bit control information sent from the host processor, in the instruction register (IR) and the data register (DR). Since the internal operation of the R61505V is controlled by the signals sent from the host processor, the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (IB15 ~ IB0) are called instruction. The following are the kinds of instruction of the R61505V.

1. Specify index
2. Display control
3. Power management control
4. Set internal GRAM address
5. Transfer data to and from the internal GRAM
6. γ -correction
7. Window address control
8. Panel Display Control

Normally, the instruction to write data is used the most often. The internal GRAM address is updated automatically as data is written to the internal GRAM, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the load on the host processor. The R61505V writes instructions consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycle).

Instruction Data Format

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID [7]	ID [6]	ID [5]	ID [4]	ID [3]	ID [2]	ID [1]	ID [0]

The index register specifies the index R00h to RFFh of the control register or RAM control to be accessed using a binary number from “0000_0000” to “1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

Display Control

Device Code Read (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	1	0	1	1	0	1	0	1	0	0	0	0	0	1	0	1

The device code “B505”H is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shifts from S1 to S720.

When SS = “1”, the source driver output shifts from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, color data is output in the order of R, G and then B.

When SS = “1” and BGR = “1”, color data is output in the order of B, G and then R.

When changing the SS and the BGR bit settings, RAM data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “Scan mode setting”.

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	BC0	0	0	0	0	0	0	0	0	NW0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NW0: When line inversion waveform is selected (BC0=1), NW0 bit sets number of line, N, as alternating cycle of line inversion. Line inversion is operated every N+1 line cycle. NW0 bit can be set to 1 or 2.

Table 18

NW[0]	Alternating cycle
0	Every line
1	Every 2 lines

BC0: Selects the liquid crystal drive waveform VCOM. See “Line Inversion AC Drive” for details.

BC0 = 0: frame inversion waveform is selected.

BC0 = 1: line inversion waveform is selected.

In either liquid crystal drive method; the polarity inversion is halted in blank period (back and front porch periods).

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRIR EG	DFM	0	BGR	0	0	0	0	ORG	0	I/D [1]	I/D [0]	AM	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

The entry mode register includes instruction bits for setting how to write data from the host processor to the GRAM in the R61505V.

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the R61505V writes data to the internal GRAM.

AM = “0”, sets the horizontal direction.

AM = “1”, sets the vertical direction.

When making a window address area, the data is written only within the area in the direction determined by I/D1-0, AM bits.

I/D[1:0]: Either increments (+1) or decrements (-1) the address counter (AC) automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]). The AM bit sets either horizontal or vertical direction in updating RAM address counter automatically when writing data to the internal RAM.

ORG: Moves the origin address according to the I/D setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed RAM write function. Also see Figure 4 and Figure 5.

ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.

ORG = 1: The origin address “h00000” is moved according to the I/D[1:0] setting.

Notes: 1. When ORG = 1, only the origin address “h00000” can be set.

2. In RAM read operation, make sure to set ORG = 0.

BGR: Reverses the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.

BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

BGR = 0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR = 1

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

DFM: In combination with the TRIREG setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM = 0 when not transferring data via 16-bit or 8-bit interface.

TRIREG: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 80-system 8-bit interface operation,

TRIREG = 0: 16-bit RAM data is transferred in two transfers.

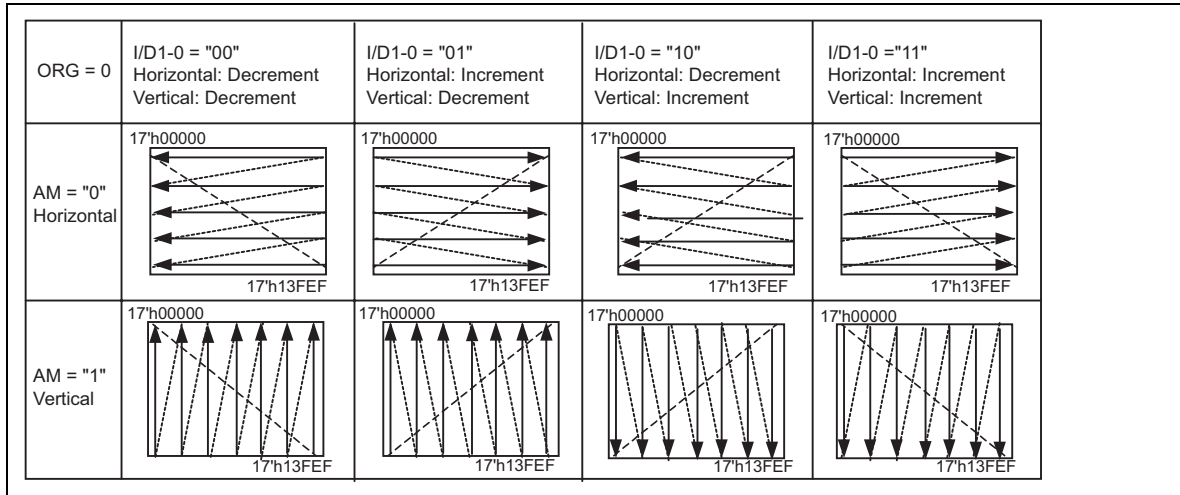
TRIREG = 1: 18-bit RAM data is transferred in three transfers.

In 80-system 16-bit bus interface operation,

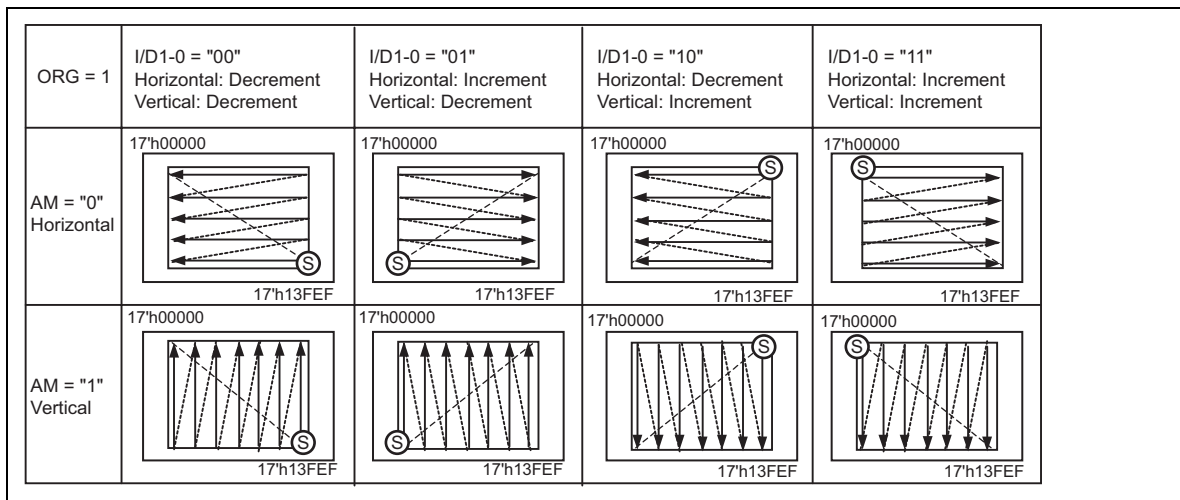
TRIREG = 0: 16-bit RAM data is transferred in one transfer.

TRIREG = 1: 18-bit RAM data is transferred in two transfers.

Make sure TRIREG = 0 when not transferring data via 16-bit or 8-bit interface. Also, set TRIREG = 0 during read operation.

**Figure 4 Automatic address update (ORG = 0, AM, I/D)**

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of RAM write operation.

**Figure 5 Automatic address update (ORG = 1, AM, I/D)**

Note 1: When ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area ("S" in circle in the above figure).

Note 2: When ORG = 1, make sure to set the address "h00000" in the RAM address set registers (R210h, R21h). Setting other addresses is inhibited.

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PTDE	0	0	0	BASE E	0	0	0	0	COL	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

COL: When COL = 1, grayscale amplifiers other than V0 and V63 halt displaying images so that power consumption is reduced. Also, only 8 colors are available. See “8-color Display Mode” in “Instruction Setting Sequence” for details.

Table 19

COL	Display color
0	262,144
1	8

Note: When COL = 1, do not write the data corresponding to the grayscales, for which the operation of amplifier is halted.

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The R61505V drives liquid crystal with non-lit display level or drives only partial image display area.

BASEE = 1: A base image is displayed on the panel.

PTDE: PTDE is the display enable bit of a partial image.

PTDE=0: Partial image is not displayed. Only base image is displayed.

PTDE=1: Partial image is displayed. Write BASEE=0 to turn off a base image.

Table 20

BASEE	PTDE	VLE	COL	State
0	0	*	*	Halt display operation
1	0	0	0	260k color display operation
1	0	0	1	8-color display operation
1	0	1	0	260k color display operation with scroll function enabled
0	1	*	0	260k color partial display operation
0	1	*	1	8 color partial display operation

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	FP [7]	FP [6]	FP [5]	FP [4]	FP [3]	FP [2]	FP [1]	FP [0]	BP [7]	BP [6]	BP [5]	BP [4]	BP [3]	BP [2]	BP [1]	BP [0]
Default value		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

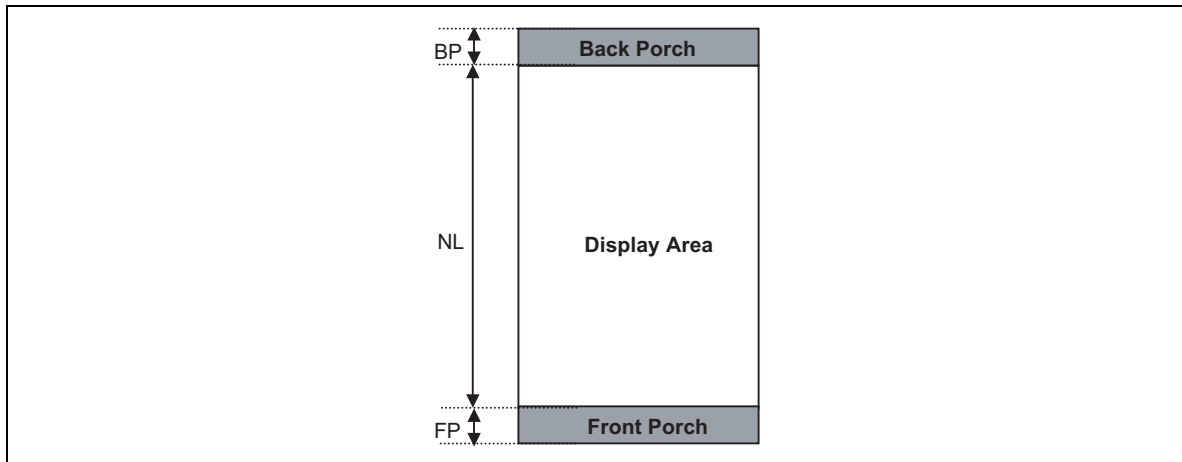
FP [7:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [7:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Table 21

FP[7:0] BP[7:0]	Front porch period	Back porch period
8'h00	Setting inhibited	Setting inhibited
8'h01	Setting inhibited	Setting inhibited
8'h02	Setting inhibited	2 lines
8'h03	3 lines	3 lines
8'h04	4 lines	4 lines
8'h05	5 lines	5 lines
8'h06	6 lines	6 lines
8'h07	7 lines	7 lines
8'h08	8 lines	8 lines
8'h09	9 lines	9 lines
8'h0A	10 lines	10 lines
8'h0B	11 lines	11 lines
8'h0C	12 lines	12 lines
8'h0D	13 lines	13 lines
8'h0E	14 lines	14 lines
8'h0F	15 lines	15 lines
:	:	:
8'h7F	127 lines	127 lines
8'h80	128 lines	128 lines
8'h81	Setting inhibited	Setting inhibited
:	:	:
8'hFF	Setting inhibited	Setting inhibited

**Figure 6 Front and Back Porch periods**

Note to Setting BP and FP

Set the BP and FP bits as follows:

$BP \geq 2 \text{ lines}$	$FP \geq 3 \text{ lines}$	$FP + BP \leq 256 \text{ lines}$
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Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS [2]	PTS [1]	PTS [0]	0	0	PTG	0	ISC [3]	ISC [2]	ISC [1]	ISC [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

ISC [3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 22

ISC[3:0]	Scan cycle
4'h0	Setting inhibited
4'h1	3 frames
4'h2	5 frames
4'h3	7 frames
4'h4	9 frames
4'h5	11 frames
4'h6	13 frames
4'h7	15 frames
4'h8	17 frames
4'h9	19 frames
4'hA	21 frames
4'hB	23 frames
4'hC	25 frames
4'hD	27 frames
4'hE	29 frames
4'hF	31 frames

PTG: Sets the scan mode in non-display area

Table 23

PTG	Scan mode in non-display area
0	Normal scan
1	Interval scan

Note: Select frame-inversion AC drive when interval scan is selected.

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V31 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 24 Source output level and voltage generating operation in non-display drive period

	PTS[1:0]	Source output level in non lit display area		Grayscale amplifier operation in non lit display are	Step-up clock frequency in non lit display are
		Positive polarity	Negative polarity		
0	00	V63	V0	V0 to V63	Register setting (DC0, DC1)
	01	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)
	10	GND	GND	V0 to V63	Register setting (DC0, DC1)
	11	Hi-z	Hi-z	V0 to V63	Register setting (DC0, DC1)
1	00	V63	V0	V0, V63	DC0 setting x 1/2
	01	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)	(Setting inhibited)
	10	GND	GND	V0, V63	DC0 setting x 1/2
	11	Hi-z	Hi-z	V0, V63	DC0 setting x 1/2

Note: Define source polarity in non lit display area by NDL bit. Note that if PTS[2]=1, step-up operation may not be executed successfully depending on DC0 and RTN* values.

Display Control 4 (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARK KOE	FMI [2]	FMI [1]	FMI [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the R61505V starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits. See [FMARK Interface](#) for details.

Table 25

FMI[2]	FMI[1]	FMI[0]	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	ENC [2]	ENC [1]	ENC [0]	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets the interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the R61505V performs display operation.

Table 26 RGB interface operation

RIM[1]	RIM[0]	Bus width	Colors	Used pins
0	0	18-bit RGB interface (1 transfer/pixel)	262,144	DB17-0
0	1	16-bit RGB interface (1 transfer/pixel)	65,536	DB17-13, 11-1
1	0	Setting inhibited	-	-
1	1	Setting inhibited	-	-

Note: Instruction bits are set only via system interface.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 27 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting inhibited

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 28 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface
1	RGB interface

ENC[2:0]: Sets the RAM write cycle via RGB interface.

Table 25 RAM Write Cycle

ENC[2:0]	RAM Write Cycle (frame periods)
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
3'h3	4 frames
3'h4	5 frames
3'h5	6 frames
3'h6	7 frames
3'h7	8 frames

Frame Marker Position (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	FMP [8]	FMP [7]	FMP [6]	FMP [5]	FMP [4]	FMP [3]	FMP [2]	FMP [1]	FMP [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period (IOVCC-GND amplitude signal). FMARK can be used as the trigger signal for frame synchronous write operation. See [FMARK Interface](#) for details.

Make sure the setting restriction $9'h000 \leq \text{FMP} \leq \text{BP} + \text{NL} + \text{FP}$.

Table 29

FMP[8:0]	FMARK output position
9'h000	0 th line
9'h001	1 st line
9'h002	2 nd line
⋮	⋮
9'h14E	334 th line
9'h14F	335 th line
9'h150~1FF	Setting disabled

VCOM Low Power Control (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	VEM [1]	VEM [0]	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VEM [1:0]: VCOM equalize function control bit.

When VEM [0]="1", VCOM falls to GND level when switching to VCOMH to VCOML (VCOMH → GND → VCOML).

When VEM [1] = "1", VCOM rises to VCI level when switching to VCOML to VCOMH (VCOML → VCI → VCOMH).

Make sure that $VCI < VCOMH$ and $GND > VCOML$.

Table 30

VEM[1:0]	Operation
2'h0	Normal VCOM drive (No equalizing operation)
2'h1	Equalize VCOMH (VCOMH→VCOML)
2'h2	Equalize VCOML (VCOML→VCOMH)
2'h3	Equalize VCOMH/VCOML

Note: Check the trade-off between the quality of display on the panel and the power efficiency before use.

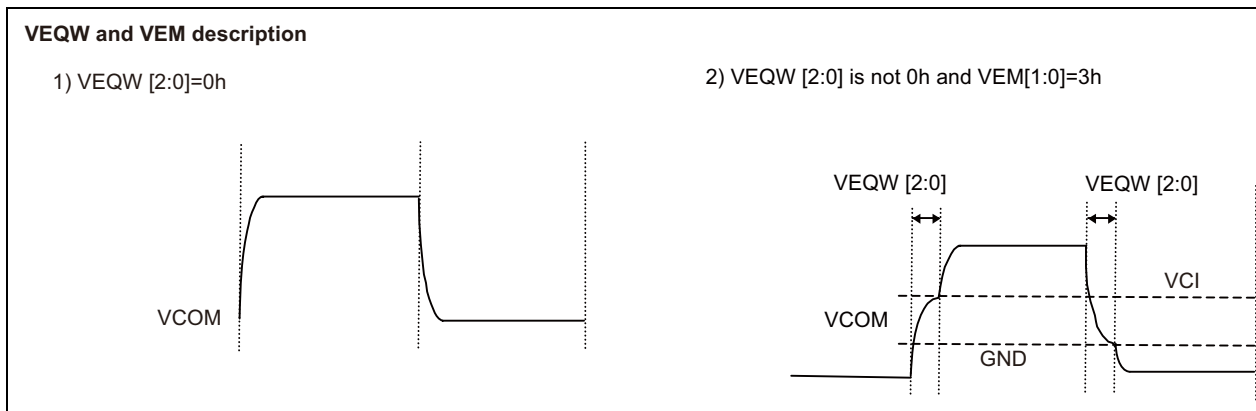


Figure 7

Note: See R93h and R98h for VEQWI and VEQWE descriptions.

External Display Interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK

DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = "0" and disables data write operation when ENABLE = "1".

EPL = 1: writes data DB17-0 when ENABLE = "1" and disables data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of HSYNC pin.

HSPL = 0: low active

HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.

VSPL = 0: low active

VSPL = 1: high active

Power Control

Power Control 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	BT [2]	BT [1]	BT [0]	0	0	AP [1]	AP [0]	0	DSTB	0	0
Default value		0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0

DSTB: When DSTB = 1, the R61505V enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the R61505V enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[1:0] = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

Table 31 Constant current in amplifier in LCD power supply

AP[1:0]	LCD power supply circuits
2'h0	Halt operation
2'h1	0.5
2'h2	0.75
2'h3	1

Note: In this table, the constant current in operational amplifiers is the ratio to the constant current when AP[1:0] is set to 2'h3.

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

Table 32 Step up factor and output voltage level

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Setting inhibited			
3'h1				
3'h2				
3'h3	VCI1 x2 [x 2]	-VCI1 [x -1]	DDVDH x 3 [x 6]	-(VCI1+DDVDH x 2) [x -5]
3'h4				-(DDVDH x 2) [x -4]
3'h5 (Default)				-(VCI1+DDVDH) [x -3]
3'h6			VCI1+DDVDH x 2 [x 5]	-(VCI1+DDVDH x 2) [x -5]
3'h7				-(DDVDH x 2) [x -4]

- Notes: 1. The step-up factor from VCI1 is shown in the brackets [].
2. Set the following voltages within the respective ranges:
- DDVDH = 6.0V (max.)
 - VGH = 18.0V (max.)
 - VGL = -13.5V (max.)
 - VGH-VGL= 28.0V (max.)
 - VCL=-3.0V(max.)

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	DC1 [2]	DC1 [1]	DC1 [0]	0	DC0 [2]	DC0 [1]	DC0 [0]	0	VC [2]	VC [1]	VC [0]
Default value		0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1

DC1[2:0]: Defines step-up clock frequency for the step-up circuit 2. The step-up clock is synchronized with internal clock.

Table 33

DC1[2:0]	Step-up clock frequency for the step-up circuit 2 (f_{DCDC2})
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	Line frequency / 4
3'h3	Line frequency / 8
3'h4	Line frequency / 16
3'h5	Setting inhibited
3'h6	Halt step-up circuit 2
3'h7	Setting inhibited

To calculate step-up clock frequency for the step-up circuit 2

Step-up clock frequency (f_{DCDC2}) = line frequency / $2^{(N)}$ [Hz]

= Clock frequency internal operation f_{osc} / number of clock per line x
division ratio x $2^{(N)}$ [Hz]

f_{osc} : Clock frequency internal operation

Number of clock per line: RTNI [4:0] or RTNE [4:0]

Division ratio: DIVI [1:0] or DIVE [1:0]

N: DC1[2:0] value

DC0[2:0]: Defines step-up clock frequency for the step-up circuit 1. The step-up clock is synchronized with internal clock.

Table 34

DC0[2:0]	Step-up clock frequency for the step-up circuit 1 (f_{DCDC1})
3'h0	Setting inhibited
3'h1	Setting inhibited
3'h2	Setting inhibited
3'h3	$f_{\text{OSC}} / 8$
3'h4	$f_{\text{OSC}} / 16$
3'h5	$f_{\text{OSC}} / 32$
3'h6	Halt step-up circuit 1
3'h7	Setting inhibited

Note 1: Make sure that $f_{\text{DCDC1}} \geq f_{\text{DCDC2}}$.

Note 2: Make sure to set DC0 and RTN* bits so that

Step-up cycle of the Step-up circuit 1 ≤ 1 line cycle.

Otherwise the step-up operation may fail.

To calculate step-up clock frequency for the step-up circuit 1

Step-up clock frequency (f_{DCDC1}) = Reference clock frequency / 2^N [Hz]

= Clock frequency for internal operation f_{osc} / division ratio $\times 2^N$ [Hz]

f_{osc} : Clock frequency internal operation

Division ratio: DIVI [1:0] or DIVE [1:0]

N: DC1[2:0] value

VC [2:0]: Defines VCI1 level.

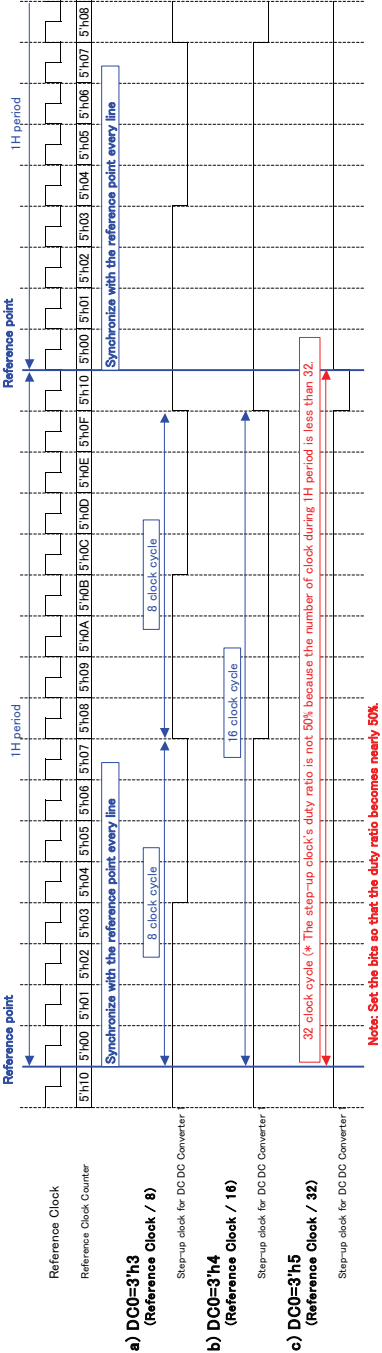
Table 35

VC[2:0]	VCI1 (Reference for step-up operation)
3'h0	Setting inhibited
3'h1	$0.94 \times \text{VCILVL}$
3'h2	$0.89 \times \text{VCILVL}$
3'h3	Setting inhibited
3'h4	Setting inhibited
3'h5	$0.76 \times \text{VCIVLV}$
3'h6	Setting inhibited
3'h7	$1.00 \times \text{VCILVL}$

■ Examples of DC0 values and Step-up clock for DC DC converter 1

DDCC Converter 1 charges and boosts voltage level in synchronization with step-up clock generated in the timing generator circuit. Step-up clock frequency for DC DC Converter 1 is decided by DC0 bit which determines division ratio for the reference clock. (In order to prevent flicker, the step-up clock for DC DC Converter 1 synchronizes with display operation's reference points every line.)
Note) Set DC0 and RTNx so that (Step-up frequency for DC DC converter 1) \geq (Line frequency).
If the restriction is not followed, duty ratio becomes less than 50% during the boosting operation causing the step-up circuit's malfunction.

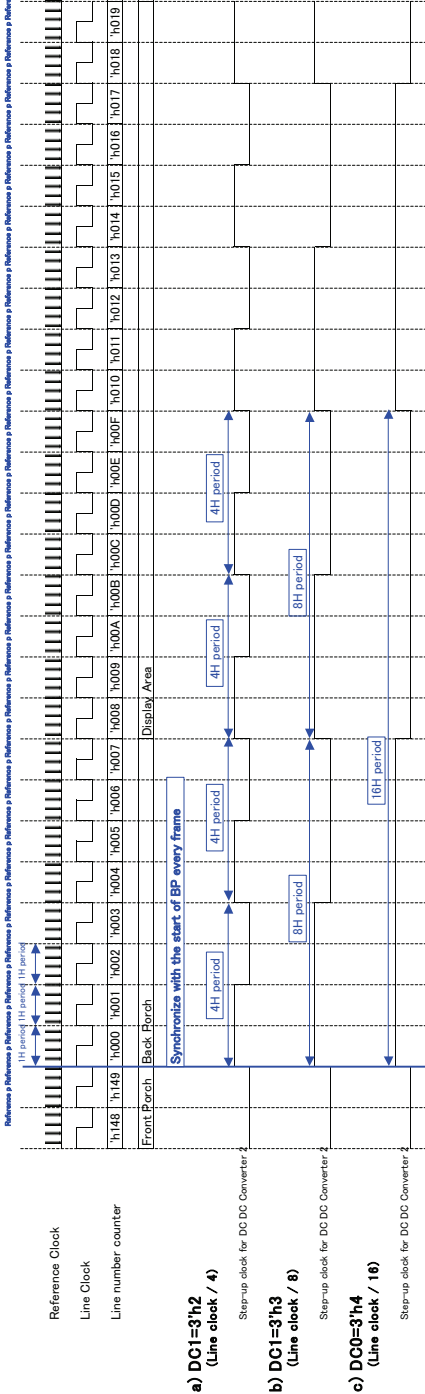
Example: DIVn=2'h1, RTN=5'h11 (Reference clock period=internal operation clock / 2, 1H period=17 clocks)



■ Examples of DC1x values and Step-up clock for DC DC converter 2

DDCC Converter 2 charges and boosts voltage level in synchronization with step-up clock generated in the timing generator circuit. Step-up clock frequency for DC DC Converter 2 is decided by DC1x bit which determines division ratio for the reference clock. (In order to prevent flicker, the step-up clock for DC DC converter 2 synchronizes with the start of BP every frame.)

Example: BP=FP=8'h08, NL=7'h4F (Front porch=back porch=8 lines, liquid crystal drive line=320 lines)



Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VRH [0]	0	0	0	VCM R	1	0	PSON	PON	VRH [4]	VRH [3]	VRH [2]	VRH [1]
Default value		0	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1

VRH[4:0]: Sets the factor to generate VREG1OUT

Table 36

VRH[4:0]	VREG1OUT
5'h00	Halt (Hi-z)
5'h01-5'h0F	Setting inhibited
5'h10	$VCIR \times 1.600$
5'h11	$VCIR \times 1.625$
5'h12	$VCIR \times 1.650$
5'h13	$VCIR \times 1.675$
5'h14	$VCIR \times 1.700$
5'h15	$VCIR \times 1.725$
5'h16	$VCIR \times 1.750$
5'h17	$VCIR \times 1.775$
5'h18	$VCIR \times 1.800$
5'h19	$VCIR \times 1.825$
5'h1A	$VCIR \times 1.850$
5'h1B	$VCIR \times 1.875$
5'h1C	$VCIR \times 1.900$
5'h1D	$VCIR \times 1.925$
5'h1E	$VCIR \times 1.950$
5'h1F	$VCIR \times 1.975$

Note: Make sure that $VREG1OUT \leq (DDVDH-0.5)V$ in setting VC and VRH bits.

PON, PSON: Turns power supply on. Write PON and PSON to turn power supply on. Internal power supply operation starts. Follow the Power On sequences.

Table 37 Power supply sequences (PSON, PON)

PSON	PON	Operation
0	0	Power supply OFF sequence
0	1	Power supply OFF sequence
1	0	Power supply OFF sequence
1	1	Power supply ON sequence

VCMR: Select VCOMH voltage level from external resistance (VCOMR), internal electronic volumes VCM1 and VCM2.

Table 38

VCMR	VCOMH level
0	VCOMR
1 (Default)	Internal electronic volume

Note: Internal electronic volume is adjusted by VCM1 and VCM2 bits.

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VDV [4]	VDV [3]	VDV [2]	VDV [1]	VDV [0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0]: Set VCOM alternating amplitude in the range of VREG1OUTx0.70 to VREG1OUTx1.32.

Table 39 VDV Setting

VDV[4:0]	VCOM Amplitude	VDV[4:0]	VCOM Amplitude
5'h0	VREG1OUT×0.70	5'h10	VREG1OUT×1.02
5'h1	VREG1OUT×0.72	5'h11	VREG1OUT×1.04
5'h2	VREG1OUT×0.74	5'h12	VREG1OUT×1.06
5'h3	VREG1OUT×0.76	5'h13	VREG1OUT×1.08
5'h4	VREG1OUT×0.78	5'h14	VREG1OUT×1.10
5'h5	VREG1OUT×0.80	5'h15	VREG1OUT×1.12
5'h6	VREG1OUT×0.82	5'h16	VREG1OUT×1.14
5'h7	VREG1OUT×0.84	5'h17	VREG1OUT×1.16
5'h8	VREG1OUT×0.86	5'h18	VREG1OUT×1.18
5'h9	VREG1OUT×0.88	5'h19	VREG1OUT×1.20
5'hA	VREG1OUT×0.90	5'h1A	VREG1OUT×1.22
5'hB	VREG1OUT×0.92	5'h1B	VREG1OUT×1.24
5'hC	VREG1OUT×0.94	5'h1C	VREG1OUT×1.26
5'hD	VREG1OUT×0.96	5'h1D	VREG1OUT×1.28
5'hE	VREG1OUT×0.98	5'h1E	VREG1OUT×1.30
5'hF	VREG1OUT×1.00	5'h1F	VREG1OUT×1.32

Note: Set VDV[4:0] so that VCOM amplitude becomes 6.0V or smaller.

RAM Access Control**RAM Address Set (Horizontal Address) (R20h)****RAM Address Set (Vertical Address) (R21h)**

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R 20	W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 21	W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the R61505V writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM = “1”), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

Note 2: In internal clock operation and VSYNC interface operation (RM = “0”), the address AD16-0 is set when executing the instruction.

Table 40 GRAM Address setting range

AD[16:0]	GRAM Data Setting
17'h00000 – 17'h000EF	Bitmap data on the 1 st line
17'h00100 – 17'h001EF	Bitmap data on the 2 nd line
17'h00200 – 17'h002EF	Bitmap data on the 3 rd line
17'h00300 – 17'h003EF	Bitmap data on the 4 th line
17'h00400 – 17'h004EF	Bitmap data on the 5 th line
:	:
17'h13C00 – 17'h13CEF	Bitmap data on the 317 th line
17'h13D00 – 17'h13DEF	Bitmap data on the 318 th line
17'h13E00 – 17'h13EEF	Bitmap data on the 319 th line
17'h13F00 – 17'h13FEF	Bitmap data on the 320 th line

GRAM Data Write (R22h)

R/W	RS	
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operations.
RGB i/f operation		RAM write data WD[17:0] is transferred via different data bus in different interface operations.

WD[17:0]: The R61505V develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The R61505V automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. The DFM bit sets the format to develop 16-bit data into the 18-bit data in 16-bit or 8-bit interface operation.

Note: When writing data in the GRAM via system interface while using the RGB interface, make sure that write operations via two interfaces do not conflict one another.

GRAM Data Read (R22h)

R/W	RS	
R	1	RAM read data RD[17:0] is transferred via different data bus in different interface operations.

RD[17:0]: 18-bit data read from the GRAM. RAM read data RD[17:0] is transferred via different data bus in different interface operation.

When the R61505V reads data from the GRAM to the host processor, the first word read immediately after RAM address set is not outputted, so that it is invalid. Valid data is sent to the data bus when the R61505V reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

Note: This register is disabled in RGB interface operation.

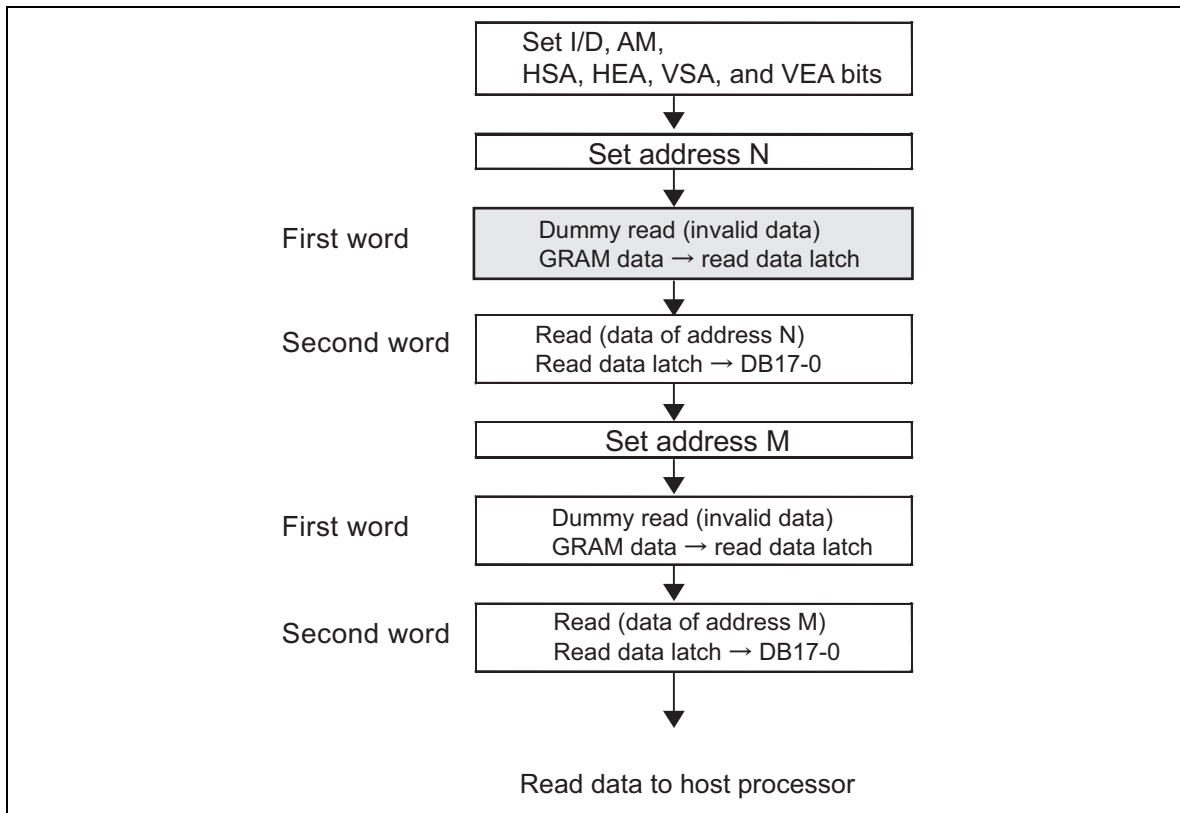


Figure 8 GRAM Read Sequence

NVM(NON-VOLATILE MEMORY) Write Control**NVM Data Read 1 (R28), NVM Data Read 2 (R29h), NVM Data Read 3 (R2Ah)**

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28	R/W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID [3]	UID [2]	UID [1]	UID [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R29	R/W	1	0	0	0	0	0	0	0	0	0	VC M1 [6]	VC M1 [5]	VC M1 [4]	VC M1 [3]	VC M1 [2]	VC M1 [1]	VC M1 [0]
	Default		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R2A	R/W	1	0	0	0	0	0	0	0	0	VC MSE L	VC M2 [6]	VC M2 [5]	VC M2 [4]	VC M2 [3]	VC M2 [2]	VC M2 [1]	VC M2 [0]
	Default		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

UID[3:0]: The data bits UID[3:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting (CALB) to this register. UID[3:0] can be used to write and read user identification code in NVM.

The setting value in UID[3:0] bits is enabled when not reading out the setting value from NVM via CALB setting.

VCM1[6:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM1[6:0], make sure to set VCMSEL = 1.

When using the data written in NVM for setting the VCOMH level, the data bits VCM1[6:0] are written to the designated address in NVM and the written data can be read out from NVM by instruction setting (CALB) to this register. When the data bits VCM2[6:0] are written in NVM before writing the data bits VCM1[6:0] to NVM, the VCM1[6:0] setting value written in NVM cannot be used for setting the VCOMH level.

VCM2[6:0]: Selects the factor of VREG1OUT to generate VCOMH. When enabling the setting valued in VCM2[6:0], make sure to set VCMSEL = 0. The function of VCM2[6:0] instruction is the same as that of VCM1[6:0].

Write the setting value in VCM2[6:0] bits and VCMSEL = 0 in the designated addresses of NVM, when reading out the setting value written in NVM for VCOMH level setting and the data is already written in the designated address of VCM1[6:0] in the NVM. The VCM2[6:0] data bits written in NVM can be read out via CALB setting for setting the VCOMH level.

Note: When R2A register is read after setting CALB=1 (RA4h), data in IB6-5, R2Ah, is not always 0 and different data may be read out from different die.

VCMSEL: When VCMSEL = 1, VCM1 is selected. When VCMSEL = 0, VCM2 is selected.

Table 41

VCM1[6:0] VCM2[6:0]	VCOMH			VCM1[6:0] VCM2[6:0]	VCOMH			VCM1[6:0] VCM2[6:0]	VCOMH		
7'h 00	VREG1OUT	X	0.492	7'h2B	VREG1OUT	X	0.664	7'h56	VREG1OUT	X	0.836
7'h 01	VREG1OUT	X	0.496	7'h2C	VREG1OUT	X	0.668	7'h57	VREG1OUT	X	0.840
7'h 02	VREG1OUT	X	0.500	7'h2D	VREG1OUT	X	0.672	7'h58	VREG1OUT	X	0.844
7'h03	VREG1OUT	X	0.504	7'h2E	VREG1OUT	X	0.676	7'h59	VREG1OUT	X	0.848
7'h04	VREG1OUT	X	0.508	7'h2F	VREG1OUT	X	0.680	7'h5A	VREG1OUT	X	0.852
7'h05	VREG1OUT	X	0.512	7'h30	VREG1OUT	X	0.684	7'h5B	VREG1OUT	X	0.856
7'h06	VREG1OUT	X	0.516	7'h31	VREG1OUT	X	0.688	7'h5C	VREG1OUT	X	0.860
7'h07	VREG1OUT	X	0.520	7'h32	VREG1OUT	X	0.692	7'h5D	VREG1OUT	X	0.864
7'h08	VREG1OUT	X	0.524	7'h33	VREG1OUT	X	0.696	7'h5E	VREG1OUT	X	0.868
7'h09	VREG1OUT	X	0.528	7'h34	VREG1OUT	X	0.700	7'h5F	VREG1OUT	X	0.872
7'h0A	VREG1OUT	X	0.532	7'h35	VREG1OUT	X	0.704	7'h60	VREG1OUT	X	0.876
7'h0B	VREG1OUT	X	0.536	7'h36	VREG1OUT	X	0.708	7'h61	VREG1OUT	X	0.880
7'h0C	VREG1OUT	X	0.540	7'h37	VREG1OUT	X	0.712	7'h62	VREG1OUT	X	0.884
7'h0D	VREG1OUT	X	0.544	7'h38	VREG1OUT	X	0.716	7'h63	VREG1OUT	X	0.888
7'h0E	VREG1OUT	X	0.548	7'h39	VREG1OUT	X	0.720	7'h64	VREG1OUT	X	0.892
7'h0F	VREG1OUT	X	0.552	7'h3A	VREG1OUT	X	0.724	7'h65	VREG1OUT	X	0.896
7'h10	VREG1OUT	X	0.556	7'h3B	VREG1OUT	X	0.728	7'h66	VREG1OUT	X	0.900
7'h11	VREG1OUT	X	0.560	7'h3C	VREG1OUT	X	0.732	7'h67	VREG1OUT	X	0.904
7'h12	VREG1OUT	X	0.564	7'h3D	VREG1OUT	X	0.736	7'h68	VREG1OUT	X	0.908
7'h13	VREG1OUT	X	0.568	7'h3E	VREG1OUT	X	0.740	7'h69	VREG1OUT	X	0.912
7'h14	VREG1OUT	X	0.572	7'h3F	VREG1OUT	X	0.744	7'h6A	VREG1OUT	X	0.916
7'h15	VREG1OUT	X	0.576	7'h40	VREG1OUT	X	0.748	7'h6B	VREG1OUT	X	0.920
7'h16	VREG1OUT	X	0.580	7'h41	VREG1OUT	X	0.752	7'h6C	VREG1OUT	X	0.924
7'h17	VREG1OUT	X	0.584	7'h42	VREG1OUT	X	0.756	7'h6D	VREG1OUT	X	0.928
7'h18	VREG1OUT	X	0.588	7'h43	VREG1OUT	X	0.760	7'h6E	VREG1OUT	X	0.932
7'h19	VREG1OUT	X	0.592	7'h44	VREG1OUT	X	0.764	7'h6F	VREG1OUT	X	0.936
7'h1A	VREG1OUT	X	0.596	7'h45	VREG1OUT	X	0.768	7'h70	VREG1OUT	X	0.940
7'h1B	VREG1OUT	X	0.600	7'h46	VREG1OUT	X	0.772	7'h71	VREG1OUT	X	0.944
7'h1C	VREG1OUT	X	0.604	7'h47	VREG1OUT	X	0.776	7'h72	VREG1OUT	X	0.948
7'h1D	VREG1OUT	X	0.608	7'h48	VREG1OUT	X	0.780	7'h73	VREG1OUT	X	0.952
7'h1E	VREG1OUT	X	0.612	7'h49	VREG1OUT	X	0.784	7'h74	VREG1OUT	X	0.956
7'h1F	VREG1OUT	X	0.616	7'h4A	VREG1OUT	X	0.788	7'h75	VREG1OUT	X	0.960
7'h20	VREG1OUT	X	0.620	7'h4B	VREG1OUT	X	0.792	7'h76	VREG1OUT	X	0.964
7'h21	VREG1OUT	X	0.624	7'h4C	VREG1OUT	X	0.796	7'h77	VREG1OUT	X	0.968
7'h22	VREG1OUT	X	0.628	7'h4D	VREG1OUT	X	0.800	7'h78	VREG1OUT	X	0.972
7'h23	VREG1OUT	X	0.632	7'h4E	VREG1OUT	X	0.804	7'h79	VREG1OUT	X	0.976
7'h24	VREG1OUT	X	0.636	7'h4F	VREG1OUT	X	0.808	7'h7A	VREG1OUT	X	0.980
7'h25	VREG1OUT	X	0.640	7'h50	VREG1OUT	X	0.812	7'h7B	VREG1OUT	X	0.984
7'h26	VREG1OUT	X	0.644	7'h51	VREG1OUT	X	0.816	7'h7C	VREG1OUT	X	0.988
7'h27	VREG1OUT	X	0.648	7'h52	VREG1OUT	X	0.820	7'h7D	VREG1OUT	X	0.992
7'h28	VREG1OUT	X	0.652	7'h53	VREG1OUT	X	0.824	7'h7E	VREG1OUT	X	0.996
7'h29	VREG1OUT	X	0.656	7'h54	VREG1OUT	X	0.828	7'h7F	VREG1OUT	X	1.000
7'h2A	VREG1OUT	X	0.660	7'h55	VREG1OUT	X	0.832				

γ Control γ Control 1 ~ 10 (R30h ~ R39h)

		IB																
	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	6	IB5	IB4	IB3	IB2	IB1	IB0
R 30	W	1	0	0	0	PR0 P01 [4]	PR0 P01 [3]	PR0 P01 [2]	PR0 P01 [1]	PR0 P01 [0]	0	0	0	PR0 P00 [4]	PR0 P00 [3]	PR0 P00 [2]	PR0 P00 [1]	PR0 P00 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 31	W	1	PR0 P04 [3]	PR0 P04 [2]	PR0 P04 [1]	PR0 P04 [0]	PR0 P03 [3]	PR0 P03 [2]	PR0 P03 [1]	PR0 P03 [0]	0	0	0	PR0 P02 [4]	PR0 P02 [3]	PR0 P02 [2]	PR0 P02 [1]	PR0 P02 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 32	W	1	0	0	0	PR0 P06 [4]	PR0 P06 [3]	PR0 P06 [2]	PR0 P06 [1]	PR0 P06 [0]	0	0	0	0	PR0P 05 [3]	PR0P 05 [2]	PR0 P05 [1]	PR0 P05 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 33	W	1	0	0	0	PR0 P08 [4]	PR0 P08 [3]	PR0 P08 [2]	PR0 P08 [1]	PR0 P08 [0]	0	0	0	PR0 P07 [4]	PR0 P07 [3]	PR0 P07 [2]	PR0 P07 [1]	PR0 P07 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 34	W	1	0	0	PI0 P3 [1]	PI0 P3 [0]	0	0	PI0 P2 [1]	PI0 P2 [0]	0	0	PI0 P1 [1]	PI0 P1 [0]	0	0	PI0 P0 [1]	PI0 P0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 35	W	1	0	0	0	PR0 N01 [4]	PR0 N01 [3]	PR0 N01 [2]	PR0 N01 [1]	PR0 N01 [0]	0	0	0	PR0 N00 [4]	PR0 N00 [3]	PR0 N00 [2]	PR0 N00 [1]	PR0 N00 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 36	W	1	PR0 N04 [3]	PR0 N04 [2]	PR0 N04 [1]	PR0 N04 [0]	PR0 N03 [3]	PR0 N03 [2]	PR0 N03 [1]	PR0 N03 [0]	0	0	0	PR0 N02 [4]	PR0 N02 [3]	PR0 N02 [2]	PR0 N02 [1]	PR0 N02 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 37	W	1	0	0	0	PR0 N06 [4]	PR0 N06 [3]	PR0 N06 [2]	PR0 N06 [1]	PR0 N06 [0]	0	0	0	0	PR0 N05 [3]	PR0 N05 [2]	PR0 N05 [1]	PR0 N05 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 38	W	1	0	0	0	PR0 N08 [4]	PR0 N08 [3]	PR0 N08 [2]	PR0 N08 [1]	PR0 N08 [0]	0	0	0	PR0 N07 [4]	PR0 N07 [3]	PR0 N07 [2]	PR0 N07 [1]	PR0 N07 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 39	W	1	0	0	PI0 N3 [1]	PI0 N3 [0]	0	0	PI0 N2 [1]	PI0 N2 [0]	0	0	PI0 N1 [1]	PI0 N1 [0]	0	0	PI0 N0 [1]	PI0 N0 [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PR0P00[4:0] R0 reference level adjustment register for positive polarity

PR0N00[4:0] R0 reference level adjustment register for negative polarity

PR0P01[4:0] R1 reference level adjustment register for positive polarity

PR0N01[4:0] R1 reference level adjustment register for negative polarity

PR0P02[4:0] R2 reference level adjustment register for positive polarity

PR0N02[4:0] R2 reference level adjustment register for negative polarity

PR0P03[3:0] R3 reference level adjustment register for positive polarity

PR0N03[3:0]	R3 reference level adjustment register for negative polarity
PR0P04[3:0]	R4 reference level adjustment register for positive polarity
PR0N04[3:0]	R4 reference level adjustment register for negative polarity
PR0P05[3:0]	R5 reference level adjustment register for positive polarity
PR0N05[3:0]	R5 reference level adjustment register for negative polarity
PR0P06[4:0]	R6 reference level adjustment register for positive polarity
PR0N06[4:0]	R6 reference level adjustment register for negative polarity
PR0P07[4:0]	R7 reference level adjustment register for positive polarity
PR0N07[4:0]	R7 reference level adjustment register for negative polarity
PR0P08[4:0]	R8 reference level adjustment register for positive polarity
PR0N08[4:0]	R8 reference level adjustment register for negative polarity
PI0P0~1[1:0]	Interpolation adjustment register for positive polarity (V2~V7)
PI0N0~1[1:0]	Interpolation adjustment register for negative polarity (V2~V7)
PI0P2~3[1:0]	Interpolation adjustment register for positive polarity (V56~61)
PI0N2~3[1:0]	Interpolation adjustment register for negative polarity (V56~V61)

Window Address Control**Window Horizontal RAM Address (Start Address) (R50h)****Window Horizontal RAM Address (End Address) (R51h)****Window Vertical RAM Address (Start Address) (R52h)****Window Vertical RAM Address (End Address) (R53h)**

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R 50	W	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 51	W	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
	Default		0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R 52	W	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 53	W	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]
	Default		0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation.

In setting, make sure that

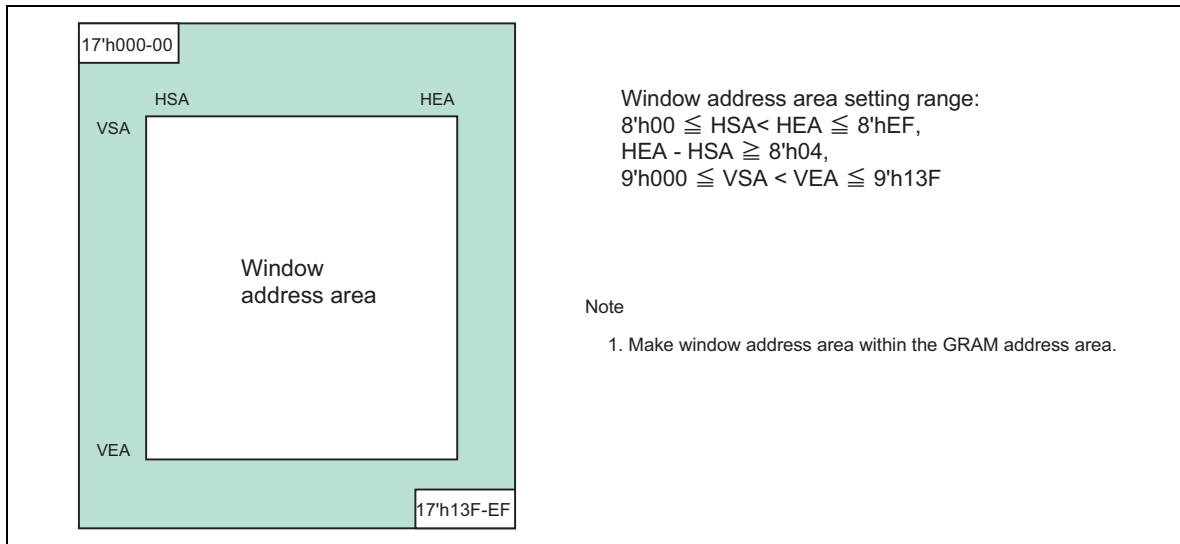
$$8'h00 \leq HSA < HEA \leq 8'hEF \text{ and}$$

$$8'h04 \leq HEA - HSA.$$

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation.

In setting, make sure that

$$9'h000 \leq VSA < VEA \leq 9'h13F.$$

**Figure 9 GRAM Address Map and Window Address Area**

Base Image Display Control**Driver Output Control (R60h),****Base Image Display Control (R61h)****Vertical Scroll Control (R6Ah)**

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R60	W	1	GS	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	0	0	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]
	Default		0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R61	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R6A	W	1	0	0	0	0	0	0	0	VL [8]	VL [7]	VL [6]	VL [5]	VL [4]	VL [3]	VL [2]	VL [1]	VL [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 42

NL[5:0]	Number of drive lines
6'h00-6'h1C	Setting inhibited
6'h1D	240 lines
6'h1E	248 lines
6'h1F	256 lines
6'h20	264 lines
6'h21	272 lines
6'h22	280 lines
6'h23	288 lines
6'h24	296 lines
6'h25	304 lines
6'h26	312 lines
6'h27	320 lines
6'h28-6'h3F	Setting inhibited

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the R61505V to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

Table 43 GRAM Data-grayscale level inversion

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the R61505V starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

Table 44

VLE	Base image
0	Fixed
1	Enable scrolling

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

Table 45

NDL	Non-display area	
	Positive	Negative
0	V63	V0
1	V0	V63

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure $VL[8:0] \leq 320$.

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

Table 46

SCN[5:0]	Gate Line No (Scan start position)			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G1	G(N)	G1	G(2N – 320)
6'h01	G9	G(N+8)	G16	G(2N – 304)
6'h02	G17	G(N+16)	G33	G(2N – 288)
6'h03	G25	G(N+24)	G49	G(2N – 272)
6'h04	G33	G(N+32)	G65	G(2N – 256)
6'h05	G41	G(N+40)	G81	G(2N – 240)
6'h06	G49	G(N+48)	G97	G(2N – 224)
6'h07	G57	G(N+56)	G113	G(2N – 208)
6'h08	G65	G(N+64)	G129	G(2N – 192)
6'h09	G73	G(N+72)	G145	G(2N – 176)
6'h0A	G81	G(N+80)	G161	G(2N – 160)
6'h0B-6'h2F	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

When setting the SCN bit, make sure to satisfy the restriction below:

Table 47

SM	GS	Restriction
0	0	$(\text{Scan start position} - 1) + (\text{Number of line (NL bit)}) \leq 320$
0	1	Scan start position ≤ 320
1	0	$(\text{Scan start position} - 1)/2 + (\text{Number of line (NL bit)}) \leq 320$
1	1	Scan start position ≤ 320

Partial Display Control Instruction**Partial Image Display Position (R80h)****Partial Image RAM Address (Start Line Address) (R81h)****Partial Image RAM Address (End Line Address) (R82h)**

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R 80	W	1	0	0	0	0	0	0	0	PTDP [8]	PTDP [7]	PTDP [6]	PTDP [5]	PTDP [4]	PTDP [3]	PTDP [2]	PTDP [1]	PTDP [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 81	W	1	0	0	0	0	0	0	0	PTSA [8]	PTSA [7]	PTSA [6]	PTSA [5]	PTSA [4]	PTSA [3]	PTSA [2]	PTSA [1]	PTSA [0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R 82	W	1	0	0	0	0	0	0	0	PTE A[8]	PTE A[7]	PTE A[6]	PTE A[5]	PTE A[4]	PTE A[3]	PTE A[2]	PTE A[1]	PTE A[0]
	Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP[8:0]: Sets the display position of partial image.

If PTDP0 = “9’h000”, the partial image is displayed from the first line of the base image.

PTSA[8:0], PTEA[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image. In setting, make sure that PTSA ≤ PTEA.

Panel Interface Control

Panel Interface Control 1(R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI [1]	DIVI [0]	0	0	0	RTNI [4]	RTNI [3]	RTNI [2]	RTNI [1]	RTNI [0]
Default value		0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the R61505V's display operation is synchronized with internal clock.

Table 48 Clocks per line (internal clock operation: 1 clock = 1 OSC)

RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line	RTNI[4:0]	Clocks per Line
5'h00-5'h0F	Setting inhibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

Note: In Power Supply Instruction Setting, Deep Standby Exit Sequence and Sleep Mode Exit Sequence, RTNI bit must be set at the "Initial instruction setting" stage.

DIVI[1:0]: Sets the division ratio of the internal clock frequency. The R61505V's internal operation is synchronized with the frequency divided internal clock. When DIVI[1:0] setting is changed, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, adjust the frame frequency too. For details, see "Frame-Frequency Adjustment Function".

The setting in DIVI[1:0] is disabled in RGB interface operation. Setting DIVI \neq 2'h0 is inhibited.

Table 49 Division ratio of the internal clock

DIVI[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Note: In Power Supply Instruction Setting, Deep Standby Exit Sequence and Sleep Mode Exit Sequence, DIVI bit must be set at the "Initial instruction setting" stage.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{f_{osc}}{\text{Clocks per line} \times \text{division ratio} \times (\text{line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

f_{osc} : Internal oscillation frequency

Line: Number of lines to drive the LCD (NL bits)

Division ratio: DIVI

Clocks per line: RTNI

Panel Interface Control 1-1 (R91h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	SPCWI[3]	SPCWI[2]	SPCWI[1]	SPCWI[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SPCWI [3:0]: The bit is used to set source VCI pre-charge period. Pre-charge period is set by SPCWI[3:0] starting from the source output alternating position defined by SPCWI [3:0]. This bit is disabled when RGB interface is selected.

Table 50

SPCWI [3:0] Source VCI pre-charge period

3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks
3'h8	8 clocks
3'h9	9 clocks
3'hA	10 clocks
3'hB	11 clocks
3'hC	12 clocks
3'hD	13 clocks
3'hE	14 clocks
3'hF	15 clocks

Note: The unit clock here is the frequency divided clock, which is set according to the division ratio set by DIVI (R90h).

Panel Interface Control 2(R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOW I[2]	NOW I[1]	NOW I[0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

Table 51

NOWI[2:0]	Non-overlap period	NOWI[2:0]	Non-overlap period
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: The internal clock is the frequency divided clock, which is set by DIVI (R90h) bits.

Panel Interface Control 3(R93h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	VEQWI[2]	VEQWI[1]	VEQWI[0]	0	0	0	0	0	MCP I[2]	MCP I[1]	MCP I[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

VEQWI[2:0]: Sets VCOM equalize period. Equalizing operation continues for the period defined by VEQWI bit starting from the VCOM alternating position defined by MCPI[2:0]. VEQWI setting is enabled when VEM[1:0]=1 or larger (R0Eh) and display operation of the R61505V is synchronized with internal clock.

VEQWI is disabled when RGB interface is selected.

Table 52**VEQWI[2:0] VCOM equalize period**

3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: DIVI (R90h) sets division ratio of clock frequency.

MCPI[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled display operation of the R61505V is synchronized with internal clock.

The setting is enabled in display operation via RGB interface.

Table 53

MCPI[2:0]	Source output position	MCPI[2:0]	Source output position
3'h0	Setting inhibited	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: DIVI (R90h) sets division ratio of clock frequency.

Panel Interface Control 4 (R94h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDT I[2]	SDT I[1]	SDT I[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SDTI[2:0]: Defines source output alternating position within 1H period.

SDTI is disabled when RGB interface is selected.

Table 54

SDTI[2:0]	Source output alternating position
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: DIVI (R90h) sets division ratio of clock frequency.

Panel Interface Control 5 (R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE [1]	DIVE [0]	0	0	RTN E[5]	RTN E[4]	RTN E[3]	RTN E[2]	RTN E[1]	RTN E[0]
Default value		0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0

RTNE[5:0]: Sets RTNE[5:0] and DIVE[1:0] bits so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK which should be inputted in 1H period. The RTNE[5:0] setting is enabled in display operation via RGB interface.

$(PCDIVH + PCDIVL) \times DIVE[1:0] \text{ (division ratio)} \times RTNE[5:0] \text{ (Number of DOTCLK)} \leq \text{Number of DOTCLK in 1H period}$

DIVE[1:0]: Sets the division ratio of DOTCLK frequency. The R61505V's internal operation is synchronized with the frequency divided DOTCLK. The setting in DIVE[1:0] is enabled in RGB interface operation.

Table 55 Division ratio of DOTCLK**DIVE[1:0] Division Ratio**

2'h0	Setting disabled
2'h1	1/4
2'h2	1/8
2'h3	1/16

Internal clock frequency is calculated by below formula:

$$\text{DOTCLK} / (\text{DIVE} \times (\text{PCDIVL} + \text{PCDIVH}))$$

See also R9Ch.

Table 56 DOTCLK per line (1H period)

RTNE[5:0]	DOTCLK per line (1H)	RTNE[5:0]	DOTCLK per line (1H)
6'h00	Setting disabled	6'h20	32 clocks
6'h01	Setting disabled	6'h21	33 clocks
6'h02	Setting disabled	6'h22	34 clocks
6'h03	Setting disabled	6'h23	35 clocks
6'h04	Setting disabled	6'h24	36 clocks
6'h05	Setting disabled	6'h25	37 clocks
6'h06	Setting disabled	6'h26	38 clocks
6'h07	Setting disabled	6'h27	39 clocks
6'h08	Setting disabled	6'h28	40 clocks
6'h09	Setting disabled	6'h29	41 clocks
6'h0A	Setting disabled	6'h2A	42 clocks
6'h0B	Setting disabled	6'h2B	43 clocks
6'h0C	Setting disabled	6'h2C	44 clocks
6'h0D	Setting disabled	6'h2D	45 clocks
6'h0E	Setting disabled	6'h2E	46 clocks
6'h0F	Setting disabled	6'h2F	47 clocks
6'h10	16 clocks	6'h30	48 clocks
6'h11	17 clocks	6'h31	49 clocks
6'h12	18 clocks	6'h32	50 clocks
6'h13	19 clocks	6'h33	51 clocks
6'h14	20 clocks	6'h34	52 clocks
6'h15	21 clocks	6'h35	53 clocks
6'h16	22 clocks	6'h36	54 clocks
6'h17	23 clocks	6'h37	55 clocks
6'h18	24 clocks	6'h38	56 clocks
6'h19	25 clocks	6'h39	57 clocks
6'h1A	26 clocks	6'h3A	58 clocks
6'h1B	27 clocks	6'h3B	59 clocks
6'h1C	28 clocks	6'h3C	60 clocks
6'h1D	29 clocks	6'h3D	61 clocks
6'h1E	30 clocks	6'h3E	62 clocks
6'h1F	31 clocks	6'h3F	63 clocks

Panel Interface Control 5-1 (R96h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	SPC WE [3]	SPC WE [2]	SPC WE [1]	SPC WE [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SPCWE [3:0]: The bit is used to set source VCI pre-charge period. Pre-charge period is set by SPCWE[3:0] starting from the source output alternating position defined by SPCWE [3:0]. This bit is enabled when RGB interface is selected.

Table 57

SPCWE [3:0]	Source VCI pre-charge period
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks
3'h8	8 clocks
3'h9	9 clocks
3'hA	10 clocks
3'hB	11 clocks
3'hC	12 clocks
3'hD	13 clocks
3'hE	14 clocks
3'hF	15 clocks

Panel Interface Control 6 (R97h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOW E[2]	NOW E[1]	NOW E[0]	0	0	0	0	0	0	0	0
Default value		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

NOWE[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

Table 58**NOWE [2:0] Non-overlap period**

3'h0	Setting disabled
3'h1	1
3'h2	2
3'h3	3
3'h4	4
3'h5	5
3'h6	6
3'h7	7

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK].

Panel Interface Control 7 (R98h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	VEQWE [2]	VEQWE [1]	VEQWE [0]	0	0	0	0	0	MCPE [2]	MCPE [1]	MCPE [0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

VEQWE [2:0]: VEQWE sets VCOM equalize period. Equalizing operation continues for the period defined by VEQWE bit starting from the VCOM alternating position defined by MCPE [2:0]. VEQWE setting is enabled when VEM[1:0]=1 or larger (R0Eh).

Table 59**VEQWE[2:0] VCOM equalize period**

3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

MCPE[2:0]: Sets the source output timing by the number of internal clock from the reference point. The setting is enabled in display operation via RGB interface.

Table 60

MCPE[2:0]	Source output position	MCPE[2:0]	Source output position
3'h0	Setting Disabled	3'h4	4 clocks
3'h1	1 clock	3'h5	5 clocks
3'h2	2 clocks	3'h6	6 clocks
3'h3	3 clocks	3'h7	7 clocks

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK].

Panel Interface Control 8 (R99h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE[2]	SDTE[1]	SDTE[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SDTE[2:0]: Defines source output alternating position within 1H period.

SDTE is enabled when RGB interface is selected.

Table 61

SDTE[2:0]	Source output alternating position
3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK]

Panel Interface Control 9 (R9Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	PCD IVH [2]	PCD IVH [1]	PCD IVH [0]	0	PCD IVL [2]	PCD IVL [1]	PCD IVL [0]
Default		0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

PCDIVH[2:0], PCDIVL[2:0]:

When DM [1:0] = 2'h1 and RGB I/F is selected, internal clock used for display operation switches from internal oscillation to DOTCLKD. PCDIVH and PCDIVL bits define division ratio of DOTCLKD to DOTCLK.

PCDIVH defines number of DOTCLK during DOTCLKD is high in the units of 1 clock.

PCDIVL defines number of DOTCLK during DOTCLKD is low in the units of 1 clock.

Make sure that PCDIVL = PCDIVH or PCDIVH-1.

Also, write PCDIVH and PCDIVL values so that DOTCLKD frequency is the closest to internal oscillation clock frequency 600KHz.

See “Setting Example of Display Control Clock in RGB Interface Operation” for details.

Table 62**PCDIVH[2:0]**

3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Table 63**PCDIVL[2:0]**

3'h0	Setting inhibited
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

NVM (NON-VOLATILE MEMORY) Control**NVM Control 1 (RA0h), NVM Control 2 (RA1h)**

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R A0	R/W	1	0	0	0	0	0	0	0	0	TE	0	EOP [1]	EOP [0]	0	0	NV AD [1]	NV AD [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R A1	R/W	1	NV DAT [15]	NV DAT [14]	NV DAT [13]	NV DAT [12]	NV DAT [11]	NV DAT [10]	NV DAT [9]	NV DAT [8]	NV DAT [7]	NV DAT [6]	NV DAT [5]	NV DAT [4]	NV DAT [3]	NV DAT [2]	NV DAT [1]	NV DAT [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TE: Enables access to the NVM when TE=1.

EOP [1:0]: Internal NVM control bits to control write and erase operations.

Table 64

EOP[1:0]	NVM control
2'h0	Halt
2'h1	Write
2'h2	Setting disabled
2'h3	Erase

NVAD: Specifies address to access on the NVM for write and erase operation. An address consists of 16 bits. To write to the NVM, write the data that users wish to write in NVDAT (RA1h) and write EOP=2'h1 to enable the write operation. To erase, define the address users wish to erase data from and write EOP=2'h3 to enable the erase operation. See “NVM Control Sequence” for details.

Table 65

NVAD[1:0]	NVDAT [15]/[7]	NVDAT [14]/[6]	NVDAT [13]/[5]	NVDAT [12]/[4]	NVDAT [11]/[3]	NVDAT [10]/[2]	NVDAT [9]/[1]	NVDAT [8]/[0]
2'h0 (MS byte)	VCMSEL	VCM1 [6]	VCM1 [5]	VCM1 [4]	VCM1 [3]	VCM1 [2]	VCM1 [1]	VCM1 [0]
2'h0 (LS byte)	1	VCM2 [6]	VCM2 [5]	VCM2 [4]	VCM2 [3]	VCM2 [2]	VCM2 [1]	VCM2 [0]
2'h1 (MS byte)	1	1	1	1	UID1 [3]	UID1 [2]	UID1 [1]	UID1 [0]
2'h1 (LS byte)	1	1	1	1	1	1	1	1

MS byte =NVDAT [15:8]. LS byte=NVDAT [7:0].

VCM1[6:0]: Defines factor to adjust VCOMH level when VCMSEL=1.

VCM2[6:0]: Defines factor to adjust VCOMH level when VCMSEL=0.

UID1[3:0]: User ID.

NVM Control 3 (RA3h), NVM Control 4 (RA4h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R A3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NV VRF	0	0
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R A4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CAL B
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NVVRF: Defines erase verify mode. Used only in the erase sequence. See “NVM Erase Sequence” for details.

CALB: When CALB=1, all data in NVM is read out and written to internal registers. When finished, CALB is set to 0.

●R61505V Instruction List

Rev 1.00 2008.01.31
Rev 1.10 2008.02.05

Main category	Sub Category	Upper Code	Lower Code	Note
Index	Index	Index	Index	
0*	00h Device Code Read (Default)	ALMD1[7]	ALMD1[0]	Device code "8505"
01h	Driver Output Control (Default)	0	0	
02h	LCD Drive Wave Control (Default)	0	0	
03h	Entry Mode (Default)	TRREQ	DEFM	
07h	Display Control 1 (Default)	0	0	
08h	Display Control 2 (Default)	FP0[1]	FP0[0]	
09h	Display Control 3 (Default)	0	0	
0Ah	Display Control 4 (Default)	0	0	
0Ch	External Display Interface Control 1 (Default)	0	0	
0Dh	Frame Master Position (Default)	0	0	
0Eh	VCOM Low Power Control (Default)	0	0	
0Fh	External Display Interface Control 2 (Default)	0	0	
1*	10h Power Control 1 (Default)	0	0	
11h	Power Control 2 (Default)	0	0	
12h	Power Control 3 (Default)	0	0	
13h	Power Control 4 (Default)	0	0	
2*	20h RAM Address Set (Horizontal Address) (Default)	0	0	
21h	RAM Address Set (Vertical Address) (Default)	0	0	
22h	RAM Data Write / RAM Data Read (Default)	0	0	
23h	NVM Data Read 1 (Default)	0	0	
24h	NVM Data Read 2 (Default)	0	0	
2Ah	NVM Data Read 3 (Default)	0	0	
3*	30h γ Control 1 (Default)	0	0	
31h	γ Control 2 (Default)	0	0	
32h	γ Control 3 (Default)	0	0	
33h	γ Control 4 (Default)	0	0	
34h	γ Control 5 (Default)	0	0	
35h	γ Control 6 (Default)	0	0	
36h	γ Control 7 (Default)	0	0	
37h	γ Control 8 (Default)	0	0	
38h	γ Control 9 (Default)	0	0	
39h	γ Control 10 (Default)	0	0	
5*	50h Window Horizontal RAM Address (Start Address) (Default)	0	0	
51h	Window Horizontal RAM Address (End Address) (Default)	0	0	
52h	Window Vertical RAM Address (Start Address) (Default)	0	0	
53h	Window Vertical RAM Address (End Address) (Default)	0	0	
6*	60h Driver Output Control (Default)	0	0	
61h	Base Image Display Control (Default)	0	0	
6Ah	Vertical Scroll Control (Default)	0	0	
8*	80h Partial Image Display Position (Default)	0	0	
81h	Partial Image RAM Address (Start Line Address) (Default)	0	0	
82h	Partial Image RAM Address (End Line Address) (Default)	0	0	
9*	90h Panel Interface Control 1 (Default)	0	0	
91h	Panel Interface Control 2 (Default)	0	0	
92h	Panel Interface Control 3 (Default)	0	0	
93h	Panel Interface Control 4 (Default)	0	0	
94h	Panel Interface Control 5 (Default)	0	0	
95h	Panel Interface Control 6 (Default)	0	0	
96h	Panel Interface Control 7 (Default)	0	0	
97h	Panel Interface Control 8 (Default)	0	0	
98h	Panel Interface Control 9 (Default)	0	0	
A*	A0h NVM Control 1 (Default)	0	0	
A1h	NVM Control 2 (Default)	0	0	
A2h	NVM Control 3 (Default)	0	0	
A3h	NVM Control 4 (Default)	0	0	

Reset Function

The R61505V is initialized by the RESET input. During reset period, the R61505V is in a busy state and instruction from the host processor and GRAM access are not accepted. The R61505V's internal power supply circuit unit is initialized also by the RESET input.

1. Initial state of instruction bits (default)

See the instruction list. The default values are shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period.

3. Output pin initial state

Pin name	After H/W reset
DB[17:0]	Hi-Z
SDO	Hi-Z
FMARK	GND
VDD	1.5V
VCI1	Hi-Z
C11P/C11M	Hi-Z/Hi-Z
C12P/C12M	Hi-Z/Hi-Z
C13P/C13M	Hi-Z/GND
C21P/C21M	VCI/GND
C22P/C22M	VCI/GND
VREG1OUT	GND
VCOML	GND
VCOMH	VCI(DDVDH)
VCL	GND
VGL	GND
VGH	VCI
DDVDH	VCI
VCOM	GND
VCOMOL/VCOMOR	GND
S1-720	GND
G1-320	GND

Basic Operation

The basic operation modes of the R61505V are shown in the following diagram.. When making a transition from one mode to another, refer to instruction setting sequence.

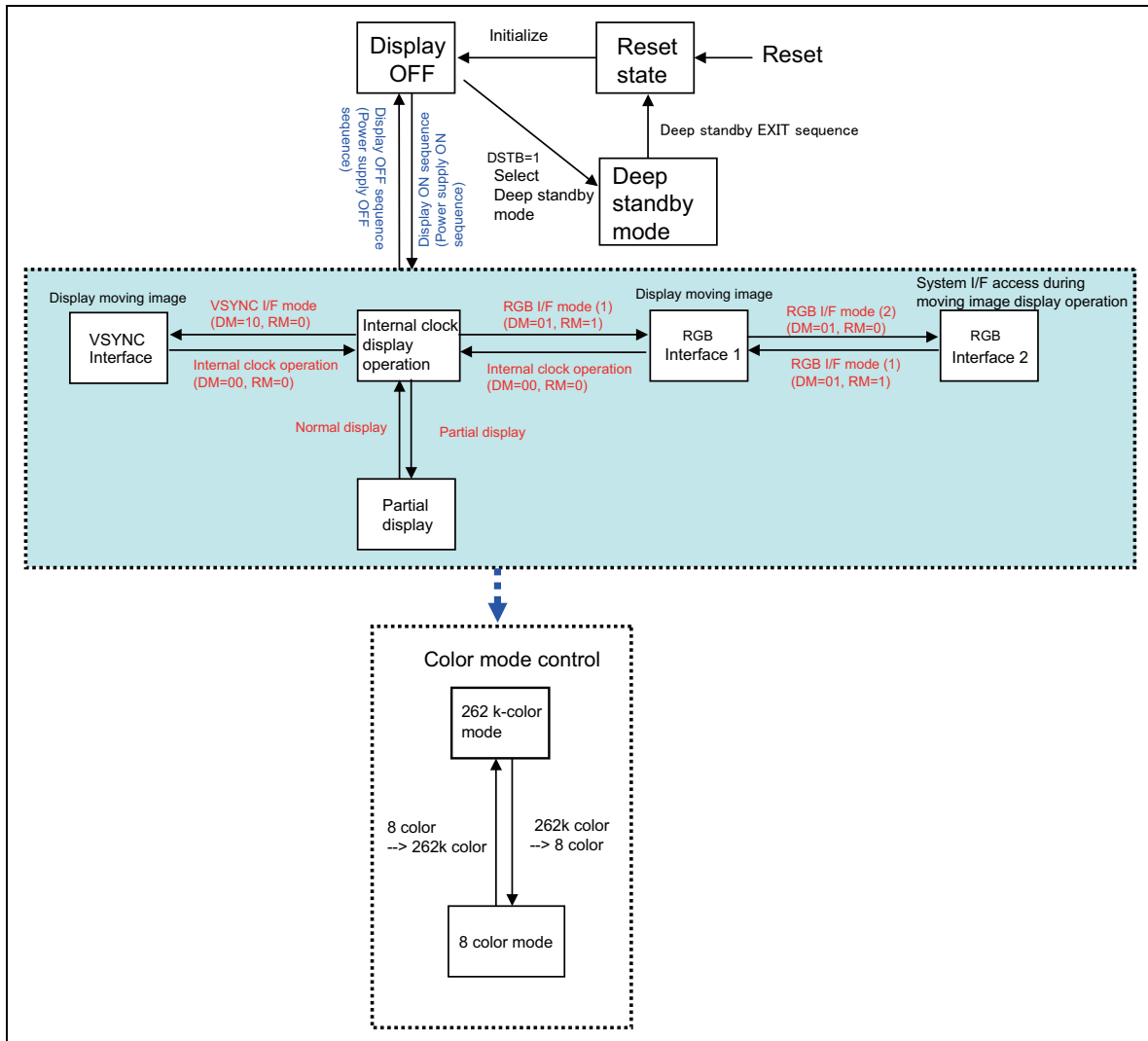


Figure 10

Interface and Data Format

The R61505V supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The R61505V can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the R61505V supports RGB interface and VSYNC interface, which enables data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the R61505V writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the R61505V's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The R61505V operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 66 Operation Modes

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

- Notes:
1. Instructions are set only via system interface.
 2. The RGB and VSYNC interfaces cannot be used simultaneously.
 3. Do not change RGB interface operation setting (RIM1-0) during RGB interface operation.
 4. See the "External Display Interface" section for the sequences when switching from one mode to another.

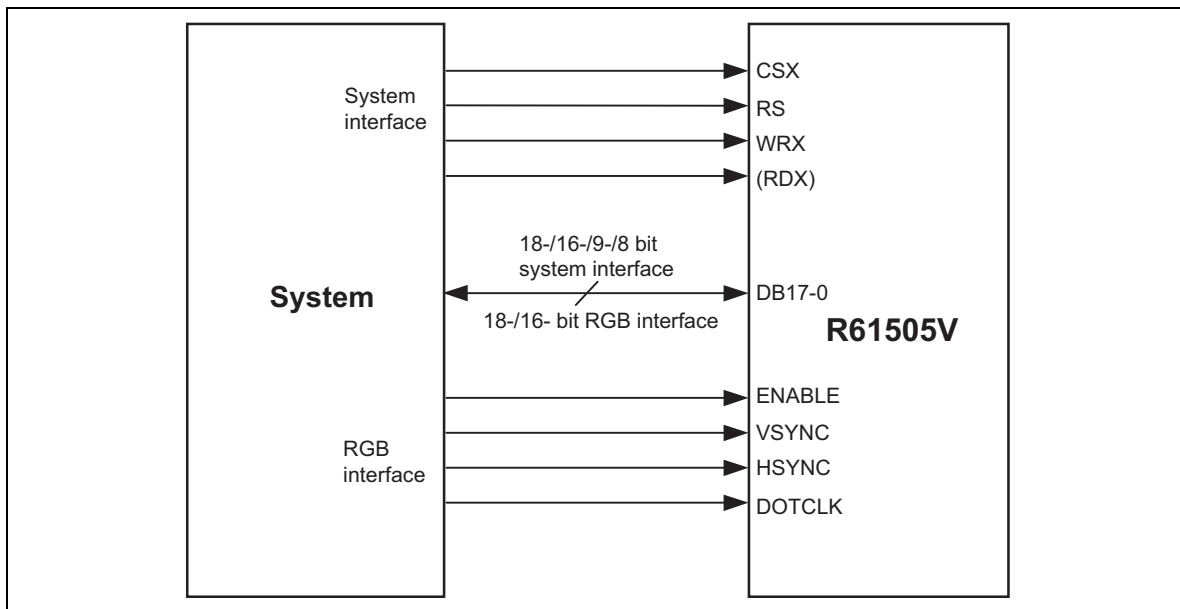


Figure 11

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61505V transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. Window address function can minimize the total number of data transfer for moving picture display because only the moving picture data is transferred to the RAM, enabling the R61505V to display a moving picture and another image stored in the RAM simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61505V by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the setting of these periods.

RGB interface operation (2)

This mode enables the R61505V to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the RAM address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61505V to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the “VSYNC Interface” section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61505V according to the instruction settings for these periods.

FMARK interface operation

In the FMARK interface operation, data is written to internal RAM via system interface synchronizing with the frame mark signal (FMARK), realizing tearing-less moving picture while using conventional system interface. In this case, there are restrictions in speed and method of writing RAM data. See “FMARK interface” for detail.

System Interface

The following are the kinds of system interfaces available with the R61505V. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 67 IM Bit Settings and System Interface

IM3	IM2	IM1	IM0	Interfacing Mode with Host processor	DB Pins	Colors
0	0	0	0	Setting inhibited	-	-
0	0	0	1	Setting inhibited	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 *see Note1
0	0	1	1	80-system 8-bit interface	DB17-10	262,144 *see Note2
0	1	0	0	Clock synchronous serial interface	-	65,536
0	1	0	1	Setting inhibited	-	-
0	1	1	0	Setting inhibited	-	-
0	1	1	1	Setting inhibited	-	-
1	0	0	0	Setting inhibited	-	-
1	0	0	1	Setting inhibited	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	262,144
1	0	1	1	80-system 9-bit interface	DB17-9	262,144
1	1	0	0	Setting inhibited	-	-
1	1	0	1	Setting inhibited	-	-
1	1	1	0	Setting inhibited	-	-
1	1	1	1	Setting inhibited	-	-

Notes: 1. 262,144 colors in 16-bit 2-transfer mode.
2. 262,144 colors in 8-bit 2-transfer mode.

80-system 18-bit Bus Interface

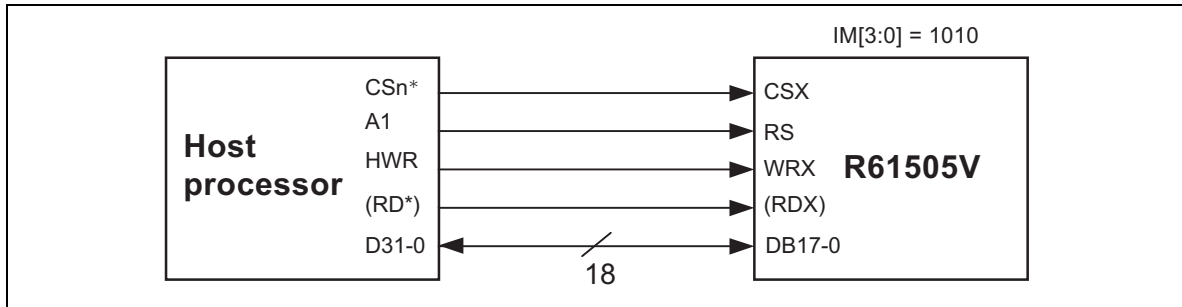


Figure 12 18-bit interface

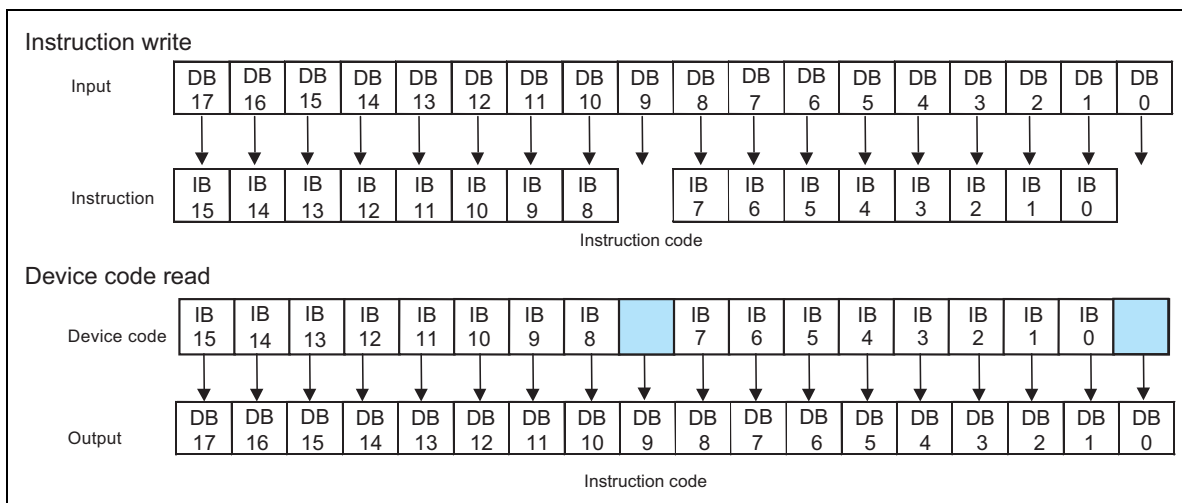


Figure 13 18-bit Interface Data Format (Instruction Write / Device Code Read) (IM[3:0]=1010)

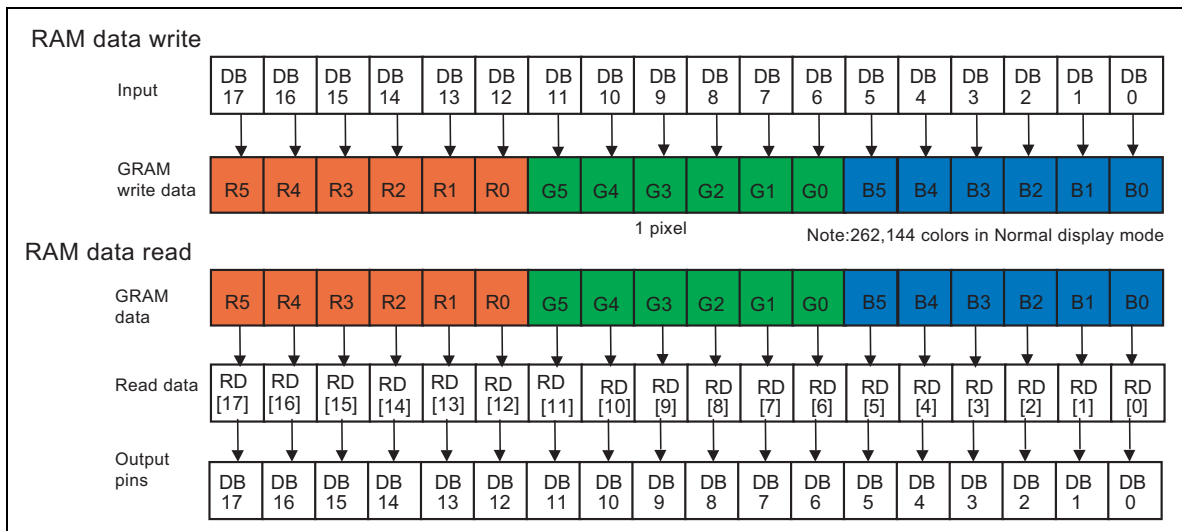


Figure 14 18-bit Interface Data Format (RAM Data Write / RAM Data Read)

80-system 16-bit Bus Interface

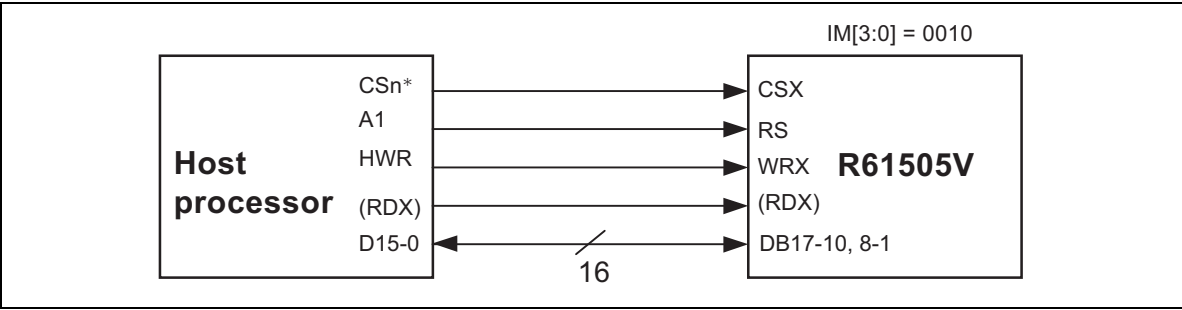


Figure 15 16-bit interface

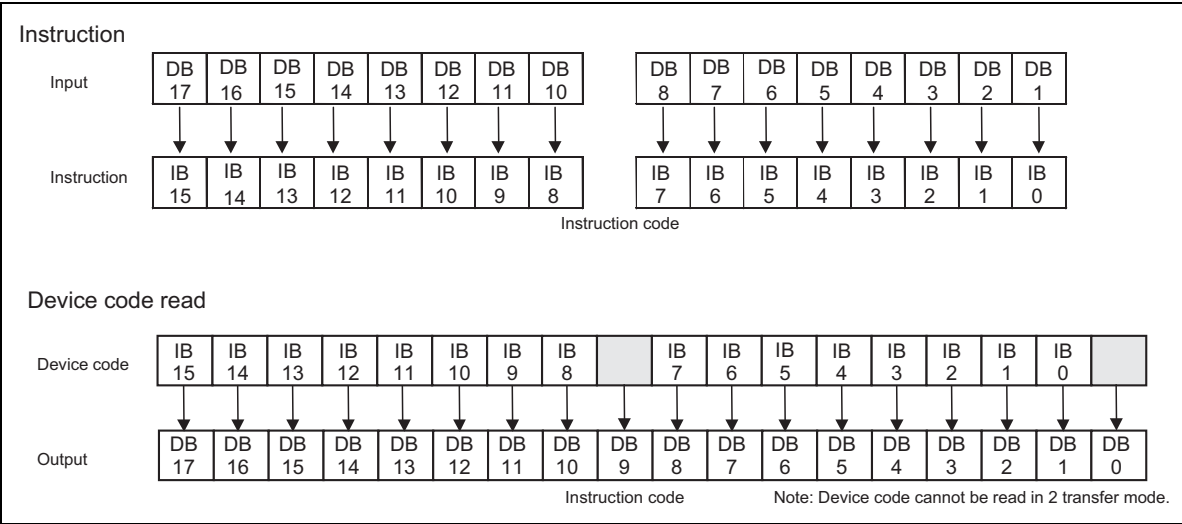
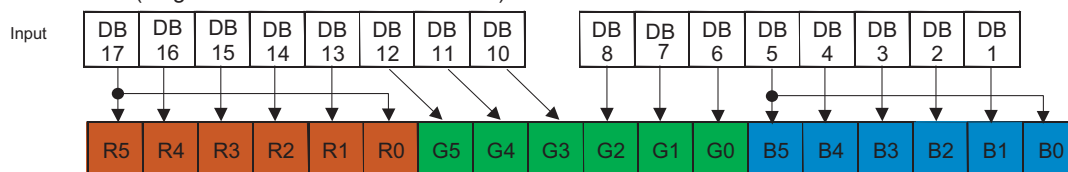


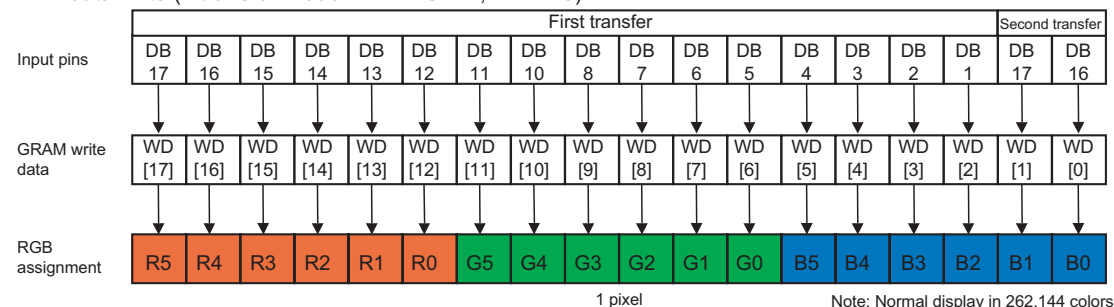
Figure 16 16-bit Interface Data Format (Instruction Write / Device Code Read)

RAM data write (single transfer mode: TRIREG = 0)



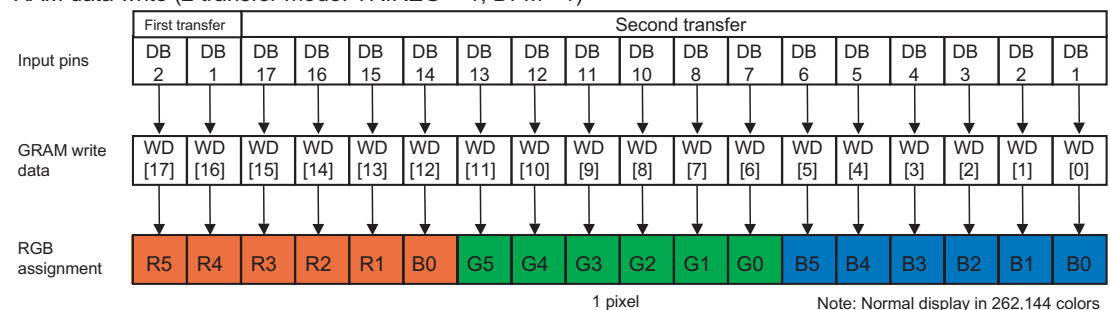
Note: Normal display in 65,536 colors

RAM data write (2 transfer mode: TRIREG = 1, DFM = 0)



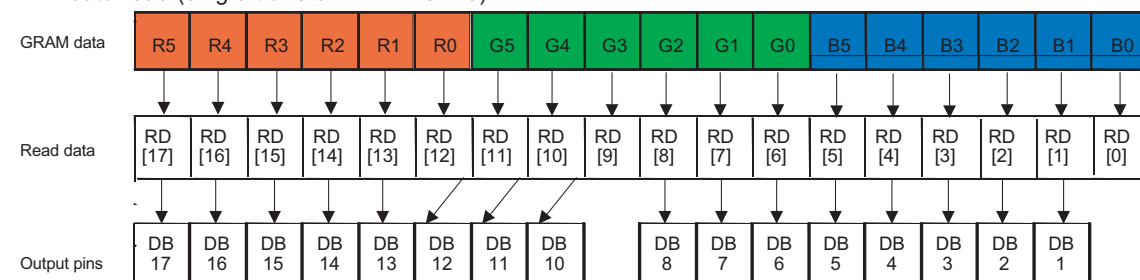
Note: Normal display in 262,144 colors

RAM data write (2 transfer mode: TRIREG = 1, DFM = 1)



Note: Normal display in 262,144 colors

RAM data read (single transfer: TRIREG = 0)



Note: Data cannot be read in 2-transfer operation.

Figure 17 16-bit Interface Data Format (RAM data write / RAM data read)

Data Transfer Synchronization in 16-bit Bus Interface operation

The R61505V supports data transfer synchronization function to reset the counters for upper 16-/2-bit and lower 2-/16-bit transfers in 16-bit 2-transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 2/16 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

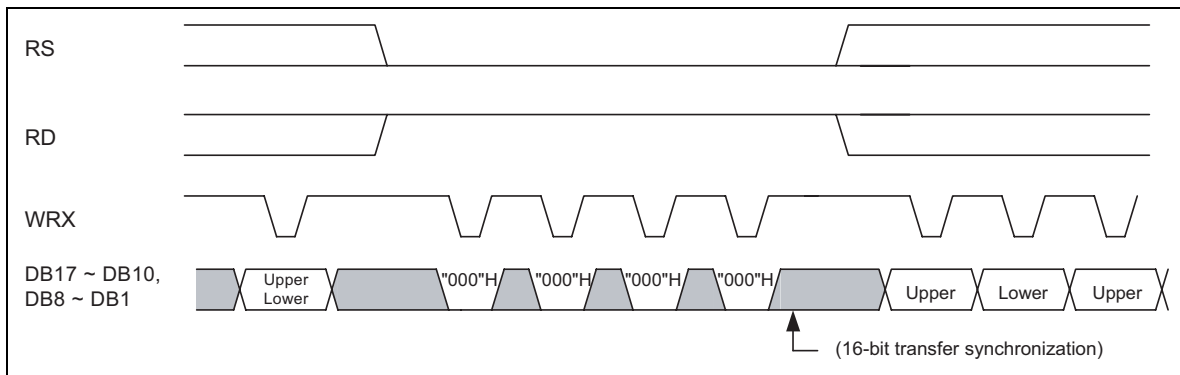


Figure 18 16-bit Data Transfer Synchronization

80-system 9-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

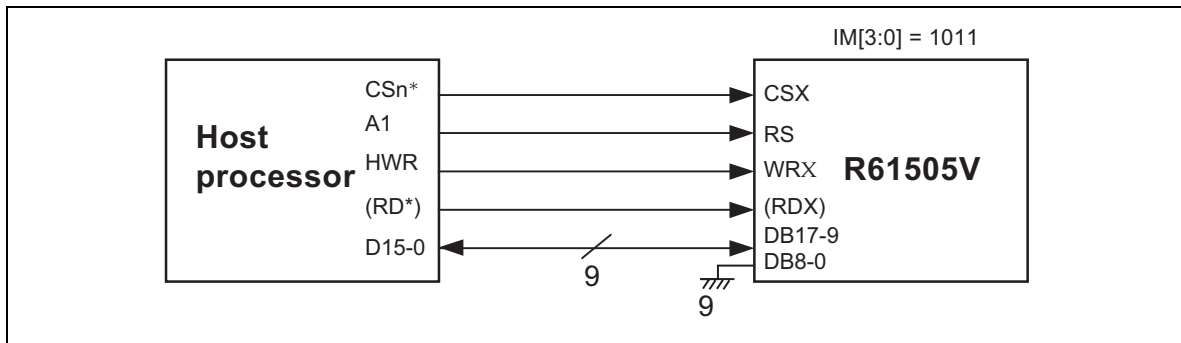


Figure 19 9-bit interface

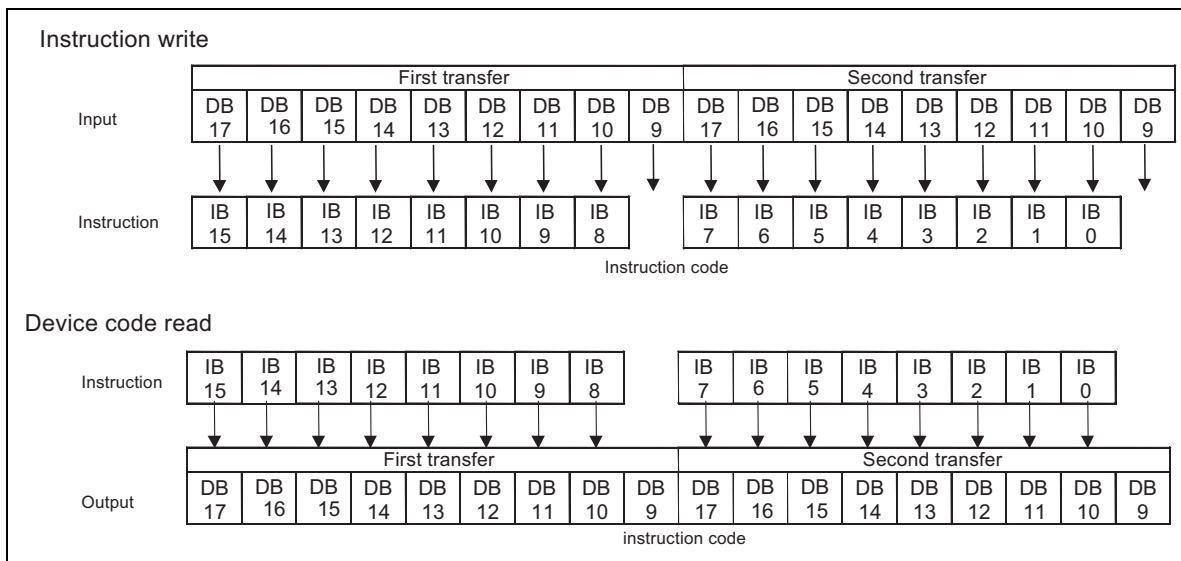


Figure 20 9-bit Interface Data Format (Instruction Write / Device Code Read)

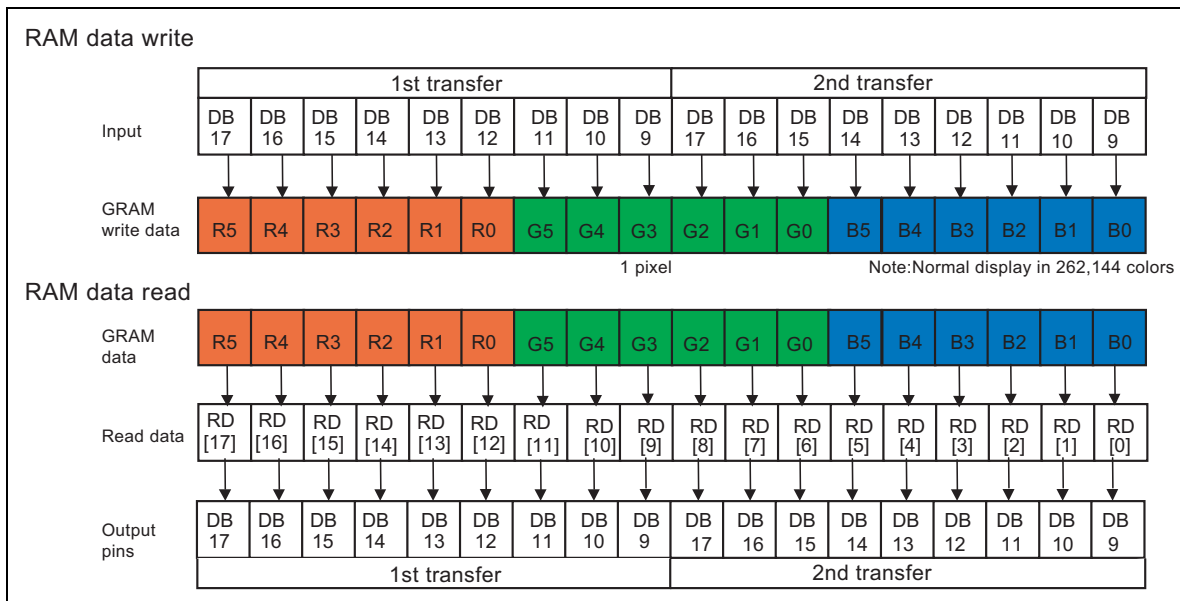


Figure 21 9-bit Interface Data Format (RAM Data Write/ RAM Data Read)

Data Transfer Synchronization in 9-bit Bus Interface operation

The R61505V supports data transfer synchronization function to reset the counters for upper and lower 9-bit transfers in 9-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 9 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

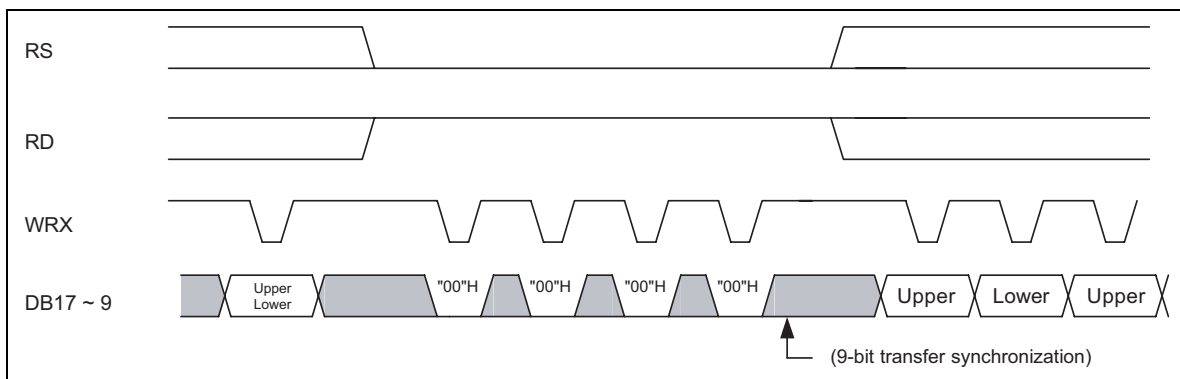


Figure 22 9-bit Data Transfer Synchronization

80-system 8-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either IOVCC or GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

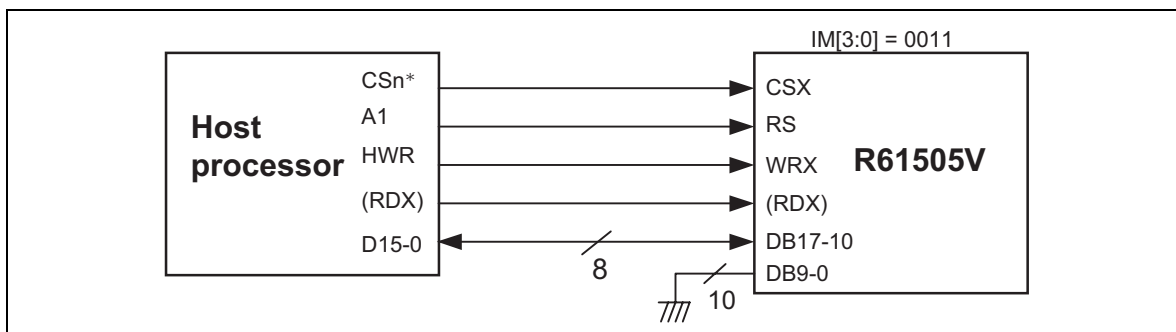


Figure 23 8-bit interface

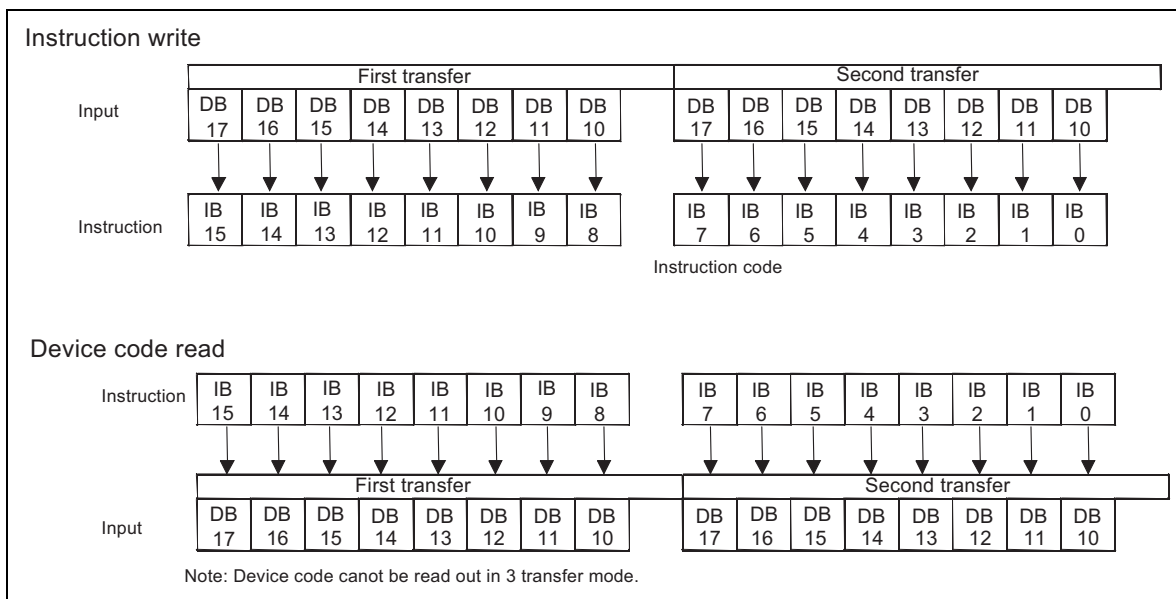


Figure 24 8-bit Interface Data Format (Instruction Write / Device Code Read)

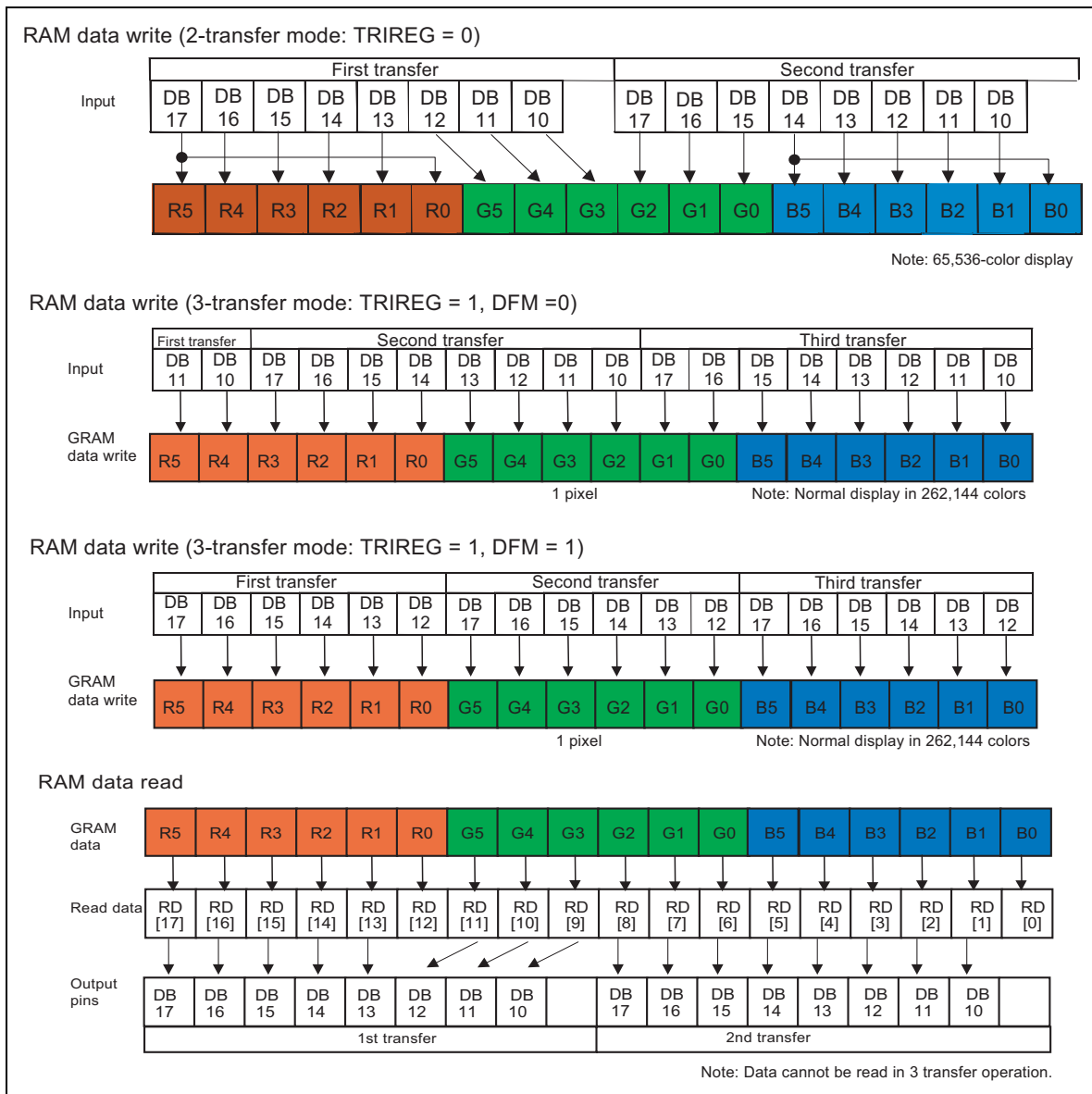


Figure 25 8-bit Interface Data Format (RAM Data Write / RAM Data Read)

Data Transfer Synchronization in 8-bit Bus Interface operation

The R61505V supports data transfer synchronization function to reset the counters for upper and lower 8-bit transfers in 8-bit bus transfer mode. When a mismatch occurs in upper and lower data transfers due to noise and so on, the 00H instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper 8 bits. The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.

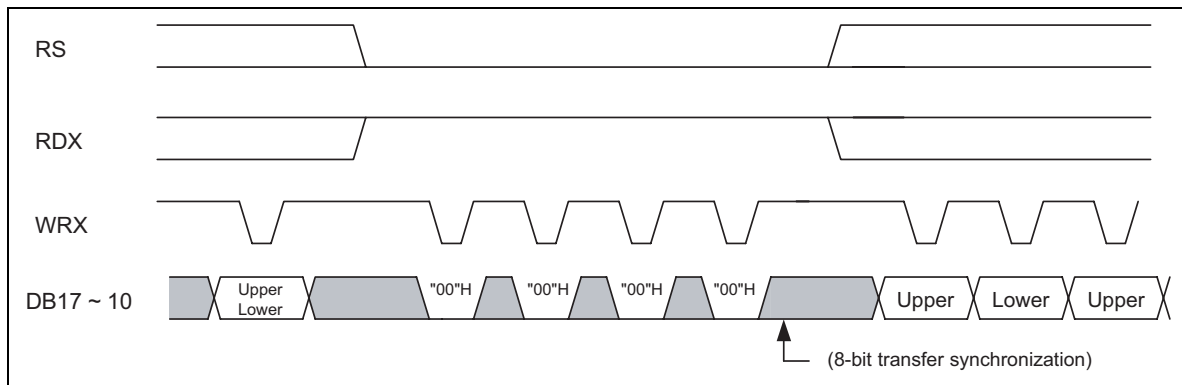


Figure 26 8-bit Data Transfer Synchronization

Serial Interface

The serial interface is selected by setting the IM3/2/1/0 pins to the GND/IOVCC/GND/GND levels, respectively. The data is transferred via chip select line (CSX), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, unused DB17-0 pins must be fixed at either IOVCC or GND level.

The R61505V recognizes the start of data transfer on the falling edge of CSX input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CSX input. The R61505V is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code ("011100") assigned to the R61505V are compared and agreed. Then, the R61505V starts taking in subsequent data. Two different chip addresses must be assigned to the R61505V because the seventh bit of the start byte is register select bit (RS). When RS = 0, index register write operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The R61505V receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The R61505V writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the R61505V starts transferring or receiving data in units of bytes. The R61505V transfers data from the MSB. The R61505V's instruction consists of 16 bits and it is executed inside the R61505V after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The R61505V expands RAM write data into 18 bits when writing them to the internal GRAM. The first byte received by the R61505V following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

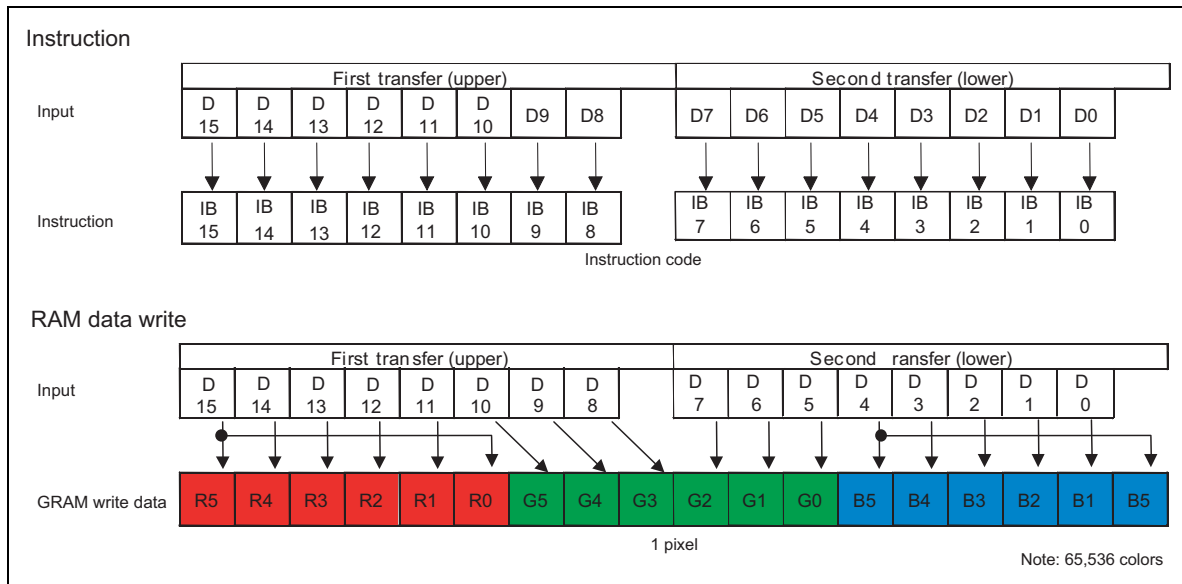
When reading data from the GRAM, valid data is not transferred to the data bus until first five bytes of data are read from the GRAM following the start byte. The R61505V sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 68 Start Byte Format

Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	0		

Table 69 Functions of RS, R/W bits

RS	R/W	Function
0	0	Set index register
0	1	Setting inhibited
1	0	Write instruction or RAM data
1	1	Read register settings or RAM data

**Figure 27 Serial Interface Data Format**

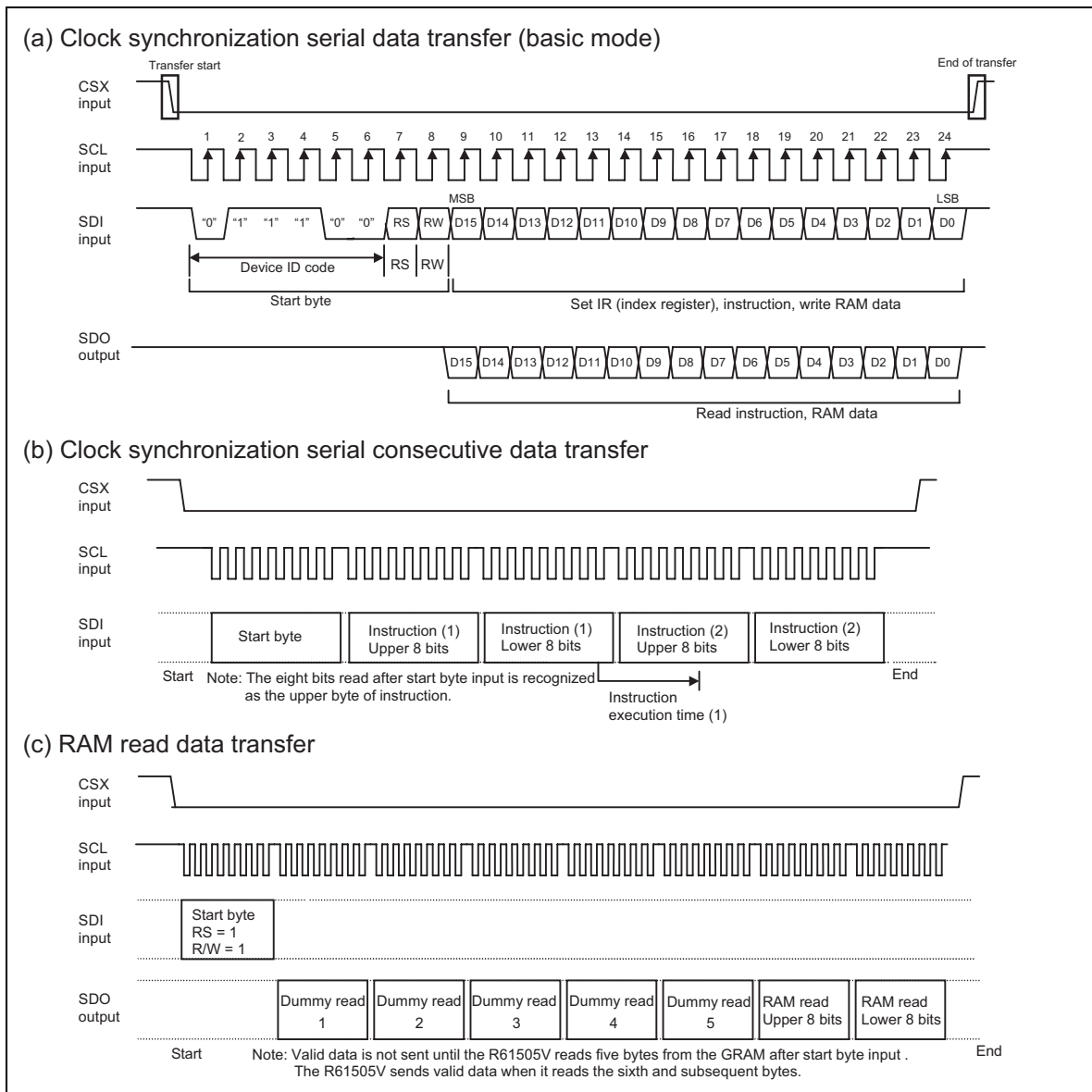


Figure 28 Data Transfer in Serial interface

VSYNC Interface

The R61505V supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

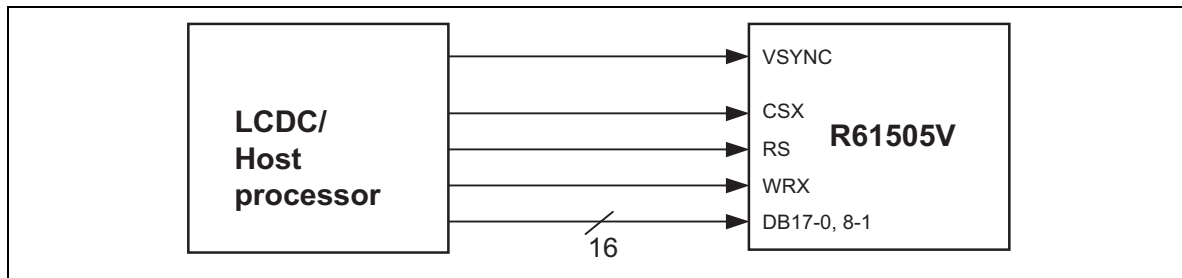


Figure 29 VSYNC Interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the R61505V rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display.

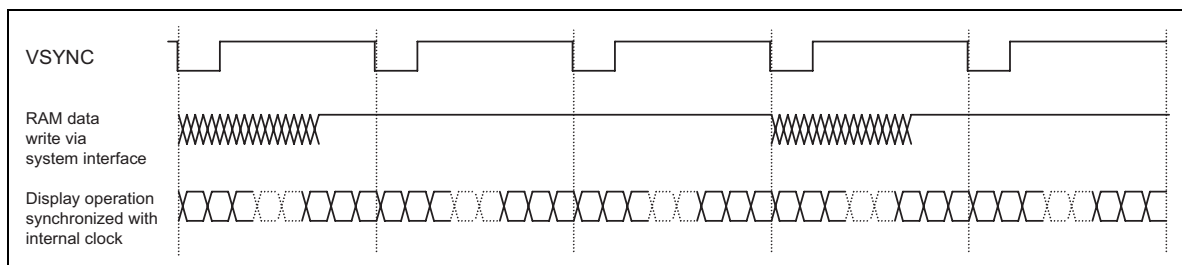


Figure 30 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz]

$$= \text{FrameFrequency} \times (\text{DisplayLines(NL)} + \text{FrontPorch(FP)} + \text{BackPorch(BP)}) \times 16(\text{clocks}) \times \text{variance}$$

$$\text{RAMWriteSpeed}(\text{min.})[\text{Hz}] > \frac{240 \times \text{DisplayLines(NL)}}{((\text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times \text{DivisionRatio} \times \text{ClockPer1H}) \times \frac{1}{f_{osc}}}$$

Note: When RAM write operation does not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel size	240 RGB × 320 lines (NL = 6'h27: 320 lines)
Total number of lines (NL)	320 lines
Back/front porch	13/3 lines (BP = 8'h'D, FP = 8'h3)
Frame frequency	60 Hz
Maximum internal oscillation frequency	600kHz × 1.07 = 642kHz
Clock division ratio (DIVE)	1
Number of clock per 1H period (RTNE)	30

RTN*: RTNI or RTNE. DIV*: DIVI or DIVE.

- Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±7% for variances and guarantee that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM write [Hz]

$$> 240 \times 320 / \{((13 + 320 - 2) \text{ lines} \times 1 \times 30 \text{ clocks}) \times 1/642 \text{ kHz}\} = 4.97 \text{ MHz}$$

- Notes: 1. In this example, it is assumed that the R61505V starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must be at least a margin of 2 lines between the line to which the R61505V has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 4.97MHz or faster, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61505V

starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

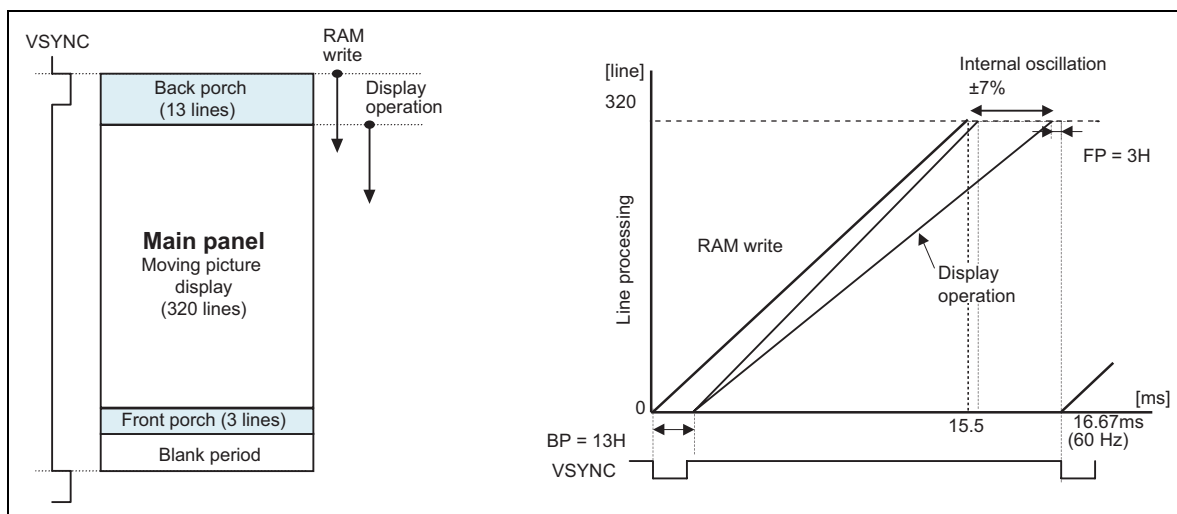


Figure 31 Write/Display Operation Timing via VSYNC Interface

Notes to VSYNC Interface operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margin in setting RAM write speed for VSYNC interface operation.
2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

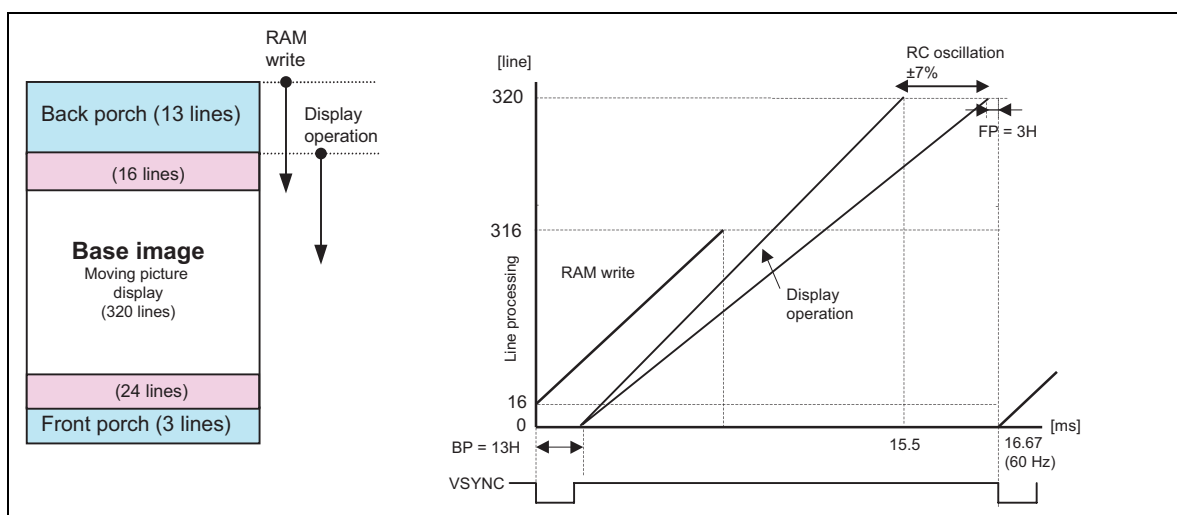


Figure 32 RAM Write Speed Margins

3. The front porch period continues from the end of one frame period to the next VSYNC input.
4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.
5. The partial display and vertical scroll functions are not available in VSYNC interface operation.
6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.

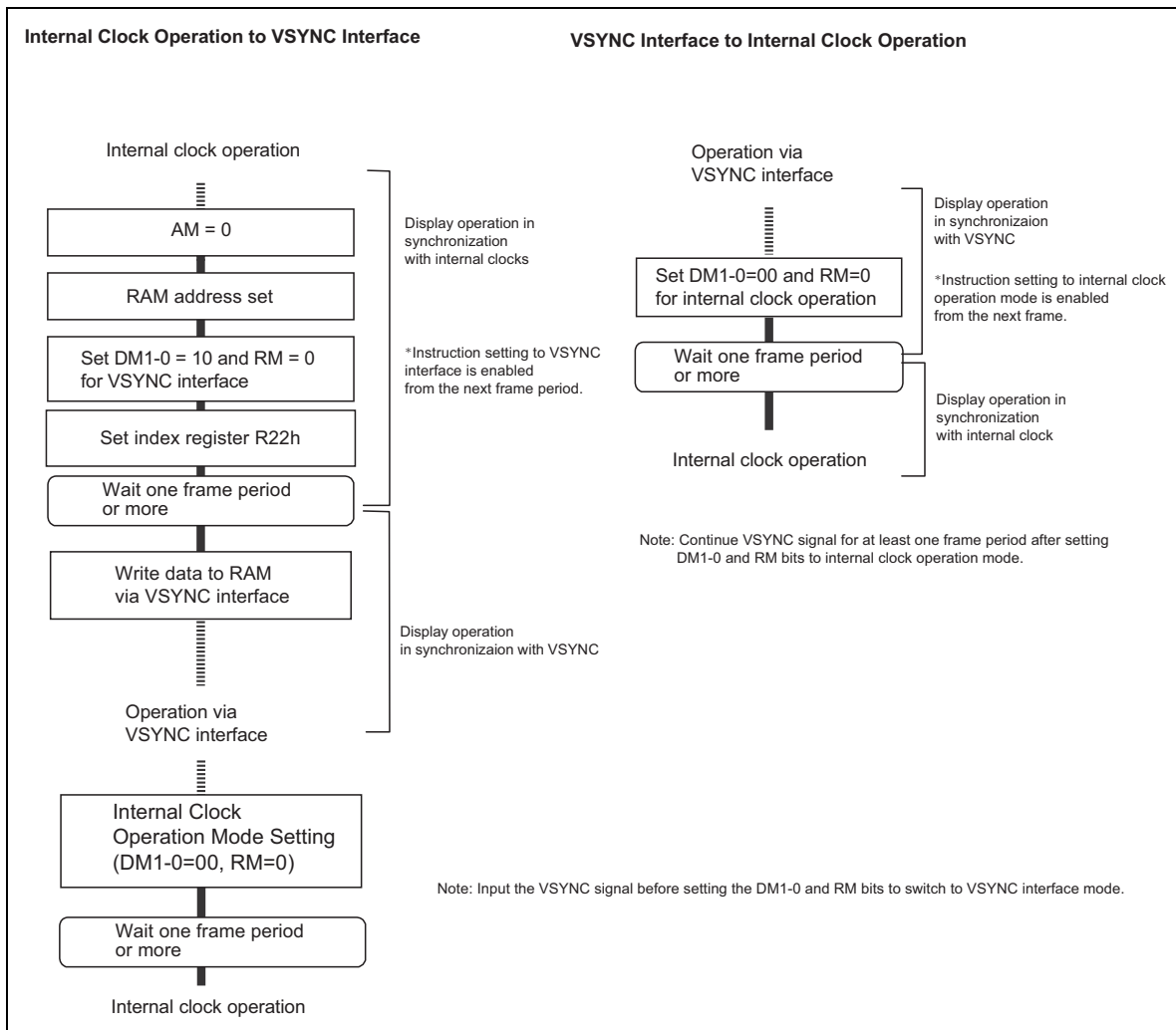


Figure 33 Sequences to Switch between VSYNC and Internal Clock Operation Modes

FMARK Interface

In the FMARK interface operation, data is written to internal RAM via system interface synchronizing with the frame mark signal (FMARK), realizing tearing less video image while using conventional system interface. FMARK output position is set in units of line using FMP bit. Set the bit considering data transfer speed.

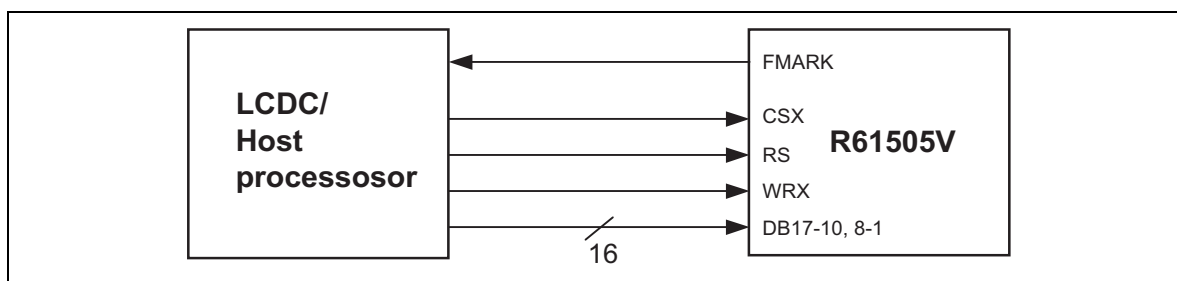


Figure 34 Display synchronous data transfer interface

In this operation, moving picture display is enabled via system interface by writing data at higher than the internal display operation frequency to a certain degree, which guarantees rewriting the moving picture RAM area without causing flicker on the display.

The data is written in the internal RAM. Therefore, when moving picture is displayed, data is written only to the moving picture display area without using RGB or VSYNC interface, minimizing number of data transfer required for moving picture display.

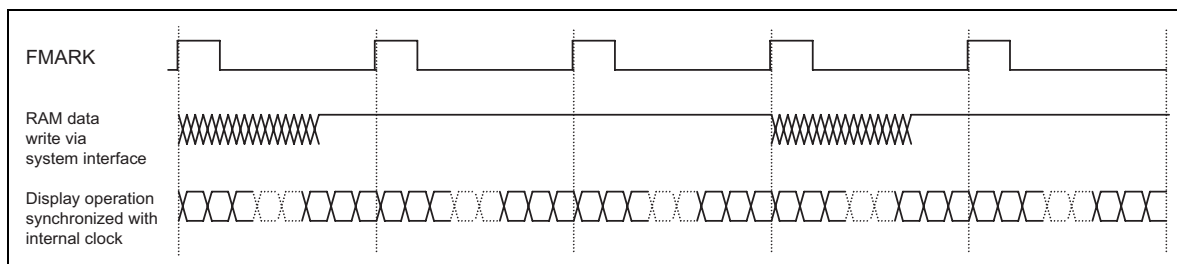


Figure 35 Moving Picture Data Transfers via FMARK function

When transferring data in synchronization with FMARK signal, minimum RAM data write speed must be taken into consideration. They must be more than the values calculated from the following equations.

$$RAMWriteSpeed(\text{min.})[Hz] > \frac{240 \times DisplayLines(NL)}{(FP + BP) + DisplayLines(NL) - margins) \times DivisionRatio(DIVE) \times ClockPer1H(RTNE) \times \frac{1}{fosc}}$$

Notes: When RAM write operation is not started immediately following the rising edge of FMARK, the time from the rising edge of FMARK until the start of RAM write operation must also be taken into account. RTN*: RTNI or RTNE. DIV*: DIVI or DIVE.

Examples of calculating minimum RAM data write speed is as follows. The above calculation shows RAM write speed per 1 pixel and is different from write speed defined by data transfer format of each interface.

[Example]

Panel size	240 RGB × 320 lines
Total number of lines (NL)	320 lines
Back/front porch	13/3 lines (BP = 8h'D, FP = 8'h3)
Frame marker position (FMP)	Display end line (320 th line)
Frame frequency	60 Hz
Maximum internal operation clock	600kHz × 1.07 = 642kHz
Clock division ratio (DIVE)	1
Number of clock per 1H period (RTNE)	30

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantee that display operation is completed within one FMARK cycle.

2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]

$$> 240 \times 320 / \{((13+3 + 320 - 2) \text{ lines} \times 1 \times 30 \text{ clocks}) \times 1/642 \text{ kHz}\} = 4.95 \text{ MHz / pixel}$$

- Notes: 1. In this example, it is assumed that the R61505V starts writing data in the internal RAM on the rising edge of FMARK.
2. There must be at least a margin of 2 lines between the line to which the R61505V has just written data and the line where display operation on the LCD is performed.
3. The FMARK signal output position is set to the line specified by register.

In this example, RAM write operation at a speed of 4.95MHz/pixel or faster, when starting on the rising edge of FMARK, guarantees the completion of data write operation in a certain line address before the R61505V starts the display operation of the data written in that line and can write moving picture data without causing flicker on the display.

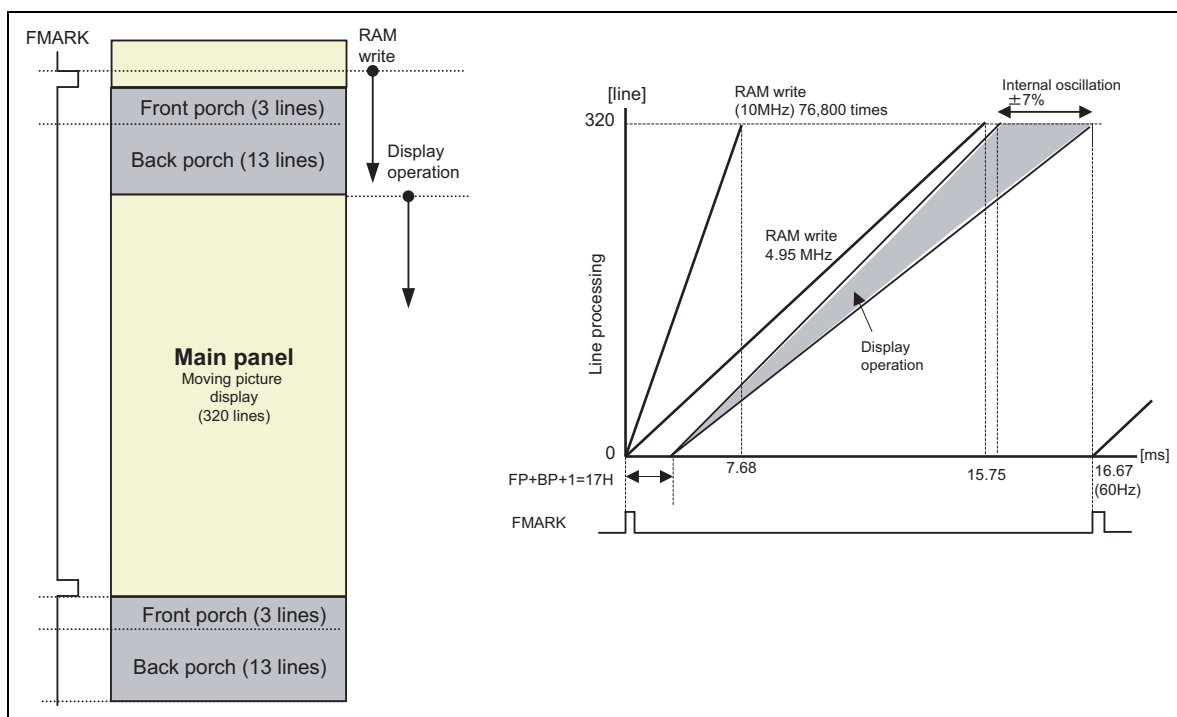


Figure 36

Note to display operation synchronous data transfer using FMARK signal

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margin in setting RAM write speed for this operation.

FMP bit setting

The host processor detects FMARK signal outputted at the position defined by FMP bit. The R61505V outputs an FMARK pulse when the R61505V is driving the line specified by FMP[8:0] bits. The FMARK signal can be used as a trigger signal to write display data in synchronization with display operation by detecting the address where data is read out for display operation.

The FMARK output interval is set by FMI[2:0] bits. Set FMI[2:0] bits in accordance with display data rewrite cycle and data transfer rate. This setting is enabled when FMARKOE = 1.

Table 70

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1 st line
9'h002	2 nd line
:	:
9'h14D	333 rd line
9'h14E	334 th line
9'h14F	335 th line
9'h150 ~ 1FF	Setting disabled

Table 71

FMI[2]	FMI[1]	FMI[0]	FMARK Output interval
0	0	0	1 frame period
0	0	1	2 frame periods
0	1	1	4 frame periods
1	0	1	6 frame periods
Other setting			Setting disabled

FMP setting example

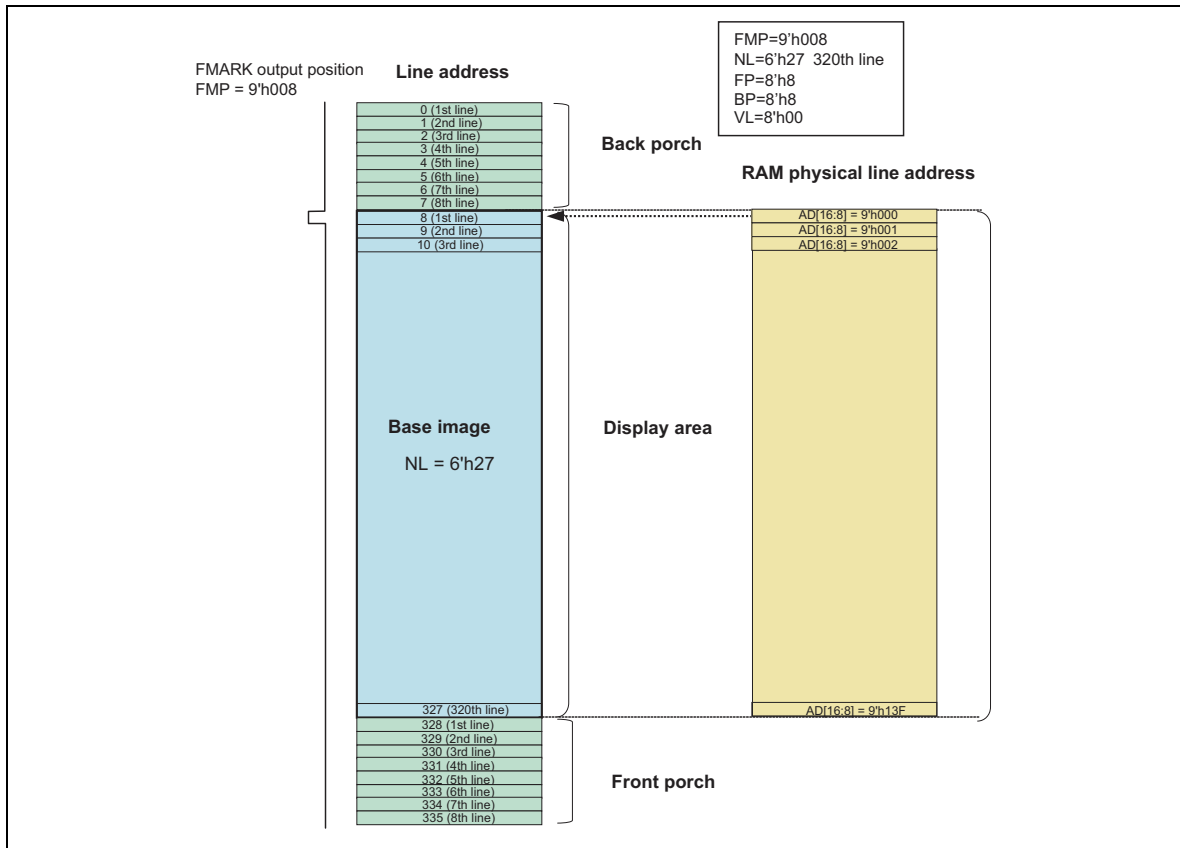


Figure 37

External Display Interface

The R61505V supports the RGB interface. The interface format is set by RM[1:0] bits. The internal RAM is accessible via RGB interface.

Table 72 RGB interface

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	Setting inhibited	-
1	1	Setting inhibited	-

Note: Using more than two interfaces at a time is prohibited.

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function. In RGB interface operation, front and back porch periods must be made before and after the display period.

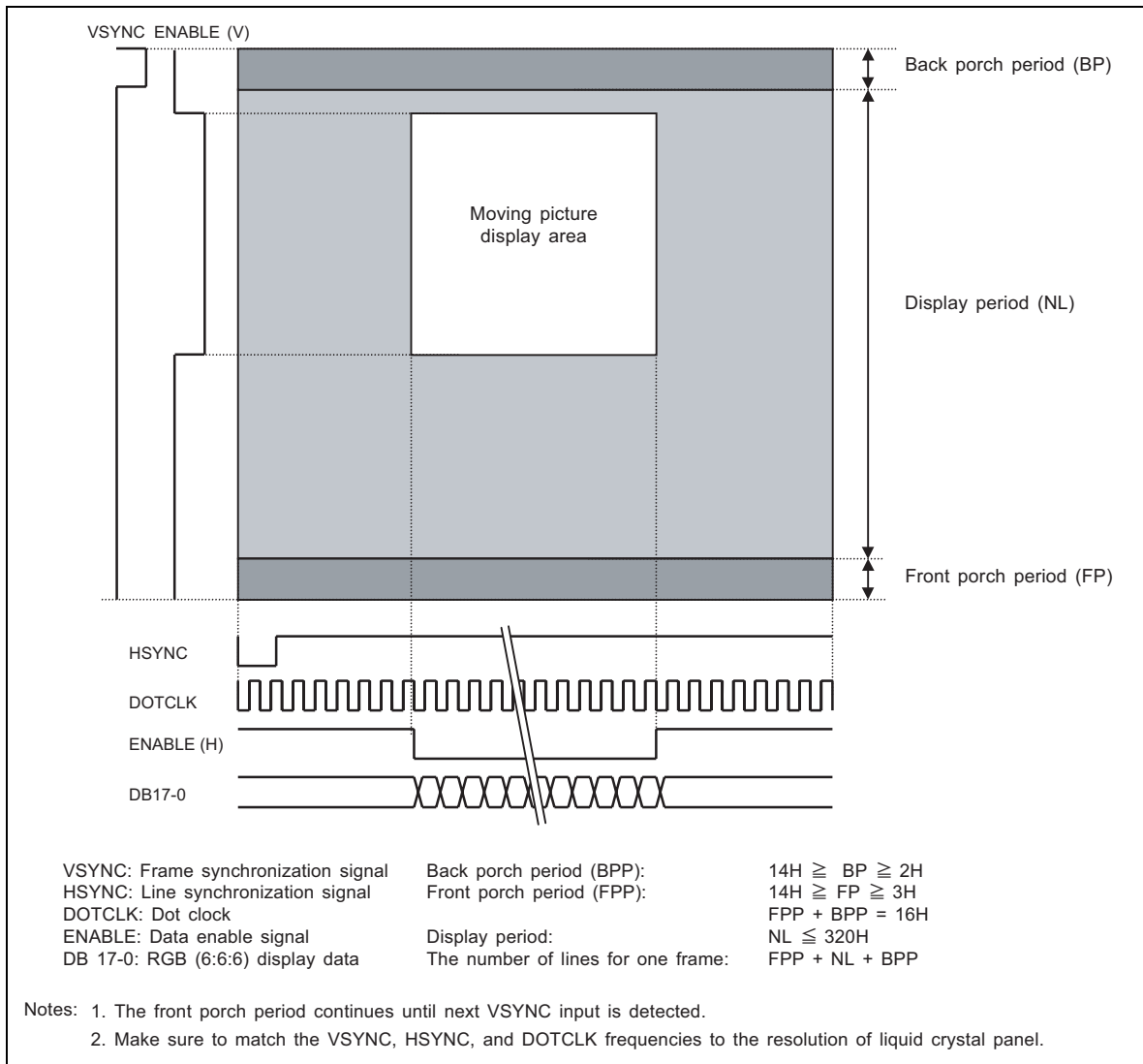


Figure 38 Display Operation via RGB Interface

Polarities of VSYNC, HSYNC, ENABLE, and DOTCLK Signals

The polarities of VSYNC, HSYNC, ENABLE, and DOTCLK signals can be changed by setting the DPL, EPL, HSPL, and VSPL bits respectively for convenience of system configuration.

RGB Interface Timing

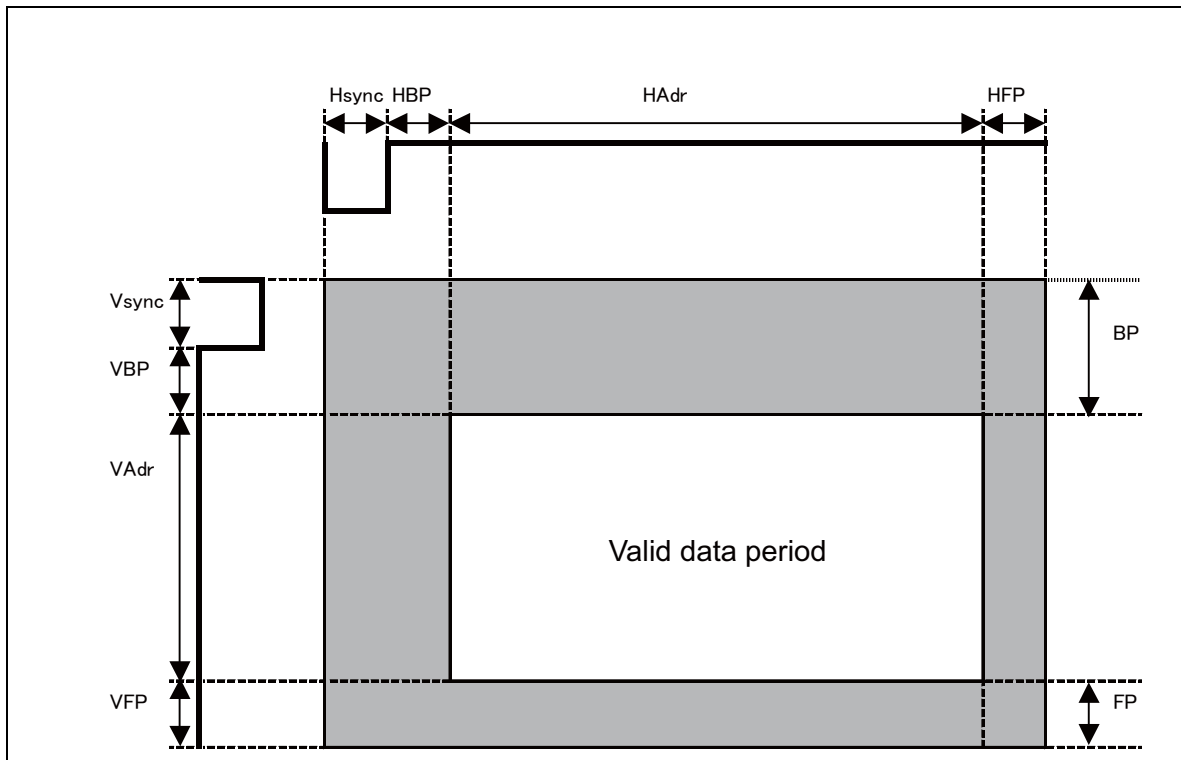


Figure 39

Table 73

Parameters	Symbols	Min.	Typ.	Max.	Step	Unit
Horizontal Synchronization	Hsync	2	10	16	1	DOTCLKCYC
Horizontal Back Porch	HBP	2	20	24	1	DOTCLKCYC
Horizontal Address	HAdr	—	240	—	1	DOTCLKCYC
Horizontal Front Porch	HFP	2	10	16	1	DOTCLKCYC
Vertical Synchronization	Vsync	1	2	4	1	Line
Vertical Back Porch	VBP	1	2	—	1	Line
Vertical Address	VAdr	—	320	—	1	Line
Vertical Front Porch	VFP	3	4	—	1	Line

Notes: 1. Typ. is the setting example under the following usage conditions (resolution of the panel = QVGA 240 x 320, clock frequency = 5.64 MHz, frame frequency = about 60 Hz).

2. In case of setting, make sure (Number of DOTCLK in 1H period) \geq RTNE[5:0] (number of clocks) \times DIVE[1:0] (Division ratio) \times (PCDIVL + PCDIVH). The setting example is shown in next page.

Setting Example of Display Control Clock in RGB Interface Operation

Register

The display operation is performed by the internal clock (DOTCLKD) generated by dividing the frequency of DOTCLK.

PCDIVH[2:0] defines number of DOTCLK during DOTCLKD is high in the units of 1clock.

PCDIVL[2:0] defines number of DOTCLK during DOTCLKD is low in the units of 1clock.

Also, write PCDIVH and PCDIVL values so that DOTCLKD frequency is the closest to internal oscillation clock frequency (600KHz). Make sure that $PCDIVL = PCDIVH$ or $PCDIVH - 1$. Make sure that (number of DOTCLKs in 1H) \geq RTNE (number of clocks) * DIVE (division ratio) * (PCDIVL + PCDIVH).

Setting example: in case of setting the frame frequency to 60Hz

Internal clock: Internal oscillation clock = 600kHz
 DIVE = 2'b0 (1/1)
 RTNE = 30 clocks
 FP = 8'h8, BP = 8'h8, NL = 6'h27 (320 lines)
 $\rightarrow 59.52\text{Hz}$

DOTCLK: Hsync = 10 clocks
 HBP = 20 clocks
 HFP = 10 clocks
 $60\text{Hz} \times (8+320+8) \text{ lines} \times (10+20+240+10) \text{ clocks} = 5.64\text{MHz}$
 DOTCLK frequency = 5.64MHz
 $5.64\text{MHz} / 600\text{kHz} = 9.4 \rightarrow$ Write PCDIVH and PCDIVL values so that DOTCLK frequency is divided into 8.
 $5.64 / 9 = 6.27\text{kHz}$
 $(6.27\text{kHz} / 1) / 30 \text{ clocks} / 336 \text{ lines} = 62.2\text{Hz}$

PCDIVH: 3'h4

PCDIVL: 3'h4

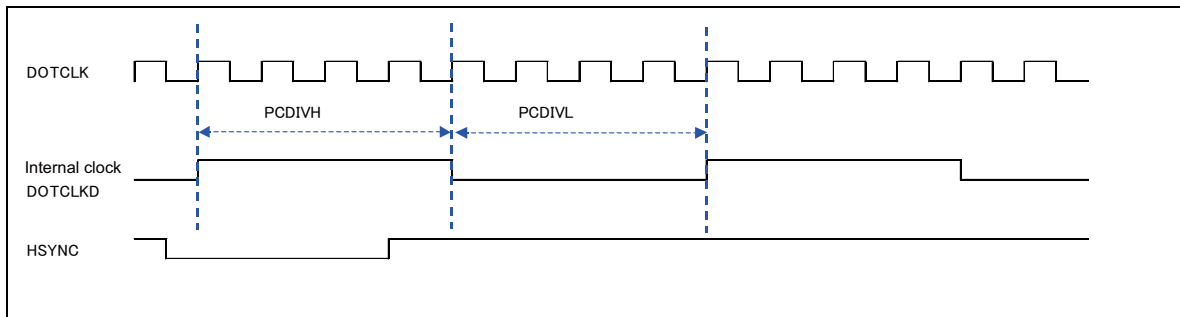


Figure 40

RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

16-/18-bit RGB Interface Timing

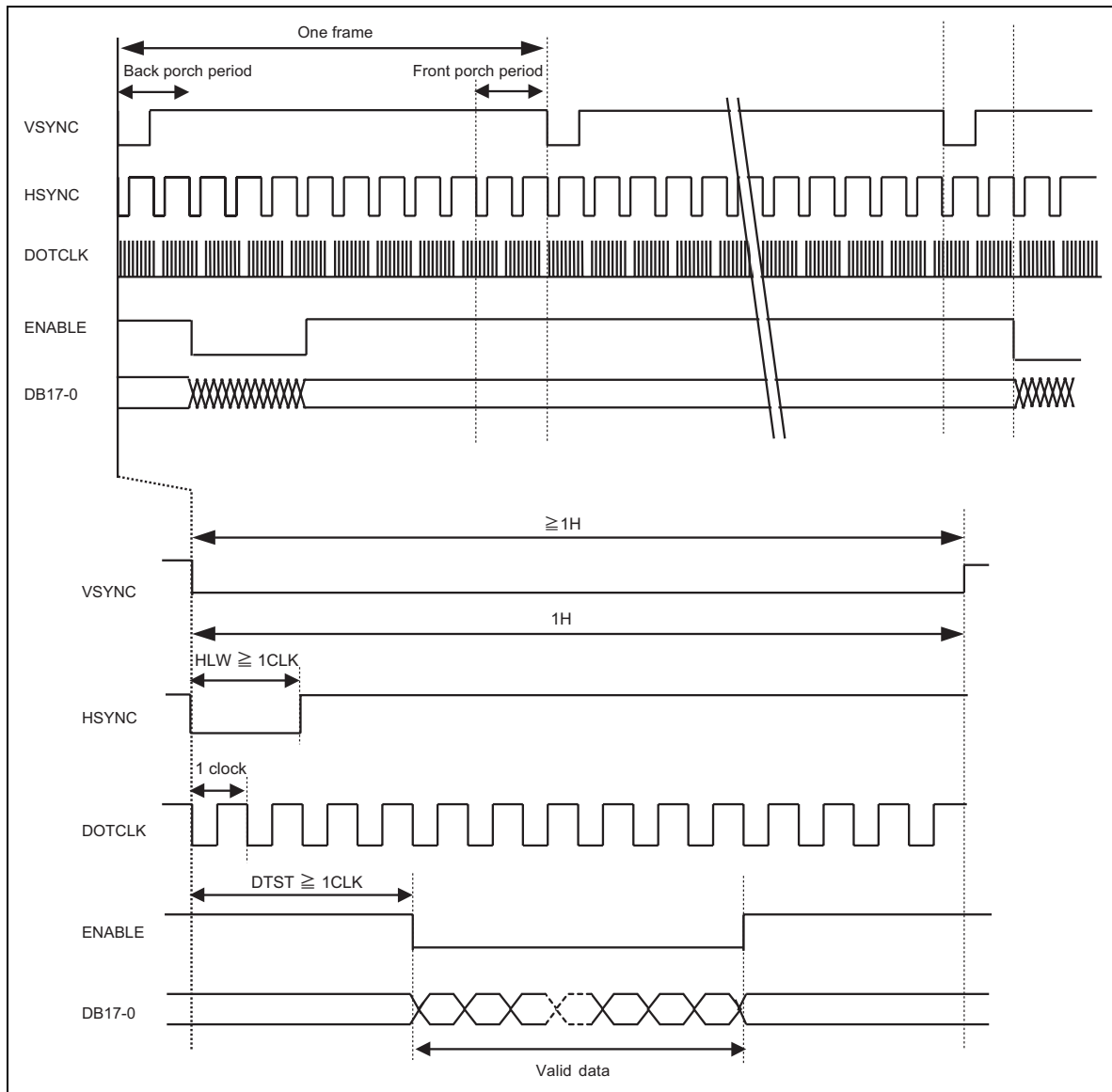


Figure 41

Note: VLW: VSYNC Low period
 HLW: HSYNC Low period
 DTST: Data transfer setup time

Moving Picture Display via RGB Interface

The R61505V supports RGB interface for moving picture display and incorporates RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. It becomes possible to transfer only the data written over the moving picture area
3. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
4. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

RAM access via system interface in RGB interface operation

The R61505V allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the RAM via system interface, set ENABLE “High” to stop writing data via RGB interface. Then set RM = “0” to enable RAM access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = “1” and the index register to R22h to start accessing RAM via RGB interface. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

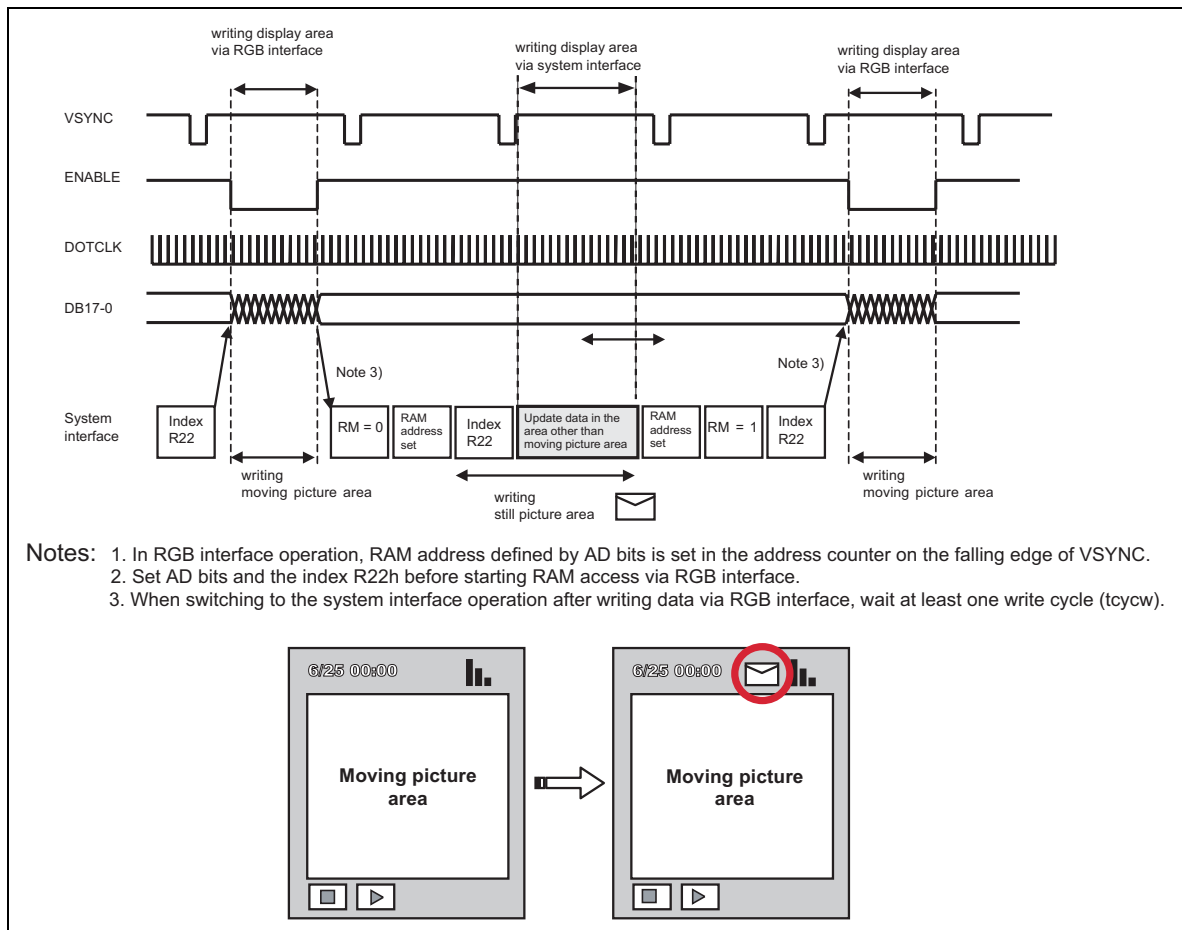


Figure 42 Updating the Still Picture Area while Displaying Moving Picture

16-bit RGB interface

The 16-bit RGB interface is selected by setting RIM1-0 = 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

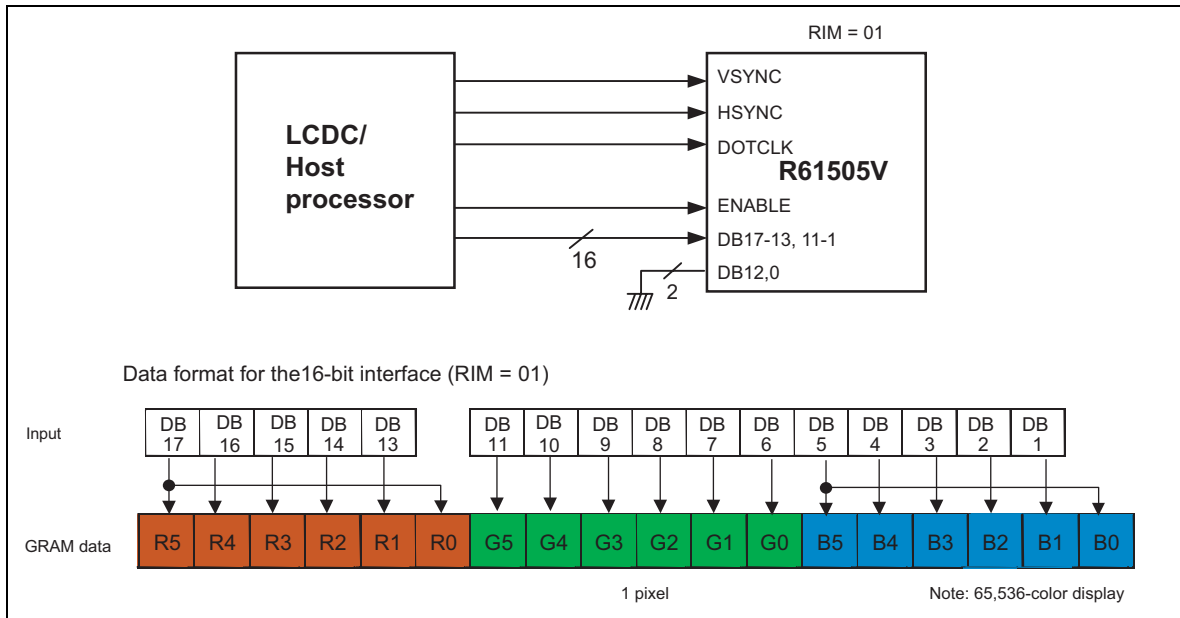


Figure 43 Example of 16-Bit RGB Interface and Data Format

18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM1-0 = 00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

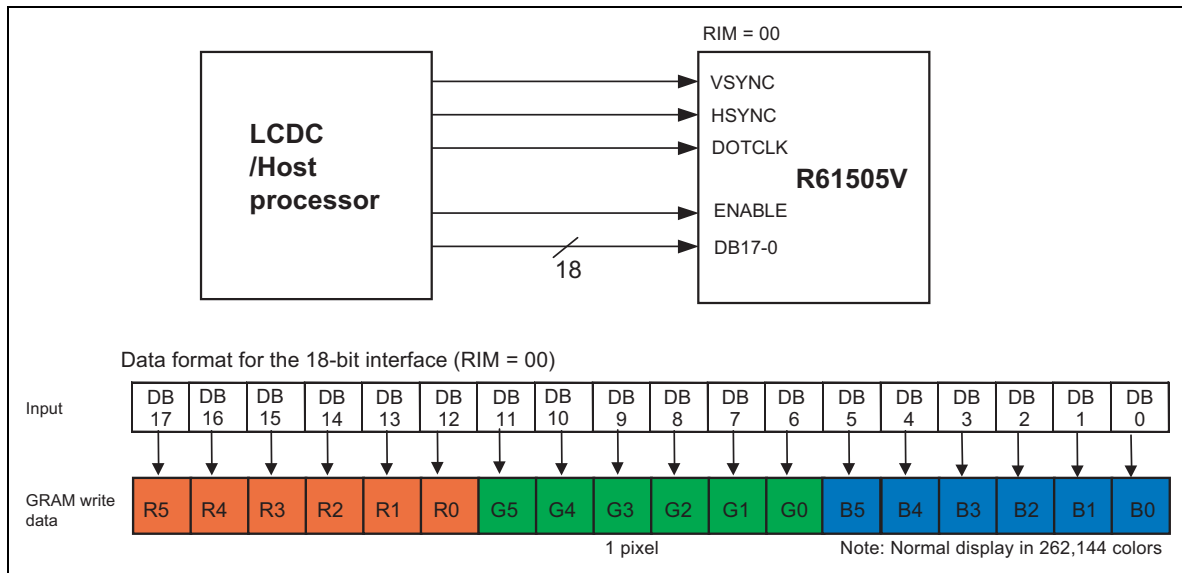


Figure 44 Example of 18-bit RGB Interface and Data Format

Notes to RGB interface operation

a. The following functions are not available in external display interface operation.

Table 74 Functions Not Available in External Display Interface operation

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

b. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.

c. The reference clock to generate liquid crystal panel controlling signals in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.

d. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

e. In RGB interface operation, front porch period continues after the end of frame period until next VSYNC input is detected.

f. In RGB interface operation, RAM address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

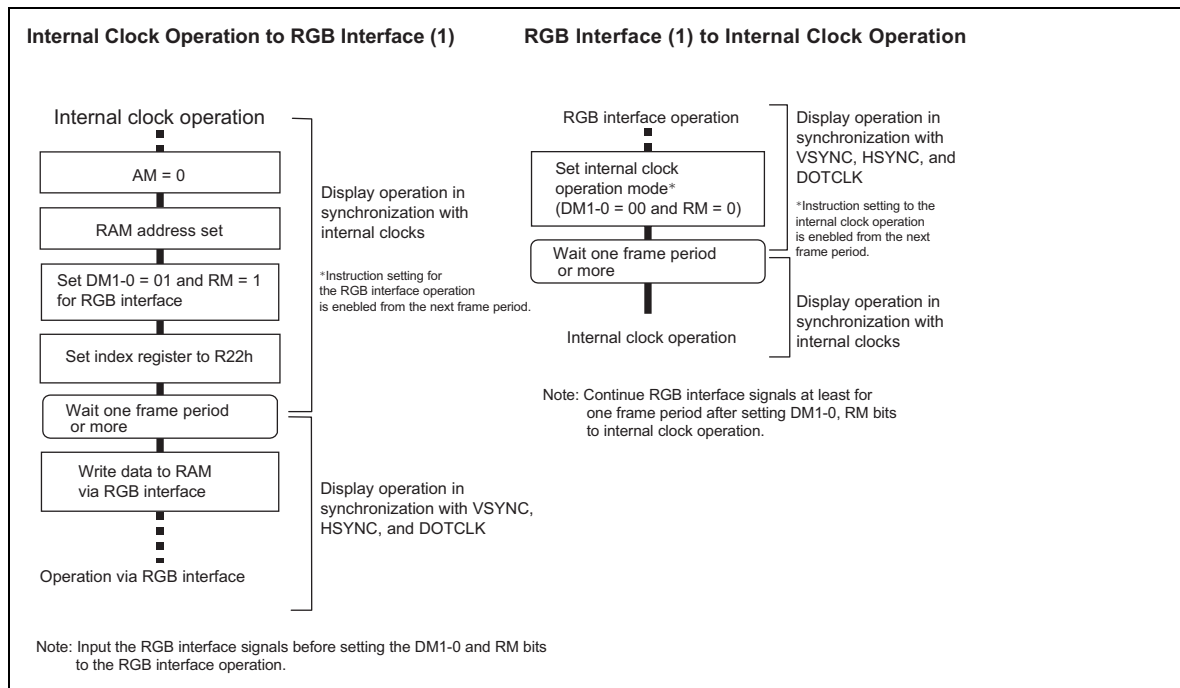


Figure 45 RGB and Internal Clock Operation Mode switching sequences

RAM Address and Display Position on the Panel

The R61505V has memory to store display data of 240RGB x 320 lines. The R61505V incorporates a circuit to control partial display, which allows switching driving method between full-screen display mode and partial display mode.

The R61505V makes display arrangement setting and panel driving position control setting separately and specifies RAM area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set PTSA and PTEA bits to specify the RAM area for a partial image
2. Set the display position of the partial image on the base image by setting PTDP.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE and PTDE) to display images

Normal display	BASEE = 1, PTDE=0
Partial display	BASEE = 0, PTDE = 1

5. Rewrite BASEE and PTDE bits when switching full display and partial display of the base image.

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing RAM data.

Table 75

	Display ENABLE	Numbers of lines	RAM area
Base image	BASEE	NL	(BSA, BEA) = (9'h000, 9'h13F)

Notes 1: The base image is displayed from the first line of the screen.

- 2: Make sure $NL \leq 320 \text{ (lines)} = BEA - BSA$ when setting a base image RAM area. BSA and BEA are fixed to 9'h000, 9'h13F, respectively.

Table 76

	Display ENABLE	Display position	RAM area
Partial image	PTDE	PTDP	(PTSA, PTEA)

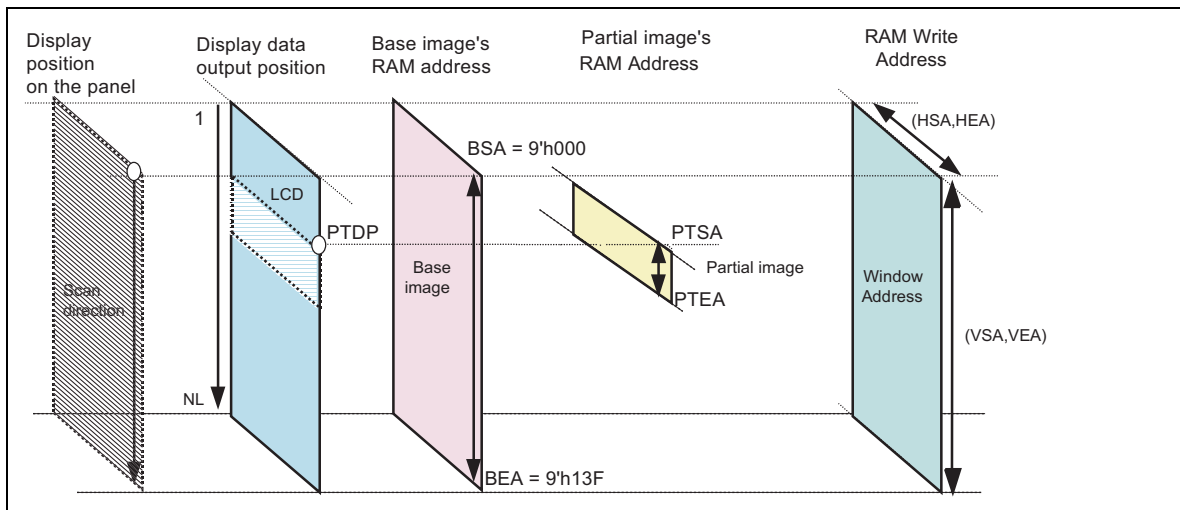


Figure 46 RAM Address, display position and drive position

Restrictions in setting display control instruction

There are restrictions in coordinates setting for display data, display position and partial display.

(1) Screen setting

In setting the number of lines to drive the liquid crystal panel, make sure that the total number of lines is 320 lines or less ($NL \leq 320$ lines).

(2) Base image display

1. The base image is displayed from the first line of the screen: $BSA = 1^{st}$ line (of the display panel)
2. The base image RAM area (specified by $BSA = 000$, $BEA = 13F$) must include the same or more number of lines set by NL bits (liquid crystal panel drive lines): $BEA - BSA = 320 \text{ lines} \geq NL$

The following figure shows the relationship among the RAM address, display position, and the lines driven for the display.

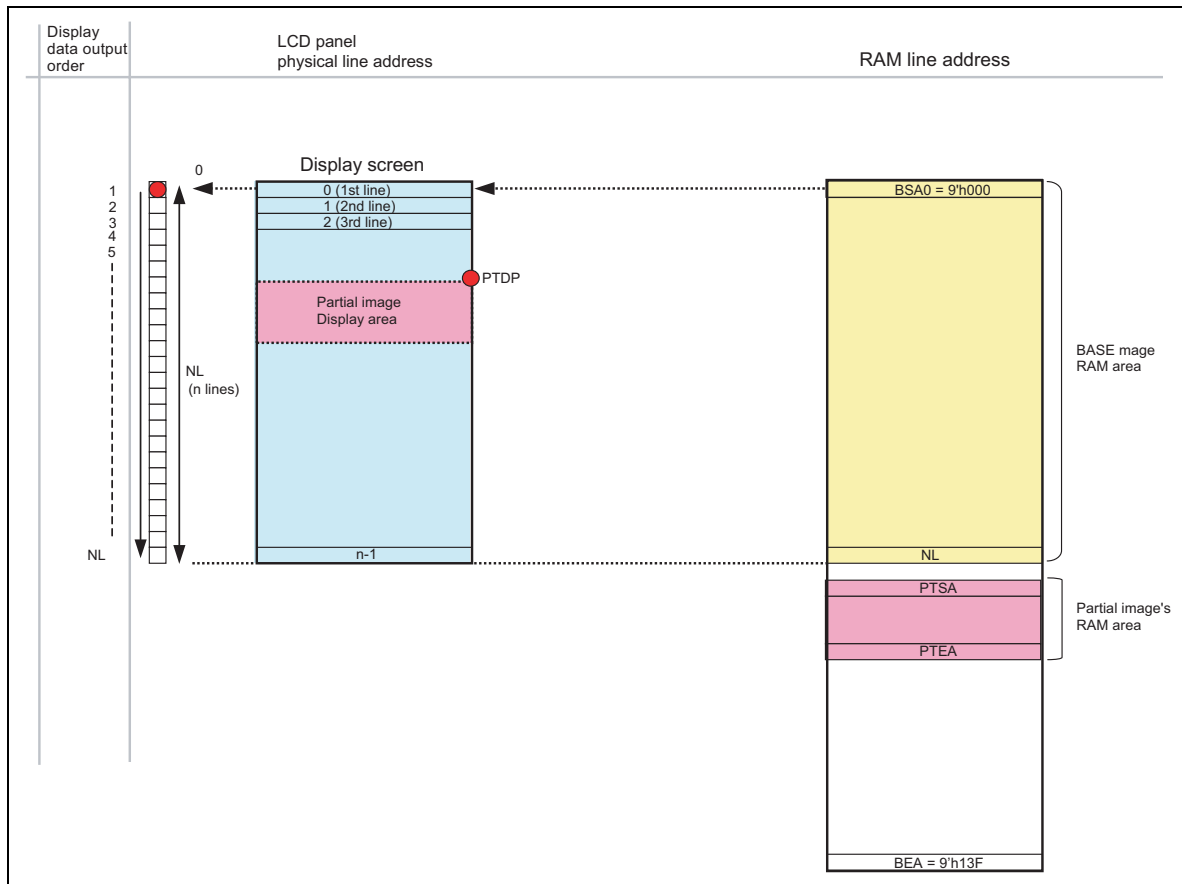


Figure 47 Display RAM address and panel display position

Note: This figure shows the relationship between RAM line address and the display position on the panel. In the R61505V's internal operation, the data is written in the RAM area specified by the window address setting registers.

Instruction setting example

The followings are examples of settings for 240 (RGB) x 320 (lines) panel.

1. Full screen display with no partial image

The following is an example of settings for full screen display.

Table 77

Base image display instruction	
BASEE	1
NL[5:0]	6'h27
PTDE	0

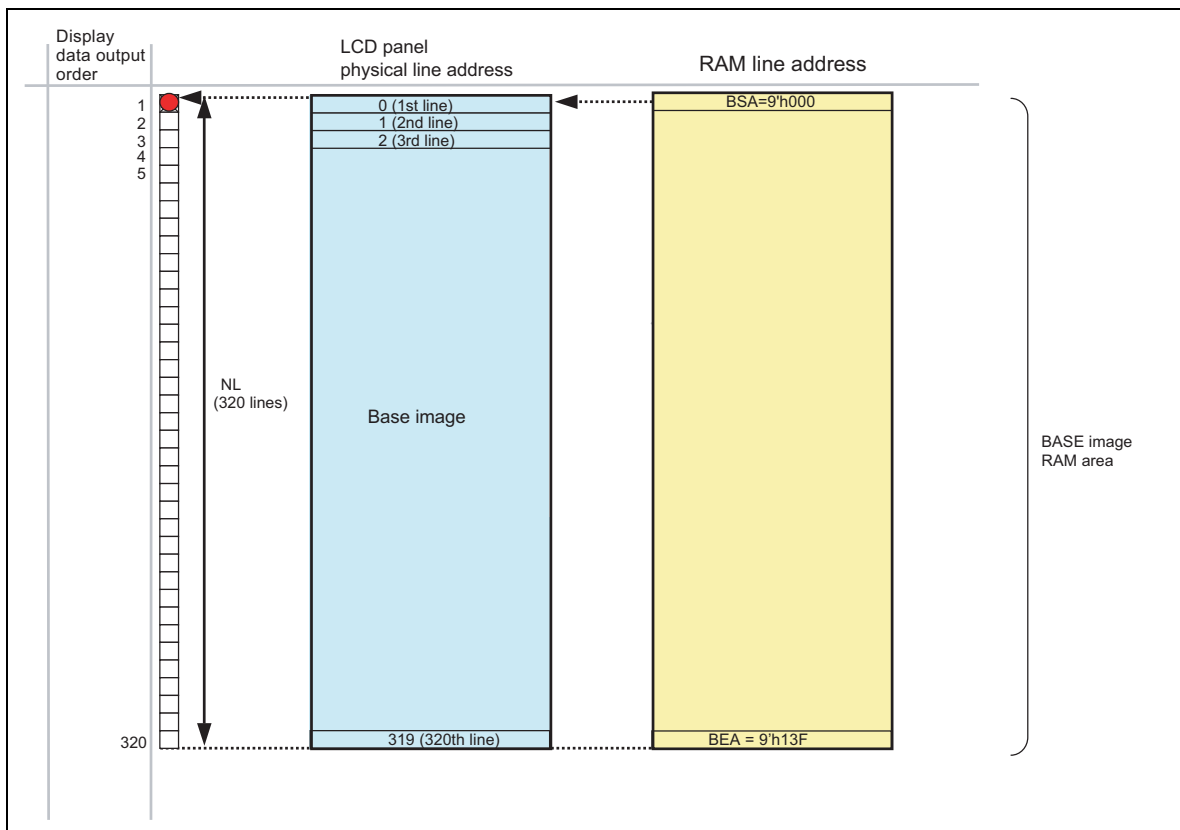


Figure 48 Full screen display with no partial image

2. Partial Display

The following is an example of settings for displaying only partial image and turning off the base image.
The partial image is displayed at the designated position.

Table 78

Base image display instruction	
BASEE	0
NL[5:0]	6'h27

Partial image display instruction	
PTDE	1
PTSA [8:0]	9'h000
PTEA [8:0]	9'h00F
PTDP [8:0]	9'h080

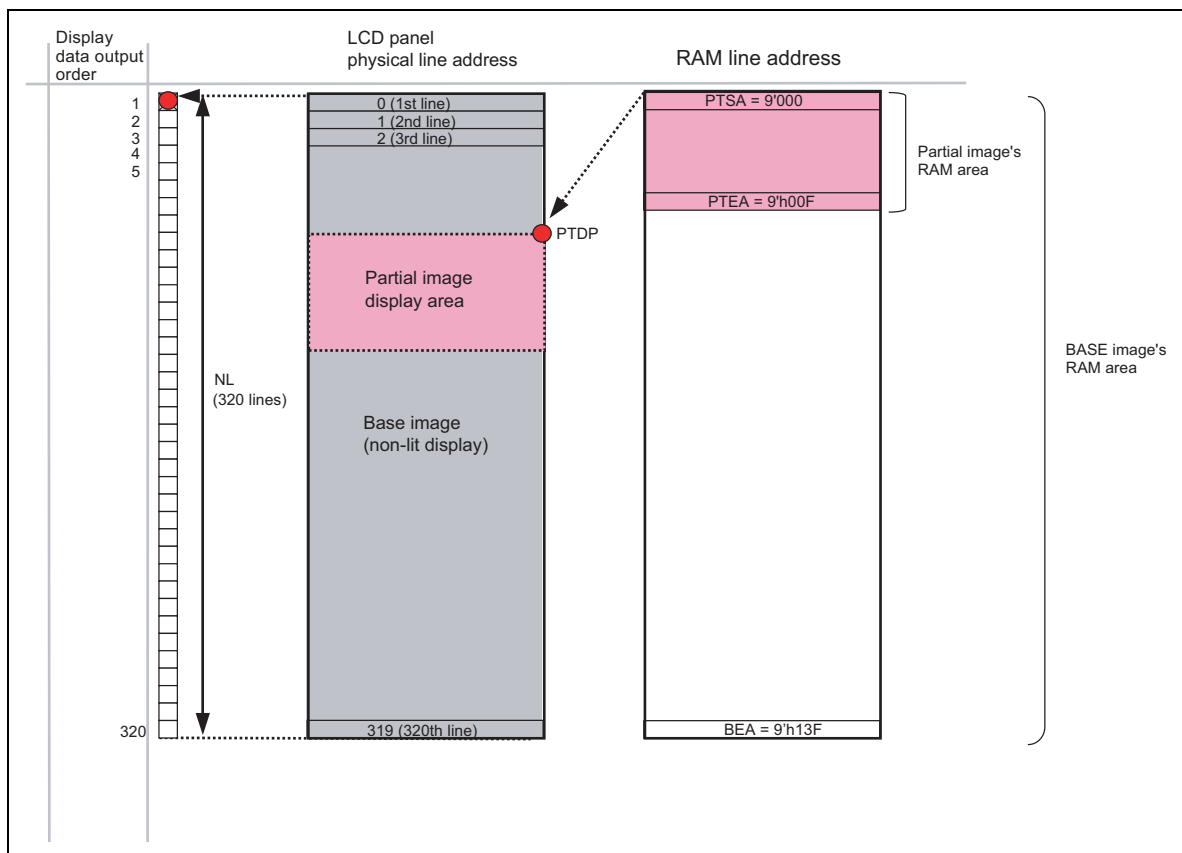


Figure 49 Partial Display

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the R61505V to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area setting range]

(Horizontal direction) $8'h00 \leq HSA < HEA \leq 8'hEF$
 (Vertical direction) $9'h000 \leq VSA < VEA \leq 9'h13F$

[RAM Address setting range]

(RAM address) $HSA \leq AD[7:0] \leq HEA$
 $VSA \leq AD[16:8] \leq VEA$

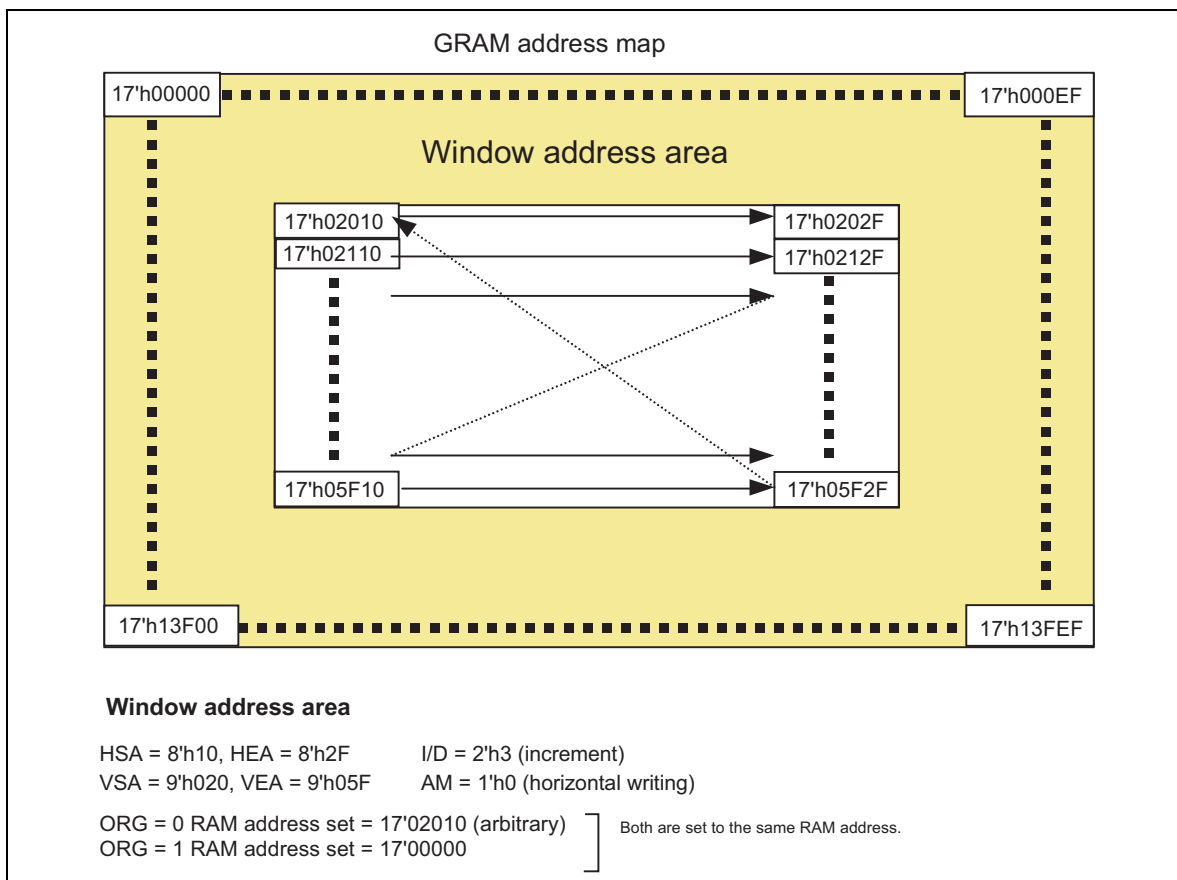


Figure 50 Automatic address update within a Window Address Area

Scan Mode Setting

The R61505V can set the gate pin assignment and the scan direction in the following 4 different ways by setting SM and GS bits to realize various connections between the R61505V and the LCD panel.

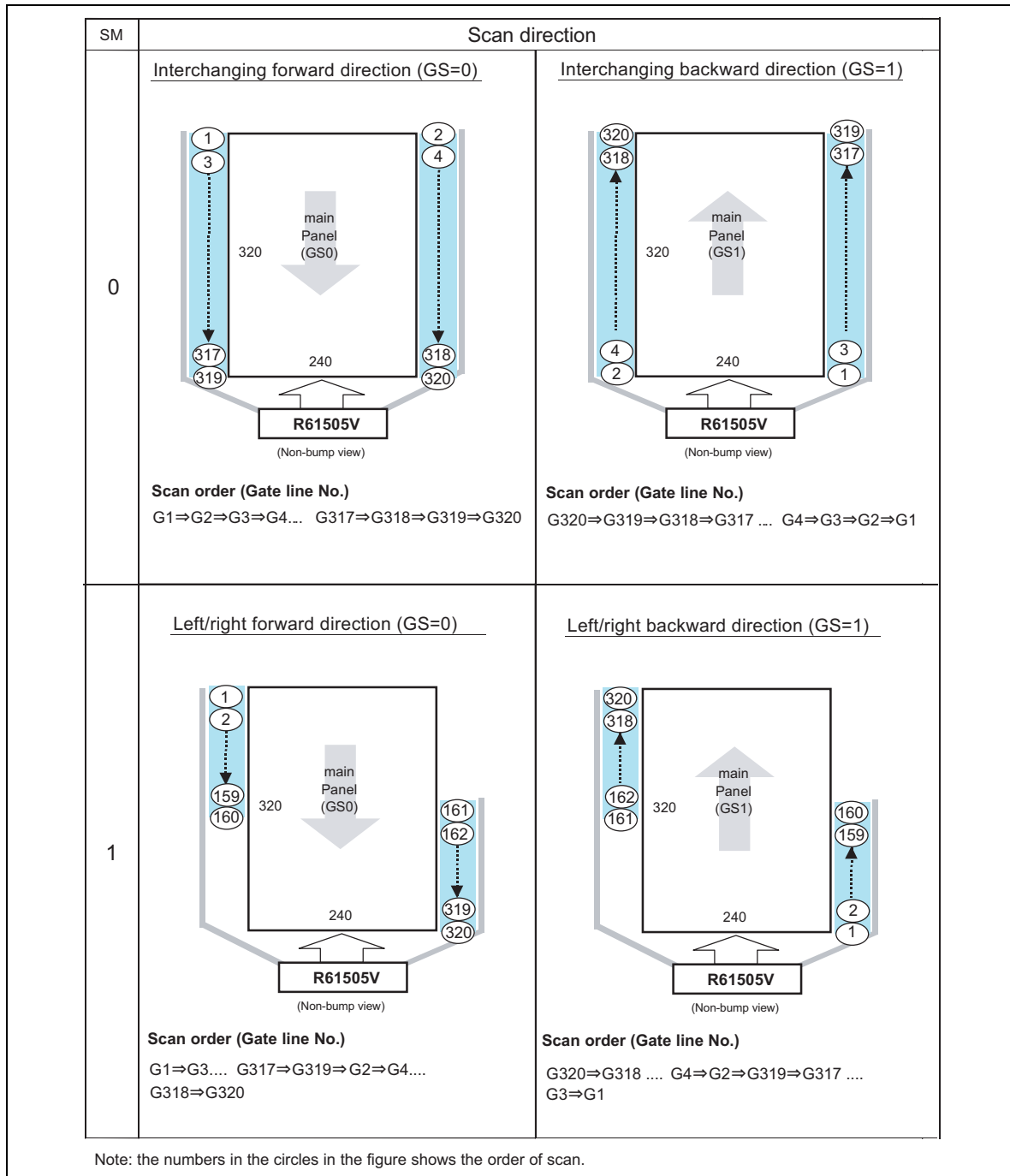


Figure 51

8-color Display Mode

The R61505V has a function to display in eight colors. In this display mode, only V0 and V63 are used and power supplies to other grayscales (V1 to V62) are turned off to reduce power consumption.

In 8-color display mode, the γ -adjustment registers R30h-R39h are disabled and the power supplies to V1 to V62 halt. The R61505V does not require rewriting GRAM data for 8-color display. Only MSBs of red, green and blue data is used to display image on the panel.

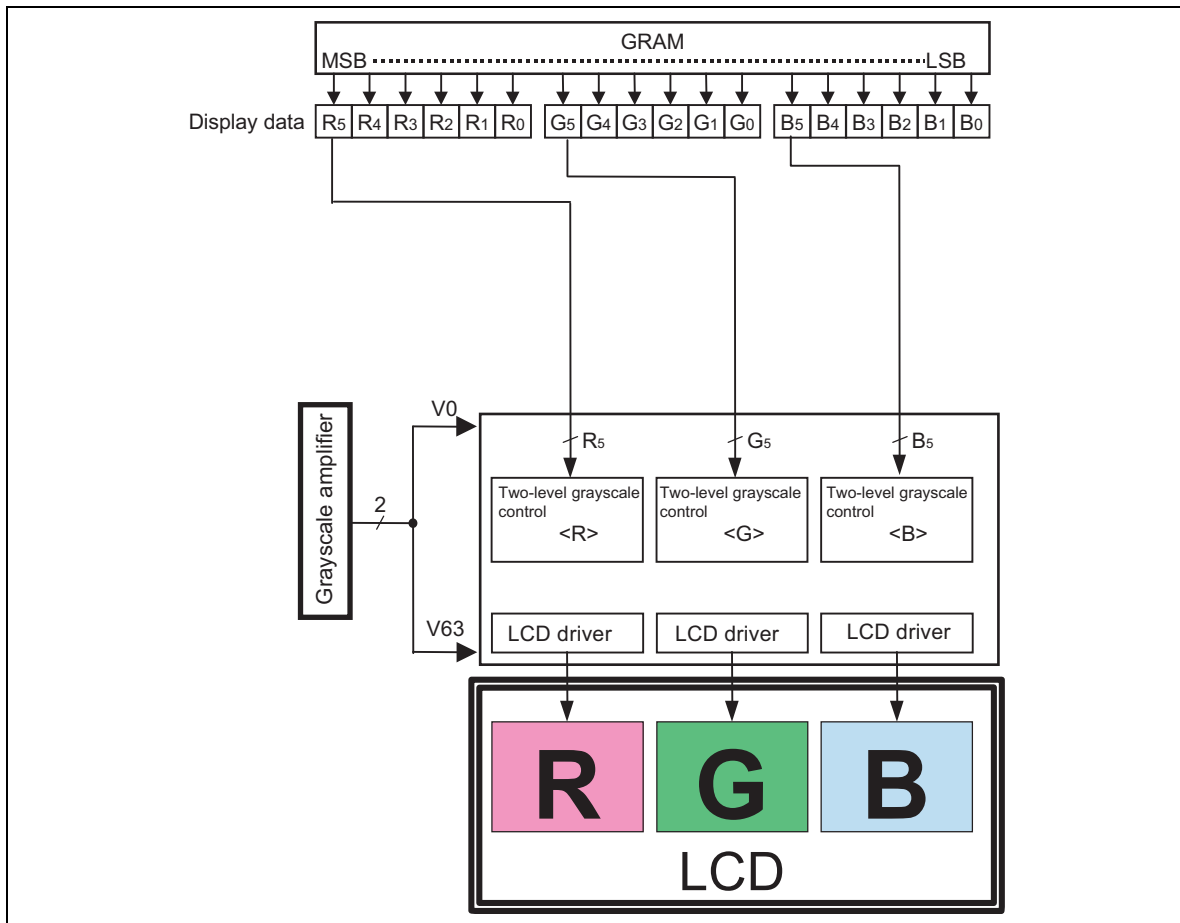


Figure 52 8-color Display Mode

Line Inversion AC Drive

The R61505V supports n-line inversion alternating current drive in addition to frame-inversion liquid crystal alternating current drive. The timing to invert the electric current can be set to either every line or every two lines. Set line number of inversion timing checking display quality on liquid crystal display. Note that less number of line leads to higher inversion frequency of liquid crystal and more charge/discharge battery in liquid crystal display.

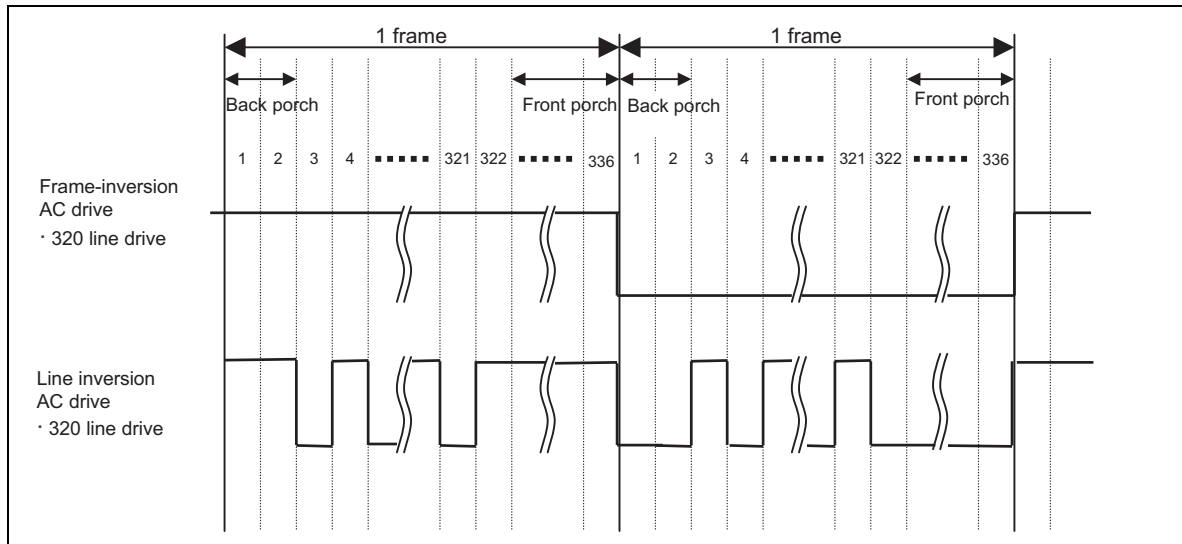


Figure 53 Example of Alternating Signals for n-line Inversion

Note: Polarity of signals does not invert during blank periods, namely back and front porch periods. N-line inversion operation starts from the first line of a display area.

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the R61505V draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of line inversion AC drive, selected by setting BC0=1 (R02h), polarity is inverted as the R61505V draws one line, and a blank period lasting for (BP+FP) periods is inserted when the R61505V draws one frame.

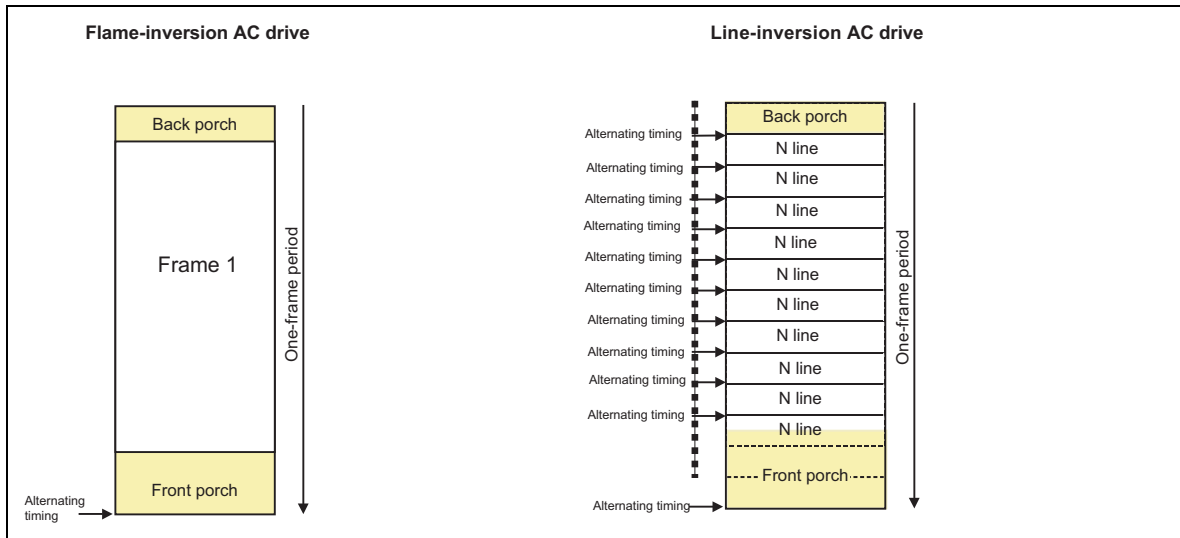


Figure 54 Alternating Timing

Note: Frame inversion AC drive is available only in 8-color display mode. Check the quality of display on the panel.

Frame-Frequency Adjustment Function

The R61505V supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIV, RTN bits without changing the oscillation frequency.

The R61505V allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIVI and RTNI settings, the R61505V can operate at high frame frequency when displaying a moving picture, which requires the R61505V to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between liquid crystal drive duty and frame frequency

The following equation represent the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTNI) and the operation clock frequency division ratio setting bit (DIVI).

Equation for calculating frame frequency

$$FrameFrequency(f_{FLM}) = \frac{f_{osc}}{NumberofClocks / line \times DivisionRatio \times (Line + FP + BP)} [Hz]$$

f_{osc} : clock frequency for internal operation (600kHz)

Number of clocks per line: RTNI bit

Division ratio: DIVI bit

Line: number of lines to drive the LCD panel (NL bit)

Number of lines for front porch : FP

Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

f_{osc} : 600kHz

Number of lines: 320 lines

1H period: 30 clock cycles (RTNI[4:0] = "1E")

Division ratio of operating clock: 1

Front porch: 8 lines

Back porch: 8 lines

$$f_{FLM} = 600kHz / (30 \text{ clocks} \times 1/1 \times (320 + 8 + 8) \text{ (lines)}) \div 60Hz$$

Partial Display Function

The partial display function allows the R61505V to drive lines selectively to display partial image by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

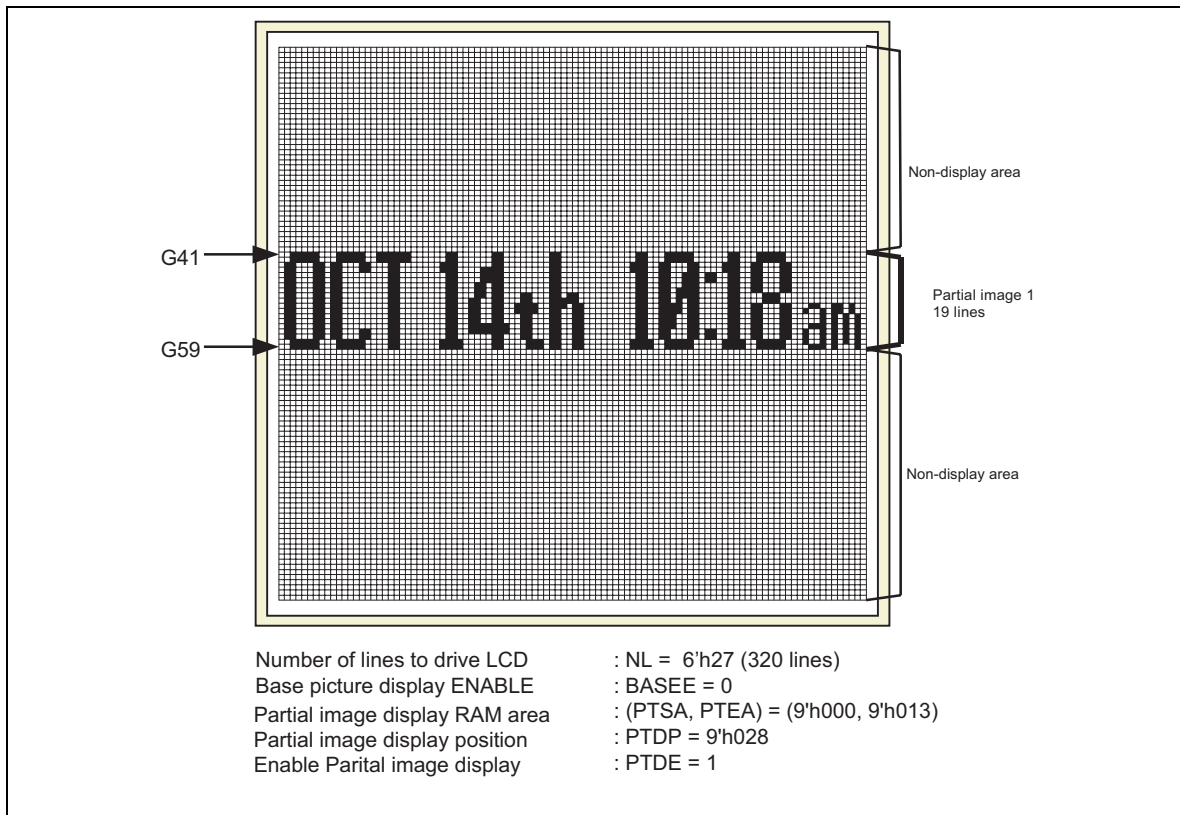


Figure 55 Partial display example

Note: See the “RAM Address and Display Position on the Panel” for details on the relationship between the display positions of partial images and respective RAM area setting.

Liquid Crystal Panel Interface Timing

The relationships between RGB interface signals and liquid crystal panel control signals in internal operation and RGB interface operations are as follows

Internal clock operation

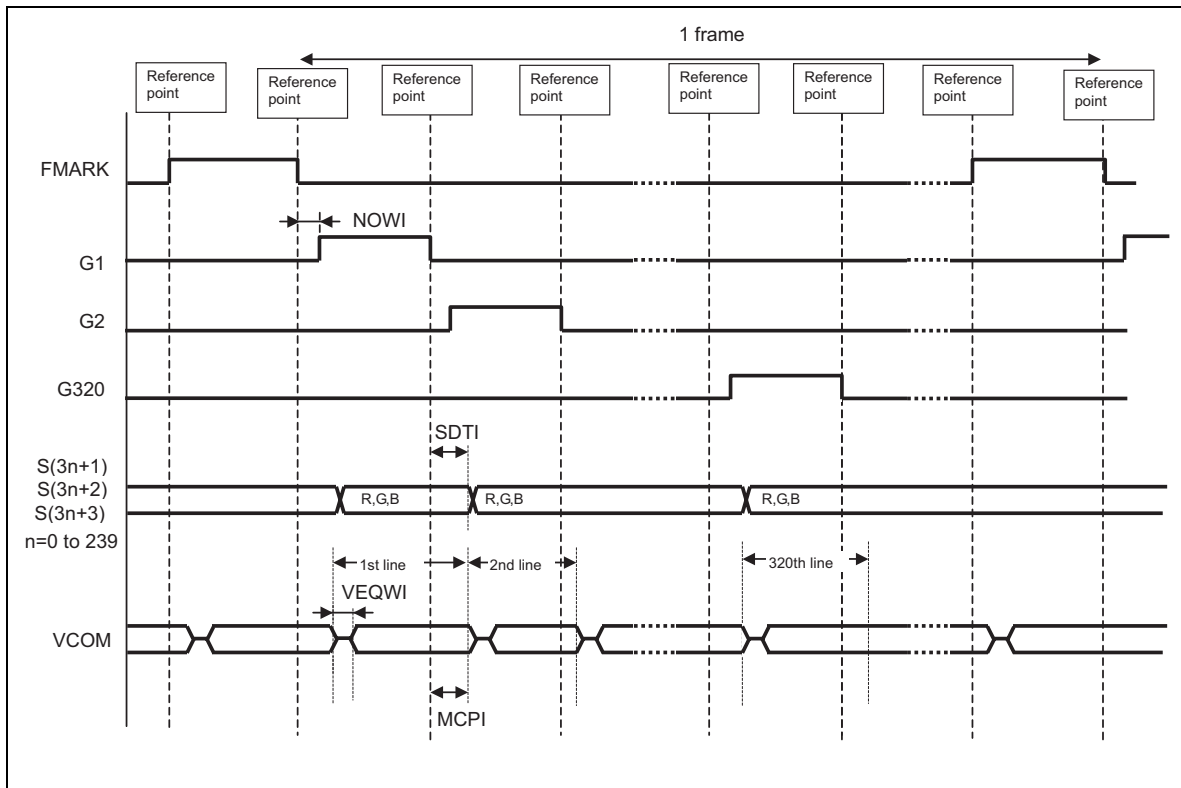


Figure 56

VCOM alternating position and source output alternating position can be set separately.

RGB interface operation

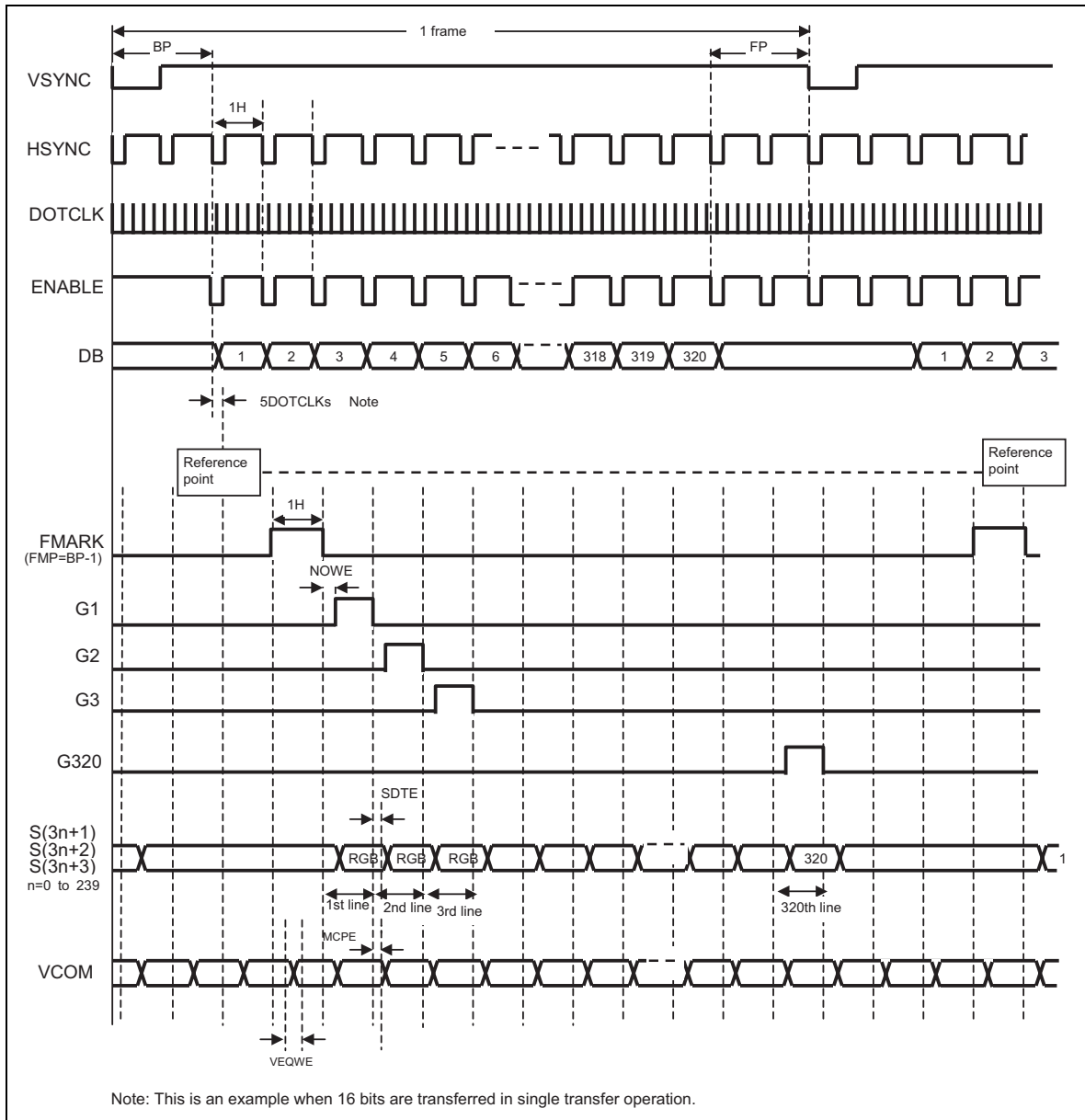


Figure 57

γ Correction Function

γ Correction Function

The R61505V supports γ -correction function to make the optimal colors according to the characteristics of the panel. The R61505V has registers for positive and negative polarities to allow different settings.

γ Correction Circuit

The following figure shows the γ -correction circuit. According to the settings of variable resistors R0 to R8, the voltage the level of which is the difference is between VREG1OUT and VGS is evenly divided into 8 grayscale reference voltages (V0, V1, V8, V20, V43, V55, V62 and V63). Other 42-grayscale voltages are generated by setting the level at a certain interval between the reference voltages. For grayscale voltage, see “Grayscale Voltage Calculation Formula”.

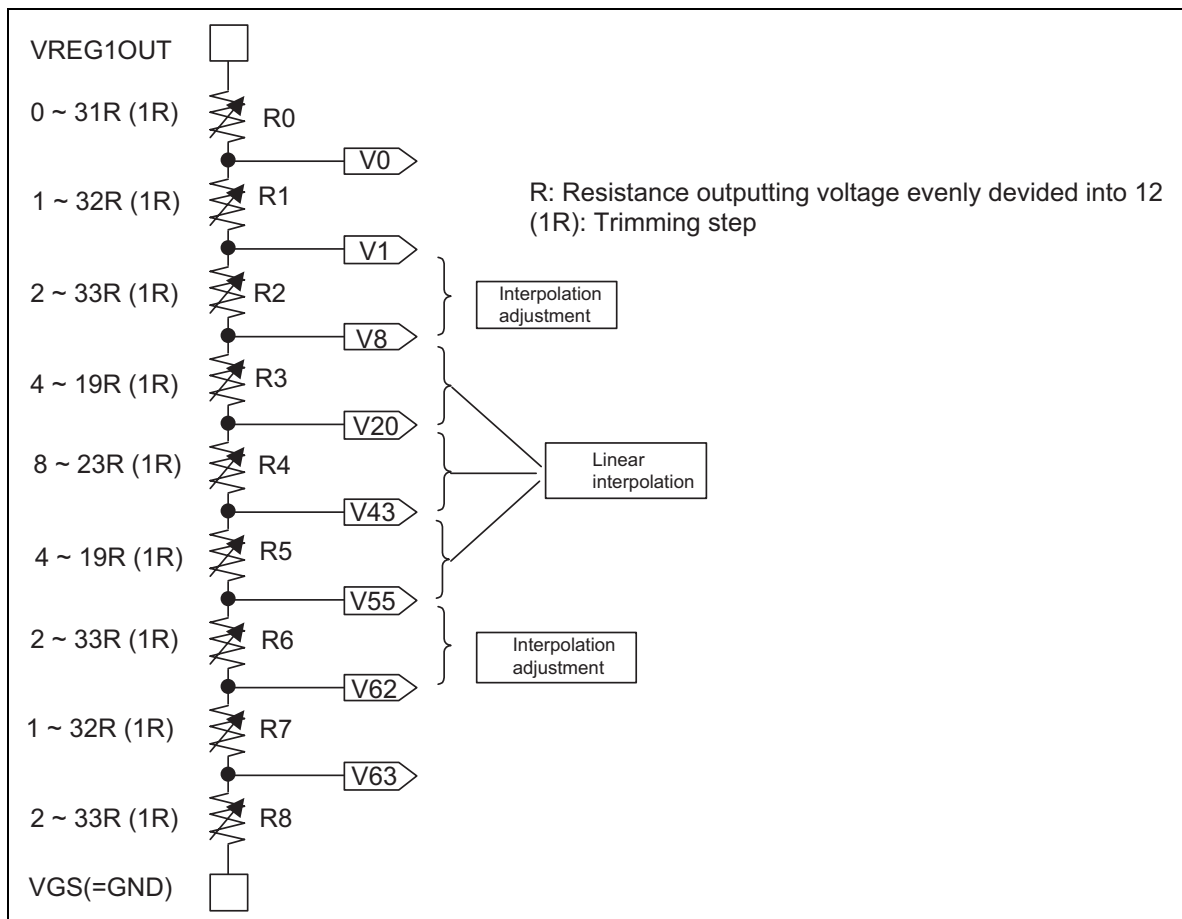


Figure 58

γ Correction Registers

The γ -correction registers include 42-bit reference level adjustment registers for each of positive polarity and negative polarity and 8-bit interpolation adjustment registers.

Reference level adjustment registers**Table 79 Reference level adjustment registers**

Resistor	Gamma	
	Positive polarity	Negative polarity
R0	PR0P00[4:0]	PR0N00[4:0]
R1	PR0P01[4:0]	PR0N01[4:0]
R2	PR0P02[4:0]	PR0N02[4:0]
R3	PR0P03[3:0]	PR0N03[3:0]
R4	PR0P04[3:0]	PR0N04[3:0]
R5	PR0P05[3:0]	PR0N05[3:0]
R6	PR0P06[4:0]	PR0N06[4:0]
R7	PR0P07[4:0]	PR0N07[4:0]
R8	PR0P08[4:0]	PR0N08[4:0]

Table 80 Reference level adjustment registers and resistors

Resistor	Register		Resistance	Resistor	Register		Resistance
	Name	Value			Name	Value	
R0	PR**0[4:0]	5'h00	0R	R5	PR**5[3:0]	4'h0	4R
		5'h01	1R			4'h1	5R
		5'h02	2R			4'h2	6R
		⋮	⋮			⋮	⋮
		5'h1F	31R			4'hF	19R
R1	PR**1[4:0]	5'h00	1R	R6	PR**6[4:0]	5'h00	2R
		5'h01	2R			5'h01	3R
		5'h02	3R			5'h02	4R
		⋮	⋮			⋮	⋮
		5'h1F	32R			5'h1F	33R
R2	PR**2[4:0]	5'h00	2R	R7	PR**7[4:0]	5'h00	1R
		5'h01	3R			5'h01	2R
		5'h02	4R			5'h02	3R
		⋮	⋮			⋮	⋮
		5'h1F	33R			5'h1F	32R
R3	PR**3[3:0]	4'h0	4R	R8	PR**8[4:0]	5'h00	2R
		4'h1	5R			5'h01	3R
		4'h2	6R			5'h02	4R
		⋮	⋮			⋮	⋮
		4'hF	19R			5'h1F	33R
R4	PR**4[3:0]	4'h0	8R				
		4'h1	9R				
		4'h2	10R				
		⋮	⋮				
		4'hF	23R				

Note: ** in the above table represents 0P/0N/1P/1N/2P/2N.

Interpolation Registers

Table 81 Interpolation Registers

Interpolation adjustment	Gamma	
	Positive polarity	Negative polarity
V2 ~ V7	PI0P0[1:0]	PI0N0[1:0]
	PI0P1[1:0]	PI0N1[1:0]
V56 ~ V61	PI0P2[1:0]	PI0N2[1:0]
	PI0P3[1:0]	PI0N3[1:0]

Table 82 Interpolation factor for V2 to V7

(See “Grayscale Voltage Calculation Formula” for IPV* level)

PI**0[1:0]	PI**1[1:0]	IPV2	IPV3	IPV4	IPV5	IPV6	IPV7
2'h0	2'h0	81%	67%	52%	39%	26%	13%
	2'h1	78%	61%	43%	33%	22%	11%
	2'h2	73%	52%	31%	23%	15%	8%
	2'h3	72%	50%	28%	21%	14%	7%
2'h1	2'h0	80%	68%	56%	42%	28%	14%
	2'h1	76%	62%	48%	36%	24%	12%
	2'h2	70%	52%	35%	26%	17%	9%
	2'h3	69%	50%	31%	23%	16%	8%
2'h2	2'h0	78%	70%	61%	46%	30%	15%
	2'h1	74%	63%	53%	39%	26%	13%
	2'h2	66%	53%	39%	29%	20%	10%
	2'h3	64%	50%	36%	27%	18%	9%
2'h3	2'h0	78%	70%	63%	47%	31%	16%
	2'h1	73%	64%	54%	41%	27%	14%
	2'h2	65%	53%	41%	31%	20%	10%
	2'h3	63%	50%	37%	28%	19%	9%

Table 83 Interpolation factor for V56 to V61

PI**3[1:0]	PI**2[1:0]	IPV56	IPV57	IPV58	IPV59	IPV60	IPV61
2'h0	2'h0	87%	74%	61%	48%	33%	19%
	2'h1	89%	78%	67%	57%	39%	22%
	2'h2	92%	85%	77%	69%	48%	27%
	2'h3	93%	86%	79%	72%	50%	28%
2'h1	2'h0	86%	72%	58%	44%	32%	20%
	2'h1	88%	76%	64%	52%	38%	24%
	2'h2	91%	83%	74%	65%	48%	30%
	2'h3	92%	84%	77%	69%	50%	31%
2'h2	2'h0	85%	70%	54%	39%	30%	22%
	2'h1	87%	74%	61%	47%	37%	26%
	2'h2	90%	80%	71%	61%	47%	34%
	2'h3	91%	82%	73%	64%	50%	36%
2'h3	2'h0	84%	69%	53%	38%	30%	22%
	2'h1	86%	73%	59%	46%	36%	27%
	2'h2	90%	80%	69%	59%	47%	35%
	2'h3	91%	81%	72%	63%	50%	37%

Note: ** in the above tables represents 0P/0N/1P/1N/2P/2N.

Table 84 Grayscale Voltage Calculation Formula

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	$\Delta V \times \Sigma (R1 \sim R8) / \text{SUMR}$	V32	$V43 + (V20 - V43) \times 11/23$
V1	$\Delta V \times \Sigma (R2 \sim R8) / \text{SUMR}$	V33	$V43 + (V20 - V43) \times 10/23$
V2	$V8 + (V1 - V8) \times \text{IPV2}$	V34	$V43 + (V20 - V43) \times 9/23$
V3	$V8 + (V1 - V8) \times \text{IPV3}$	V35	$V43 + (V20 - V43) \times 8/23$
V4	$V8 + (V1 - V8) \times \text{IPV4}$	V36	$V43 + (V20 - V43) \times 7/23$
V5	$V8 + (V1 - V8) \times \text{IPV5}$	V37	$V43 + (V20 - V43) \times 6/23$
V6	$V8 + (V1 - V8) \times \text{IPV6}$	V38	$V43 + (V20 - V43) \times 5/23$
V7	$V8 + (V1 - V8) \times \text{IPV7}$	V39	$V43 + (V20 - V43) \times 4/23$
V8	$\Delta V \times \Sigma (R3 \sim R8) / \text{SUMR}$	V40	$V43 + (V20 - V43) \times 3/23$
V9	$V20 + (V8 - V20) \times 11/12$	V41	$V43 + (V20 - V43) \times 2/23$
V10	$V20 + (V8 - V20) \times 10/12$	V42	$V43 + (V20 - V43) \times 1/23$
V11	$V20 + (V8 - V20) \times 9/12$	V43	$\Delta V \times \Sigma (R5 \sim R8) / \text{SUMR}$
V12	$V20 + (V8 - V20) \times 8/12$	V44	$V55 + (V43 - V55) \times 11/12$
V13	$V20 + (V8 - V20) \times 7/12$	V45	$V55 + (V43 - V55) \times 10/12$
V14	$V20 + (V8 - V20) \times 6/12$	V46	$V55 + (V43 - V55) \times 9/12$
V15	$V20 + (V8 - V20) \times 5/12$	V47	$V55 + (V43 - V55) \times 8/12$
V16	$V20 + (V8 - V20) \times 4/12$	V48	$V55 + (V43 - V55) \times 7/12$
V17	$V20 + (V8 - V20) \times 3/12$	V49	$V55 + (V43 - V55) \times 6/12$
V18	$V20 + (V8 - V20) \times 2/12$	V50	$V55 + (V43 - V55) \times 5/12$
V19	$V20 + (V8 - V20) \times 1/12$	V51	$V55 + (V43 - V55) \times 4/12$
V20	$\Delta V \times \Sigma (R4 \sim R8) / \text{SUMR}$	V52	$V55 + (V43 - V55) \times 3/12$
V21	$V43 + (V20 - V43) \times 22/23$	V53	$V55 + (V43 - V55) \times 2/12$
V22	$V43 + (V20 - V43) \times 21/23$	V54	$V55 + (V43 - V55) \times 1/12$
V23	$V43 + (V20 - V43) \times 20/23$	V55	$\Delta V \times \Sigma (R6 \sim R8) / \text{SUMR}$
V24	$V43 + (V20 - V43) \times 19/23$	V56	$V62 + (V55 - V62) \times \text{IPV56}$
V25	$V43 + (V20 - V43) \times 18/23$	V57	$V62 + (V55 - V62) \times \text{IPV57}$
V26	$V43 + (V20 - V43) \times 17/23$	V58	$V62 + (V55 - V62) \times \text{IPV58}$
V27	$V43 + (V20 - V43) \times 16/23$	V59	$V62 + (V55 - V62) \times \text{IPV59}$
V28	$V43 + (V20 - V43) \times 15/23$	V60	$V62 + (V55 - V62) \times \text{IPV60}$
V29	$V43 + (V20 - V43) \times 14/23$	V61	$V62 + (V55 - V62) \times \text{IPV61}$
V30	$V43 + (V20 - V43) \times 13/23$	V62	$\Delta V \times (R7 + R8) / \text{SUMR}$
V31	$V43 + (V20 - V43) \times 12/23$	V63	$\Delta V \times R8 / \text{SUMR}$

Note: Make sure that

$$\Delta V = V_{\text{REG1OUT}} - V_{\text{GS}}$$

$$\text{SUMR} = \Sigma (R0 \sim R8) \geq 70R$$

$$V63 \geq 0.2V$$

Table 85 GRAM Data and the Grayscale Voltage

GRAM data	Grayscale voltage				GRAM data	Grayscale voltage			
	REV = 1		REV = 0			REV = 1		REV = 0	
	Positive polarity	Negative polarity	Positive polarity	Negative polarity		Positive polarity	Negative polarity	Positive polarity	Negative polarity
6'h00	V0	V63	V63	V0	6'h20	V32	V31	V31	V32
6'h01	V1	V62	V62	V1	6'h21	V33	V30	V30	V33
6'h02	V2	V61	V61	V2	6'h22	V34	V29	V29	V34
6'h03	V3	V60	V60	V3	6'h23	V35	V28	V28	V35
6'h04	V4	V59	V59	V4	6'h24	V36	V27	V27	V36
6'h05	V5	V58	V58	V5	6'h25	V37	V26	V26	V37
6'h06	V6	V57	V57	V6	6'h26	V38	V25	V25	V38
6'h07	V7	V56	V56	V7	6'h27	V39	V24	V24	V39
6'h08	V8	V55	V55	V8	6'h28	V40	V23	V23	V40
6'h09	V9	V54	V54	V9	6'h29	V41	V22	V22	V41
6'h0A	V10	V53	V53	V10	6'h2A	V42	V21	V21	V42
6'h0B	V11	V52	V52	V11	6'h2B	V43	V20	V20	V43
6'h0C	V12	V51	V51	V12	6'h2C	V44	V19	V19	V44
6'h0D	V13	V50	V50	V13	6'h2D	V45	V18	V18	V45
6'h0E	V14	V49	V49	V14	6'h2E	V46	V17	V17	V46
6'h0F	V15	V48	V48	V15	6'h2F	V47	V16	V16	V47
6'h10	V16	V47	V47	V16	6'h30	V48	V15	V15	V48
6'h11	V17	V46	V46	V17	6'h31	V49	V14	V14	V49
6'h12	V18	V45	V45	V18	6'h32	V50	V13	V13	V50
6'h13	V19	V44	V44	V19	6'h33	V51	V12	V12	V51
6'h14	V20	V43	V43	V20	6'h34	V52	V11	V11	V52
6'h15	V21	V42	V42	V21	6'h35	V53	V10	V10	V53
6'h16	V22	V41	V41	V22	6'h36	V54	V9	V9	V54
6'h17	V23	V40	V40	V23	6'h37	V55	V8	V8	V55
6'h18	V24	V39	V39	V24	6'h38	V56	V7	V7	V56
6'h19	V25	V38	V38	V25	6'h39	V57	V6	V6	V57
6'h1A	V26	V37	V37	V26	6'h3A	V58	V5	V5	V58
6'h1B	V27	V36	V36	V27	6'h3B	V59	V4	V4	V59
6'h1C	V28	V35	V35	V28	6'h3C	V60	V3	V3	V60
6'h1D	V29	V34	V34	V29	6'h3D	V61	V2	V2	V61
6'h1E	V30	V33	V33	V30	6'h3E	V62	V1	V1	V62
6'h1F	V31	V32	V32	V31	6'h3F	V63	V0	V0	V63

Power-supply Generating Circuit

The following figures show the configurations of liquid crystal drive voltage generating circuit of the R61505V.

Power supply circuit connection example 1

VCI1 voltage level is defined by VC bit (R11h).

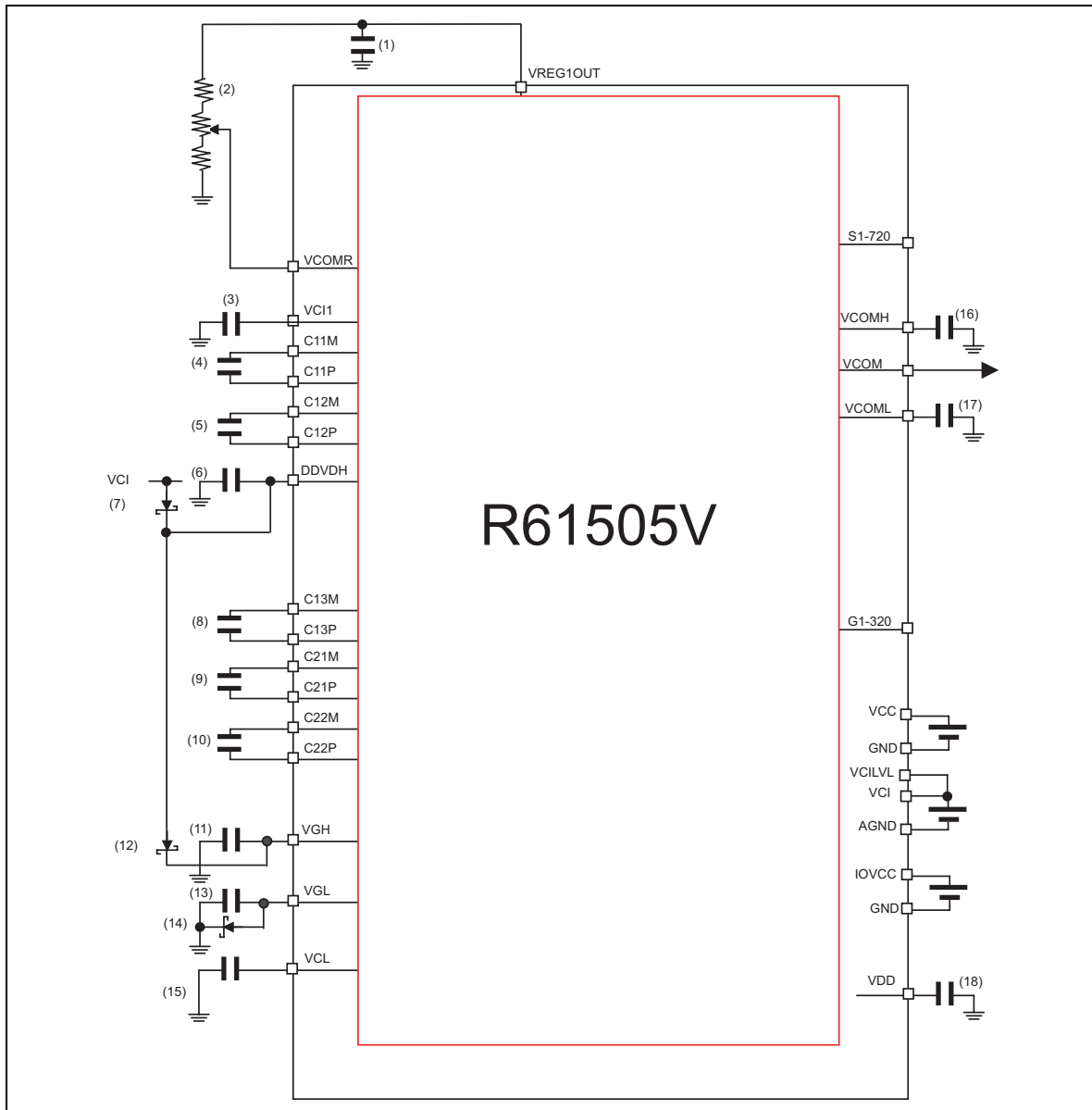
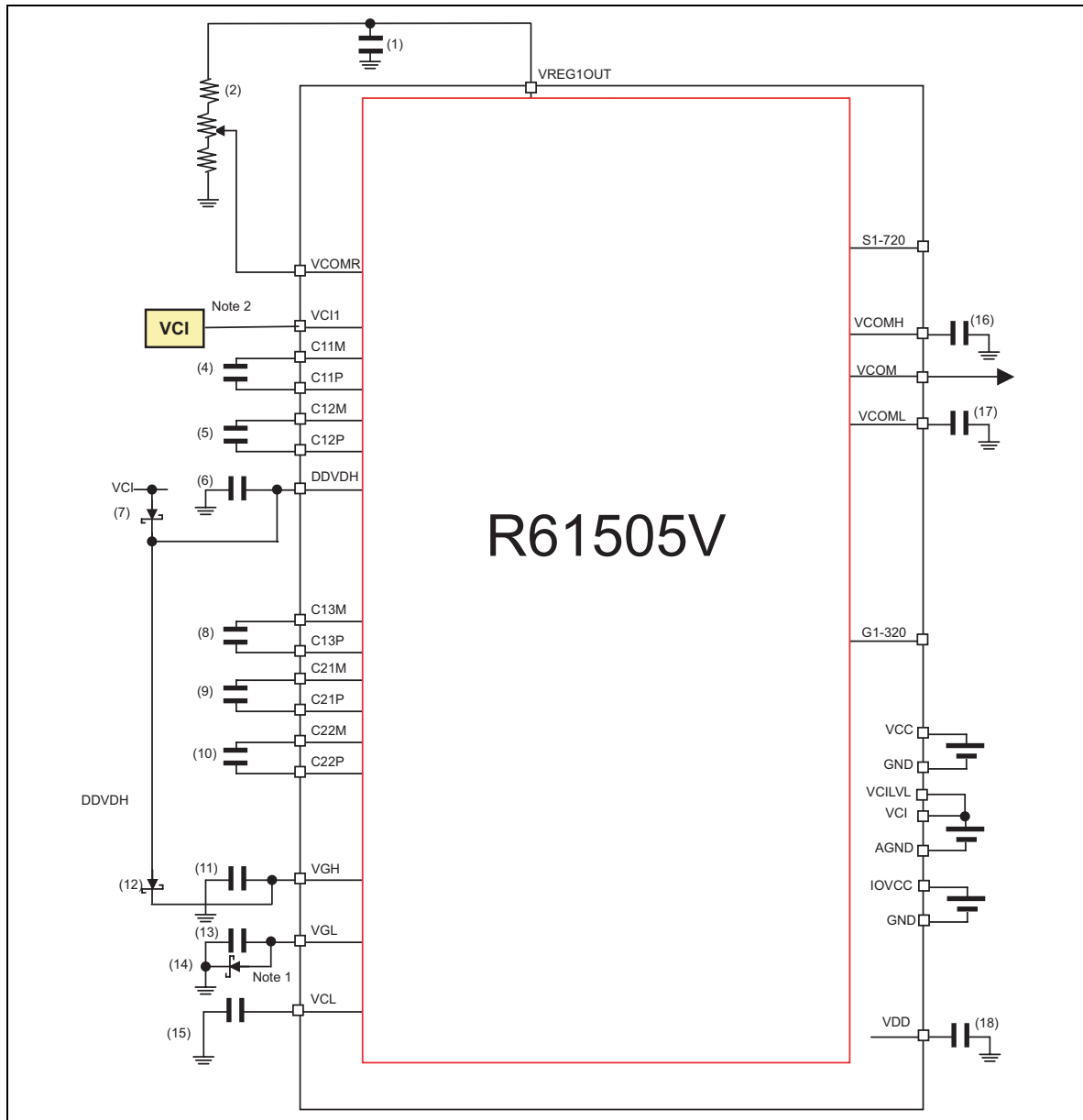


Figure 59

Note: The wiring resistances between the schottky diode and GND/VGL must be 10Ω or less.

Power supply circuit connection example 2 (VCI voltage is directly applied to VCI1 pin)

In the following example, the electrical potential VCI is directly applied to VCI1. In this case, step-up operation is more effective although VCI1 voltage level cannot be defined by VC bit (R11h).

**Figure 60**

- Notes: 1. The wiring resistances between the schottky diode and GND/VGL must be 10Ω or less.
 2. When directly applying the VCI level to VCI1, set VC = 3'h7. Capacitor connection to VCIOUT is not required.

Specifications of Power-supply Circuit External Elements

The specifications of external elements connected to the power-supply circuit of the R61505V are as follows. The numbers in the parentheses correspond with the numbers of the elements in the section “Power Supply Generating Circuit”.

Table 86 Capacitor

Capacitance	Voltage proof	Pin Connection
1 μ F (B characteristics)	6V	(1) VREG1OUT, (3) VCI1, (4) C11P, C11M, (5) C12P, C12M, (8) C13P, C13M, (15) VCL, (16) VCOMH, (17) VCOML
	3V	(18) VDD
	10V	(6) DDVDH, (9) C21P, C21M, (10) C22P, C22M
	25V	(11) VGH, (14) VGL

Table 87 Schottky Diode

Specification	Pin Connection
VF < 0.38V (max)/ IF=5mA @ 25C, VR ≥ 25V (Recommended diode: HS*226)	(14) GND–VGL, (12) DDVDH–VGH, (7) VCI–DDVDH

Table 88 Variable Resistor

Specification	Pin Connection
> 200 k Ω	(2) VCOMR

Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the R61505V and the TFT display application voltage waveforms and electrical potential relationship.

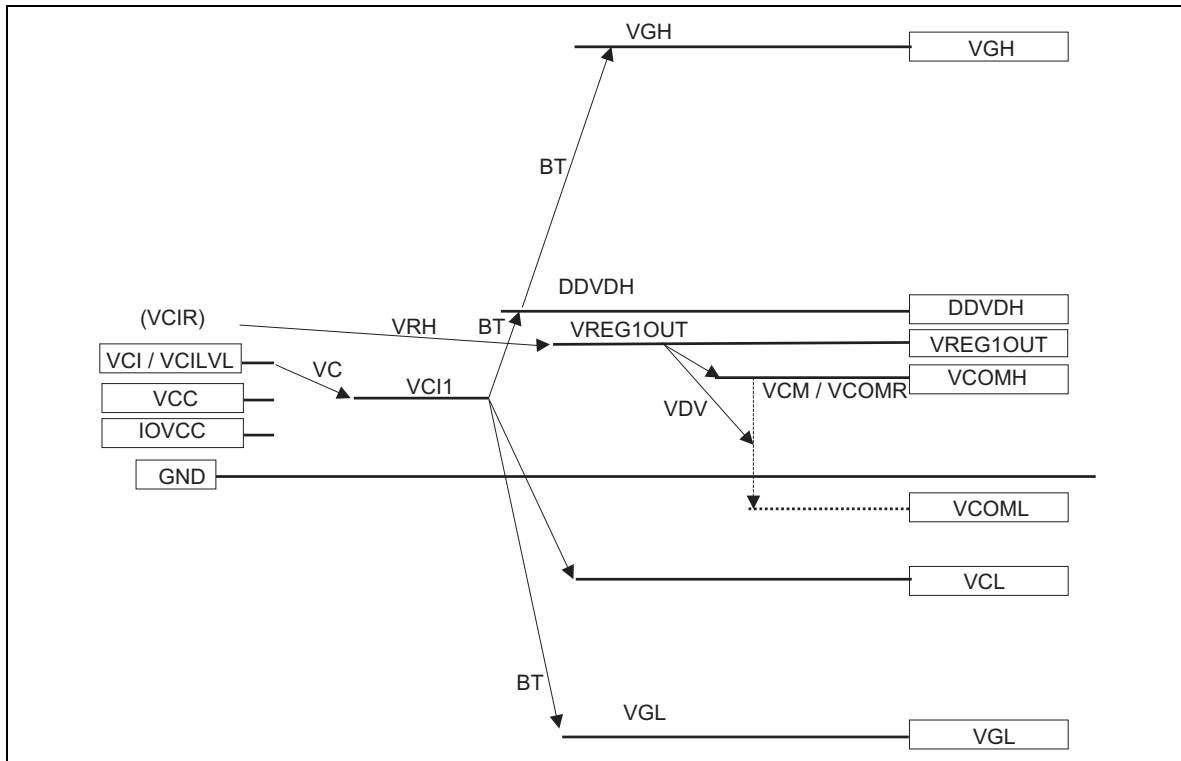


Figure 61

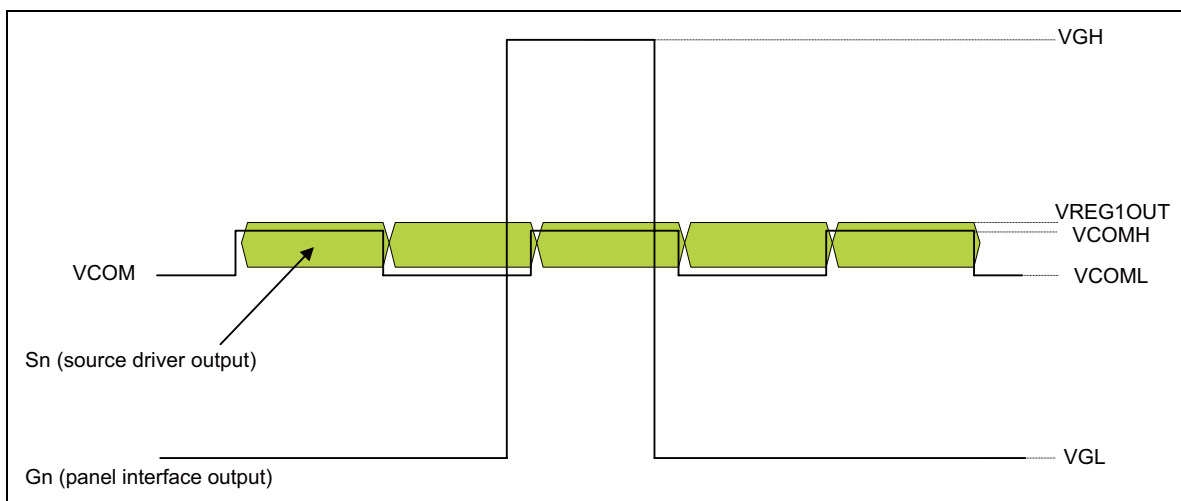


Figure 62 Liquid crystal application voltage waveform and electrical potential

VCOMH Voltage Adjustment Sequence

When adjusting the VCOMH voltage by setting VCM1 [6:0] in the R29'h register (internal VCOMH level adjustment circuit), follow the sequence below. The R61505V can retain the VCOMH level adjustment setting values in NVM, which allows erasing 5 times.

To write data onto the NVM, set VCOMH adjusting register VCM1 [6:0] (R29h), VCMSEL and VCM2[6:0] (R2Ah) so that these registers correspond with NVM write data register NVDAT [15:0]. See NVM write, read and erase sequences in the section "NVM Control Sequence".

If data has been erased from the bit, the bit value is set to "1". The bit to which data is not written should be set to 1.

If VCMSEL=1, VCM1 is enabled. If VCMSEL=0, VCM2 is enabled.

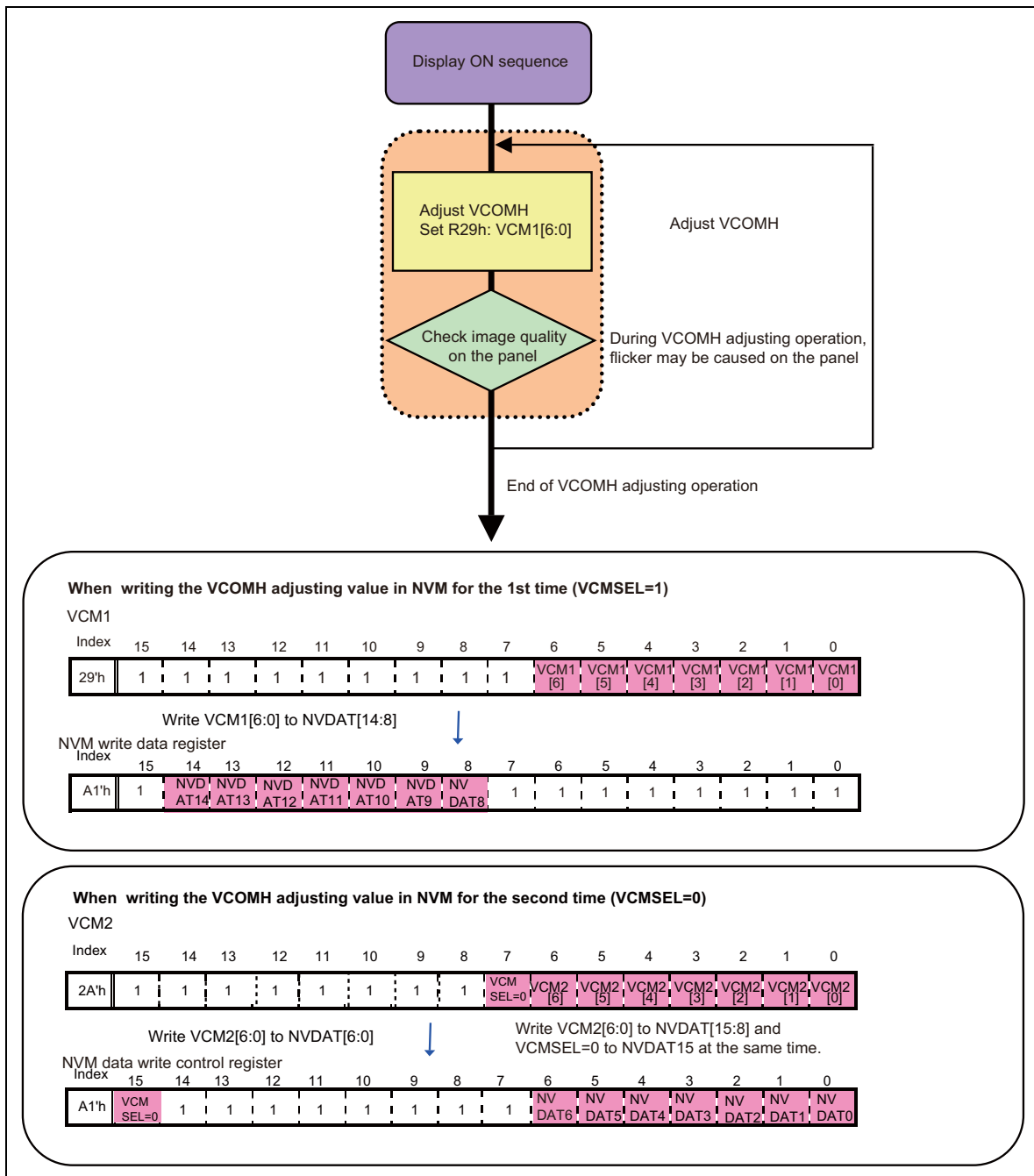


Figure 63

NVM Control Sequence

Apply voltages to VPP1, 2, 3A, 3B and 3C pins as the table below when executing NVM write, read and erase.

Table 89

Operation	Power supply voltage		Time	Note	Temperature
NVM Write	VPP1	$9.2 \pm 0.3V$	Write period: 150ms±50ms	-	+20 ~ +30C
	VPP2	$9.2 \pm 0.3V$			
	VPP3A	Open or GND			
NVM Erase	VPP1	$9.2 \pm 0.3V$	Erase period: 10ms±1ms x n time(s) (n = 60 or less, total = within 300ms)	Verify NVM erase at intervals of 10ms±1ms.	+20 ~ +30C
	VPP2	$9.2 \pm 0.3V$			
	VPP3A	$-9.2 \pm 0.3V$			
Except NVM Write/Erase	VPP1	Open or GND	-	-	-40 ~ +85C
	VPP2	Open or GND			
	VPP3A	Open or GND			

Note: NVM data rewrite operation should be performed up to 5 times per address.

Follow the sequences shown in this section to use NVM.

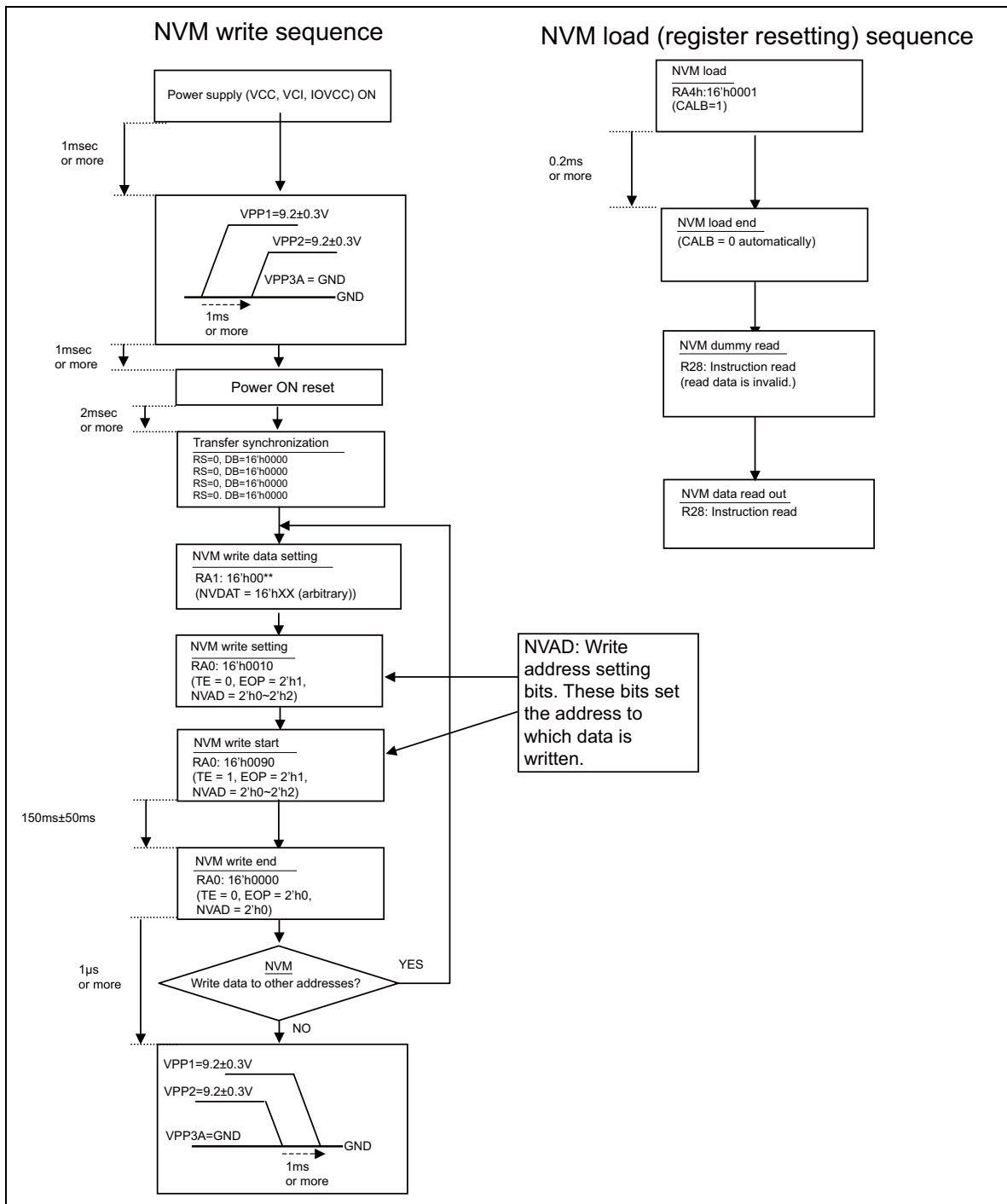


Figure 64

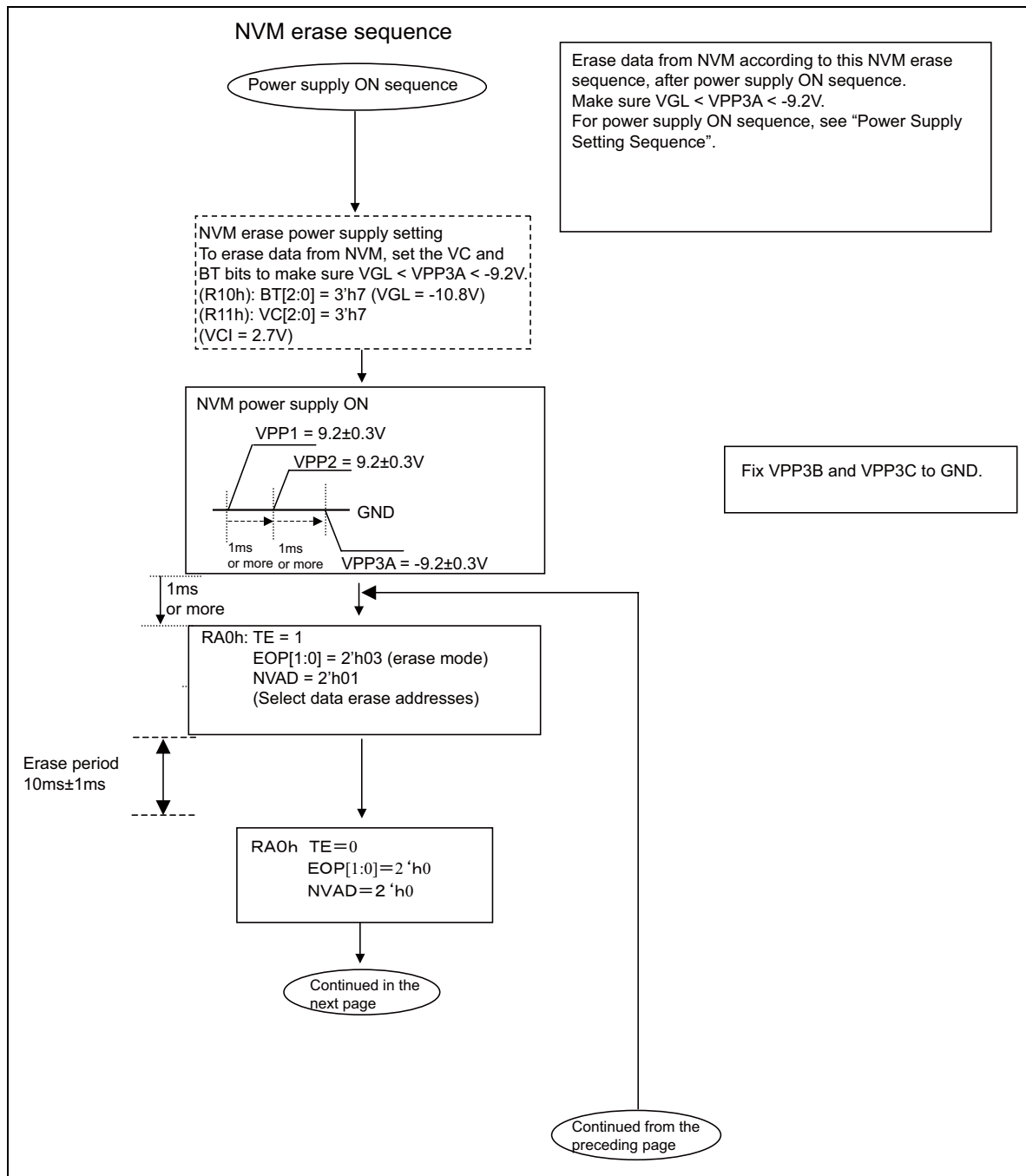


Figure 65

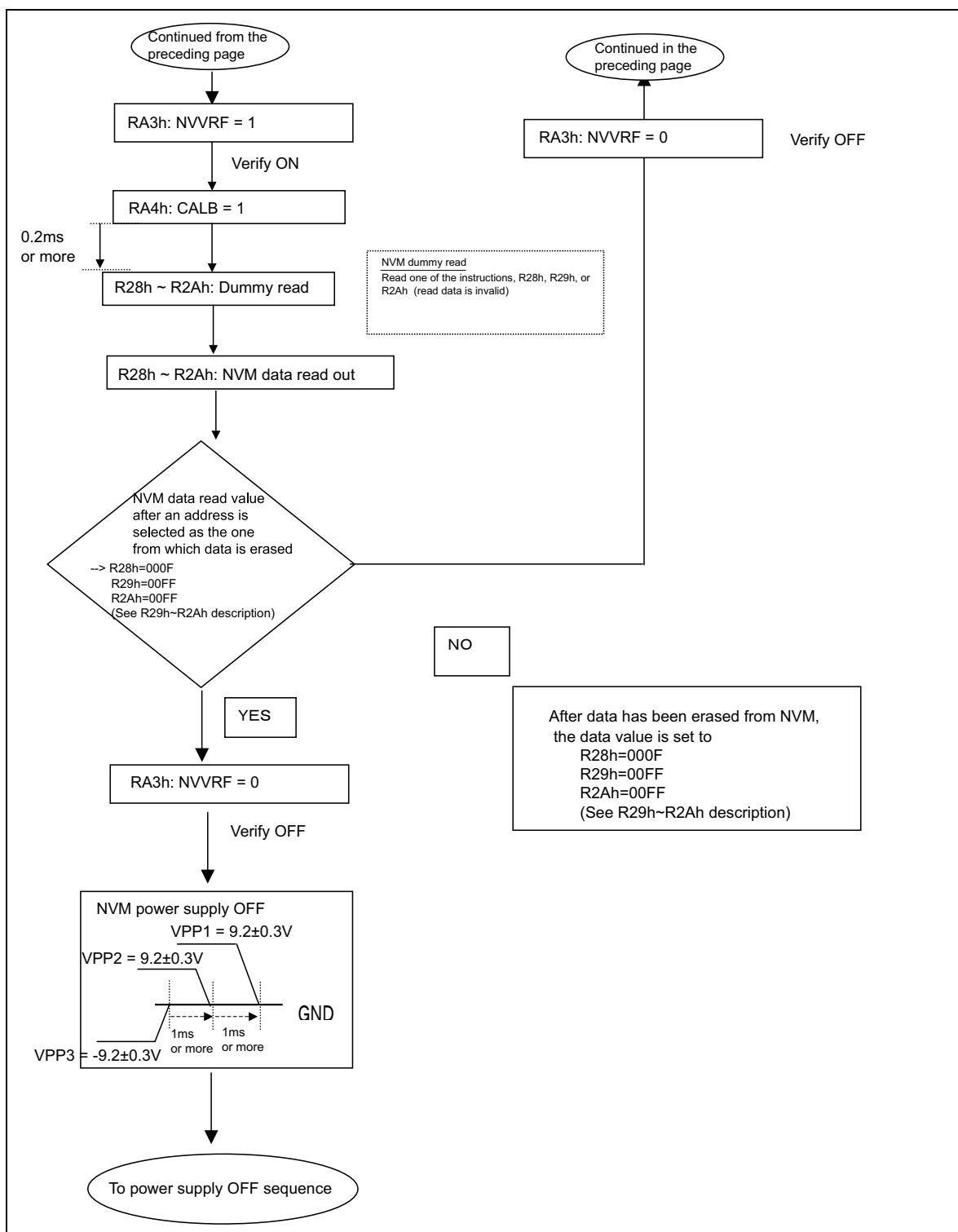


Figure 66

Power Supply Setting Sequence

Power supply ON/OFF sequences are as follows. Execute these sequences when turning the display on/off, and setting/exiting sleep mode.

R61505U Compatible Sequence

Execute the following sequences when the software used with the R61505V is compatible with that used with the display module incorporating the R61505U.

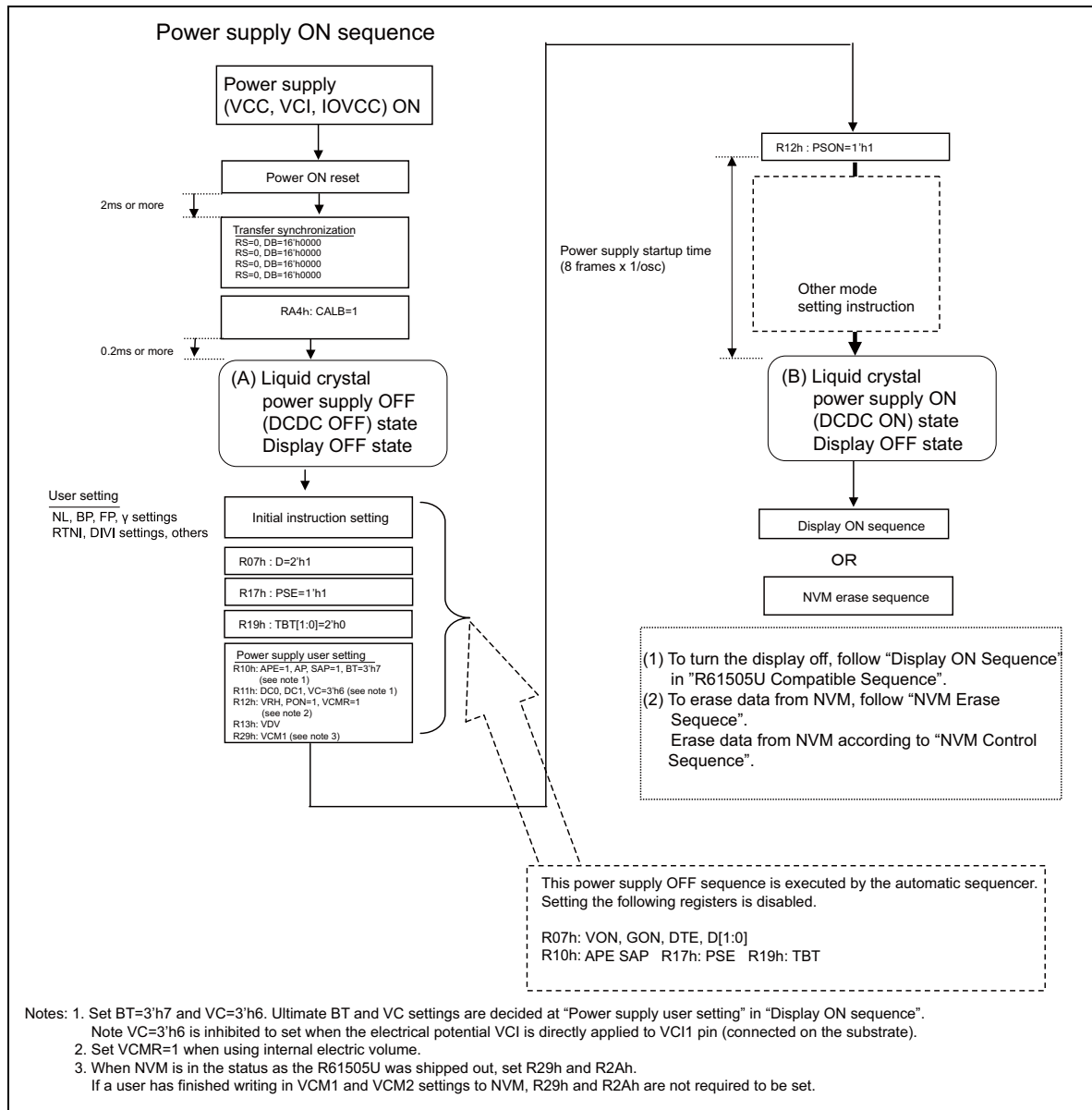


Figure 67

Power supply OFF sequence

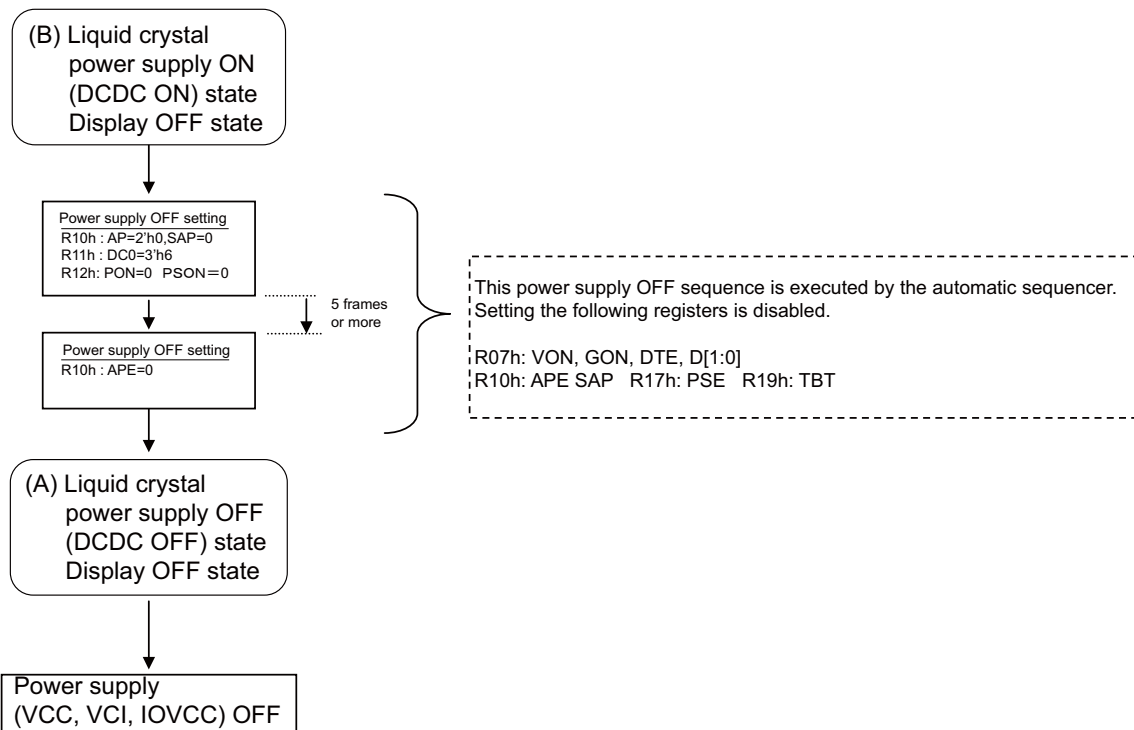


Figure 68

R61505V Setting Sequence

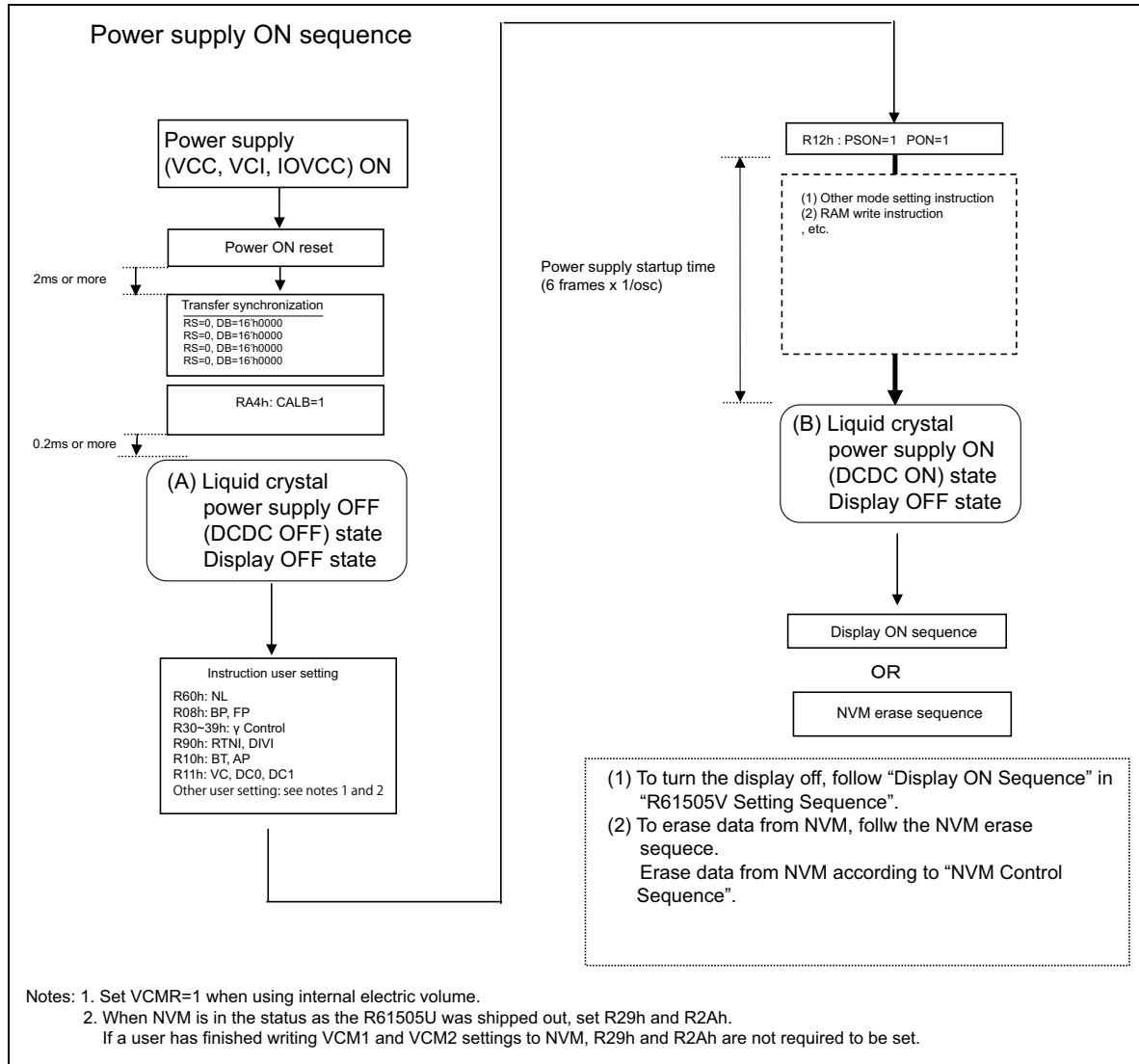


Figure 69

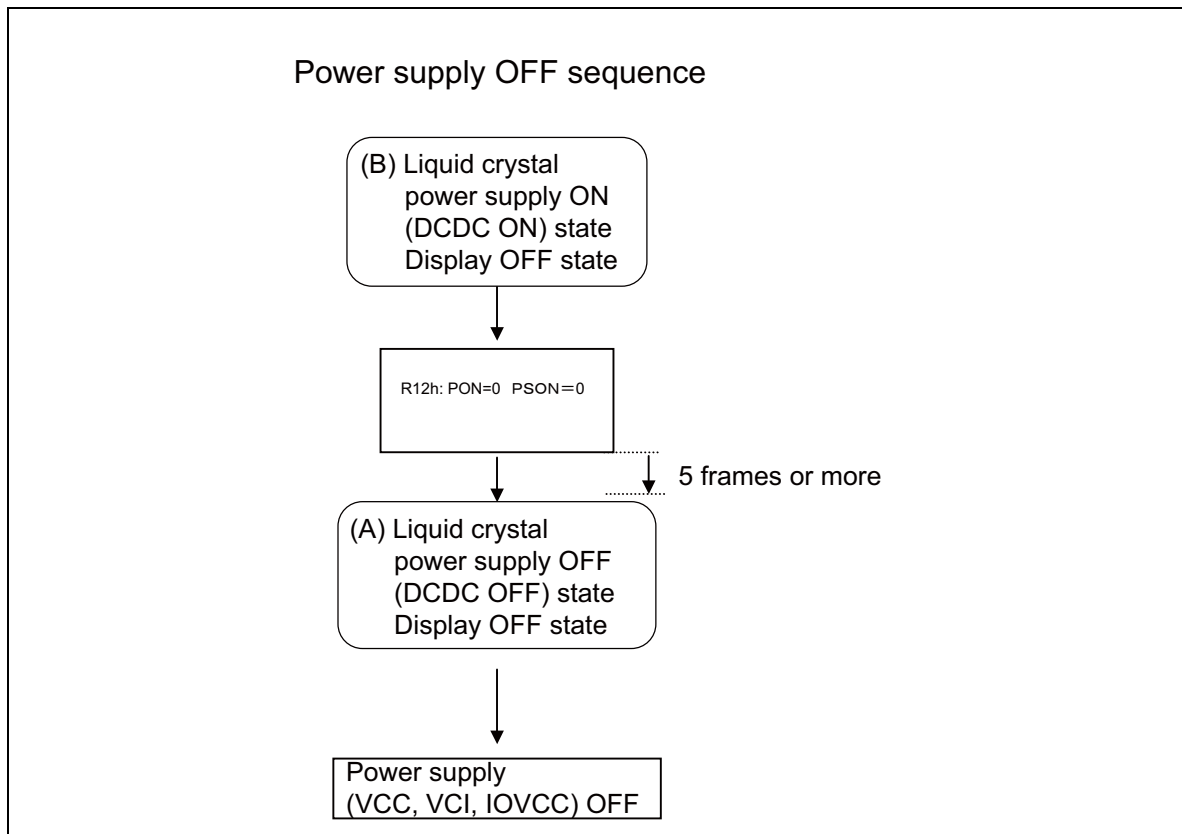


Figure 70

Instruction Setting Sequence

The following are the sequences for various instruction settings. When setting instruction in the R61505V, follow the relevant sequence below.

R61505U Compatible Sequence

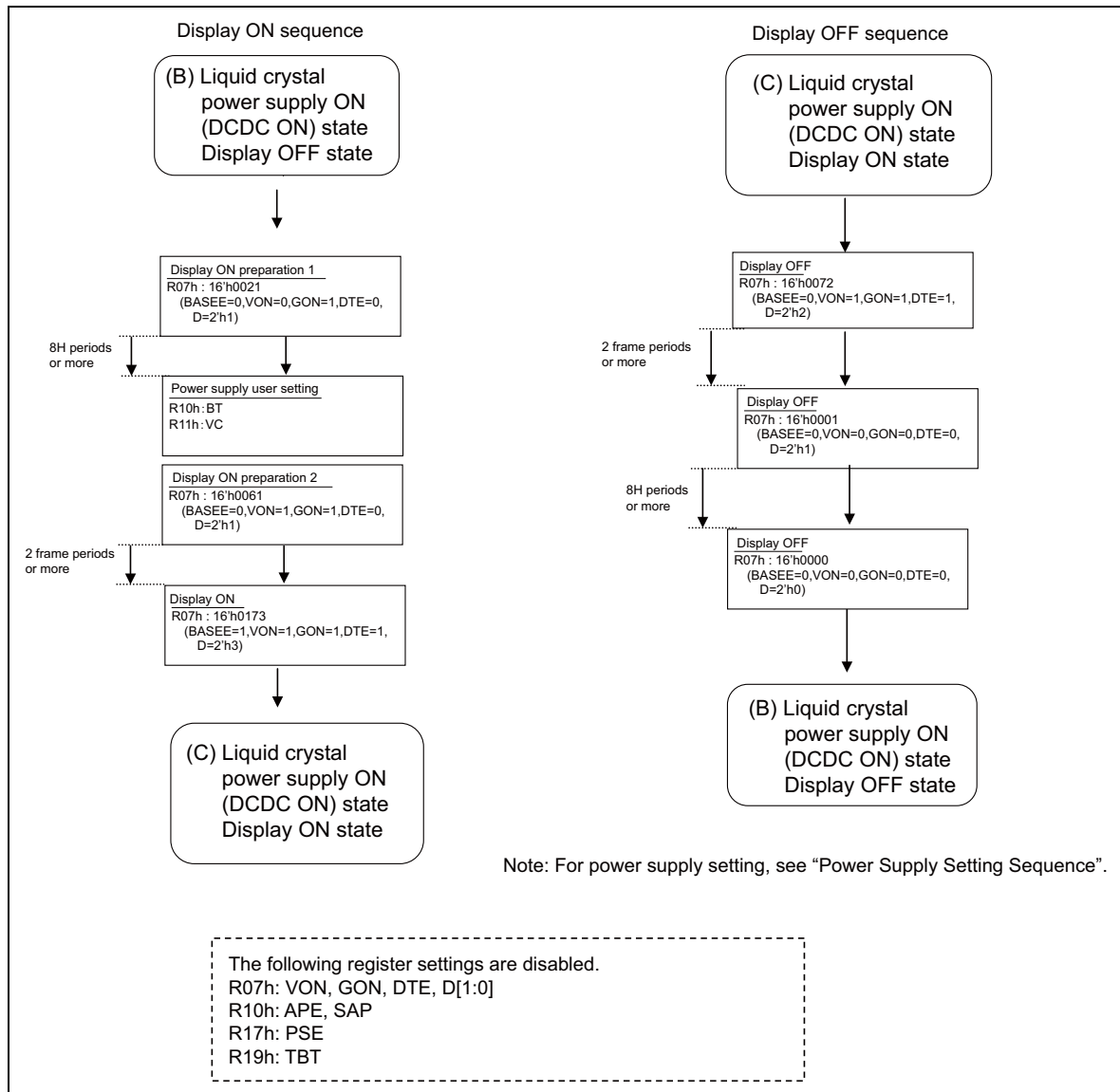
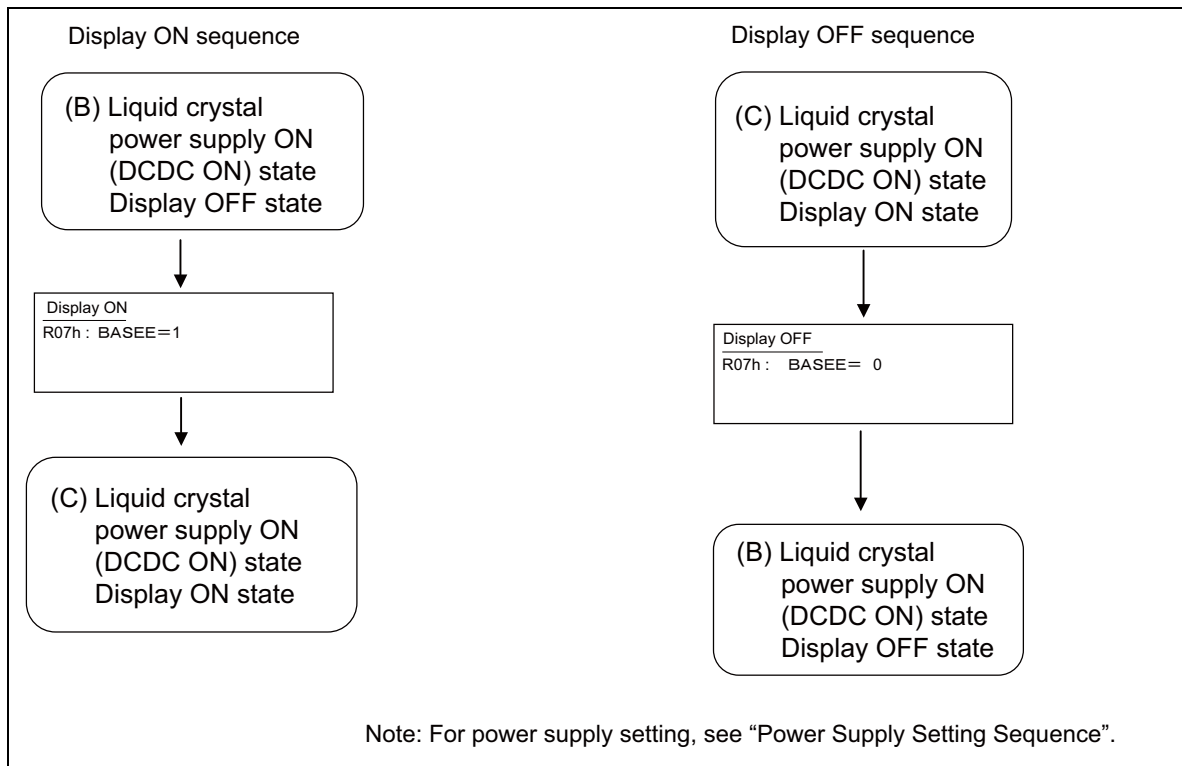


Figure 71

R61505V Setting Sequence

To make the R61505V operate according to the following sequence, develop software newly (this software is not compatible with that used with the display module incorporating the R61505U).

**Figure 72**

Other Mode Transition Setting Sequences

Deep Standby Mode IN/EXIT Sequences

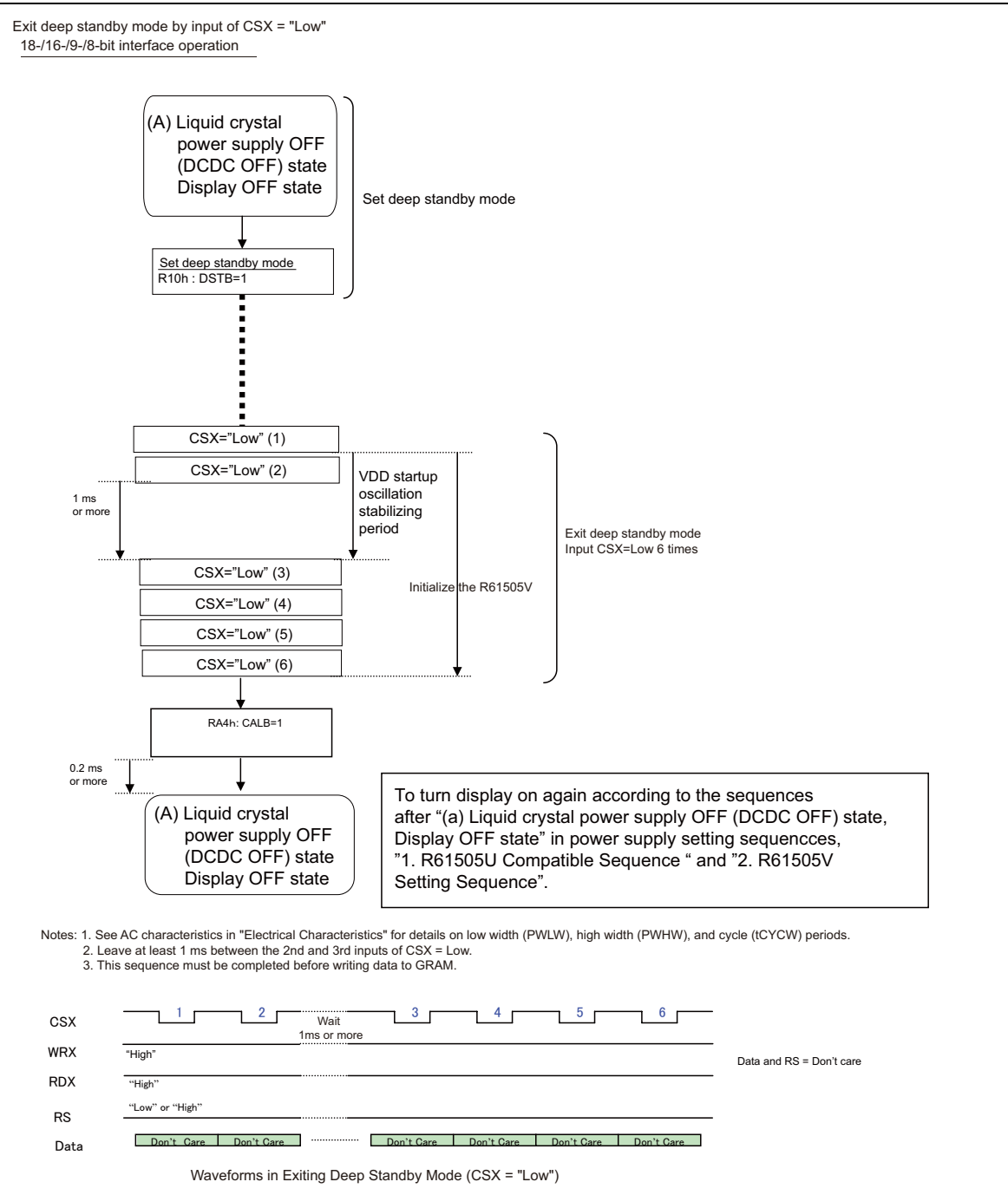


Figure 73 Cancel standby mode by inputting CS="Low" (18-/ 16-/ 9-/ 8- bit interface)

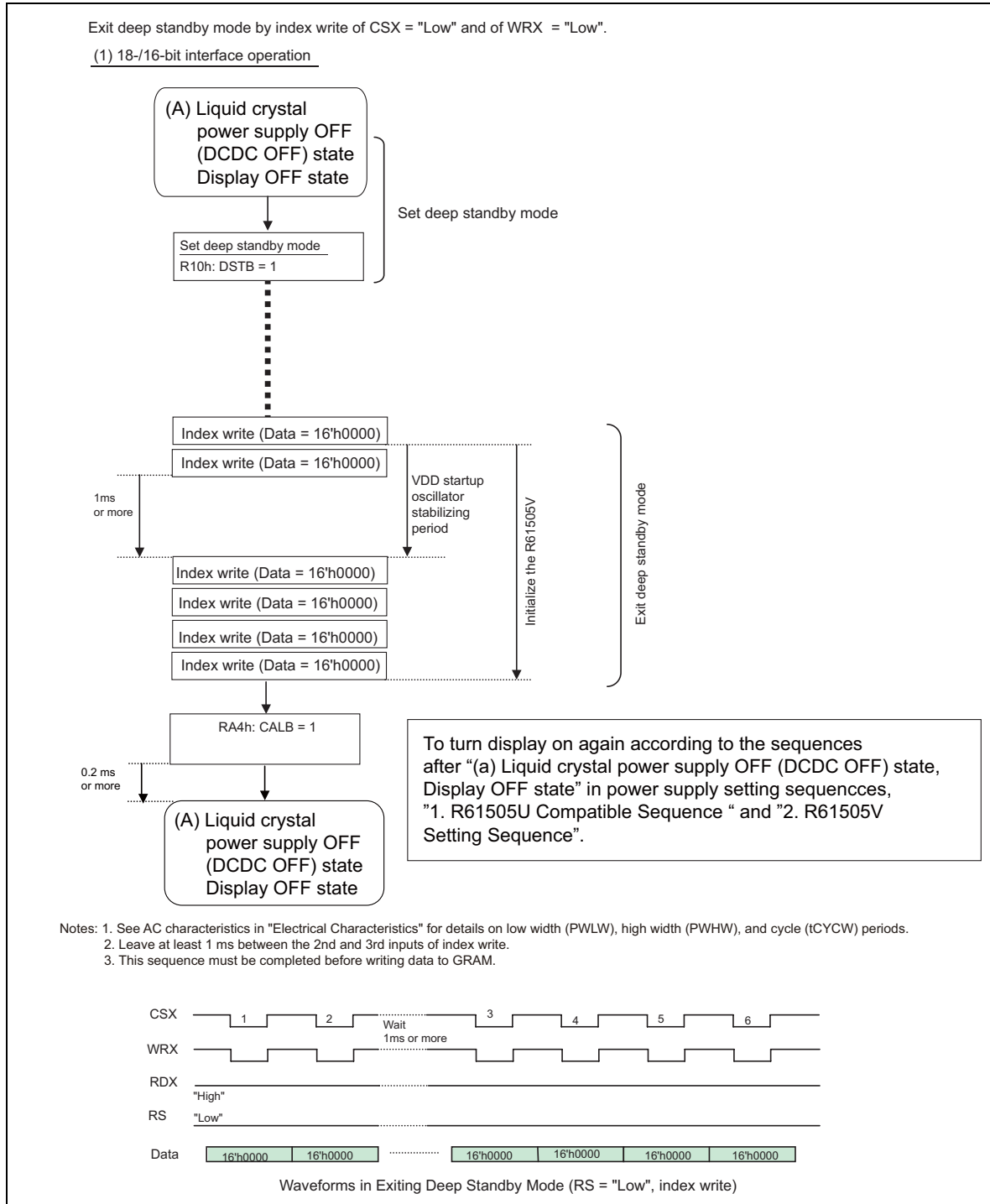
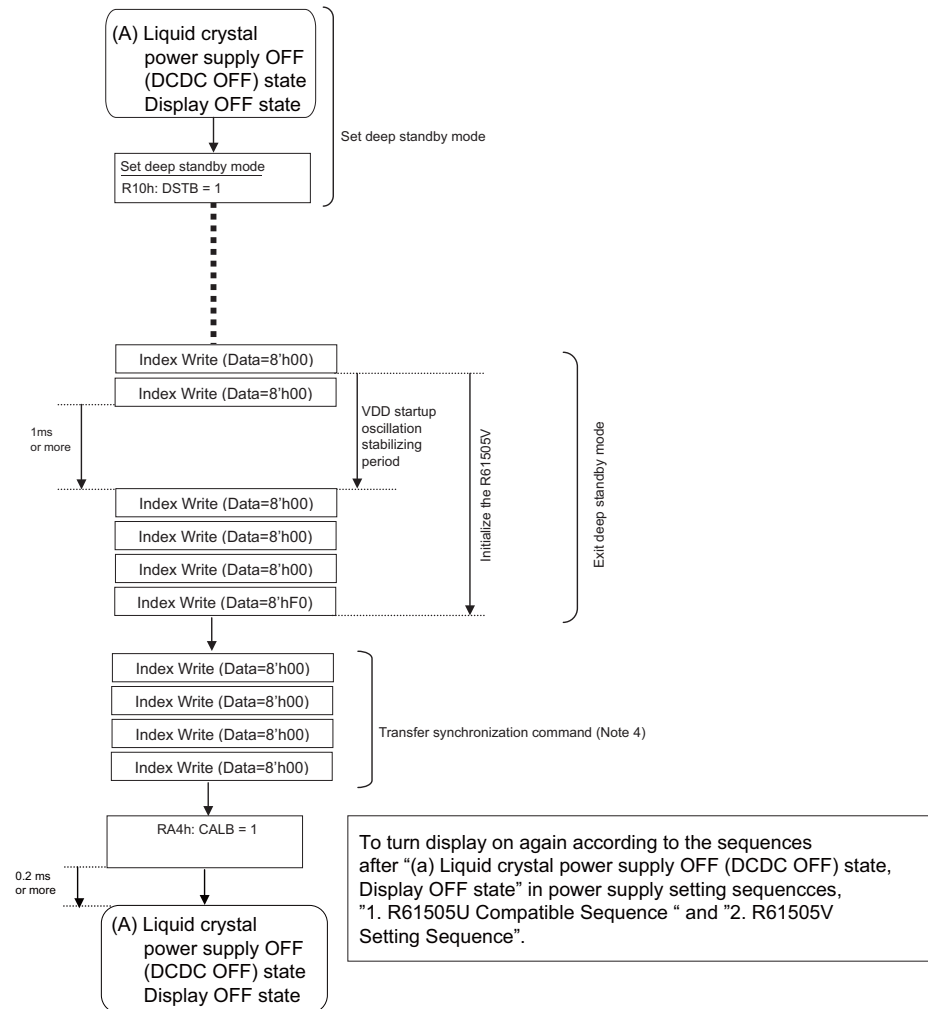
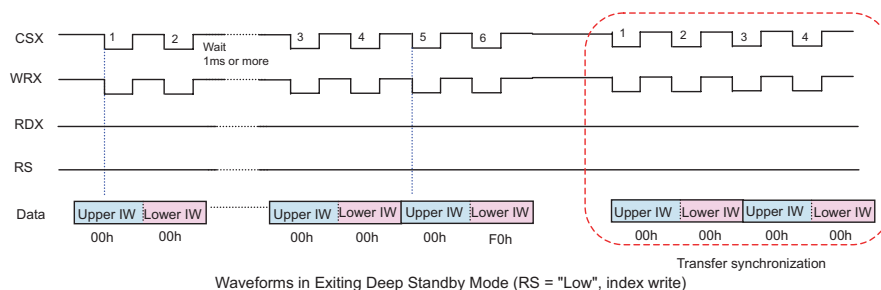


Figure 74 Cancel deep standby mode by inputting CS="Low" and WR="Low" (18-/ 16 bit interface)

(2) 9-/8-bit interface operation



Notes: 1. See AC characteristics in "Electrical Characteristics" for details on low width (PWLW), high width (PWHW), and cycle (tCYCW) periods.
2. Leave at least 1 ms between the 2nd and 3rd inputs of index write.
3. This sequence must be completed before writing data to GRAM.
4. Set transfer synchronization command data to 8'h00 in 8-bit interface operation, and 9'h00 in 9-bit interface operation, respectively.



Execute transfer synchronization command after exiting deep standby mode by input of RS = Low and index write.

Figure 75 Cancel deep standby mode by inputting CS="Low" and WR="Low" (9-/ 8- bit interface)

8-color Mode Setting

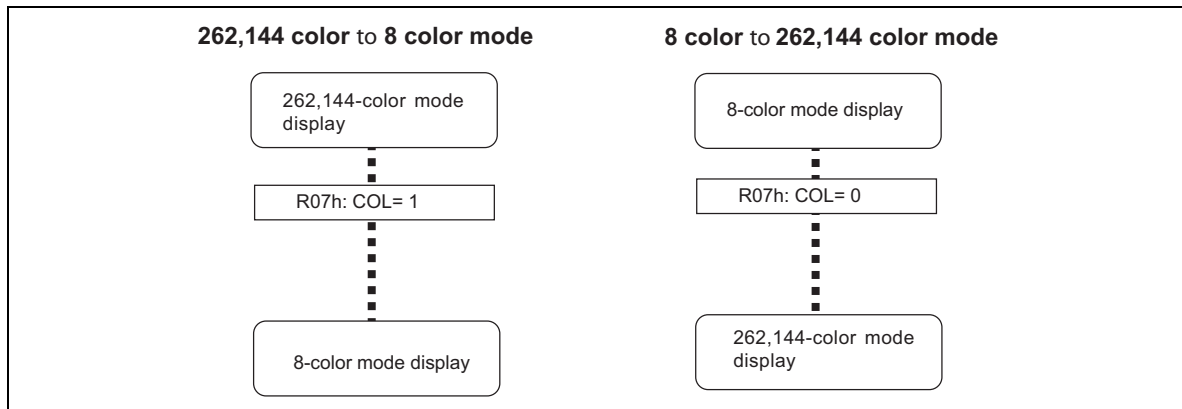


Figure 76

Partial Display Setting

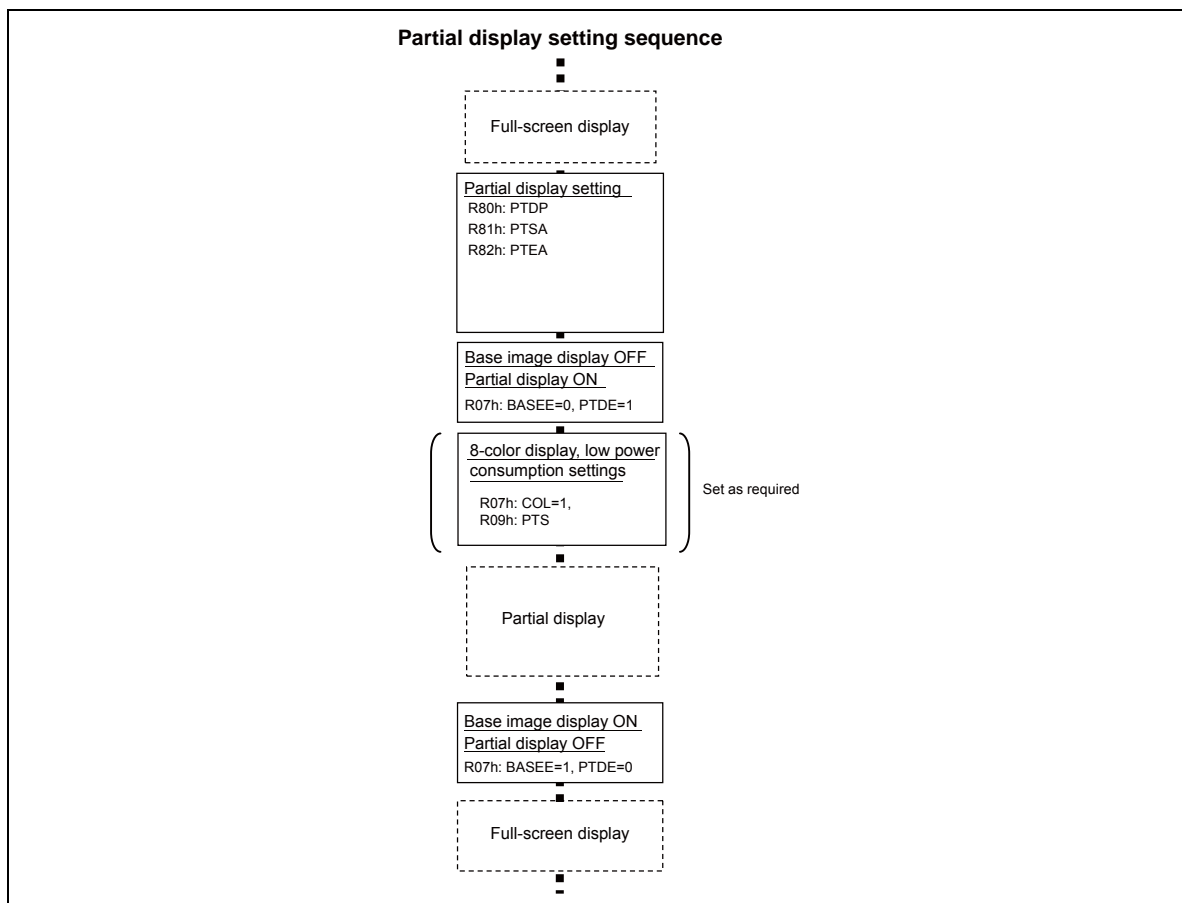


Figure 77

Absolute Maximum Ratings

Table 90

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VCC, IOVCC	V	-0.3 ~ +4.6	1, 2
Power Supply Voltage 2	VCI – AGND	V	-0.3 ~ +4.6	1, 3
Power Supply Voltage 3	DDVDH – AGND	V	-0.3 ~ +6.5	1, 4
Power Supply Voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ~ +9.0	1, 5
Power Supply Voltage 7	AGND – VGL	V	-0.3 ~ +13.0	1, 6
Power Supply Voltage 8	VGH– VGL	V	-0.3 ~ +30.0	1
Power Supply Voltage 9	VPP1	V	-0.3 ~ +10.0	1
Power Supply Voltage 10	VPP2	V	-0.3 ~ +10.0	1
Power Supply Voltage 11	VPP3A	V	-10.0 ~ +0.3	1
Input Voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1
Operating Temperature	Topr	°C	-40 ~ +85	1, 7
NVM Write Temperature	Twep	°C	+20 ~ +30	1
NVM Erase Temperature	Teep	°C	+20 ~ +30	1
Storage Temperature	Tstg	°C	-55 ~ +110	1

Notes 1. If the R61505V is used beyond the absolute maximum ratings, the LSI may be permanently damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure $VCC(\text{high}) \geq GND(\text{low})$, $IOVCC(\text{high}) \geq GND(\text{low})$.
3. Make sure $VCI(\text{high}) \geq AGND(\text{low})$.
4. Make sure $DDVDH(\text{high}) \geq AGND(\text{low})$.
5. Make sure $DDVDH(\text{high}) \geq VCL(\text{low})$.
6. Make sure $AGND(\text{high}) \geq VGL(\text{low})$.
7. The DC/AC characteristics of die and wafer products are guaranteed at 85°C.

Electrical Characteristics

DC Characteristics

Table 91 DC Characteristics 1 (VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C) (See note 1)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input "High" level voltage 1 Except RESETX pin	V_{IH1}	V	IOVCC=1.65V ~ 3.30V	$0.80 \times$ IOVCC	—	IOVCC	2, 3
Input "Low" level voltage 1 Except RESETX pin	V_{IL1}	V	IOVCC=1.65V ~ 3.30V	-0.3	—	$0.20 \times$ IOVCC	2, 3
Input "High" level voltage 2 RESETX pin	V_{IH2}	V	IOVCC=1.65V ~ 3.30V	$0.90 \times$ IOVCC	—	IOVCC	2, 3
Input "Low" level voltage 2 RESETX pin	V_{IL2}	V	IOVCC=1.65V ~ 3.30V	-0.3	—	$0.10 \times$ IOVCC	2, 3
Output "High" level voltage 1 (DB0-17, FMARK)	V_{OH}	V	IOVCC=1.65V ~ 3.30V, IOH=-0.1mA	$0.8 \times$ IOVCC	—	—	2
Output "Low" level voltage 1 (DB0-17, FMARK)	V_{OL}	V	IOVCC=1.65V ~ 3.30V, IOL=0.1mA	—	—	$0.20 \times$ IOVCC	2
Input / Output leakage current	I_{LI}	μ A	Vin=0 ~ IOVCC	-1	—	1	4
Current Consumption ((IOVCC-GND) + (VCC-GND)) Normal operation mode (260k-color, display operation)	I_{OP1}	μ A	fosc=600kHz (320 line drive), IOVCC=VCC=3.00V, fFLM=70Hz, Ta=25°C, RAM data: 18'h000000 See below for other data.	—	190	400	5
Current Consumption ((IOVCC-GND) + (VCC-GND)) 8-color mode, 64-line partial display operation	I_{OP2}	μ A	fosc=600kHz (64-line, partial display), IOVCC=VCC=3.00V, fFLM=40Hz, Ta=25°C, RAM data: 18'h'000000 See below for other data.	—	140	—	5
Current Consumption ((IOVCC-GND) + (VCC-GND)) Deep standby mode	I_{DST}	μ A	IOVCC=VCC=3.00V, Ta=25°C	—	0.1	1.0	5
Current Consumption ((IOVCC-GND) + (VCC-GND)) RAM access mode	I_{RAM1}	mA	IOVCC=2.40V, VCC=3.00V, tCYCW=125ns, Ta=25°C, I80-8bit-I/F, TRIREG=1'h1, Consecutive RAM access during display operation.	—	2.0	—	5

LCD Power Supply Current (VCI-GND) 260-k color display operation	Ici1	mA	IOVCC=1.8V, VCC=VCI=2.8V, 320 line drive, fFLM=60Hz, Ta=25°C, Frame memory data: 18'h00000, REV=0, BC0=0, FP0=8, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h4, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel, COL=0	—	3.2	5.0	5
LCD Power Supply Current (VCI-GND) 8-color (64-line partial) display operation	Ici2	mA	IOVCC=1.8V, VCC=VCI=2.8V, 64 line partial display, fFLM=40Hz, Ta=25°C, Frame memory data: 18'h00000, REV=0, BC2=0, FP2=5, BP2=8, VC=3'h1, BT=3'h4, VRH=5'h18, VCM=7'h7F, VDV=5'h11, AP2=2'h3, DC02=3'h4, DC12=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) No load on the panel, COL=1	—	0.8	—	5
Output voltage dispersion	ΔV_O	mV	—	—	5	—	6
Average output voltage variance	ΔV_{Δ}	mV	—	-35	—	35	7

Table 92 DC Characteristics 2 (Step-Up Circuit Characteristics)

Item	Unit	Test Condition	Min.	Typ.	Max.	Note
Step-up Output Voltage	DDVDH	V	4.8	5.1	-	-
		IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, No load on the panel, Iload1= -3 [mA]				
	VGH	V	14.4	15.1	-	-
		IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload2=-100[uA], No load on the panel				
	VGL	V	-	-10.0	-9.6	-
		IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload3=+100[uA], No load on the panel				
	VCL	V	-	-2.55	-2.4	-
		IOVCC=VCC=2.8V, VCI =2.8V, Ta=25°C, VC=3'h1, BT=3'h4, AP=2'h3, DC0=3'h4, DC1=3'h2, C11=C12=C13=C21=C22=1[uF]/B characteristics, DDVDH=VGH=VGL=VCL=1[uF]/B characteristics, Iload4=+200[uA], No load on the panel				

Table 93 DC Characteristics 3 (NVM Control)

Item			Symbol	Unit	Test condition	Min.	Typ.	Max.	Note
NVM current consumption	Write	VPP1-AGND	I_{VPP1W}	mA	VPP1=9.2V VPP2=9.2V VPP3A=GND (during Write period)	—	—	1.0	
		VPP2-AGND	I_{VPP2W}	mA		—	—	30.0	
		VPP3A-AGND	I_{VPP3AW}	mA		—	—	1.0	
	Erase	VPP1-AGND	I_{VPP1E}	mA	VPP1=9.2V VPP2=9.2V VPP3A= -9.2V (during Erase period)	—	—	1.0	
		VPP2-AGND	I_{VPP2E}	mA		—	—	1.0	
		VPP3A-AGND	I_{VPP3AE}	mA		—	—	1.0	

Table 94 Power supply voltage range for NVM Control

Item	Symbol	Unit	Min.	Typ.	Max.	Operation
Power supply voltage	VPP1	V	8.9	9.2	9.5	Write
		V	8.9	9.2	9.5	Erase
Power supply voltage	VPP2	V	8.9	9.2	9.5	Write
		V	8.9	9.2	9.5	Erase
Power supply voltage	VPP3A	V	-0.3	0.0	+0.3	Write
		V	-8.9	-9.2	-9.5	Erase

Table 95 Internal Reference Voltage (VCC = 2.50V ~ 3.30V, Ta = 25°C)

Item	Symbol	Unit	Min.	Typ.	Max.	Note
Internal Reference Voltage	VCIR	V	-	2.50	-	11

AC Characteristics

(VCC= 2.50V~3.30V, IOVCC=1.65V~3.30V, Ta=-40C~+85C) (See note 1)

Clock Characteristics

Table 96

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.
Internal oscillation clock	f _{osc}	kHz	IOVCC=VCC=3.0V 25°C	558	600	642

80-System Bus Interface Timing Characteristics (18-/ 16-bit Interface)

Table 97 (IOVCC=1.65V ~ 3.30V)

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	t _{CYCW}	ns	Figure A	75	—	—
	Read	t _{CYCR}	ns	Figure A	450	—	—
Write low-level pulse width		PWLW	ns	Figure A	40	—	—
Read low-level pulse width		PWLR	ns	Figure A	170	—	—
Write high-level pulse width		PWHW	ns	Figure A	25	—	—
Read high-level pulse width		PWHR	ns	Figure A	250	—	—
Write / Read rise/ fall time		t _{WRr} , t _{WRf}	ns	Figure A	—	—	25
Setup time	Write (RS to CSX, WRX)	t _{AS}	ns	Figure A	0	—	—
	Read (RS to CSX, RDX)		ns	Figure A	10	—	—
Address hold time		t _{AH}	ns	Figure A	2	—	—
Write data setup time		t _{DSW}	ns	Figure A	25	—	—
Write data hold time		t _H	ns	Figure A	10	—	—
Read data delay time		t _{DDR}	ns	Figure A	—	—	150
Read data hold time		t _{DHR}	ns	Figure A	5	—	—

80-System Bus Interface Timing Characteristics (9-/ 8-bit Interface)**Table 98 (IOVCC=1.65V ~ 3.30V)**

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW	ns	Figure A	70	—	—
	Read	tCYCR	ns	Figure A	450	—	—
Write low-level pulse width		PWLW	ns	Figure A	30	—	—
Read low-level pulse width		PWLR	ns	Figure A	170	—	—
Write high-level pulse width		PWHW	ns	Figure A	25	—	—
Read high-level pulse width		PWHR	ns	Figure A	250	—	—
Write / Read rise/ fall time		tWRr, WRf	ns	Figure A	—	—	25
Setup time	Write (RS to CSX, WRX)	tAS	ns	Figure A	0	—	—
	Read (RS to CSX, RDX)		ns	Figure A	10	—	—
Address hold time		tAH	ns	Figure A	2	—	—
Write data setup time		tDSW	ns	Figure A	25	—	—
Write data hold time		tH	ns	Figure A	10	—	—
Read data delay time		tDDR	ns	Figure A	—	—	150
Read data hold time		tDHR	ns	Figure A	5	—	—

Clock-synchronized Serial Interface Timing Characteristics**Table 99 (IOVCC=1.65V ~ 3.30V)**

Item		Symbol	Unit	Timign Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (receive)	tSCYC	ns	Figure B	100	—	20,000
	Read (transmit)	tSCYC	ns	Figure B	350	—	20,000
Serial clock high-level width	Write (receive)	tSCH	ns	Figure B	40	—	—
	Read (transmit)	tSCH	ns	Figure B	150	—	—
Serial clock low-level width	Write (receive)	tSCL	ns	Figure B	40	—	—
	Read (transmit)	tSCL	ns	Figure B	150	—	—
Serial clock rise/fall time		tSCr, tSCf	ns	Figure B	—	—	20
Chip select setup time		tCSU	ns	Figure B	20	—	—
Chip select hold time		tCH	ns	Figure B	60	—	—
Serial input data setup time		tSISU	ns	Figure B	30	—	—
Serial input data hold time		tSISH	ns	Figure B	30	—	—
Serial output data delay time		tSOD	ns	Figure B	—	—	130
Serial output data hold time		tSOH	ns	Figure B	5	—	—

Reset Timing Characteristics**Table 100 (IOVCC = 1.65V ~ 3.30V)**

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Reset wait time		trW	ms	Figure C-1	1	—	—
Reset low-level width		tRES	ms	Figure C-2	1	—	—
Reset rise time		trRES	μs	Figure C-2	—	—	10

RGB Interface Timing Characteristics**Table 101 18-/ 16- bit RGB Interface (IOVCC=1.65V ~ 3.30V)**

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
VSYNC/HSYNC setup time	tSYNCS	clock	Figure D	0.5	—	1.5
ENABLE setup time	tENS	ns	Figure D	10	—	—
ENABLE hold time	tENH	ns	Figure D	20	—	—
DOTCLK low-level pulse width	PW _{DL}	ns	Figure D	40	—	—
DOTCLK high-level pulse width	PW _{DH}	ns	Figure D	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure D	100	—	—
Data setup time	tPDS	ns	Figure D	10	—	—
Data hold time	tPDH	ns	Figure D	40	—	—
DOTCLK, VSYNC and HSYNC rise/fall time	trgbr, trgbf	ns	Figure D	—	—	25

LCD Driver Output Characteristics

Table 102

Item	Symbol	Unit	Test condition	Min.	Typ	Max	Note
Source driver output delay time	tdds	μs	IOVCC=1.80V, VCC=VCI=2.80V, Ta=25°C, REV=0, BC0=0, FP0=5, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, PR*P00=PR*N00=5'h00, PR*P01=PR*N01=5'h02, PR*P02=PR*N02=5'h04, PR*P03=PR*N03=4'h8, PR*P04=PR*N04=4'hF, PR*P05=PR*N05=4'h8, PR*P06=PR*N06=5'h04, PR*P07=PR*N07=5'h02, PR*P08=PR*N08=5'h04, PIR*P0= PIR*P1= PIR*P2= PIR*P3=2'h0 PIR*N0= PIR*N1= PIR*N2= PIR*N3=2'h0 (*: 0, 1, 2) Same change from same grayscale at all-time division source output pin. Time to reach ±35mV when VCOM polarity changes. Load resistance R=10kohm, Load capacitance C=20pF	—	25	—	9
VCOM output delay time	tddv	μs	IOVCC=1.80V, VCC=VCI=2.80V, Ta=25°C, REV=0, BC0=0, FP0=5, BP0=8, VC=3'h1, BT=3'h4, VRH=5'h1D, VCM=7'h7F, VDV=5'h11, AP0=2'h3, DC00=3'h4, DC10=3'h2, SEPVCM=0 Time to reach ±35mV when voltages on V0~V63 pins change. Load resistance R=100ohm, Load capacitance C=10nF	—	25	—	10

Notes on Electrical Characteristics

1. DC/AC electrical characteristics of bare die and wafer products are guaranteed at +85°C.
2. The followings illustrate the configurations of input, I/O, and output pins.

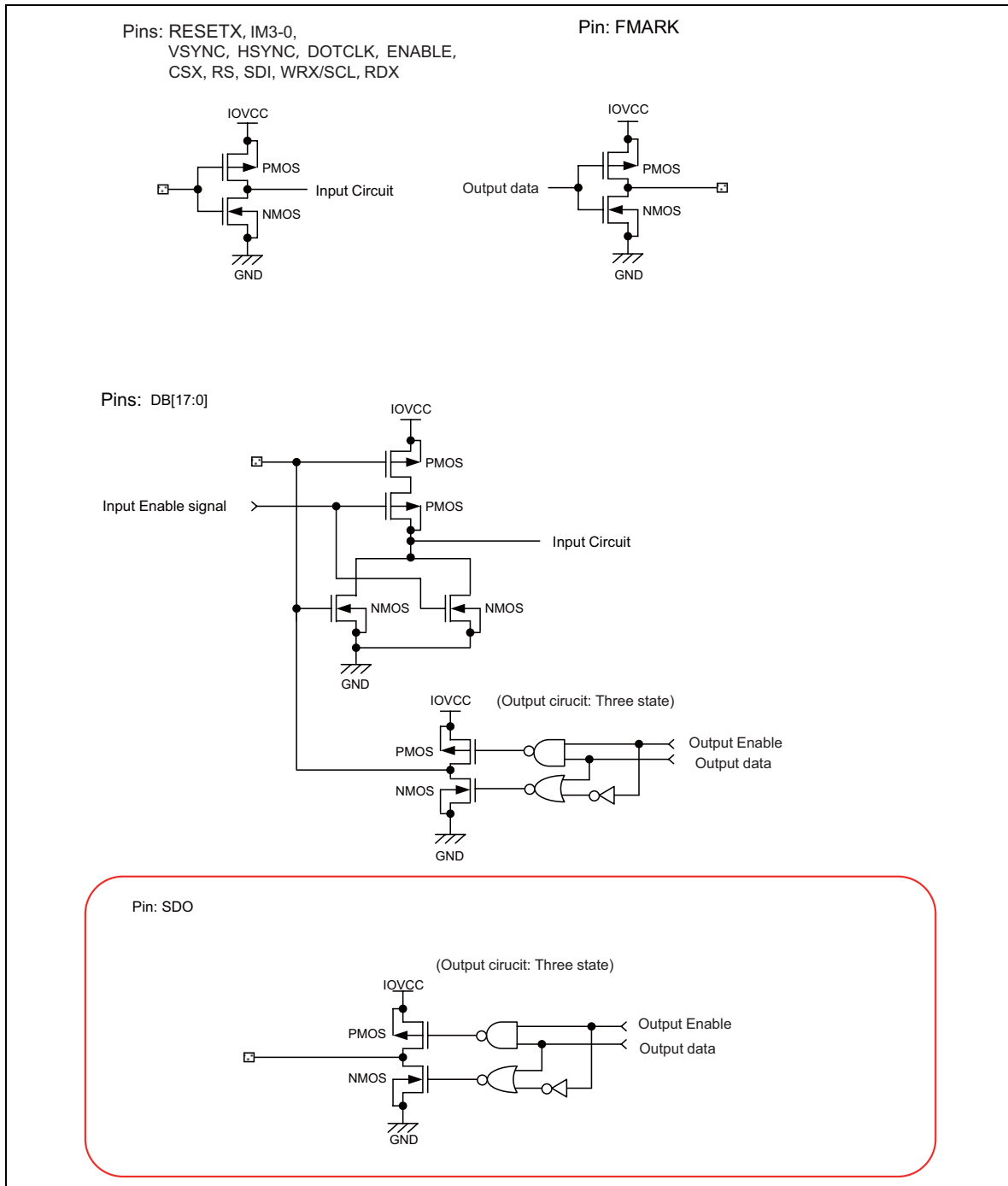


Figure 78

3. Fix pins as follows; TEST1 to TEST5 pins to GND, VDDTEST and VREFC pins to ground (AGND), and IM3/2/1/0 pins to IOVCC or ground (GND).
4. This excludes the current in the output-drive MOS.
5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CSX pin is “high” or “low” while not accessing via interface pins.
6. The output voltage deviation is the difference in the voltages between output pins that are placed side by side in same display mode.
7. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for one chip with same display data.
8. This applies to internal oscillators when using an internal oscillator.
9. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality on the actual panel in use.
10. VCOM output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line checking the quality on the actual panel in use.
11. Internal reference voltage VCIR depends on temperature as shown in following graph.

Test Circuits

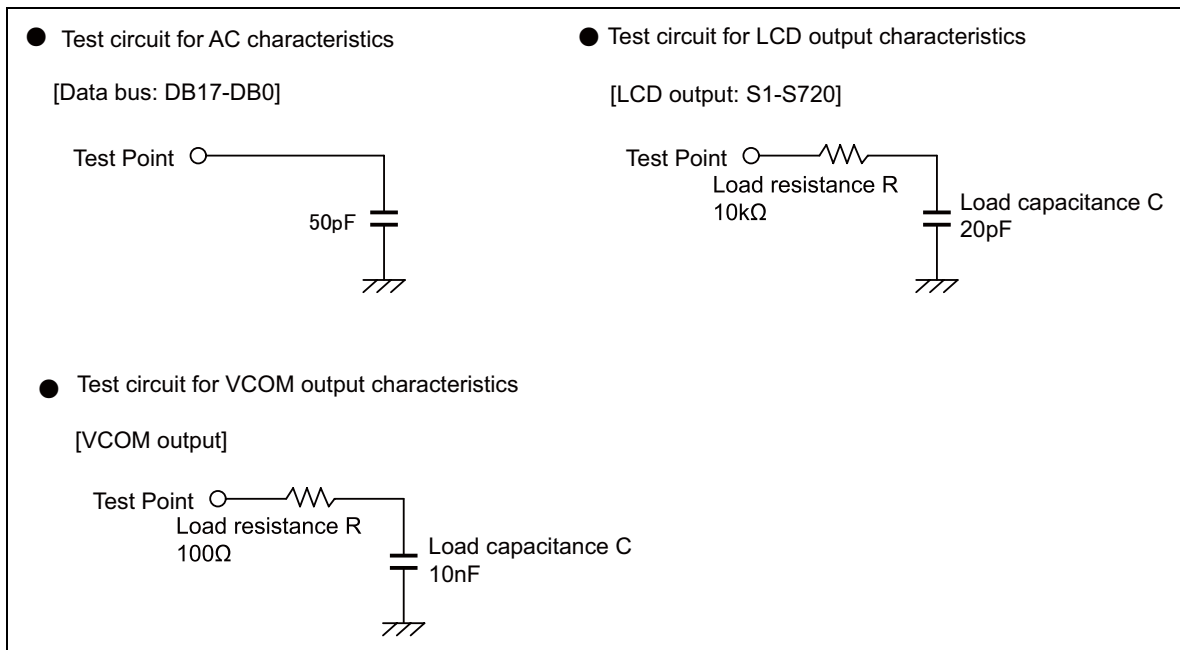


Figure 79

Timing Characteristics

80-System Bus Interface

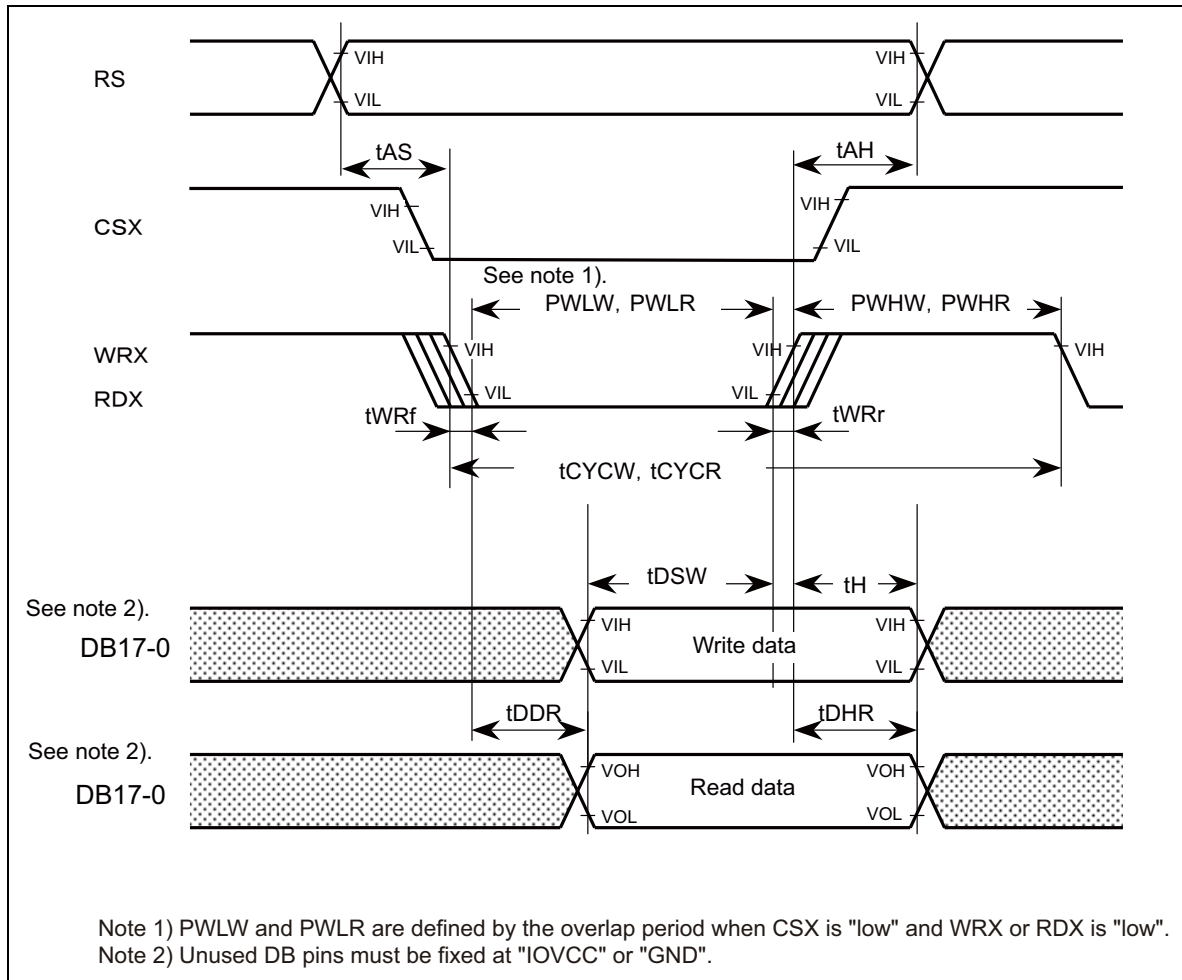


Figure A

Clock Synchronous Serial Interface

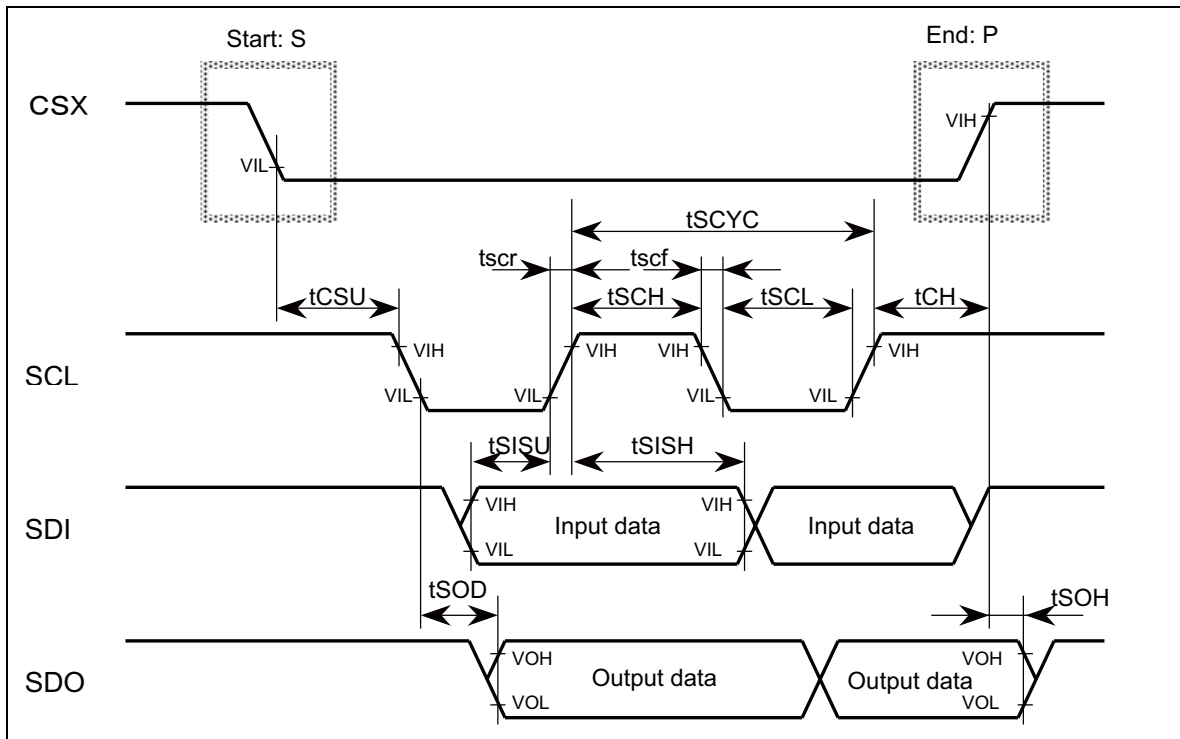


Figure B

Reset Operation

Figure C-1 Reset timing when power supply is input

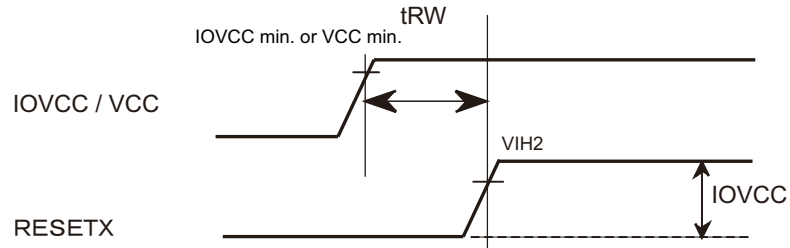


Figure C-2 Reset timing during normal operation

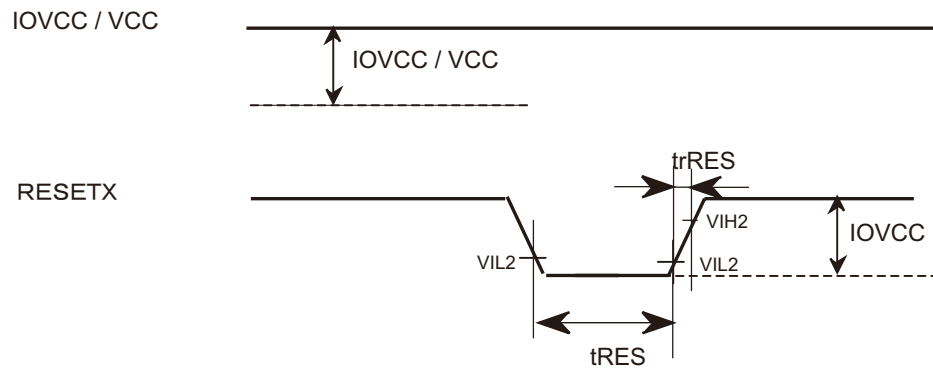
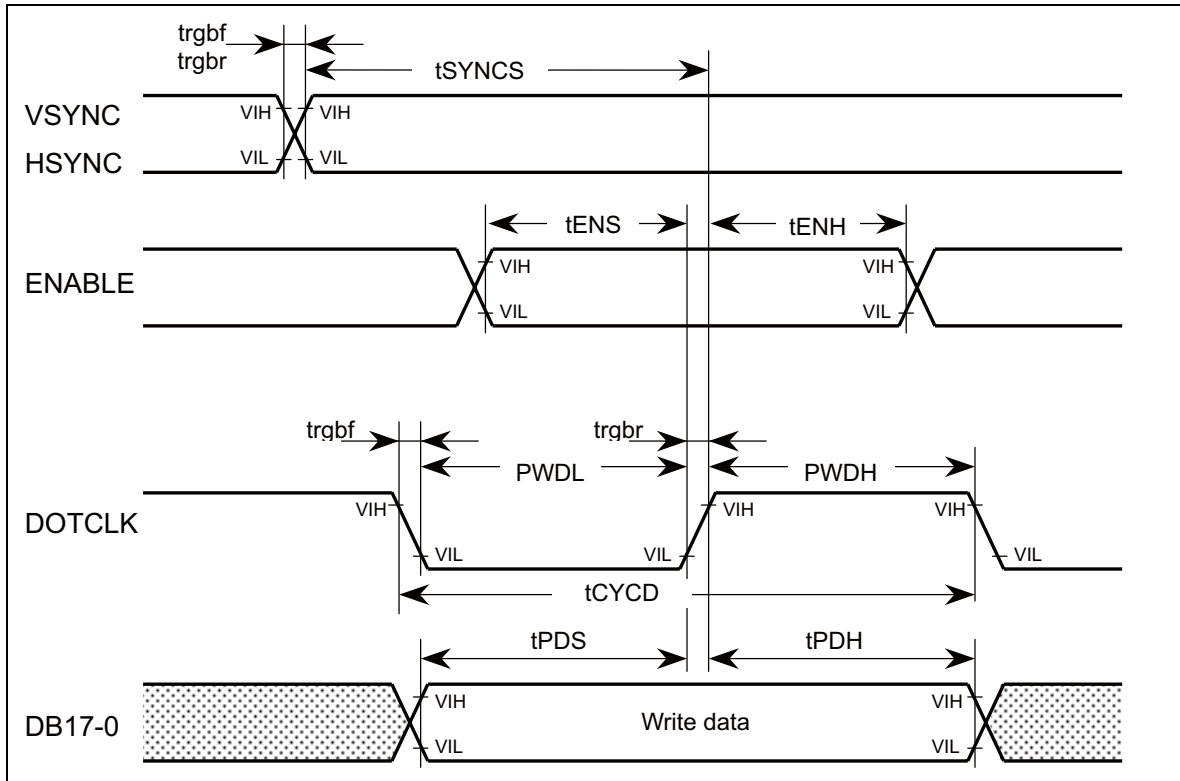
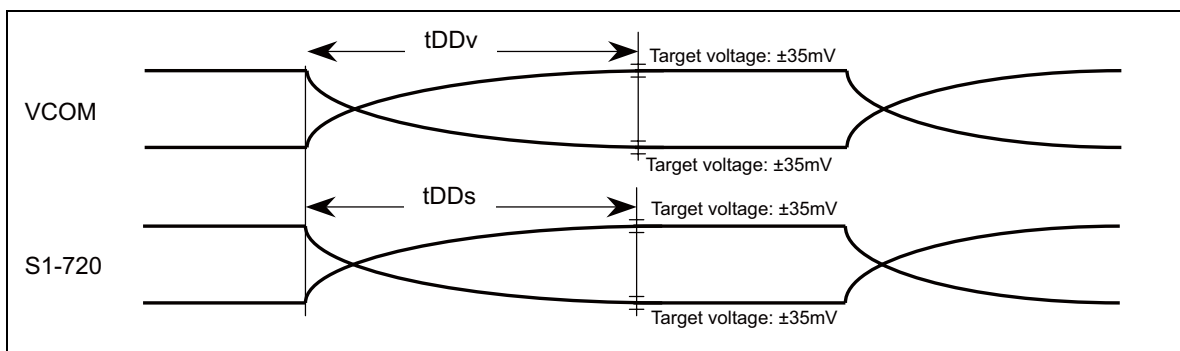


Figure C-1, C-2

RGB Interface**Figure D RGB Interface Timing****LCD Driver Output and VCOM Output****Figure E LCD Driver Output and VCOM Output**

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Revision Record

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
0.01	Sept.14, 2007		First issue		
0.02	Oct.25, 2007	All pages	RC oscillation → internal oscillation		
		6	Error correction (delete the description of high-speed RAM write function).		
		7	Source driver liquid crystal drive/VCOM power supply: DDVDH-GND, VCL-GND, VCI-VCL → DDVDH, VREG1OUT, VCL, VCI Gate drive power supply: VGH-GND, VGL-GND, VGH-VGL → VGH, VGL Internal reference voltage VCIR to generate VREG1OUT → Internal reference voltage to generate VREG1OUT Note (patent) added.		
		8	Table 1 Power supply specification VPP1, 2, 3A, 3B, 3C (Power supply for the NVM) (Write) VPP1: $9.0V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP2: $7.5V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) (Erase) VPP1: $9.0V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP2: $9.0V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP3A : $-9.0V \pm 0.1V \rightarrow -8.2 \pm 0.3V$ (TBD)		
		11-12	Table 5 (Difference between the R61505U and the R61505V's registers) added.		
		13	Figure 1 Block diagram: TEVCI2 inserted. VCI1: Input → input/output Liquid crystal drive level generating circuit → Liquid crystal drive level generating circuit (Internal step-up circuit 1, 2)		
		18	Table 9: Error correction (SDO: I/O → O).		
		20	Table 11: Error correction (VCC and IOVCC: delete "VCC ≥ IOVCC") VPP pins: description changed. Voltage table moved to "NVM Control Sequence". VPP3B and 3C pin description moved to Table 14. VPP3A when not used GND → AGND.		
		21	Table 12, VC1: Added "Define the voltage so that DDVDH, VGH and VGL do not exceed the ratings." Error correction (DDVDH, VGH, VGL, VCL: I → O).		
		22	Table 13 LCD drive pins: When not in use Open → "-"		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
			"		
		23	Table 14: VPP3B, VPP3C pins added. Pin name changed. VCI2→TEVCI2. DUMMYR description: Added "DUMMYR pins are short-circuited as below: DUMMYR1 and DUMMYR6 DUMMYR2 and DUMMYR5 DUMMYR3 and DUMMYR4"		
		24	PAD Arrangement inserted. (Rev. 0.10, 2007.09.20)		
		25	Chip size etc. inserted.		
		26-39	Pad Coordinates inserted (Rev.1.0, 2007.10.20).		
		40	Bump arrangement (Figure 3) inserted.		
		47	R02h IB10 "0"→ "1"		
		53	Error correction (FP: 2 lines → 3 lines).		
		57	R0Ch RIM bit description, Table 26: RIM[1:0]="10" "-- Setting inhibited.		
		60	R0Eh Figure 7 VEQW, VEM description: Error correction. (VEQW[1:0] → [2:0], correct the note of the table)		
		62-63	R10h SLP and SAP bits deleted. Default of AP bit changed. AP[1:0]="00" → "11"		
		63	Table 32 BT bit table Note 2: VGH-VGL= 28.0V (max.) added.		
		65	Error correction (RN* → RTN*). Note 2 to Table 34 (DC0 bit) added. Formula for Step-up circuit 1: 2(N-1) → 2N		
		66	Waveform inserted.		
		67	R12h VRH's default value changed. VRH [4:1]= "0000" → "1111"		
		79	SCN[6] deleted.		
		81	Table 46 (SCN bit) changed		
		84	Error correction (Table 50: 0 clocks → Setting inhibited).		
		85	Error correction (R93h MCPI[0]'s default: 0 → 1, 0 clocks → "Setting inhibited").		
		86	R94h SDTI[0]'s default: 0 → 1		
		87	DIVE bit description: Table 54 changed. Added "Internal clock frequency is calculated by below formula: DOTCLK / (DIVE x (PCDIVL + PCDIVH)) See also R9Ch."		
		89	R97h Note to Table 56 "1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK]." → 1 clock = (Number of		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by																																				
			data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK].																																						
		90	R98h Note to Table 58 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK].” → 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK], delete “(see note)” from 3’h4.																																						
		91	R99h Note to Table 59 DIVE (R95h) sets division ratio of clock frequency. → 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) x (PCDIVL + PCDIVH)) [DOTCLK]																																						
		92	Panel Interface Control 9 (R9Ch) inserted.																																						
		93	RA1h Table 63 Bit allocation changed.																																						
			<table><tr><td>3’h1 (MS byte)</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>3’h1 (LS byte)</td><td>1</td><td>1</td><td>1</td><td>1</td><td>ID1 [3]</td><td>ID1 [2]</td><td>ID1 [1]</td><td>ID1 [0]</td></tr></table> → <table><tr><td>3’h1 (MS byte)</td><td>1</td><td>1</td><td>1</td><td>1</td><td>ID1 [3]</td><td>ID1 [2]</td><td>ID1 [1]</td><td>ID1 [0]</td></tr><tr><td>3’h1 (LS byte)</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>	3’h1 (MS byte)	1	1	1	1	1	1	1	1	3’h1 (LS byte)	1	1	1	1	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	3’h1 (MS byte)	1	1	1	1	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	3’h1 (LS byte)	1	1	1	1	1	1	1	1		
3’h1 (MS byte)	1	1	1	1	1	1	1	1																																	
3’h1 (LS byte)	1	1	1	1	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]																																	
3’h1 (MS byte)	1	1	1	1	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]																																	
3’h1 (LS byte)	1	1	1	1	1	1	1	1																																	
		95	Instruction List inserted. (Rev 0.0 2007. 10. 12)																																						
		108	Error correction (add note).																																						
		115	VSYNC interface, RAM write speed calculation example: Error correction Back/front porch 14/2 lines (BP = 4h'E, FP = 4'h2) → 13/3 lines (BP = 8h'D, FP = 8'h3) DIV* → DIVE, RTN* → RTNE Minimum speed for RAM write [Hz] > 240 × 320 / {((14 + 320 – 2) lines × 1 × 30 clocks) × 1/642 kHz} = 4.95 MHz → Minimum speed for RAM write [Hz] > 240 × 320 / {((13 + 320 – 2) lines × 1 × 30 clocks) × 1/642 kHz} = 4.97 MHz Add the description of RTN* and DIV*.																																						
		116	Figure 31: Back porch (14 lines) → (13 lines) Front porch (2 lines) → (3 lines) BP=14H → 13H FP=2H → 3H Figure 32 Back porch (14 lines) → (13 lines) Front porch (2 lines) → (3 lines) BP=14H → 13H																																						

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
			FP=2H → 3H		
		118	Error correction (DIV* → DIVE, RTN* → RTNE), add the description of RTN* and DIV*.		
		119	<p>FMARK interface, RAM write speed calculation example: Error correction</p> <p>Back/front porch 14/2 lines (BP = 4'hE, FP = 4'h2) → 13/3 lines (BP = 8'hD, FP = 8'h3)</p> <p>Minimum speed for RAM writing [Hz] $> 240 \times 320 / \{((8+8 + 320 - 2) \text{ lines} \times 1 \times 30 \text{ clocks}) \times 1/642 \text{ kHz}\} = 4.95 \text{ MHz / pixel}$</p> <p>→ Minimum speed for RAM writing [Hz] $> 240 \times 320 / \{((13+3 + 320 - 2) \text{ lines} \times 1 \times 30 \text{ clocks}) \times 1/642 \text{ kHz}\} = 4.95 \text{ MHz / pixel}$</p>		
		120	<p>Figure 36: 280 lines → 320 lines.</p> <p>Back porch (14 lines) → (13 lines)</p> <p>Front porch (2 lines) → (3 lines)</p> <p>Main Panel Moving Picture display (320 lines) → (280 lines)</p>		
		121	<p>Figure 37: Error correction.</p> <p>FP=4'h8 → 8'h3, BP=4'h8 → 8'hD</p>		
		123	<p>Figure 38: 2H → 3H (FP)</p> <p>Error correction (delete "and high-speed write mode (HWM = 1)").</p>		
		124-125	Add the description of RGB interface timing.		
		147	Change the description of gamma correction registers.		
		156	<p>Figure 61 Voltage Setting Pattern Diagram</p> <p>VCILVL → VCI/VCILVL</p> <p>VCC / VCI → VCC</p> <p>Figure 62: Add "VGL"</p>		
		144 (Rev 0.01)	NVM Write Sequence deleted.		
		145 (Rev 0.01)	NVM Data Read Sequence deleted.		
		146 (Rev 0.01)	NVM Erase Sequence deleted.		
		147 (Rev 0.01)	Verify Sequence deleted.		
		158	Figure 63: Error correction (A2'h → 2'Ah).		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
		159	NVM Control sequence: Table 87 and description added.		
		160	Figure 64: VPP1 = VPP1: $9.0V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP2: $7.5V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) 100 ~ 20ms $\rightarrow 150ms \pm 50ms$ (TBD)		
		161	Figure 65: VPP1: $9.0V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP2: $7.5V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP3A = - $9.0V \pm 0.1V \rightarrow -8.2 \pm 0.3V$ (TBD) Erase period: 3 ~ 10ms $\rightarrow 5ms \pm 1ms$ (TBD) $9.0V \rightarrow -8.2V$		
		162	Figure 66: VPP1: $9.0V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP2: $7.5V \pm 0.1V \rightarrow 9.2 \pm 0.3V$ (TBD) VPP3A = - $9.0V \pm 0.1V \rightarrow -8.2 \pm 0.3V$ (TBD)		
		163	R61505U compatible sequence Figure 67: Power supply ON sequence SAP bit added to setting disabled register list.		
		164	R61505U compatible sequence Figure 68: Power supply OFF sequence SAP bit added to setting disabled register list. “(C) Liquid crystal power supply ON” and “Display OFF sequence” deleted.		
		165	R61505V Setting sequence Figure 69: SAP bit deleted from “instruction user setting”		
		166	R61505V Setting sequence Figure 70: Power supply OFF sequence SAP bit added to setting disabled register list. “(C) Liquid crystal power supply ON” and “Display OFF sequence” deleted.		
		154 (Rev 0.01)	Sleep mode sequence deleted.		
		165	Figure 69: Delete SAP.		
		169	Figure 73 Deep standby EXIT sequence, CSX="Low" Display OFF Sequence \rightarrow (A) Liquid crystal power supply OFF (DCDC OFF) state, Display OFF state		
		170	Figure 74 Deep standby EXIT sequence, CSX="Low" and WRX="Low", 18-/16-bit interface Display OFF Sequence \rightarrow (A) Liquid crystal power supply OFF (DCDC OFF) state, Display OFF state		
		171	Figure 75 Deep standby EXIT sequence, CSX="Low" and WRX="Low", 9-/8-bit interface Display OFF Sequence \rightarrow (A) Liquid crystal power supply OFF (DCDC OFF) state, Display OFF state, FFh \rightarrow F0h.		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by															
		173	Table 88 Absolute Maximum Ratings: NVM Erase Temperature added.																	
		174	Table 89 DC Characteristics 1 Add “(See note)”. VIH → VIH1, VIH2 VIL → VIL1, VIL2 IRAM1 : tCYCW=70ns → tCYCW=125ns Typ. 7.2 → 2.0																	
		175	Table 89 DC Characteristics 1 (Continued) Ici1, Ici2: gamma registers’ setting added.																	
		176	Table 90 DC Characteristics 2 (Step-Up Circuit Characteristics): DDVDH, VGH, VGL, VCL DC0=3’h5 → 3’h4 Min, Typ and Max values changed.																	
		177	Table 91 and 92 inserted. (Table 91 NVM Control, Table 92 Power supply voltage range for NVM Control (TBD))																	
		178	Add “(See note)”.																	
		180	Table 98 Reset Timing Characteristics Reset wait time added.																	
		181	Table 99 18-/ 16- bit RGB Interface Timing Characteristics tSYNCS, Min 0 → 0.5 tSYNCS, Max 1 → 1.5																	
		182	Figure 78: Pin names changed.																	
		187	Reset operation: Figure C changed.																	
0.10	Feb. 15, 2008	All pages	Error correction. (Pin name changed. IM0/ID → IM0)																	
		8	Power Supply Specification Table 1 TBD deleted. VPP3A : -8.2±0.3V → -9.2±0.3V																	
		10	Table 2 Serial interface added.																	
		13	Figure 1 Block Diagram Error correction. (IM3-1, IM0/ID → IM3-0)																	
		15	Block Function Table 8 (IM)																	
			<table><tr><td>0</td><td>1</td><td>0</td><td>*</td><td>Clock synchronous serial interface</td></tr></table> ↓ <table><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Clock synchronous serial interface</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td></tr></table>	0	1	0	*	Clock synchronous serial interface	0	1	0	0	Clock synchronous serial interface	0	1	0	1	Setting disabled		
0	1	0	*	Clock synchronous serial interface																
0	1	0	0	Clock synchronous serial interface																
0	1	0	1	Setting disabled																
		18	Pin Function Table 9 Interface																	

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
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0	1	0	*(ID)	Clock synchronous serial interface
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↓

0	1	0	0	Clock synchronous serial interface
0	1	0	1	Setting disabled

- 24 PAD Arrangement Rev 0.10 → Rev. 0.20
- 25 Figure 2 Alignment Mark changed.
- 26~3 Pad Coordinates Rev 1.0 → Rev. 1.1
- 9
- 41 Wiring Example and Recommended Wiring Example Rev 0.00 → Rev 0.10
- 73 R29h (NVM Data Read 2) IB7 Default "0"→"1"
Error correction.
VCM1 description: "Make sure to set VCMSEL = 0"
→ "VCMSEL=1".
VCM2 description: "Make sure to set VCMSEL = 1"
→ "VCMSEL=0".
"Write the setting value in VCM2[6:0] bits and
VCMSEL = 1 " → "VCMSEL = 0" .
- 85 Panel Interface Control 1-1 (91h) inserted.
- 91 Panel Interface Control 5-1 (R96h) inserted.
- 96 NVM Control 1 (RA0h), NVM Control 2 (RA1h)
Table 65 Error correction. (3'h0 → 2'h0, ID→UID)
Bit allocation of VCM1 and VCM2 changed.
- 98 Instruction List Rev 0.0 → Rev 1.10
- 104 Table 67 IM Bit Settings and System Interface
- | | | | | |
|---|---|---|---|------------------------------------|
| 0 | 1 | 0 | * | Clock synchronous serial interface |
|---|---|---|---|------------------------------------|
- ↓
- | | | | | |
|---|---|---|---|------------------------------------|
| 0 | 1 | 0 | 0 | Clock synchronous serial interface |
| 0 | 1 | 0 | 1 | Setting inhibited |
- 114 Serial Interface description
Delete "the IM0/ID pin functions as the ID pin"
the 6-bit device identification code ("011110") → the
6-bit device identification code ("011100")
Delete "The least significant bit of the device
identification code is determined by setting the ID pin.
Send "01110" to the five upper bits of the device
identification code."

Table 68 ID → 0. Note to Table 68 deleted.
- 116 Figure 28 (a) Device ID code "01110 ID" → "011100"

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
		158	Table 87 (Schottky Diode) $V_F < 0.4 \text{ V}/20 \text{ mA}@25^\circ\text{C}$, $V_R \geq 25 \text{ V}$ $\rightarrow V_F < 0.38 \text{ V (max)}/I_F=5\text{mA} @ 25^\circ\text{C}$, $V_R \geq 25 \text{ V}$		
		161	Figure 63 Error correction. (Bit allocation of VCM1 and VCM2)		
		162	NVM Control Sequence TBD deleted. Table 89: Error correction. (NVM Read \rightarrow NVM Erase) $V_{PP3A} = -8.2\text{V} \pm 0.3\text{V} \rightarrow -9.2\text{V} \pm 0.3\text{V}$ Erase period: $5\text{ms} \pm 1\text{ms} \times n \text{ time(s)}$ $\rightarrow 10 \pm 1\text{ms} \times n \text{ time(s)}$		
		163	Figure 64 TBD deleted.		
		164	Figure 65 TBD deleted. $V_{PP3A} = -8.2\text{V} \rightarrow -9.2\text{V}$ Erase period: $5\text{ms} \pm 1\text{ms} \rightarrow 10\text{ms} \pm 1\text{ms}$		
		165	Figure 66 TBD deleted. Erase address $16'h\text{FFFF} \rightarrow R28h=000F$, $R29h=00FF$, $R2Ah=00FF$ (See $R28h \sim R2Ah$ description) $V_{PP3} V_{PP3A} = -8.2\text{V} \pm 0.3\text{V} \rightarrow -9.2\text{V} \pm 0.3\text{V}$		
		177	Electrical Characteristics Table 91 I_{OP1} Max. TBD $\rightarrow 400$		
		178	Table 91 (continued) I_{CI1} Test condition changed. Typ $2.4 \rightarrow 3.2$, Max. TBD $\rightarrow 5.0$ I_{CI2} Test condition changed.		
		177-178	Table 91: Note numbers changed.		
		180	Table 93 (NVM Control) $I_{V_{PP2W}} 30.0 \text{ (TBD)} \rightarrow 30.0$ $V_{PP3A} = -8.2\text{V} \rightarrow -9.2\text{V}$ Table 94 V_{PP3A} Min $-7.9 \rightarrow -8.9\text{V}$ Typ. $-8.2 \rightarrow -9.2\text{V}$ Max. $-8.5 \rightarrow -9.5$ Table 95 (Internal Reference Voltage) Min TBD \rightarrow " " (bar) Max TBD \rightarrow " " (bar) Note number changed.		
		183	Table 99 Error correction. ($t_{SIH} \rightarrow t_{SISH}$)		
		185	Table 102 (LCD Driver Output Characteristics): Note number changed. Test condition changed.		

Rev.	Date	Page No.	Contents of Modification	Drawn by	Approved by
		177-185	Deleted "Note: These values are target and subject to change."		
		186	Figure 78 Figure added.		
		187	Note 6 (in rev 0.02) deleted. Note 6 (Note 7 in Rev0.02): "The output voltage deviation is reference value." deleted.		