Design of a 28T Full Adder using 28 nm CMOS Technology

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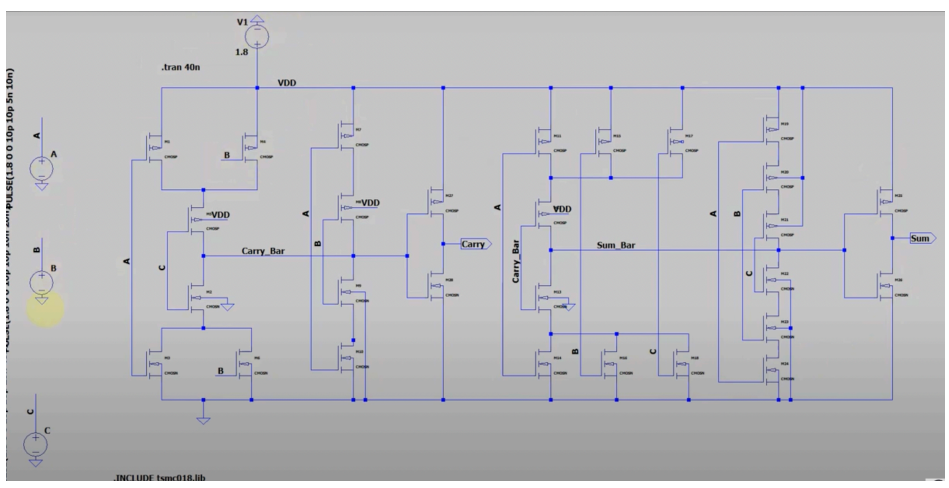
Abstract—Full adder is an essential component for the design and development of all types of processors like digital signal processors (DSP), microprocessors etc. In most of these systems adder lies in the critical path that affects the overall speed of the system.An adder is a digital circuit that performs addition of numbers and it plays an important role in today's digital world. In processors and other kinds of computing devices, Adders are used in the arithmetic logic units. They are also utilized in other parts of the processors for calculating addresses, table indices, increment and decrement operations and other similar operations because it is the basic building block of on-chip libraries. Also, it can be used for the construction of many number representations and it is a trivial to modify an adder into an adder-subtractor. Full adder reduces circuit complexity and can be integrated in the calculators for addition and subtraction operations. At DSP oriented system and at networking side full adder is used mostly. Full adders can be cascaded (e.g.: ripple carry adder) easily so that one can make a cascade to add any number of bits that form the word-width of a system.

Reference Circuit Details

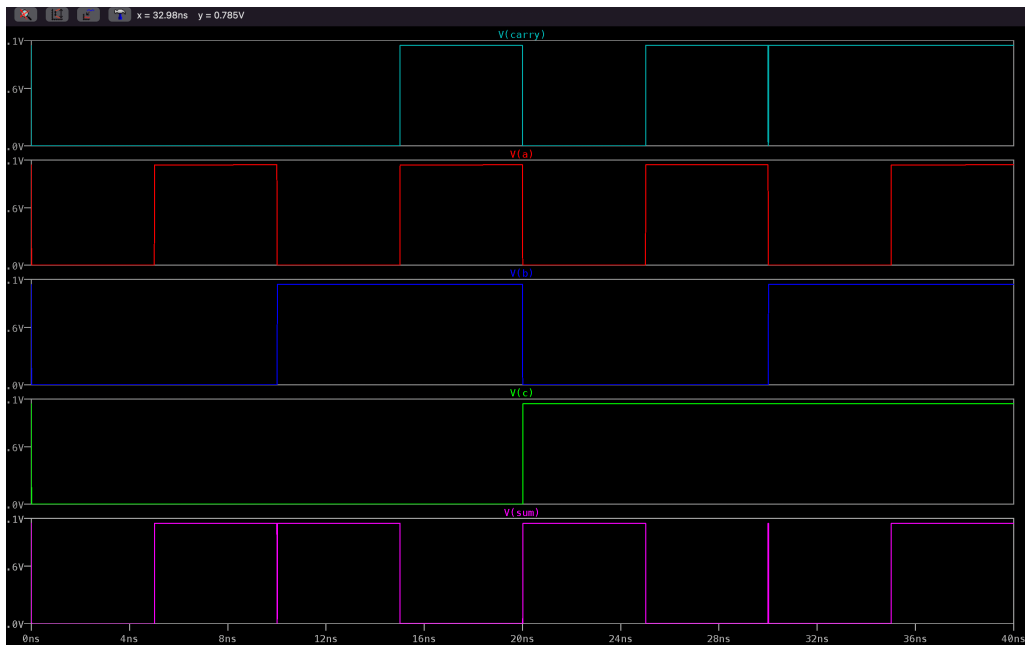
Conventional CMOS Full Adder is the most basic full adder implementation techniques. Conventional CMOS Full Adder consists of 28 transistors. A, B and Cin are the inputs and Sum & Cout are the outputs. Static logic provides robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS pass-transistor logic and reduce the number of transistors required to implement a given logic function but these suffer from static power dissipation. On the other hand, dynamic logic requires less silicon area for implementation of complex function but charge leakage and charge refreshing are required which reduces the frequency of operation. This circuit uses both NMOS and PMOS transistors. In Conventional CMOS Full Adder, there are many leakage paths which lead to more sub threshold leakage.

Reference Circuit Diagram



LTSpice Simulation

Reference Circuit Waveforms



LTSpice Simulation Waveforms

References :

1)Analysis and Performance Evaluation of 1-bit Full Adder Using Different Topologies

http://pnrsolution.org/Datacenter/Vol5/Issue1/26.pdf

2)Power and Delay Comparison in between Different types of Full Adder Circuits

https://www.ijareeie.com/upload/september/7_Power%20and%20Delay%20Comparison.pdf

3)Youtube Video - https://www.youtube.com/watch?v=AXU_J4wr_yA

IITH/SNPS/VSD - Cloud-based Analog IC Design Hackathon