RTL8211F(D)(I) UTP <=> RGMII
QFN-40 Pin Reference Schematic

REVISION HISTORY

RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic V1.0

RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic V1.01

* Change the value of C5/C6 for RTL8211FDI/FI application.

RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic V1.02

* Fix the name of the path.

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Size A	Document Number RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic	Rev 1.02
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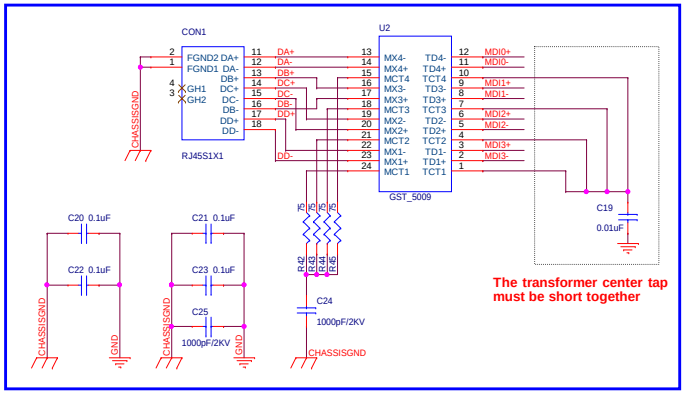
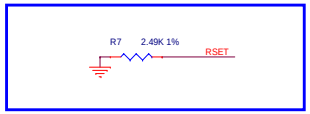
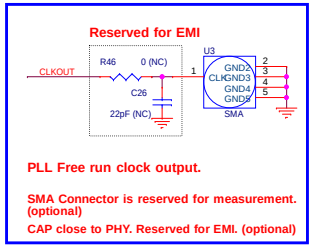
RJ45 & Transformer



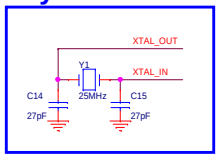
RSET



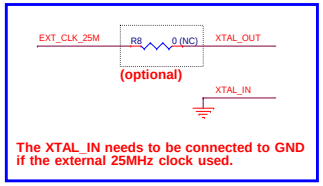
PLL Clock Out



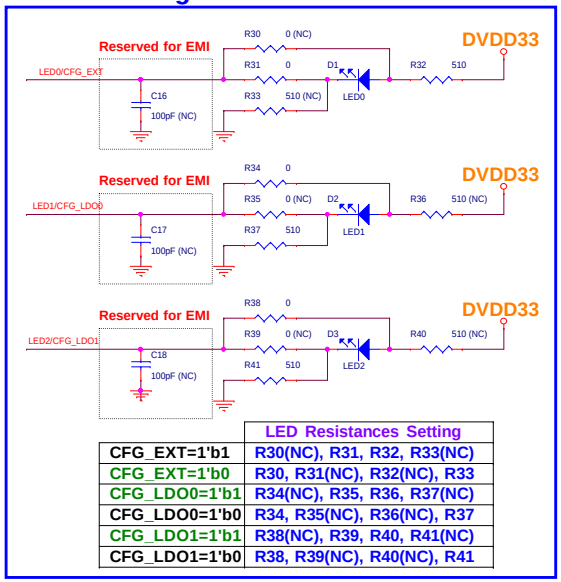
Crystal Case



External clock Case

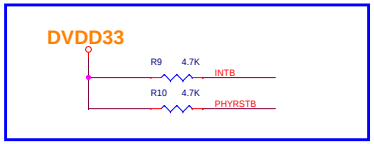


LEDs Configuration

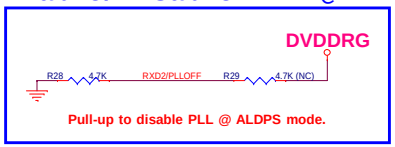


LED Resistances Setting	
CFG_EXT=1'b1	R30(NC), R31, R32, R33(NC)
CFG_EXT=1'b0	R30, R31(NC), R32(NC), R33
CFG_LDO0=1'b1	R34(NC), R35, R36, R37(NC)
CFG_LDO0=1'b0	R34, R35(NC), R36(NC), R37
CFG_LDO1=1'b1	R38(NC), R39, R40, R41(NC)
CFG_LDO1=1'b0	R38, R39(NC), R40(NC), R41

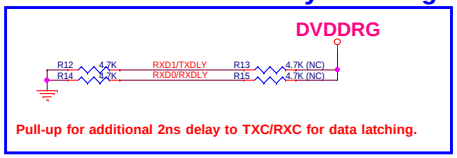
PHY RESET/INTB



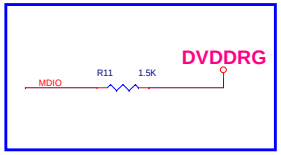
Enable/Disable PLL @ ALDPS

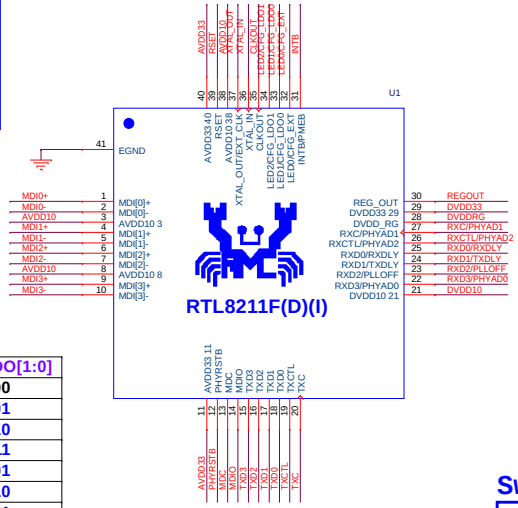


RGMII TXC/RXC Delay Config.

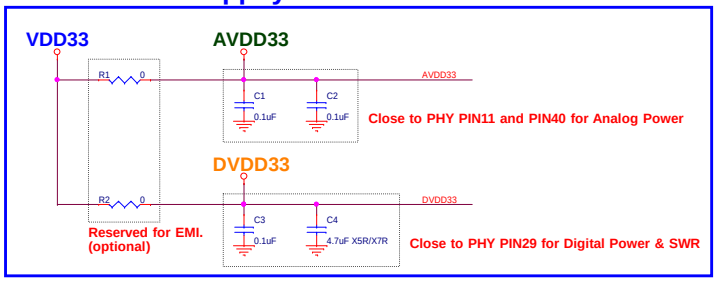


MDIO

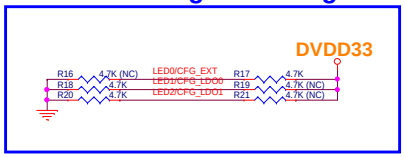




3.3V Power Supply

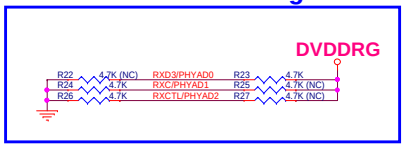


RGMII Voltage Config.



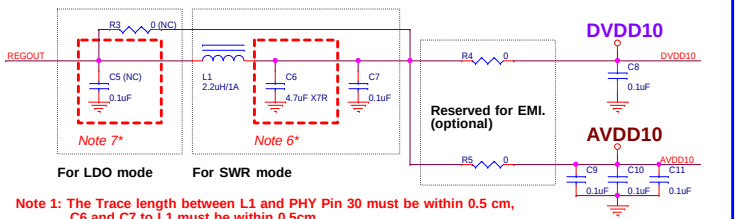
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

PHY Address Config.



PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

Switching Regulator



Note 1: The Trace length between L1 and PHY Pin 30 must be within 0.5 cm, C6 and C7 to L1 must be within 0.5cm.

Note 2: Bypass CAPs close to PHY DVDD10/AVDD10 power pins.

Note 3: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.

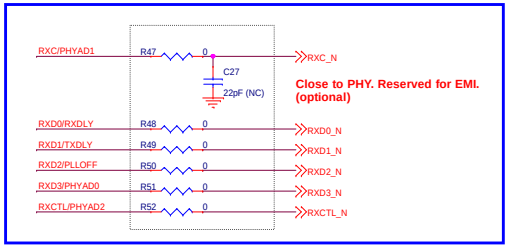
Note 4: R3 is reserved to change the DVDD10/AVDD10 supply source to LDO mode (RTL8211FD).

Note 5: No design change of PCB model is needed if R3 is reserved. If only RTL8211FD used for particular PCB model, directly short REGOUT to DVDD10/AVDD10.

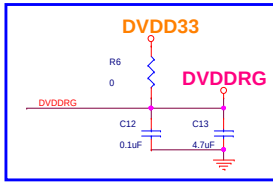
Note 6: If RTL8211FI is selected, the C6 should be replaced as 10uF X7R capacitor for industrial grade application. Please refer to the datasheet for other industrial grade information.

Note 7: If RTL8211FDI is selected, the C5 should be replaced for industrial grade application and the value is still under testing.

RGMII RX Filter Network



RGMII Power



Note 1: R6 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.

Note 2: DVDDRG must be short (or R6 be mounted) to DVDD33 if the external RGMII 3.3V is selected.

Note 3: R6 must be removed if the internal or external 2.5V/1.8V/1.5V RGMII is selected.

Note 4: CAPs must be closed to pin28 for EMI consideration.

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Title	RTL8211F(D)(I) UTP <=> RGMII QFN-40 Pin Reference Schematic: PHY	
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