DONGWHEE KIM

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SUMMARY

Circuit Design Engineer at Samsung Electronics, Hwaseong, South Korea, specializing in high-speed memory interfaces. Skilled in analyzing HBM I/O circuits and backed by a strong academic record in designing reliable and efficient memory systems, including research presented at DATE, HPCA, and SC conferences. Dedicated to advancing memory technology through innovative solutions.

- **Research Interests**: Computer Architecture, Memory Systems, RAS (Reliability, Availability, and Serviceability)

EDUCATION

Sungkyunkwan University (SKKU) **Suwon, Korea**

M.S., Semiconductor and Display Engineering *Feb. 2022 – Feb. 2024*

- Thesis: "Unity ECC: Unified Memory Protection Against Bit and Chip Errors" (Advisor: Prof. Jungrae Kim)
- *Teaching Assistant,* "Digital System Design" (Spring 2022) [SSE3016-41]

B.S., Semiconductor Systems Engineering *Mar. 2016 – Feb. 2022*

- *Teaching Assistant,* "AI Basics & Uses" (Spring 2021) [GEDT020-I1]

EMPLOYMENT

Samsung Electronics Memory Division **Hwaseong, Korea**

Circuit Design Engineer *Mar. 2024 – Present*

- HBM I/O Circuit Design
- Analyzed HBM I/O circuits to perform tasks such as signal integrity issues, interface design, and clock path design for high-speed memory interfaces.

Summer Intern *Jul. 2021 – Aug. 2021*

- DRAM Rowhammer Prevention Algorithm
- Implemented refresh algorithms against various DRAM row access patterns while minimizing read disturbance and power consumption.

SKKU Scalable Architecture Lab **Suwon, Korea**

Research Assistant, Dept. of Semiconductor and Display Engineering *Sep. 2020 – Dec. 2023*

- Reliable Memory System and DRAM Microarchitecture
- Developed reliable and efficient memory systems through research on innovative Error Correcting Codes and DRAM Microarchitecture.

PUBLICATIONS

[1] Y. Lim, **D. Kim**, and J. Kim, "SELCC: Enhancing MLC Reliability and Endurance with Single-cell Error Correction Codes," *Design, Automation & Test in Europe Conference & Exhibition (**DATE**), IEEE, 2024*.
Best Paper Award [Website] [Paper] [Slides] [Poster]

[2] J. Lee, W. Jung, **D. Kim**, D. Kim, J. Lee, and J. Kim, "Agile-DRAM: Agile Trade-Offs in Memory Capacity, Latency, and Energy for Data Centers," *The 30th IEEE International Symposium on High-Performance Computer Architecture (**HPCA**), 2024.*
[Website] [Paper] [Slides] [Poster]

[3] **D. Kim**, J. Lee, W. Jung, M. Sullivan, and J. Kim, "Unity ECC: Unified Memory Protection Against Bit and Chip Errors," *The ACM/IEEE International Conference for High Performance Computing, Networking, Storage and Analysis (**SC**), 2023.*
Best Student Paper Finalist, Invited to SAIF 2023 [Website] [Paper] [Slides] [Poster] [GitHub] [NVIDIA Research]

[4] W. Jung, **D. Kim**, and J. Kim, "Synergistic Integration: An Optimal Combination of On-Die and Rank-Level ECC for Enhanced Reliability," *The 20th International SoC Design Conference (ISOCC), IEEE, 2023.* [Website] [Paper] [Poster]

[5] Y. Lim, **D. Kim**, and J. Kim, "SCC: Efficient Error Correction Codes for MLC PCM," *The 20th International SoC Design Conference (ISOCC), IEEE, 2023.* [Website] [Paper] [Poster]
[6] K. Kwon, **D. Kim**, S. Park, and J. Kim, "EPA ECC: Error-Pattern-Aligned ECC for HBM2E," *International Technical Conference on Circuits/Systems, Computers, and Communications (ITC-CSCC), IEEE, 2023.* [Website] [Paper] [Slides]
[7] **D. Kim***, Y. Lim*, S. Han, and J. Kim, "DNN Retraining Method Reducing Accuracy Degradation in Packet-Lossy Environments," *Journal of Korean Institute of Information Scientists and Engineers (KIISE), Vol. 50, No. 3, 2023.* [Website] [Paper] (* equal contributions)
[8] **D. Kim** and J. Kim, "YOCO: Unified and Efficient Memory Protection for High Bandwidth Memory," *The 19th International SoC Design Conference (ISOCC), IEEE, 2022.* [Website] [Paper] [Slides]

AWARDS & HONORS

Awards

DATE 2024 Best Paper Award [Link] — *Mar. 2024*
SC 2023 Best Student Paper Nomination [Link] — *Nov. 2023*
Fall 2023 CICE Superior Research Award (Second Place) [Link] — Sep. 2023 - *Feb. 2024*

Invited Presentation

Samsung AI Forum (SAIF) – Presented a poster on outstanding research in Computer Engineering. — *Nov. 2023*

Scholarships

Samsung Electronics Industry-Academia Scholarship ***(full tuition & stipend)*** — *Mar. 2020 – Feb. 2024*
Undergraduate Research Program TA Scholarship — *Apr. 2023, Aug. 2023*
Director's Recommendation Scholarship — *Nov. 2021*
Undergraduate Research Program Student Success Scholarship — *May 2021*
Merit-based Semiconductor Education Scholarship — *Aug. 2019*
Samsung Semiconductor Scholarship ***(full tuition, 8 semesters)*** — *Mar. 2016 – Feb. 2022*

PATENTS

[1] J. Kim and **D. Kim**, "Method and Apparatus for Generating Code for Single Symbol Error Correction and Double Error Correction," KR Patent 10-2656075, 2024. [Website] [Patent]
[2] J. Kim and **D. Kim**, "Code Generation Method, Error Correction Code Generation Apparatus, and Storage Medium Storing Instructions to Perform Code Generation Method," US Patent 18,506,336, 2023 (Pending).

EDUCATIONAL RESOURCE

ECC-ExerSim (Error-Correcting Code Exercise and Simulator) [GitHub] — *Sep. 2023*

- Korea Copyright Commission, No. C-2023-043210
- Study the fundamentals of Error Correcting Codes through practical experimentation and develop experimental methodologies to evaluate the reliability of memory systems based on these principles.

PROFICIENCY IN SKILLS

Languages: C/C++, Python, Verilog, System Verilog
Technologies: TensorFlow, PyTorch, LaTex
Standards: DDR, HBM
Tools: Vivado, VCS (GitHub), Verdi

LEADERSHIP EXPERIENCE

Military Service — **Seoul, Korea**

Honorary Discharge as a Sergeant, Auxiliary Police 112 Strike Force — *Apr. 2017 – Dec. 2018*

- Received the Commendation from the Commissioner of the Seoul Metropolitan Police Agency. — *Oct. 2017*