SELCC: Enhancing MLC Reliability and Endurance with Single-cell Error Correction Codes

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Abstract

Conventional DRAM's limitations in volatility, high static power consumption, and scalability have led to the exploration of alternative technologies such as Phase Change Memory (PCM) and Resistive RAM (ReRAM). Storage-Class Memory (SCM) emerges as a target application for these emerging technologies, offering non-volatility and higher capacity through Multi-Level Cells (MLCs). However, MLCs face issues of reliability and reduced endurance. To address this, our paper introduces a novel Error Correction Codes (ECC) method, "Single Eight-Level Cell Correcting" (SELCC) ECC. This technique efficiently corrects single-cell errors in 8-level cell memories using existing ECC syndromes without added redundancy. SELCC enhances memory reliability and improves 8LC memory endurance by 3.2 times, surpassing previous solutions without significant overheads.

Proposed Method

▪ Error Patterns in MLC Memory

In MLC PCM memory, resistance drifts due to structural relaxation and wear-outs from phase transitions are the primary causes of errors. Resistance drift, associated with Gray coding, gradually increases a cell's resistance, potentially causing a single-bit error by shifting the cell to a higher resistance level. On the other hand, wear-outs, resulting from the mechanical stress of repeated heating and cooling during phase transitions, weaken the cell's structural integrity and eventually lead to its disconnection from the electrode. This results in the cell's resistance jumping to the maximum level, inducing errors of potentially unlimited magnitude. To enhance the reliability and endurance of MLC PCM, addressing single-cell errors is crucial, as these errors are confined to the boundaries of the individual cell.

Fig.1 shows the 7 possible single-cell error patterns in 8LC memory.

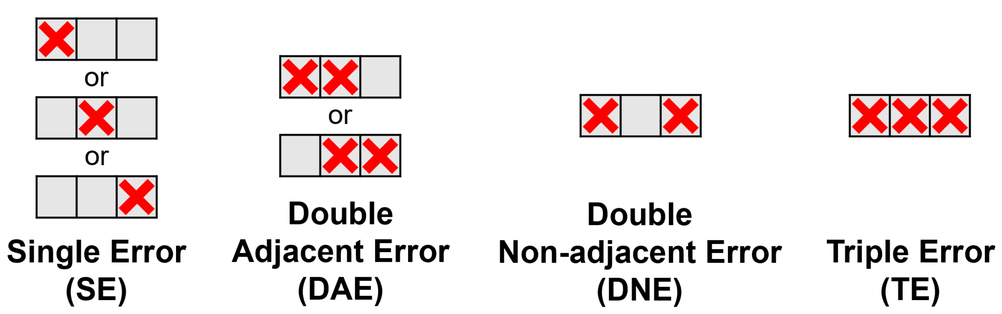

Fig.1) Single-cell Error Patterns in 8LC Memory.

▪ Single-cell Error Correction Codes

Table 1 compares the correction capabilities of previous ECC schemes with those of SELCC, noting that SELCC is the only scheme capable of addressing all single-cell error patterns with the same number of redundancy bits.

Scheme	Possible error patterns on a single cell				Redundancy ratio
	Single error	Double-adjacent error	Double non-adjacent error	Triple adjacent error	
SEC-DED	O	X	X	X	12.5%
SEC-DAEC	O	O	X	X	12.5%
SEC-DAEC-TAEC	O	O	X	O	12.5%
IP-DAEC	X	O	O	O	12.5%
SELCC (proposed)	O	O	O	O	12.5%

Table 1) Comparison of ECC schemes in correcting single 8LC error patterns.

SELCC achieves single-cell error correction by leveraging unused syndromes in conventional SEC-DED codes, which use only 72 out of the possible 255 nonzero syndromes to correct all single errors across a 72-bit codeword span. However, SELCC focuses on errors that do not cross cell boundaries, efficiently mapping 168 distinct error patterns (24 8LC cells in a 72-bit word * 7 single-cell error patterns) onto unique syndromes. This method significantly enhances the reliability and efficiency of error correction without exceeding redundancy constraints. The SELCC H-matrix required for this purpose must satisfy the following conditions.

① Every column must be nonzero.
② Each column must be unique.
③ The sum of two or three columns within any cell boundaries must be nonzero and unique.

Results

▪ Reliability Improvements

Table 2 compares the error correction capabilities of various schemes against single-cell errors. All schemes, except IP-DAEC, can fully correct single errors, with IP-DAEC achieving a 2/3 correction rate. While the SEC-DED scheme cannot correct double errors, both SEC-DAEC and SEC-DAEC-TAEC correct 2/3 of double errors, excluding non-adjacent cases, whereas IP-DAEC shows a 100% correction capability. Only SEC-DAEC-TAEC and IP-DAEC can handle triple errors, with SELCC standing out by correcting any single-cell error using the same redundancy ratio.

Error scenario	SEC-DED	SEC-DAEC	SEC-DAEC-TAEC	IP-DAEC	SELCC (proposed)
Single error	100%(0%)			67.97% (0%)	100%(0%)
Double error	0%(0%)	66.69% (16.69%)	66.63% (29.21%)	100%(0%)	100%(0%)
Triple error	0%(0%)	0% (66.62%)	100%(0%)		100%(0%)

Table 2) Comparison of ECC schemes in correction capabilities against single 8LC errors. (SDC probabilities are noted in parenthesis.)

▪ Endurance Improvements

By setting the COV at 20% and aiming for an operational reliability where 99.99% of 72-bit words are free from defective cells, SELCC achieves a significant 3.2× increase in endurance.

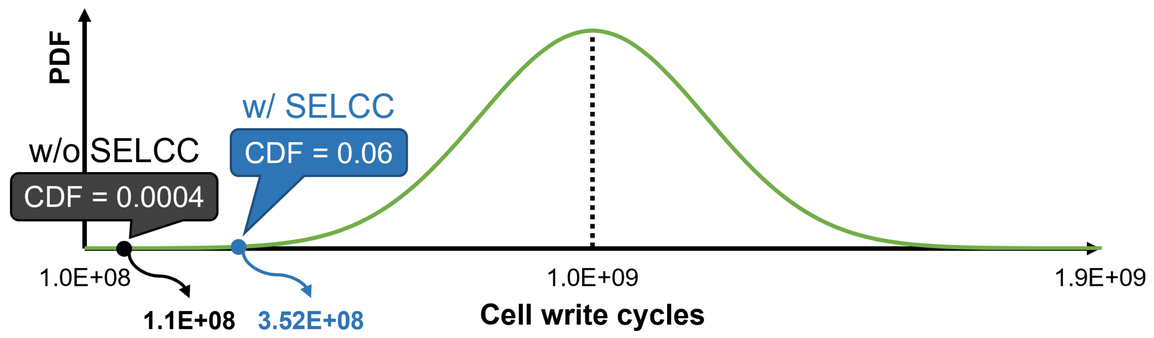

Fig.2) Probability density function of cell write cycles.

▪ Hardware Overheads

Despite its superior correction capability, SELCC incurs hardware overheads comparable to existing ECCs. It exhibits a modest 0.09ns increase in latency at 1.5GHz, suggesting that future process technologies could further reduce this. The area requirement slightly rises due to additional comparators but remains negligible relative to processor die sizes. Although power consumption is higher than that of SEC-DED, it is minimal in the context of the overall power usage of modern processors.

Conclusion

We introduced a novel ECC, termed SELCC, tailored to enhance the reliability and longevity of 8LC SCMs. While MLC memories bring forth the benefits of non-volatility and higher capacity, their integration as SCMs raises concerns about reliability and endurance due to inevitable resistance drifts and cell wear-outs. Prior ECC solutions with similar overheads fell short of addressing all single-cell errors, mandating a separate mechanism to enhance SCM lifetimes. SELCC significantly improves both reliability and endurance (by 3.2 times) by correcting all single-cell errors. This enhancement is achieved without the need for additional redundancy.

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