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Synergistic Integration: An Optimal Combination of On-Die and Rank-Level ECC for Enhanced Reliability

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ABSTRACT

Memory reliability is especially key to attaining resilience at scale, where effective error detection and correctionare essential for ensuring data integrity and preventing system failures. Technologies such as On-Die Error Correction Code (OD-ECC) and Rank-Level ECC (RL-ECC) have evolved independently, mitigating various errors and enhancing reliability. However, investigating an optimal combination between OD-ECC and RL-ECC could lead to further improvements. In particular, the optimal scheme and mapping between OD-ECC with Bounded Fault (BF) applied and RL-ECC in DDR5 have yet to be explored. This paper investigates the importance of scheme consistency for reliability in memory sub-systems and provides guidelines for RLECC design for system companies.

INTRODUCTION

• **Problem** The use of On-die ECC, which increases the reliability of DRAM, is rather likely to cause Silent Data Corruption (SDC) from a system perspective. The use of On-die ECC, which increases the reliability of DRAM, is rather likely to cause Silent Data Corruption (SDC) from a system perspective.

METHODLOGY

• **OD-ECC** In DDR5's OD-ECC a BF design has been implemented to prevent mis-correction of multiple faults into different bounds. There are two tyupes of bounds : 16bits, 32bits.

•**RL-ECC** We base our approach on Reed-Solomon Codes with symbol sizes of 8 bits and 16 bits, considering a balance between overhead and latency.

•we divided the schemes into based on (# of DQ x BL count per symbol)

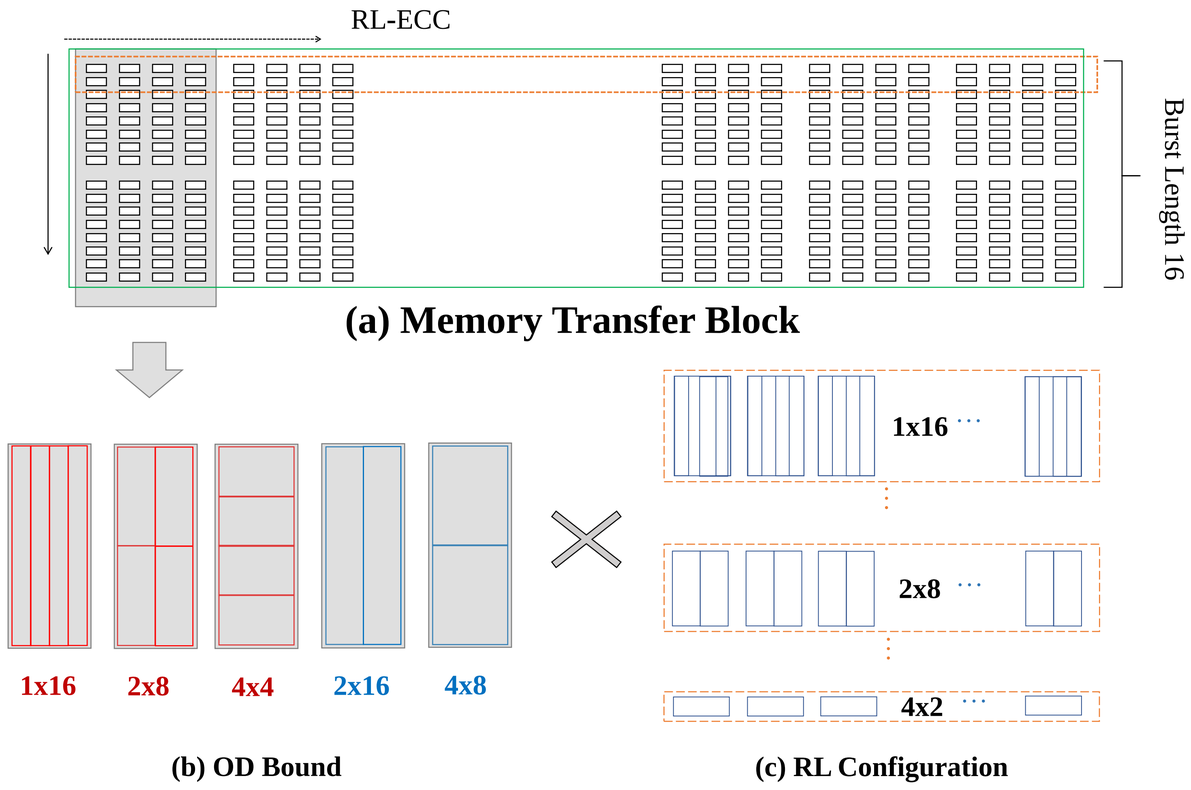

Figure 1. OD-ECC and RL-ECC combinations scheme in (b) OD-Bound Scheme in Table1. (c) Partial RL-ECC Scheme in Table2. In this paper, 30 combinations are created using the matrices in (b) and (c).

EXPERIMENTAL RESULT

• Randomly inject errors on data blocks to emulate error scenarios. Errors were generated and injected into the data blocks based on these models, with each bit within the affected region having a 50% chance of switching from correct to incorrect

• Of the 30 (OD X RL) matrices and each of the 6 error injection tests,We will focus on the representative MBBE scenario shown in Figure 2.

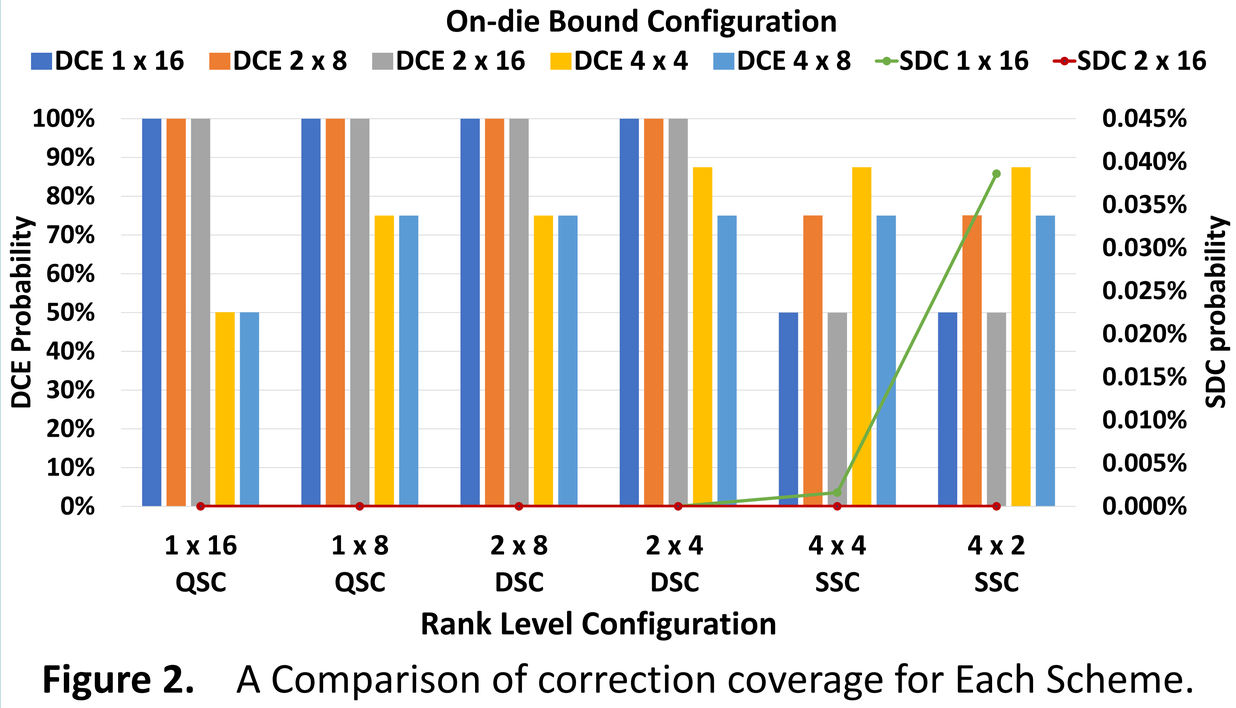

Figure 2. A Comparison of correction coverage for Each Scheme. MBBE scenarios are injected into two separate chips. Each bar represents the OD-ECC Bound.

• **Result** we have found that the scheme illustrated as an example in DDR5 (a narrow and elongated form of ODECC bound, limited to a 1DQ width) and the currently most used form of RL scheme represented by Chip-kill (wider scheme with a symbol width of 4DQs) are not the most effective options.

• **Conclusion** This observation emphasizes the strong correlation between these two aspects and conveys a message to system companies that RL-ECC design should consider the Bound shapes in DDR5.