YOCO: Unified and Efficient Memory Protection for High Bandwidth Memory

Dongwhee Kim and Jungrae Kim

Sungkyunkwan University

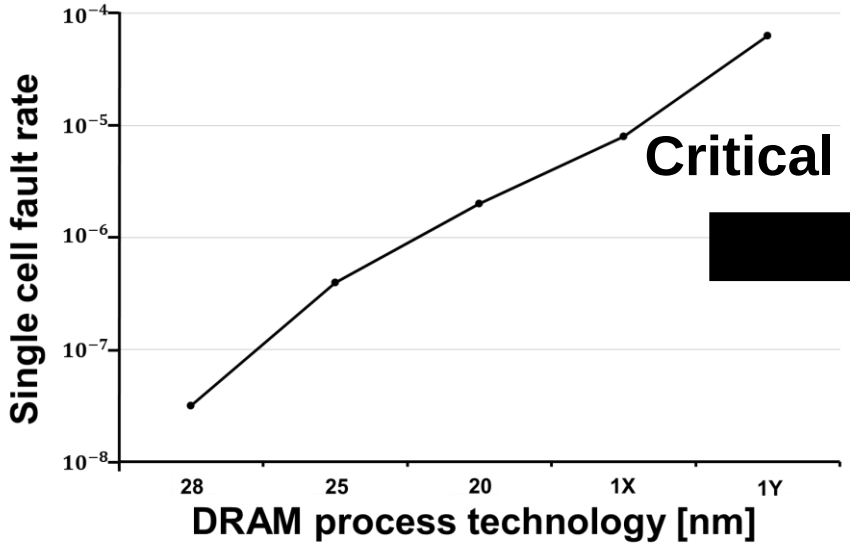
Outline

- Introduction
- Background
- Motivation
- YOCO (You Only Code Once)
- Evaluation
- Conclusion

Introduction

- **Error correction code in modern memory systems**
  - **Pros : Yield ⬆**
  - **Cons : Storage overhead ⬆ , protection cost ⬆**

Maximize yield with minimal protection overhead



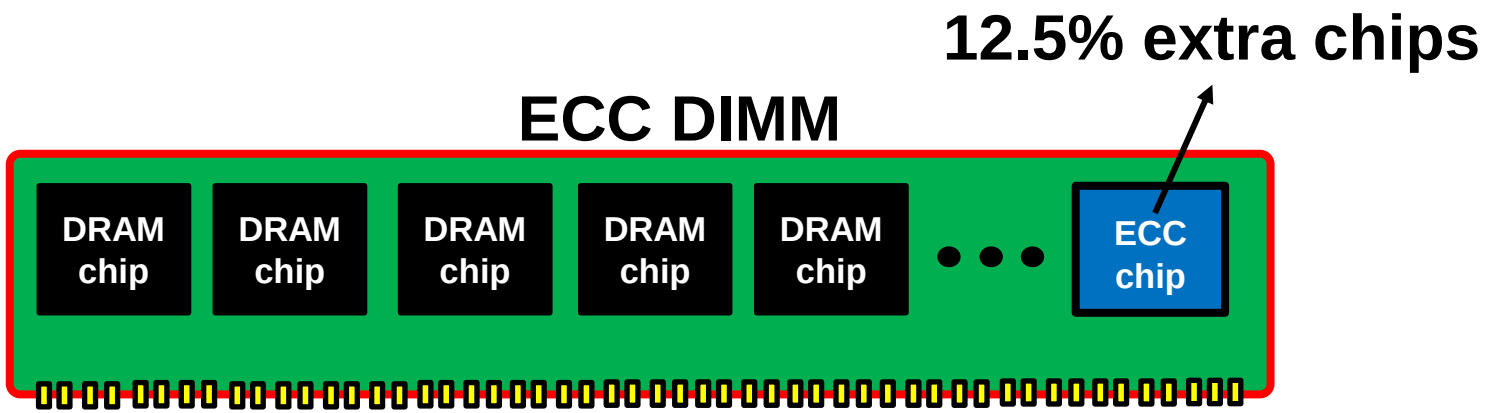
Single cell fault rate as DRAM process technology shrinks [1]

Critical Issue!

Datacenter DRAM [2]

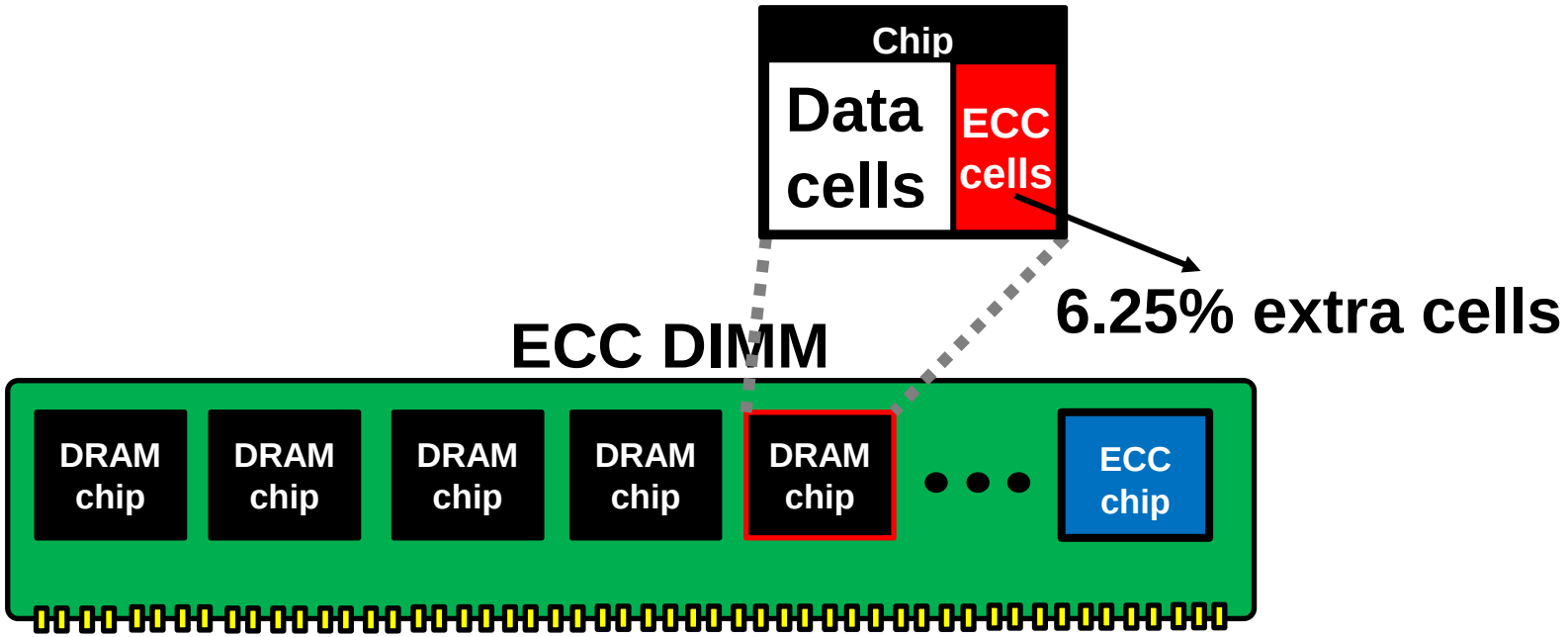
Background

- **System ECC (S-ECC)**
  - **Using extra chips**
  - **Can correct severe multi-bit errors (Reed-Solomon code)**
  - **Can prevent system from failures (System companies)**



Background

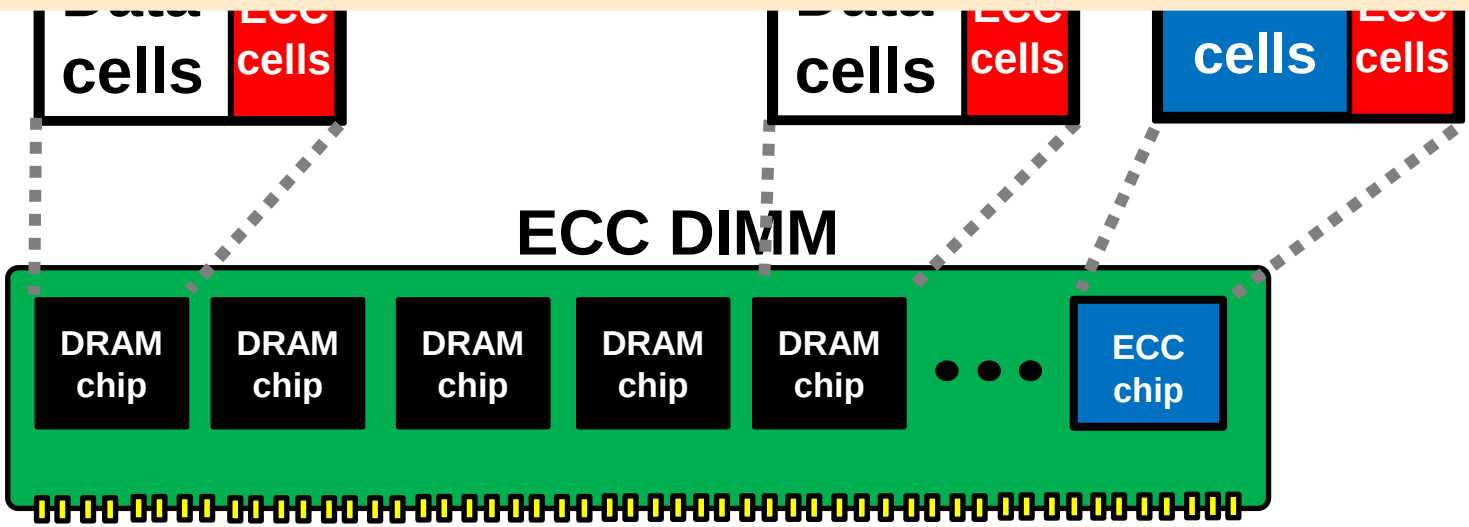
- On-die ECC (O-ECC)
  - Using extra cells within a chip
  - Can correct randomly distributed errors
  - Can hide error information (DRAM vendors)



Motivation

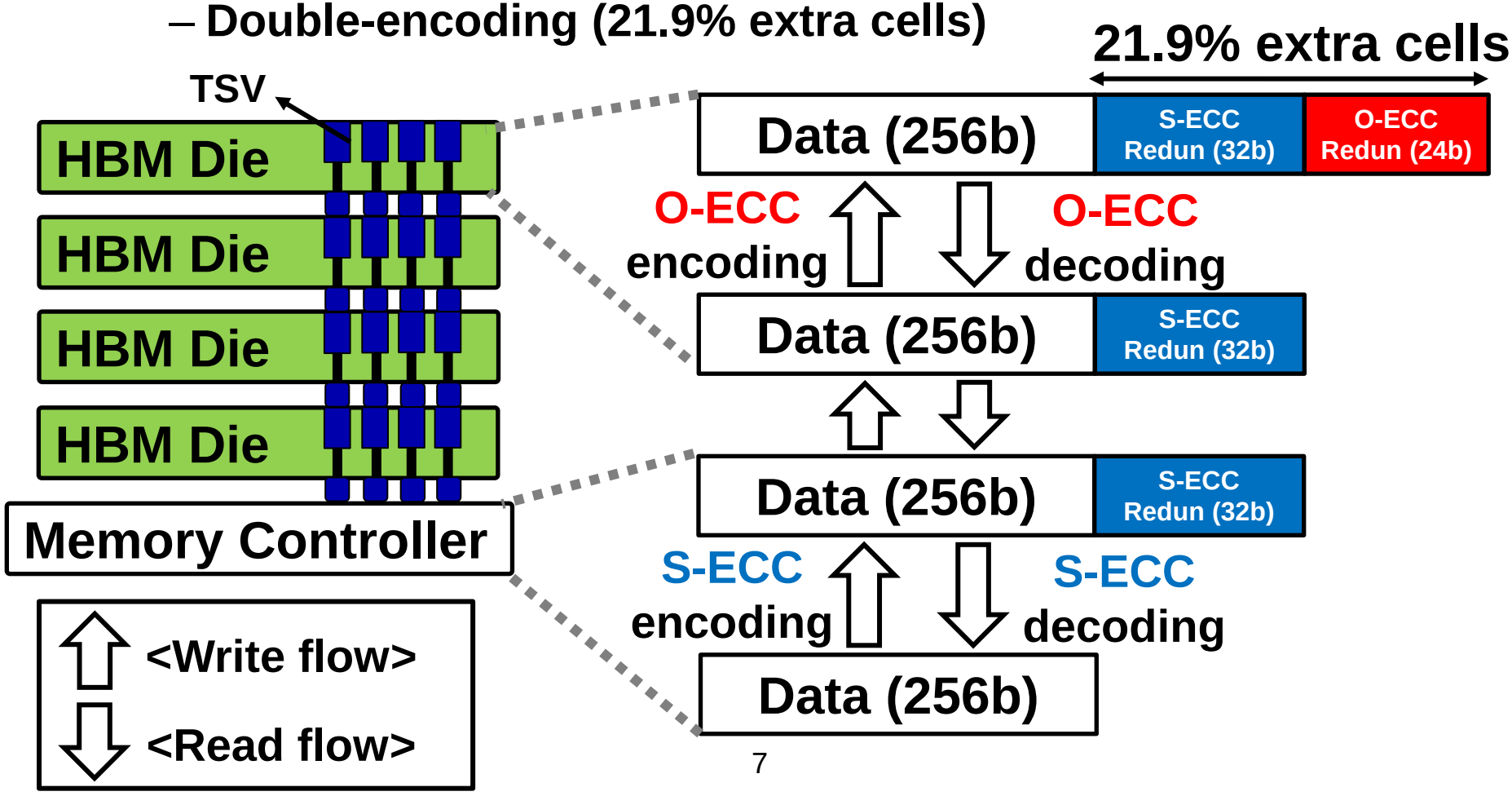
- **Combining two ECCs**
  - **Can correct severe multi-bit errors and randomly distributed errors**
  - **At high storage costs (21.9% extra cells)**

Correct both severe multi-bit errors and random bit errors using the same redundancy and single encoding



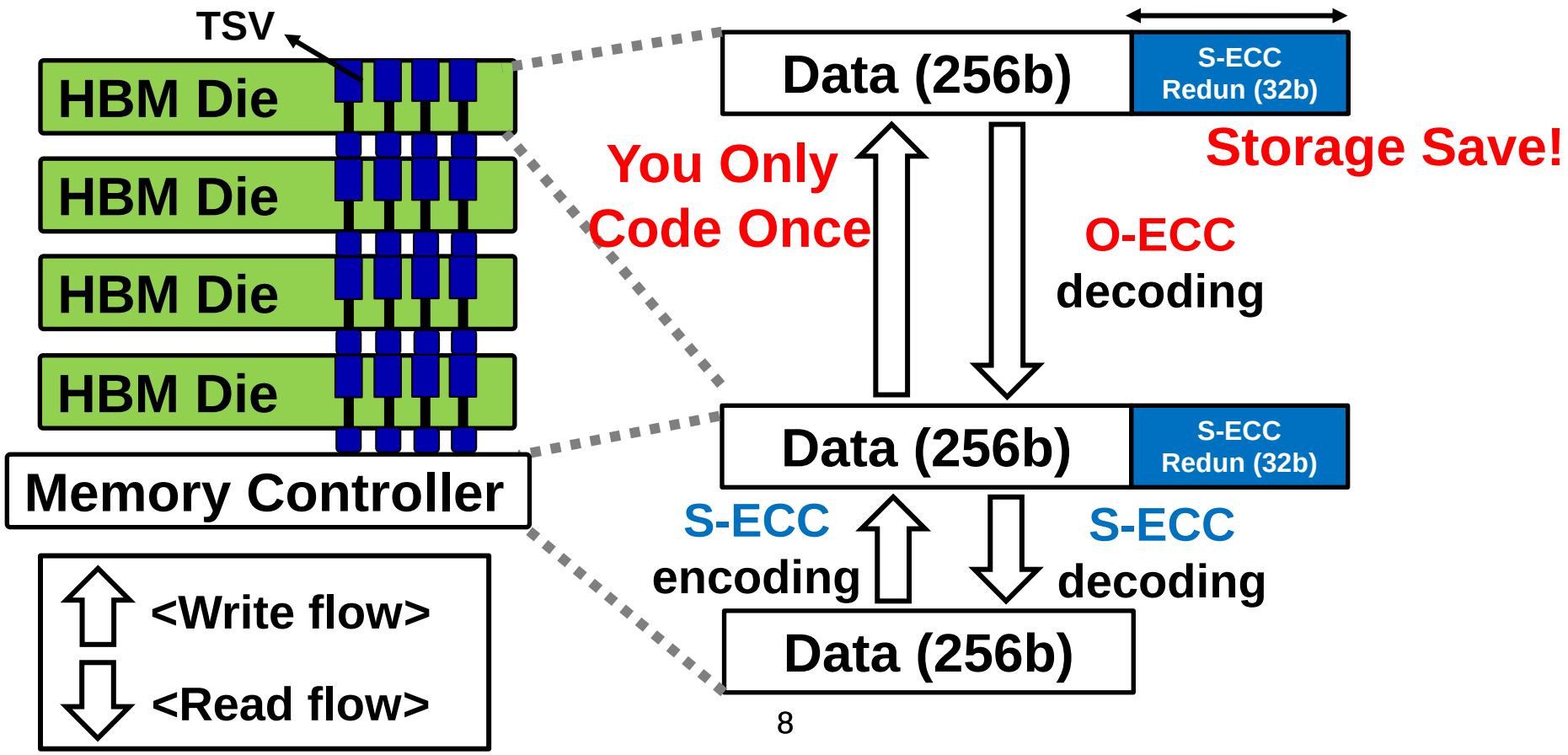
Prior Work

- HBM2E
  - Double-encoding (21.9% extra cells)



YOCO

- **Remove O-ECC redundancy**
  - **No O-ECC encoding**



YOCO

- **Encoding**
  - Single encoding in S-ECC
  - No encoding in O-ECC

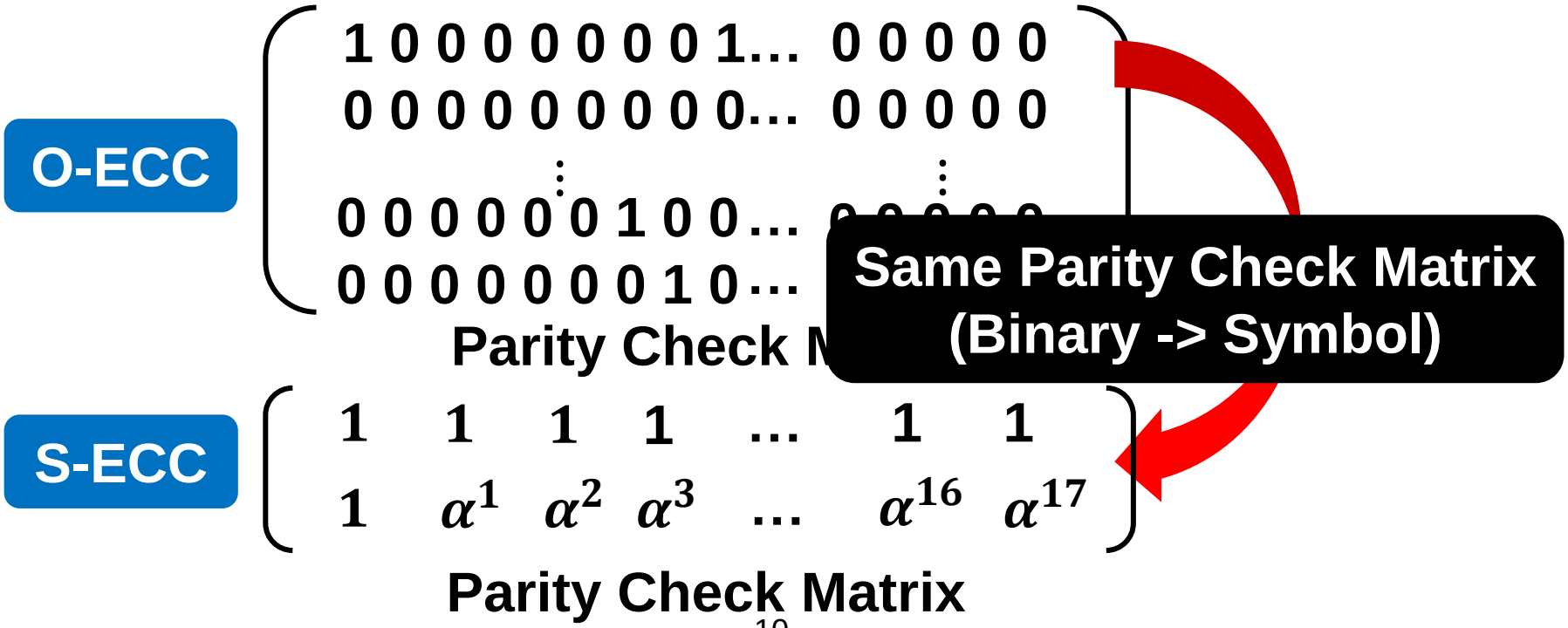
S-ECC

$$\begin{pmatrix} \alpha^{26} & \alpha^{1} & \alpha^{0} & 0 & \cdots & 0 & 0 \\ \alpha^{198} & \alpha^{25} & 0 & \alpha^{0} & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & & \vdots & \vdots \\ \alpha^{43} & \alpha^{121} & 0 & 0 & \cdots & 0 & \alpha^{0} \end{pmatrix}$$

Generator Matrix
over GF(2^8)

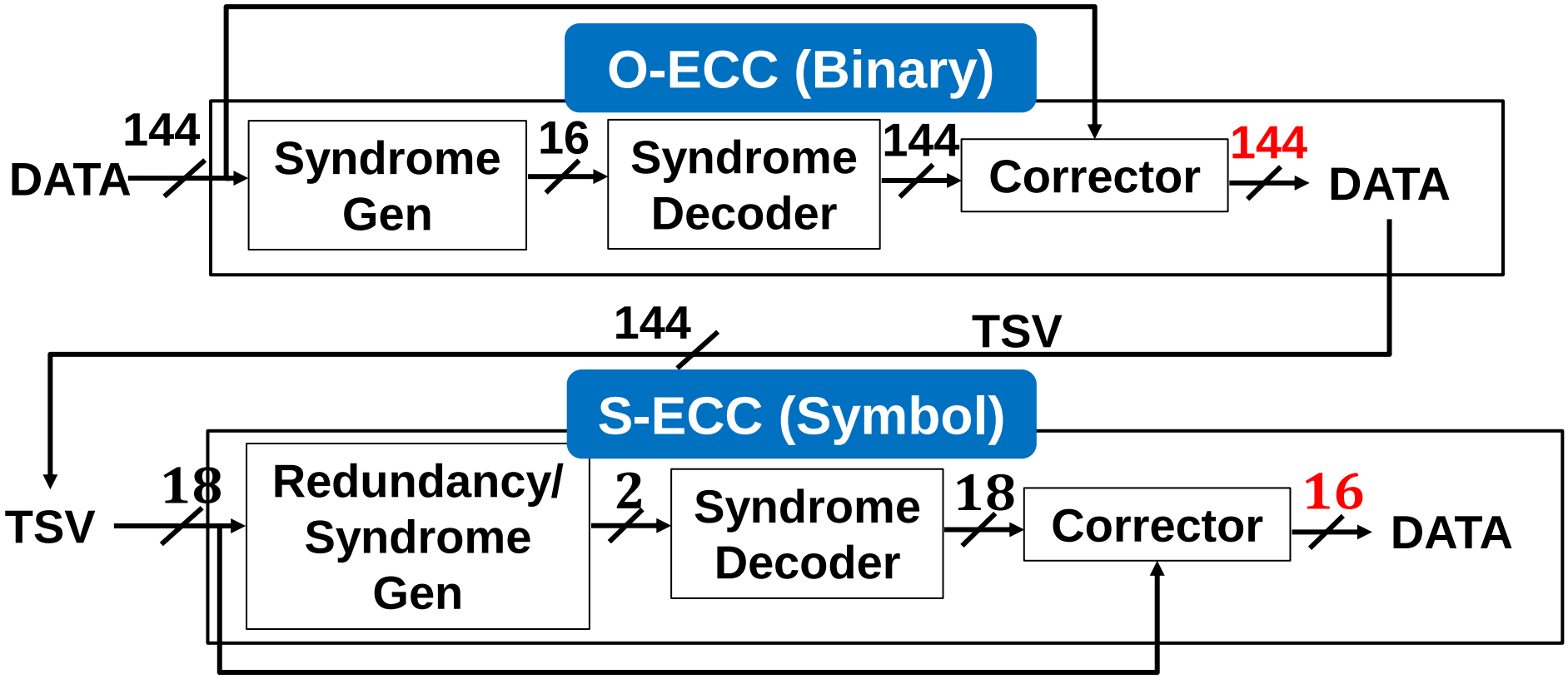
YOCO

- **Decoding**
  - **O-ECC : SEC-DED (144, 128) X 2**
  - **S-ECC : Single-Symbol Correction [18, 16] X 2**



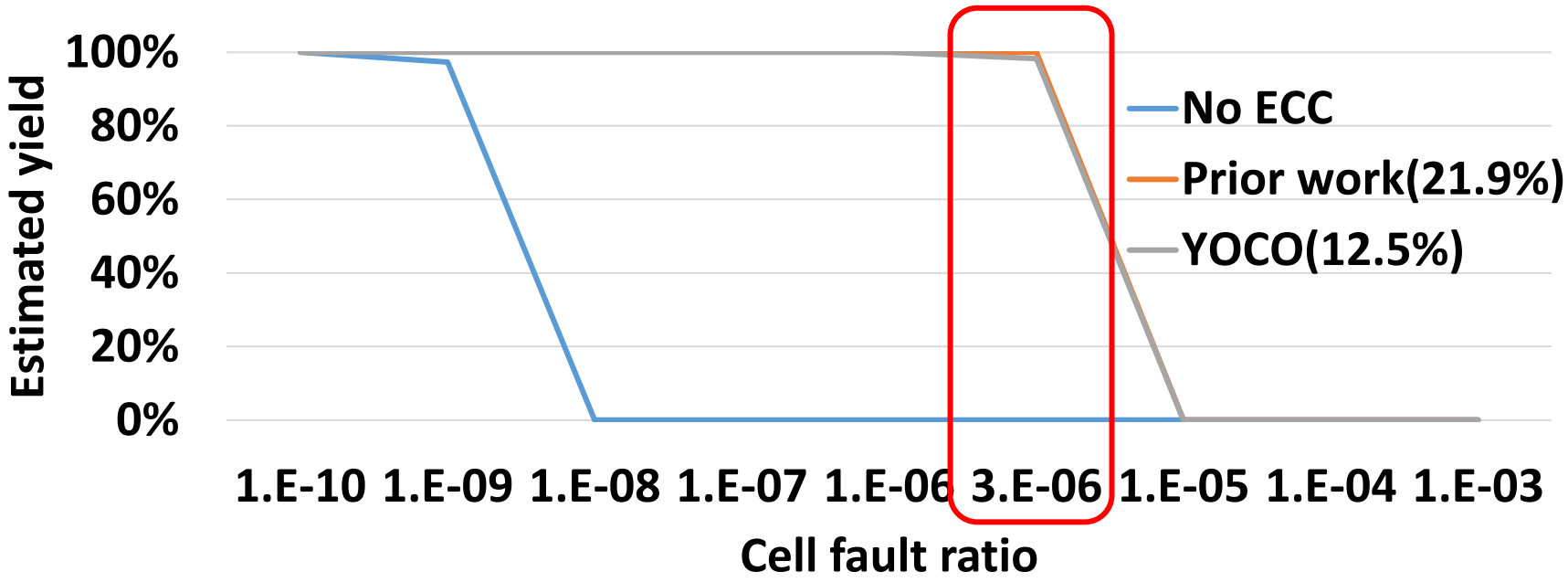
YOCO

- **Decoding**
  - **Using the same redundancy**



Evaluation

- **Comparison of estimated yield**
  - **Reduce ECC storage!**
  - **Maintain almost the same-level yield**



Conclusion

- **We propose YOCO, providing the almost same level of protection as separate S-ECC and O-ECC but reduces the redundancy by encoding only once.**

- **Reduce the overall ECC storage overhead**
  - ✓**21.9%** ➡ **12.5%**
- **No O-ECC encoding logic! (You Only Code Once)**

Thank you

Backup slides

- **Decoding**
  - No error : $S_0 = 0$ and $S_1 = 0$
  - SSC : S_0 = error value and S_1/S_0 = error location
  - SEC : $S_0 = \alpha^0 \sim \alpha^7$ and S_1/S_0 = error location
  - DED : ($S_0 \neq 0$ and $S_0 \neq \alpha^0 \sim \alpha^7$) or ($S_0 = 0$ and $S_1 \neq 0$)

$$\begin{pmatrix} 1 & 1 & 1 & 1 & \dots & 1 & 1 \\ \alpha^0 & \alpha^1 & \alpha^2 & \alpha^3 & \dots & \alpha^{16} & \alpha^{17} \end{pmatrix} \rightarrow \begin{pmatrix} S_0 \\ S_1 \end{pmatrix}$$

Parity-Check Matrix Syndromes

Reference

- [1] S. Cha et al., “Defect Analysis and Cost-effective Resilience Architecture for Future DRAM Devices,” in HPCA, 2017.
- [2] “The case for cold DRAM in the data center”, Rambus blog.last modified Oct 5. 2017, accessed Sep 8, 2022, https://www.rambus.com/blogs/the-case-for-cold-dram-in-the-data-center/