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3D SEMICONDUCTOR IC'S

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List of figure:

Abstract

Three-dimensional integrated circuits (3-D ICs) offer significant improvements over two-dimensional circuits, and promise a solution to the severe problems that are being, and will be, encountered as monolithic process geometries are reduced to below 65 nm.

1. Introduction

Silicon technologies have been grown rapidly in past 50 years following Moore's Law. This brought the prosperity of semiconductor industry. However, in recent several technology nodes it has been facing more technical challenges, design complexity and cost increases. In mean time, many 3D-IC technologies have been becoming available gradually in past several years. These 3DIC technologies provide alternative of future growth opportunities. They provide more functionality, better power performance and reduction of design cycles, by integrating different technologies (for example memory vs. logic vs. analog vs. sensors, etc.) and different functional chips, as well as allowing die partitions.

2. Moore's Law

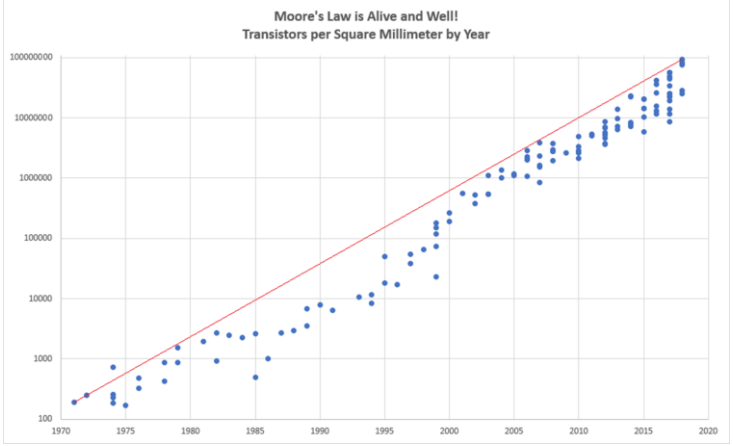

Figure 1:Transistors per Square Millimeter by Year, 1971–2018. Logarithmic scale.

Moore's Law refers to Moore's perception that the number of transistors on a microchip doubles every two years, though the cost of computers is halved. Moore's Law states that we can expect the speed and capability of our computers to increase every couple of years, and we will pay less for them. Another tenet of Moore's Law asserts that this growth is exponential.

Three-dimensional ICs are perhaps the best hope for carrying ICs further along the path of Moore's Law. In addition to obvious size benefits and possible cost be nefits, they can address issues of heterogeneous integration, power and performance, and logical span of control.

3. 3D Integrated circuit

3D Integrated circuit is a MOS (metal-oxide semiconductor) integrated circuit (IC) manufactured by stacking silicon wafers or dies and interconnecting them vertically using, for instance, through-silicon visa (TSVs) or Cu-Cu connections, 3D IC is a chip which accommodates two or more layers of active electronic components and a trend to vertically stack integrated circuits (ICs) or circuitry has emerged as a viable solution for meeting electronic device requirements such as higher performance, increased functionality, lower power consumption, and a smaller footprint. The various methods and processes used to achieve this are called **3D integration technologies**.

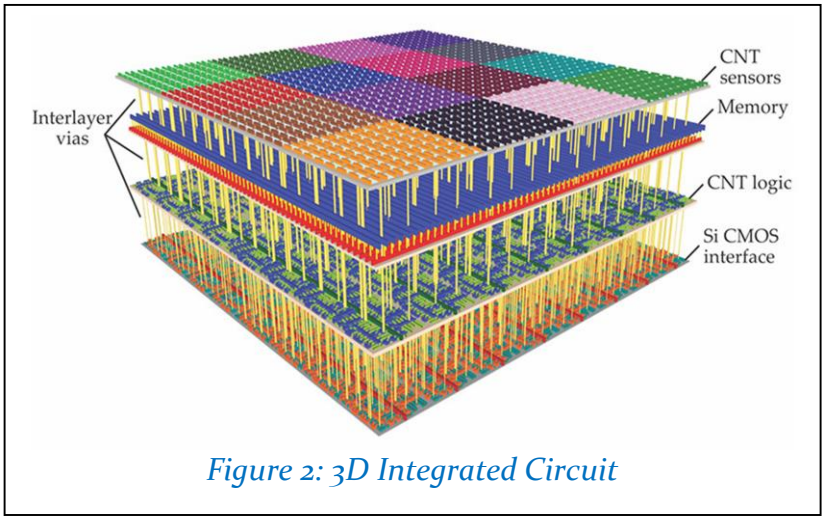

Figure 2: 3D Integrated Circuit

4. 2D, 2.D and 3D:

The 2D IC approach consists of connecting different discrete devices with their packages using a printed circuit board (mechanical support with conductive tracks).

This connection technology has significant limitations in terms of area and performance because it suffers from large interconnect lengths as well as an interconnect bandwidth bottleneck. To increase performance of 2D ICs continued research and development is a necessity.

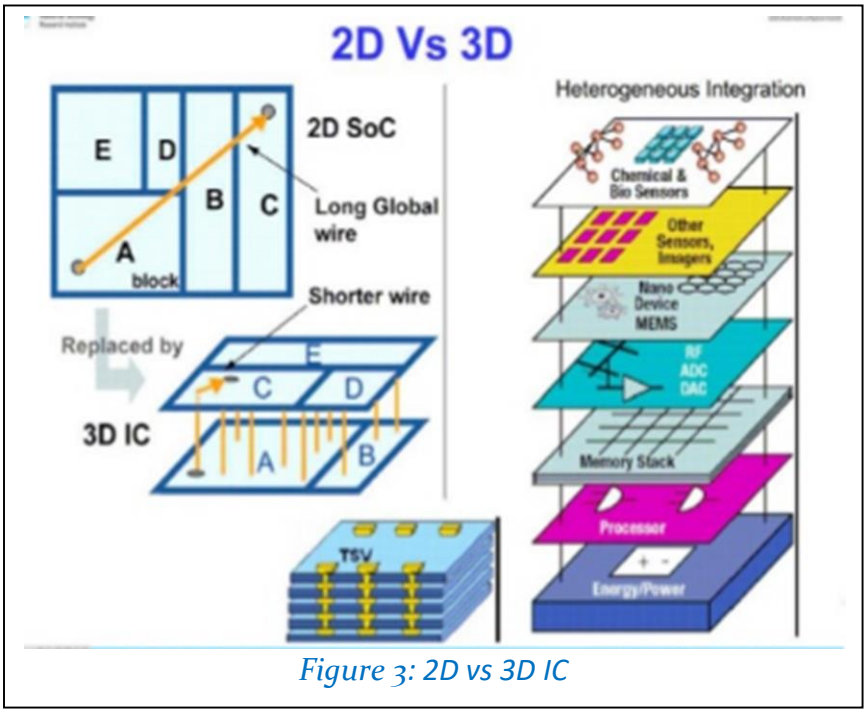

Figure 3: 2D vs 3D IC

2.5D interposer is a configuration where dies are mounted side-by-side on a silicon, glass, or organic interposer using through silicon vias (TSVs) through the interposer. (When glass or organic laminate is used as the interposer substrate, the vias are called through glass vias (TGV) and through substrate via (TSV) respectively.) Communication between the dies takes place via circuitry fabricated on the interposer.

3D ICs can be divided into 3D Stacked ICs (3D-SICs), which refers to stacking IC chips and interconnecting them with TSVs; and true 3D ICs, which use fab prosses to stack multiple device layers on a single chip, which may or may not use Very fine pitch TSVs to form the interconnect.

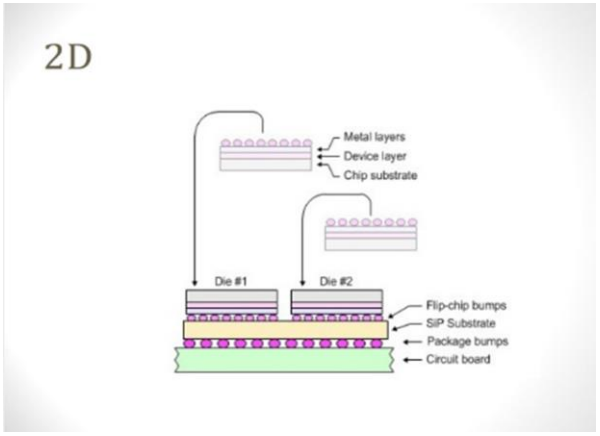

Figure4: 2D IC Structure

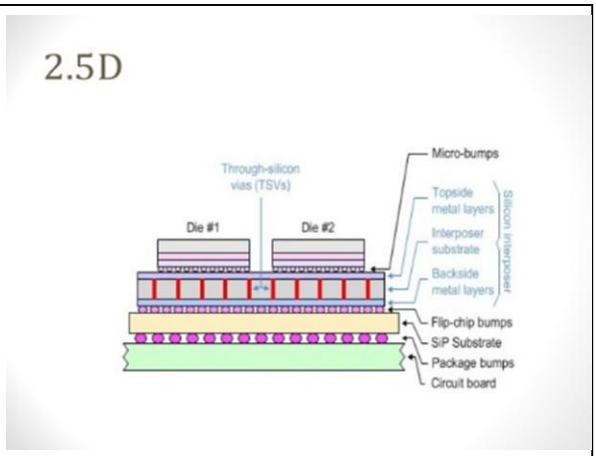

Figure 5: 2.5D IC Structure

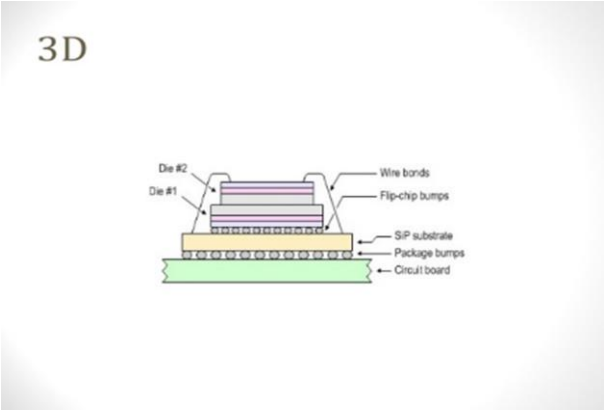

Figure 6: 3D IC Structure

5. Advantages of 3D IC's:

5.1. Timing delay:

Is the time taken to transfer data from one transistor to another, 3D IC's take the smaller timing delay could help to achieve higher frequencies.

The timing delay for 3D IC's is smaller than 2D IC's.

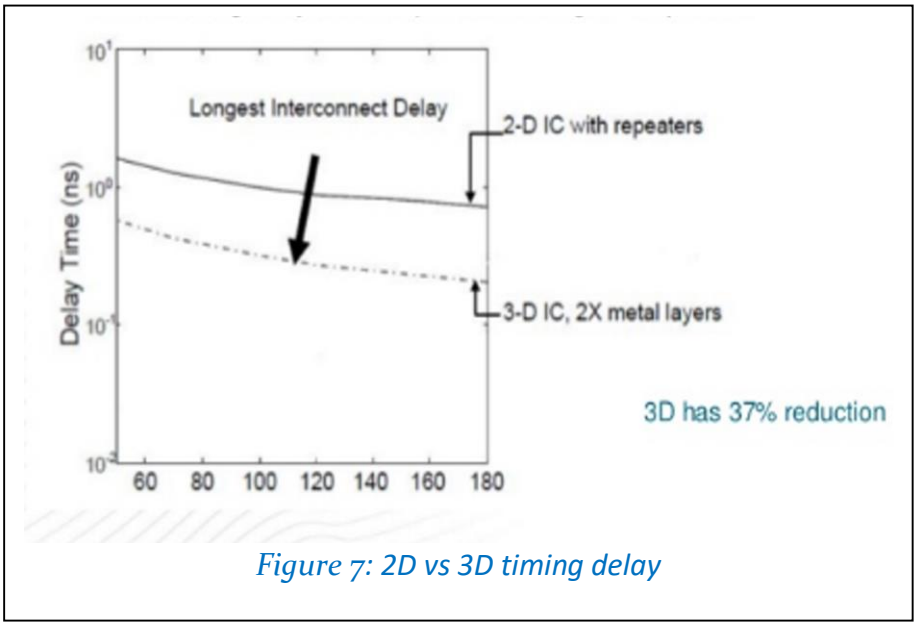

Figure 7: 2D vs 3D timing delay

5.2. Length of metal wire connection

Is the length of metal used to connect one transistor to another, 3D IC's use shorter metal to reduce timing delay and power consumption.

Reduction in the interconnect lengths reduces RC delays and increase chip timing performance.

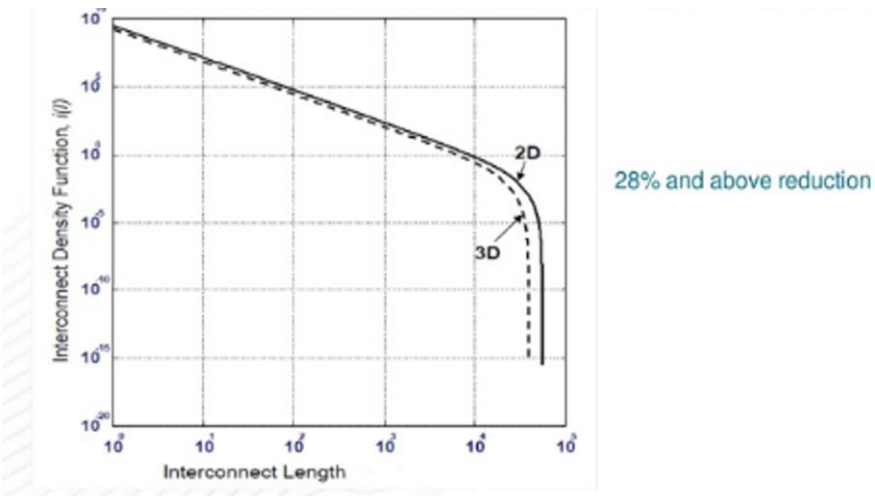

Figure 8: 3D IC provide the shorter wire than 2D

5.3. Data transfer rate

3D IC's ability to transfer more data rat per second more than 2D IC's

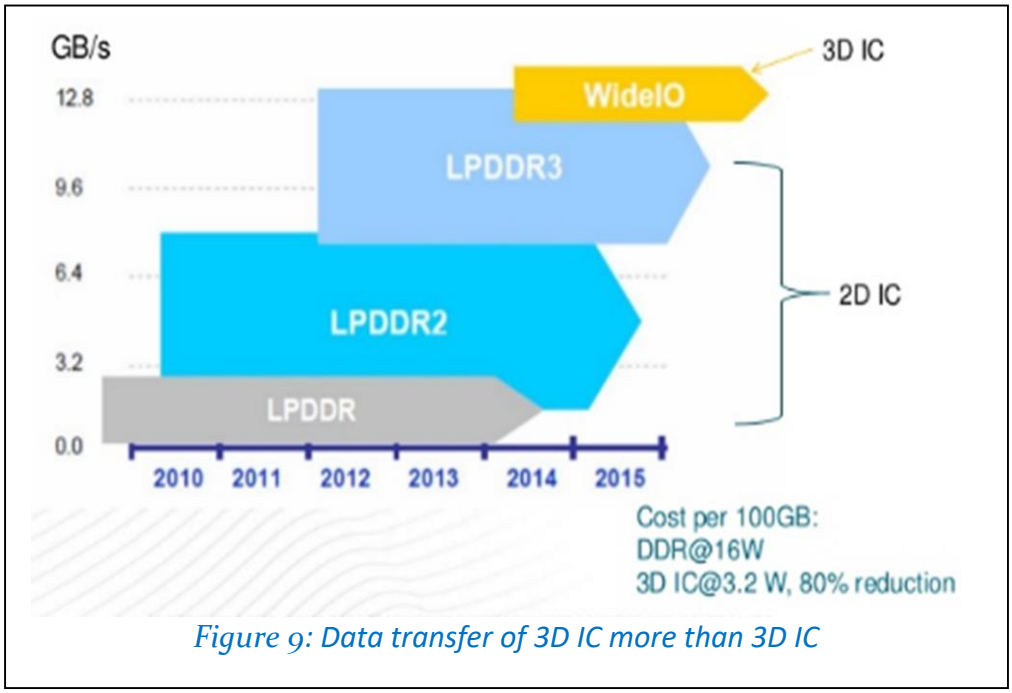

Figure 9: Data transfer of 3D IC more than 3D IC

5.4. Chip area:

3D IC's provide smallest size of silicon chip

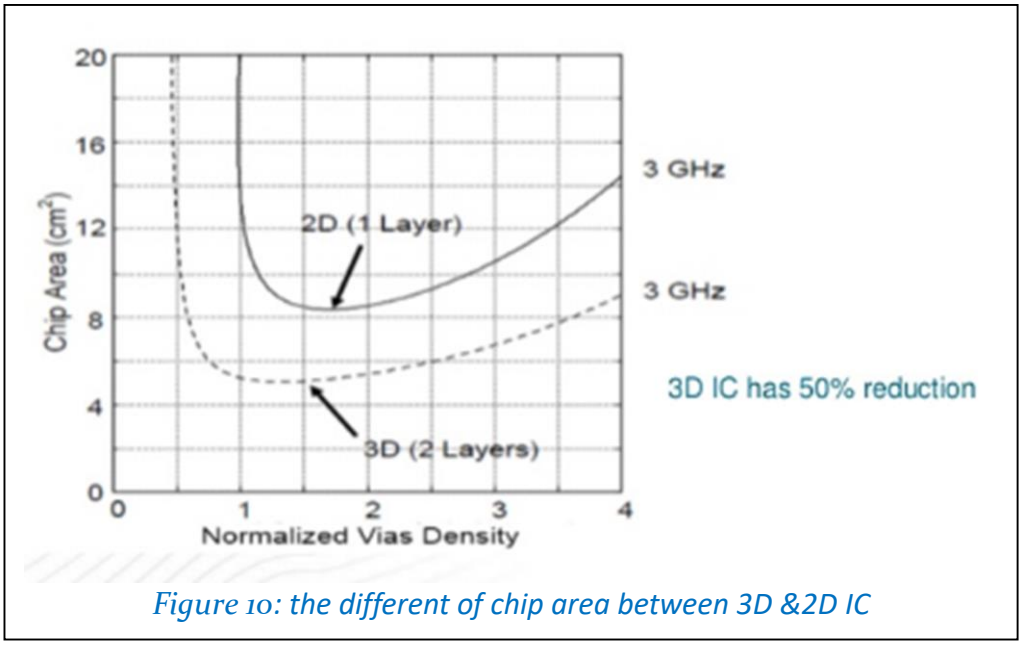

Figure 10: the different of chip area between 3D &2D IC

5.5. Operating frequency:

The higher frequency the better than smaller, 3D IC's provide higher frequency' higher frequency means higher speed of clock

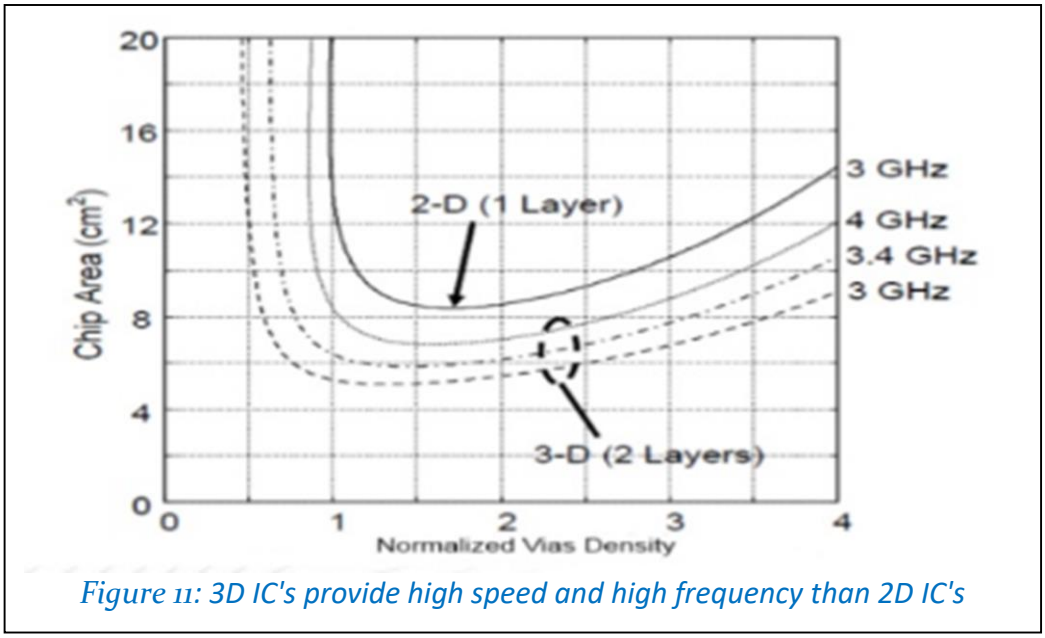

Figure 11: 3D IC's provide high speed and high frequency than 2D IC's

5.6. Energy consumption:

3D IC's provide less energy consumption than 2D IC's

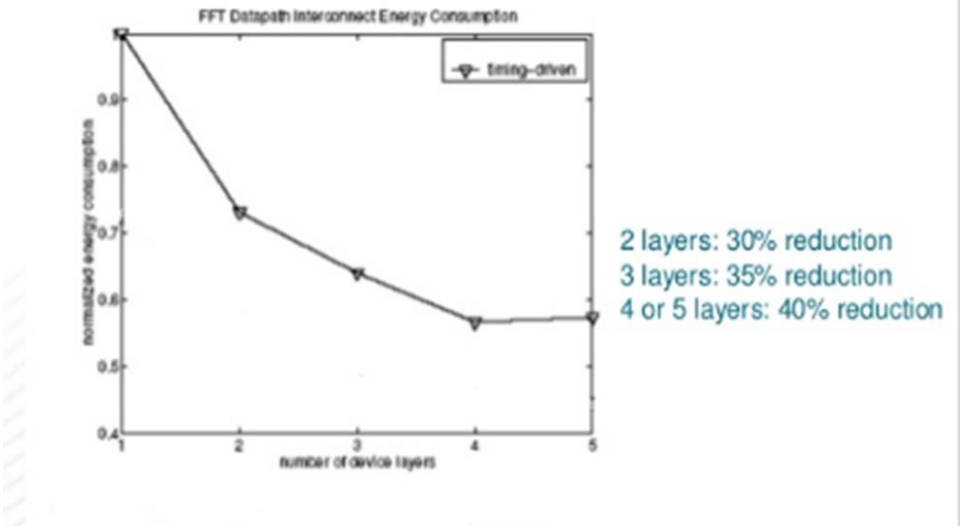

Figure 12: This graph shows the reduction in a normalized energy consumption with number of wire layers.

6.Manufacturing technology of 3D IC

There are four ways to built 3D IC:

1. Monolithic
2. Wafer on wafer
3. Die on wafer
4. Die on die

Monolithic:

Monolithic 3D ICs are built in layers on a single semiconductor wafer, which is then diced into 3D ICs. There is only one substrate, hence no need for aligning, thinning, bonding, or through-silicon vias. Process temperature limitations are addressed by partitioning the transistor fabrication to two phases. A high temperature phase which is done before layer transfer followed by a layer transfer using ion-cut, also known as layer transfer, which has been used to produce Silicon on Insulator (SOI) wafers for the past two decades. Multiple thin (10s–100s

nanometer scale) layers of virtually defect-free Silicon can be created by utilizing low temperature (<400°C) bond and cleave techniques, and placed on top of active transistor circuitry. Follow by finalizing the transistors using etch and deposition processes. This monolithic 3D IC technology has been researched at Stanford University under a DARPA-sponsored grant.

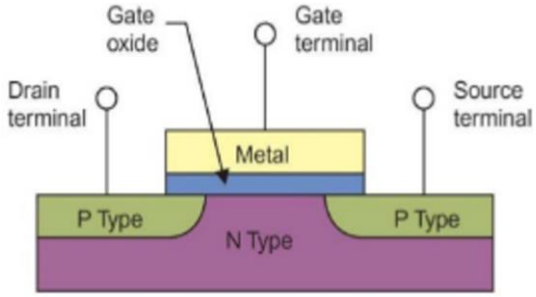

Figure 13: Monolithic 3D IC

Wafer on wafer

Electronic components are built on two or more semiconductor wafers, which are then aligned, bonded, and diced into 3D ICs. Each wafer may be thinned before or after bonding. Vertical connections are either built into the wafers before bonding or else created in the stack after bonding. These "through-silicon vias" (TSVs) pass through the silicon substrate(s) between active layers and/or between an active layer and an external bond pad. Wafer-to-wafer bonding can reduce yields, since if any 1 of N chips in a 3D IC are defective, the entire 3D IC will be defective. Moreover, the wafers must be the same size, but many exotic materials are manufactured on much smaller wafers than CMOS logic or DRAM (typically 300 mm), complicating heterogeneous integration.

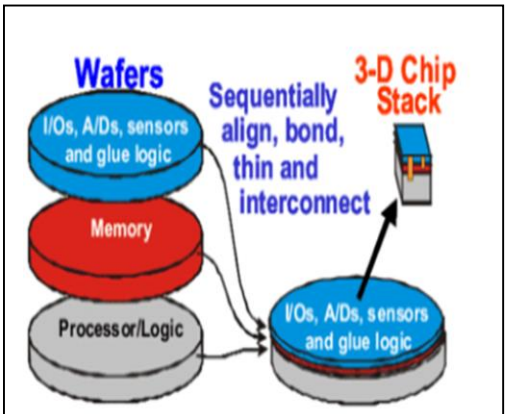

Figure 14: wafer on wafer 3D IC

Die on wafer

Electronic components are built on two semiconductor wafers. One wafer is diced; the singulated dice are aligned and bonded onto die sites of the second wafer. As in the wafer-on-wafer method, thinning and TSV creation are performed either before or after bonding. Additional die may be added to the stacks before dicing.

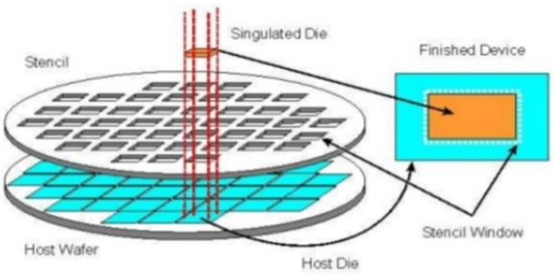

Figure 15: Die on Wafer 3D IC

Die on die

Electronic components are built on multiple die, which are then aligned and bonded. Thinning and TSV creation may be done before or after bonding. One advantage of die-to-die is that each component die can be tested first, so that one bad die does not ruin an entire stack.[12] Moreover, each die in the 3D IC can be binned beforehand, so that they can be mixed and matched to optimize power consumption and performance (e.g. matching multiple dice from the low power process corner for a mobile application).

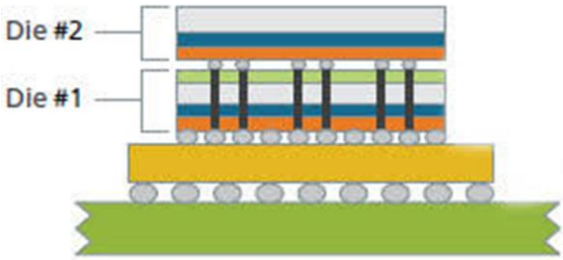

Figure 16: Die on die 3D IC

7. packing technology

The idea of 3D is not new. Two widely used technologies—system-in-package (SiP) and package-on-package (PoP)—have already demonstrated the benefits of using the third dimension in IC design. Both have enabled designers to pack more functionality at higher speeds and lower power into smaller spaces than mounting individual chips on a printed circuit board (PCB) allows. Both also have shown that combining building blocks on a die level or as packaged parts can save development time as well as cost and reduces the risk of respins. In spite of all these benefits, 3D ICs will not replace the proven 2D ICs. To the contrary, 2D ICs are the building blocks for 3D ICs and will continue to grow rapidly.

Stacked die:

Are being driven by the trend of smaller, tighter and more powerful devices. **Die stacking** is the process of mounting m ultiple chips on top of each other within a single semicondu ctor package. It is also known as chip stacking.

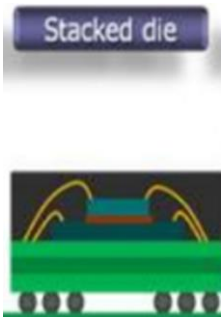

Figure 17: Stacked Die

Package on package (PoP)

Is an integrated circuit packaging method to combine vertically discrete logic and memory ball grid array (BGA) packages. Two or more packages are installed atop each other, i.e. stacked, with a standard interface to route signals between them. This allows higher component density in devices, such as mobile phones, personal digital assistants (PDA), and digital cameras, at the cost of slightly higher height requirements. Stacks with more than 2 packages are uncommon, due to heat dissipation considerations

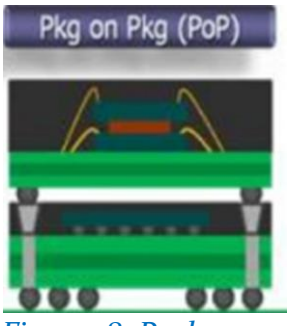

Figure 18: Package on Package

Through-silicon via (TSV) technology

Is the heart and most important key enabling technology of three-dimensional (3D) Si integration and 3D integrated circuit (IC) integration. It provides the opport unity for the shortest chip-to-chip interconnects and the smallest pad size and pit ch of interconnects. Stacking chips in 3D with TSVs ("Through-Si Vias") as intercon nects is today a "hot" new advanced packaging technology platform for memories , CMOS imagers and MEMS. Although the technical challenges for 3D ICs are close to be overcome, the cost of the technology is still a major hurdle. Compared with other interconnection technologies, such as wire bonding, the advantages of TSV include:

1) Better electrical performance
2) Lower power consumption
3) Wider data width and thus bandwidth
4) Higher density
5) Smaller weight
6) Lighter weight
7) Lower cost (hopefully)

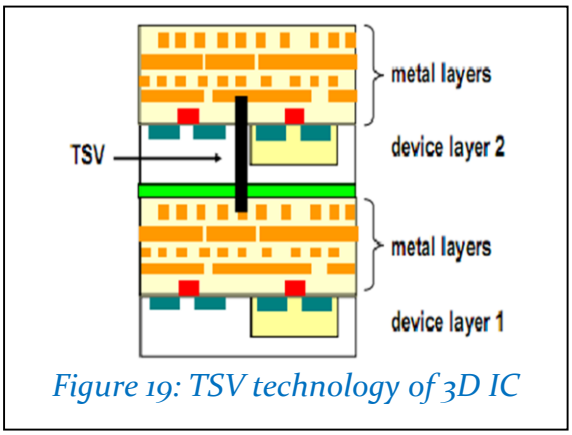

Figure 19: TSV technology of 3D IC

A system in a package (SiP) or system-in-package

Is a number of integrated circuits enclosed in one or more chip carrier packages that may be stacked using package on package.[1] The SiP performs all or most of the functions of an electronic system, and is typically used inside a mobile phone, digital music player, etc. Dies containing integrated circuits may be stacked vertically on a substrate. They are internally connected by fine wires that are bonded to the package. Alternatively, with a flip chip technology, solder bumps are used to join stacked chips together. A SiP is like a system on a chip (SoC) but less tightly integrated and not on a single semiconductor die.

SiP dies can be stacked vertically or tiled horizontally, unlike less dense multi-chip modules, which place dies horizontally on a carrier. SiP connects the dies with

standard off-chip wire bonds or solder bumps, unlike slightly denser three-dimensional integrated circuits which connect stacked silicon dies with conductors running through the die.

8. 3D ICs vs. 3D packaging

3D Packaging refers to3D integration schemes that rely on traditional methods of interconnect such as wire bonding and flip chip to achieve vertical stacks. ...

Three-dimensional integrated circuit (3D IC) is a MOS (metal-oxide semiconductor) integrated circuit (IC) manufactured by stacking silicon wafers or dies and interconnecting them vertically using, for instance, through-silicon vias (TSVs) or Cu-Cu connections, so that they behave as a single device to achieve ...

9. Conclusion:

- 3D IC's integration can reduce the wiring, thereby reducing the capacitances , power dissipation and chip area improves performance.
- Digital and analog circuits can be formed with better noise performance.
- It more cost effective thane 2D integration.
- 3D IC's will be the first of a new generation of dense, inexpensive chips having less delay and interconnection losses that will replace the conventional storage and recording media.