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Question 1.

- (a) A binary multiplier that multiplies two 4-bit binary words

For each 4-bit word we are multiplying, there are 16 possible values it can have. So the number of combinations for the inputs is $16^2 = 256$. Then we know that for multiplying two 4-bit numbers, the “worst case” in terms of bits required to represent the output is 8-bits. So, we need 256 words, 8 bits per word.

- (b) A 3-bit adder subtracter

For the 3-bit inputs there are $8^2 = 64$ possible combinations of the inputs. We will need an extra bit to specify if we want to add or subtract. The most output bits an operation would need is 4-bits because $111 + 111 = 1110$. So we will need 128 words, 4-bits per word.

Question 2.

- (a) How many $4\text{Mi} \times 16$ chips are needed to provide a total memory capacity of 64 Mi-bytes?

$$4\text{Mi} = 2^2\text{Mi} = 2^2 \cdot 2^{20} = 2^{22}$$

If the width of the chip is 16-bits = 2^4 bits, then each chip has a capacity of $2^{22} \cdot 2^4 = 2^{26}$ bits.

Our target for total memory capacity is 64 Mi-bytes = 2^6 Mi-bytes = $2^6 \cdot 2^{20}$ bytes. = $2^6 \cdot 2^{20} \cdot 2^3$ bits = 2^{29} bits. So we will need $2^{29}/2^{26} = 2^3$ chips.

8 $4\text{Mi} \times 16$ chips

- (b) How many address bits are needed for our larger, 64 Mi-byte-memory assuming the same word size as the individual chips?

Within one chip, we have 2^{22} words. We then need to decide between the 8 available chips. So we will have 2^{25} addresses.

25 bits for 2^{25} addresses.

- (c) How many of the address bits are connected to each RAM chip?

We will need to use 3 bits to determine which out of the 8 chips the data goes to. So we will have $25 - 3 = 22$ remaining bits for the address inside each chip.

- (d) How many of the address bits must be decoded for the chip select?

There are 3 bits for the chip select. The size of the decoder is $3 : 8$ or 3×8 .

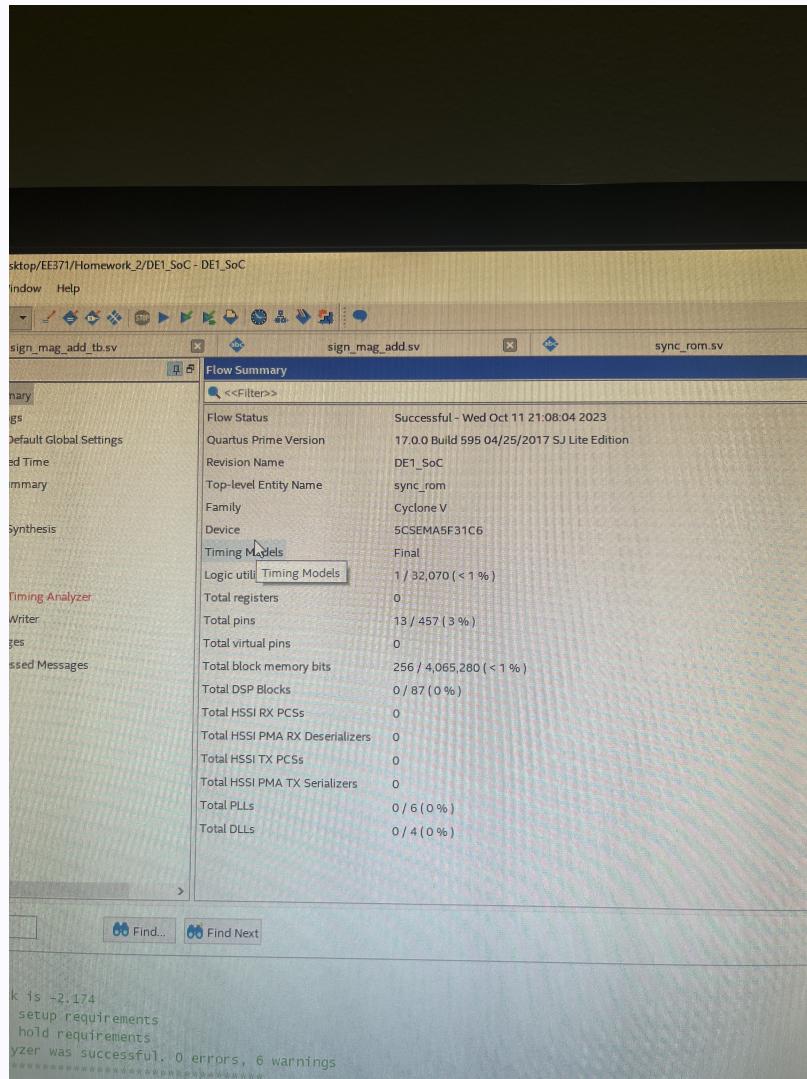
Question 3.

(a) Show the resource utilization

Sign mag:

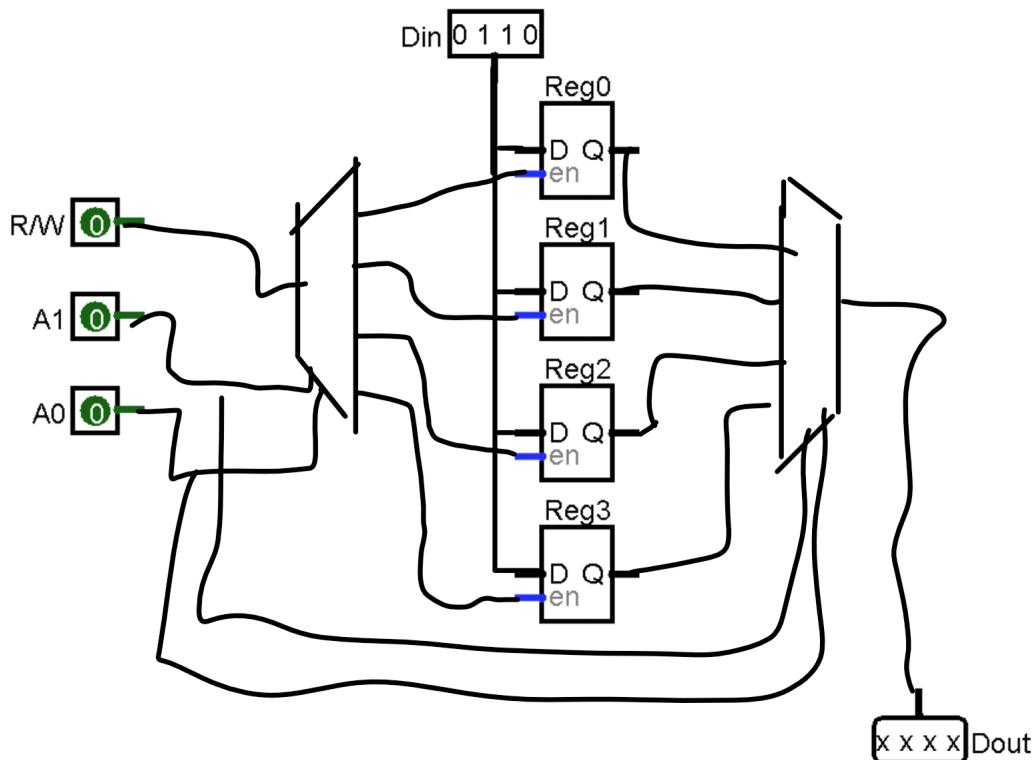
	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins	Full Hierarchy Name	Entity Name	Library Name
1	sign_mag_add	9 (9)	0 (0)	0	0	12	0	sign_mag_add	sign_mag_add	work

Sync rom:

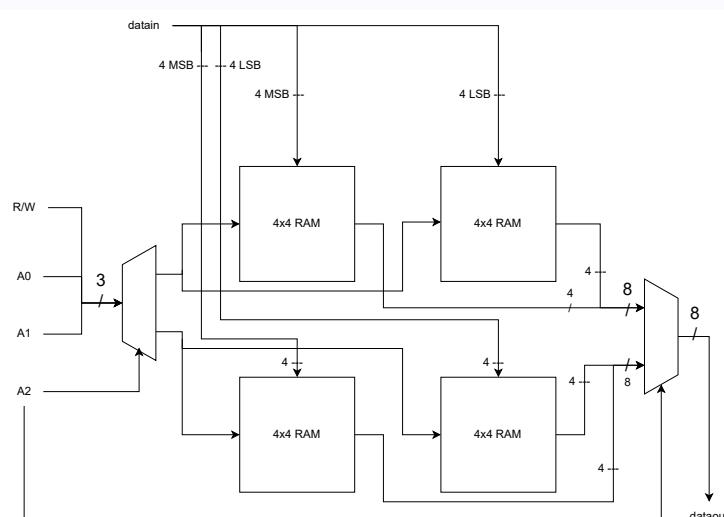


Question 4.

- (a) Complete the diagram below for an implementation of the 4×4 register file.



- (b) Construct a 8×8 memory diagram using the given 4×4 as a building block.



Question 5. Experience Report

We found this homework to be pretty simple and short. Problem 3 was definitely the most confusing and took the most time.

Question 1: 10 minutes

Question 2: 10 minutes

Question 3: 45 minutes

Question 4: 20 minutes