Design of Digital Circuits and Systems, HW4

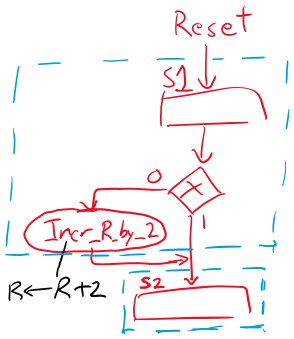
Algorithmic State Machines with Datapath

Solution Outlines

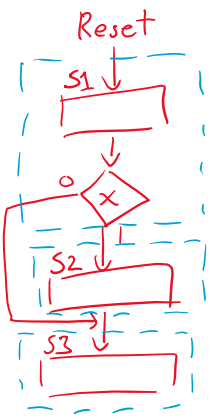
Problem 1:

Control signal name in (a) may be different, but should be appropriately descriptive.
Decision boxes in (c) may be structured differently (*e.g.*, one decision box on xy).

a)



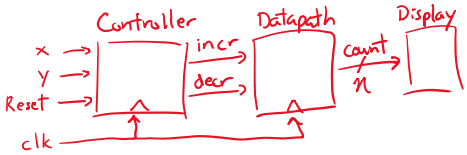
b)



c)

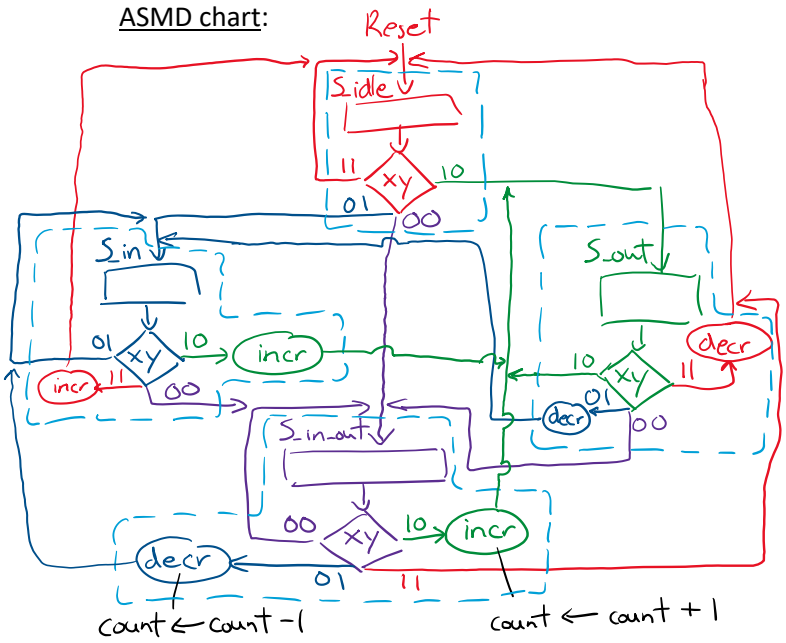
Problem 2:

Block diagram:



Note: in practice, the asynchronous inputs x and y should be synchronized to the clock to avoid metastability.

ASMD chart:



Problem 3:

Sample solution code not provided. Changes made to code should be explained in document or indicated in comments in the code.

Major fixes:

- The shift register needs to be 8 bits wide.
- The shift register needs to shift to the left, not the right.
- The counter was missing `3'b111` as its first argument (`.R`).
- Testbench for divider (*divider_tb.sv*) should be created to verify behavior.

Minor fixes:

- Modules should be parameterized instead of using local parameters.
- Nets and variables can be declared logic.
- Comments should be added to follow style guidelines.