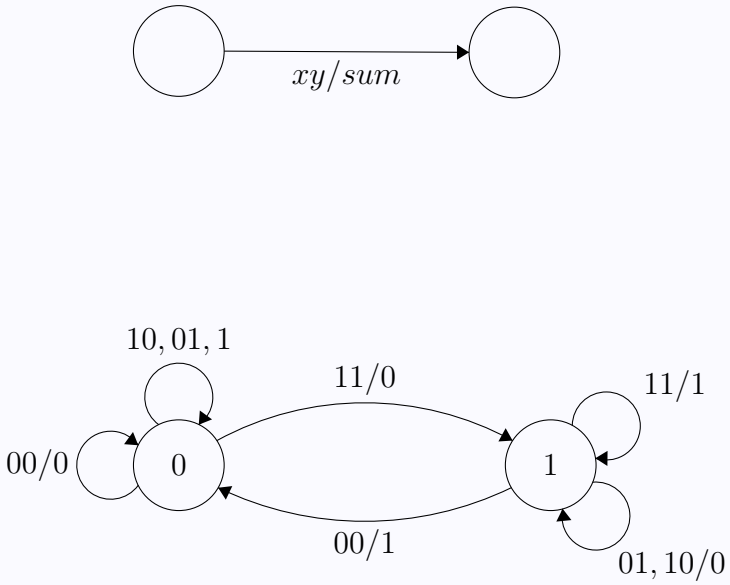
Contents

Collaborators: Cameron Jennings

Question 1.

(a) Draw out the state diagram of this circuit. Don't forget a reset state.



(b) Implement modules `hw1p1` and `hw1p1_tb`, which thoroughly simulates an instance of called dut.

Implemented in SystemVerilog, submitted on gradescope

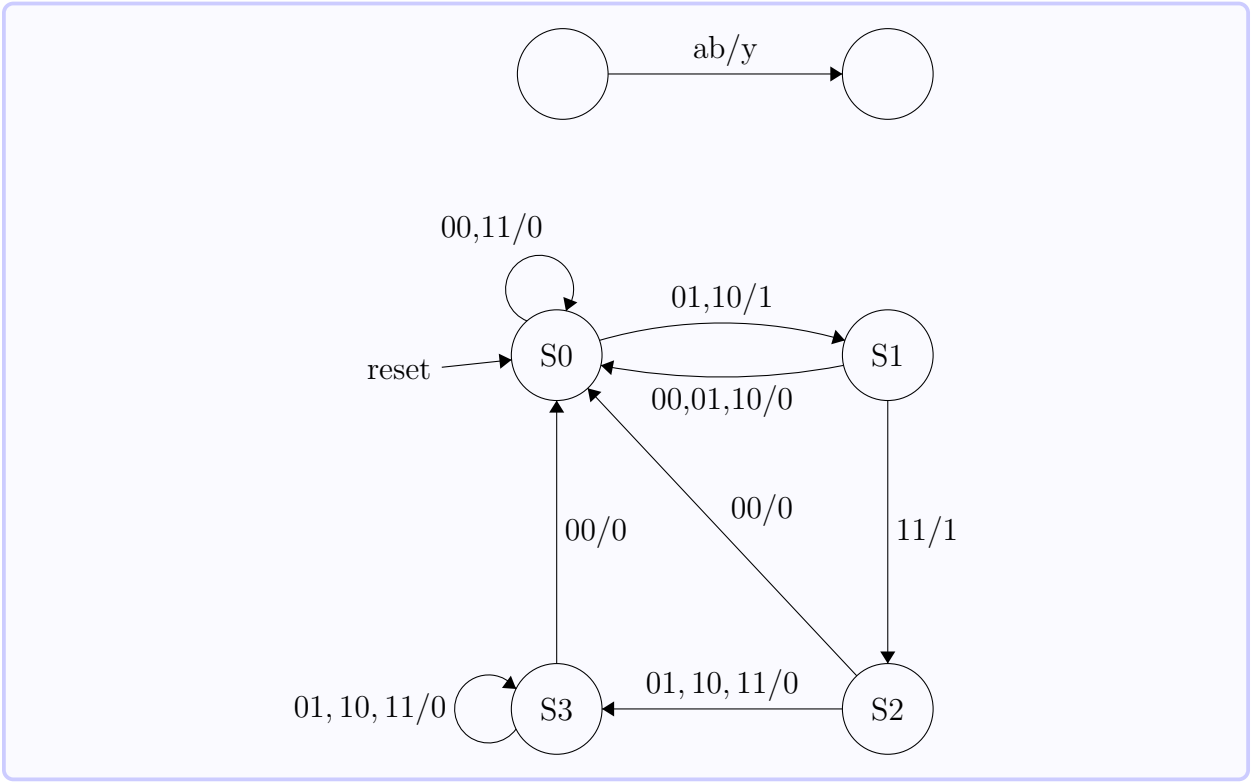
Question 2.

(a) Implement modules `hw1p2` and `hw1p2_tb` which thoroughly simulates an instance of hw1p2 called dut.

Implemented in SystemVerilog

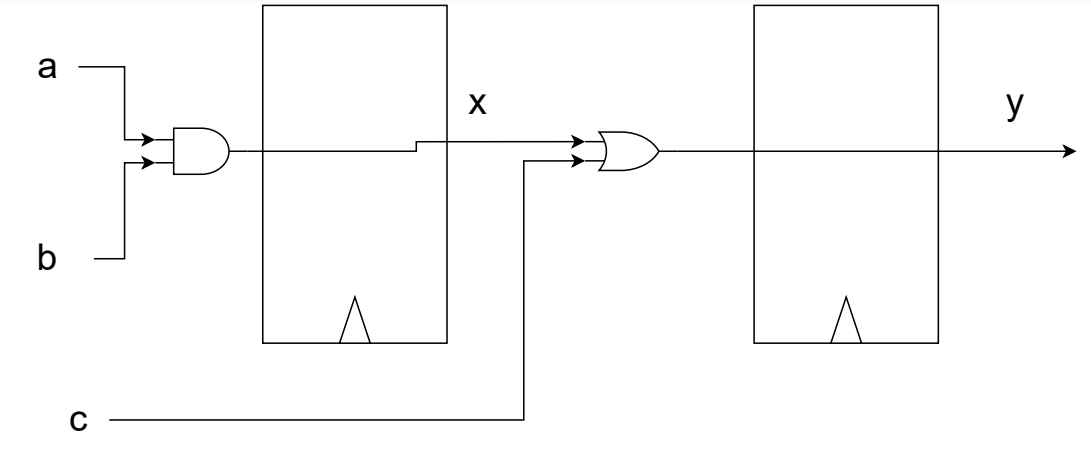
Question 3.

(a) Draw out the state diagram for the FSM

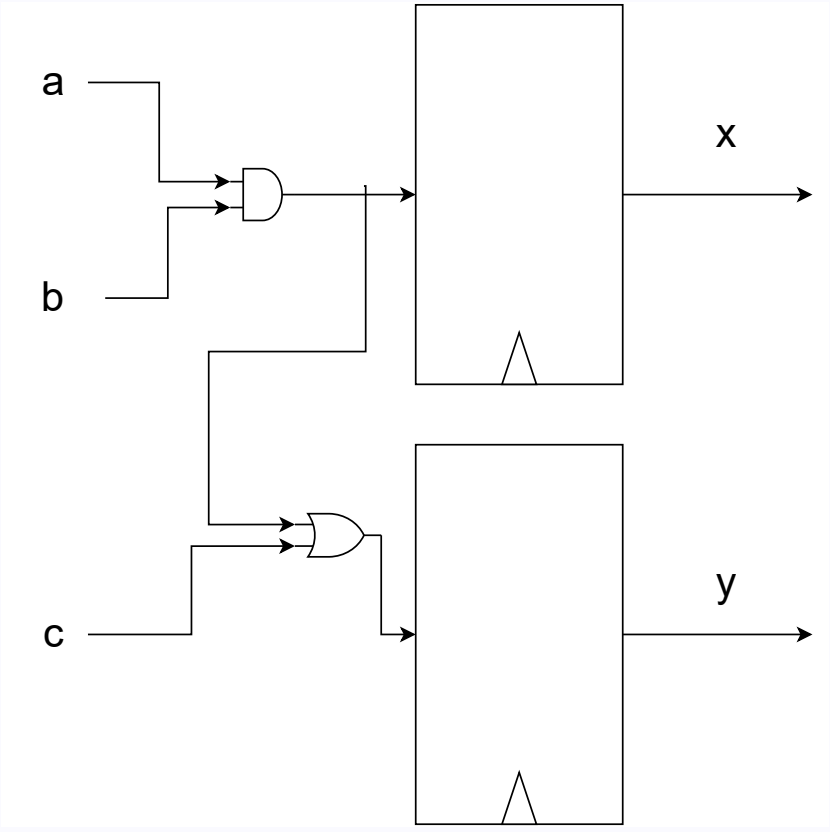


Question 4. Sketch the hardware each circuit implies

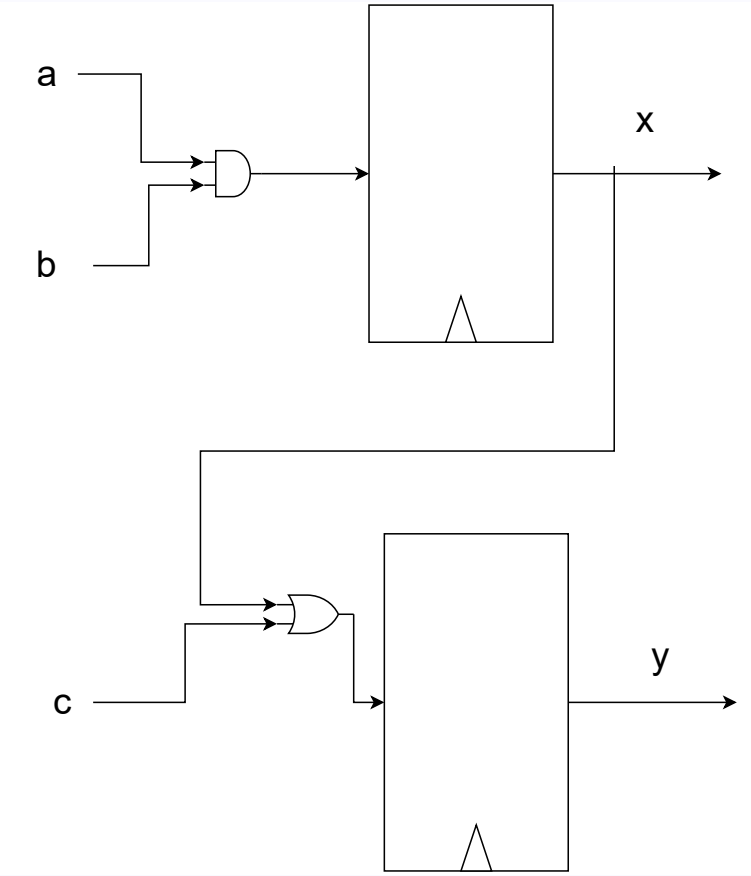
(a) Circuit 1 Parallel



(b) Circuit 1 Sequential



(c) Circuit 2 Parallel



(d) Circuit 2 Sequential