Contents

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Question 1.

(a) Breifly explain your approach. Describe a high level the change you made to the code and how you verified that it works correctly.

Our approach was to change the lower-level modules first and use testbenches to verify they have the expected behavior. That started with the reg file by changing it so we can write 16 bits at a time.

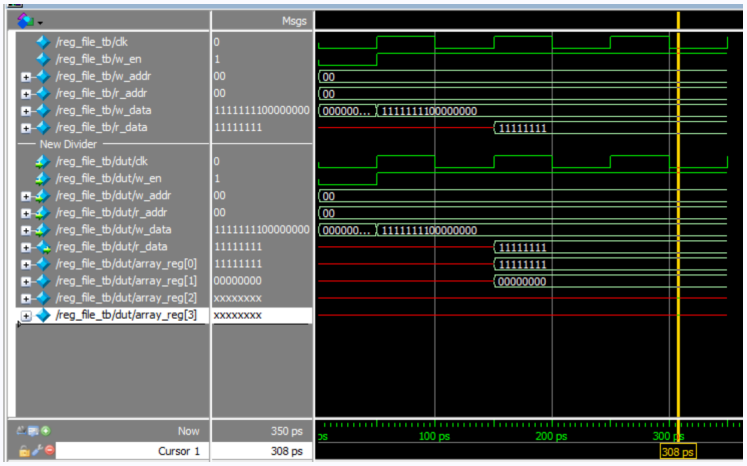
We then changed the controller to accomodate the logic of writing 16 bits at a time. This includes incrementing the write address by two, and changing it so that the buffer is full when the read and write pointers are within 1 address apart.

We ensured the `reg_file` module was working by using a testbench to demonstrate that we could write 16 bits with the MSB and LSB in the correct order in the buffer. We then ensured the `fifo_ctrl` module was working by using a test bench to demonstrate that reading and writing moves the correct pointers and the `full` signal was asserted when the buffer was actually full.

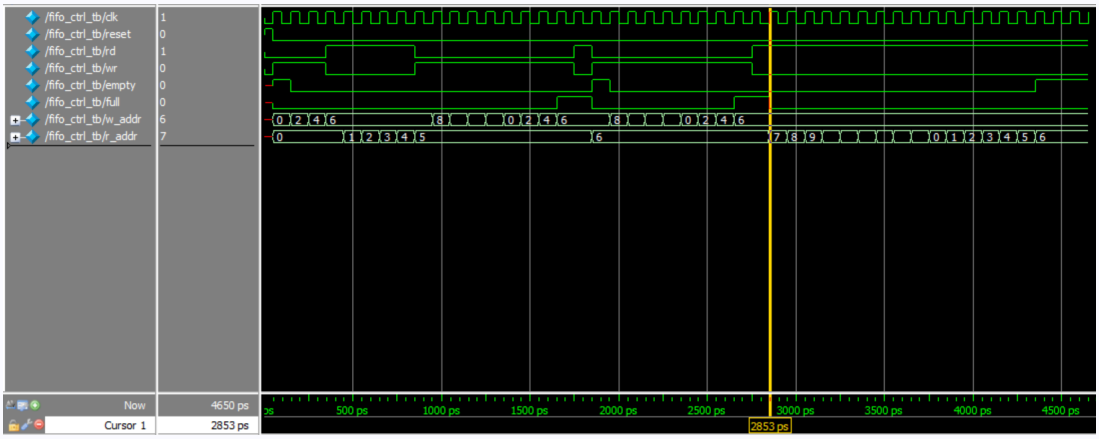
We then ensured the `fifo` was working by using a testbench to demonstrate that we could write to the buffer (16 bits at a time) and read from the buffer (8 bits at a time).

(b) Simulation Results

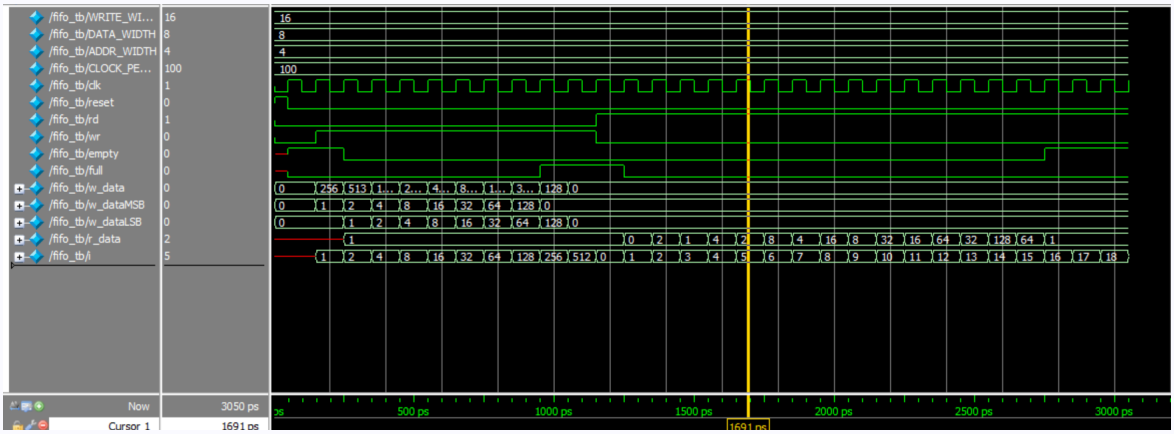
Reg File Simulation:



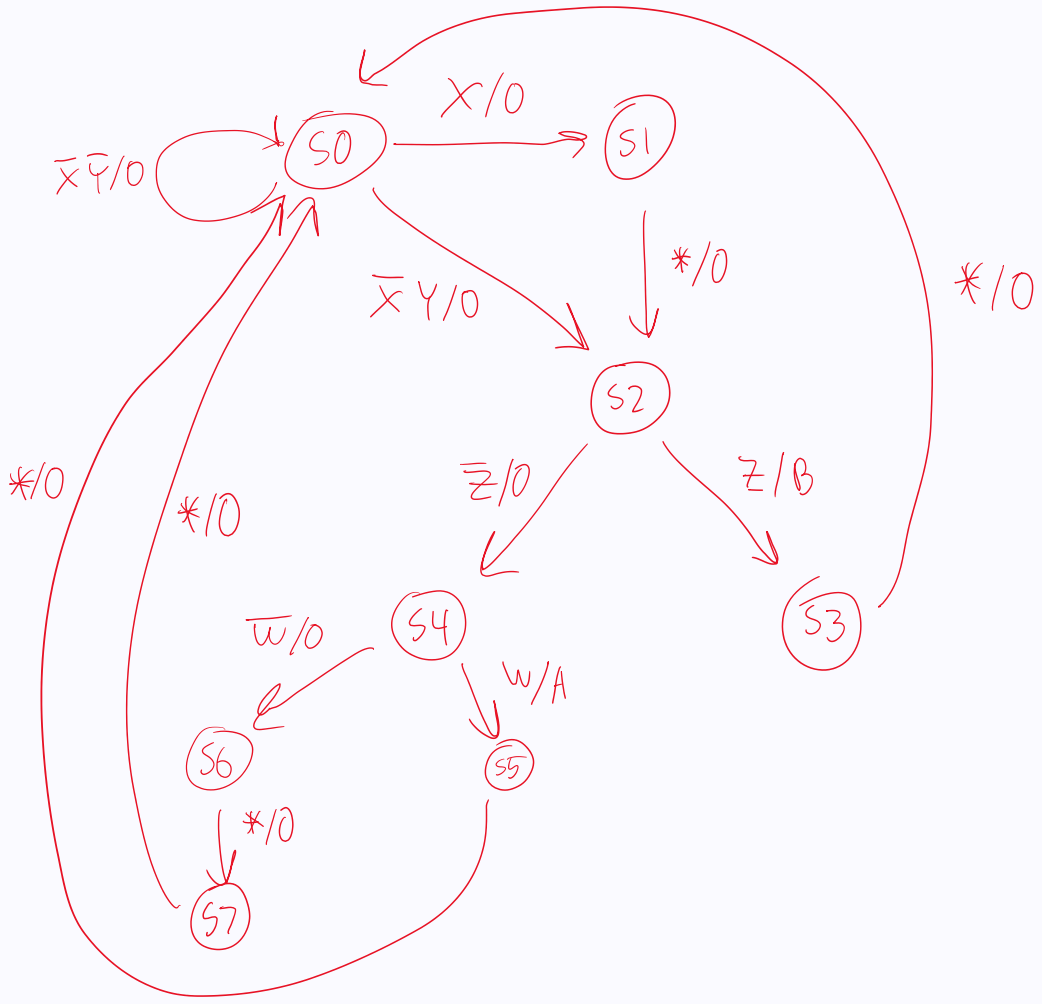
Fifo Ctrl Simulation:



Fifo Simulation:



Question 2.



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Question 3.

(a) Describe/explain the difference in timing between the Moore and Mealy outputs. How do the ASM blocks help indicate the timings?

The difference in timing is due to mealy being asynchronous while moore is syrchnous. Moore output is dependent on the state of the machine which is synced with the clock. Therefore when the clock updates the state, the output will be triggered at the same instant. However with Mealy machines, the output is also dependent on the input to the system, which can occur at anytime. Considering the state of the machine is idle between clock cycles, a proper input can trigger an output do to a combination of state and input. Thefore, the output for a Mealy machine can change at any point in time regardless of clock. The ASM blocks indicate timing because the Mealy outputs come after the state block which may contain Moore outputs. So, the distinction of which type of output it is, is made clear in an ASM chart.

(b) In your opinion, how does tracing an ASM chart compare to tracing an FSM diagram.

We think ASM charts are cleaner to look at. We also think that FSM diagrams are easier to translate into verilog. However with an chart, it is easier to see the computations that are happening / why the hardware is designed the way it is.

Question 4. Experience Report

We found this homework to be somewhat simple and short. Problem 1 was definitely the most confusing and took the most time.

Question 1: 2 hours

Question 2: 20 minutes

Question 3: 45 minutes