Design of Digital Circuits and Systems, HW3

Buffers and ASM

Deliverables (Gradescope)

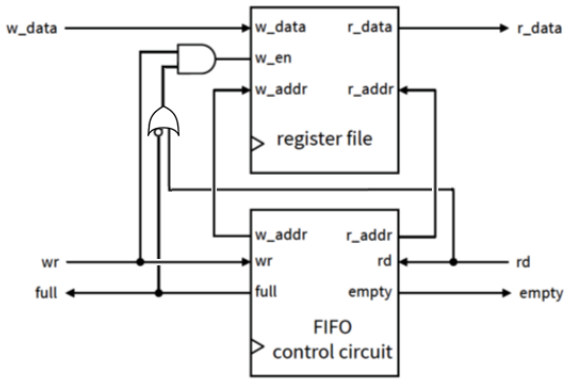
1) Homework problem solutions (*i.e.*, text, diagrams, screenshots, work) in a single PDF file ending in `.pdf` (all lowercase).
   a) At the end of this document, estimate how long you spent working on the homework and rate the difficulty on the following scale: Very Hard — Hard — Moderate — Easy — Very Easy
2) SystemVerilog files `fifo.sv`, `fifo_ctrl.sv`, `reg_file.sv`, `fifo_tb.sv`, and `hw3p3.sv`.

Problems

Problem 1:

> ⚠ This problem will *not* be autograded so you will need to include screenshots of your ModelSim simulation in your PDF file. While a full explanation won't be required, please point out what special situations you tested in your simulation (and where).

You are provided with three SystemVerilog files that implement the FIFO buffer shown below (`fifo.sv`, `fifo_ctrl.sv`, `reg_file.sv`) and an empty test bench (`fifo_tb.sv`).



In some applications, the widths of the write port and read port of a FIFO buffer are not the same. For example, a subsystem may write 16-bit data into the FIFO buffer and another subsystem only reads and removes 8-bits of data at a time.

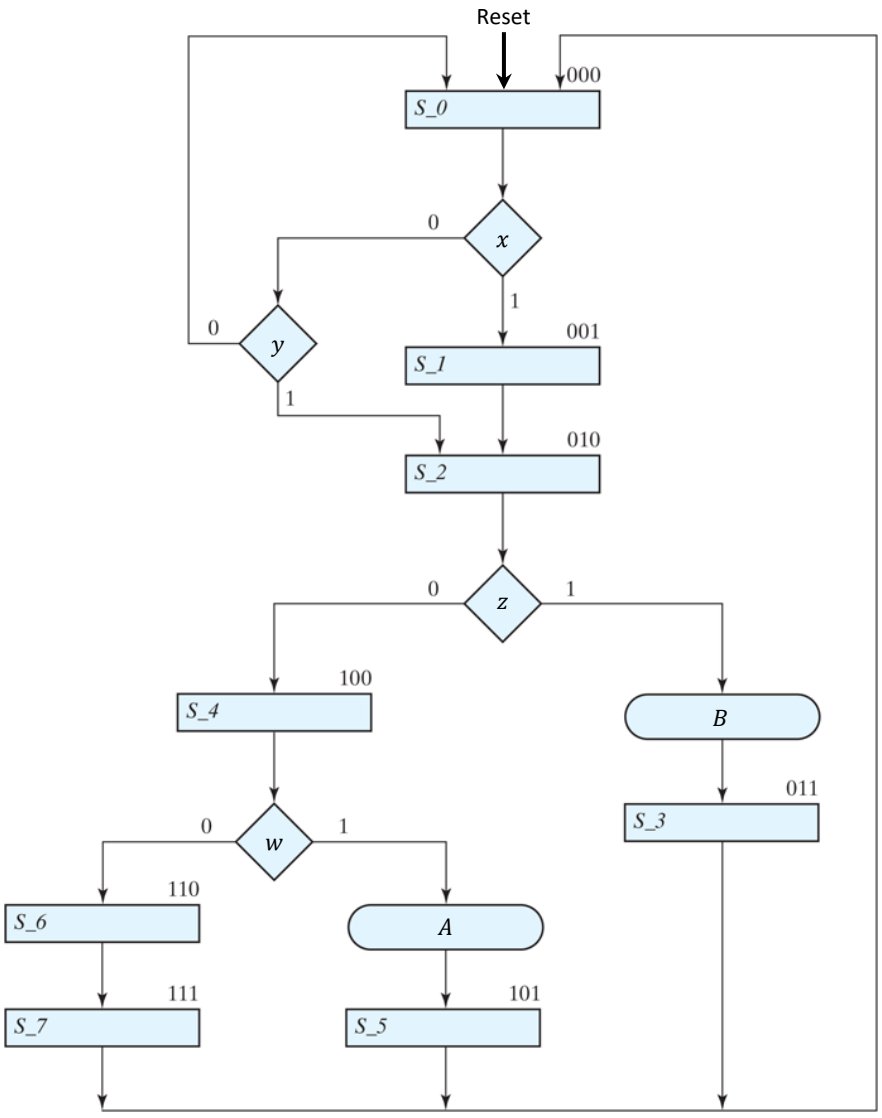
Assume that the width of the write port is twice the width of the read port. Once written, the upper half (*i.e.*, most significant bits) of the data should be read before the lower half.

- Redesign the FIFO with a modified controller and register file and verify its operation. The `DATA_WIDTH` parameter should be the width of the read port.
- *Briefly* explain your approach: describe at a high level the changes you made to the code and how you verified that it works correctly. Be sure to provide your simulation results.

Problem 2:

An ASM chart is shown below.

- Draw the equivalent state diagram.



Problem 3:

The ASM chart for Example #4 from Lecture 5 is reproduced below.

- Implement the ASM chart in the provided file *hw3p3.sv* and write the test bench to *thoroughly* test the state machine.
  - Do not modify the given port names, including both spelling and capitalization.
  - Make sure to use both **ps** and **ns** as state signals.
  - You should simulate the test bench to verify the expected behavior, but do not need to submit a screenshot or explanation of the simulation.
- Describe/explain the difference in timing between the Moore and Mealy outputs. How do the ASM blocks help indicate the timings?
- In your opinion, how does tracing an ASM chart compare to tracing an FSM diagram?