Contents

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Question 1.

$$\begin{aligned}
\text{hold slack} &= \text{DAT}_h - \text{DRT}_h \\
&= \text{min data path} - \text{max clock path} \\
&= (T_{\text{clk1}} + T_{\text{CO}} + T_{\text{data min}}) - (T_{\text{clk2}} + T_{\text{hold}}) \\
&= 6\text{ns} - 3.5\text{ns} \\
&= 2.5\text{ns}
\end{aligned}$$

The hold slack meets timing requirements.

$$\begin{aligned}
\text{setup slack} &= \text{DRT}_{\text{su}} - \text{DAT}_{\text{su}} \\
&= \text{min clock path} - \text{max data path} \\
&= (T + T_{\text{clk2}} - t_{\text{su}}) - (T_{\text{clk1}} + T_{\text{CO}} + T_{\text{data max}}) \\
&= (6.67\text{ns} + 2\text{ns} - 2\text{ns}) - (1\text{ns} + 2\text{ns} + 5\text{ns}) \\
&= -1.33\text{ns}
\end{aligned}$$

The setup slack does not meet the timing requirements because it is negative.

Question 2.

The max data path is In → AND → NOR → reg1.

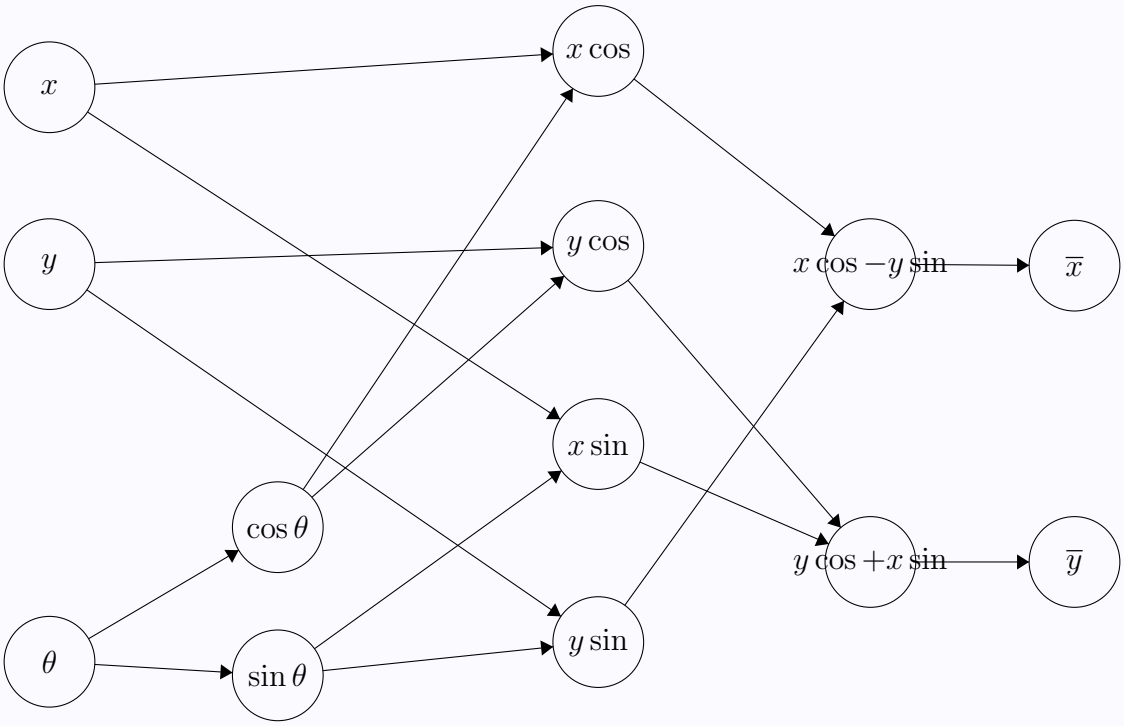
$$\begin{aligned}
\text{setup slack} &= \text{DRT}_{\text{su}} - \text{DAT}_{\text{su}} \\
&= \text{min clock path} - \text{max data path} \\
&= (T_{\text{period}} + T_{\text{clk1,min}} - t_{\text{su}}) - (T_{\text{in, max}} + T_{\text{AND, max}} + T_{\text{NOR, max}}) \\
&= (100\text{ns} + 4\text{ns} - 10\text{ns}) - (17\text{ns} + 40\text{ns} + 30\text{ns}) \\
&= 94\text{ns} - 87\text{ns} \\
&= 7\text{ns}
\end{aligned}$$

The min clock path is reg1 → AND → reg2.

$$\begin{aligned}
\text{hold slack} &= \text{DAT}_{h} - \text{DRT}_{h} \\
&= \text{min data path} - \text{max clock path} \\
&= (T_{\text{clk1,min}} + T_{\text{CO, min}} + T_{\text{AND, min}}) - (T_{\text{launch}} + T_{\text{clk2,max}} + T_{\text{hold}}) \\
&= (4\text{ns} + 8\text{ns} + 35\text{ns}) - (0\text{ns} + 3\text{ns} + 5\text{ns}) \\
&= 47\text{ns} - 8\text{ns} \\
&= 39\text{ns}
\end{aligned}$$

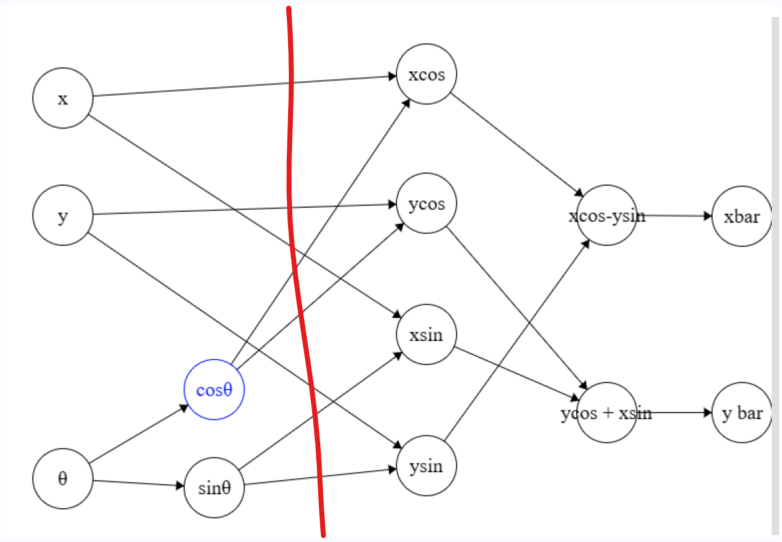
Question 3.

(a) Draw the DFG



(b) Cuts

1 stage cut

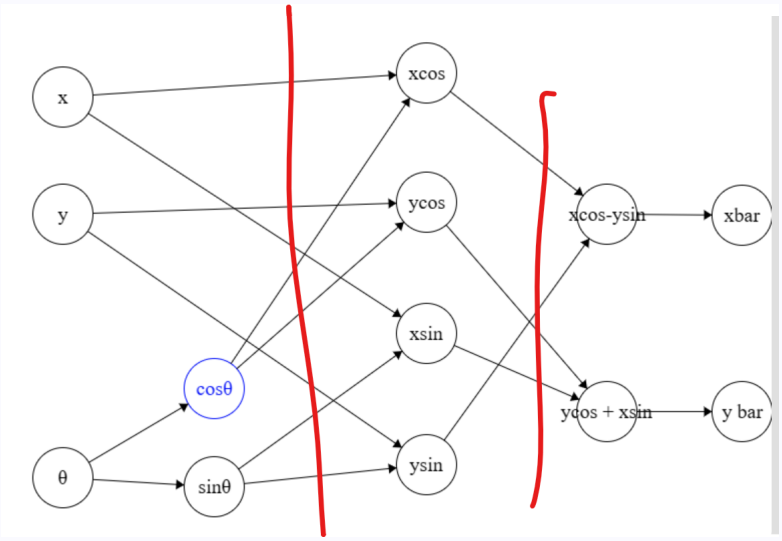


The clock period for this pipelined circuit is:

$$\max(10\text{ns} + 100\text{ns}, 10\text{ns} + 60\text{ns} + 30\text{ns}) = 110\text{ns}$$

.

2 stage cut



The clock period for this pipelined circuit is:

$$\max(10\text{ns} + 100\text{ns}, 10\text{ns} + 60\text{ns}, 10\text{ns} + 30\text{ns}) = 110\text{ns}$$

.

(c)

2-stage

$$\begin{aligned}\text{latency} &= \#\text{ of stages} \cdot T_{\text{period}} + T_{\text{CO}} \\ &= 2 \cdot 110\text{ns} + 10\text{ns} \\ &= 220\text{ns} + 10\text{ns} \\ &= 230\text{ns}\end{aligned}$$

3-stage

$$\begin{aligned}\text{latency} &= \#\text{ of stages} \cdot T_{\text{period}} + T_{\text{CO}} \\ &= 3 \cdot 110\text{ns} + 10\text{ns} \\ &= 330\text{ns} + 10\text{ns} \\ &= 340\text{ns}\end{aligned}$$

Question 4.

(a) What element adds the most delay?

The datapath adds the most delay with 16.138ns. The DRT is 15.989ns. DAT is 20.248 ns. Using setup slack equation, DRT - DAT, this would give us -4.259ns. To ensure setup meets timing requirements, we should add at least 4.259ns.

(b) Does the same element add the most delay for hold slack? Why does this make sense?

No. The longest timing element in delay slack is the clock delay. This makes makes sense because it's the longest clock path which determines the hold slack.

(c) What is the fastest frequency you can set the clock to for this to pass setup timing?

The new DAT is 16.759ns. Therefore that's the period we need for our clock. The frequency would be $\frac{1}{16.759\text{ns}}$ which gives 5.96×10^7Hz.

(d) SETUP: Which of the options had the most setup slack?

Fast/0C

(e) SETUP: How does increasing voltage speed change the speed of a circuit?

Increasing voltage increases speed.

(f) SETUP: How does increasing temperature change the speed of a circuit?

Increasing temperature slows down the circuit

(g) HOLD: Which of the options had the most hold slack?

Fast/0C

(h) HOLD: How does increasing voltage speed change the speed of a circuit?

Increasing voltage increases speed.

(i) HOLD: How does increasing temperature change the speed of a circuit?

Increasing temperature slows down the circuit

Question 5. Experience Report

We found this homework to be moderate. Question 3 had some tricky parts where we almost forgot to add the last T_{CO}. Question 4 took a while.

Question 1: 30 minutes

Question 2: 30 minutes

Question 3: 30 minutes

Question 4: 1 hour.