Universidad de las Américas Puebla

Escuela de ingeniería

Departamento de computación, electrónica y mecatrónica

UDLAP®

Lab report #3

Course: Digital design LRT2022-1

Topic: Simplifying Boolean functions

Team: Mesa 1

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1 Abstract

Abstract

2 Analisis

2.1 Schematic

Boolean Functions

F_1 = (((A) nand (B)) nor ((B) xnor (C))) nand (((C) xor (D)) or ((B) xnor (C))) F_2 = (((D) and (not(B))) and ((A) xor (B))) or (not ((C) and not(A)))

Tables

Table 1: Function 1

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Table 2: Function 2

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$F(ABCD)$ is true for:

- $\overline{ABC}D$
- $\overline{AB}CD$
- $\overline{A}B\overline{CD}$
- $\overline{A}B\overline{C}D$
- $A\overline{BC}D$
- $A\overline{B}C\overline{D}$
- $A\overline{B}CD$
- $AB\overline{CD}$
- $AB\overline{C}D$

$F(ABCD)$ is false for:

- $\overline{ABCD}$
- $\overline{AB}C\overline{D}$
- $\overline{A}BC\overline{D}$
- $\overline{A}BCD$
- $A\overline{BCD}$
- $ABC\overline{D}$
- $ABCD$

Canonical form using Miniterms:

$$F(ABCD) = m_1 + m_3 + m_4 + m_5 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}$$

Canonical form using Maxiterms:

$$F(ABCD) = M_0 \cdot M_2 \cdot M_6 \cdot M_7 \cdot M_8 \cdot M_{14} \cdot M_{15}$$

2.2 Schemes

3 Discussion

3.1 Comments

First of all, all the complete diagrams and electrical images can be found in the appendix. The tables have two representation formats. The Table 1 shows the state of two inputs put together and compared. As for the table 2, there is the F and T which represent true for T or false for F, which can also be seen as 1 for true and 0 for false as in Table 1. The analysis taken to check the canonic forms is shown in the Analysis section. As for a letter with decoration represents true state, therefore the list is the points at which the system output is considered true or false. With that and with the table, we can name the first row of states as m_0 and increasing. We can then express both canonic forms with m and subindex of the row it represents.

Next there are the schemes which are actual simulations using Multisim of the thing they represent. They are used to represent the logic behind the implementation on the protoboard. Inside records we have the actual simulations of the working circuits at full. The EP waves show the active and unactive states of those circuits. I elaborated the same as in the tables, for Figure 5 I concentrated the outputs for the same inputs. The difference comes with the Figure 6 which is focused on the function F(ABCD). To be able to generate those waves I used the Active HDL software and the code provided in the code section in the appendix.

I managed to implement the logic gates as follows(All states are included in the apendix):

These figures are only one of the states taken from camera in real implementations. The most important thing to consider here are the volts of 5V and amperes of 0.3mA. Some of the images appear to be on or off, that is because during the placement of the switch there was confusion which led to flip the switch upside down, still, the expected behaiviour was the same, just the state of the lever was different because of the flipping. That mirror image problem also appeared because of the difficulty of doing all the gates together the same day and splitting the tests in different days.

3.2 Conclusion

Based on the information of comparison between representations with schemes, waves and tables we can conclude that the system indeed worked the same. Although the components in the actual circuit varied, they worked as expected based on the table. The most difficult part was not to get confused during the connection of the funtion F(ABCD) which had that difficulty on the amount of cables derived and the lack of a 3 gate AND logic gate to simplify the connections. That is reflected in the multisim simulation because of the amount of inputs I had to create which were connected through the same keyboard key.

A Code

B Schemes

References