Heimadæmi05 Greining og Hönnun stýrikerfa TÖV201G

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6.4

6.4* The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?

6.4 Lausn

- 101101 -> 1101; 0110; 1011; 1101; 0110; 1011

6.11

6.11 A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if
(a) the normal outputs of the flip-flops are connected to the clock and
(b) the complement outputs of the flip-flops are connected to the clock?

6.11 lausn

- a) A count down counter
- b) A count up counter

6.14

6.14 How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following counts?
(a) *1001100111
(b) 1111000111
(c) 0000001111

6.14 Lausn

- a) * 1001100111 = **4;**
- b) 1111000111 = **9;**
- c) 0000001111 = **10**

6.19

6.19 The flip-flop input equations for a BCD counter using *T* flip-flops are given in Section 6.4. Obtain the input equations for a BCD counter that uses (a) *JK* flip-flops and (b)* *D* flip-flops. Compare the three designs to determine which one is the most efficient.

6.19 Lausn

- a) JK flip-flops

Let Q_1, Q_2, Q_4, Q_8 represent 4-bits of the counter's present state and A8, A4, A2, A1 represent the next state.

Present state				Next State				JK flip-flop							
Q_8	Q_4	Q_2	Q_1	A_8	A_4	A_2	A_1	J_{A8}	K_{A8}	J_{A4}	K_{A4}	J_{A2}	K_{A2}	J_{A1}	K_{A1}
0	0	0	0	0	0	0	1	0	x	0	x	0	x	1	x
0	0	0	1	0	0	1	0	0	x	0	x	1	x	x	1
0	0	1	0	0	0	1	1	0	x	0	x	x	0	1	x
0	0	1	1	0	1	0	0	0	x	1	x	x	1	x	1
0	1	0	0	0	1	0	1	0	x	x	0	0	x	1	x
0	1	0	1	0	1	1	0	0	x	x	0	1	x	x	1
0	1	1	0	0	1	1	1	0	x	x	0	x	0	1	x
0	1	1	1	1	0	0	0	1	x	x	1	x	1	x	1
1	0	0	0	1	0	0	1	x	0	0	x	0	x	1	x
1	0	0	1	0	0	0	0	x	1	0	x	0	x	x	1

Upon inspection of the table we get the equations
JK flip-flop Ipmlentation

$J_{A1} = 1$
$K_{A1} = 1$

$J_{A2} = A_1Q_8'$
$K_{A2} = Q_1$

$J_{A4} = Q_1Q_2$
$K_{A4} = Q_1Q_2$

$J_{A18} = Q_1Q_2Q_4$
$K_{A8} = Q_1$

- b) D flip-flop

Present state				Next State				JK flip-flop			
Q_8	Q_4	Q_2	Q_1	A_8	A_4	A_2	A_1	D_8	D_4	D_2	D_1
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	0	0	0	0	0	0	0	0

$D_1 = Q_1'$
$D_2 = \sum(1, 2, 5, 6) = Q_2Q_1' + Q_8'Q_2'Q_1$
$D_4 = \sum(3, 4, 5, 6) = Q_4Q_1' + Q_4Q_2' + Q_4'Q_2Q_1$
$D_8 = \sum(7, 8) = Q_8Q_1' + Q_4Q_2Q_1$

Dont cares $= \sum(10, 11, 12, 13, 14, 15)$

Simplifying with K-maps

D_2) $D_2 = \sum(1, 2, 5, 6) = Q_2Q_1' + Q_8'Q_2'Q_1$

	00	01	11	10
00		1		1
01		1		1
11	x	x	x	x
10			x	x

$= Q_2Q_1' + Q_8'Q_2'Q_1$

D_4) $D_4 = \sum(3, 4, 5, 6) = Q_4Q_1' + Q_4Q_2' + Q_4'Q_2Q_1$

	00	01	11	10
00			1	
01	1	1		1
11	x	x	x	x
10			x	x

$= Q_4Q_2' + Q_2Q_1Q_4' + Q_4Q_1'$

D_8) $D_8 = \sum(7, 8) = Q_8Q_1' + Q_4Q_2Q_1$

	00	01	11	10
00				
01			1	
11	x	x	x	x
10	1		x	x

$= Q_1'Q_8 + Q_4Q_2Q_1$

- c) Determine the most effictive of the three designs

Equation using T flip flops

$TQ_1 = 1$
$TQ_2 = Q_8'Q_1$
$TQ_4 = Q_2Q_1$
$TQ_8 = Q_8Q_1 + Q_4Q_2Q_1$

Equation Using D flip flops

$D_1 = Q_1'$
$D_2 = Q_2Q_1' + Q_8'Q_2'Q_1$
$D_4 = Q_4Q_1' + Q_4Q_2' + Q_4'Q_2Q_1$
$D_8 = Q_8Q_1' + Q_4Q_2Q_1$

Equations JK flip-flop Ipmlentation

$J_{A1} = 1$
$K_{A1} = 1$

$J_{A2} = A_1Q_8'$
$K_{A2} = Q_1$

$J_{A4} = Q_1Q_2$
$K_{A4} = Q_1Q_2$

$J_{A18} = Q_1Q_2Q_4$
$K_{A8} = Q_1$

In this case the logic of the **T flip-flops is the easiest.** Using T flip-flops will be the fastest and has fewer delays and power consumption. **T flip-flop is the most efficient**

6.A0

6.A0 Útfærið taktvísan (e. syncrounus) binary counter sem hefur talnaröðina :

0-2-4-6-8-10-12-14.

- Þegar teljarinn fer upp í 14 á hann að fara í 0 á næsta klukkupúls.
    - Útgangurinn Y á að vera 1 þegar teljarinn er í 6 og 12.
- Notist við D-Vippur.

6.A0 Lausn

- Step 1/2

To implement the binary counter in sync with the given sequence of numbers, you need a 4-D flip-flop because you need to count up to 14 (which requires 4 bits).

The binary equivalent of the sequence is

- 0000
- 0010
- 0100
- 0110
- 1000

- 1010
- 1100
- 1110

Explanation:

To change from 14 to 9, we have to reset the first and second bits and increment the third bit. The fourth bit stays the same. Binary equal to 9 is 1001, so the next state after 1110 (14) should be 1001 (9).

The output **Y should be 1 when** the counter is at 6 (0110) and 12 (1100). Therefore, we can use an **AND gate** with inputs from the third and fourth flip-flops to generate the output.

Explanation:

Where (Q3,Q2,Q1,Q0) is the current state, (Q3,Q2,Q1,Q0)' is the next state, 1 is the time pulse, and Y is the output.

Current State	Next State	D3	D2	D1	D0	Y
0000	0001	0	0	0	1	0
0001	0010	0	0	1	0	0
0010	0011	0	0	1	1	0
0011	0100	0	1	0	0	0
0100	0101	0	1	0	1	0
0101	0110	0	1	1	0	0
0110	0111	0	1	1	1	1
0111	1000	1	0	0	0	0
1000	1001	1	0	0	1	0
1001	1010	0	1	1	0	0
1010	1011	1	0	1	0	0
1011	1100	1	1	0	0	0
1100	1101	1	1	0	1	1
1101	1110	1	1	1	0	0

Explanation: The current state is represented by D flip-flops and the next state is generated by a combinational circuit based on the current state and the input.

To implement the circuit, we can use four D flip-flops connected as a binary counter and a 4-input AND gate to produce the Y output. We also need a 2-input MUX to select the next state based on the registration.