

# VINCIT: UMA Case Study (Codename Sparta)

## Operational Definitions of Global Non-Reconstructibility ( $\neg$ Rec) and Empirical Validation on Unified Memory Architecture (v1206)

**Author:** V. Loventre (Codename: Cronos) **Target Architecture:** Apple Silicon M1 (SoC Unified Memory) **Date:** January 23, 2026 **Version:** 1206 (Scientific Release) **DOI:** 10.5281/zenodo.18363521

### ABSTRACT

#### The Grammar of the Global and the "Sparta" Ground Truth

This work defines a mathematical grammar for information systems whose global structure cannot be deduced from the sum of their local parts. Contrary to reductionist approaches, the Loventre System (v1206) postulates the existence of primitive geometric properties — configuration space (**C**), basins (**B**), and barriers (**B\_bar**) — that constrain computation before it even occurs.

This operational model finds its validation in the "Gold Run" experimental session, conducted on Unified Memory Architecture (SoC M1, codename "Sparta"). Tests indicate that the principle of Global Non-Reconstructibility ( $\neg$ Rec) is not merely an algorithmic hypothesis, but a physical constraint measurable in the system's behavior under stress.

Key findings of the v1206 certification include:

- Bus ABS (49.81 GB/s):** Proof that global accessibility ( $\rightarrow$ ) has an impassable physical asymptote.
- P-like Resilience:** The system's ability to maintain structural coherence even under saturation, provided geometric accessibility constraints are respected.

## PART I: OPERATIONAL MODEL AND INFORMATION GEOMETRY

### 1.1 The Configuration Space (C)

We define **C** not as a set of memory addresses, but as the topological space of all possible permutations of the system state. In this space, distance is not measured in bytes, but in "access cost."

### 1.2 The Information Basin (B)

A Basin is a subset of  $C$  where the transition cost between two states is negligible (CPU L1/L2 Cache). It represents a region of "local linearity" where computation is predictable.

### 1.3 The Barrier ( $B_{\text{bar}}$ )

The Barrier is the geometric limit where the cost of fetching information exceeds the energy required to process it. In the M1 architecture, this coincides with the physical saturation of the Fabric Interconnect (the transition from RAM to Swap/SSD).

---

## PART I-BIS: FOUNDATIONS OF COMPUTATIONAL THERMODYNAMICS

### 1.4 The Von Neumann Entropy Limit

We introduce the thermodynamic variable  $S$  (Entropy) applied to the computational bus. When the throughput approaches the **ABS (Asymptotic Bus Saturation)** limit, the system entropy diverges. The bus is no longer a neutral channel; it becomes an active variable in the equation.

### 1.5 The Collapse of Determinism

Approaching the Barrier  $B_{\text{bar}}$ , the system undergoes a phase transition. The time required to retrieve a specific bit becomes non-deterministic due to contention queues. In this regime, the system behaves like a **Black Hole** for information: requests enter, but the retrieval time tends toward infinity relative to the CPU clock cycle.

---

## PART II: EMPIRICAL VALIDATION (THE "GOLD RUN")

### 2.1 Methodology

The "Sparta" testbench subjected the Apple Silicon M1 SoC to a progressive stress test, forcing the allocation of **20 GB** of protected memory (Wired Memory) to trigger the intervention of the Swap compressor.

### 2.2 Telemetry Results

The "Gold Run" produced the following certified metrics:

- **Peak Throughput: 49.81 GB/s** (The ABS Wall).
- **Swap Usage: 0 bytes** (During the coherence phase), proving the stability of the kernel scheduler.
- **Thermal Throttling:** Not observed. The constraint was purely geometric (bandwidth), not thermal.

### 2.3 Phenomenological Observation

At the exact moment of maximal density, the system exhibited "micro-freezes" (jitter). These are not errors, but the physical manifestation of the **Event Horizon** of the bus. The CPU is waiting for data that physics cannot deliver faster than the speed of light allows through the silicon interconnect.

---

## SECTION 17: THE ANNIHILATION PROTOCOL

### 17.1 Procedure

At the conclusion of the Gold Run, the operator "Cronos" executed the atomic sequence:

1. **Logical Termination (killall):** Instantaneous arrest of processes and sockets.
2. **Physical Deletion (rm -rf):** The **20 GB** of generated "Matter" were not archived; they were destroyed. The data existed only in the instant of transit.
3. **Synchronization (sync):** Forced flushing of buffers.

### 17.2 The Meaning of Absence

With the execution of this protocol, the "Cathedral of Logic" is dismantled. No residue remains. Only the **Ground Truth Log** remains. This act confirms that the Loventre System is not the set of files on the disk, but the set of geometric laws that governed them. The files may disappear, but the Axiom remains true.

---

## CONCLUSION AND PROSPECTS: GENERATIVE INVERSION

**From Obstruction to Resource** The data certifies that the Barrier **B\_bar** is not just a limit, but a resource. The deterministic identification of an **NP-Blackhole** regime allows for **Generative Inversion**.

**Chaos Harvesting** If the system can recognize a zone of "computational silence" where information is not reconstructible ( $\neg \text{Rec}$ ), it is theoretically possible to exploit this zone as a source of **certified high-quality entropy** for Post-Quantum cryptographic key generation.

With the Gold Run of January 23, 2026, the VINCIT framework ceases to be merely a monitoring hypothesis and becomes a validated platform for the study of limiting geometries in silicon.

---

## APPENDIX A: OPERATIONAL DEFINITIONS (Summary)

- **$\kappa$  (Kappa):** Structural Resistance (Allocation Latency / CPU Cycles).
- **H (Entropy):** Data Dispersion (Page Faults + Swap I/O).
- **B (Barrier):** Physical Boundary RAM/SSD (**20 GB, 49.81 GB/s**).

