Computer Architecture Final Project

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1 Git Repository

`https://github.com/hurryingauto3/Pipelined-RISC-V-Processor`

2 Status

a) All instructions in single cycle processor are working fine: **True**
b) Single Cycle processor is correctly executing bubble sort algorithm: **False**
c) All instructions are working fine in the pipelined processor: False: **False**
d) Hazard detection is working fine in the pipelined processor: False: **False**
e) Stall circuitry is working fine in the pipelined processor: False: **False**
f) Pipelined processor is correctly executing bubble sort algorithm: False: **False**

3 Explanation

The RISC V Processor is functioning correctly and executing all the pre-present commands however we were unable to branch. The BEQ command only worked if we didn't invert the Zero wire and the BGT command only worked if we invert the Zero wire.

Project was unable to be completed due to the multiple other deadlines that are larger than 30 percent of those grades.