Lab 5

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Semester II (2017)

1 Latches and Flip Flops

Design a gated S-R flip-flop (latch) Circuit with the following properties:

- This circuit allows inputs to affect the outputs only when $C = 1$
- When $C = 0$, the latch holds the last state value at its output
- Extra Credit: Draw ASM (Algothrmic State Machine) for set dominant S-R flip-flop. Hint: "Set dominat" means illegal state gives an output of 1.