UNIVERSITY OF DUBLIN
TRINITY COLLEGE

Faculty of Engineering, Mathematics and Science

School of Computer Science & Statistics

Integrated Computer Science Programme **Trinity Term 2014**

CS1026 – Digital Logic Design

Monday, 28th April 2014 **Sports Centre** **14:00 - 17:00**

Prof. John Waldron and Dr. Eoin Creedon

Instructions to Candidates

You must answer TWO questions from Section A and TWO questions from Section B.

Please answer Section A and Section B in separate answer booklets.

Each question is worth 25 marks.

Permitted Materials

Non-programmable calculators are permitted for this examination. Please indicate the make and model of your calculator on the front of your first answer book.

Section A

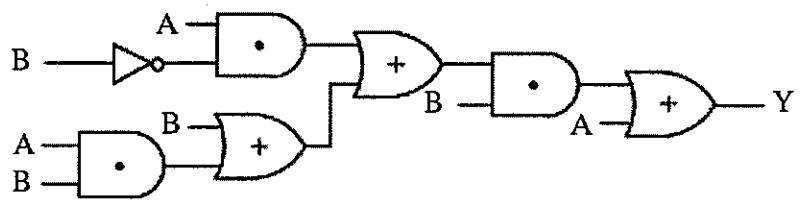
1. (a) Write down the truth table of an Exclusive OR gate. Draw the traditional symbol for an EOR gate. (5 marks)

   (b) Draw a circuit diagram to show how an Exclusive OR gate can be constructed using only four NAND gates. (10 marks)

   (c) Write down the truth table for a half adder and draw a circuit to implement it using an Exclusive OR gate and an AND gate. (10 marks)

2. (a) Write down the truth table of a NAND gate. Draw a circuit diagram showing a CMOS implementation of a 2-input NAND gate that uses four transistors. (5 marks)

   (b) Write down a boolean expression for the circuit shown below. Using the theorems of boolean algebra find and draw the simplest circuit that implements the function Y.



   (10 marks)

   (c) Find the minterms of the following boolean expression by first plotting it on a karnaugh map

   wyz + w'x' + wxz' (10 marks)

3. (a) Write down the truth table for a two to four line decoder with active low enable and active low outputs. (5 marks)

   (b) Draw a circuit to implement a two to four line decoder with active low enable and active low outputs using only inverters and NAND gates. (10 marks)

   (c) Draw a circuit that implements a full adder using only a decoder and external OR gates. (10 marks)

Section B

1. (a) Explain *positively* edge triggered and *negatively* edge triggered flip-flops. (4 marks)

   (b) Explain the terms *setup time* and *hold time* in relation to flip-flops. (6 marks)

   (c) Discuss Algorithmic State Machines, including details on the symbols that make up a typical ASM diagram. (10 marks)

   (d) Describe and discuss *self starting* counters. (5 marks)

2. Using Quine-McCluskey create the minimal circuit which will identify if a user input number is a prime number or not, in the range 2 to 63. The circuit should output a 1 if the number is prime and a zero otherwise. Prime numbers are numbers which are divisible only by themselves or 1. **Use of any other method will attract no marks.** (25 marks)

3. (a) List the excitation table of a *JK* flip-flop. (5 marks)

   (b) Use *JK* flip-flops to design the logic for a synchronous counter that counts in the following sequence:

   0, 1, 3, 2, 6, 7, 5, 4

   The counter should return to 0 after it reaches 4. Verify that the counter is self starting. (20 marks)