CS1026 – Digital Logic Design

Episode 2

Alistair Morris [1]

[1]Distributed Systems Group
Trinity College Dublin

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Today's Overview

When and where things happen?

- Lectures and Tutorials
  - As on timetable
- Labs once a week
  - Starting on 2^{nd} week
  - Continual Individual Assessment!
    1. You check labs set a week beforehand
    2. Simulate/build and document
    3. Show and *explain* findings to a TA
    4. E-Mail me *PDF* by *23:59* on Friday

Submission by E-Mail

PDF only to *morrisa5@scss.tcd.ie* (Me)

- Put Module Code (CS1026) in Subject
- Student Code somewhere in PDF docs
- Make sure you attach PDF! ;-)

Late Submissions

- Not possible
- Awarded 0 marks

About groups

- Labs and tutorials split into groups
  - Maximise contact time
- Groups (Surnames)
  1. A – H
  2. I – P
  3. Q – Z
- Play Fair – *Keep to your groups*
  - Times at: bitbucket.com/morrisa5/DLD/timetable.pdf

Keeping in Touch

Course run by 3 people

- Lecturer
  - Alistair Morris
  - *morrisa5@scss.tcd.ie*
- TA.1
  - Derek
- TA.2
  - Shane

Gaining Marks

- Marks split between Exam and Coursework
- Labs make up coursework mark
  - 0–3 Marks awarded by TA for showing at lab
  - 0–3 Marks awarded by me for PDF docs
  - Product of marks taken as %
  - 1 Mark added for "Wow factor"
- Average (mean) taken over term

Example

- Good Student: $\frac{2\times3+1}{100}\% = 70\%$ (First Class)
- Silly Student: $\frac{3\times0+0}{100}\% = 0\%$ (Epic Fail)

Marking Scheme

For 0 marks

Easy – Don't turn up/submit

For 1 mark

Attempted but student has poor understanding

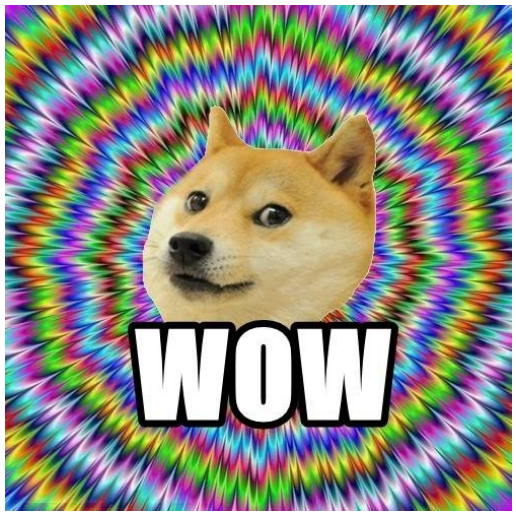
For 2 marks

Attempted and student has some understanding

For 3 marks

Completed and student has *full* understanding

Wow Factor



- Based on PDF submitted
- *Shows* exemplary understanding
  - Even if you made mistakes
  - Hint: *Write your working!*

What we expect in the docs

A PDF one-pager containing:

1. The answers
2. All of your working and explanation
3. Diagrams/description of solution

A note about diagrams

- Please embed in PDF
- Use a CAD tool (e.g. Logisim)
  - I.e. No scans unless you *can* draw!
  - It's quicker/more fun!

But what about attendance?

- Turn up for marks!
  - and so you know what to do! ;-)
- No class registers
  - You take responsibility!

Feedback

CSV at: bitbucket.com/morrisa5/DLD/feedback.csv

- Updated Weekly
- Displays only Student No.

TAs will also give you tips

- They look for marks
- React to these
  - For full marks in docs

Can I skip Labs, resubmit Labs, etc.

NO, NEIN, etc. *

- * – with exceptions
  - e.g. Illness, Deadline Conflicts, etc.

Remember

- The TA will give you tips in Lab
- React to these for *full marks* in doc

Themes

1. Boolean Algebra, Functions, and Minimisation
2. Analysing Combinational Logic Circuits
3. Introduction to Feedback Circuits
4. Sequential Circuit Design
5. Finite State Machine Optimisation
6. Verilog Hardware Description Language (Verilog)
7. VHDL Hardware Description Language (VHDL)
8. Commercial Digital Integrated Circuits

Extra course material

- No recommended book for course
  - A reference section details Papers, Book Chapters, etc.
  - Not compulsory but could help
- All content found in slides, tutorials, etc.
  - Tutorial and lab problems similar to exam

Wikipedia health warning

- An excellent resource to get basics
- BUT it can go off on tangents!

That's it (for now)

Thanks.. Any Questions?

You can ask later at:

morrisa5@scss.tcd.ie

Useful links

- Notes/Slides: bitbucket.com/morrisa5/dld
- LinkedIn: ie.linkedin.com/in/alistair-morris-9712b247

References (Homework) I

Useful references will usually go here!