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09/03/2017

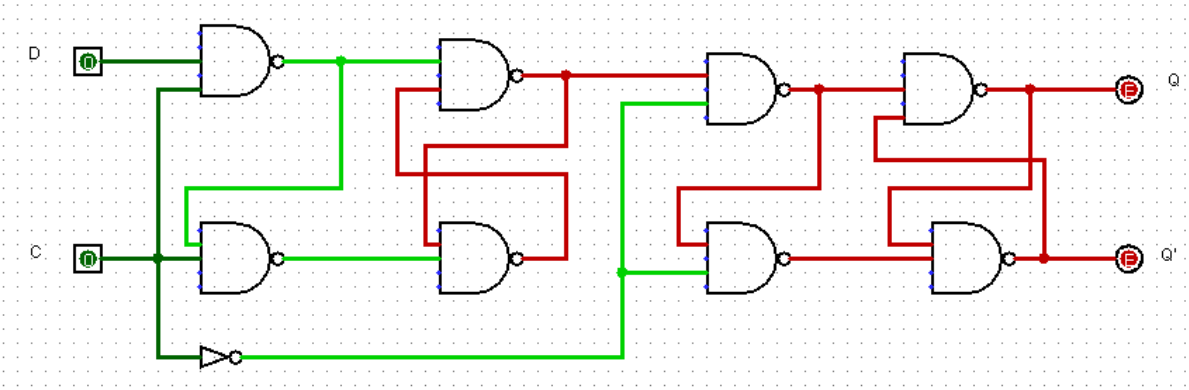
LAB 6 WRITE UP

Title: CS1026 Lab 6

Date: 09/03/2017

Aim:

- To design a negatively edged triggered D Flip Flop circuit
- To draw the Present-State/Next-State Table for a JK Flip Flop
- To draw an Algorithmic State Machine for a JK Flip Flop



Analysis:

- I began by drawing the PS/NS table for a negatively edged D Flip Flop circuit
- I then designed and tested the above circuit to ensure it matched the table
- I then drew the PS/NS table for a JK Flip Flop using the lecture notes
- From this table I then drew an Algorithmic State Machine diagram for a JK Flip-Flop

JK Flip Flop PS/NS Table:

J	K	Q	Q’	Comment
0	0	Q	Q’	Hold State (null)
0	1	J	K	J and K different, Q takes J
1	0	J	K	J and K different, Q takes J
1	1	Q’	Q	Invert States Q and Q’

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Algorithmic State Machine (ASM) for JK Flip Flop: