Lab 7

Shane Sheehan
sheehas1@scss.tcd.ie

Semester II (2017)

1 Algorithmic State Machines I

Design a synchronous sequential circuit called "Div-by-3".

- Give an output Z that divides a system clock frequency f CLK by 3.
- Assume a duty cycle of two-thirds (2 CLK cycle high, 1 cycle low).
- Design the circuit using JK flip-flops.

E-Mail to Sheehan1@tcd.ie by Sunday 23:59