

CS1026 – Digital Logic Design

Last one – Inspection Design Methods

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Today's Overview

1 Classical Design

2 Example 1

3 Example 2

4 Q&A

Limitations with Classical Design I

We can only use the classical design method with:

- A small number of inputs
- States
- Outputs

The K-maps required become too difficult to draw and work with.

Limitations with Classical Design II

The Inspection Design Method provides ways to write the excitation equation using:

- A timing diagram
- A state diagram
- A ASM chart

For a synchronous Finite State Machine.

Limitations with Classical Design III

By observing or inspecting the present state (PS) and next state (NS) for each state variable:

- We can write the D , T and $J - K$ excitation equations

The equations derived using inspections do not give minimum equations however.

Limitations with Classical Design IV

We have two inspection methods:

- 1 The Set-Hold 1 Method
- 2 Clear-Hold 0 Method

Limitations with Classical Design V

We use the following table to write D excitation equations directly from a state diagram, ASM chart or timing diagram.

| Present State (PS/NS) Y_i Y_i^+ | | D_i | Comment | User for 1s (Set-Hold 1) | Use for 0s (Clear-Hold 0) |
|-------------------------------------------|---|-------|-------------------|-----------------------------|------------------------------|
| 0 | 0 | 0 | Hold 0 transition | | D_i' |
| 0 | 1 | 1 | Set transition | D_i | |
| 1 | 0 | 0 | Clear transition | | D_i' |
| 1 | 1 | 1 | Hold 1 transition | D_i | |

Limitations with Classical Design VI

The “Set-Hold 1 Method” obtains the D excitation equations for the 1s of each state variable (flip-flop outputs):

- $$D_i = \sum(\text{PS.external input conditions for set}) + \sum(\text{PS.external input conditions for hold 1}) \text{ for } i = 1, 2, 3, \dots$$

Limitations with Classical Design VII

The “Set-Hold 0 Method” can be used to obtain the D excitation equations for the 0s of each state variable (flip-flop outputs)

- $D_i = \sum(\text{PS.external input conditions for clear}) + \sum(\text{PS.external input conditions for hold 0})$ for $i = 1, 2, 3, \dots$

Limitations with Classical Design VIII

For both of the methods:

- If we have not completely specified FSM meaning and some state values as dont cares
 - Enter them as such so that we can use them in later reduction

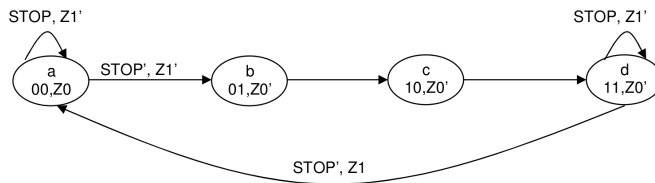
Simple Example I

Obtain the excitation equations for the following state diagram of a Mixed Moore-Mealy machine:

- State – Y_1Y_2
- Input – STOP
- Output – Z_0Z_1

Simple Example II

Our state chart:



Simple Example III

By inspecting all state transitions ($Y1 = 0 \implies Y1^+ = 1$) and all Hold 1 transitions ($Y1 = 1 \implies Y1^+ = 1$):

- We can write the D1 excitation equation:

$$\blacksquare D1 = Y1'.Y2 + Y1.Y2' + Y1.Y2.STOP$$

Simple Example IV

Now repeat the previous step for D2 using Y2 transitions..

- By observing (or inspecting) all transitions
($Y2 = 0 \implies Y2^+ = 1$) and all Hold 1 transitions
($Y2 = 1 \implies Y2^+ = 1$)
 - We can write the D1 excitation equation:
$$D2 = Y1'.Y2'.STOP' + Y1.Y2' + Y1.Y2.STOP$$

Simple Example V

Alternatively..

We could also look for the 0s function using Clear-hold 0 method to find $D1'$ and $D2'$

Simple Example VI

Based on the state diagram Z0

- We see that we have a Moore-type output
 - It only depends on the state variables (flip-flop outputs)

Simple Example VII

| | | Y2 | |
|----|---|----|---|
| | | 0 | 1 |
| Y1 | 0 | 1 | 0 |
| | 1 | 0 | 0 |

$$Z0 = Y1'.Y2'$$

We will use a K-map with state variables to find minimized the $Z0$ equation

Simple Example VIII

Z_1 is a Mealy-type output since it depends on both the state variables and external input

| | | | | | |
|------|---|-------------------------------|----|----|----|
| | | Y ₁ Y ₂ | | | |
| | | 00 | 01 | 11 | 10 |
| STOP | 0 | 0 | 0 | 1 | 0 |
| | 1 | 0 | 0 | 0 | 0 |

$$Z_0 = Y_1 \cdot Y_2 \cdot \text{STOP}'$$

Again we use a K-map with state variables plus external input to find minimize Z_1 equation

Real World Example I

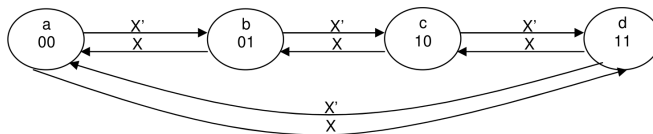
A question

Design a synchronous 2-bit Binary up down counter that counts up when input signal $X = 0$ and counts down when input signal $X = 1$

- State – Y_1Y_2
- Input – X

Real World Example II

The state chart:



Real World Example III

Use the *Set Clear Method* to obtain the J-K excitation equations for the 1s of each state variable (flip-flop outputs):

- By observing all the sets ($Y1 = 0 \implies Y1^+ = 1$), we can write the J1 excitation equation:

- $J1 = Y1'.Y2.X' + Y1'.Y2'.X = Y2'.X + Y2.X'$

Real World Example IV

Also..

- By observing all the clears ($Y1 = 1 \implies Y1^+ = 0$), we can write the K1 excitation equation:

- $K1 = Y1.Y2'.X + Y1.Y2.X' = Y2'.X + Y2.X'$

Real World Example V

Now we repeat this for the second Flip Flop:

- By observing all the sets ($Y2 = 0 \implies Y2^+ = 1$), we can write the J2 excitation equation:

- $$J2 = Y1'.Y2'.X' + Y1'.Y2'.X + Y1.Y2'.X' + Y1.Y2'.X = Y1'.Y2' + Y1.Y2' = Y2'$$

Real World Example VI

Finally:

- By observing all the clears ($Y2 = 1$ $Y2 = 0$), we can write the $K2$ excitation equation:

$$\begin{aligned} \blacksquare K2 &= Y1'.Y2.X' + Y1'.Y2.X + Y1.Y2.X' + Y1.Y2.X = \\ &Y1'.Y2 + Y1.Y2 = Y2 \end{aligned}$$

References (Homework) I