Coláiste na Tríonóide, Baile Átha Cliath
Trinity College Dublin
Ollscoil Átha Cliath | The University of Dublin

Faculty of Engineering, Mathematics and Science

School of Computer Science & Statistics

Integrated Computer Science Programme **Trinity Term 2016**
Year 1 Annual Examinations

CS1026 – Digital Logic Design

Wednesday 11th May 2016 **RDS Main Hall** **14:00 – 17:00**

Prof. John Waldron and Mr. Alistair Morris

Instructions to Candidates:

You must answer TWO questions from Section A and TWO questions from Section B. Each question is worth 25 marks. Please answer Section A and Section B in separate answer booklets. You may not start this examination until you are instructed to do so by the Invigilator.

Materials permitted for this examination:

Non-programmable calculators are permitted for this examination — please indicate the make and model of your calculator on each answer book used.

Section A

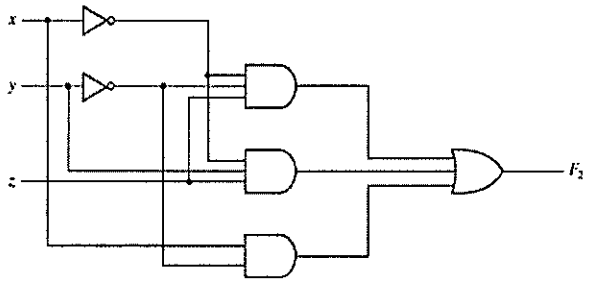
1. (a) Write down the truth table of an Exclusive OR gate. Draw the traditional symbol for an Exclusive OR gate. (5 marks)

   (b) Draw a circuit diagram to show how an Exclusive OR gate can be constructed using only four NAND gates. (10 marks)

   (c) Write down the truth table for a half adder and draw a circuit to implement it using an Exclusive OR gate and an AND gate. (10 marks)

2. (a) Write down the idempotent rules of Boolean algebra, derived from the combination of a single variable with itself. (5 marks)

   (b) Write down a boolean expression for the circuit shown below. Using the theorems of boolean algebra find and draw the simplest circuit that implements the function F_2.



   (10 marks)

   (c) Simplify the function

   F(A, B, C, D) = AC'D' + A'C + ABC + AB'C + A'C'D'

   using a Karnaugh map and draw the resulting circuit. (10 marks)

3. (a) Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. x is the most significant bit and z the least. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

   Write down the truth table for the circuit. (7 marks)

   (b) Your solution should show a Karnaugh map, a boolean function and a circuit diagram for each of the three outputs. (18 marks)

Section B

4. (a) Explain *positively* edge triggered and *negatively* edge triggered flip-flops.

(5 marks)

(b) Demonstrate how a SR Flip Flop can implement a bi-stable memory device (also referred to as a latch).

(5 marks)

(c) Give the Present-State/Next-State (PS/NS) Table for a SR Flip Flop and its corresponding Karnaugh Map.

(10 marks)

(d) Give the Algorithmic State Machine (ASM) for a SR Flip Flop.

(5 marks)

5. Using Quine-McCluskey create the minimal circuit which will implement the boolean function: $F(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$.
Note: The use of any other method will attract no marks.

(25 marks)

6. Build a 2-bit binary up-counter with a Ripple Carry Output (RCO) using JK flip-flops. Hint: You should use the Seven-Step Classical Design Process for Synchronous Sequential Digital Circuits.

(25 marks)