

CS1026 – Digital Logic Design

Sequential Logic Analysis

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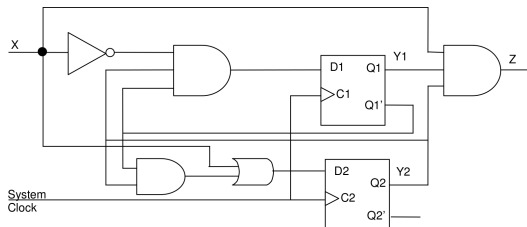
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Today's Overview

- 1 Method of analysing sync circuits
- 2 Applying the five step analysis technique
- 3 A useful book

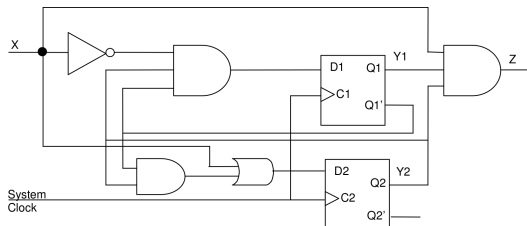
Analysing Sync Circuits [Nelson et al., 1995] I



We can use Flip Flops to work out how a Synchronous circuit works

- How does it behave?

Analysing Sync Circuits [Nelson et al., 1995] II



Assign a present state variable to each flip flop in the system.

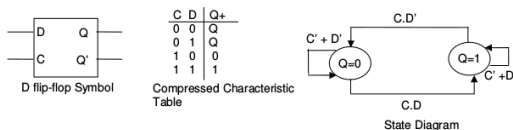
- Y_i represents flip-flop outputs for $i = 1, 2, 3, \dots$

Analysing Sync Circuits [Nelson et al., 1995] III

Write the excitation-input equation for each of the flip-flops and the external-output (Moore and/or mealy equations).

- After completing this step, we define D_i , J_i , K_i , T_i where $i = 1, 2, 3 \dots$
 - This denotes the number of flip-flops used

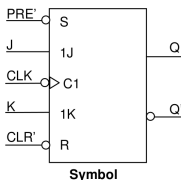
Analysing Sync Circuits [Nelson et al., 1995] V



For D flip-flops:

- $Y_i = D_i$ for $i = 1, 2, 3, \dots$

Analysing Sync Circuits [Nelson et al., 1995] VI



Characteristic Table

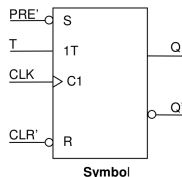
J	K	Q ⁺	Comment
0	0	Q	no change
0	1	0	reset condition
1	0	1	set condition
1	1	Q'	toggle

Characteristic equation: $Q^+ = J \cdot Q' + K' \cdot Q$

For J-K flip-flops:

■ $Y_i = J_i \cdot Y_i' + K_i' \cdot Y_i$ for $i = 1, 2, 3, \dots$

Analysing Sync Circuits [Nelson et al., 1995] VII



Characteristic Table

T	Q*	Comment
0	Q	no Change
1	Q'	toggle

Characteristic equation: $Q^* = T'.Q + T.Q'$

Also for T flip-flops

■ $Y_i = T_i \oplus Y_i$ for $i = 1, 2, 3, \dots$

but we don't see these much now!

Analysing Sync Circuits [Nelson et al., 1995] VIII

Y1	Y2	X	Y1 ⁺	Y2 ⁺	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	0	1	1

Obtain a Present State (PS) /Next State (NS) table (or a composite K-map) using the next state and external-out equations

- Separate K-maps can be used for the external outputs!

Analysing Sync Circuits [Nelson et al., 1995] IX

Y1	Y2	X	Y1 ⁺	Y2 ⁺	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	0	1	1

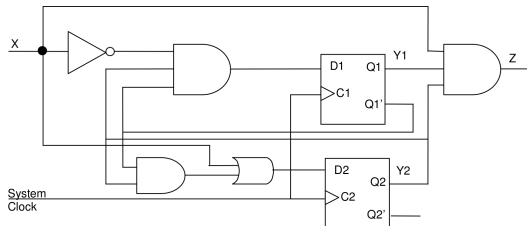
Use the PS/NS table or the K-map to obtain a state diagram

- Then we can draw ASM chart or timing diagram to show the behavior of the circuit

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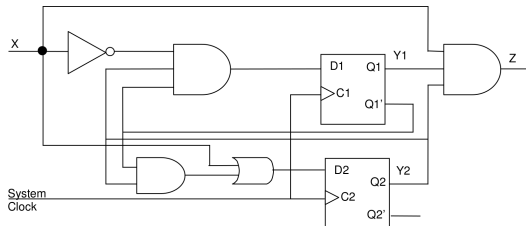


An example II



Note: We have a Mealy-type machine since the output depends on external input and flip-flop outputs.

An example III



Assign a present state variable to each flip flop in the synchronous system. Y_i representing flip-flop outputs for $i = 1, 2, 3, \dots$

Hint

Refer to the schematic!

An example IV

Write the excitation-input equation for the flip-flops and the equation for the external-output (Moore and/or mealy equations). After this step is completed, the values of D_i , Z should be defined for all flip-flops:

- $D1 = X'.Y1'.Y2$
- $D2 = Y1'.Y2 + X$
- $Z = Y1.Y2.X$

An example V

Substitute the excitation-input equation into the characteristic equations for the flip-flops to obtain the *next state* equations.

- Remember for D flip-flops:

- $Y_i = D_i$ for $i = 1, 2, 3, \dots$
- $Y1 = D1 = X'.Y1'.Y2$
- $Y2 = D2 = Y1'.Y2 + X$

An example VI

PS/NS Table

Y1	Y2	X	Y1 ⁺	Y2 ⁺	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	0	1	1

OR

Composite K-map where:

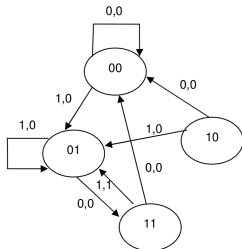
→ Ys and Xs are independent variables

→ Ys⁺ and Zs are Dependent

		X	
		0	1
Y ₁ Y ₂	00	00,0	01,0
	01	11,0	01,0
	11	00,0	01,1
	10	00,0	01,0
		Y ₁ ⁺ Y ₂ ⁺ .Z	

Obtain a PS/NS table or a composite K-map using the next state and external-output (Mealy and/or Moore) equations. Separate K-maps can also help with the external outputs.

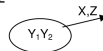
An example VII



Classic State machine

- * Links show input, output in 1s and 0s
- * State is inside the circles

Legend

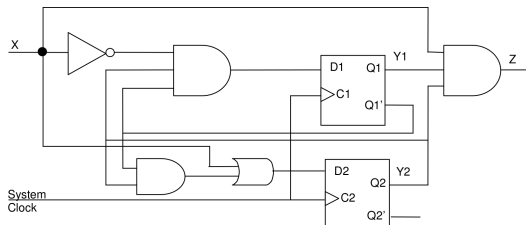


Notes

- 1) State 00 is reset
- 2) Output Z=1 only when the input sequence is 101, so this could be "101" pattern detector.
- 3) State "10" is referred to as "illegal state", "unused state" or an "unreachable state".
- 4) One way to ensure you don't end up in illegal state is to have a power on reset.

Use the PS/NS table or the composite K-map to obtain a state diagram to show the behavior of the circuit.

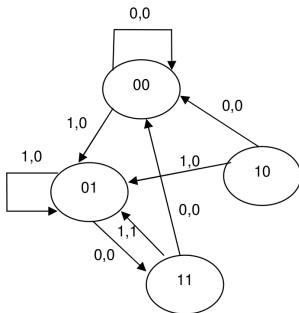
An example VIII



Note

Since we have two flip-flops, the state machine has 4 states.

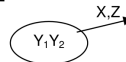
An example IX



Classic State machine

- * Links show input, output in 1s and 0s
- * State is inside the circles

Legend



Notes

- 1) State 00 is reset
- 2) Output Z=1 only when the input sequence is 101, so this could be "101" pattern detector.
- 3) State "10" is referred to as "illegal state", "unused state" or an "unreachable state".
- 4) One way to ensure you don't end up in illegal state is to have a power on reset.

An example X

In the case of Moore machines, we put outputs inside the circle:

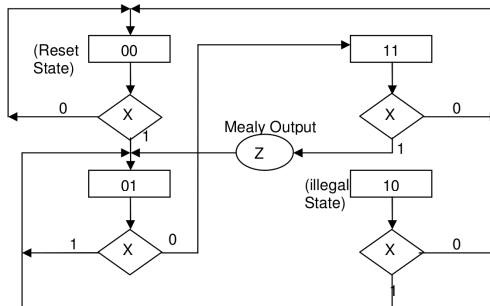
- They only depends on the current state

This constitutes a simplified State machine

It shows the links between states in Boolean expressions.

An example XI

An Algorithmic State Machine (ASM) also describes the functionality:



Note: When Z is not shown, it is assumed the output is 0.

References (Homework) I



Nelson, V. P., Nagle, H. T., Carroll, B. D., and Irwin, J. D.
(1995).

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