BRANDON DOOLEY (#16327446)
03/04/2017

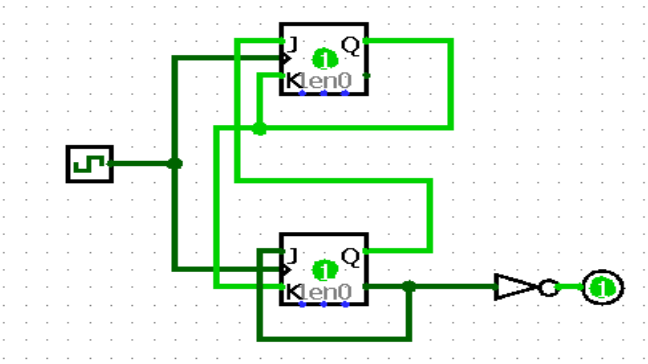
LAB 7 WRITE UP

Title: CS1026 Lab 7

Date: 03/04/2017

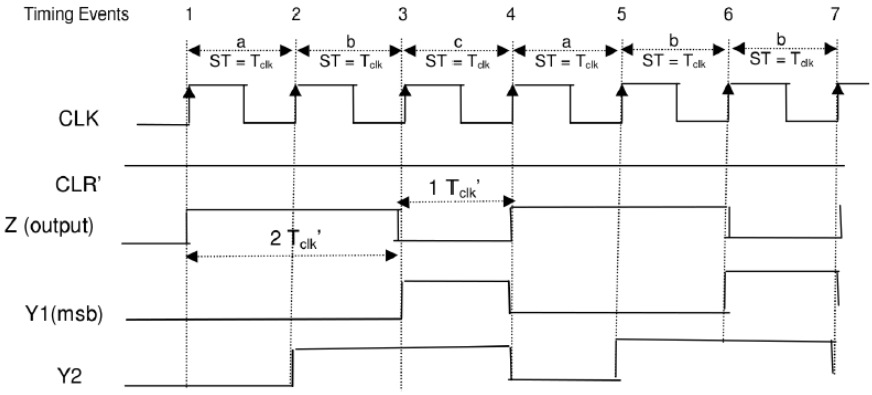
Aim:

- To design a synchronous sequential circuit that divides a system clock frequency *f* CLK by 3 using JK Flip-Fops



Analysis:

- I began by drawing the CLK timing diagram for the desired circuit
- I then drew the *Characteristic Table* for a JK Flip-Flop
- From this I devised the *Output Excitation Table* for a JK Flip-Flop
- I then also devised the *Input Excitation Table* for a JK Flip-Flop
- Using the above tables I then created 3 Karnaugh Maps that I then used to come up with a solution Z for the system



BRANDON DOOLEY (#16327446)
03/04/2017

LAB 7 WRITE UP

JK Flip Flop Characteristic Table:

J	K	Y+
0	0	Y
0	1	0
1	0	1
1	1	Q'

Output Excitation Table for JK Flip Flop:

J	K	Y+
0	0	Y
0	1	0
1	0	1
1	1	Q'

Input Excitation Table for JK Flip Flop:

Y	Y+	J	K
0	0	0	-
0	1	1	-
1	0	-	1
1	1	-	0

K Map for System:

Y1	Y2	Y1+	Y2 +	J1	K1	J2	K2	Z
0	0	0	1	0	1	1	0	1
0	1	1	1	1	0	1	0	1
1	1	0	0	0	1	0	1	0
1	0	-	-	-	-	-	-	-