TRINITY COLLEGE DUBLIN
THE UNIVERSITY OF DUBLIN

Faculty of Engineering, Mathematics and Science

School of Computer Science & Statistics

Integrated Computer Science Programme **Trinity Term 2015**
Year 1 Annual Examinations

CS1026 – Digital Logic Design

Monday, 27th April 2015 **Sports Centre** **14:00 - 17:00**

Prof. John Waldron and Dr. Eoin Creedon

Instructions to Candidates

You must answer TWO questions from Section A and TWO questions from Section B.

Please answer Section A and Section B in separate answer booklets.

Each question is worth 25 marks.

Permitted Materials

Non-programmable calculators are permitted for this examination. Please indicate the make and model of your calculator on the front of your first answer book.

Section A

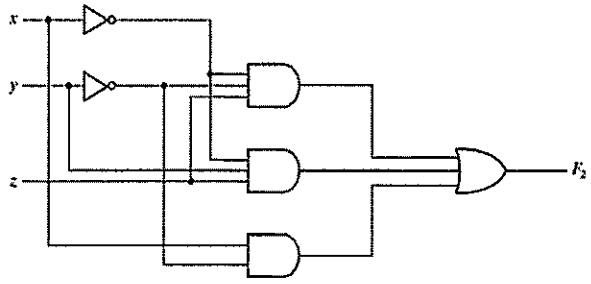
1. (a) Write down the truth table of a two input XNOR gate. Draw the traditional symbol for a two input XNOR gate. (5 marks)

   (b) Draw a timing diagram showing the four possible input combinations and corresponding output of a two input XNOR gate. (10 marks)

   (c) Draw diagrams showing the construction of a two input AND gate and a two input OR gate using diode resistor logic. What is the principal disadvantage of diode resistor logic? (10 marks)

2. (a) Write down the four idempotent rules of Boolean algebra, derived from the combination of a single variable with itself. (5 marks)

   (b) Write down a boolean expression for the circuit shown below. Using the theorems of boolean algebra find and draw the simplest circuit that implements the function F_2.



   (10 marks)

   (c) Simplify the function

   F(A, B, C, D) = AC'D' + A'C + ABC + AB'C + A'C'D'

   using a Karnaugh map and draw the resulting circuit. (10 marks)

3. (a) Implement the following Boolean function with a 4 x 1 multiplexer and external gates.

F (A, B, C, D) = Σ (1, 2, 5, 7, 8, 10, 11, 13, 15)

Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D . These values are obtained by expressing F as a function of C and D for each of the four cases when AB = 00, 01, 10, and 11. Write down a truth table showing all input cases and derive the logic for the data lines. (16 marks)

(b) Draw the resulting circuit using minimum external gates and labelling all inputs clearly (9 marks)

Section B

1. (a) Encoding of data was detailed during the course. What is data encoding? Give an example. (4 marks)

   (b) Explain the terms *setup time* and *hold time* in relation to flip-flops. (6 marks)

   (c) Explain synchronous and asynchronous sequential circuits. What issues and problems arise with asynchronous logic that make synchronous logic advantageous? (8 marks)

   (d) From the state diagram, Figure 1, produce the associated state table. (7 marks)

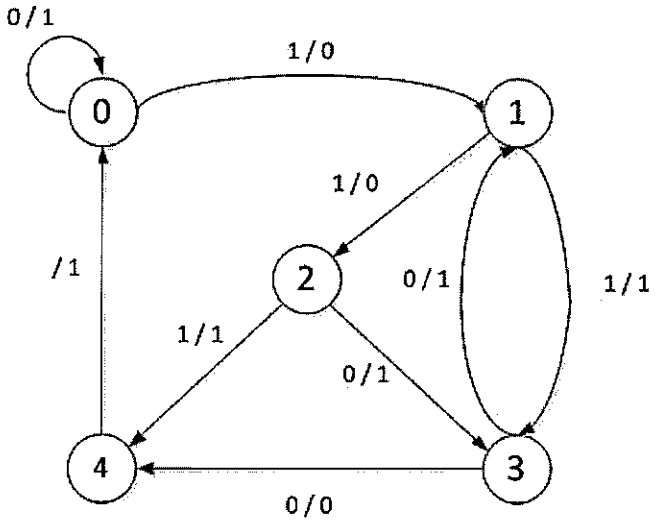


Figure 1: State Diagram

2. Based on the following operations of an up counter:

   - User input which controls the counter starting
   - Counter starts from zero and loops over 32 numbers (0 - 31)
   - A second user control input to say if increment by 1 or 2 with the following operation
     - if the counter is less than 16 and the input is active, increment by 2, otherwise by 1
     - if the counter is greater than or equal to 16 and the input is active, increment by 1, otherwise by 2

   (a) Produce the Algorithmic State Machine for the above circuit operations. (10 marks)

   (b) Identify the data path components that are needed for the circuit. (3 marks)

   (c) Produce the state table and state equations. (8 marks)

   (d) Create the logic diagram of the circuit. (4 marks)

3. Examine the synchronous sequential logic circuit below, Figure 2:

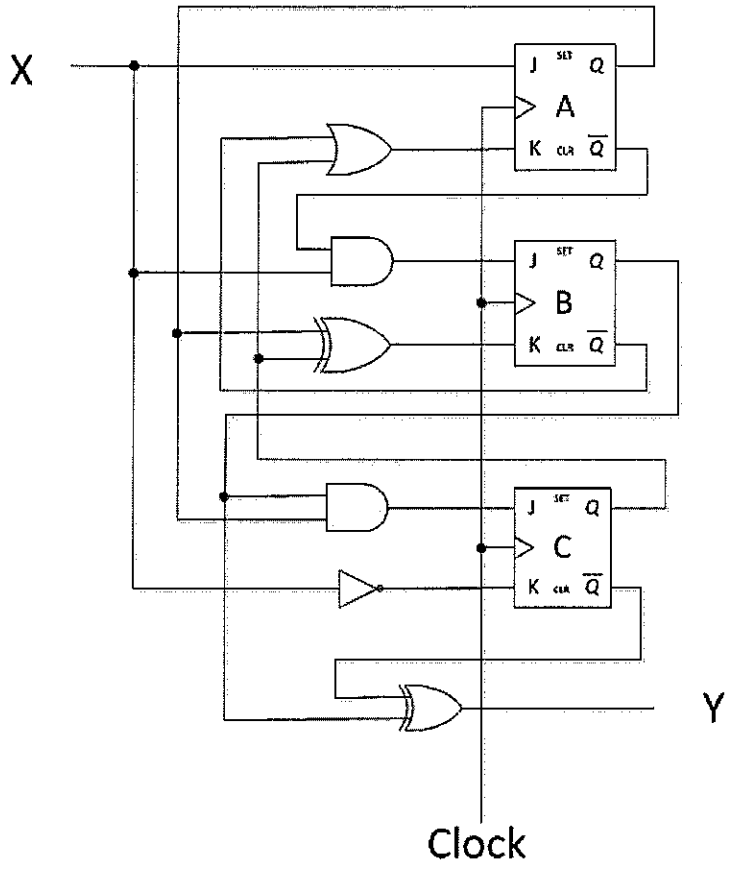


Figure 2: Synchronous sequential circuit

(a) Derive the state equations for this circuit. (5 marks)

(b) Derive the state table for this circuit. (10 marks)

(c) Using the state table, draw the equivalent state diagram. (10 marks)