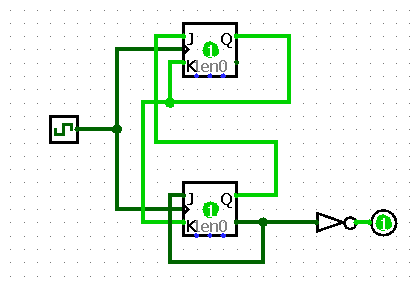
**Title:** CS1026 Lab 7

**Date:** 03/04/2017

**Aim:**

* To design a synchronous sequential circuit that divides a system clock frequency *f* CLK by 3 using JK Flip-Fops

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**Analysis:**

* I began by drawing the CLK timing diagram for the desired circuit
* I then drew the *Characteristic Table* for a JK Flip-Flop
* From this I devised the *Output Excitation Table* for a JK Flip-Flop
* I then also devised the *Input Excitation Table* for a JK Flip-Flop
* Using the above tables I then created 3 Karnaugh Maps that I then used to come up with a solution Z for the system

