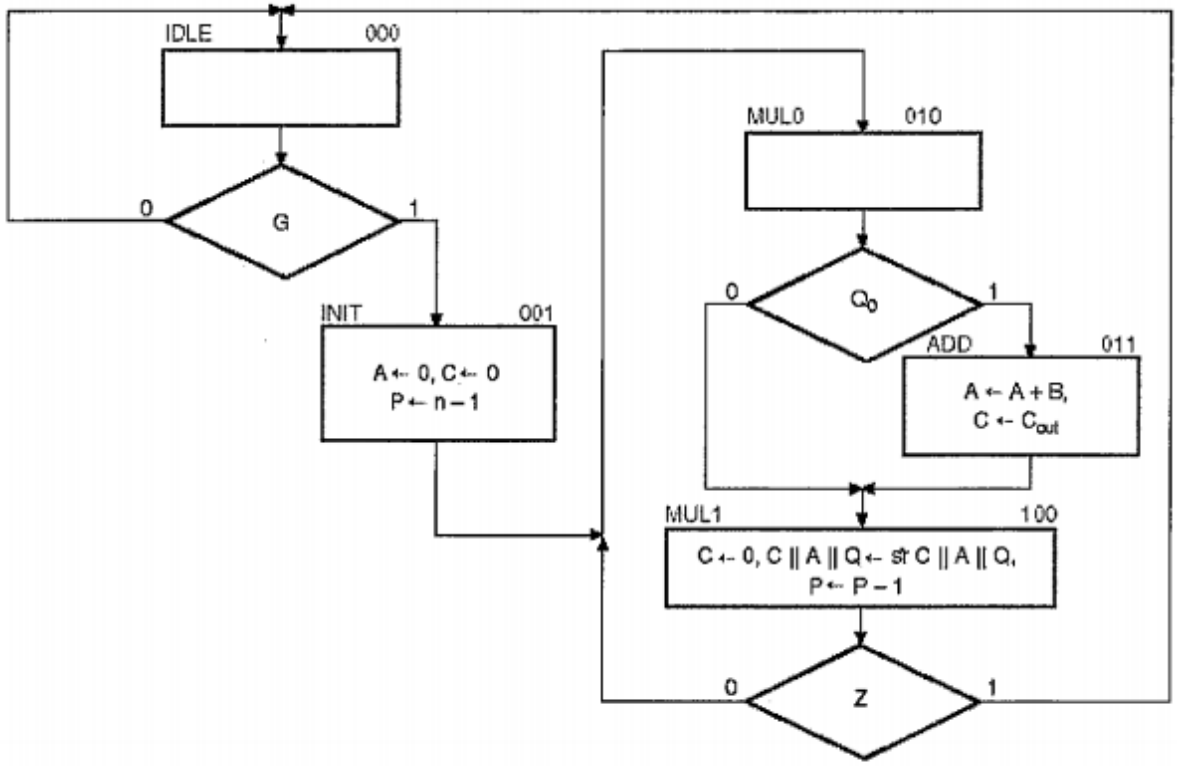
Credit: KVH

1.

The following ASM Chart describes the sequential operations of a Binary Multiplier:



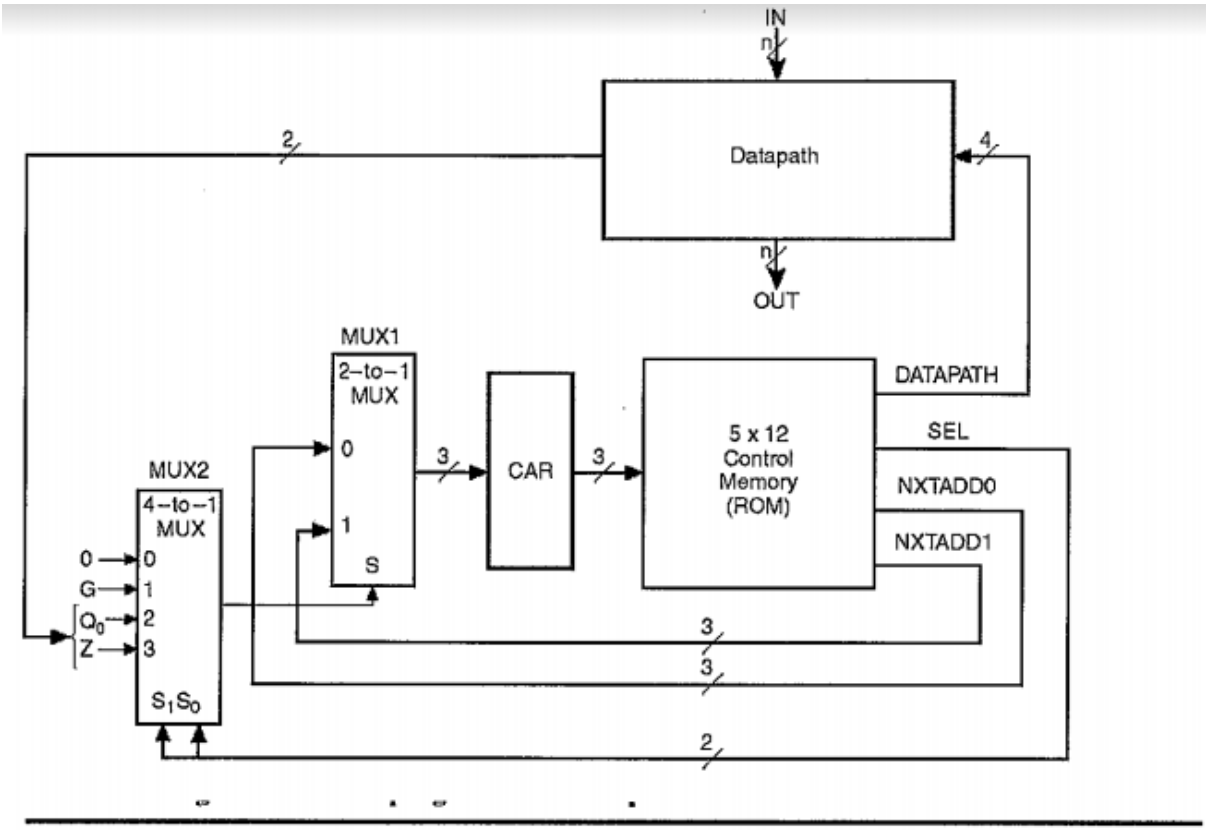
a) The above ASM Chart is suitable for a microcoded control implementation. What would you need to change in order to make the ASM suitable for a hardwired solution? Why is this modification necessary?

[5 marks]

Q1) a)

The states INIT and ADD would need to be replaced with conditional output boxes. This is due to the fact that in a hardwired solution, control words are not stored, unlike the microcoded solution, and so can be made to dynamically depend on the value of control input.

Hence, the additional states in the microcoded solution, which were supplying the alternative control words, may be removed.



Control Signal	Register Transfers	States in Which Signal is Active	Micro-instruction Bit Position	Symbolic Notation
Initialize	$A \leftarrow 0, P \leftarrow n-1$	INIT	0	IT
Load	$A \leftarrow A+B, C \leftarrow C_{out}$	ADD	1	LD
Clear_C	$C \leftarrow 0$	INIT, MUL1	2	CC
Shift_dec	$C\|A\|Q \leftarrow \text{sr } C\|A\|Q, P \leftarrow P-1$	MUL1	3	SD

b) Please provide microcode for the above Control Memory (5x12) that implements the above ASM Chart. Discuss how the control hardware executes your microcode.

[15 marks]

Q1) b)

State	Address		NXTADDR1	NXTADDR0	SEL	SD	CC	LD	IT
IDLE	000		001	000	01	0	0	0	0
INIT	001		000	010	00	0	1	0	1
MUL0	010		011	100	10	0	0	0	0
ADD	011		000	100	00	0	0	1	0
MUL1	100		000	010	11	1	1	0	0

000 - The control hardware starts off in the IDLE state. The SEL bits specify that G should be used to decide the next address. If G = ‘0’, it returns to the IDLE state, otherwise it goes to the INIT state.

001 - From INIT, Clear_C and Initialise are sent to the datapath. The SEL bit selects ‘0’ as input to the address multiplexer, thus always selecting NXTADDR0 (state MUL0) next.

010 - From MUL0, nothing is sent to the datapath, the SEL bits select Q_0 to decide between moving to the ADD or MUL1 state. If Q_0 = ‘1’ it executes ADD, else MUL1.

011 - From here, LOAD is sent to the datapath and the SEL bit selects ‘0’, setting the next address to NXTADDR0 (MUL1).

100 - From MUL1, Clear_C and Shift_dec go to the datapath. The SEL bits select Z as the input to decide between MUL0 or IDLE as the next address.