UNIVERSITY OF DUBLIN
TRINITY COLLEGE

Faculty of Engineering and Systems Sciences

Department of Computer Science

BA (Mod) Computer Science **Trinity Term 2007**

Senior Freshman Examination

2BA4 – Computer Architecture I

Tuesday 5th June 2007 **Goldsmith Hall** **09:30 – 12:30**

Dr Dan McCarthy & Dr Michael Manzke

Instructions to Candidates

Answer FIVE questions, at least TWO from each section.

Please use separate answer books for each section

SECTION A (Dr D Mc Carthy)

1.

a) Draft the schematic of a four-bit functional unit which will efficiently implement the following micro-operations under the control of a two-bit select control S:

[10 marks]

S	Micro-operation
00	A + B
01	A – 1
10	A + 1
11	A – B

b) Add to your schematic of part a) circuits to generate the four status bits, Z=Zero, N=Negative, C=Carry-out, V=oVerflow.

[4 marks]

c) Assume that your arithmetic unit of parts a) and b) is attached to a register file with registers R0, R1, R2, R3 with provision to load the registers with an arbitrary four-bit datum. Draft a symbolic register transfer sequence that will test each functional and status circuit at least once.

[6 marks]

2.

a) Describe a technique by which four registers R0, R1, R2, R3 may be interconnected to permit every possible register interchange to take place, i.e. Ri ← Rj where 0≤i,j≤3. Briefly identify the principal advantage and disadvantage of the technique that you have presented.

[10 marks]

b) Design an efficient bus system to accommodate the following set of register transfers, showing clearly the method of both source register selection and destination register load control. Assume that all control signals are mutually exclusive.

C_0: R0 ← R2, R2 ← R0
C_1: R1 ← R3, R0 ← R3
C_2: R1 ← R2, R3 ← R0
C_3: R0 ← R3, R2 ← R1

[10 marks]

3.

a) Explain how the performance of a processor datapath may be improved by the introduction of pipeline registers.

[10 marks]

b) A processor datapath consists of a register file R followed by five major components C_i i=1,5, each with a maximum propagation delay as follows:

[10 marks]

Component	R	C_1	C_2	C_3	C_4	C_5
Max. propogation delay nS	1	2	5	9	3	5

(i) Compute the maximum clock frequency that can be used for this datapath.

(ii) If the datapath is pipelined as three stages using pipeline registers with a proprogation delay of 1 nS then how should the components be divided into stages for maximum performance, and what is the maximum clock frequency that can be achieved?

4.

a) Draw a schematic of a micro-programmed control unit for a datapath which will allow the implementation of the following instructions:

i) Single-cycle datapath micro-instructions.

ii) Unconditional branches.

iii) Conditional branches based on the overflow bit V being set or reset, i.e. BV or BNV.

[10 marks]

b) Give an ASM showing the sequence of instruction fetch and execution for the following single word instructions consisting of an OPCODE followed by appropriate operand fields:

Instruction format	RT description
ADD: DR:SA:SB	R[DR] ← R[SA] + R[SB]
BV: BRADRS	V: PC ← BRADRS, NOT V: PC ← PC + 1

Note that the instruction sub-fields of OPCODE, DR, SA, SB, and BRADRS are all available directly from the instruction register IR.

[10 marks]

SECTION B (Dr. M. Manzke)

5.

a) Compare the following types of output pins. Your comparison should explain how switches could be used to demonstrate each output type's operation:

- Tri-State
- Fully-Driven
- Partially-Driven

[7 marks]

b) Examine why Tri-State and Partially Driven output pins should not be connected to the same line?

[5marks]

c) The following are proposed output pins for a new I/O controller. Determine the type of output pin that should be used for these pins.

(i) Baud Clock- Outputs a clock signal that is a multiple of the commonly used baud rates, for use by the I/O system components.

(ii) Bus Request - this controller is designed to work with a standard processor so it will not always be Bus Master. This output pin is used to request access to the bus from the processor. Note that there will other controllers in the system also wanting to request such an access.

(iii) Data Bus Pins – Connects the device to the data bus for read and write operations.

[8 marks]

6.

Assume you aim to interconnect the following components in a microprocessor system through a shared bus:

- 1 × CPU MC68008 (20 Address Pins)
- 1 × EPROM (8k)
- 2 × RAM (2k)
- 1 × RAM (4k)
- 2 × IO-Devices (eight 8bit registers)

a) Your design should provide a detailed memory map. The memory map must place the first RAM device at base address $4000. Your map should also comply with all the design rules. Your solution should include the first and last address of every device and indicate the system bus address lines that are connected to the individual devices.

[8 marks]

b) Develop VHDL code that implements your decoder design.

[8 marks]

c) You may relax particular design rule(s) for the IO devices. Why could this be helpful? Please discuss the consequences.

[4 marks]

7.

a) Compare read and write cycles that allow the Motorola 68008 CPU to load and store data into RAM, ROM and other devices' registers. Your comparison must include all signals that are involved in such bus transactions.

[6 marks]

b) Design external digital logic that can be used to adjust the bus cycle time in order to allow slower and faster devices to communicate with the CPU over the same system bus.

[7 marks]

c) Provide a detailed design for the VPA & VMA signal generation. Provide a timing diagram that shows the following signals: CPU-clock, E-clock, IO-select, VPA and VMA. What are the conditions that require the VPA signal to be active and how does this relate to the connection of interrupt to the CPU?

[7 marks]

8.

a) Explain the basic operations of the Logic Analyser that was used for the microprocessor project. Give examples for situations that require the use of a logic Analyser and circumstances in which you would use an Oscilloscope. List the signals that must be attached to the Logic Analyser in order to observe system-bus transactions related to the execution of the following code:

[5 marks]

```
            00000000        1  INITSP   EQU   $00000
            00000400        2  LOOP     EQU   $00400
            00000400        3  INITPC   EQU   LOOP
                            4
00000000                    5  org      $00000
00000000    00000000        6  dc.l     INITSP
00000004    00000400        7  dc.l     INITPC
                            8
00000400                    9  org      LOOP
00000400    4EF8 0400       10 jmp      LOOP
00000404                    11 end

No errors detected
No warnings generated
```

b) The above assembly source code is taken from a *.lis file. You can assume that the code is stored in the system's ROM device. This device has a base-address of $00000. Examine how you could achieve the observation of all bus transactions that relate to the execution of the entire code including the acquisition of the SSP and the PC? How would you group and configure the signals for this measurement?

[5 marks]

c) Develop a listing of the Logic Analyser readings in sequential order and analyse how this data relates to the execution of the above code.

[10 marks]