UNIVERSITY OF DUBLIN

TRINITY COLLEGE

Faculty of Engineering, Mathematics and Science
School of Computer Science and Statistics

B.A.(Mod.) Computer Science
Senior Freshman Supplemental Examination

Trinity Term 2008

2BA4 – Computer Architecture I

Tuesday 3 June 2008 **Goldhall** **09:30-12:30**

Mr. Ross Brennan, Dr. Michael Manzke

Answer **FIVE** questions, at least **TWO** from each section.

Use separate answer books for section A and section B.

SECTION A

1.

a) Discuss the advantages and disadvantages of a *SR/SL Shifter* unit and a *Barrel Shifter* unit.

[5 marks]

b) Write VHDL code that implements a *4-bit Barrel Shifter*.

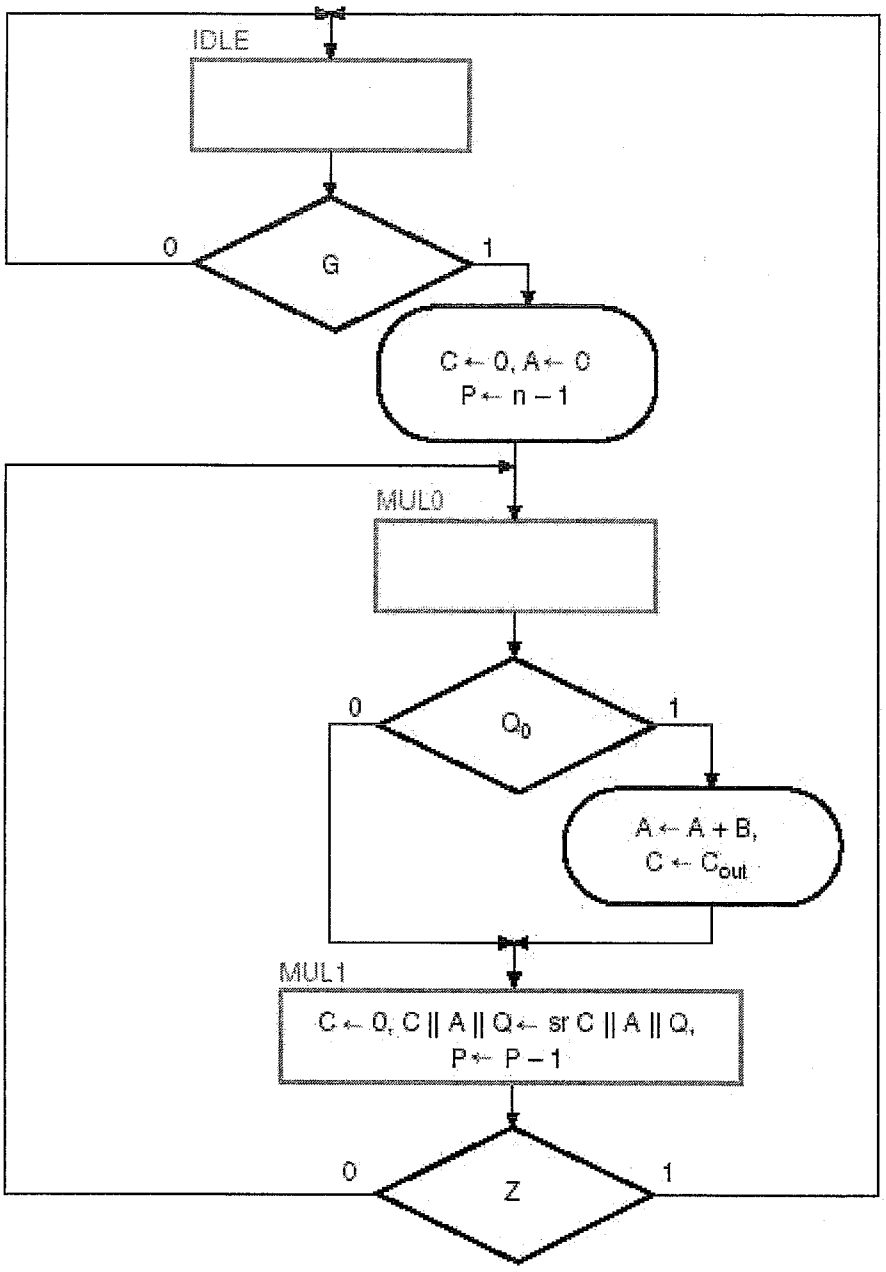
[10 marks]

c) Explain how you would test your VHDL code from part (b).

[5 marks]

2.

The following Algorithmic State Machine (ASM) chart shows the operation of a *Binary Multiplier*.



a) Provide an example (multiply two binary numbers) that explains the operations of the *Binary Multiplier*.

[10 marks]

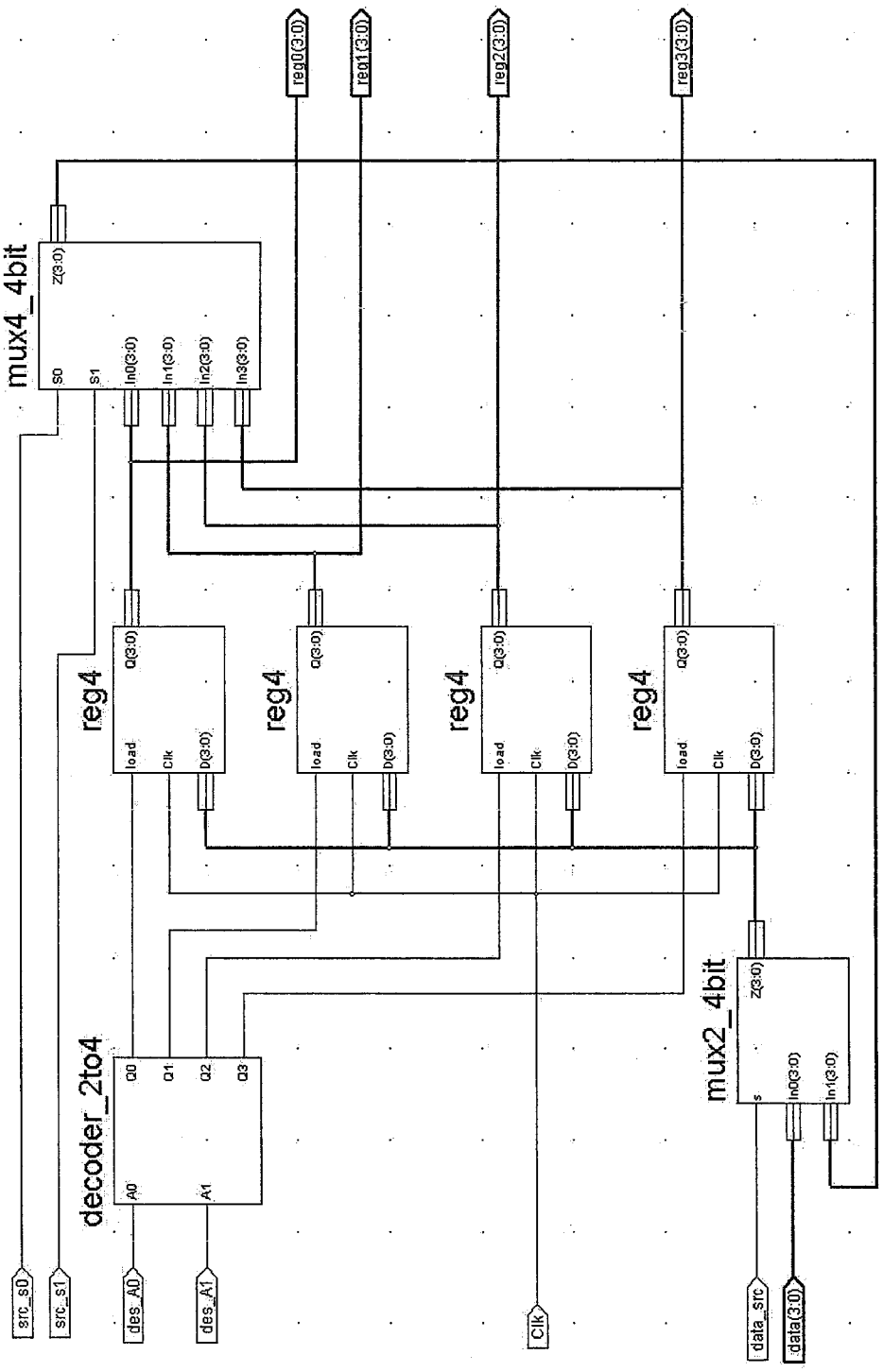
b) Write VHDL code that implements the *Binary Multiplier* through a VHDL-state-machine-process and other VHDL-processes.

[10 marks]

3.

a) Write VHDL code that implements the following Register-file.

[12 marks]



b) Discuss the register transfer operations that can be performed with this Register-file.

[8 marks]

4.

a) Draft a schematic that represents a *Multiple-cycle Microprogrammed Instruction Set Processor Control Unit*. The *Control Unit* should receive 16-bit instructions from memory that holds *data* and *instructions*. The memory supplies instructions to the *Control Unit* and the data are communicated with the *Datapath Unit*. The *Control Unit* controls a *Datapath* with a 9 x 16 *Register-file* and a *Function Unit*. The *Function Unit* provides feedback to the *Control Unit* through V, C, N and Z status flags. The 9^{th} register is a dedicated register to store data between micro-operations. Your solution should contain the following components: *PC, IR, CAR, 2 x MUX and 256 x 28 Control Memory*.

[10 marks]

b) Provide a discussion of the operations that take place while instructions are fetched and executed.

[10 marks]

SECTION B

5.

a) Describe the bus protocol and signalling interface that the Motorola MC68008 CPU uses to communicate with memory devices.

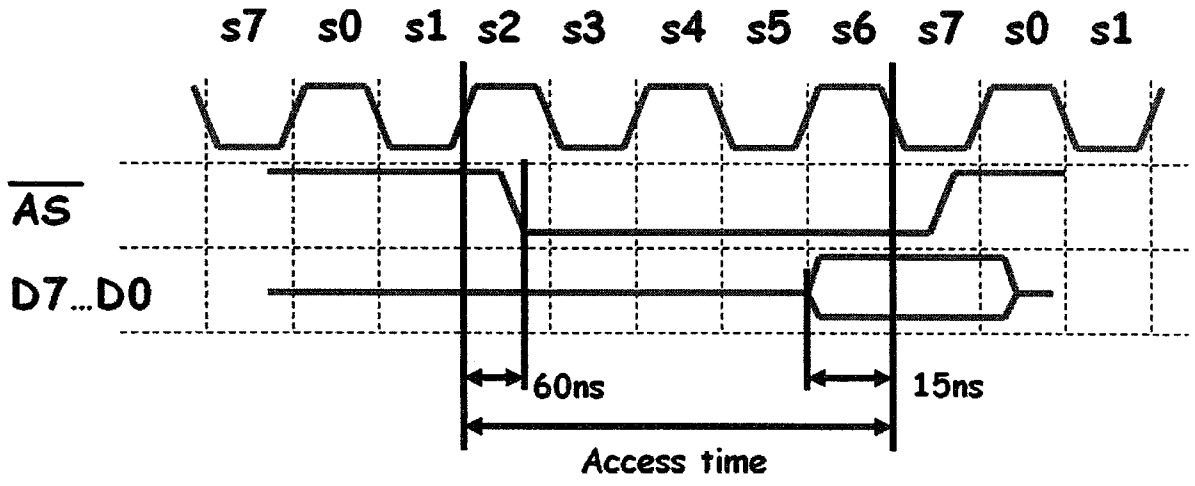
[5 marks]

b) How does this compare to the bus protocol and signalling interface used to communicate with the I/O (M6800 compatible) devices?

[5 marks]

c) Discuss the purpose of bus-cycle wait-states and explain how they could be implemented using the CPLD. Assuming a clock frequency of 8MHz and 0 wait-states, calculate the maximum access latency a device may have in order to operate correctly given the timing diagram below.

[10 marks]



6.

a) Describe each of the following types of output pin: Tri-State, Fully-Driven and Partially-Driven. Explain why Tri-State and Partially-Driven output pins should not be connected together. What is the difference between a pull-up and pull-down resistor and under what circumstances should they be used?

[8 marks]

b) Describe the basic operation and purpose of a Logic State Analyser and an Oscilloscope as used during the microprocessor project.

[4 marks]

c) Give examples of situations from your project work where you needed to use a Logic State Analyser and where you needed to use an Oscilloscope and discuss how these instruments aided in the debugging and verification of the operation of the microprocessor boards.

[8 marks]

7.

a) What is the purpose of a system memory-map and what are the general requirements that should be followed when designing one?

[4 marks]

b) Design a detailed memory-map that complies with all of the design rules specified as part of the microprocessor project and satisfies the following system requirements:

- 1 x MC68008 CPU [20 address pins, reset @ $00000]
- 1 x 8k EEPROM
- 4 x 4k RAM
- 2 x 4-byte R6551 ACIAs

The components are to be connected together using a shared bus and the RAM devices should start at address location $4000. Your solution should include the first and last address of every device and should indicate the address-bus lines that are connected to each device.

[8 marks]

c) Given the following entity port declaration, implement your decoder design from part (b), using VHDL code.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity decoder is
     port(
        CLOCK, E        : in  std_logic;
        A19, A18, A17   : in  std_logic;
        A16, A15, A14   : in  std_logic;
        A13, A12, A11   : in  std_logic;
        AS              : in  std_logic;
        FC0, FC1, FC2   : in  std_logic;
        CSROM           : out std_logic;
        CSRAM1          : out std_logic;
        CSRAM2          : out std_logic;
        CSRAM3          : out std_logic;
        CSRAM4          : out std_logic;
```

```
        CSIO1           : out std_logic;
        CSIO2           : out std_logic;
        DTACK           : out std_logic;
        VPA             : out std_logic;
        VMA             : out std_logic
    );
end decoder;
```

[8 marks]

8.

a) What is a LINE 1111 exception? What are the advantages of using a LINE 1111 exception to call system subroutines "by number"?

[4 marks]

b) Describe the sequence of events that occurs when the MC68008 detects a regular interrupt request from an external device. Explain the difference between regular interrupt handling and interrupt auto-vectoring.

[8 marks]

c) Assuming a MC68008 based microprocessor system that is similar to the system that you assembled in your coursework, you are required to design and implement a transparent link programme, using MC68008 assembly. Your solution should initialise and then enter an infinite loop that alternately polls 2 x R6551 ACIAs that are attached to the microprocessor system. When incoming data are detected on one of the ACIAs, it should be read into local memory and then written back out to both of the ACIAs. The RAM area starts at address location $4000, the *command register* should be initialised to *$0B* (no parity and no interrupts) and the *control register* should be initialised to *$18* (1200 baud). *Bit-4* of the *status register* indicates transmitter *data register* empty and *bit-3* of the status register indicates receiver data register full. You should provide a *flow-chart* as well as a pseudo-code description that shows the operation of your solution in addition to the assembly code.

```
IODEV1    EQU    $80000    * ACIA1 base location
IODEV2    EQU    $C0000    * ACIA2 base location
IODATA    EQU    0         * Data register offset
IOSTAT    EQU    1         * Status register offset
IOCOMM    EQU    2         * Command register offset
IOCNTL    EQU    3         * Control register offset
```

[8 marks]