Component : dewarp\_m2m\_regbank

|  |  |
| --- | --- |
| Description : |  |

Block : ip\_info

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Name | Description | Reset |
| 0x00 | [ip\_version](#_65428e9a-4026-4a69-af7f-791b753739a0) | IP version. | 0x0000 0000 |

2

Block : signal\_regs

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Name | Description | Reset |
| 0x08 | [recon\_start](#_7d802e36-5218-4316-a4fd-245db2f7a38d) | Transform start signal. | 0x0000 0000 |

2

Block : image\_configuration\_regs

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Name | Description | Reset |
| 0x10 | [base\_addr\_in\_0](#_7ffc4834-5b0c-44a5-be7c-c379c5c9bb02) | First base address of the input image. | 0x0000 0000 |
| 0x14 | [addr\_stride\_in\_0](#_107f0dda-938a-4a92-934c-131cf8592324) | First address stride of the input image. | 0x001E 0000 |
| 0x18 | [base\_addr\_in\_1](#_7bbfdb88-fddb-4e60-919b-e7fb8c90b929) | Second base address of the input image. | 0x0080 0000 |
| 0x1C | [addr\_stride\_in\_1](#_e587c529-dc3f-4503-ba63-938237094901) | Second address stride of the input image. | 0x0007 8000 |
| 0x20 | [base\_addr\_in\_2](#_c4018dfa-455f-4e69-821a-ec261762f390) | Third base address of the input image. | 0x00C0 0000 |
| 0x24 | [addr\_stride\_in\_2](#_729155e4-31d1-42a4-b8da-a37f773d8a2b) | Third address stride of the input image. | 0x0007 8000 |
| 0x28 | [base\_addr\_out\_0](#_e2ae36fe-9aeb-4d3b-84fa-aafe8d5a4633) | First base address of the output image. | 0x0100 0000 |
| 0x2C | [addr\_stride\_out\_0](#_b4298cb8-497c-49ed-8ae6-822619cd7e76) | First address stride of the output image. | 0x001E 0000 |
| 0x30 | [base\_addr\_out\_1](#_2a3503dc-4be9-4379-86fa-f0595b3f1ba6) | Second base address of the output image. | 0x0180 0000 |
| 0x34 | [addr\_stride\_out\_1](#_c0a3b976-4780-4a09-af48-287974d3d2a4) | Second address stride of the output image. | 0x0007 8000 |
| 0x38 | [base\_addr\_out\_2](#_ff0258e3-fb0d-489d-b848-e4cf2c5070f5) | Third base address of the output image. | 0x01C0 0000 |
| 0x3C | [addr\_stride\_out\_2](#_b7e57c27-bbc3-4002-b60c-bb74382491f0) | Third address stride of the output image for. | 0x0007 8000 |
| 0x40 | [input\_size](#_02cef0d0-10f0-4cb3-b209-0981ae567bea) | Size of the input image. | 0x02D0 0500 |
| 0x44 | [output\_size](#_c380ab25-2175-4763-ae09-d1fbcb988e00) | Size of the output image. | 0x02D0 0500 |
| 0x48 | [image\_format](#_4a0bc11d-ca0c-4b5a-b56a-ab1f8663a256) | Input/output image format and color/ir enable signals. | 0x0101 0808 |
| 0x4C | [default\_color](#_280b28b3-3881-46f0-b53e-5a69444db430) | Default color for invalid pixels. | 0x8080 8080 |

2

Block : mapping\_parameter\_regs

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Name | Description | Reset |
| 0x50 | [cam\_mat\_fx](#_489e9b76-eac7-435c-a8c0-079bf2af3a8d) | fx of the camera matrix. | 0x0000 3001 |
| 0x54 | [cam\_mat\_sx](#_1dd8956a-60b1-44cc-a47d-a718b4f27db9) | sx of the camera matrix. | 0x0000 10FD |
| 0x58 | [cam\_mat\_cx](#_bb31ca8f-8957-4fd6-a21c-150b8e7800f7) | cx of the camera matrix. | 0x0000 4FEC |
| 0x5C | [cam\_mat\_fy](#_1127cedf-7c6c-4f59-b6ec-0f3b3abe0f60) | fy of the camera matrix. | 0x0000 2FEE |
| 0x60 | [cam\_mat\_cy](#_6ca25981-b114-405d-b37a-ac8f1a9b7d7f) | cy of the camera matrix. | 0x0000 2CE2 |
| 0x64 | [dist\_coeff\_k1](#_42958e86-4d97-4213-baaf-efaa7ecda7fd) | Distortion coefficient k1. | 0x0000 7E80 |
| 0x68 | [dist\_coeff\_k2](#_c97008e8-e100-4096-bae0-a80d0ecdbf4b) | Distortion coefficient k2. | 0x0000 0C73 |
| 0x6C | [dist\_coeff\_k3](#_25264a31-e1f9-4528-952e-38cbc6f5c8ee) | Distortion coefficient k3. | 0x000F DE1F |
| 0x70 | [dist\_coeff\_k4](#_7225604e-ca73-4e00-8927-c1341d20a352) | Distortion coefficient k4. | 0x0000 0536 |
| 0x74 | [homography\_h11](#_3e765969-b735-4d49-9320-ca4c08faa7ea) | h11 of the homography matrix. | 0x0003 DF79 |
| 0x78 | [homography\_h12](#_d5249fef-09b7-4cf4-be0b-a24166720671) | h12 of the homography matrix. | 0x0000 1368 |
| 0x7C | [homography\_h13](#_59269f68-9fae-4066-a8ed-8d63b9d54263) | h13 of the homography matrix. | 0x0000 261B |
| 0x80 | [homography\_h21](#_f54203f6-7784-42bd-b3d8-d0a03e8c42f4) | h21 of the homography matrix. | 0x0003 DD8E |
| 0x84 | [homography\_h22](#_778ad632-8179-42a1-8042-30f9010bca3d) | h22 of the homography matrix. | 0x0003 E8B1 |
| 0x88 | [homography\_h23](#_7d17703b-2062-4c7d-b0e1-0f714b4722fb) | h23 of the homography matrix. | 0x0000 0BF0 |
| 0x8C | [is\_fisheye](#_ce66337a-9038-4ad4-842e-f6f08aa85149) | Use fisheye model. | 0x0000 0001 |

2

Block : peripheral\_configuration\_regs

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Name | Description | Reset |
| 0xA0 | [cache\_timeout\_cnt](#_101a96d9-a002-4eaf-ad02-930aa9e79432) | Read cache timeout count. | 0x0000 0000 |
| 0xA4 | [axi\_outstanding](#_740163f5-0167-4f06-8c39-a15133c09a31) | AXI maximum outstanding count. | 0x0000 0F0F |
| 0xA8 | [interrupt\_delay](#_d8544496-2c29-4c4c-956b-da91539948c3) | Done interrupt delay count. | 0x0000 0100 |
| 0xAC | [interrupt\_clear\_cnt](#_77e74cbf-2274-46df-9da6-bc21325447db) | Done interrupt clear count. | 0x0000 0000 |

2

Block : interrupt\_clear\_regs

|  |  |  |  |
| --- | --- | --- | --- |
| Address | Name | Description | Reset |
| 0xB0 | [interrupt\_clear](#_05aa1a56-5e26-4acc-b20a-a166cd91d1b6) | Done interrupt clear signal. | 0x0000 0000 |

2

Block: ip\_info

|  |  |
| --- | --- |
| Description | : |

3

Register: ip\_version

|  |  |
| --- | --- |
| Description | : IP version. |
| Offset | : 0x0 |
| Absolute Address | : 0x00 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ip\_version | | | | | | | | | | | | | | | |
| RO - 0x0000 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ip\_version | | | | | | | | | | | | | | | |
| RO - 0x0000 0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | ip\_version | IP version. | RO  -  - | 0x0000 0000 |

6

Block: signal\_regs

|  |  |
| --- | --- |
| Description | : |

3

Register: recon\_start

|  |  |
| --- | --- |
| Description | : Transform start signal. |
| Offset | : 0x0 |
| Absolute Address | : 0x08 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | | | | | | | ready |  | | | | | | | start |
|  | | | | | | | RO - 0x0 |  | | | | | | | WO - 0x0 |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 8 | ready | Transform ready signal. | RO  -  - | 0x0 |
| 0 | start | Transform start signal. | WO  WC  - | 0x0 |

6

Block: image\_configuration\_regs

|  |  |
| --- | --- |
| Description | : |

3

Register: base\_addr\_in\_0

|  |  |
| --- | --- |
| Description | : First base address of the input image. |
| Offset | : 0x0 |
| Absolute Address | : 0x10 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| base\_addr\_in\_lsb\_0 | | | | | | | | | | | | | | | |
| RW - 0x0000 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| base\_addr\_in\_lsb\_0 | | | | | | | | | | | | | | | |
| RW - 0x0000 0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | base\_addr\_in\_lsb\_0 | Base address of the input image for IRRGB, YU/YV(422 sequential), Y(422/420 interleaved), or IR (IR only) channel. | RW  -  - | 0x0000 0000 |

6

Register: addr\_stride\_in\_0

|  |  |
| --- | --- |
| Description | : First address stride of the input image. |
| Offset | : 0x4 |
| Absolute Address | : 0x14 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | addr\_stride\_in\_0 | | | | | | | | | | | |
|  | | | | RW - 0x0 1E00 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| addr\_stride\_in\_0 | | | | | | | |  | | | | base\_addr\_in\_msb\_0 | | | |
| RW - 0x0 1E00 | | | | | | | |  | | | | RW - 0x0 | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:8 | addr\_stride\_in\_0 | Address stride of the input image for IRRGB, YU/YV(422 sequential), Y(422/420 interleaved), or IR (IR only) channel. | RW  -  - | 0x0 1E00 |
| 3:0 | base\_addr\_in\_msb\_0 | Base address of the input image for IRRGB, YU/YV(422 sequential), Y(422/420 interleaved), or IR (IR only) channel. | RW  -  - | 0x0 |

6

Register: base\_addr\_in\_1

|  |  |
| --- | --- |
| Description | : Second base address of the input image. |
| Offset | : 0x8 |
| Absolute Address | : 0x18 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| base\_addr\_in\_lsb\_1 | | | | | | | | | | | | | | | |
| RW - 0x0080 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| base\_addr\_in\_lsb\_1 | | | | | | | | | | | | | | | |
| RW - 0x0080 0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | base\_addr\_in\_lsb\_1 | Base address of the input image for IR (RGB-IR, YUV422-IR) or U/V (422/420 interleaved) channel. | RW  -  - | 0x0080 0000 |

6

Register: addr\_stride\_in\_1

|  |  |
| --- | --- |
| Description | : Second address stride of the input image. |
| Offset | : 0xC |
| Absolute Address | : 0x1C |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | addr\_stride\_in\_1 | | | | | | | | | | | |
|  | | | | RW - 0x0 0780 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| addr\_stride\_in\_1 | | | | | | | |  | | | | base\_addr\_in\_msb\_1 | | | |
| RW - 0x0 0780 | | | | | | | |  | | | | RW - 0x0 | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:8 | addr\_stride\_in\_1 | Address stride of the input image for IR (RGB-IR, YUV422-IR) or U/V (422/420 interleaved) channel. | RW  -  - | 0x0 0780 |
| 3:0 | base\_addr\_in\_msb\_1 | Base address of the input image for IR (RGB-IR, YUV422-IR) or U/V (422/420 interleaved) channel. | RW  -  - | 0x0 |

6

Register: base\_addr\_in\_2

|  |  |
| --- | --- |
| Description | : Third base address of the input image. |
| Offset | : 0x10 |
| Absolute Address | : 0x20 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| base\_addr\_in\_lsb\_2 | | | | | | | | | | | | | | | |
| RW - 0x00C0 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| base\_addr\_in\_lsb\_2 | | | | | | | | | | | | | | | |
| RW - 0x00C0 0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | base\_addr\_in\_lsb\_2 | Base address of the input image for IR (422/420-IR interleaved) channel. | RW  -  - | 0x00C0 0000 |

6

Register: addr\_stride\_in\_2

|  |  |
| --- | --- |
| Description | : Third address stride of the input image. |
| Offset | : 0x14 |
| Absolute Address | : 0x24 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | addr\_stride\_in\_2 | | | | | | | | | | | |
|  | | | | RW - 0x0 0780 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| addr\_stride\_in\_2 | | | | | | | |  | | | | base\_addr\_in\_msb\_2 | | | |
| RW - 0x0 0780 | | | | | | | |  | | | | RW - 0x0 | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:8 | addr\_stride\_in\_2 | Address stride of the input image for IR (422/420-IR interleaved) channel. | RW  -  - | 0x0 0780 |
| 3:0 | base\_addr\_in\_msb\_2 | Base address of the input image for IR (422/420-IR interleaved) channel. | RW  -  - | 0x0 |

6

Register: base\_addr\_out\_0

|  |  |
| --- | --- |
| Description | : First base address of the output image. |
| Offset | : 0x18 |
| Absolute Address | : 0x28 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| base\_addr\_out\_lsb\_0 | | | | | | | | | | | | | | | |
| RW - 0x0100 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| base\_addr\_out\_lsb\_0 | | | | | | | | | | | | | | | |
| RW - 0x0100 0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | base\_addr\_out\_lsb\_0 | Base address of the output image for IRRGB, YU/YV(422 sequential), Y(422/420 interleaved), or IR (IR only) channel. | RW  -  - | 0x0100 0000 |

6

Register: addr\_stride\_out\_0

|  |  |
| --- | --- |
| Description | : First address stride of the output image. |
| Offset | : 0x1C |
| Absolute Address | : 0x2C |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | addr\_stride\_out\_0 | | | | | | | | | | | |
|  | | | | RW - 0x0 1E00 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| addr\_stride\_out\_0 | | | | | | | |  | | | | base\_addr\_out\_msb\_0 | | | |
| RW - 0x0 1E00 | | | | | | | |  | | | | RW - 0x0 | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:8 | addr\_stride\_out\_0 | Address stride of the output image for IRRGB, YU/YV(422 sequential), Y(422/420 interleaved), or IR (IR only) channel. | RW  -  - | 0x0 1E00 |
| 3:0 | base\_addr\_out\_msb\_0 | Base address of the output image for IRRGB, YU/YV(422 sequential), Y(422/420 interleaved), or IR (IR only) channel. | RW  -  - | 0x0 |

6

Register: base\_addr\_out\_1

|  |  |
| --- | --- |
| Description | : Second base address of the output image. |
| Offset | : 0x20 |
| Absolute Address | : 0x30 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| base\_addr\_out\_lsb\_1 | | | | | | | | | | | | | | | |
| RW - 0x0180 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| base\_addr\_out\_lsb\_1 | | | | | | | | | | | | | | | |
| RW - 0x0180 0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | base\_addr\_out\_lsb\_1 | Base address of the output image for IR (RGB-IR, YUV422-IR) or U/V (422/420 interleaved) channel. | RW  -  - | 0x0180 0000 |

6

Register: addr\_stride\_out\_1

|  |  |
| --- | --- |
| Description | : Second address stride of the output image. |
| Offset | : 0x24 |
| Absolute Address | : 0x34 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | addr\_stride\_out\_1 | | | | | | | | | | | |
|  | | | | RW - 0x0 0780 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| addr\_stride\_out\_1 | | | | | | | |  | | | | base\_addr\_out\_msb\_1 | | | |
| RW - 0x0 0780 | | | | | | | |  | | | | RW - 0x0 | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:8 | addr\_stride\_out\_1 | Address stride of the output image for IR (RGB-IR, YUV422-IR) or U/V (422/420 interleaved) channel. | RW  -  - | 0x0 0780 |
| 3:0 | base\_addr\_out\_msb\_1 | Base address of the output image for IR (RGB-IR, YUV422-IR) or U/V (422/420 interleaved) channel. | RW  -  - | 0x0 |

6

Register: base\_addr\_out\_2

|  |  |
| --- | --- |
| Description | : Third base address of the output image. |
| Offset | : 0x28 |
| Absolute Address | : 0x38 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| base\_addr\_out\_lsb\_2 | | | | | | | | | | | | | | | |
| RW - 0x01C0 0000 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| base\_addr\_out\_lsb\_2 | | | | | | | | | | | | | | | |
| RW - 0x01C0 0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | base\_addr\_out\_lsb\_2 | Base address of the output image for IR (422/420-IR interleaved) channel. | RW  -  - | 0x01C0 0000 |

6

Register: addr\_stride\_out\_2

|  |  |
| --- | --- |
| Description | : Third address stride of the output image for. |
| Offset | : 0x2C |
| Absolute Address | : 0x3C |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | addr\_stride\_out\_2 | | | | | | | | | | | |
|  | | | | RW - 0x0 0780 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| addr\_stride\_out\_2 | | | | | | | |  | | | | base\_addr\_out\_msb\_2 | | | |
| RW - 0x0 0780 | | | | | | | |  | | | | RW - 0x0 | | | |

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| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:8 | addr\_stride\_out\_2 | Address stride of the output image for IR (422/420-IR interleaved) channel. | RW  -  - | 0x0 0780 |
| 3:0 | base\_addr\_out\_msb\_2 | Base address of the output image for IR (422/420-IR interleaved) channel. | RW  -  - | 0x0 |

6

Register: input\_size

|  |  |
| --- | --- |
| Description | : Size of the input image. |
| Offset | : 0x30 |
| Absolute Address | : 0x40 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | input\_height | | | | | | | | | | | |
|  | | | | RW - 0x2D0 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | | | | input\_width | | | | | | | | | | | |
|  | | | | RW - 0x500 | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:16 | input\_height | Height of the input image. | RW  -  - | 0x2D0 |
| 11:0 | input\_width | Width of the input image. | RW  -  - | 0x500 |

6

Register: output\_size

|  |  |
| --- | --- |
| Description | : Size of the output image. |
| Offset | : 0x34 |
| Absolute Address | : 0x44 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | output\_height | | | | | | | | | | | |
|  | | | | RW - 0x2D0 | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | | | | output\_width | | | | | | | | | | | |
|  | | | | RW - 0x500 | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 27:16 | output\_height | Height of the output image. | RW  -  - | 0x2D0 |
| 11:0 | output\_width | Width of the output image. | RW  -  - | 0x500 |

6

Register: image\_format

|  |  |
| --- | --- |
| Description | : Input/output image format and color/ir enable signals. |
| Offset | : 0x38 |
| Absolute Address | : 0x48 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | ir\_enable |  | | | | | | | color\_enable |
|  | | | | | | | RW - 0x1 |  | | | | | | | RW - 0x1 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | | | | output\_format | | | |  | | | | input\_format | | | |
|  | | | | RW - 0x8 | | | |  | | | | RW - 0x8 | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 24 | ir\_enable | IR channel enable signal. | RW  -  - | 0x1 |
| 16 | color\_enable | Color channel enable signal. | RW  -  - | 0x1 |
| 11:8 | output\_format | Color format of the output image.  0 : YUV422-IR (2-plane).  1 : YVU422-IR (2-plane).  2 : UVY422-IR (2-plane).  3 : VUY422-IR (2-plane).  4 : YUV422-IR (3-plane).  5 : YVU422-IR (3-plane).  6 : YUV420-IR (3-plane).  7 : YVU420-IR (3-plane).  8 : IRRGB (1-plane).  9 : IRBGR (1-plane).  A : RGB-IR (2-plane).  B : BGR-IR (2-plane).  C : IR8BIT (1-plane).  D : IR16BIT (1-plane).  E : IR32BIT (1-plane). | RW  -  - | 0x8 |
| 3:0 | input\_format | Color format of the input image.  0 : YUV422-IR (2-plane).  1 : YVU422-IR (2-plane).  2 : UVY422-IR (2-plane).  3 : VUY422-IR (2-plane).  4 : YUV422-IR (3-plane).  5 : YVU422-IR (3-plane).  6 : YUV420-IR (3-plane).  7 : YVU420-IR (3-plane).  8 : IRRGB (1-plane).  9 : IRBGR (1-plane).  A : RGB-IR (2-plane).  B : BGR-IR (2-plane).  C : IR8BIT (1-plane).  D : IR16BIT (1-plane).  E : IR32BIT (1-plane). | RW  -  - | 0x8 |

6

Register: default\_color

|  |  |
| --- | --- |
| Description | : Default color for invalid pixels. |
| Offset | : 0x3C |
| Absolute Address | : 0x4C |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| default\_color | | | | | | | | | | | | | | | |
| RW - 0x8080 8080 | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| default\_color | | | | | | | | | | | | | | | |
| RW - 0x8080 8080 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 31:0 | default\_color | Default color in IRRGB format. | RW  -  - | 0x8080 8080 |

6

Block: mapping\_parameter\_regs

|  |  |
| --- | --- |
| Description | : |

3

Register: cam\_mat\_fx

|  |  |
| --- | --- |
| Description | : fx of the camera matrix. |
| Offset | : 0x0 |
| Absolute Address | : 0x50 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| fx | | | | | | | | | | | | | | | |
| RW - 0x3001 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | fx | fx of the camera matrix [U11F5]. | RW  -  - | 0x3001 |

6

Register: cam\_mat\_sx

|  |  |
| --- | --- |
| Description | : sx of the camera matrix. |
| Offset | : 0x4 |
| Absolute Address | : 0x54 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| sx | | | | | | | | | | | | | | | |
| RW - 0x10FD | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | sx | sx of the camera matrix [S4F12]. | RW  -  - | 0x10FD |

6

Register: cam\_mat\_cx

|  |  |
| --- | --- |
| Description | : cx of the camera matrix. |
| Offset | : 0x8 |
| Absolute Address | : 0x58 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cx | | | | | | | | | | | | | | | |
| RW - 0x4FEC | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | cx | cx of the camera matrix [U11F5]. | RW  -  - | 0x4FEC |

6

Register: cam\_mat\_fy

|  |  |
| --- | --- |
| Description | : fy of the camera matrix. |
| Offset | : 0xC |
| Absolute Address | : 0x5C |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| fy | | | | | | | | | | | | | | | |
| RW - 0x2FEE | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | fy | fy of the camera matrix [U11F5]. | RW  -  - | 0x2FEE |

6

Register: cam\_mat\_cy

|  |  |
| --- | --- |
| Description | : cy of the camera matrix. |
| Offset | : 0x10 |
| Absolute Address | : 0x60 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cy | | | | | | | | | | | | | | | |
| RW - 0x2CE2 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | cy | cy of the camera matrix [U11F5]. | RW  -  - | 0x2CE2 |

6

Register: dist\_coeff\_k1

|  |  |
| --- | --- |
| Description | : Distortion coefficient k1. |
| Offset | : 0x14 |
| Absolute Address | : 0x64 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | k1 | | | |
|  | | | | | | | | | | | | RW - 0x0 7E80 | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| k1 | | | | | | | | | | | | | | | |
| RW - 0x0 7E80 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 19:0 | k1 | Distortion coefficient k1 [S1F19]. | RW  -  - | 0x0 7E80 |

6

Register: dist\_coeff\_k2

|  |  |
| --- | --- |
| Description | : Distortion coefficient k2. |
| Offset | : 0x18 |
| Absolute Address | : 0x68 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | k2 | | | |
|  | | | | | | | | | | | | RW - 0x0 0C73 | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| k2 | | | | | | | | | | | | | | | |
| RW - 0x0 0C73 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 19:0 | k2 | Distortion coefficient k2 [S1F19]. | RW  -  - | 0x0 0C73 |

6

Register: dist\_coeff\_k3

|  |  |
| --- | --- |
| Description | : Distortion coefficient k3. |
| Offset | : 0x1C |
| Absolute Address | : 0x6C |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | k3 | | | |
|  | | | | | | | | | | | | RW - 0xF DE1F | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| k3 | | | | | | | | | | | | | | | |
| RW - 0xF DE1F | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 19:0 | k3 | Distortion coefficient k3 [S1F19]. | RW  -  - | 0xF DE1F |

6

Register: dist\_coeff\_k4

|  |  |
| --- | --- |
| Description | : Distortion coefficient k4. |
| Offset | : 0x20 |
| Absolute Address | : 0x70 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | k4 | | | |
|  | | | | | | | | | | | | RW - 0x0 0536 | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| k4 | | | | | | | | | | | | | | | |
| RW - 0x0 0536 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 19:0 | k4 | Distortion coefficient k4 [S1F19]. | RW  -  - | 0x0 0536 |

6

Register: homography\_h11

|  |  |
| --- | --- |
| Description | : h11 of the homography matrix. |
| Offset | : 0x24 |
| Absolute Address | : 0x74 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | h11 | |
|  | | | | | | | | | | | | | | RW - 0x3 DF79 | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| h11 | | | | | | | | | | | | | | | |
| RW - 0x3 DF79 | | | | | | | | | | | | | | | |

5

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| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 17:0 | h11 | h11 of the homography matrix [S-3F21]. | RW  -  - | 0x3 DF79 |

6

Register: homography\_h12

|  |  |
| --- | --- |
| Description | : h12 of the homography matrix. |
| Offset | : 0x28 |
| Absolute Address | : 0x78 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | h12 | |
|  | | | | | | | | | | | | | | RW - 0x0 1368 | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| h12 | | | | | | | | | | | | | | | |
| RW - 0x0 1368 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 17:0 | h12 | h12 of the homography matrix [S-9F27]. | RW  -  - | 0x0 1368 |

6

Register: homography\_h13

|  |  |
| --- | --- |
| Description | : h13 of the homography matrix. |
| Offset | : 0x2C |
| Absolute Address | : 0x7C |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | h13 | |
|  | | | | | | | | | | | | | | RW - 0x0 261B | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| h13 | | | | | | | | | | | | | | | |
| RW - 0x0 261B | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 17:0 | h13 | h13 of the homography matrix [S5F13]. | RW  -  - | 0x0 261B |

6

Register: homography\_h21

|  |  |
| --- | --- |
| Description | : h21 of the homography matrix. |
| Offset | : 0x30 |
| Absolute Address | : 0x80 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | h21 | |
|  | | | | | | | | | | | | | | RW - 0x3 DD8E | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| h21 | | | | | | | | | | | | | | | |
| RW - 0x3 DD8E | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 17:0 | h21 | h21 of the homography matrix [S-9F27]. | RW  -  - | 0x3 DD8E |

6

Register: homography\_h22

|  |  |
| --- | --- |
| Description | : h22 of the homography matrix. |
| Offset | : 0x34 |
| Absolute Address | : 0x84 |
| Addressing Mode | : 32-bits |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | h22 | |
|  | | | | | | | | | | | | | | RW - 0x3 E8B1 | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| h22 | | | | | | | | | | | | | | | |
| RW - 0x3 E8B1 | | | | | | | | | | | | | | | |

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| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 17:0 | h22 | h22 of the homography matrix [S-3F21]. | RW  -  - | 0x3 E8B1 |

6

Register: homography\_h23

|  |  |
| --- | --- |
| Description | : h23 of the homography matrix. |
| Offset | : 0x38 |
| Absolute Address | : 0x88 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | h23 | |
|  | | | | | | | | | | | | | | RW - 0x0 0BF0 | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| h23 | | | | | | | | | | | | | | | |
| RW - 0x0 0BF0 | | | | | | | | | | | | | | | |

5

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| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 17:0 | h23 | h23 of the homography matrix [S5F13]. | RW  -  - | 0x0 0BF0 |

6

Register: is\_fisheye

|  |  |
| --- | --- |
| Description | : Use fisheye model. |
| Offset | : 0x3C |
| Absolute Address | : 0x8C |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | | | | | | | | | | | | | | | is\_fisheye |
|  | | | | | | | | | | | | | | | RW - 0x1 |

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| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 0 | is\_fisheye | Whether to use fisheye model for lens distortion correction. | RW  -  - | 0x1 |

6

Block: peripheral\_configuration\_regs

|  |  |
| --- | --- |
| Description | : |

3

Register: cache\_timeout\_cnt

|  |  |
| --- | --- |
| Description | : Read cache timeout count. |
| Offset | : 0x0 |
| Absolute Address | : 0xA0 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| cache\_timeout\_cnt | | | | | | | | | | | | | | | |
| RW - 0x0000 | | | | | | | | | | | | | | | |

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | cache\_timeout\_cnt | Read cache timeout count.  Cache entries remaining longer than this count are flushed. | RW  -  - | 0x0000 |

6

Register: axi\_outstanding

|  |  |
| --- | --- |
| Description | : AXI maximum outstanding count. |
| Offset | : 0x4 |
| Absolute Address | : 0xA4 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | | max\_ros | | | | | |  | | max\_wos | | | | | |
|  | | RW - 0x0F | | | | | |  | | RW - 0x0F | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 13:8 | max\_ros | Maximum read outstanding count. | RW  -  - | 0x0F |
| 5:0 | max\_wos | Maximum write outstanding count. | RW  -  - | 0x0F |

6

Register: interrupt\_delay

|  |  |
| --- | --- |
| Description | : Done interrupt delay count. |
| Offset | : 0x8 |
| Absolute Address | : 0xA8 |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| done\_delay | | | | | | | | | | | | | | | |
| RW - 0x0100 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | done\_delay | Done interrupt delay count.  IREQ\_DONE signal is delayed by this count. | RW  -  - | 0x0100 |

6

Register: interrupt\_clear\_cnt

|  |  |
| --- | --- |
| Description | : Done interrupt clear count. |
| Offset | : 0xC |
| Absolute Address | : 0xAC |
| Addressing Mode | : 32-bits |

4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| done\_clear\_cnt | | | | | | | | | | | | | | | |
| RW - 0x0000 | | | | | | | | | | | | | | | |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 15:0 | done\_clear\_cnt | Done interrupt clear count.  IREQ\_DONE is cleared automatically after this count. | RW  -  - | 0x0000 |

6

Block: interrupt\_clear\_regs

|  |  |
| --- | --- |
| Description | : |

3

Register: interrupt\_clear

|  |  |
| --- | --- |
| Description | : Done interrupt clear signal. |
| Offset | : 0x0 |
| Absolute Address | : 0xB0 |
| Addressing Mode | : 32-bits |

4

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|  | | | | | | | | | | | | | | | done\_clear |
|  | | | | | | | | | | | | | | | RW - 0x0 |

5

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit | Name | Description | SW Access  HW Access  Protection | Reset |
| 0 | done\_clear | IREQ\_DONE interrupt clear signal. | RW  WC  - | 0x0 |

6

Access policy

|  |  |  |  |
| --- | --- | --- | --- |
| Access policy | Description | Effect of a Write on Current Field Value | Effect of a Read on Current Field Value |
| RO | Read Only | No effect. | No effect. |
| RW | Read Write | Changed to written value. | No effect. |
| RC | Read Clears All | No effect. | Sets all bits to 0. |
| RS | Read Sets All | No effect. | Sets all bits to 1. |
| WRC | Write, Read Clears All | Changed to written value. | Sets all bits to 0. |
| WRS | Write, Read Sets All | Changed to written value. | Sets all bits to 1. |
| WC | Write Clears All | Sets all bits to 0. | No effect. |
| WS | Write Sets All | Sets all bits to 1. | No effect. |
| WSRC | Write Sets All, Read Clears All | Sets all bits to 1. | Sets all bits to 0. |
| WCRS | Write Clears All, Read Sets All | Sets all bits to 0. | Sets all bits to 1. |
| W1C | Write 1 to Clear | If the bit in the written value is a 1, the corresponding bit in the field is set to 0. Otherwise, the field bit is not affected. | No effect. |
| W1S | Write 1 to Set | If the bit in the written value is a 1, the corresponding bit in the field is set to 1. Otherwise, the field bit is not affected. | No effect. |
| W1T | Write 1 to Toggle | If the bit in the written value is a 1, the corresponding bit in the field is inverted. Otherwise, the field bit is not affected. | No effect. |
| W0C | Write 0 to Clear | If the bit in the written value is a 0, the corresponding bit in the field is set to 0. Otherwise, the field bit is not affected. | No effect. |
| W0S | Write 0 to Set | If the bit in the written value is a 0, the corresponding bit in the field is set to 1. Otherwise, the field bit is not affected. | No effect. |
| W0T | Write 0 to Toggle | If the bit in the written value is a 0, the corresponding bit in the field is inverted. Otherwise, the field bit is not affected. | No effect. |
| W1SRC | Write 1 to Set, Read Clears All | If the bit in the written value is a 1, the corresponding bit in the field is set to 1. Otherwise, the field bit is not affected. | Sets all bits to 0. |
| W1CRS | Write 1 to Clear, Read Sets All | If the bit in the written value is a 1, the corresponding bit in the field is set to 0. Otherwise, the field bit is not affected. | Sets all bits to 1. |
| W0SRC | Write 0 to Set, Read Clears All | If the bit in the written value is a 0, the corresponding bit in the field is set to 1. Otherwise, the field bit is not affected. | Sets all bits to 0. |
| W0CRS | Write 0 to Clear, Read Sets All | If the bit in the written value is a 0, the corresponding bit in the field is set to 0. Otherwise, the field bit is not affected. | Sets all bits to 1. |
| W0 | Write Only | Changed to written value | No effect. |
| W0C | Write Only Clears All | Sets all bits to 0. | No effect. |
| W0S | Write Only Sets All | Sets all bits to 1. | No effect. |
| W1 | Write Once | Changed to written value if this is the first write operation after a hard reset. Otherwise, has no effect. | No effect. |
| W01 | Write Only, Once | Changed to written value if this is the first write operation after a hard reset. Otherwise, has no effect. | No effect. |

7