Politecnico di Torino

Collegio di Elettronica, Telecomunicazioni e Fisica

Report for the course
Integrated Systems Architecture

Master degree in Electrical Engineering

Group: XYZ

Names: John, Paul, George, Ringo

Signature 1: _____

Signature 2: _____

Signature 3: _____

Signature 4: _____

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Contents

CHAPTER 1

Lab 1: design and implementation of a digital filter

1.1 Reference model development

1.1.1 Matlab model

The frequency response of the filter is shown in Figure 1.1.

Figure 1.1: Caption for my first figure

The coefficients of the filter have one bit for the integer part and XYZ bits for the fractional part. They correspond to the integer values shown in Table 1.1.

1.1.2 C model and THD

The number of bits after each multiplication is XYZ and the THD is XYZ dB.

1.1.3 Explanations, comparisons and comments

As it can be observed ... bla, bla, bla, ...

Table 1.1: Caption for my first table

b_0	10
b_1	115
...	

1.2 VLSI implementation

1.2.1 Architecture

The architecture of the filter is shown in Figure 1.2 and the timing diagram in Figure 1.3.

Figure 1.2: Caption for my figure

Figure 1.3: Caption for my figure

Simulation

To process all the samples the simulation lasts XYZ ns. A snapshot from XYZ ns to KLM ns is shown in Figure 1.4 to highlight the behaviour of the filter when VIN moves from 0 to 1 and viceversa.

Figure 1.4: Caption for my figure

1.2.2 Logic synthesis

Snapshots showing slack met and power consumption are shown in Figures 5, 6 and 7.

Results of the synthesis are shown in Table 1.2.

1.2.3 Place and route

Snapshots showing no timing violation (timeDesign Summary table for both setup and hold modes) and power consumption are shown in Figures 8, 9 and 10.

Results of the place and route are shown in Table 1.3.

Figure 1.5: Figures 5, 6 and 7

Table 1.2: Caption for my table: A is the area, P is the power consumption and T is the simulation time.

f_M=...	A=...	-	T=...
$f_M/2$=...	A=...	P=...	T=...

1.2.4 Explanations, comparisons and comments

As it can be observed ... bla, bla, bla, ...

1.3 Advanced architecture development

Table 1.3: Caption for my table: A is the area, P is the power consumption and T is the simulation time.

$f_M/2$=...	A=...	P=...	T=...

Figure 1.6: Figures 8, 9 and 10

CHAPTER 2

Lab 2: digital arithmetic

2.1 FPU model

2.1.1 Simulation

The FPU has been stimulated with the following numbers, corresponding to the hexadecimal configuration shown in Table 2.1.

Figure ... shows a snapshot of the simulation. As it can be observed stimulating the FPU with the numbers shown in Table 2.1 the results are the expected ones.

2.1.2 Synthesis

Table ... shows the results of the experiments required in the assignment.

2.1.3 Explanations, comparisons and comments

As it can be observed ... bla, bla, bla, ...

2.1.4 R4-MBE multiplier

The circuit implementing the R4-MBE is shown in Fig. ... The Dadda-like tree is shown in Fig. ... with the required compressors. Moreover, the figure shows how sign extension has been simplified to avoid unnecessary compressors.

Simulation

Standalone multiplier Figure ... shows a snapshot of a simulation for the designed multiplier as a standalone block.

Whole FPU Figure ... shows a snapshot of a simulation for the designed multiplier included in the whole FPU.

Table 2.1: Caption ...

a		b		r	
15	0x4b80	204	0x5a60	3060	0x69fa
			...		

Synthesis

The results of the synthesis are shown in ... (you can add a new table or put the results as part of the previous table).

Explanations, comparisons and comments

As it can be observed ... bla, bla, bla, ...

CHAPTER 3

Lab 3: RISC-V-lite

3.1 Architecture definition

The code to run on the RISC-V-lite processor is:

```
.section .init, "ax"
.global _start
_start:
    .cfi_startproc
    .cfi_undefined ra
    .option push
    .option norelax
    la gp, __global_pointer$
    .option pop
    la sp, __stack_top
    add s0, sp, zero
    jal ra, main
el:
    j el
    .cfi_endproc
    .end
```

The architecture that has been designed is shown in Fig. 3.1

Figure 3.1: ...

3.1.1 Explanations and comments

As it can be observed ... bla, bla, bla, ...

3.2 Architecture verification

The architecture has been verified via simulation. Figs. 2 ... n show the obtained waveforms. In particular, Fig. $n-1$ shows that the pipeline is not sensitive to the memory latency and that the protocol works as expected. Finally, as shown in Fig, n, the total number of clock cycles to execute the *maxx* application with the fake memory wrapper is ...

3.2.1 Explanations and comments

As it can be observed ... bla, bla, bla, ...

3.3 Architecture - logic synthesis results

The maximum frequency achieved by the architecture is ... with a total area equal to .... Indeed, Figs. $n+1$ and $n+2$ show slack met and area breakdown.

3.3.1 Explanations and comments

As it can be observed ... bla, bla, bla, ...

3.4 Architecture - place and route

The maximum frequency achieved by the architecture is ... with a total area equal to .... Indeed, Figs. $n+1$ and $n+2$ show slack met and area breakdown.

3.4.1 Explanations and comments

As it can be observed ... bla, bla, bla, ...

3.5 Including the SSRAM in the architecture

The complete architecture with the SSRAMs is shown in Fig. $n+3$.

3.5.1 Explanations and comments

As it can be observed ... bla, bla, bla, ...

3.6 Complete architecture verification

The architecture has been verified via simulation, as shown by the following figures. In particular, Fig. XYZ shows that the total number of clock cycles to execute the code is ...

3.6.1 Explanations and comments

As it can be observed ... bla, bla, bla, ...

3.7 Complete architecture - logic synthesis results

The maximum frequency achieved by the advanced architecture is ... with a total area equal to .... Indeed, the following figures show slack met and area breakdown.

3.7.1 Explanations and comments

As it can be observed ... bla, bla, bla, ...