JFET Circuits II

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Introduction

In this lab, we built various useful electronics circuits using JFETs, such as amplifier, attenuator, modulator, timer and a phase splitter. Along with different combination of resistors and capacitors on the source, gate, and drain terminals, we explore what JFETs can be used for as well as scenarios in which JFET has its shortcomings. We further investigate the characteristics of JFETs through its effects on the circuits as well as the applications of the paired JFETs we obtained from lab 5.

5.1

We construct the amplifier as shown in Fig. 1.

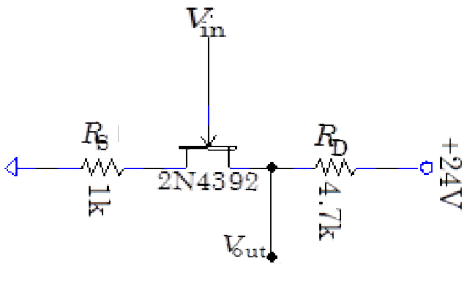

Figure 1: Schematic of an amplifier.

Without the signal applied, we measured the voltages across the respective terminals of the JFET and current through the drain and source to get a V_{GS} value of 1.60V±0.592 mV, V_{DS} of 11.42V ± 5.3704mV, I_{DS} of 0.0149± 2.188×10^{-6}mA. The theoretical gain is computed as below, by assuming that the assumption that the trans-conductance is high:

$$G = -\frac{R_D}{R_s + r_s} \approx -\frac{R_D}{R_s} \qquad (1)$$

and obtain a predicted gain of -4.7.

We drove the amplifier with a 10kHz , $1V_{pp}$ signal sine wave and record the V_out. The V_{out} is measured at 200mV when we input a signal of 1.00V. So we compute the gain by taking the ratio of the voltage output and input:

$$\text{Gain} = -\frac{V_{out}}{V_{in}} = \frac{1.00V}{200mV} = -5 \qquad (2)$$

The experimental value is within ≈ 10% of the theoretical predicted value.

As we tune the waveform generator, the maximum undistorted output amplitude is found to be 4.30V, and above that we can clearly see that the bottom part of the output signal is flat, as shown in Fig.2

The fact that the gain is also a function of the V_{in} is what limits the amplitude. The diode in the JFET rectifies the bottom portion of the signal as we have seen in the previous lab. But for a small signal amplitude, the effect is negligible, however for larger amplitude (¿4.3V) this functional dependency of the gain results in the distortion.

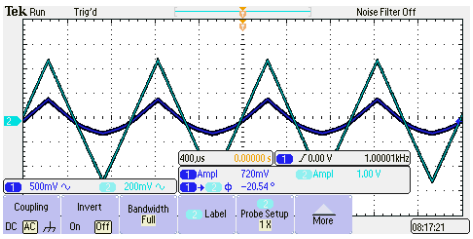

Figure 2: Scope trace for the distorted output signal. Channel 1 shows the output signal and Channel 2 shows the original input signal.

There is not much change in the output amplitude when the JFET is cooled, the gain remains at around 4, as we have previously found in 2. By substituting our JFET with four other JFETS and examining its cooling behaviour, we found that the gain for each JFET is still around 4 as shown in the $-\frac{V_{out}}{V_{in}}$ calculations below:

$$Gain_{JFET1} = -\frac{40.8V}{9.80V} = -4.16$$

$$Gain_{JFET2} = -\frac{40.0V}{9.80V} = -4.08$$

$$Gain_{JFET3} = -\frac{40.8V}{9.90V} = -4.12$$

$$Gain_{JFET4} = -\frac{40.8V}{9.80V} = -4.16$$

5.2

To improve the gain in the Fig.1 setup, we increased the R_D by a factor of ten. This decreases the V_{DS} substantially to 0.023V± 0.0028mV. The gain is much higher than in 5.1 :

$$\text{Gain} = -\frac{990mV}{16mV} = -61.9 \qquad (3)$$

The higher resistance results in a higher potential drop across R_D, so that no matter how big the gain is, the V_{out} is still very small. This is evident from the low value of V_{DS}, since the voltage drop can occur across R_D and across the source and drain of the JFET.

5.3

Again, we want to increase the gain: this time by decreasing the R_s in the denominator of Eq.4, which describes the common mode gain:

$$Gain = \frac{R_D}{2R_1 + R_s + r_s} \qquad (4)$$

In this new setup, the gain is now -6.43 [1].The maximum undistorted output amplitude is$1.80V_{pp}$, beyond this, the scope pattern flattens.

Cooling the JFET increases the V_{out}, therefore also increases the gain for the same input voltage. We tried these for four other JFETs as summarized in Table.1. The fractional variation in the gain is larger for this circuit than the Fig.1 setup is a result of the 500Ω source resistor. Since the impedance of the JFET is comparable to the 500Ω resistor, the JFET exhibits a stronger temperature dependence. This is not ideal for building electronic circuits and so increasing the gain is not as simple as simply increasing the source resistance.

JFET	Before	After
1	-6.04	-6.39
2	-7.43	-7.48
3	-3.74	-6.26
4	-4.17	-4.00

Table 1: Computed gain values for four JFETs, before and after cooling.The percentage increase of most JFETs were within 10% (With the exception of JFET 3 which seems to be an outlier.)

5.4

We increase the gain by bypassing the source resistor with the addition of a 1μF capacitor across the source resistor. By feeding in a 10kHz, 1V_{pp}, sine wave, the gain

[1] $\frac{-2.96V}{460mV} = -6.43$

we experimentally computed was -30.9. We compute the source resistance as the total impedance of the RC combination as :

$$Z = \frac{1}{\sqrt{(\frac{1}{R})^2 + (wc)^2}} \tag{5}$$

Plugging in w $=2\pi$(10kHz) and the nominal value for R, we get Z = 15.9Ω. Then we substitute this relation as source resistor (R_S) into the gain equation by :

$$G \approx \frac{-R_D}{R_S} = -\frac{4.7k\Omega}{15.9\Omega} \tag{6}$$

which yields a gain of around 296. We scan through different frequency and measure the V_{in}, V_{out} for computing the gain. We find that generally as the frequency increase, the gain also increases.

This bypassing setup still yields a temperature-dependent circuit. Cooling the JFET caused a 18.11% increase in the output voltage, and thereby the same percent change in the gain. Compared with the circuit in 5.3 this is even more temperature-dependent. This strong temperature dependence arise from the fact that temperature decrease results in a lower r_s. This results in a larger G, since G is inversely proportional to r_s as shown in Eq.6.

5.5

We built the differential amplifier as shown in 3 by connecting the two 100kΩ and 10kΩ resistors to ground. Driving the V_+, with 1kHz, 0.1V_{pp} sine wave, we get a signal amplitude of 3.00±3.64 × 10^{-4} V. Connecting the scope to the V_{invout} terminal, we get approximately the same amplitude. The phase measurement is 140.7° and -54° respectively.

Then we drive the V_- using the same signal and we again obtain a signal amplitude of 3.00±3.64 × 10^{-4} V. Connecting the scope to the V_{invout} terminal, we get approximately the same amplitude. The phase measurement is -82.50° and 70.00° respectively. Such behavior is expected because the two sides of the differential amplifier is supposed to exhibit symmetrical behavior, so it does not matter whether we drive on V_+ or V_-.

Next, we drive both V_+ or V_- with the same 0.1V signal and obtain V_{out} of 1.00V, so the common mode gain is around 10. By putting on a random JFET, the V_{out} is 1.35V. Along with the voltage drop measurement across the R_{drain} measured at 6.23V and another measured at 1.00V, this deviation from the previously measured voltage drop leads us to conclude that the differential amplifier circuit does not work anymore if we connect a pair of unmatched JFET.

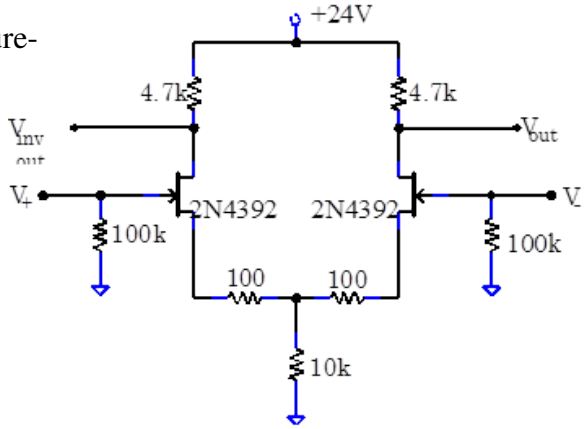

Figure 3: Differential amplifier schematic.

Due to the left-right symmetry of the circuit, the resulting voltage is approximately the same when driven from V_+ and V_-, and when measured from V_{invout} and V_{out}. There is a ≈180° phase shift between the input and output signal.

5.6

By driving a 100mV_{pp} input signal on both terminal we obtain the results summa-

V_{out}/V Amplitude (mV)	720	820
V_{out}/V Phase(°)	140.7	-82.50
V_{invout}/V Amplitude(mV)	710	860
V_{invout}/V Phase(°)	-54	70

Table 2: Amplitude and phase measurements from V_{invout} and V_{out}.

rized in Table.2.

5.7

We feed a 1kHz, 0.1V_{pp}, triangular wave and varied the output amplitude with the potentiometer on the attentuator, as shown in Fig.4. We find that the signal becomes distorted beyond a certain amplitude. The circuit is linear because it still retains the triangular form, however it becomes nonlinear as we go to amplitudes beyond 300mV. This is probably due to the JFET which has a linear (Ohmic) region at lower voltages [2] and exhibits nonlinear behaviors at higher voltages.

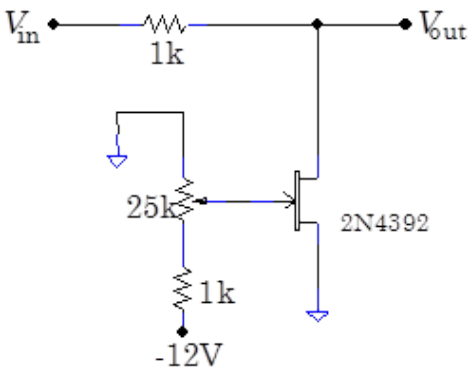

Figure 4: JFET Attenuator setup.

5.8

In order to linearize the attentuator shown in Fig.4, we added two 100kΩ resistors. We set the potentiometer so that we achieve the greatest attenuation on the input signal. Treating the whole red boxed region as R_2 in Fig.6, we use the voltage divider equation to find the drain source resistance:

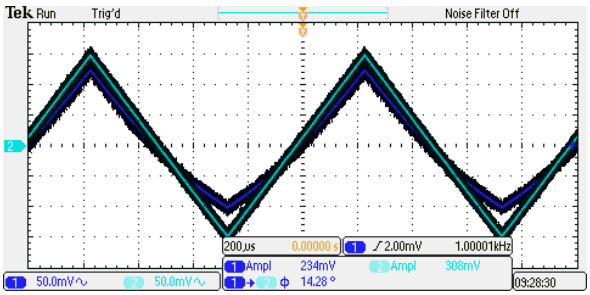

Figure 5: Channel 1 shows the distorted signal for an amplitude slightly beyond 300mV. This can be compared with the Channel 2 original signal in cyan.

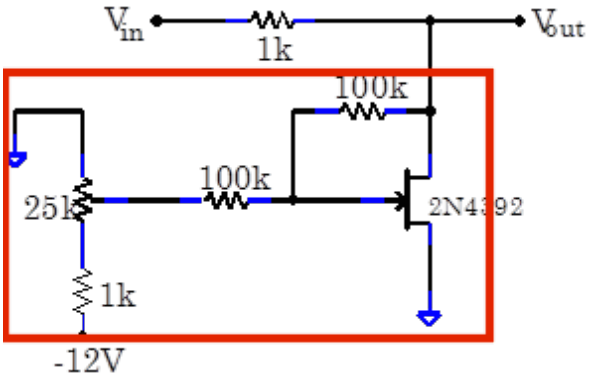

Figure 6: JFET Attenuator schematic.

$$V_{out} = \frac{R_2}{R_1 + R_2} V_{in}$$

$$230mV = \frac{R_2}{1000\Omega + R_2}(318mV)$$

Solving for R_2 yields 2613Ω, this is the lowest possible JFET drain-source resistance corresponding to this setting.

The largest input signal that can pass relatively distorted is 500mV. After setting the potentiometer to this maximum attainable attentuation, we measured the gate source voltage as 3.1263V±0.8mV and the drain source

[2] Towards the left hand side of the JFET characteristic curve which plots I_D and V_{DS}.

voltage as 30.259mV±0.008mV. The V_{in} is measured at 3.18mV±0.04mV and V_{out} is measured at 230mV±0.03mV.

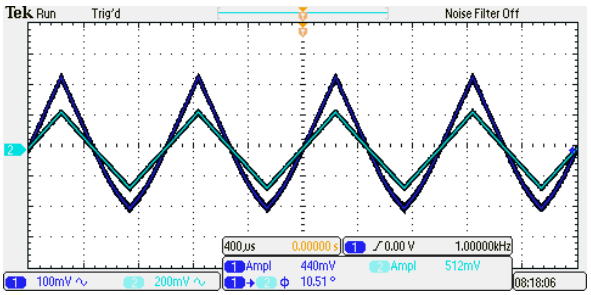

Figure 7: The Channel 1 trace shows that beyond the limit of 500mV, the signal can become distorted.

5.9

We built the JFET Modulator circuit as shown in Fig. 8 and feding in a $1V_{pp}$input carrier wave of 1MHz, by adding a 1.0μF capacitor to the JFET attenuator circuit. Using another function generator to drive the a 1kHz, $1V_{pp}$ sine wave on the potentiometer gate signal, we find that the input carrier wave (1MHz) is modulated by the 1kHz wave. The modulated output signal is shown in Fig.9.

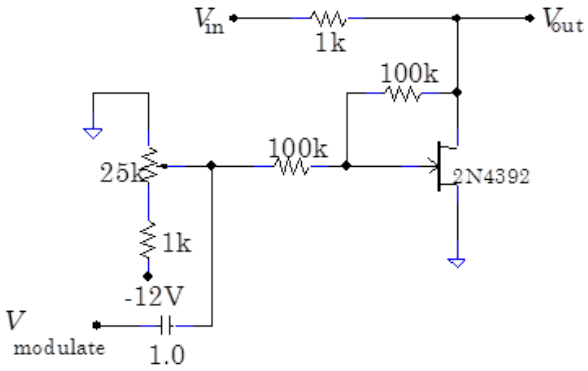

Figure 8: JFET Modulator schematic.

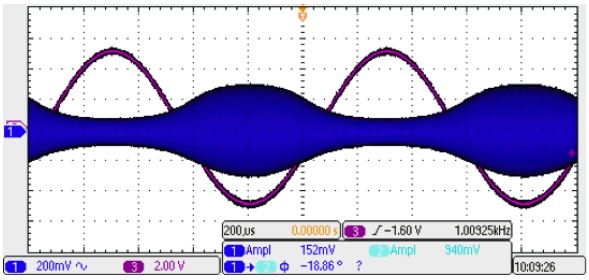

Figure 9: Scope traces for the AM signal. Channel 1 shows the modulated V_{out}, whose amplitude has a lower resulting amplitude than the 1kHz signal in Channel 3.

5.10

We tune the AM radio to a quiet channel in the AM band at around 540kHz. The wire is connected to the V_{out} and acts as an AM transmitter for the output signal. We tune the frequency of the modulating signal from the wave generator and then heard the audio signal when the modulating frequency is adjusted to 552kHz. This modulating frequency is very close to the bands that our AM radio is tuned to detect. [3]

5.11

Due to the left-right symmetry on both sides of the differential amplifier, [4] both JFETs responds the same way to the . As the differential amplifier is built from a matched pair of transistors on both sides. Therefore it is value to assume that the transistors are approximately identical, having a common mode drive. The common mode gain is computed by:

$$\text{Gain} = \frac{R_D}{2Z_{out} + R_s + r_s} = \frac{R_D}{2Z_{out} + R_s + 1/g}$$

[3] We also found that the signal sounds a lot cleaner if we coiled the transmitting wire around the antenna of the AM radio receiver.

[4] In theory, the same JFET,R_D and R_S.

where g is the JFET's trans-conductance [5]

The differential gains for the differential amplifier is computed as :

$$\text{Gain} = \frac{R_D}{R_S + r_s} = \frac{R_D}{R_S + 1/g}$$

5.12

We fed in +24V input on both sides of the surprise circuit as shown in Fig.12. The

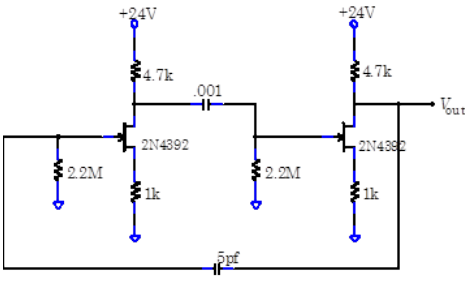

Figure 10: Surprise circuit setup.

circuit acts like a periodic timer, outputting a square wave with period of 1200μs. This happens because the voltage through the 0.001μF capacitor pinches off. Then, after some time period, the capacitor charges up and the 5pF capacitor also pinches off. Since there is quite a difference between the capacitance of the two capacitor, this explains the pattern shown in Fig.11 as the signal is comprised of a prolonged flattened region followed by a short dip (which is actually a much shorter flattened region).

5.13

We designed and built a unity gain phase splitter as shown in Fig.12. We connected a 12V power supply to the V_{out+} terminal and fed in a 1V_{pp}, 1kHz sine wave.

As intended, the circuit splits the input signal into two signal (as shown on Channel

[5]This should be simmilar for both JFETs

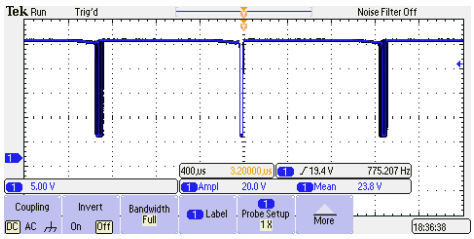

Figure 11: Channel 2 shows the original DC signal, which is just noise.

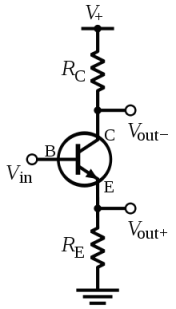

Figure 12: Phase Splitter Design. We set both the R_E and the R_C equal to 10kΩ in order to split the two signals into equal magnitude and opposite phase.

1 and 3 of Fig.13). We observe that these two signals are almost 180° out of phase with each other. The phase splitting resulted in a V_{out-} output signal amplitude that is a few orders of magnitude less thanV_{out+}. This is due to the fact that the roughly-half-a-period phase shift causes the superposition of the input signal and the V_{out-} to almost zero (24.8mV), whereas the superposition of the input and the V_{out+} adds up to a larger amplitude of 0.70V.

5.14

We built a temperature, and JFET-independent high gain amplifier as shown in Fig.14. We substituted a R_1resistor of 520kΩ and a $R_2$1kΩ resistor for the circuit. The gain was computed from the input and output voltage ratio as $\frac{9.12V}{228mV} = 40$. Unlike the previous circuits that we built, the circuit was not per-

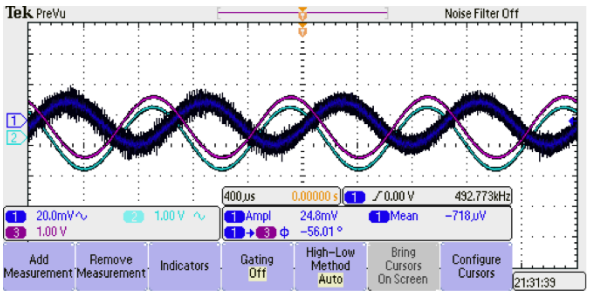

Figure 13: Channel 1 shows the measure of V_{out-} ; Channel 2 shows the original input signal; Channel 3 shows the V_{out+}

turbed as we cooled it and maintained approximately the same gain .

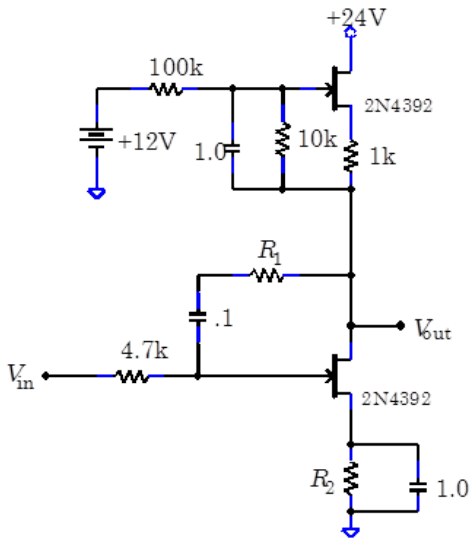

Figure 14: High Gain Amplifier Circuit

Using an unmatched JFET, the gain was reduced to 14 ($\frac{1.44V}{0.10V}$). Using a new unmatched pair of JFET the gain decreased to a even lower value of 2. The distinction between the former and latter case is that the R_1 and R_2 we used was not chosen to be the right ones for obtaining a gain of 40 for the new JFETs. However this should not have mattered because the feedback designed in this high gain amplifier should have made the circuit independent of JFET characteristics. Since the JFET is operating at the linear regime, the gain of the circuit can be simply calculated as a voltage divider:

$$\text{Gain} = -\frac{R_D}{R_s + r_s} = -\frac{R_D}{Z_{out} + 1/g} \quad (7)$$

where the Z_{out} is the finite stiffness of the current source and g is the transconductance of the JFET, following the same line of reasoning in our 5.11 differential gain derivation.

5.15

1. The R_1 and the associated subcircuit containing 0.1μF capacitor sets the gain through feedback since it has direct control over V_{out}, which is used to compute the gain.
2. The entire top half of the circuit acts as a current source to increase the gain. This current source is has high current gain and is self-biased. It serves as a stiff current source to the lower half of the circuit.
3. The R_2 resistor and 1μF capacitor increases the open-loop gain by providing an AC bypass capacitor.
4. The lower part of circuit JFET operates in a linearize regime, therefore we can treat the JFET's impedance as a resistor. The R_2 and 1μF capacitor
5. The 12V voltage supply assures that the drain source voltage across both JFETs is approximately 12V. This 12V voltage supply is independent of the JFET characteristic.
6. There is an oscillation of current between 1.0μF capacitor in the top half of the circuit until it equilibriates. This provides a bypass for AC signals and increases the stiffness of the current source.

Conclusion

In this lab, we investigated the various applications of JFETs in electronic circuits. We build and design an amplifier, attenuator, modulator, timer and a phase splitter using JFETs along with different combination of resistors and capacitors on the source, gate, and drain terminals. We further explore the characteristics of JFETs through its effects on the circuits such as the temperature-dependent gain in 5.3 and the importance of the "matched" JFETs as seen in 5.5. Finally, we investigate an operational amplifier circuit contructed from JFETs.

Acknowledgments

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