# UART module doc

In this document you will find the UART module component description.

## Overview

This UART module is basically gathering two state machines to handle the RX and TX ports of the FPGA.

The entire module is wrapped with Avalon-MM interface (slave form) and, in the current project, integrated with a JTAG to Avalon Master Bridge unit inside a QSYS system.

The Avalon span is a 1B (8b) wide, with an address span of 1b.

Altogether, the Avalon interface addresses two internal registers, one for rxdata and one for txdata, both registered are “avalonian” intermediate level for the txd and rxd ports.

This resembles the qsys component for the uart RS-232, but is ready for the USB-TTL I/O pins of the FPGA.

This is also the basis for the future communication interface for a control unit.