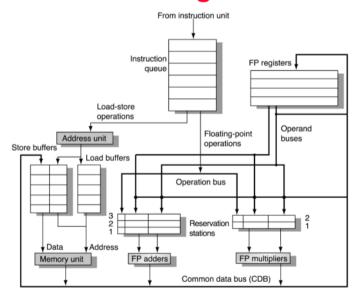
# **Examples of behavior of the Tomasulo's architecture**

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#### **Tomasulo Organization**



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#### **Reservation Station Components**

- Op—Operation to perform in the unit (e.g., + or –)
- Qj, Qk—Reservation stations producing source registers
- Vj, Vk—Value of Source operands
- Rj, Rk—Flags indicating when Vj, Vk are ready
- **Busy—Indicates reservation station and FU is busy**

Register result status—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions that will write that register.

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#### **Three Stages of Tomasulo Algorithm**

1. Issue—get instruction from FP Op Queue

If reservation station free, the scoreboard issues instr & sends operands (renames registers).

2. Execution—operate on operands (EX)

When both operands ready then execute; if not ready, watch CDB for result

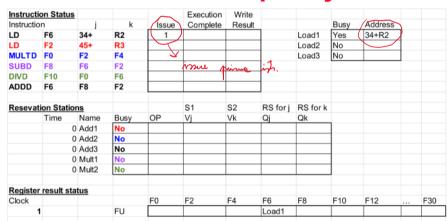
3. Write result—finish execution (WB)

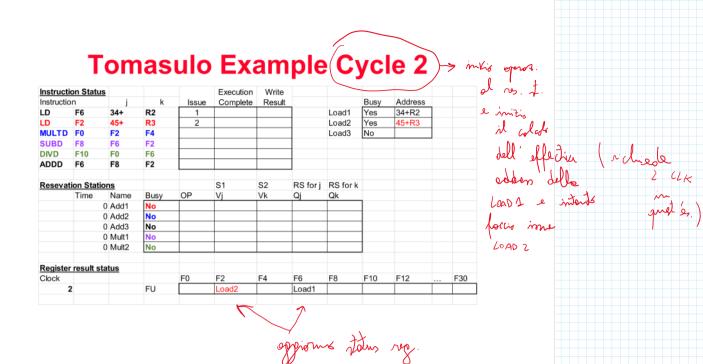
Write on Common Data Bus to all awaiting units; mark reservation station available.

Instructi	on Status				Execution	Write									
Instruction	n	j	k	Issue	Complete	Result			Busy	Address					
LD	F6	34+	R2					Load1	No					1	~ _ ~
LD	F2	45+	R3					Load2	No			$\nearrow$		L	$\mathcal{S}$
MULTD	F0	F2	F4				1 \	Load3	No			)			FFER
SUBD	F8	F6	F2				1							Die	
DIVD	F10	F0	F6											120-	t + F C
ADDD	F6	F8	F2					_							. ( ) .
Resevat	tion Statio	ns			S1	S2	RS for j	RS for k							
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk							
	(	Add1	No						1)						
	(	Add2	No						1 POT	17719110	3 00	Į.	NO		
	(	Add3	No						1)			ملم	1 ml-		
	(	Mult1	No						15			-			(
	(	Mult2	No						] } ^	1221910 2 pa	DIV	/m UK T	(onche	ne i	li
Register	result sta	atus											solibe	man, s	i cosi
Clock				F0	F2	F4	F6	F8	F10	F12		F30			
(	0		FU										]		

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#### **Tomasulo Example Cycle 1**





Instruction	on Status				Execution	Write							
Instructio	n	j	k	Issue	Complete	Result			Busy	Address			
LD	F6	34+	R2	1	(3)			Load1	Yes	34+R2			
LD	F2	45+	R3	2		1.1		Load2	Yes	45+R3			
MULTD	F0	F2	F4	3		Media		Load3	No				
SUBD	F8	F6	F2			Hours	μ ,	12					
DIVD	F10	F0	F6			odore	b cal	راه لهر	1				
ADDD	F6	F8	F2				1. 40	400	O				
Resevat	ion Station	าร			S1	S2	RS for j	RS for k					
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk					
	0	Add1	No		Τ'				1				
	0	Add2	No										1.
	0	Add3	No									11	7()
	0	Mult1	Yes	MULTD		R[F4]	Load2		4		Mad	him	X - 100
	0	Mult2	No						,				l-m Π5.5
Register	result sta	tus										<u> </u>	1665.
Clock				F0	F2	F4	F6	F8	F10	F12		F30	
3	3		FU	Mult1	Load2		Load1						7

Instructi	on Status				Execution	Write							
Instructio	n	j	k	Issue	Complete	Result			Busy	Address			
LD	F6	34+	R2	1	3	4		Load1	No				
LD	F2	45+	R3	2	4			Load2	Yes	45+R3			
MULTD	F0	F2	F4	3				Load3	No				
SUBD	F8	F6	F2	4									
DIVD	F10	F0	F6										
ADDD	F6	F8	F2										
Resevat	ion Station	<u>15</u>			S1	S2	RS for j	RS for k					
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk					
	0	Add1	Yes	SUBD	M[34+R2]			Load2	6	- ς	0117	'n.	RES. ST.
	0	Add2	No									, ,	
	0	Add3	No										
	0	Mult1	Yes	MULTD		R[F4]	Load2						
	0	Mult2	No										
Register	result sta	tus											
Clock				F0	F2	F4	F6	F8	F10	F12		F30	
4	1		FU	Mult1	Load2		M[34+R2]	Add1					
								1					

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## **Tomasulo Example Cycle 5**

Instructi	on Status				Execution	Write						
Instructio	n	j	k	Issue	Complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4								
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2									
Resevat	ion Statio	ns			S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	(	Add1	Yes	SUBD	M[34+R2]	M[45+R3	1		1			
	(	Add2	No		<b>—</b>							16610ru DAT1
	(	Add3	No							-	_ ′	14 0.01
	(	Mult1	Yes	MULTD	M[45+R3]	R[F4]			1			PATI
	(	Mult2	Yes	DIVD		M[34+R2	Mult1					\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Register	result sta	atus										
Clock				F0	F2	F4	F6	F8	F10	F12		F30
5	5		FU	Mult1	M[45+R3]		M[34+R2]	Add1	Mult2			



Instructi	on Status				Execution	Write					
Instructio	n	j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4							
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6							
Resevat	ion Station	ns			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	2	Add1	Yes	SUBD	M[34+R2]	M[45+R3]					
	0	Add2	Yes	ADDD		M[45+R3]	Add1				
	0	Add3	No								
	10	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
	0	Mult2	Yes	DIVD		M[34+R2	Mult1		4	mema	non
										na d	i gret
Register	result sta	<u>ıtus</u>								700	a show
Clock				F0	F2	F4	F6	F8	F10	F12	F30
6	3		FU	Mult1	M[45+R3]		Add2	Add1	Mult2		

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#### **Tomasulo Example Cycle 7**

LD F6 34+ R2 1 3 4 Load1 No	structio	n Status				Execution	Write					
LD	struction	n	j	k	Issue	Complete	Result			Busy	Address	
MULTD         F0         F2         F4         3         Load3         No           SUBD         F8         F6         F2         4         7           DIVD         F10         F0         F6         5           ADDD         F6         F2         6           Resevation Stations         S1         S2         RS for j         RS for k           Qi         Qk         Qj         Qk           1 Add1         Yes         SUBD         M[34+R2]         M[45+R3]           0 Add2         Yes         ADDD         M[45+R3]         Add1           9 Mult1         Yes         MULTD         M[45+R3]         R[F4]           0 Mult2         Yes         DIVD         M[34+R2]         Mult1           Register result status         F0         F2         F4         F6         F8         F10         F12	)	F6	34+	R2	1	3	4		Load1	No		
SUBD   F8   F6   F2   4   7	)	F2	45+	R3	2	4	5		Load2	No		
DIVD	JLTD	F0	F2	F4	3				Load3	No		
Resevation Stations	JBD	F8	F6	F2	4	7						
S1   S2   RS for j   RS for k	VD	F10	F0	F6	5			R				
Time Name 1 Add1 Yes SUBD M[34+R2] M[45+R3]	DDD	F6	F8	F2	6			1				
1 Add1	sevatio	on Station	<u>15</u>			S1	S2	RS for j	RS for k			
0 Add2		Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
0 Add3		1	Add1	Yes	SUBD	M[34+R2]	M[45+R3]					
9 Mult1		0	Add2	Yes	ADDD		M[45+R3]	Add1				
0 Mult2 Yes DIVD M[34+R2] Mult1    Register result status   F0   F2   F4   F6   F8   F10   F12		0	Add3	No								
Register result status         F0         F2         F4         F6         F8         F10         F12		9	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
Clock F0 F2 F4 F6 F8 F10 F12		0	Mult2	Yes	DIVD		M[34+R2]	Mult1				
	egister	result sta	tus									
	ock				F0	F2	F4	F6	F8	F10	F12	 F30
7   FU   Mult1   M[45+R3]   Add2   Add1   Mult2	7			FU	Mult1	M[45+R3]		Add2	Add1	Mult2		

Instructi	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6							
Resevat	ion Station	<u>15</u>			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No								
	0	Add2	Yes	ADDD	MD-MD	M[45+R3]					
	0	Add3	No								
	8	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1				
Register	result sta	tus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
8	3		FU	Mult1	M[45+R3]		Add2	M[]-M[]	Mult2		
								A			

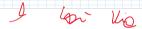
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#### **Tomasulo Example Cycle 9**

Instruction	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6							
Resevat	ion Station	ıs			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No								
	2	Add2	Yes	ADDD	M[]-M[]	M[45+R3]					
	0	Add3	No								
	7	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1				
Register	result sta	tus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
g	1		FU	Mult1	M[45+R3]		Add2	МП-МП	Mult2		

Instructi	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10						
Resevat	ion Station	ns			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No						]		
	1	Add2	Yes	ADDD	M[]-M[]	M[45+R3]					
	0	Add3	No								
	6	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1				
Register	result sta	tus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
10	)		FU	Mult1	M[45+R3]		Add2	M[]-M[]	Mult2		

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## **Tomasulo Example Cycle 11**

Instruction	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					
Resevat	on Station	ıs			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No						1		
	0	Add2	No								
	0	Add3	No								
	5	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1				
Register	result stat	tus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
11			FU	Mult1	M[45+R3]		(M-M)+M	МП-МП	Mult2		

Instructi	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					
Resevat	ion Station	ns			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No						]		
	0	Add2	No								
	0	Add3	No								
	4	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
	0	Mult2	Yes	DIVD		M[34+R2	Mult1				
Register	result sta	tus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
12	2		FU	Mult1	M[45+R3]		Add2	M[]-M[]	Mult2		

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#### **Tomasulo Example Cycle 13**

Instruction	on Status				Execution	Write						
		j	k	Issue	Complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No		1	
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3				Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						
Resevat	ion Station	<u>18</u>			S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	3	Mult1	Yes	MULTD	M[45+R3]	R[F4]						
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1					
Register	result sta	tus										
Clock				F0	F2	F4	F6	F8	F10	F12		F30
13			FU	Mult1	M[45+R3]		(M-M)+M	MATL MATL	Mult2			

Instructi	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3				Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					
Resevat	ion Station	ns			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No		Τ				1		
	0	Add2	No								
	0	Add3	No								
	2	Mult1	Yes	MULTD	M[45+R3]	R[F4]					
	0	Mult2	Yes	DIVD		M[34+R2	Mult1				
Register	result sta	tus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
14	ı		FU	Mult1	M[45+R3]		(M-M)+M	M[]-M[]	Mult2		

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## **Tomasulo Example Cycle 15**

Instruction	on Status				Execution	Write						
		j	k	Issue	Complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No			
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3	15			Load3	No			
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5								
ADDD	F6	F8	F2	6	10	11						
Resevat	on Station	ıs			S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	1	Mult1	Yes	MULTD	M[45+R3]	R[F4]						
	0	Mult2	Yes	DIVD		M[34+R2]	Mult1					
Register	result sta	tus										
Clock				F0	F2	F4	F6	F8	F10	F12		F30
15			FU	Mult1	M[45+R3]		(M-M)+M	мп-мп	Mult2		$T^{-}$	

Instructi	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3	15	16		Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					
Resevat	ion Statio	ns			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	(	Add1	No								
	(	Add2	No								
	(	Add3	No								
	(	Mult1	No								
	(	Mult2	Yes	DIVD	M*F4	M[34+R2]					
Register	result sta	itus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
16	5		FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2		

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## **Tomasulo Example Cycle 17**

LD F6 34+ R2 1 3 4 Load1 No  LD F2 45+ R3 2 4 5 Load2 No  MULTD F0 F2 F4 3 15 16 Load3 No  SUBD F8 F6 F2 4 7 8  DIVD F10 F0 F6 5 ADDD F6 F8 F2 6 10 11  Resevation Stations  Time Name Busy OP Vj Vk Qj Qk  0 Add1 No 0 Add2 No 0 Add3 No 0 Mult1 No 40 Mult2 Yes DIVD M*F4 M[34+R2]	uction 5	Status				Execution	Write					
No   No   No   No   No   No   No   No			j	k	Issue	Complete	Result			Busy	Address	
MULTD F0         F2         F4         3         15         16         Load3         No           SUBD F8         F6         F2         4         7         8           DIVD F10         F0         F6         5         —           ADDD F6         F8         F2         6         10         11           Resevation Stations           Time         Name         Busy         OP         Vj         Vk         Qj         Qk           0 Add1         No         —         —         —         —         Qj         Qk           0 Add3         No         —	F6	-6	34+	R2	1	3	4		Load1	No		
SUBD   F8   F6   F2   4   7   8	F2	2	45+	R3	2	4	5		Load2	No		
DIVD	TD F0	<del>-</del> 0	F2	F4	3	15	16		Load3	No		
ADDD F6 F8 F2 6 10 11    Resevation Stations   S1 S2 RS for j RS for k	D F8	8	F6	F2	4	7	8					
S1   S2   RS for j   RS for k	) F1	10	F0	F6	5							
Time Name Busy OP Vj Vk Qj Qk  0 Add1 No 0 Add2 No 0 Add3 No 0 Mult1 No 40 Mult2 Yes DIVD M*F4 M[34+R2]	D F6	-6	F8	F2	6	10	11					
0 Add1	evation	n Statior	ns			S1	S2	RS for j	RS for k			
0 Add2 No	Tir	Γime	Name	Busy	OP	Vj	Vk	Qj	Qk			
0 Add3 No		0	Add1	No								
0 Mult1 No		0	Add2	No								
40 Mult2 Yes DIVD M*F4 M[34+R2]  Register result status		0	Add3	No								
Register result status		0	Mult1	No								
		40	Mult2	Yes	DIVD	M*F4	M[34+R2]					
Clock F0 F2 F4 F6 F8 F10 F12	ster res	esult sta	tus									
	k				F0	F2	F4	F6	F8	F10	F12	 F30
17 FU M*F4 M[45+R3] (M-M)+M M[]-M[] Mult2	17			FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2		

Instructi	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3	15	16		Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5							
ADDD	F6	F8	F2	6	10	11					
Resevat	ion Station	ns			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	0	Add1	No						1		
	0	Add2	No								
	0	Add3	No						1		
	0	Mult1	No								
	39	Mult2	Yes	DIVD	M*F4	M[34+R2]					
Register	result sta	tus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
18	3		FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2		

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## **Tomasulo Example Cycle 56**

Instructi	on Status				Execution	wnte						
		j	k	Issue	Complete	Result			Busy	Address		
LD	F6	34+	R2	1	3	4		Load1	No		1	
LD	F2	45+	R3	2	4	5		Load2	No			
MULTD	F0	F2	F4	3	15	16		Load3	No		1	
SUBD	F8	F6	F2	4	7	8						
DIVD	F10	F0	F6	5	56							
ADDD	F6	F8	F2	6	10	11						
Resevat	ion Station	ns			S1	S2	RS for j	RS for k				
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk				
	0	Add1	No									
	0	Add2	No									
	0	Add3	No									
	0	Mult1	No									
	1	Mult2	Yes	DIVD	M*F4	M[34+R2]						
Register	result sta	<u>tus</u>										
Clock				F0	F2	F4	F6	F8	F10	F12		F30
56	6		FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	Mult2			

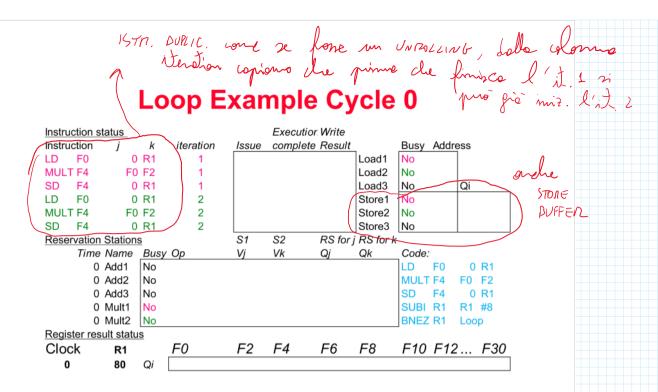
Instructi	on Status				Execution	Write					
		j	k	Issue	Complete	Result			Busy	Address	
LD	F6	34+	R2	1	3	4		Load1	No		
LD	F2	45+	R3	2	4	5		Load2	No		
MULTD	F0	F2	F4	3	15	16		Load3	No		
SUBD	F8	F6	F2	4	7	8					
DIVD	F10	F0	F6	5	56	57					
ADDD	F6	F8	F2	6	10	11					
Resevat	ion Statio	ns			S1	S2	RS for j	RS for k			
	Time	Name	Busy	OP	Vj	Vk	Qj	Qk			
	(	Add1	No								
	(	Add2	No								
	(	Add3	No								
	(	Mult1	No								
	(	Mult2	No								
Register	result sta	itus									
Clock				F0	F2	F4	F6	F8	F10	F12	 F30
57	7		FU	M*F4	M[45+R3]		(M-M)+M	M[]-M[]	M*F4/M		

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#### **Tomasulo Loop Example**

Loop: LD F0 R1 0 MULTD F4 F0 F2 SD F4 0 R1 SUBI R1 R1 #8 R1 **BNEZ** Loop

- Multiply takes 4 clock cycles
- · Loads have cache misses



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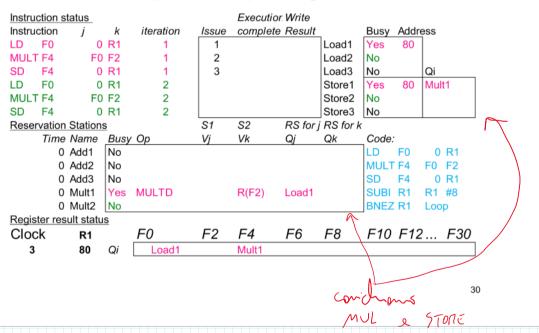
#### **Loop Example Cycle 1**

Instruc	tion s	tatus				Execution	Write					
Instruc	ction	j	k	iteration	Issue	complete	Result		Busy	Addre	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1				Load2	No			
SD	F4	0	R1	1				Load3	No		Qi	
LD	F0	0	R1	2				Store1	No			
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	Stations	3		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	No						SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	р
Regist	er res	ult status	<u>s</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
1		80	Qi	Load1								

Instruc	ction s	tatus				Execution	Write					
Instruc	ction	j	k	iteration	Issue	complete	Result		Busy	Addre	ess	
LD	F0	0	R1	1	1			Load1	Yes	80		
MULT	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1				Load3	No		Qi	
LD	F0	0	R1	2				Store1	No			
MULT	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Reser	vation	Stations	3		S1	S2	RS for j	RS for k				
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MULT	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUBI	R1	R1	#8
	0	Mult2	No						BNEZ	R1	Loo	)
Regist	er res	ult statu	<u>s</u>									
Cloc	k	R1		F0	F2	F4	F6	F8	F10	F12		F30
2		80	Qi	Load1		Mult1						

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#### **Loop Example Cycle 3**



Instru	uction	status	<u>s_</u>			Executi	Write					
Instru	uction	j	k	iteration	Issue	complet	Result	t	Busy	Add	ress	5
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2	$\sim$		Load2	No			
SD	F4	0	R1	1	3	(/4)		Load3	No		Qi	
LD	FO	0	R1	2				Store1	Yes	80	Mul	lt1
MUL	F4	FO	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	) <i>:</i>		
	0	Add1	No						LD	FO	0	R1
	0	Add2	No						MUL.	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loc	р
Regis	ster r	esult s	tatus									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F30
4		80	Qi	Load1		Mult1						

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## **Loop Example Cycle 5**

Instru	uction	status	<u>s_</u>			Executi	Write					
Instru	uction	j	k	iteration	Issue	comple	Result	t	Busy	Add	ress	5
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2				Store1	Yes	80	Mul	t1
MUL	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	e:		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loc	р
Regi	ster r	esult s	tatus	1								
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F30
5		80	Qi	Load1		Mult1						

Instru	uctior	j	k	iteration	Issue	comple	Result	t	Busy	Add	ress	3
LD	F0	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	F0	0	R1	2	6			Store1	Yes	80	Mu	lt1
MUL	F4	F0	F2	2				Store2	No			
SD	F4	0	R1	2				Store3	No			
Rese	ervatio	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code	e:		
	0	Add1	No						LD	FO	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loc	p
Regi	ster r	esult s	tatus									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F3C
6		72	Qi	Load2		Mult1						

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## **Loop Example Cycle 7**

Instru	uctior	j	k	iteration	Issue	comple	Result	t	Busy	Add	ress	3
LD	FO	0	R1	1	1			Load1	Yes	80		
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	FO	0	R1	2	6			Store1	Yes	80	Mu	t1
MUL	F4	FO	F2	2	7			Store2	No			
SD	F4	0	R1	2				Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	e <i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
	0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loc	р
Regi	ster r	esult s	tatus	1								
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F3C
7		72	Qi	Load2		Mult2						

Instr	uction	j	k	iteration	Issue	comple	Result	t	Busy	Add	ress	6
In LD	FO	0	R1	1	1			Load1	Yes	80		
LIMUI	- F4	F0	F2	1	2			Load2	Yes	72		
MSD	F4	0	R1	1	3	4		Load3	No		Qi	
SISUE	R1	R1	#8	1	4	5	6					
LIBNE	R1	Loop		1	5		-					
MLD	FO	0	R1	2	6	$\mathcal{L}$		Store1	Yes	80	Mu	lt1
SIMUL	_ F4	FO	F2	2	7	DOP	0 IL	Store2	No			
R(SD	F4	0	R1	2		RESULT of		Store3	No			
Res	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code	<b>:</b> :		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
R	0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loc	ор
CReg	ister r	esult s	tatus	1								
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F30

## **Loop Example Cycle 8**

Instr	uctior	j	k	iteration	Issue	comple	Resul	t	Busy	Add	ress	3
LD	FO	0	R1	1	1			Load1	Yes	80		
MUL	. F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	FO	0	R1	2	6			Store1	Yes	80	Mu	t1
MUL	F4	FO	F2	2	7			Store2	Yes	72	Mu	t2
SD	F4	0	R1	2	8			Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	ə <i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8
	0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loc	р
Regi	ister r	esult s	tatus	1								
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1		F3C
8	3	72	Qi	Load2		Mult2						

							CA	nyle	lo i	M	9	LC	0			C	Ge	Ger	Gen	Gen	Les
Instru	ctior	j	k	iteration	Issue	comple	Result	t	Busy	Add	ress	S				,	, (	10	10	10	10
LD	F0	0	R1	1	1	9		Load1	Yes	80				,	ی	باي	ole)	dex	dex	dex	del
MUL'	F4	F0	F2	1	2			Load2	Yes	72							^	M	MI	MI	del
SD	F4	0	R1	1	3	4		Load3	No		Qi					,	/	/ 1	7 11	7 11	7 11
LD	F0	0	R1	2	6			Store1	Yes	80	Mu	lt1									
MUL'	F4	F0	F2	2	7			Store2	Yes	72	Mu	lt2									
SD	F4	0	R1	2	8	9		Store3	No												
Rese	rvatio	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k												
	Time	Name	Busy	Ор	Vj	Vk	Qj	Qk	Code	э:											
	0	Add1	No						LD	F0	0	R1									
	0	Add2	No						MUL	F4	F0	F2									
	0	Add3	No						SD	F4	0	R1									
	0	Mult1	Yes	MULTD		R(F2)	Load1		SUB	R1	R1	#8									
	0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loc	op									
Regis	ster r	esult s	tatus																		
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1		F30									
9		72	Qi	Load2		Mult2															

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## **Loop Example Cycle 10**

Instr	uctior	j	k	iteration	Issue	comple	Resul	t	Busy	Add	ress	3
LD	FO	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2			Load2	Yes	72		
SD	F4	0	R1	1	3	4		Load3	No		Qi	
LD	FO	0	R1	2	6	10		Store1	Yes	80	Mul	t1
MUL	F4	FO	F2	2	7			Store2	Yes	72	Mul	t2
SD	F4	0	R1	2	8	9		Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	e <i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	0	Mult2	Yes	MULTD		R(F2)	Load2		BNE	R1	Loc	р
Regi	ster r	esult s	tatus	1								
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1		F3C
10	)	72	Qi	Load2		Mult2						

Instru	uctior	j	k	iteration	Issue	comple	Resul	t	Busy	Add	ress	5
LD	FO	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi	
LD	FO	0	R1	2	6	10	11	Store1	Yes	80	Mu	t1
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mu	t2
SD	F4	0	R1	2	8	9		Store3	No			
Rese	ervatio	on Sta	tions		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	ə <i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	4	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	0	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loc	р
Regi	ster r	esult s	tatus									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F30
11		64	Qi			Mult2						

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## **Loop Example Cycle 12**

Instru	uctior	j	k	iteration	Issue	comple	Resul	t	Busy	Add	ress	3
LD	F0	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mu	t1
MUL	F4	FO	F2	2	7			Store2	Yes	72	Mu	t2
SD	F4	0	R1	2	8	9		Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code	e <i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	3	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	4	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loc	р
Regi	ster r	esult s	tatus									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1		F3C
12		64	Qi			Mult2						

Instru	uctior	j	k	iteration	Issue	comple	Resul	t	Busy	Add	ress	6
LD	FO	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2			Load2	No			
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi	
LD	FO	0	R1	2	6	10	11	Store1	Yes	80	Mu	t1
MUL	F4	F0	F2	2	7			Store2	Yes	72	Mu	t2
SD	F4	0	R1	2	8	9		Store3	No			
Rese	ervatio	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Busy	Op	Vj	Vk	Qj	Qk	Code	ə <i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	2	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	3	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loc	p
Regi	ster r	esult s	tatus									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F3C
13		64	Qi			Mult2						

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## **Loop Example Cycle 14**

Instru	uctior	j	k	iteration	Issue	comple	Resul	t	Busy	Add	ress	3
LD	FO	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2	14		Load2	No			
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	Mu	t1
MUL	F4	FO	F2	2	7			Store2	Yes	72	Mu	t2
SD	F4	0	R1	2	8	9		Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	e <i>:</i>		
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	1	Mult1	Yes	MULTD	M(80)	R(F2)			SUB	R1	R1	#8
	2	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loc	р
Regi	ster r	esult s	tatus									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1		F3C
14		64	Qi			Mult2						

Instru	ictior	j	k	iteration	Issue	comple	Resul	t	Busy	Add	ress	3
LD	F0	0	R1	1	1	9	10	Load1	No			
MUL.	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	4		Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	11	Store1	Yes	80	M(8	30)*R
MUL.	F4	FO	F2	2	7	(15)		Store2	Yes	72	Mu	t2
SD	F4	0	R1	2	8	لوا		Store3	No			
Rese	rvati	on Sta	<u>tions</u>		S1	S2	RS fo	RS for	k			
	Time	Name	Bus	Ор	Vj	Vk	Qj	Qk	Code	e:		
	0	Add1	No						LD	FO	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	No						SUB	R1	R1	#8
	1	Mult2	Yes	MULTD	M(72)	R(F2)			BNE	R1	Loc	p
Regis	ster r	esult s	tatus									
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F3C
15		64	Qi			Mult2						

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Loop Example Cycle 16 ho day MUZ

Instru	uction	j	k	iteration	Issue	comple	Result	1	Busy	Add	ress	3
LD	F0	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2	14	15 /	Load2	No			
SD	F4	0	R1	1	3	4	/16	Load3	Yes	64	Qi	
LD	F0	0	R1	2	6	10	41	Store1	Yes	80	M(8	30)*R
MUL	F4	FO	F2	2	7	15	16	Store2	Yes	72	M(7	72)*R
SD	F4	0	R1	2	8	9		Store3	No			
Rese	ervati	on Sta	<u>tions</u>		S1	S2	RS for	RS for	k			
	Time	Name	Bus	Op	Vj	Vk	Qj	Qk	Code	e:		
	0	Add1	No						LD	FO	0	R1
	0	Add2	No						MUL	F4	FO	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loc	р
Regi	ster r	esult s	tatus	1								
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1		F30
16		64	Qi			Mult1						

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Instruction		j	k	iteration	Issue comple Result			Busy Address				
LD	FO	0	R1	1	1	9	10	Load1	No			
MUL	F4	F0	F2	1	2	14	15	Load2	No			
SD	F4	0	R1	1	3	4	16	Load3	Yes	64	Qi	
LD	FO	0	R1	2	6	10	11	Store1	Yes	80	M(8	30)*R
MUL.	F4	FO	F2	2	7	15	16	Store2	Yes	72	M(7	′2)*R
SD	F4	0	R1	2	8	9	17	Store3	No			
Reservation Stations				S1	S2	RS for	RS for	k				
	Time Name Busy			Op	Vj	Vk	Qj	Qk	Code:			
	0	Add1	No						LD	F0	0	R1
	0	Add2	No						MUL	F4	F0	F2
	0	Add3	No						SD	F4	0	R1
	0	Mult1	Yes	MULTD		R(F2)	Load3		SUB	R1	R1	#8
	0	Mult2	No						BNE	R1	Loc	р
Register result status												
Clo	ck	R1		F0	F2	F4	F6	F8	F10	F1.		F30
17		64	Qi			Mult1						