ELECENG 2EI4

DP #4: MOSFET XOR Gate

Instructor: Dr Haddara

Jasmine Dosanjh – dosanj5 – 400531879

Apr 6, 2025

1. Circuit Schematic

a. Circuit Schematic

The following circuit schematic was used to implement the MOSFET XOR gate:

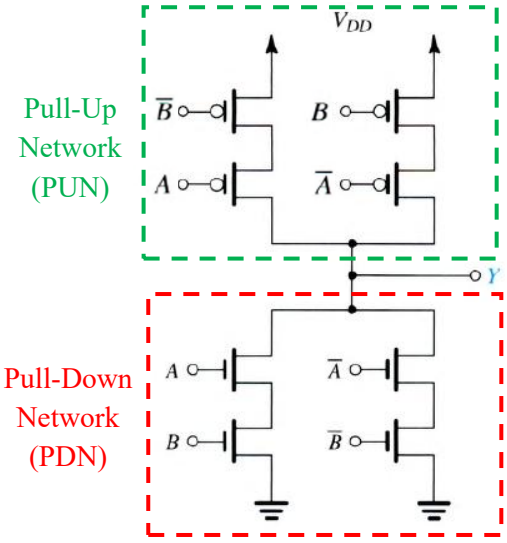

Figure 1. Schematic of XOR gate

There are two inputs, A and B, and a single output, Y, which follow the following behaviour:

Table 1. XOR gate truth table

Inputs		Output
A	B	$Y = A\bar{B} + \bar{A}B$
0	0	0
0	1	1
1	0	1
1	1	0

The circuit is designed using CMOS Logic, where:

- The PUN consists of PMOS transistors, responsible for driving the output high (5V).
- The PDN consists of NMOS transistors, responsible for pulling the output low (0V).

These networks are complementary, meaning that when one is conducting, the other is OFF.

- When A = B (either both 1 or both 0), the PDN is active.

- When A ≠ B, (one is 0, the other is 1), the PUN is active.

The PUN and PDN each have 6 MOSFETs (2 for the inverter, 4 for the function). This means a total of 12 MOSFETs were used for this implementation.

b. Ideal Sizing

Due to the symmetry of the circuit, all four paths to the output are considered the longest path, which contains 2 transistors in series. Thus, the size ratios for NMOS and PMOS transistors are expressed as

$$(W/L)_n = 2n \text{ and } (W/L)_p = 2p$$

Generally, NMOS and PMOS transistor sizing follows:

$$n = 2/1 \text{ and } p = 5/1$$

In our case:

$$2n = 4/1 \text{ and } 2p = 10/1$$

Thus, the ideal ratio of NMOS to PMOS transistor sizes is:

$$4 : 10 \rightarrow 2 : 5$$

c. Impact on Circuit Performance

We can implement the 2:5 ratio in the CD4007 IC because the inverter's voltage transfer characteristic curve is symmetrical. This means that the rise and fall times of the voltage signal are similar, thus the transition between logic levels (low to high and high to low) behaves in a balanced manner.

However, we cannot implement the 2:5 ratio as planned due to the differences in the transistor configurations. The CD4007 inverter has a single PMOS and NMOS, while the target circuit requires two PMOS and two NMOS transistors in series. This introduces different resistance values, deviating from the 1:1 ratio methodology studied in class. We need to double the transistor widths to halve resistance matching the inverter resistance, but we cannot adjust the transistor sizes in the CD4007 IC to achieve this. This means the critical timing signal may be delayed, incurring inconsistent rise and fall times within the circuit's output signals.

2. Testing

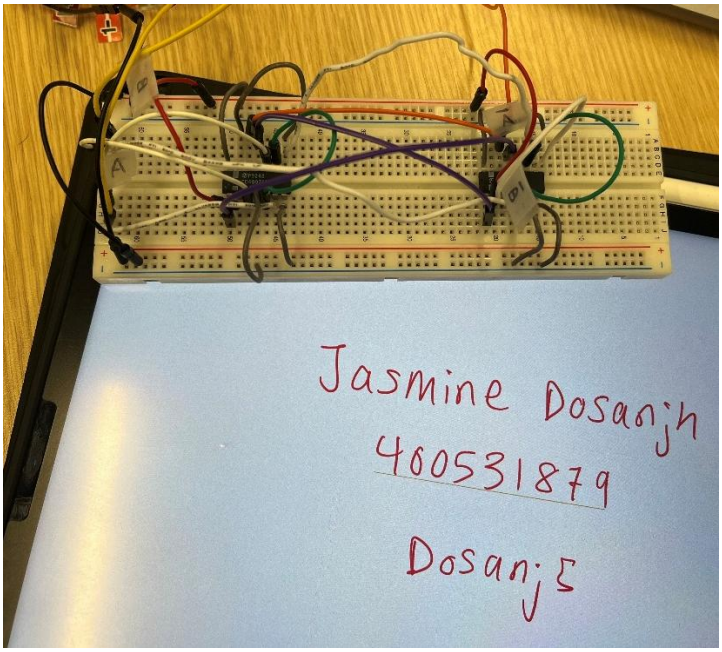

Figure 2. Physical circuit implementation

a. Functional Testing

The output signal Y (yellow) can be seen for inputs A (top blue) and B (bottom blue) respectively.

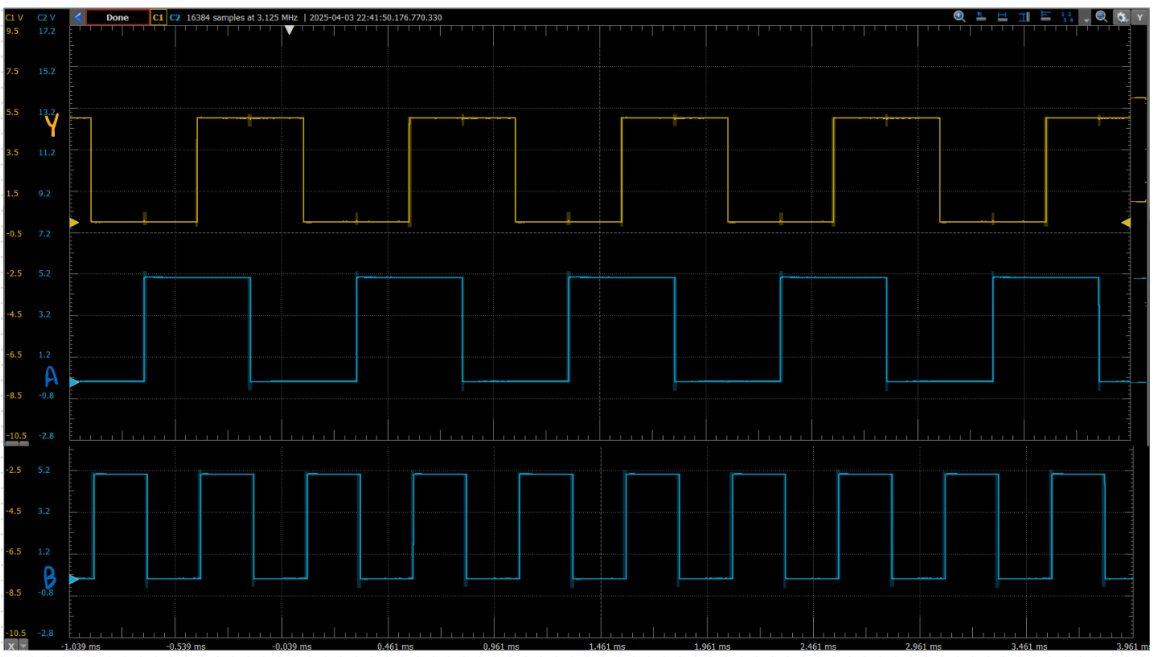

Figure 3. Functional Testing: Using Oscilloscope where Y, A, and B are plotted respectively

We can match the inputs A and B and expected output of Y to the XOR truth table seen in Table 1:

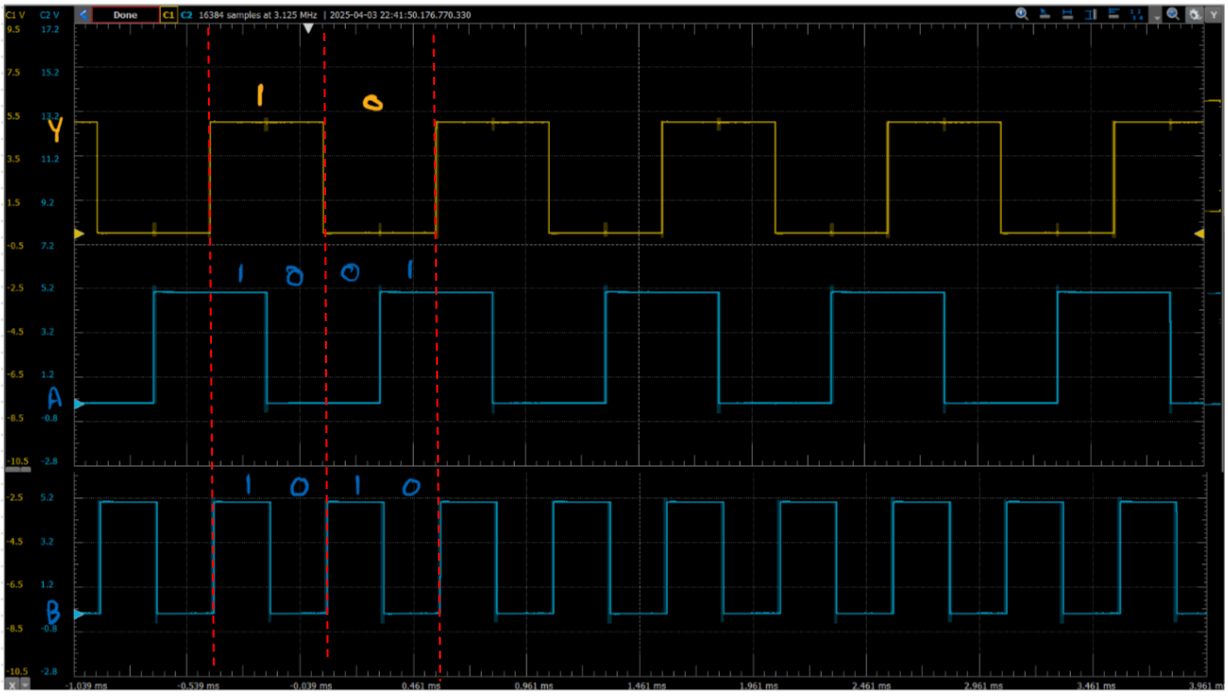

Figure 4. Functional Testing: Demonstrating XOR Function

b. Static Level Testing

Figure 5 shows the oscilloscope results for inputs A = 5V and B = square wave from 0V to 5V. The resulting output waveform for Y has $\boldsymbol{V_H \approx 5\,V}$ and $\boldsymbol{V_L \approx -0V}$**.** When the input voltages were switched, these values remained the same, shown in Figure 5

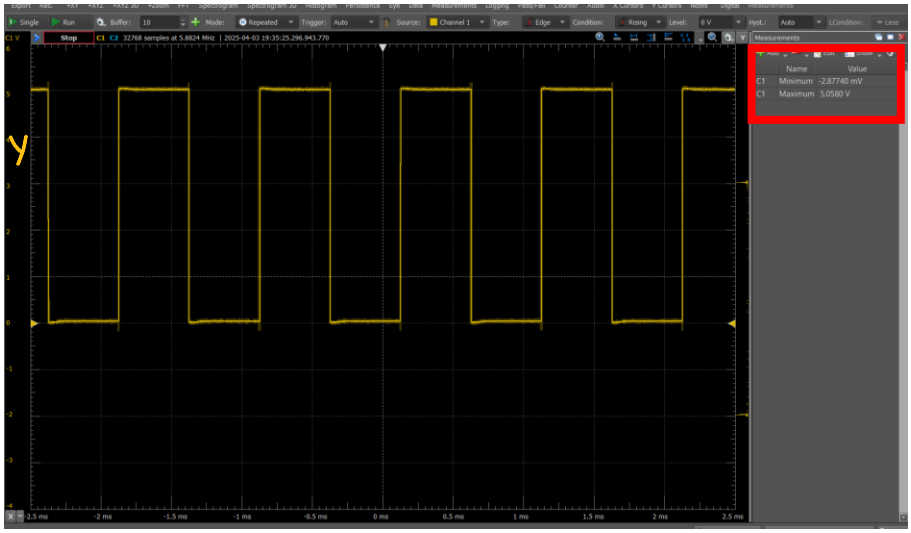

Figure 5. Static Level Testing (A = 5V, B = square wave between 0V and 5V)

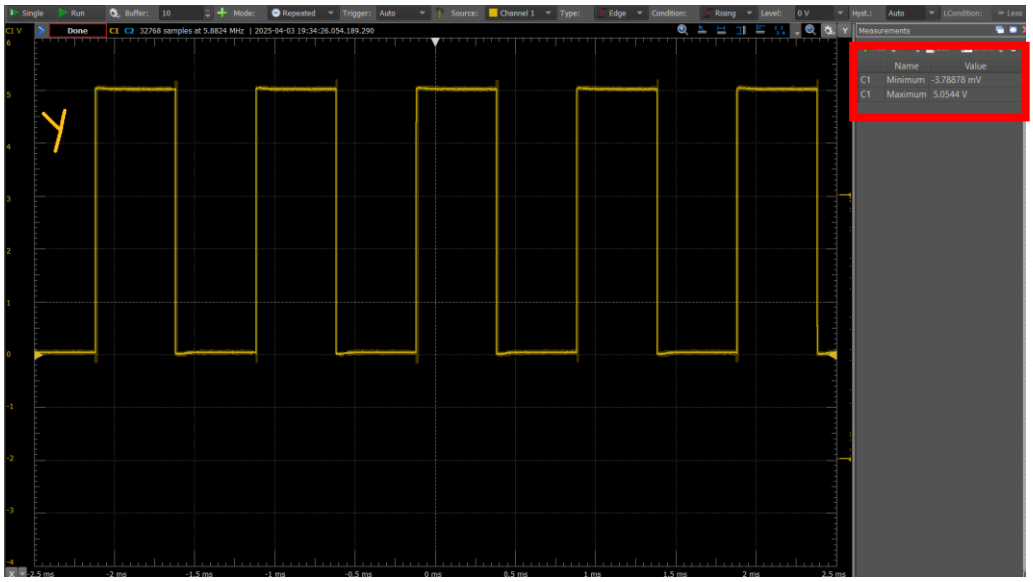

Figure 6. Static Level Testing (A = square wave between 0V and 5V, B = 5V)

3. Timing

a. Determine Rise and Fall times

Seen in Figure 7 is the waveform obtained after adding a 100nF capacitor. We measured the curves to obtain the rise and fall values of the output:

$$t_{rise} \approx 0.37924\mu s,\ t_{fall} \approx 0.37490\mu s$$

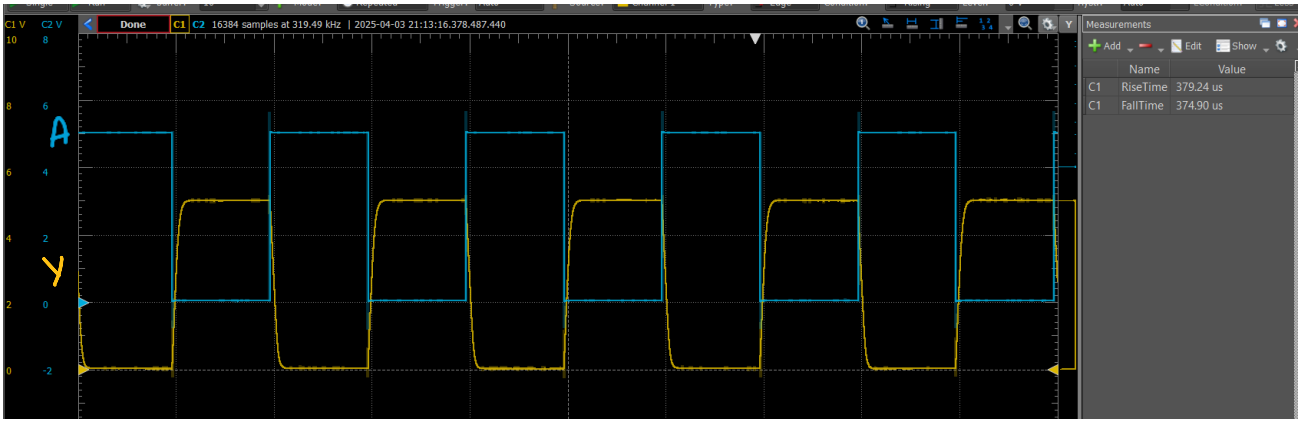

Figure 7. Output waveform with 100nF load capacitor

b. Determine τ_{PLH}, τ_{PHL}, and τ_P

As seen in Figure 8, to determine τ_{PLH}, we measured the time difference between the 50% transition of the input and the 50% transition of the output (~2.5V) when falling:

$$\tau_{PLH} \approx 619.3\mu s - 608.5\mu s \approx 10.8\mu s$$

Similarly in Figure 9, τ_{PHL} was determined by measuring the time difference between the 50% transition of the input and the 50% transition of the output when rising:

$$\tau_{PLH} \approx 5.619ms - 5.615ms \approx 4\mu s$$

Therefore, we can find τ_P:

$$\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2} \approx 0.74\ \mu s$$

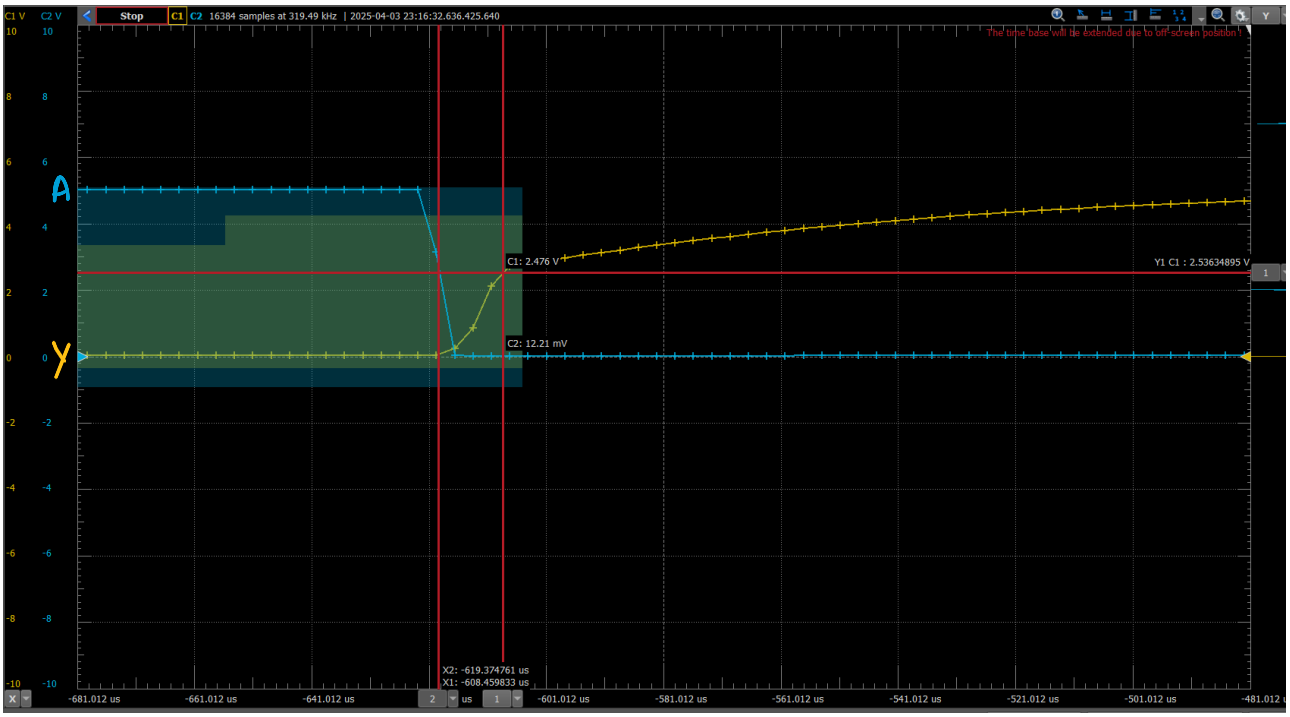

Figure 8. Finding τ_{PLH}

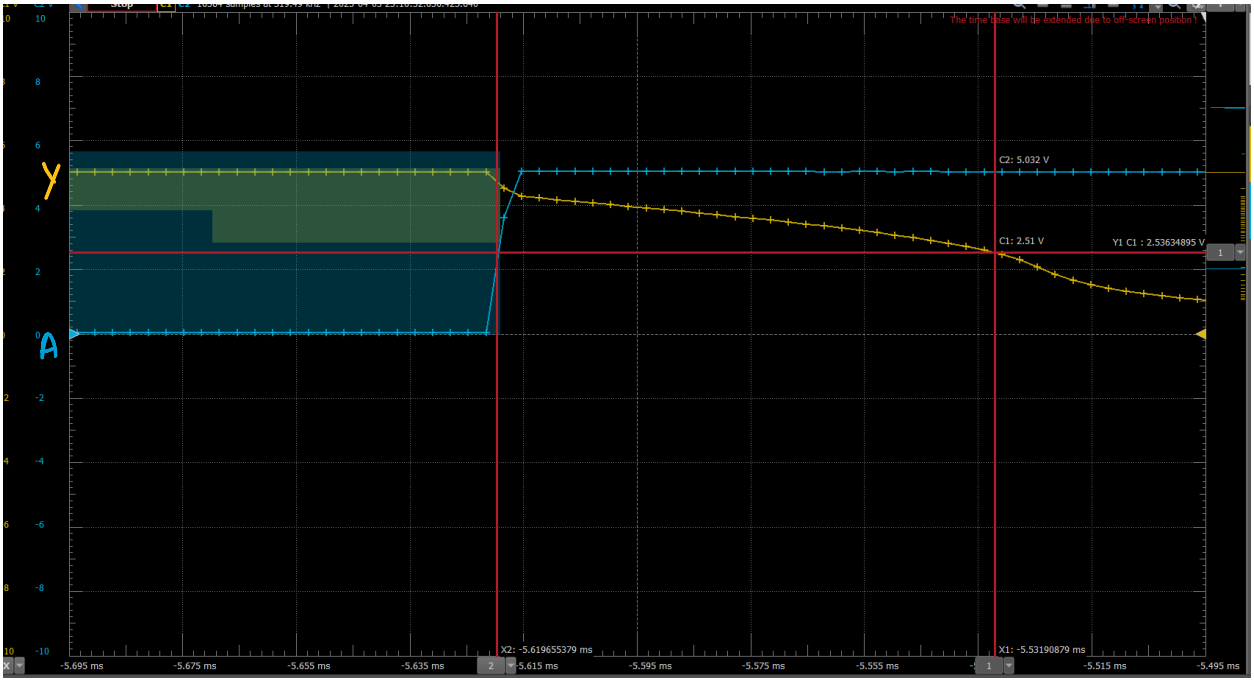

Figure 9. Finding τ_{PHL}