ELECENG 3EJ4

Lab Report #2

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Part 1 Questions

Q1. (10 Points)

(1) Step 1.2: $V_{o,min} = -3V$, $I_o = 1.848 \times 10^{-4} A$

Step 1.10: $V_{o,min} = -3V$, $I_o = 2.055 \times 10^{-4} A$

(2) Step 1.2: $R_o = \left[-2.41 \times 10^6, 4.07 \times 10^6\right]\ \Omega$

Step 1.10: $R_o = \left[-6.52 \times 10^6, 1.58 \times 10^7\right]\ \Omega$

Q2. (10 Points)

(1) $V_{o1} = 4.94V$, $V_{o2} = -3.578V$

(2) The above voltages correspond to the edge values of V_{sig}, in which the circuit functions as an amplifier:

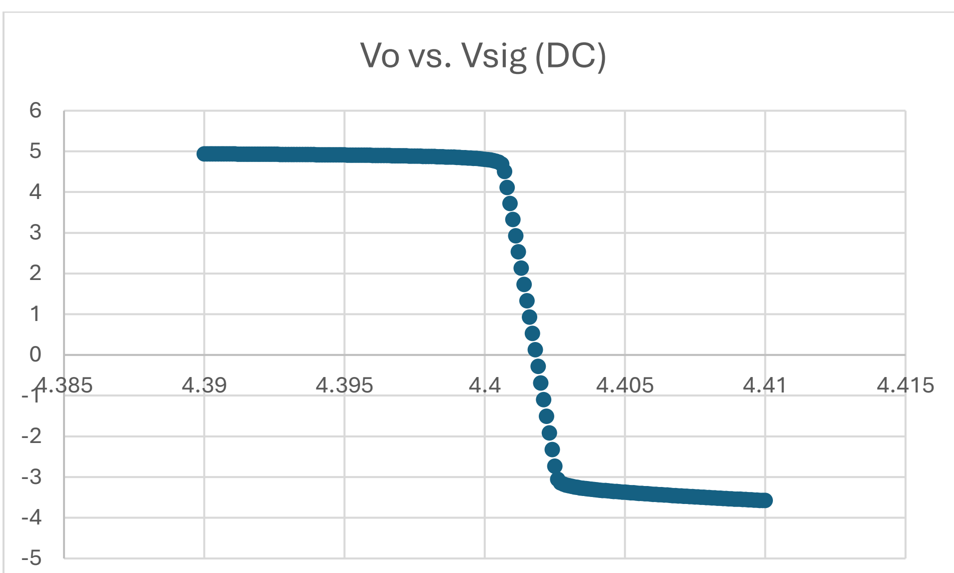
When $V_{sig(min)} = 4.39\ V \Longrightarrow V_{o1} = V_{o(max)}$

$V_{sig(max)} = 4.41\ V \Longrightarrow V_{o2} = V_{o(min)}$

Therefore, these points represent the maximum and minimum output voltages of the amplifier.

Q3. (15 Points)

(1)



The graph above has three key regions:

1. **Top flat region**: Changing V_{sig} does not change V_o, meaning there is no amplification. Since $V_o \approx V_{CC}$, the BJT conducts no current and is in cutoff.
$$\Delta V_o \approx 0 \Longrightarrow Gain = \frac{\Delta V_o}{\Delta V_{sig}} \approx 0$$
2. **Bottom flat region**: Same as top flat region, but $V_o \approx -3.6V$, meaning the BJT is fully on with no gain, meaning its in saturation.
3. **Middle steep region**: A tiny change in V_{sig} produces a large change in V_o, meaning this is where the circuit behaves like an amplifier (BJT forward active).
$$Gain = \frac{\Delta V_o}{\Delta V_{sig}} = large$$

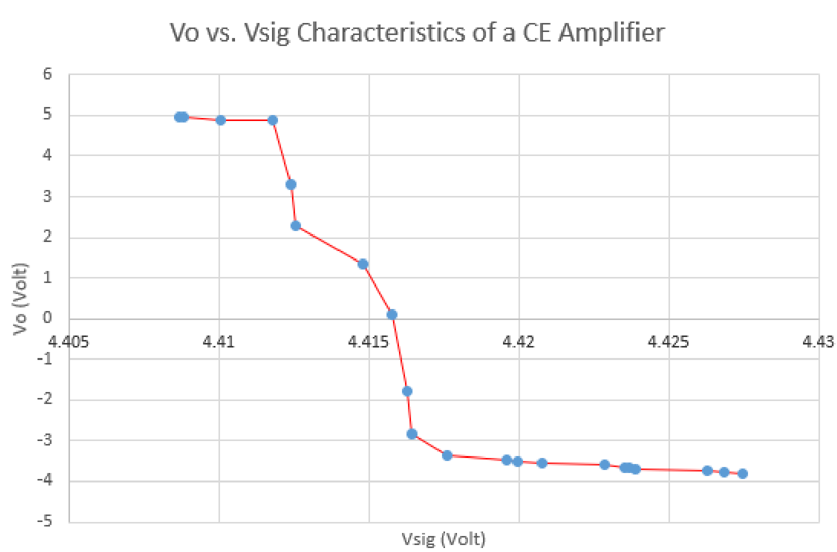
(2) From the graph in (1), for the circuit to work as an amplifier we must find the range of the middle steep region:

- $V_{sig} = [4.4006, 4.4028]\ V$
- $V_o = [4.6894, -3.175]\ V$

(3) For $V_o = 0.124 \approx 0V$:

- $V_{sig} = 4.4018V$
- $I_{C2} = 1.85 \times 10^{-4}\ A$

(4)



Q4. (10 Points)

(1) For low frequency of 100 Hz:

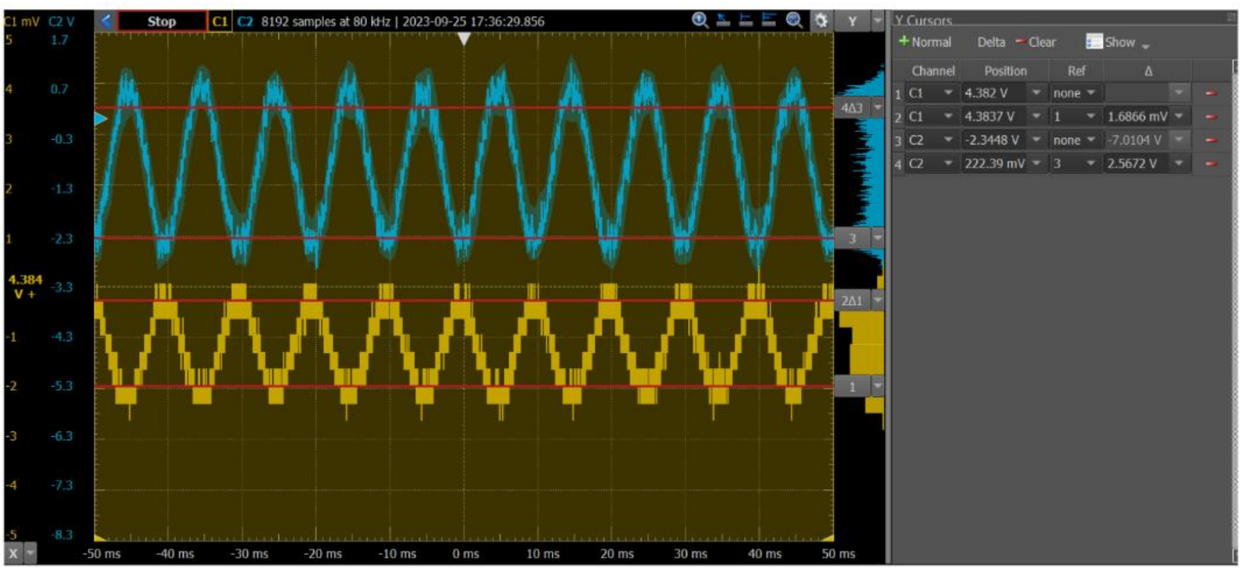
- $A_{vo} = 20\log\left(\frac{V_o}{V_i}\right) = 20\log\left(\frac{4.047V}{1mV\times 2}\right) = 20\log\left(\frac{4.047V}{0.002V}\right) = 66.1dB$
- $Phase_{low} = 179.6°$

Upper 3-dB frequency:

- $Phase_{3dB} = Phase_{low} - 45° = 134.6°$
- $f_{3dB} = 14402\ Hz$
- $A_{vo} = 20\log\left(\frac{V_o}{V_i}\right) = 20\log\left(\frac{2.84V}{0.002V}\right) = 63.04dB$

(2) The measured gain was $A_{vo} = 63.5\ dB$. This is similar to the values seen above.

(3) Adjusting the frequency of W1 to equal f_{3dB}:



For this frequency the gain is: $A_{vo} = 20\log\left(\frac{V_o}{V_i}\right) = 20\log\left(\frac{2.0299\ V}{4.5672\ mV}\right) = 52.95B$

Theoretically we expect, $A_{vo}(100Hz) \times 0.707 = 45dB$

Thus, there is a slight error between the theoretical and measured values, but they follow the same pattern that an increased frequency in V_{sig} results in a lower gain, A_{vo}.

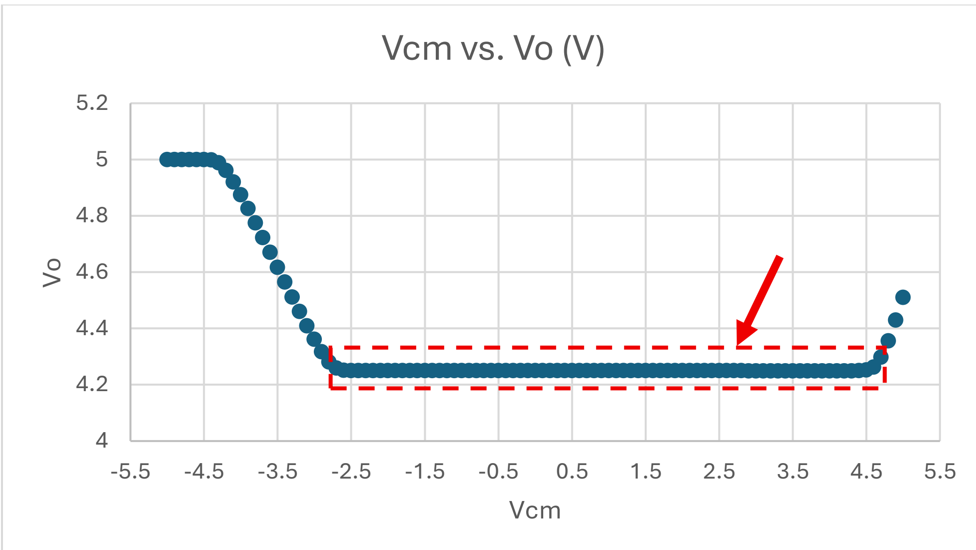
Part 2 Questions

Q5. (15 Points)

(1) When $V_{CM} = 0V$:

- $V_o = 4.2499V$
- $V_E = -0.525V$
- $I_{C2} = 9.10 \times 10^{-5}A$

(2) The range of V_{CM} to maintain the same V_o can be seen by the graph below:

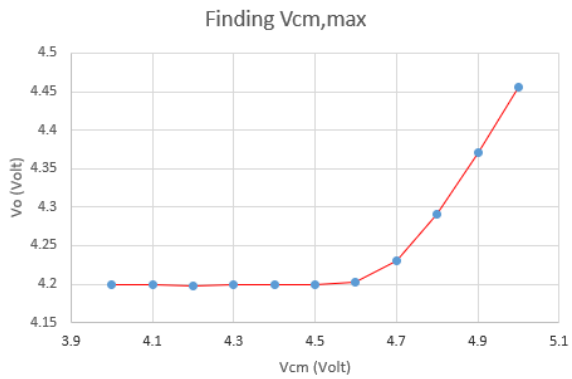


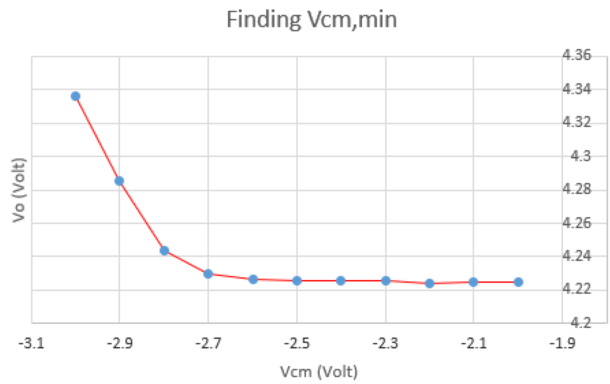
This graph shows that a constant V_o occurs for $V_{CM} = [-2.6, 4.6]\ V$.

(3) The upper and lower bounds of V_{CM} set both the transistor operation limits in the differential pair and current sink:

- Lower Bound: Limited by the need to keep the current sink Q3 on, because if V_{CM} is too low the transistor will be in cutoff.
- Upper Bound: Limited by the need to keep the transistor pairs Q1 and Q2 in active mode because if V_{CM} is too high the transistor will be in saturation.

(4) The measurement graphs below correspond to Steps 2.7 and 2.8.





The left graph from Step 2.7 shows that for a constant output voltage, $V_{CM(max)} = [4.5, 4.7]\ V$. The right graph from Step 2.8 shows $V_{CM(max)} = [-2.7, -2.5]\ V$. This matches the range $V_{CM} = [-2.6, 4.6]\ V$ found in (2).

Q6. (10 Points)

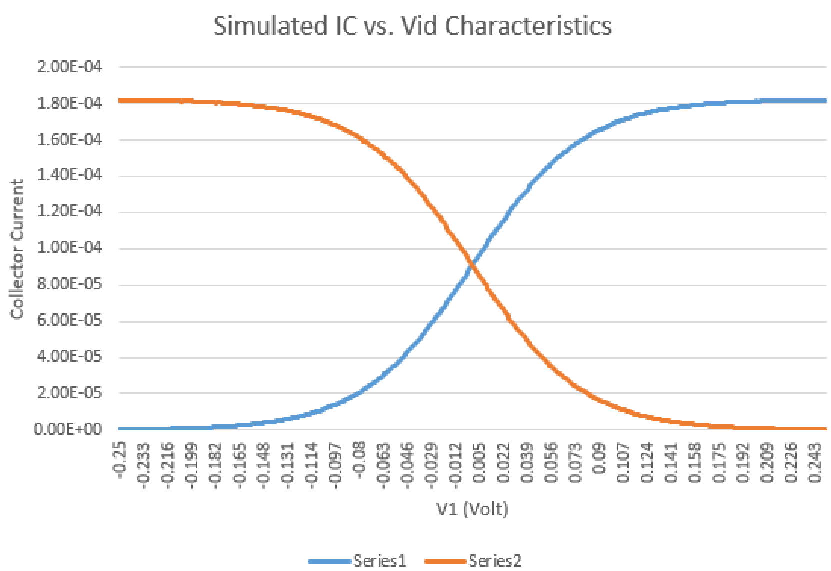
Based on the data in Step 2.3, the low-frequency voltage gain for V_{CM} is:

$A_{CM} = -86.90\ dB$ at lowest frequency $f = 0.1Hz$.

Part 3 Questions

Q7. (10 Points)

(1) Based on the simulation data obtained below in Step 3.2:



Section 9.2.3 of the textbook tells us that the limitations for the differential-mode ranges is $4V_T$ about the point of intersection of Series 1 and 2 for the DC case and $\frac{V_T}{2}$ for AC, where $V_T = 0.025\ V$.

The intersection of the series is at $V_1 = 0.004\ V$.

Thus, the DC and AC input differential-mode ranges are,

- $V_{DM} = [V_1 - 4V_T,\ V_1 + 4V_T]V = [-0.096,\ 0.104]\ V$
- $v_{dm} = \left[V_1 - \frac{V_T}{2},\ V_1 + \frac{V_T}{2}\right]V = [-0.0085,\ 0.0162]\ V$

(2) The upper and lower bounds of these input differential-mode ranges are determined by the range in which the two BJTs remain in active operation and share current. Around the intersection of the two collector current curves, both transistors conduct and the circuit behaves as a linear amplifier. For AC operation, if the differential-mode input exceeds $\pm V_T/2$, the circuit becomes nonlinear. For DC operation, if the range exceeds $\pm 4V_T$, one transistor saturates while the other cuts off, so the amplifier action is lost.

Q8. (10 Points)

(1) For step 3.3 the differential mode gain is $A_d = 19.63\ dB$.

(2) For low frequencies:

- $Phase = -0.000665535°$

Upper 3-dB frequency:

- $Phase = -0.000665535° - 45° = -45.00066554°$
- $f_{3dB} = 8332821.508\ Hz$

To find the Gain-Bandwidth Product, we must convert the gain from dB to the linear ratio (V/V):

$$A_d = 20 \log A_v \Rightarrow A_v = 10^{\frac{A_d}{20}} = 10^{\frac{19.63}{20}} = 9.5829\ V/V$$

Thus,

$$GBW = A_v \times f_{3dB} = \left(9.5829 \frac{V}{V}\right)(8332821.508Hz) = 79852595.23Hz$$

(3) Comparing the following frequencies:

- CE Amplifier (Q4): $f_{3dB} = 14402\ Hz$
- Differential Amplifier (Q8): $f_{3dB} = 8332821.508\ Hz$

In question 8, the 3dB frequency is much greater than question 4.

(4) Based on Step 3.6, the low-frequency differential gain is $A_d = 22.8\ dB$.

Q9. (10 Points)

$$CMRR = \frac{|A_d|}{|A_{cm}|} = \frac{|19.63\ dB|}{|-86.90\ dB|} = 0.22589\ dB$$