ELECENG 3EJ4

Lab Report #3

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Part 1 Questions

Q1. (15 Points)

(1) Below are the plots for the simulated and measured V_o vs V_{sig} characteristics obtained in Steps 1.2 and 1.6:

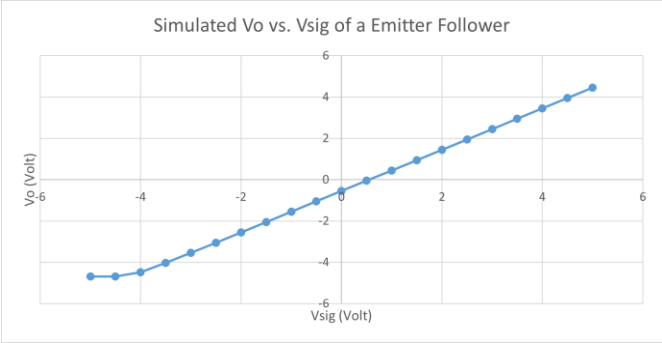

Figure 1. Simulated Data Step 1.2

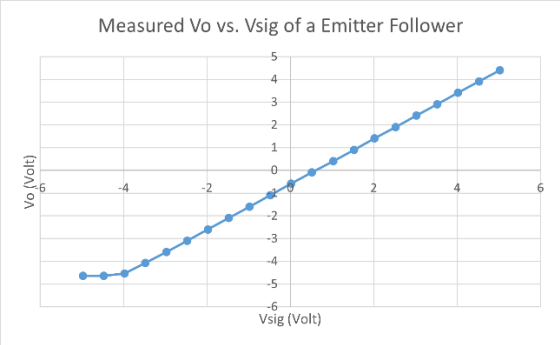

Figure 2. Measured Data Step 1.6

Both graphs are very similar, as they share the same overall shape:

Let's explain this by examining the following equation:

$$V_{BE} = V_B - V_E = V_{sig} - V_o$$

- For the first two points of both graphs, the slope is flat because for $V_{sig} \leq -4.5V$, V_o does not change. This implies that $V_{BE} < 0.7\ V$, and the BJT is in cutoff.
- Once V_o increases linearly with V_{sig}, $V_{BE} > 0.7V$ and the transistor enters the active region,

(2) The DC input range for V_{sig} is $-5V \leq V_{sig} \leq 5V$, but as mentioned in (1) V_o is flat for $V_{sig} \leq -4.5V$. This means that the circuit does not work as a common collector in this region as the gain $\frac{V_o}{V_{sig}} = 0 \neq 1$.

Thus, the DC input range for V_{sig} occurs where the BJT is in the active region, and that is $-4.5V \leq V_{sig} \leq 5V$ which corresponds to $V_o \approx [-4.5, 4.5]\ V$.

(3) According to the simulated data from Step 1.2 (refer to Figure 3), the V_{sig} value that results in $V_o \approx 0\ V$ is 0.5 V.

Vsig	Vo	IE2
Volts	Volts	Amps
-5	-4.683472277	2.24E-09
-4.5	-4.683223253	-3.15E-08
-4	-4.478345155	-2.82E-05
-3.5	-4.024650411	-9.13E-05
-3	-3.545404773	-0.000154408
-2.5	-3.052495105	-0.000184748
-2	-2.552539257	-0.000184869
-1.5	-2.052561188	-0.00018499
-1	-1.552583106	-0.000184863
-0.5	-1.052605055	-0.000184736
0	-0.552626992	-0.000184876
0.5	-0.052648962	-0.000185017
1	0.44732908	-0.000184889
1.5	0.947307092	-0.000184762
2	1.447285115	-0.000184902
2.5	1.947263106	-0.000185043
3	2.447241107	-0.000184915
3.5	2.94721908	-0.000184788
4	3.447197061	-0.000184928
4.5	3.947175015	-0.000185069
5	4.447152937	-0.000184941

Figure 3. Simulated Data Step 1.2

Q2. (10 Points)

Based on the simulation and measurement data obtained in Steps 1.3 and 1.8, the intrinsic voltage gain A_{vo} (magnitude and phase) at low frequency (100 Hz) is:

Step 1.3: $|A_{vo}| = 0\ dB \angle -8.47 \times 10^{-5\circ}$

Step 1.8: $|A_{vo}| = 0.8\ dB$

Frequency	M(V(Vo))	P(V(Vo))	Av = 20*log(|Vo|/1mV)
Hz	Volts	Degrees	dB
100	0.001	-8.47E-05	0.00

Figure 4. Simulated Data Step 1.3

ΔC1 (V) = Vsig(Peak2Peak)	ΔC2 (V) = Vo(Peak2Peak)	Voltage Gain Av (dB)
2.84E-03	3.10E-03	0.8

Figure 5. Measured Data Step 1.8

Part 2 Questions

Q3. (15 Points)

(1) Based on section 8.2.4 in the textbook, the relationship to express the mirror's output current I_o as a function of I_{REF} is given by:

$$\frac{I_o}{I_{REF}} = \frac{Area\ of\ EBJ\ of\ Q_2}{Area\ of\ EBJ\ of\ Q_1}$$

For the schematic in Fig. 3, Q1 and Q2 are the same transistors (2N3906), thus the areas will be the same. This implies that $I_o = I_{REF}$.

(2) Based on the simulation data obtained in Step 2.2,

At $I_{REF} = 0.1\ mA$, $I_o = 0.000104\ A \Rightarrow I_o = 1.04 I_{REF}$.

At $I_{REF} = 1\ mA$, $I_o = 0.000975\ A \Rightarrow I_o = 0.975 I_{REF}$.

IREF	Io
Amps	Amps
0.0001	0.000104
0.001	0.000975

Figure 6. Simulated Data Step 2.2

(3) To generate the theoretical predictions, we know from (1) that: $I_o = I_{REF}$. By plugging in the values of I_{REF} from (2),

When $I_{REF} = 1\ mA$, we should have $I_o = 1\ mA$ but we have $I_o = 0.975\ mA$.

When $I_{REF} = 0.1\ mA$, we should have $I_o = 0.1\ mA$ but we have $I_o = 0.104\ mA$.

As expected, the theoretical values are very close to the simulated ones, demonstrating almost a 1:1 relationship.

Q4. (15 Points)

(1) Based on the simulation data in Step 2.5,

Input impedance $R_{in} = 389.12\ \Omega$.

Current Gain of current mirror $A_i = 1.04\ A/A$

(2) Based on the simulation data in Step 2.6,

Output impedance $R_o = 1.58 \times 10^6\ \Omega$.

(3) Using the above information, we know that the relation to the h-parameters is:

R11 = h11 = v1/i1@v2=0 (Ohm)	Ai = h21 = i2/i1@v2=0 (A/A)
Ohm	A/A
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04
389.12	1.04

Figure 7. Simulated Data Step 2.5

$$R_{in} = h_{11}, R_o = 1/h_{22}, A_i = h_{21}$$

The linear two-port network for the current mirror is shown below:

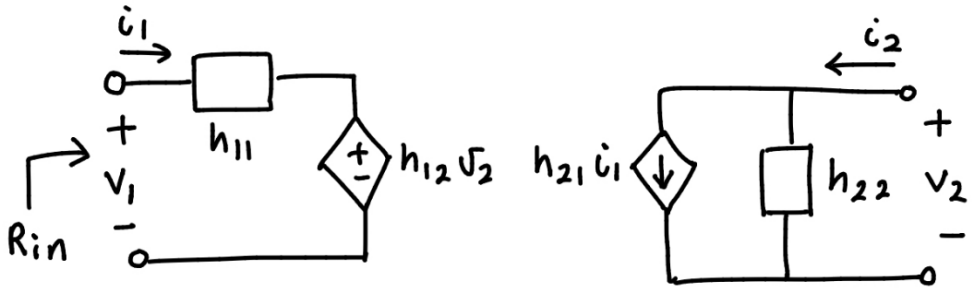

Figure 8. Linear two Port Network

With the following parameters,

$h_{11} = 389.12\ \Omega$

$h_{22} = 1.01 \times 10^{-4}\ S$

$h_{21} = 1.04$

$h_{12} = 7.05 \times 10^{-7}$ @ $100\ Hz$ to 1.41×10^{-6} @ $200\ Hz$

h12 = v1/v2@i1=0	h22 = i2/v2@i1=0	Ro = 1/(h22 - 1/RL)
V/V	S	Ohm
7.05E-07	1.01E-04	1.58E+06
7.75E-07	1.01E-04	1.58E+06
8.46E-07	1.01E-04	1.58E+06
9.16E-07	1.01E-04	1.58E+06
9.87E-07	1.01E-04	1.58E+06
1.06E-06	1.01E-04	1.58E+06
1.13E-06	1.01E-04	1.58E+06
1.20E-06	1.01E-04	1.58E+06
1.27E-06	1.01E-04	1.58E+06
1.34E-06	1.01E-04	1.58E+06
1.41E-06	1.01E-04	1.58E+06

Figure 9. Simulated Data Step 2.6

Part 3 Questions

Q5. (15 Points)

(1) Based on the simulation data in Step 3.2,

Voltage gain $A_d = 70.07\ dB$

(2) In step 3.6, the mismatch voltage calculated was $-1.27 \times 10^{-2}\ V$ which was the offset voltage applied to V_2 in subsequent steps.

(3) In Step 3.8,

Voltage gain $A_d = 60.3\ dB$

This is around 10 dB lower than the simulated value in (1).

Q6. (10 Points)

For low frequency f_L of 100 Hz:

- $Magnitude_L = 6.38\ V$
- $Phase_L = -0.518°$

Frequency	M(V(Vo))	P(V(Vo))	Ad = 20*log(|Vo|/2mV)
Hz	Volts	Degrees	dB
100	6.37860726	-0.51804511	70.07

Figure 10. Simulation data Step 3.2

The Upper 3-dB frequency f_H is the frequency at which the amplitude becomes $\frac{1}{\sqrt{2}} = 0.707$ of its low frequency value, or the phase changes 45°. This gives us:

- $Magnitude_H = Magnitude_L \times \frac{1}{\sqrt{2}} = 4.51\ V$
- $f_H = 11207\ Hz$

Frequency	M(V(Vo))	P(V(Vo))
Hz	Volts	Degrees
11207.40201	4.480928	-45.3853

Figure 11. Simulation data Step 3.2

Q7. (10 Points)

Comparing the upper 3-dB frequencies of this differential amplifier with a current mirror load, with that from Lab 2 of a differential amplifier using resistive loads…

- Lab 3 Q6: $f_H = 11207\ Hz$, $A_d = 70.07\ dB$
- Lab 2 Q8: $f_H = 8332821\ Hz$, $A_d = 19.63\ dB$.

The Lab 2 frequency is much larger than the one in this Lab. This is due to the Miller Theorem, which tells us that a higher voltage gain leads to a larger Miller capacitance, C_m, which in turn results in a smaller upper 3-dB frequency. Thus since, $f_H \propto \frac{1}{A_d}$, the larger gain of 70.07 dB in Lab 3 results in a smaller f_H, and the opposite is true of the smaller gain of 19.63 dB in Lab 2.

Q8. (10 Points)

Thus, the gain-bandwidth products (GBW) of the differential amplifier with a current mirror load, and Lab 2's differential amplifier using resistive loads are…

- Lab 3 Q6: $GBW = 3.57 \times 10^7\ Hz$
- Lab 2 Q8: $GBW = 7.95 \times 10^7\ Hz$

GBW	GBW in Step 3.6, Lab 2
Hz	Hz
3.57E+07	7.95E+07

Figure 12. Simulation data Step 3.2