Here is my understanding. The bus bridge will interface two protocols, PCIe and OCP.

First, basic OCP and PCIe protocols are modeled and simulated separately using Verilog.

Bus Bridge converts command and data of OCP formats to PCIe formats and vice versa.

Bus Bridge coverts the signals of one form (protocol) to another which is of acceptable by the receiving

end protocol. Timing requirements of each protocol must be met to ensure proper communication.

In other words, we probably have to verify that proper timing delay is fulfilled by Interconnecting Bus Bridge wrapper between Core Centric Protocol (OCP) and PCIe bus ?

Without knowing most of the details of either PCIe or OCP protocols, and in conformance with Accelera's Open Core Protocol Specification document, page 2, diagram "System Showing Wrapped Bus and OCP Instances", we declare our slaves and masters in relation to the On-Chip Bus:

**BRIDGE**

PAddr?

OCP Slave

MCmd

PCIe Master

PCIe Slave

OCP Master

rol

rol

rol

Control

PWData?

Maddr

Control ?

Addr

PTrans?

rol

MData

Addr ?

rol

rol

rol

Response

rol

DataOut

BurstLen

DataIn

PWrite?

MBurstLength

PSize?

MDataLast

DataIn ?

rol

Size ?

PBurst?

SCmdAccept

rol

PReady?

?

rol

PRData?

?

rol

SData

?

DataOut ?

SResp

PResp?

rol

SResptLast

We are given this interface

We are given this interface

The signals near (around) PCIe Master have not been researched yet: to be established. As you can see they are under question marks because they are only presumed to have those names, just for example (illustration). The example was taken from already existing document, "Implementation of bus Bridge between AHB and OCP", attached hereto.