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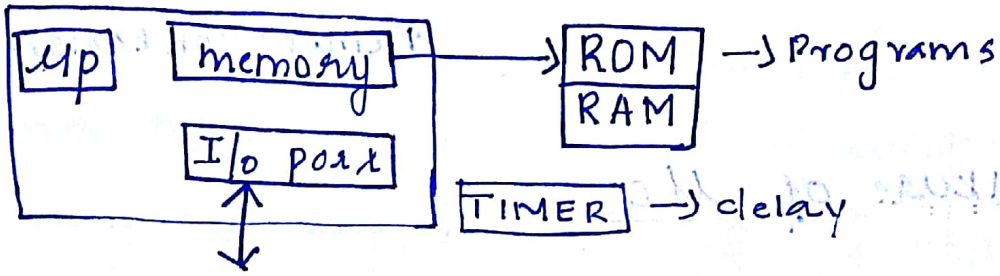
5. MICROCONTROLLER

- Computer on a chip.
- 

- Designed for small applications and dedicated applica
- Program is working in ROM – permanent
- Input is given by user it is stored in RAM
- MC is present in mouse, keyboard, remote, A/c, TV, ...
- In µp we can change the program but not in MC.

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TV

- MC is an integrated circuit that is programmed to do a specific task. MC are really just minicomputer
- MC are used for specific applications. It is used to do small & dedicated task.
- MC incoporate not only ALU & CU but also m/y and I/o ports
- TEXAS instruments are developed world's 1st MC TMS1000 in 1971

→ Difference b/w µp and MC

µP	MC
• Incoporate ALU and control unit	Incoporates ALU, CU, Prgm m/y (ROM, RAM, Data m/y) and I/o Ports
• Addition of external M/y make sys bulky and costly.	External M/y is required only if the build-in m/y is insufficient.

High computing power	Limited computing power.
It is used in general purpose applicat^n eg: pc	It is used in special purpose applicat^n eg: security s/m, instrumentat^n, video games, remote controls, ...

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→ Feature of Mc

* Bus width – 4 bit, 8 bit, 16 bit, 32 bit
  ~~808~~ 8051 – 8 bit Mc
* Memory size – 8051 has 128 byte RAM and 4Kb ROM.
  - 8052 has 256 bytes of RAM & 8Kb ROM.
  - MOTOROLA's ~~HC~~ 68HC11 has 256 bytes of RAM and 8Kb ROM
  - INDESE 8031 has no rom
* No: of instructions:
  - Complex instruction set computer (CISC)
  - Reduced " " " RISC.
* No: of build-in peripherals:
  - 8051 has 4 I/o port and two counters.
* Memory Architecture:
  - Nonneumann and Harward architecture.
* Speed:

Mc Selection

Selection ~~the~~ of the right Mc for an applicat^n is the most important part of the s/m design. The s/m designer has to first of all clearly determine the role of Mc in his design.

- He has to then begin a search for the Mc that will meet his requirements. This is done by referring to the literature such as books and data sheets.

Factors that should taken into consideration are:

- Meeting the computing needs of the task at hand efficiently and cost effectively.
- Availability of S/w development tools such as compiler, assembler and debugger.
- Wide availability and reliable source of Mc ...

- Bus width:
- memory size.
- no: of bit in peripherals
- speed
- power consumpt^n
- Package type
- Quantity required (manufacturing cost)
- development support
- Availability.

Embedded - build in memory

Harward - different memory locations for different signals.

Princeton - common memory location for all.

8051 - intel - 1st designed Mc

Types of microcontrollers

- Bits: 8, 16, 32
- memory/device: Embedded, External memory
- Instruction Set: RISC, CISC
- memory Architecture: Harvard, Princeton
- IC chips [AVSLI core]
- Family: 8051, motorola, PIC, Hitachi, Texas, ARM, others.
  - Intel, Philips, Atmel, Siemens, Dallas

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Application Examples.

I. General

- Electronic weighing Machine.
- Temprature.
- PH meter.
- proximity detectors.
- Intensity analyzer.
- Data Acquisition Sim.

II. Biomedical

- Ecg recorder.
- Patient monitoring sim.
- Blood cell counter.
- Analyzer.
- Radiation therapy sim
- ~~Physio~~ therapy sim
- Physio

Handheld Instrument

- sugar analyser
- Pressure measuring.
- Magnetic field detection.
- Target distance finder.
- Moisture meter.
- AC control.

III. Communication

- Setup Box
- Switches
- Hubs
- Routers
- Signal tracker.
- cable Tv
- Target tracker
- Signal polarizat^{n}
- Infrared remote Sensing.

IV Controller

- Temprature moisture and physical parameter controller.
- Robot control
- CNC machine control
- Industrial plant control
- Automobile.
- Realtime control.
- cable Tv
- Target tracker.
- Signal polarization.

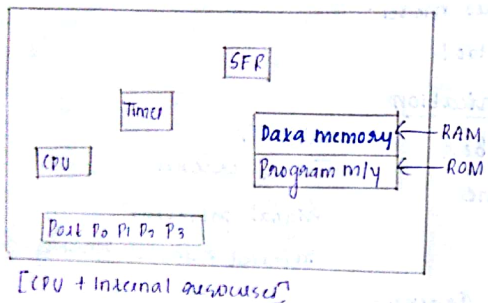
Peripheral Controll

- printer controller.
- USB port controller.
- CRT display controller.
- Land controller.
- disc drive controller.
- Miniature Copter

Process Control Slm

- Input from multiple Stage Sensors
- o/p to multiple solenoid ~~wall a~~ valves and motors.

Characteristics and Resources of a μc



[CPU + Internal resources]

- 16 bit program counter (PC) point to pgm memory
- 16 bit Data pointer (DPTR) point to data memory

SFR
DPTR – DPH, DPL

Instructions have operands of 8-bit

* SFR → Special Function Registers

Memory – RAM - programmable memory
RAM - Running time information

Registers – is as resources eg A, B, R0, R1 ... R7

SFR – dptr, Pgmcounter
- PC points to ROM
- dptr points to RAM (16 bit)

- Every thing will be 8 bit except PC, dptr

Memory Architecture

HARVARD MEMORY ARCH

- Seperate m/y address spaces for data m/y & Pgm m/y

PRINCETON MEMORY ARCHITECTURE

- Common memory address space for data memory and prgm'ml

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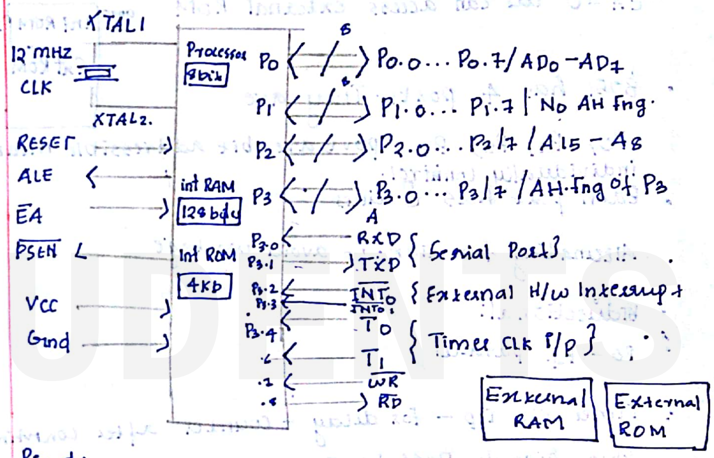
8051 microcontroller



Pin diagram

- CLK charges when power is given to μc
- CLK frequency is generated using oscillator. It is for knowing time for each instruction required
- If frequency is increased the μc performance ↑ses.
- RESET – Starting from begining / zero (using resets)
- ALE – 8 bit data ~~bus~~ & 16 bit address
  - multiplexing

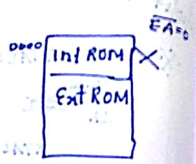
ALE = 1 address bus , ALE = 0 data bus

EA [Enable External Access] : only ROM (external)

Internal RAM - 128 bytes
Internal ROM - 4 kb.
External RAM - 64 kb
External ROM - 64 kb

this pin only works when inter ROM is discarded

$\overline{EA} = 0$ we can access external ROM



- 8051 has 4 ports. They are
  P0, P1, P2, P3 port are bit addressible means individually control.
- Each port has 8 lines
- Alternating function: to avoid wastage
- Bidirectional:
- P0 - P4 parallel
- Timer clk i/p - for delay - counter after counting then signals pass to processor then clock frequency stops.
  Counting using a trigger
  $\overline{WR}$, $\overline{RD}$ works with External RAM.
  $\overline{WR} = 0$ RAM active (writing into RAM
- Program status Enable ($\overline{PSEN}$)
  Used to read from ROM

10 mark sure.

ALU (8)

Data

- Processor + memory + ports = µc
- operands are stored in registers eg: accumulator, B.
  example mov A, R0 starting A
  mov A, R1
  ~~mov A, R~~
- PSW (prgm status word) - about the result (+/-, carry, ~~parity~~ Parity or not ~~parity~~ Parity) Flags

Address

- Identify the location
- Progm Counter & Data Pntr
  PC - address of next instruction.
  DPTR - address of the data. ⟨ DPH / DPL

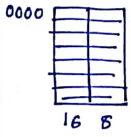
~~need~~ only once need to change DPL ∴ process fast.

Memory = Internal + External

2^7 = 128 bytes max available bit = 7 (1.111111) min (0000000

8 bit data 8 bit address.

Internal ROM



$2^2 * 2^{10} = 12$

address is 16 bit.

PORTS

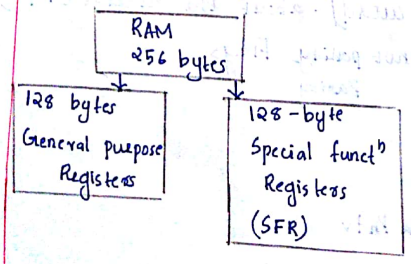
latch - data storing - 8 bit

P0 and P2 – address

Control signals

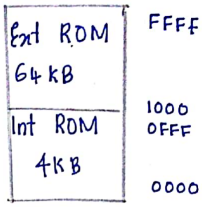
1/11/17 8051 Register Organization.

1. General purpose Registers
2. Special function Registers.

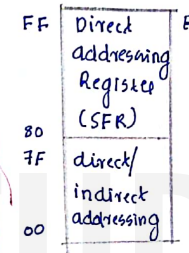


Memory

ROM

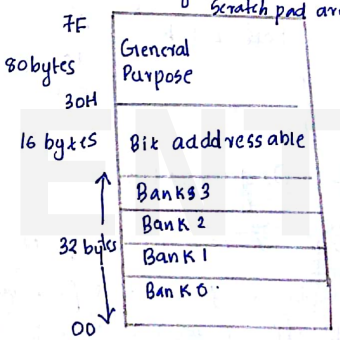


RAM



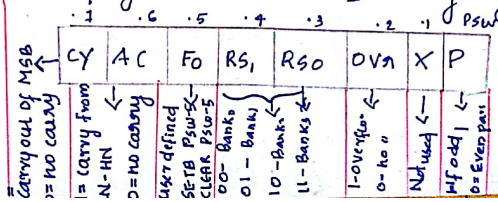
Direct/Indirect addressing

Scratch pad area.



. Each bank has R_0 - R_7 registers to reduce the opcode.

→ PSW [program status word] or flag registers



Special Function Registers

	Name	function	RAM address (Hex)
1.	A	Accumulator	0E0
2.	B	Arithmetic	0F0
3.	DPH	Addressing external memory	83
4	DPL	"	82
5	IE	Interrupt Enable control	0A8
6.	IP	Interrupt priority	0B8
7.	P_0	I/O port latch	80
8	P_1	"	90
9	P_2	"	A0
10	P_3		

Register Organisation

Register is a main part in the µc and Processors that provide a fast way to collect and store data. If we want to manipulate data with controller or processor by performing addition, substraction we can't do that directly in m/y but it needs register to process and store the data. µc contain several type of registers that can be classified according to their content / instruction that operate in them. 8051 µc contain mainly 2 types of register.

1) General Purpose Register.
2) Special Purpose Register.

3) PSW (flag registers).

11	PCON	Power Control	87
12	PSW	Program Status word	0D0
13.	SCON	Serial port control	98
14	SBUF	Serial port data buffer	99
15	SP	Stack pointer	81
16	TMOD	Timer/counter mode control	89
17	TCON	Timer/counter control	88
18	TL0	Timer 0 low byte	8A
19	TH0	Timer 0 high byte	8C
20	TL1	Timer 1 low byte	8B
21	TH1	Timer 1 high byte	8D

Address range: 80h - FFh

SFR (Special function registers) are upper RAM m/y in the 8051 µc these registers contain all peripheral related registers like P_0, P_1, P_2, P_3. Timers and counters, serial ports & INTR related register. The SFR m/y address from 80h - FFh. The SFR " implemented by bit address registers and byte address register. The registers, accumulator, P_0, P_1, P_2, P_3, IE register are bit addressible. Remaining all are byte addr.

In µc registers where data is stored, if one could manipulate its content bit by bit is called Bit addressible. If however you could manipulate the contents

only in chunks of 8 bit then it suffered to as byte addressible.

STACK & STACK POINTER

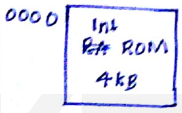
Stack refers to an area of internal RAM ie used in conjuction with certain opcode - To store & retrieve data speedily.

Address range : 32 - 7F

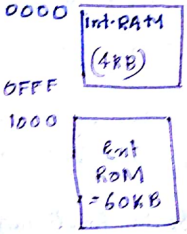
Memory Organisation

Ch 11

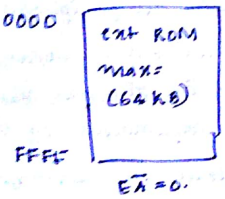
1. Internal ROM



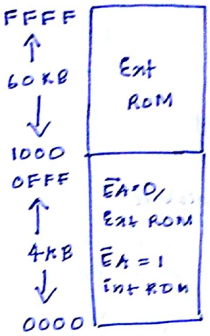
2.



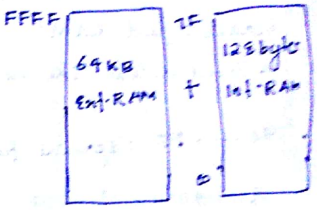
3. Only External ROM



Pgm memory



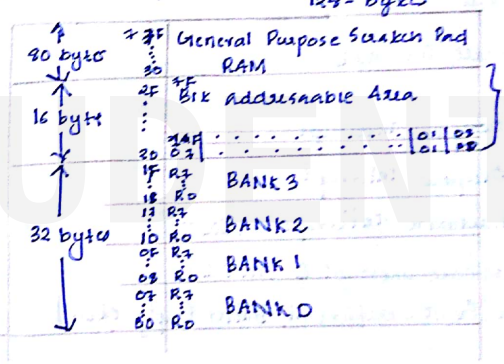
Data memory (RAM)



Instruction memory.

Structure of Int. RAM

128 bytes.



- Registers are divided into banks.
- out of 128, 32 are used for banks.
- Banking is for decreasing opcode.
- Banks are accessed by PSW3, PSW4.
- At a time only one bank can be active.
- Bit addressable area - eg: ON or OFF.
- Each location have 8 bit

General purpose ~~RAM~~ include general registers.
- Store and Forward
Scratch pad RAM.
- Speed access like cache memory

- 80 .... FF : special function Registers.

Interrupt in 8051 An interrupt is an external / internal event that disturbs the uc to inform it that a device needs its service. The pgm which is associated with the interrupt is called Interrupt Service Routine. Upon ~~A~~ creating the interrupt signal the uc

Definition

Procedure

TYPES
- Hardware
- Software interrupts.

1. Timer 0 overflow interrupt
2. Timer 1 Overflow interrupt
3. External hardware interrupt 0 (INT0)
4. External hardware Interrupt 1 (INT1)
5. Serial port Event (buffer full, Buffer Empty etc..)
6. Reset

Interrupt Control

IE → Interrupt Enable Register.
IP → Interrupt priority.

IE

EA	–	ET_2	ES	ET_1	EX_1	ET_0	EX_0

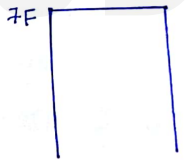
IP

.7	.6	.5	.4	.3	.2	.1	IP.0
–	–	PT_2	P_S	PT_1	PX_1	PT_0	PX_0

INT 0
Timer 0
INT 1
Timer 1
Serial Interrupts

INT: INT0: 0003h
Timer 0: 000Bh
INT1: 0013h
Timer 1: 0023h
RESET : 0000h

STACK : address range : 07 - 7F



IP.7 & IP.6 : Reserved
IP.5 : Timer 2 interrupt priority bit
IP.3 : Timer 1 " " "
IP.1 : Timer 0 " " "
IP.4 : Serial port interrupt priority bit
IP.2 : External Interrupt bit Priority bit.
IP.0 : External interrupt 0 priority bit.

EA : Global / enable / disable. To enable the interrupts this bit must be set high.

– : undefined - reserved for future one.

ET_2 : Enable / disable Timer 2 overflow interrupt.

ES: Enable/disable Serial port interrupt.
ET1: " " Timer 1 overflow interrupt.
EX1: Enable/ " External interrupt 0.

upon reset the interrupts have the following priority.
The interrupt with the highest priority gets serviced fir