

Building Neuromorphic Circuits with Memristive Devices

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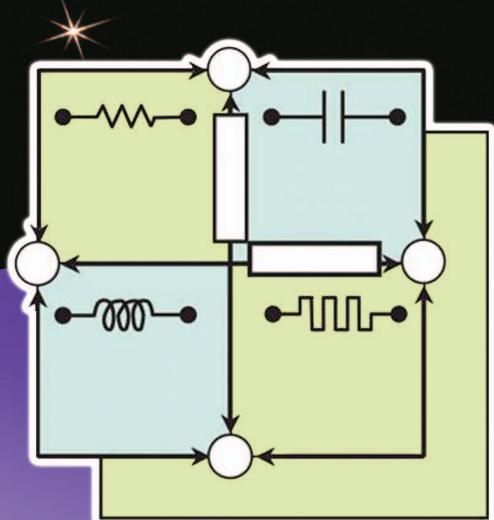
1. Introduction

The rapid, exponential growth of modern electronics has brought about profound changes to our daily lives. However, maintaining the growth trend now faces significant challenges at both the fundamental and practical levels [1]. Possible solutions include *More Moore*—developing new, alternative device structures and materials while maintaining the same basic computer architecture, and *More Than Moore*—enabling alternative computing architectures and hybrid integration to achieve increased system functionality without

trying to push the devices beyond limits. In particular, an increasing number of computing tasks today are related to handling large amounts of data, e.g. image processing as an example. Conventional von Neumann digital computers, with separate memory and processor units, become less and less efficient when large amount of data have to be moved around and processed quickly. Alternative approaches such as bio-inspired neuromorphic circuits, with distributed computing and localized storage in networks, become attractive options [2]–[6].

The re-emergence of neuromorphic systems is fueled by two factors. First, more understanding has been obtained on both biological neural networks and man-made networks through experimental and modeling

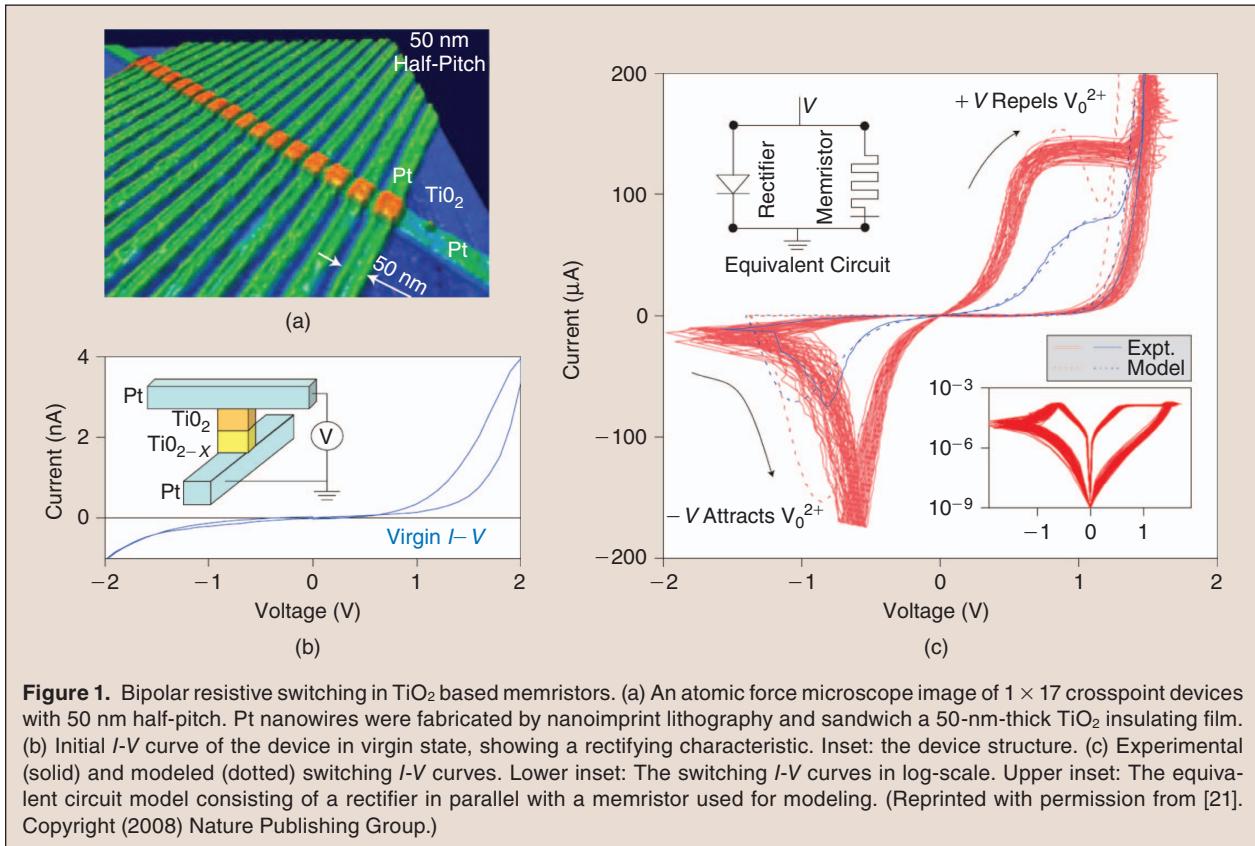
Memristors: Theory and Applications



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studies [7]–[10]. Second, the emergence of new classes of nanodevices, particularly two-terminal resistive switching devices (memristive devices) [11]–[17], makes it possible to build functional neuromorphic hardware that will not only serve to test the various neural network models but also can directly lead to new, effective, high-performance computing hardware.

In this review, we will discuss recent progress in the development of neuromorphic hardware based on nanoscale memristive devices. In particular, we will focus on a few representative device systems and show how two key properties, local adaptive learning and large connectivity, can be obtained in memristive devices that in turn make them well suited for neuromorphic applications. Significantly better understanding of the devices has been achieved in the last couple of years through extensive electrical and



material characterizations and modeling. A few network level demonstrations will also be discussed.

2. Memristive Devices

Resistive switching (RS) phenomena have been reported as early as the 1960's [18] and today such devices are extensively studied as resistive random-access memory (RRAM) for future non-volatile data storage [14]–[17], [19]–[22]. These devices generally are simple in structure (typically two-terminal) and nanoscale in dimensions (scaling < 10 nm has been demonstrated [23]), while at the same time offering excellent performance in terms of switching speed [24] and write/erase cycling [25]. Tremendous work has been performed to understand the various types of switching mechanisms that are responsible for RS phenomena in different material systems [14]–[17], [19]–[21], [26]–[30], which can be broadly categorized into valence change, electrochemical metallization, phase change, magnetoresistive, ferroelectric, electronic, and nanomechanical effects [15]. Here we focus on devices that show "analog" memristive behavior, i.e. devices that are particularly suitable for neuromorphic applications. Experimentally, devices that fall in the first three categories

(namely, valence change, electrochemical metallization, and phase change effects) have been extensively studied for this purpose and below we present results from a few representative studies.

2.1. TiO_2 Devices

The explicit connection between resistance switching and memristive effects (definition given later) was made by HP labs in 2008, where the behaviors of nanoscale TiO_2 crosspoint devices were shown to fit the descriptions of memristive devices (memristors for short throughout this review) [13]. Specifically, the devices exhibited pinched hysteresis loops (so no energy is stored) and frequency and history-dependent programming (see Fig. 1), in agreement with the predictions of memristors. Physically, RS of TiO_2 is a result of local stoichiometric change caused by the migration of oxygen vacancies (V_{Os}) and can be assigned into the valence change category. As V_{Os} act as donors in TiO_2 the accumulation/depletion of V_{Os} can cause an increase/decrease of the local conductance which in turn results in the modulation of the overall device conductance. Specifically, in the study of Yang et al. [21], the drift of oxygen vacancies towards the

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Pt/TiO₂ Schottky interface, driven by the external electric field, results in the accumulation of V_{Os} and the creation of conducting channels that switch the device in the high conductance on state. When applying electric fields with a reverse polarity, the oxygen vacancies are driven away from the Schottky barrier, hence dissolving the conducting channels and switching the device back to off state. Later it was demonstrated that the aggregation of V_{Os} in TiO₂ in the conductive region may in fact lead to the formation of a new oxygen-deficient Magnéli phase (Ti₄O₇) that is metallic, as directly revealed by TEM studies [26], [30].

Since the devices operate by the redistribution of V_{Os}, the creation of a definitive V_O distribution profile will help obtain reliable device operations. Conventionally this is achieved in a high-voltage “electroforming process” to create the oxygen vacancies and define the V_O distribution. The forming process involves electro-reduction of oxygen ions, which produces oxygen gas and leaves oxygen vacancies in the oxide films [31]. On the other hand, high-voltage forming is not desirable in practice, is hard to control and reduces device yield and reliability. Based on improved understanding of the electroforming process and the resistive switching mechanism, the forming process can be successfully eliminated either by reducing the thickness of the oxide film to keep just the switching interface, or by intentionally introducing an oxygen-deficient layer next to the switching layer in the device fabrication process as a reservoir of oxygen vacancies [31].

Improved understanding of the switching mechanism has been obtained through a series of material analyses that offered useful information on film composition, micro-crystalline structure, and switching locations [29], [30] as well as modeling that attempted to match experimental results with known physical effects, for example, the drift and diffusion current equations, [27], [32] which will be discussed later. It also needs to be noted that although the conducting channels may be formed locally, the RS process, as determined by external stimuli, can be affected by the global device design such as the electrode materials, layer stacks and structures around the switching regions [33], [34]. For example, the reactions between TiO₂ and the metal electrodes (particularly with the thermally diffused Ti adhesion layer) can create additional oxygen vacancies in TiO₂ and modulate the electronic barrier at the interface, which in turn affect the resistive switching behavior. The localized diffused adhesion material may also serve as seeds for switching channel formation, leading to improved switching reliability [34].

2.2. WO₃ Devices

Similar memristive behaviors have also been observed in other oxide materials. Here we choose WO₃ as an example. In modern CMOS processing, W is widely used as a contact

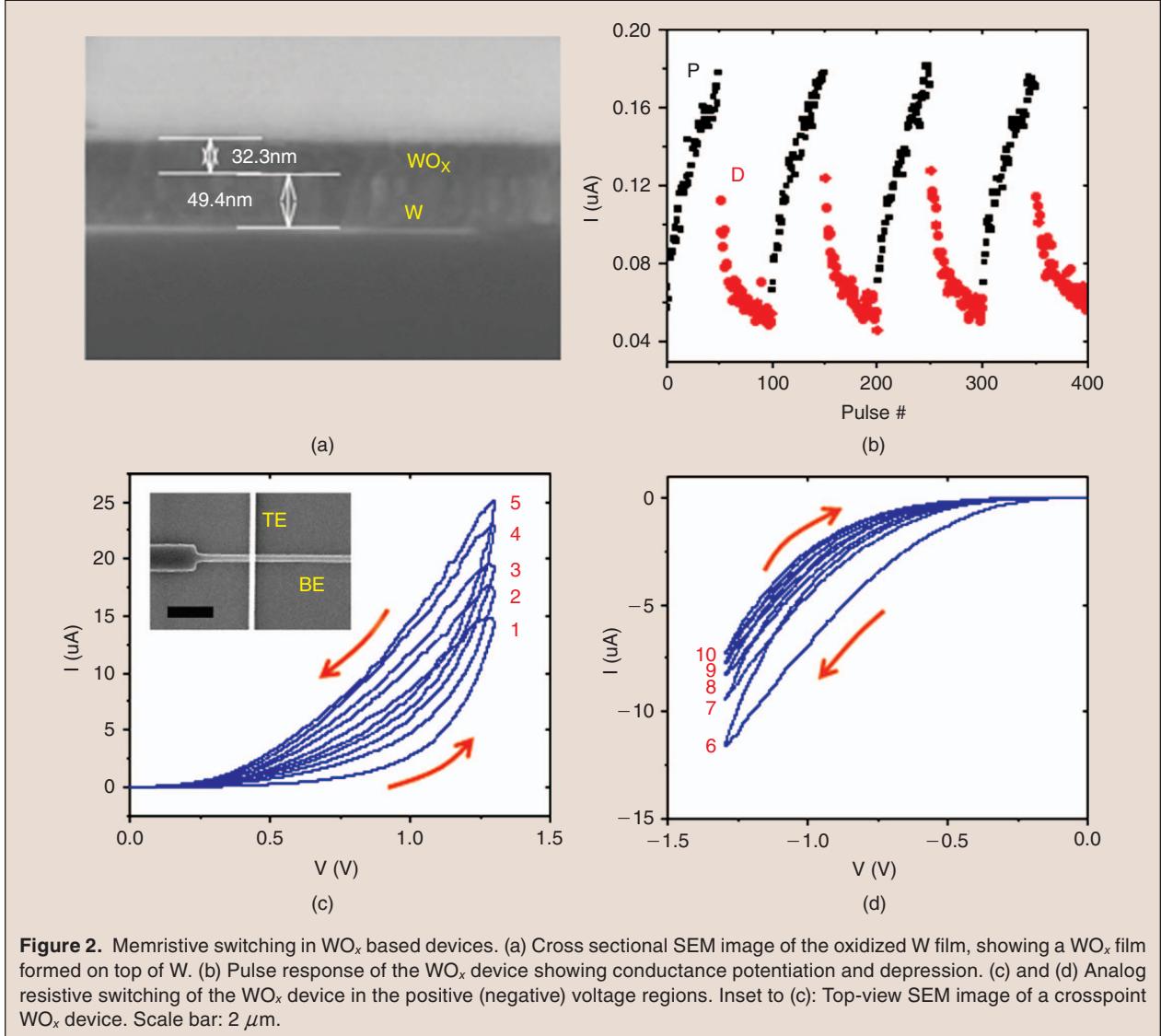
material so WO₃ can be easily incorporated into standard manufacturing processes [35]. Additionally, WO₃ has been a long-studied material with well-known characteristics and preparation methods [36]. Similar to TiO₂, WO₃ is also a transition metal oxide with many sub-stoichiometric states making them n-type semiconductors. This material system thus offers many attractive properties for device applications and has been used for both digital [37] and analog [36], [38] types of memory studies.

Typical analog-type resistive switching in WO_x based memristive devices is shown in Figure 2 in a study performed by the authors [36]. The device is composed of a Pd top electrode (TE) and a W bottom electrode (BE) sandwiching a WO_x film, as shown by the top-view scanning electron microscope (SEM) image in Fig. 2(c). A rapid thermal annealing (RTA) step was adopted to partly oxidize the W bottom electrodes, therefore directly forming a WO_x layer on top of the W bottom electrodes, as shown in Fig. 2(a). This oxidation process naturally introduced a continuous concentration gradient of oxygen vacancies [39], unlike the cases of abrupt V_O concentration profiles formed in other bilayer structures. By tuning the V_O distribution with external biases, analog-type resistive switching can be reliably obtained (see Figs. 2(b–d)) [36].

The quasi-continuous tuning of the device resistance with memory effects is the key enabling factor of memristor-based neuromorphic circuits. Briefly, the conductance modulation in memristors can be thought as being analogous to the plastic synaptic weight changes in biological synapses, so memristors can be used to emulate biological functions. This behavior is more clearly demonstrated in pulse measurements, as shown in Fig. 2(b), where positive and negative pulses (i.e. spike inputs) cause the memristor conductance to increase or decrease by incremental amounts, corresponding to the potentiation (P) and depression (D) effects, respectively. Further characterizations and modeling confirmed the oxygen vacancy motion origin of the resistive switching effects in these devices [36], which will be discussed in more detail in the next section.

2.3. Ag₂S Devices

Besides oxygen vacancy (anion) driven devices, memristive devices based on metal ion (cation) redistribution have also been reported. They fall into the category of electrochemical metallization cells. The Ag₂S atomic switch reported in 2005 was an ingenious design to control RS within a 1 nm spacing [40]. The electrochemical (redox) effect between the Ag₂S electrode and the Ag deposits determines whether a conductive bridge is formed or disrupted, thus determining what resistive (conductive) state the device is in. Later, it was found

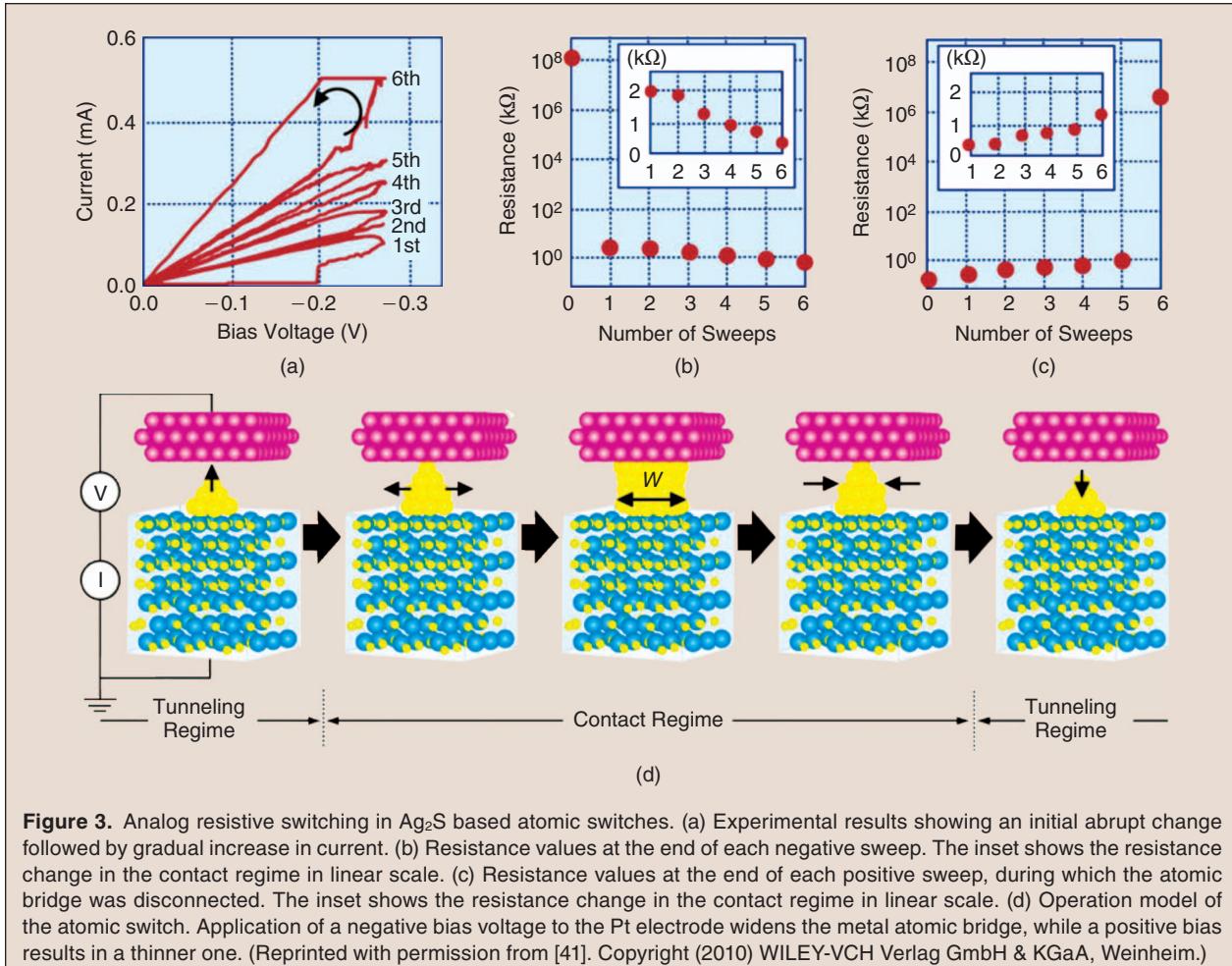


that not only the conductive bridge connection can be controlled, but the size (width/diameter) of the bridge can also be modulated to produce multilevel (analog) switching effects. Hence, the Ag_2S devices also potentially have the ability to emulate learning and memory functions of synapses [41], [42]. Specifically, electrical transport in the atomic switches can be divided into two regimes: tunneling regime and contact regime (Fig. 3). When the metal bridge has not connected the counter electrode, the electrical transport of the device is dominated by tunneling through the gap between the front of the metal bridge and the counter electrode. After the metal bridge forms contact with the counter electrode, further application of electric signals will result in lateral growth of the bridge, so the conductance is determined by the width of the bridge [41]. As a consequence, the initial contact between the metal bridge and the counter electrode will cause an abrupt transition of conduction

from tunneling to contact, hence leading to a digital-type switching behavior, while further growth of the metal bridge in the contact area will only expand the size of the bridge and lead to analog switching. This was indeed observed experimentally, as shown in Fig. 3(a). The device was initially in the tunneling regime, at about -0.2 V the contact was achieved, accompanied by a sharp increase in current. Afterwards the current was increased gradually in subsequent sweeps, corresponding to the expansion of the bridge size. The digital and analog changes in resistance in the two regimes were also clearly observed by recording the resistance values at the end of each sweep (Fig. 3(b–c)).

2.4. Ag/a-Si Devices

One of the first demonstrations of memristor-based synaptic functions was achieved by the authors in Ag/a-Si based memristive devices. Similar to the Ag_2S device,

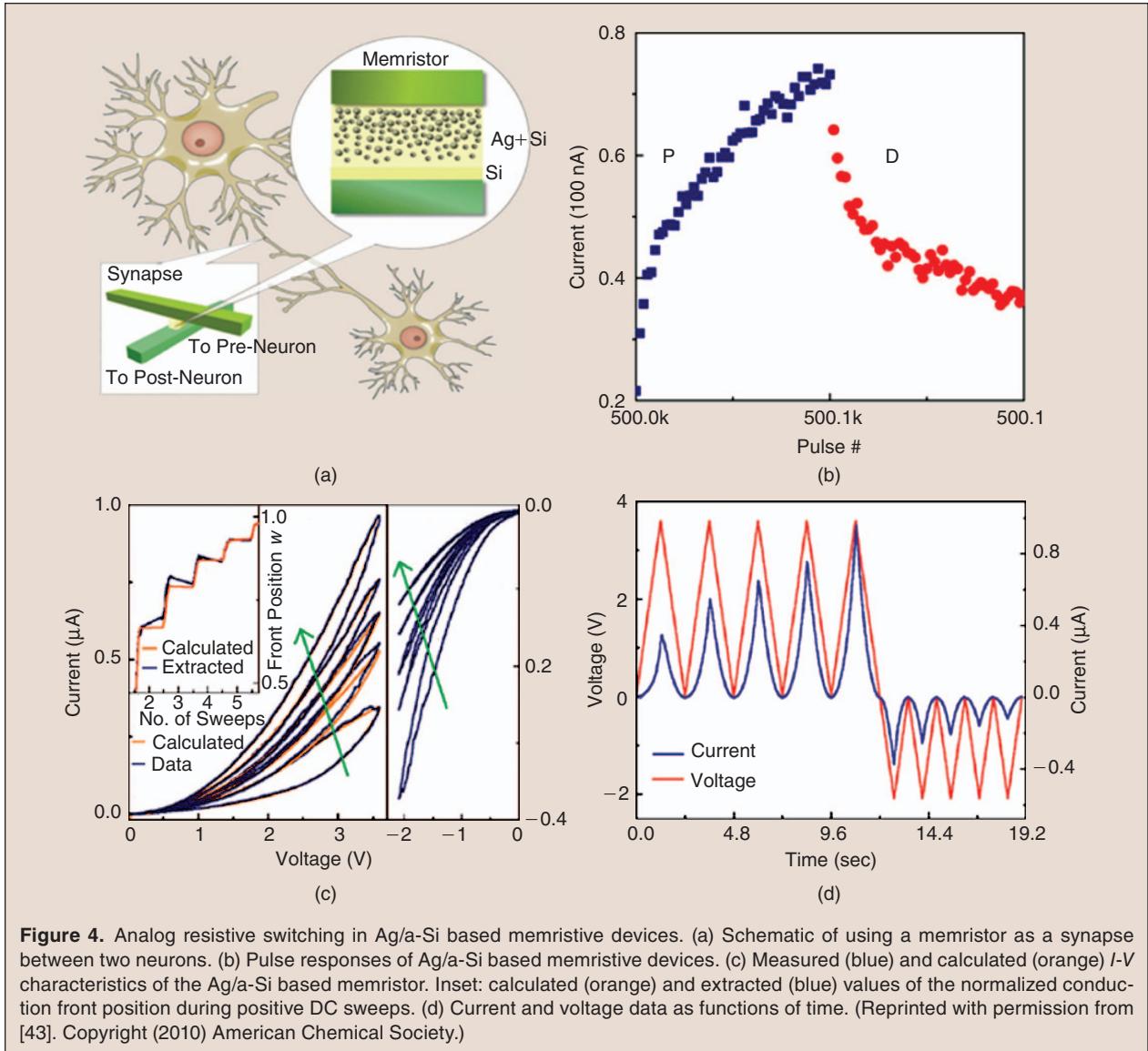


the $\text{Ag}/\text{a-Si}$ devices rely on the redistribution of Ag ions within the a-Si matrix. In digital-type devices, Ag conducting filaments can be formed/dissolved in the a-Si matrix and high performance metrics have been demonstrated for non-volatile memory applications, including high device yield of 99%, scaling potential of <50 nm, fast programming speed of 5 ns, high endurance of 10^8 , long retention of ~10 years, and multilevel storage capability [20], [44], [45]. To make the device suitable for neuromorphic applications, that is, to achieve analog switching, co-sputtering was employed to controllably incorporate Ag into the a-Si film to achieve a more gradual Ag concentration gradient as schematically shown in Fig. 4(a) [43]. Incremental analog switching, as demonstrated by both pulse measurements and DC sweeps were reliably achieved in these devices. Figure 4(b) shows the incremental adjustment of the conductance of the memristor device by a series of potentiating (3 V, 500 μ s) and depressing (-2.6 V, 500 μ s) pulses, while Figs. 4(c, d) show the evolution of the pinched hysteresis loops under DC voltage sweeps, where consecutive positive (negative) sweeps lead to gradual

conductance potentiation (depression). The analog switching can be understood by electric field-driven migration of Ag ions and resultant movement of the conduction front between the Ag-rich and Ag-poor regions in the active layer. Indeed, simulation results based on this simple model satisfactorily fitted the experimental data in Fig. 4(c). Through careful material engineering, robust RS behaviors were obtained and the devices were still functional after 1.5×10^8 P/D pulses.

2.5. GST Devices

Another group of candidates for synaptic emulation are based on phase change memory (PCM) [46]. By applying electric pulses to generate enough heat and induce local phase transitions, phase change materials can exhibit resistance switching behaviors between amorphous (high resistivity) and crystalline (low resistivity) states and this change can be quite fast and stable. GST ($\text{Ge}_2\text{Sb}_2\text{Te}_5$) is the most commonly used material for PCM. Here, phase change is achieved by heating and quenching of GST through Joule heating. Although mostly studied as a digital memory, when programming



and erasing conditions are carefully designed, the GST devices can exhibit analog type resistance changes if the amount of material being melted and re-crystallized can be controlled [47].

Shown in Fig. 5 is a demonstration of analog resistance changes in GST based devices in a study performed by Kuzum et al. [47]. The analog switching was achieved by the application of voltage pulses with incrementally increasing amplitudes, i.e., reset was performed by voltage pulses with increasing amplitude in the range of 2–4 V with 20 mV steps, while set process was achieved by using repeated staircase pulses (20 continuous pulses with amplitudes of 0.5, 0.6, 0.7, 0.8, and 0.9 V). The corresponding incremental resistance changes are shown in Fig. 5(a) for both the set and reset processes [47]. Fig. 5(b) shows the temperature distribution in the cell based on finite element simulations, illustrating that

the voltage pulses incrementally expand the region with temperature ($T > 900$ K) above the melting point of GST. These high temperature regions will be amorphized after the pulses and account for the gradual increase in resistance during reset [47].

3. Device Modeling

Memristor as a device concept was first introduced by the pioneering work of Leon Chua [11] and further formalized by Chua and Kang [12]. Briefly, a device can be called a “memristive system” if it satisfies a set of equations below, with properly chosen state variables:

$$v = R(w, i)i \quad (1)$$

$$\frac{dw}{dt} = f(w, i). \quad (2)$$

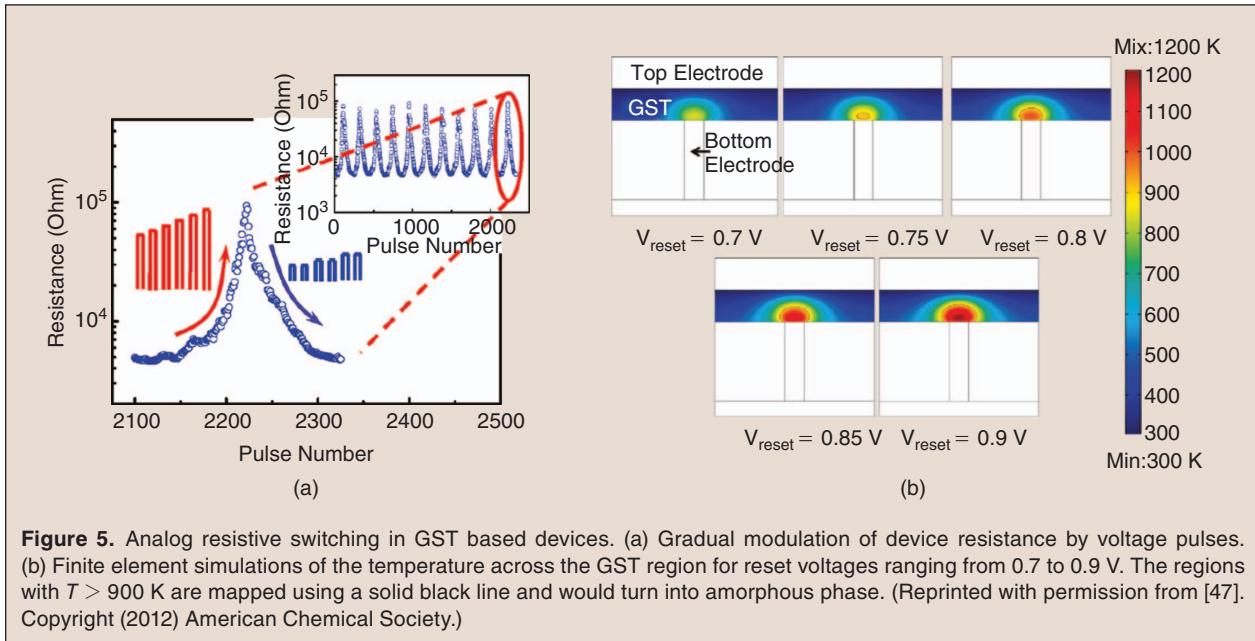


Figure 5. Analog resistive switching in GST based devices. (a) Gradual modulation of device resistance by voltage pulses. (b) Finite element simulations of the temperature across the GST region for reset voltages ranging from 0.7 to 0.9 V. The regions with $T > 900$ K are mapped using a solid black line and would turn into amorphous phase. (Reprinted with permission from [47]. Copyright (2012) American Chemical Society.)

Here the first equation is the normal I - V equation that relates voltage with current through a resistive term. However, for memristive systems, the resistance R (termed memristance) depends not only on the instantaneous inputs v and I , but also on one or a set of internal state variable(s) w . The state variable w is in turn governed in the second equation, which specifies how the state variable changes according to the current state and the instantaneous inputs. Since here only the dynamics of w (i.e. its rate) is determined, the full value of w can only be obtained from a *time integral*, i.e. Eq. (2) implies that the state of the memristor is history dependent, as observed from the experiments on various materials. This is the key difference between a memristor and other two-terminal devices without memory.

The memristor model is based on abstract mathematical equations (1–2), without necessarily specifying the physics behind them. By mapping these equations to the actual physical processes during device operation such as the ionic diffusion/drift processes during conduction channel formation, realistic device operations can be modeled within the memristor framework. Here again the key is to identify the internal state variable(s) and the corresponding dynamic equation (2). The advantage of describing the device operations in the memristor framework, vs. other phenomenological models, is that not only does this approach provide an analytical description that can be readily ported into circuit simulators, but also it helps one to identify the driving factors behind the switching effects so more accurate descriptions, particularly those governing the device dynamics, can be obtained.

3.1. State Variable As the Conduction Channel Length

The first approach to use the memristor model to explain resistive switching was performed by Strukov et al. at HP Labs when trying to characterize the switching behaviors of TiO_2 devices [13]. Recall that RS in TiO_2 is due to the movement of oxygen vacancies inside the TiO_2 film. To connect the memristor equations with physical processes, Strukov assumed that the memristor is composed of two resistors in series, one is undoped with high resistance and the other is doped by V_0 thus having low resistance [13], as schematically shown in Figs. 6(a, b). The total thickness of the film D is separated into the doped and undoped regions, and the total resistance is the sum of the two regions. The length of the doped region is taken as the state variable (w), which can be changed by moving the boundary between the two regions under external field due to the drift of V_{0s} . By assuming Ohmic electronic conduction in both regions and a linear ionic drift with an average ion mobility μ_v in a uniform field, the two memristor equations can be written as:

$$v(t) = \left(R_{\text{ON}} \frac{w(t)}{D} + R_{\text{OFF}} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \quad (3)$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{\text{ON}}}{D} i(t). \quad (4)$$

Although both assumptions—linear ionic drift and a uniform conduction front seem oversimplified the model can still successfully predict the pinched hysteresis and the history-dependent resistance changes. The model was soon refined to include non-linear effects at

high fields such as a more realistic exponential ionic drift model which applies even under normal operations [32]. In one approach, the nonlinear ionic drift was taken into account by multiplying the right side of Eq. (4) with a window function $w(1-w)/D^2$ [13]. The corresponding simulation results are shown in Fig. 6(c), where binary resistive switching can be apparently observed. It should be noted that the memristor equations used here correspond to the “current-controlled” devices which are easy to implement mathematically but are not as practical as the “voltage-controlled” devices since currents are typically much harder to control than voltages in practice, especially in large networks.

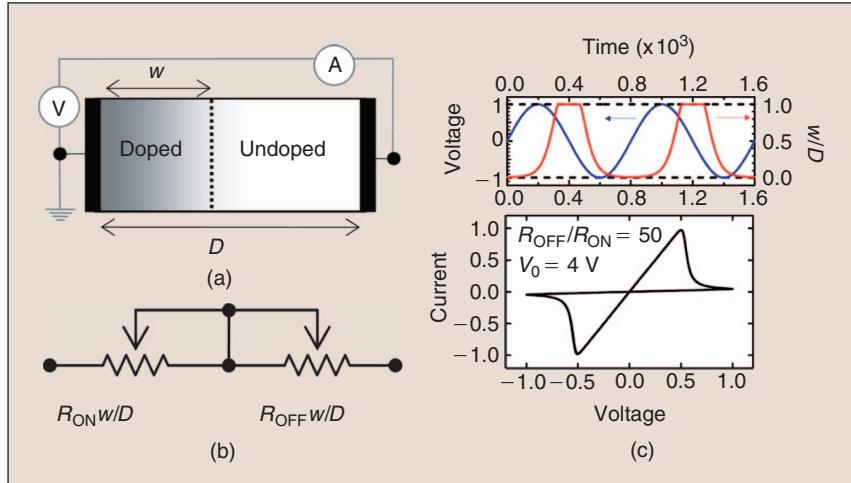


Figure 6. Memristor model for the TiO_2 devices consisting of two resistors in-series. Here the state variable corresponds to the length of the conducting (doped) region. (a) Schematic of the model. (b) Equivalent circuit of (a). (c) Simulation results incorporating nonlinear ionic drift. Upper: The voltage stimulus (blue) and the corresponding change in normalized state variable w/D (red), as functions of time. Lower: Simulated I - V characteristics. (Reprinted with permission from [13]. Copyright (2008) Nature Publishing Group.)

3.2. State Variable As the Conduction Channel Area (Width)

Instead of modeling the state variable as the conduction channel length, which typically leads to non-uniform conductance changes (i.e. the conductance scales as $1/\text{length}$), an alternative is to model the state variable as the conduction channel area (or equivalently, width). This approach seems more natural for many devices since the conduction channels typically form locally and in parallel, instead of creating a uniform front. Additional programming either increases the area (width) of the conduction channel, or increases the number of conduction channels. Both effects are equivalent mathematically and lead to an increase of the effective conduction channel area. Using the conduction channel area as the state variable also leads to more uniform conductance changes, in better agreement with experimental observations.

The first attempt to explain resistance switching using the conduction channel area as the state variable was carried out by the authors to explain the resistance switching in WO_3 [36]. Additionally, a model incorporating an exponential ionic drift equation was used to model oxygen vacancy movement at high fields [32]. In general, the overall device conductance can be calculated as the sum of the conducting regions in parallel with the Schottky barrier formed in the resistive regions, weighted by the state variable (w , which is the conducting region area normalized over the total device area), as shown in the inset of Fig. 7(a):

$$i = (1 - w)\alpha[1 - \exp(-\beta v)] + w\gamma \sinh(\delta v). \quad (5)$$

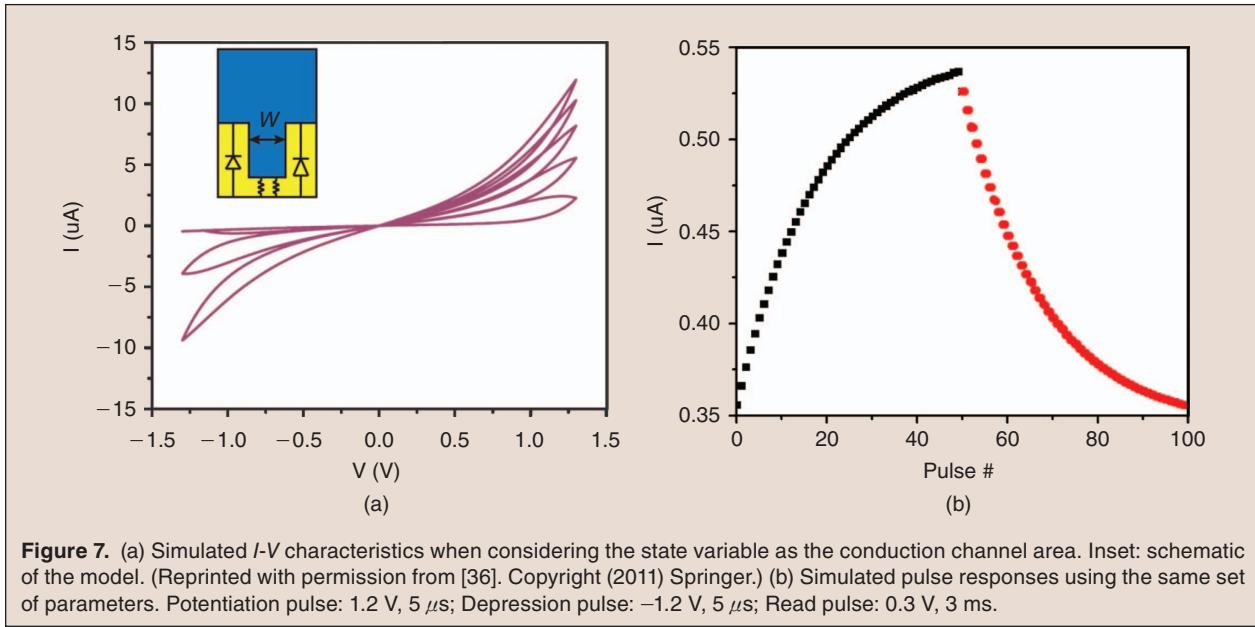
Here the first and second terms represent the contributions from Schottky emission in the resistive regions and tunneling-type conduction in the conducting channels, respectively. α , β , γ , and δ are all positive-valued fitting parameters determined by the material properties. The rate equation is determined by the expansion rate of the conduction region area which is related to the exponential ionic drift:

$$\frac{dw}{dt} = \lambda \sinh(\eta v) - \frac{w}{\tau}. \quad (6)$$

The second term w/τ is introduced here in the dynamic equation to account for the lateral diffusion of ions that constitute the conduction channels (i.e. V_{OS} here). The spontaneous diffusion causes the weakening of the conduction channels and leads to retention loss, an effect that will be discussed in more detail later on.

Figure 7 shows the simulated DC I - V characteristics and pulse responses based on Eqs. (5) and (6), where analog bipolar resistive switching can be reliably predicted using a single set of parameters. The simulation results also show decay in retention, evidenced by the overlap between consecutive I - V curves during positive voltage sweeps, agreeing well with the experimental data [36].

The use of conduction channel area as the state variable to explain RS behavior was recently applied to other oxide systems. For example, NbO_2 is another material that exhibits interesting RS behaviors [48]. Unlike TiO_2 or WO_3 based devices, switching in NbO_2 is attributed to the thermally-driven insulator-to-metal phase transition. Instead of showing memory switching (i.e. the device



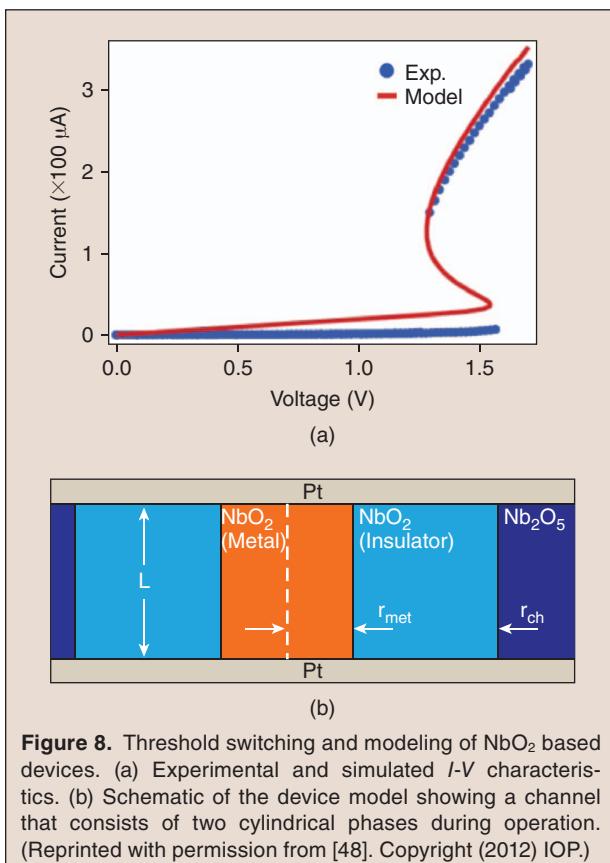
memorizes the new state after removal of the programming voltage), NbO_2 displays threshold switching characteristics (i.e. the device shows abrupt resistance changes but does not memorize the new state after removal of the programming voltage and exhibits negative differential resistance (NDR)), as shown in Fig. 8(a) in a study

performed by Pickett and Williams at HP labs. To model the switching behavior, the device was assumed to have a cylindrical core-shell geometry with a conducting core formed through the metal-insulator transition, and the state variable (u) was chosen as the normalized radius of the conducting core $u = r_{\text{met}}/r_{\text{ch}}$ (Fig. 8(b)). The corresponding equations are provided below.

$$v = f(u, i) = R_{\text{ch}}(u)i \quad (7)$$

$$\frac{du}{dt} = g(u, i) = \left(\frac{d\Delta H}{du}\right)^{-1}(R_{\text{ch}}(u)i^2 - \Gamma_{\text{th}}(u)\Delta T), \quad (8)$$

where R_{ch} is the total device resistance, ΔH is the total enthalpy change in the channel, Γ_{th} is the thermal conductance of the insulating shell, and T is the absolute temperature. This model successfully captured the threshold switching characteristics of NbO_2 devices, as displayed by the excellent agreement between simulation and experimental results shown in Fig. 8(a). Furthermore, circuit simulations based on the memristor model successfully predicted the behavior of these devices in active circuits such as the “neuristor” behaviors that can effectively emulate the lossless transmission in axons [49], [50].



studies have carefully characterized these different 2nd order effects [51]–[53] and produced more accurate analytical and numerical models. The exact switching characteristics are also sensitive to the material selection, preparation methods, neighboring structures, and operating conditions. As a result, it may not always be possible to obtain compact analytical equations in all cases. These difficulties make it even more impressive that surprisingly reliable results can be obtained from the simple first-order analytical equations within the memristor formalism [54], [55].

Another advantage of the analytical equations using the memristor formalism is that they can be readily ported into circuit simulators. Several attempts have been carried out to incorporate the memristor models into simulators such as SPICE, with the most attractive approach of building a subcircuit to emulate the dynamic state variable equation (2) [56]. Such attempts to solve the memristor equations using both the length and area as state variables in SPICE have been successfully demonstrated [36], [57], [58].

4. Synaptic Learning at the Device Level

The plasticity in conductance and the large connectivity that can be offered by memristors make them well suited for physical implementation of synaptic functions in neuromorphic circuits. For example, in a memristor crossbar network shown in Fig. 9(b), first proposed by Snider et al. [59], every neuron on the left (layer 1) can be connected to every neuron at the bottom (layer 2) through plastic connections offered by memristors. Such large connectivity is needed in neuromorphic hardware to produce the large parallelism, but is very difficult to obtain using conventional CMOS-based approaches. Additionally, the memristor synapses can offer a diverse range of biomimicking learning rules that are useful for neuromorphic computing, depending on the internal dynamics of the cations or anions that drive the conductance change.

Biologically, the weight of a synapse is jointly determined by the firing patterns of both the pre-synaptic and post-synaptic neurons connecting to it. The synapse could either be potentiated or depressed, i.e. having their connections being strengthened or weakened, depending on the neuron spike patterns, the transmission/diffusion of ions (e.g. Ca^{2+}), the activation of receptors, and many other factors [60]. Several fundamental learning rules, including rate-dependent synaptic plasticity, timing-dependent synaptic plasticity, and cooperativity [61] have been discovered and believed to be critical for

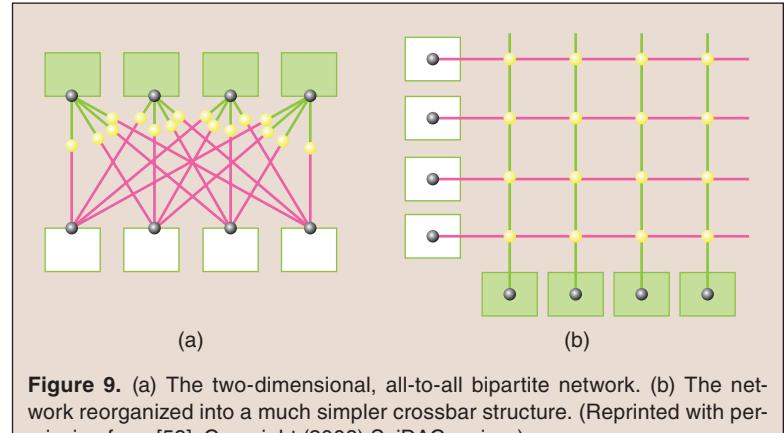


Figure 9. (a) The two-dimensional, all-to-all bipartite network. (b) The network reorganized into a much simpler crossbar structure. (Reprinted with permission from [59]. Copyright (2008) SciDAC review.)

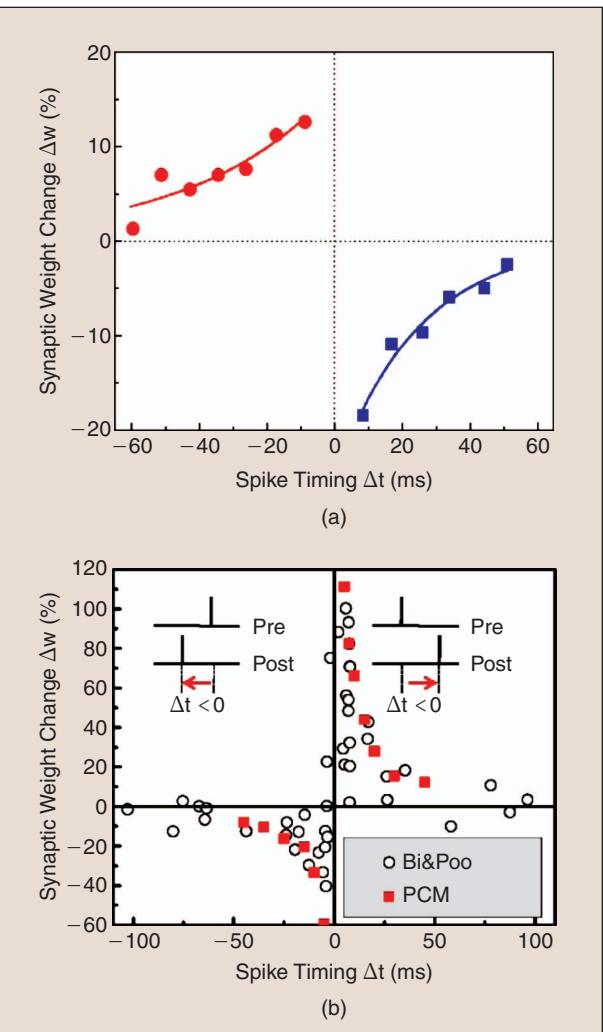


Figure 10. (a) Implementation of STDP with Ag/a-Si based memristors. (Reprinted with permission from [43]. Copyright (2010) American Chemical Society.) (b) Implementation of STDP with GST based PCM cells. (Reprinted with permission from [47]. Copyright (2012) American Chemical Society.)

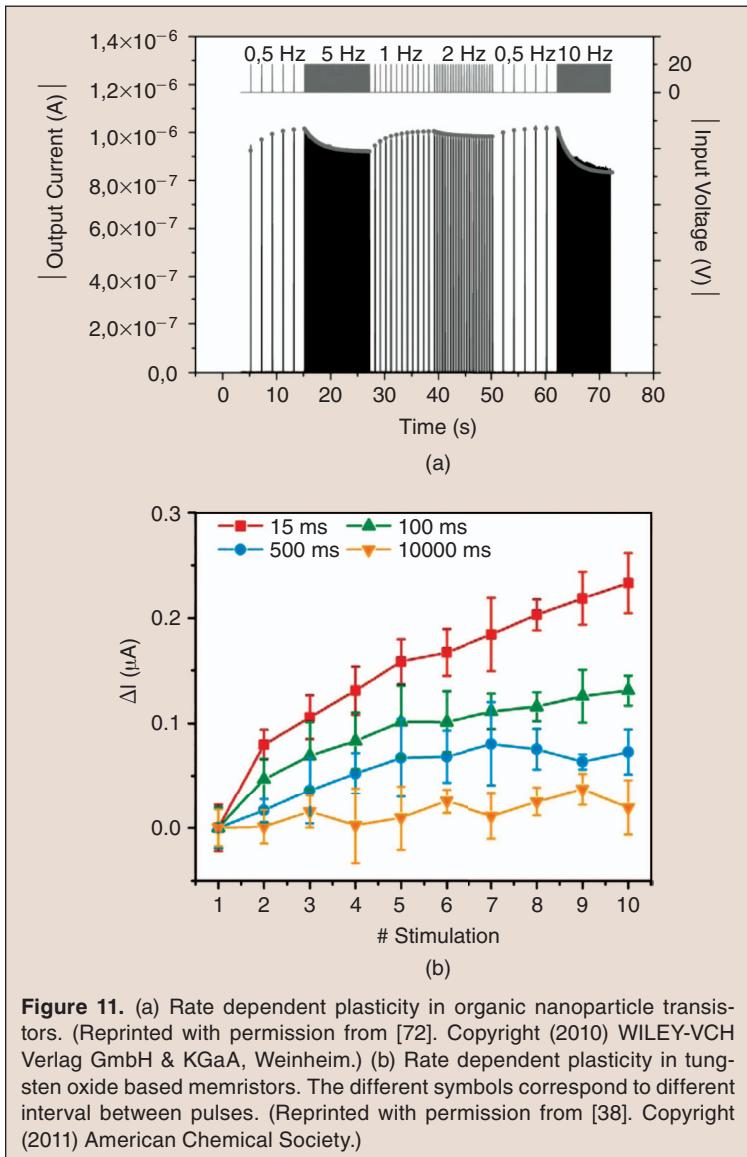


Figure 11. (a) Rate dependent plasticity in organic nanoparticle transistors. (Reprinted with permission from [72]. Copyright (2010) WILEY-VCH Verlag GmbH & KGaA, Weinheim.) (b) Rate dependent plasticity in tungsten oxide based memristors. The different symbols correspond to different interval between pulses. (Reprinted with permission from [38]. Copyright (2011) American Chemical Society.)

the efficient operation of biological systems. While these learning rules may vary according to the specific type and location of a synapse, some commonly-accepted and well-established rules are discussed here. These important local learning rules have also been successfully demonstrated in memristors.

4.1. Spike-Timing-Dependent Plasticity

Spike-Timing-Dependent Plasticity (STDP) is an important synaptic learning rule which states that the synaptic weight is modulated according to the relative timing of the pre- and post-synaptic neuron firing [62], [63]. It was first postulated by in 1949 by D. Hebb who described the effect as “*neurons that fire together, wire together*” [64]. In general, if the spike (action potential) from the pre-synaptic neuron arrives at the synaptic cleft before that of the post-synaptic neuron, potentiation will be induced. Otherwise

depression will be induced. How effectively the potentiation and depression take place in turn depends on how far apart the pre- and post-synaptic spikes arrive.

Implementation of STDP with memristors requires the careful design of neuronal input signals at both the pre- and post-terminals. The key is to find a means to translate the relative spike timing into a signal that directly controls the memristor conductance change, i.e. a specific voltage (current) waveform that controls the flux or charge through the device. Triangular waves, complementary square waves, pulses with exponentially decreasing tails, or other asymmetric waveforms are common examples of the proposed neuronal inputs which could either be realized through test programs or hardware circuits [6], [43], [47], [65]–[68]. In all of these attempts, the relative timing between the signals from the post-synaptic neuron and that of the pre-synaptic neuron determines how the signals overlap at the memristor junction, which in turn tunes the memristor conductance accordingly.

The first work of this kind was performed by the authors with a hybrid CMOS/memristor circuit, as shown in Fig. 10(a) [43]. Timing information is encoded using the time division multiplexing (TDM) scheme which allocates events to occur at their prescribed time slots, while keeping the spike amplitude constant [69]. This approach, with a fixed spike amplitude but modulated effective width, is more effective for digital neuron circuits. STDP curves with controlled time constants

and incremental changes can be obtained, and by choosing the right device parameters results in good agreement with recorded data from biological synapses can be obtained (Fig. 10(a)). Subsequent work by Kuzum et al. implemented using GST based phase change cells used a dedicated pulsing scheme that precisely controls the crystallization states of the GST devices, as shown in Fig. 10(b) [47]. By adjusting the pulsing waveforms to cause different overlapped signal amplitudes seen by the memristor, a few different forms of STDP curves were observed, similar to observations in neurobiological experiments. Several other similar studies have also been reported to obtain STDP behaviors in different material systems [65], [68].

4.2. Rate-Dependent Plasticity

In addition to STDP, rate-dependent plasticity is also a widely observed synaptic learning rule across different

kinds of synapses [61]. It is not surprising—both the pre- and post-neurons fire at seemingly random time instants and one can either group the signals arriving at the synapse by pairs from the two neurons, or by spike trains from individual neurons. In the second picture, the spike rate should have a significant effect on the synaptic plasticity. It is natural to expect that the more frequently a synapse is being stimulated, the stronger it becomes (and remains strong). For example, by stimulating biological synapses at varying rates, post-tetanic potentiation (PTP) and paired-pulse facilitation (PPF) effects were studied systematically with their according decay time constants identified [70], [71].

The key to the implementation of rate-dependent learning is identifying an internal decaying element. Without decay the device will only respond to the total number of stimulations, insensitive to the frequency (rate). However, with a decaying mechanism, the synaptic adaptation is a result of the competing effects between

the internal decay and the external stimulation and how effective the learning becomes then critically depends on the stimulation rate (with respect to the decay rate).

The first report on rate-dependency of memristive devices was by Alibart *et al.* [72] The memristive devices were based on organic nanoparticle transistors in which the synaptic plasticity was achieved by trapping and detrapping of charged carriers which in turn affect the transistor drain current. The nanoparticles were alternatively charged during the pulse period and discharged (decayed) during the intervals between pulses. The total trapped charges then depend on not only the number of pulses but also the frequency. As shown in Fig. 11(a), in the high stimulating rate case, such as 2, 5, and 10 Hz, the number of holes that are trapped in the nanoparticles exceeds that of detrapped ones. As a result, the number of holes present in the channel is increased, depressing the output current. Adversely, the output current is increased in the low stimulating rate case such as 0.5 and 1 Hz. This

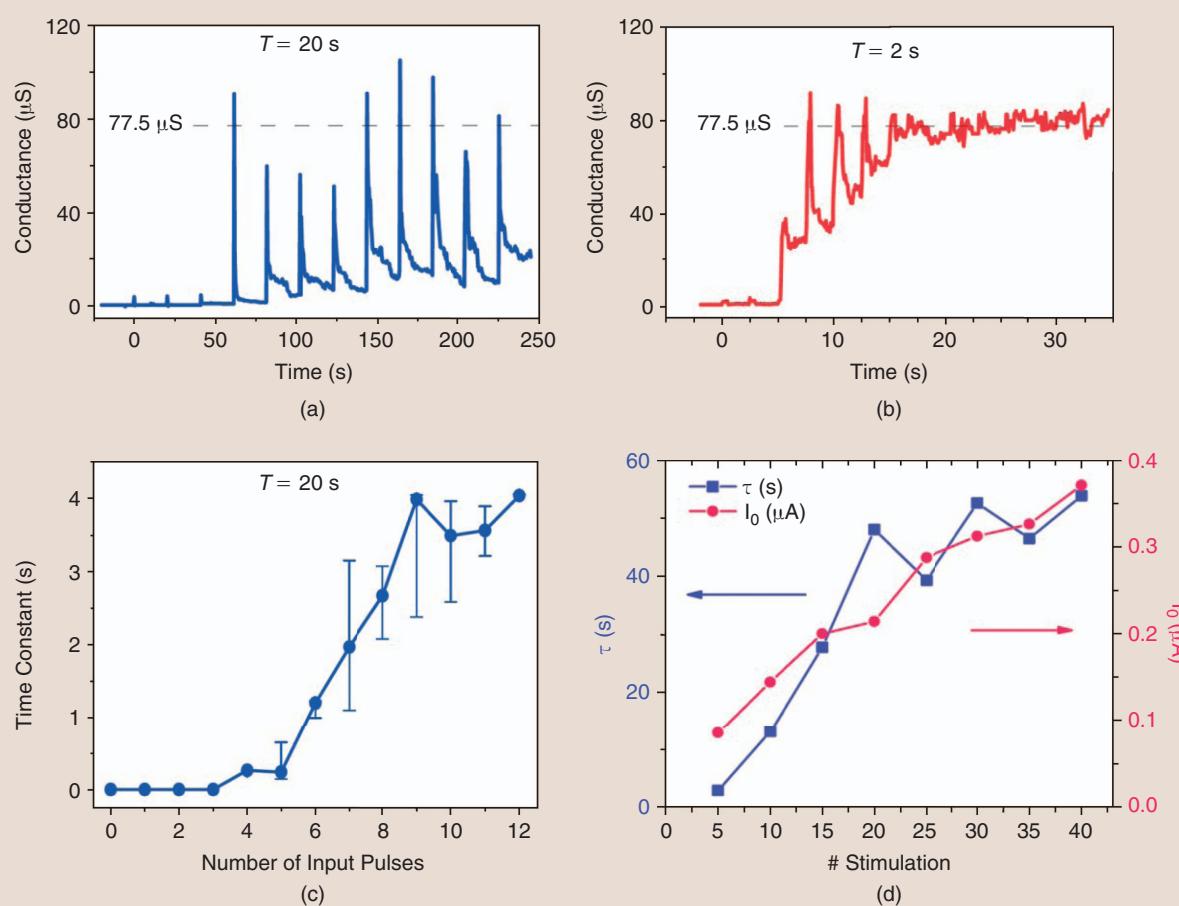


Figure 12. (a) and (b) Decay and stabilization of the conductance of Ag_2S based devices when the input pulses were applied with intervals of 20 s (a) and 2 s (b). (c) Decay time constant as a function of the number of input pulses for Ag_2S based devices. (Reprinted with permission from [42]. Copyright (2011) Nature Publishing Group.) (d) Time constant and synaptic weight as a function of the number of input pulses for WO_x based devices. (Reprinted with permission from [38]. Copyright (2011) American Chemical Society.)

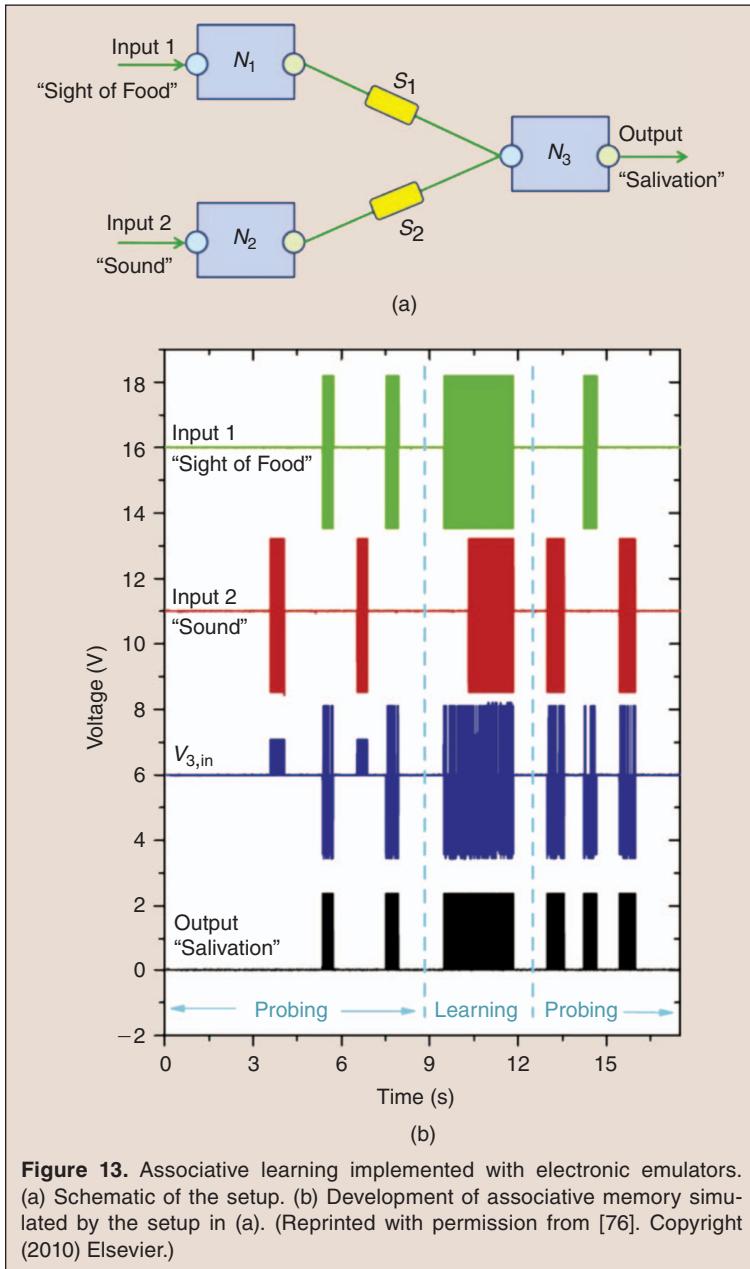


Figure 13. Associative learning implemented with electronic emulators. (a) Schematic of the setup. (b) Development of associative memory simulated by the setup in (a). (Reprinted with permission from [76]. Copyright (2010) Elsevier.)

charge trapping/detrapping process is argued to be analogous to the rate dependent synaptic plasticity caused by consumption and recovery of the finite chemical neurotransmitters in biological synapses [73] and can potentially be used to implement rate-dependent learning rules.

The nanoparticle transistor devices are however three-terminal devices which make scaling more difficult. A more systematic study on two-terminal memristor devices were performed by the authors on WO_3 memristors [38]. As shown in Fig. 11(b), a high stimulation rate (smaller interval between pulses) leads to more significant conductance enhancement while the device barely responds to stimulations at low rate, even though both the strength and the number of stimulations are identical

in each case. Here the decay term is the spontaneous diffusion of the oxygen vacancies forming the conduction channels, discussed in Eq. (6). PTP and PPF effects with behaviors similar to those in biological systems have also been obtained in these oxide memristor devices [38]. The internal decay of the conduction channels in turn suggests that the devices possess short memory retention (analogous to short-term memory in biological systems). Although short retention is obviously not desirable for non-volatile data storage, the decay and short-term memory can be desirable properties for neuromorphic circuit implementations, as will be discussed next.

4.3. Short-Term and Long-Term Plasticity

While long-term plasticity (LTP) is obviously needed for storing the processed information, it is believed that short-term plasticity (STP) helps the system process information by releasing resources that are no longer needed [60]. Biologically, it is still debatable whether these two kinds of plasticity take place at the same location and how one may trigger the other. However, it seems clear that there exist short- and long-memory regimes, separated by their retention times. Additionally, short-term memory can be converted to long-term memory after sufficient training. In computation, this corresponds to a very practical mechanism to allocate limited resources (e.g. the number of physical synapses) for the most efficient use since the more crucial the information, the longer the memory is kept.

Two independent studies were performed that showed the existence of STP and the transition of STP to LTP in memristive devices. These effects were observed first by Ohno et al. in Ag_2S devices [42], shown in Fig. 12(a). One can see that the device conductance always decays back to its initial value when low-repetition rate pulses are applied, suggesting STP. However, when the repetition rate is increased to a certain value, a stable high conductance state can be achieved (Fig. 12(b)), indicating a transition from STP to LTP and corresponding to the formation of a stable conducting bridge in the Ag_2S device. It was found that the decay time of the STP state (i.e. how fast STP loses its information) also depends on the training conditions, with longer time constants obtained when the number of input pulses is increased, as displayed in Fig. 12(c).

In another study reported at roughly the same time, the authors observed STP and STP to LTP transition in WO_3 devices, as shown in Fig. 12(d). Briefly, the conduction channel area in the memristors is increased through repeated stimulation, which not only leads to an increased conductance (weight) but also longer retention time [38]. This effect corresponds well to the memory enhancement effects observed in biological systems which lead to the transition from STP to LTP [74]. Additionally, both the stimulation rate and the total number of stimulations are found to strongly affect the memory enhancement. With sufficient stimulations, the retention time can be increased by 20 folds, indicating a transition from STP to LTP can be achieved in the memristors [38].

5. Learning at the Network Level

Memristors are perhaps the ideal candidate to implement local, synaptic learning rules for the implementation of efficient neuromorphic circuits. However, assembling a large number of individual working devices does not necessarily make a system functional. How functions emerge from biological networks is of course still an ongoing research in the field of neuroscience and research on memristor-based neuromorphic hardware in this field is still at the very early stage. Here we only focus on a few experimental studies of memristor circuits performed so far at the “network” (mostly very small scale) level.

5.1. Associative Learning

Associative learning is a form of Hebbian learning experimentally demonstrated by the training of Pavlov’s dog [75]. By pairing conditioned stimulus (e.g. sound of a bell) with unconditioned stimulus (e.g. sight of food), the dog learns to associate both events and responds (e.g. salivates) to both stimuli. Associative learning is especially important as it is believed to be behind how brains correlate individual events and how neural networks perform certain tasks very effectively. First proposed by Pershin et al., synaptic emulators and specially-designed circuitry were developed to demonstrate associative learning [76]. Fig. 13 shows the results from a study by Pershin et al., where before learning the “salivation” neuron only responds to the “sight of food” neuron input, i.e. only synapse S1 is on. By simultaneously applying stimulations to both the “sight of food” and “sound” neurons in the learning phase, synapse S2 between the “sound” neuron and the “salivation” neuron is turned on. As a result, stimulus from the “sound” neuron alone is able to excite the “salivation” neuron, therefore establishing an association between the conditioned and unconditioned stimuli. Zeigler et al. later demonstrated associative learning with $\text{Ge}_{0.3}\text{Se}_{0.7}$ memristors [77]. Along with their neuron-mimicking circuit, both associative and non-associative learning could be implemented.

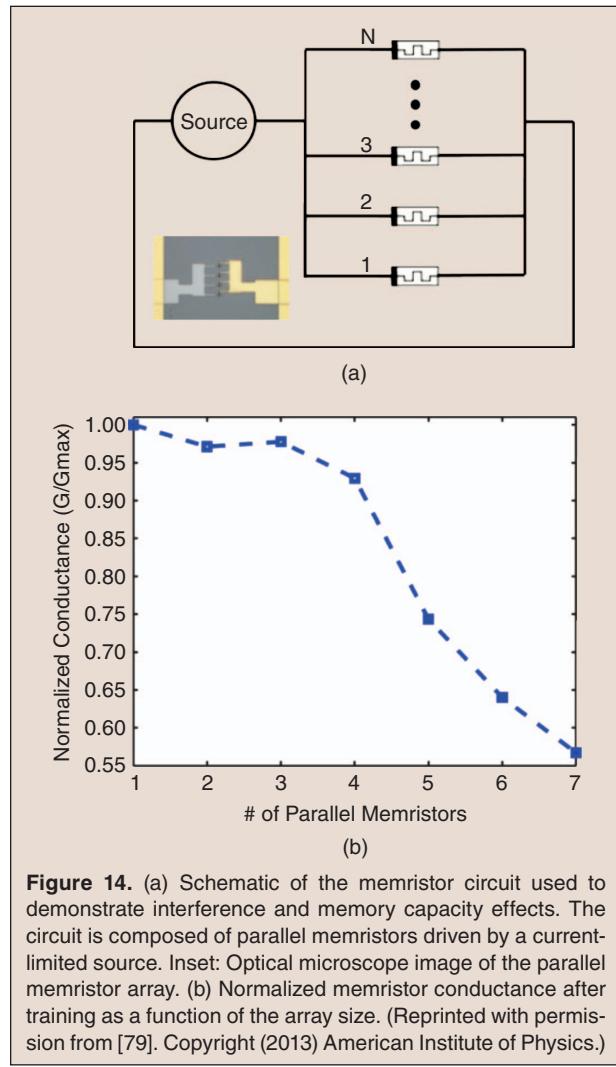
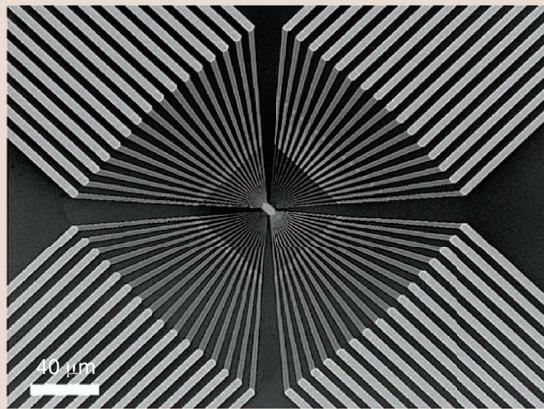


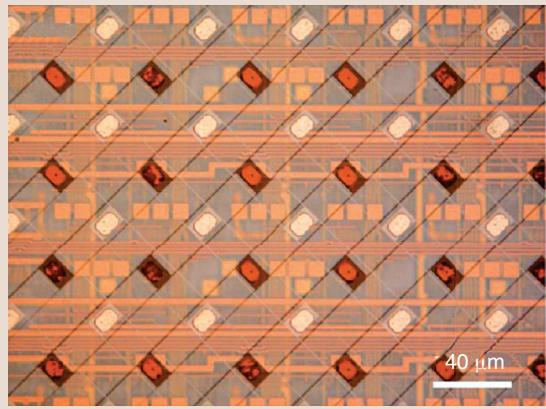
Figure 14. (a) Schematic of the memristor circuit used to demonstrate interference and memory capacity effects. The circuit is composed of parallel memristors driven by a current-limited source. Inset: Optical microscope image of the parallel memristor array. (b) Normalized memristor conductance after training as a function of the array size. (Reprinted with permission from [79]. Copyright (2013) American Institute of Physics.)

5.2. Emergent Behaviors

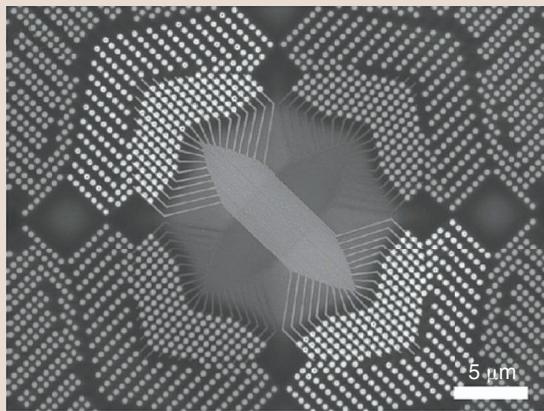
Emergent behaviors arise when individual elements interact with each other in a random, complex network, achieving collective behaviors that are not expected from the simple sum of individual elements. Since biological neural networks are highly complex systems with numerous interconnected elements, the evolution of emergent behaviors is believed to be key to the development of network functions. A primitive attempt to achieve emergent behaviors in memristor networks was performed by Stieg et al. when studying self-assembled Ag nanowire networks that are interconnected randomly [78]. A wide range of discrete, metastable conductance states were observed that were explained by the dynamic reorganization of the interconnected atomic switch network. Such collective behavior is believed to be similar to that of complex neural networks and if can be understood and controlled, can hold potential for efficient memory, information transmission and adaptability.



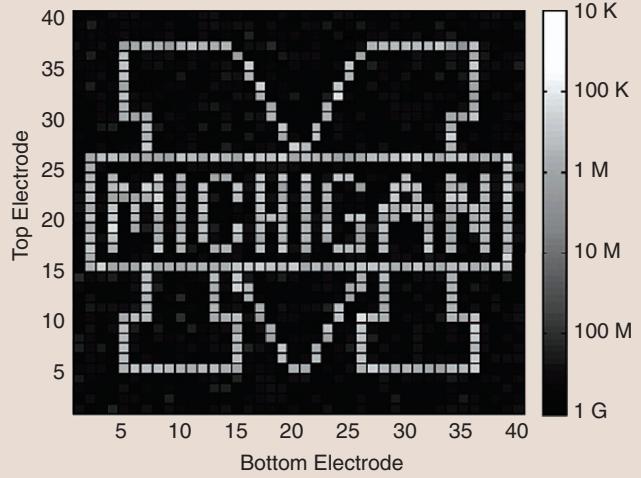
(a)



(b)



(c)



(d)

Figure 15. (a) SEM image of a 32×32 Ag/a-Si/p-Si crossbar array on an SiO_2/Si substrate. (Reprinted with permission from [19]. Copyright (2009) American Chemical Society.) (b) Optical micrograph of a Pt/TiO₂/Pt crossbar array on CMOS chip. (Reprinted with permission from [81]. Copyright (2009) American Chemical Society.) (c) SEM image of a 40×40 Ag/a-Si/SiGe crossbar array on CMOS chip. (d) A bitmap image by storing and retrieving data in the 40×40 crossbar array in (c). (Reprinted with permission from [80]. Copyright (2012) American Chemical Society.)

Emergence is one-step further in neuromorphic development because it only appears at the network level, never at the synaptic or neuronal level. However, the unpredictability of emergent behaviors also implies that there might not be a “correct” answer; instead, the behaviors of the network evolve with the characteristics of individual elements, dynamic environments, and the physical network connectivity (which can be enormous and random). As a result, useful information may only be obtained from statistics, and through a large number of controlled experiments.

5.3. Limited Capacity Effect

Another reason that unexpected results may arise when individual devices are connected in a network is that the different devices now share and compete for the same resources. Depending on the specific physical

configurations, inputs and dynamics of the network and the devices, diverse results can thus be obtained when individual elements, small networks, or large networks are formed.

The competition effect was recently demonstrated by the authors in a study focused on how resources are distributed among competing elements in a network, and how different results can be obtained depending on the network size (Fig. 14) [79]. Here a circuit of parallel-memristors connected to a constant current source was studied both through simulation and experiments using WO_3 devices. Specifically, how well the memristors are trained was found to depend on the network size, due to the competition between training (which is amplified by the interference effect) and internal state decay in each memristor. The more memristors sharing the limited current source, the less firmly each memristor is

trained, as shown by Fig. 14(b). Essentially, this study demonstrated the limited memory capacity effect found in psychology studies—the ability to recall information stored in short-term memory falls off significantly beyond a certain list size. By tuning the circuit parameters, different critical list sizes can also be obtained (e.g. a critical list size of 4 matching that found in psychology studies is shown in Fig. 14(b)).

6. Memristor Crossbar Network Hardware

Hardware implementation of more complex synaptic functions demands larger-scale memristor networks with inherently high connectivity. Several studies have been carried out recently to construct memristor arrays based on the success on single devices, mostly focusing on implementing basic memory [19], [80] and logic [81] functions so far. The simple two-terminal structure of memristive devices allows them to be integrated into crossbar networks, composed of two sets of parallel nanowire electrodes crossing each other with a memristive device formed at each crosspoint. This configuration potentially provides both the high density and high connectivity that are required to emulate neuromorphic systems. For example, a human cortex has about 10^{10} synapses/cm² in density and can be achieved in crossbar arrays with 100 nm pitch.

Fig. 15(a) shows an SEM image of a 32×32 memristor crossbar array fabricated on SiO₂/Si substrates by the authors [19]. Efforts were soon extended to building similar crossbar arrays on top of CMOS chips in order to combine the functionalities of CMOS circuits with the properties of memristive devices. Such hybrid memristor/CMOS crossbar arrays have been demonstrated with both cation and anion migration based devices, e.g. using Ag/a-Si/SiGe [80] and Pt/TiO₂/Pt [81] devices, respectively. Figure 15(b) shows the optical graph of a Pt/TiO₂/Pt array fabricated on CMOS substrate via nanoimprint lithography, following an approach based on CMOL [82], [83]. The hybrid memristor/CMOS system demonstrated field programmable gate array-like functionalities [81]. Fig. 15(c) shows a 40×40 Ag/a-Si/SiGe crossbar array fabricated on a CMOS chip using local interconnects by the authors, showing reliable memory operations (Figs. 15(c,d)) [80]. These hybrid memristor/CMOS arrays can potentially accommodate large crossbar networks and can thus provide a good platform for studying complex neuromorphic functions in these networks. However, we note that studies so far are only limited to relatively simple memory and binary logic demonstration, while the development of functional memristor-based neuromorphic networks requires much more complex neuron designs and better understanding and control of the memristor

dynamics, as well as better understanding of how functions and emergent behaviors evolve in large networks.

7. Conclusion

In summary, tremendous progress has been made in the last a few years on the development of memristive devices and the employment of such devices in neuromorphic systems. Device operation mechanism, performance optimization and modeling have been extensively studied. A diverse range of local learning rules have been demonstrated and prototype memristor crossbar arrays with very large connectivity and hybrid memristor array/CMOS neuron systems have been demonstrated. However, despite the rapid progress, the field is still only at its infancy. For example, studies of the network dynamics and emergent behaviors have just started, although preliminary results obtained from the few experimental and simulation studies to date are already quite exciting and indicate more breakthroughs to come.

Looking into the future, we have every reason to believe this field will continue to enjoy exponential growth. It is likely that in a few years memristor-based neuromorphic hardware will be available to anyone interested in them, like carbon nanotube or graphene is today to device researchers. This will further fuel the development of modeling, new algorithms and architectures to most efficiently utilize this new class of hardware, which will in turn speed up device research to take advantage of the new algorithms. It is intriguing to imagine a future where smart neuromorphic chips significantly improve our quality of life. However, this Hercules task can only be achieved through close collaborations among material scientists, device physicists, electrical and computer engineers, and computer scientists.



Ting Chang received her B.S. from National Chiao Tung University, Taiwan in 2006 and Ph.D. from the University of Michigan—Ann Arbor in 2012. At UM her research focused on neuromorphic applications of solid state memristor devices, in particular, synaptic emulation and bio-mimicking of learning behaviors in tungsten oxide-based memristors. She currently works as an engineer at Intel Corporation.



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