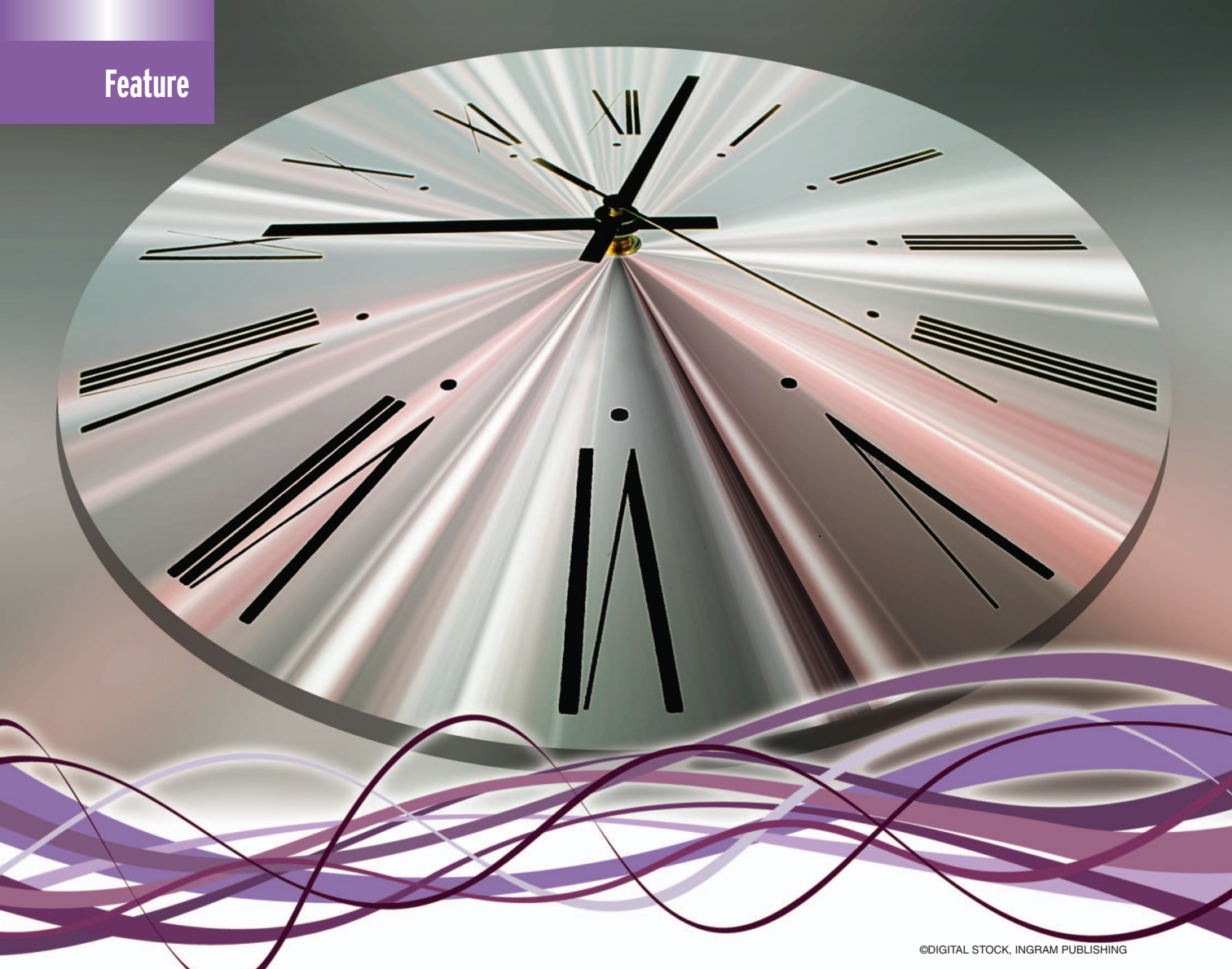

Clock Jitter Effects on Sampling: A Tutorial

Carlos Azeredo-Leme

Abstract

The effect of jitter in data converters is analyzed, with a focus on the frequency domain treatment of the corresponding phase noise. The analysis is mostly intuitive, to give the reader a good feeling for the mechanisms involved. Both open loop oscillators and phase locked loops are considered as clock sources. Several application examples are included to illustrate the concepts. Jitter self-referenced measurements are also covered with their relationships to jitter.

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1. Introduction

Clock Jitter is probably the most obscure specification in data converters. It basically describes the timing errors in the sampling operation due to clock disturbances.

In fact, the clock applied to the data converter determines the timing of the samples produced from the input signal. Therefore, the clock must be treated as a delicate analog signal and any disturbances minimized.

Assuming an Analog-to-Digital Converter, ADC, the clock is determinant to the sampling process that normally takes place at the very first stage. Fig. 1 shows a simplified form of a sampler.

When the clock goes HIGH, the switch is closed and the capacitor is charged to the value of the input signal. When the clock goes LOW, the switch is opened and the capacitor stores the value of the input signal that will be processed further for digitization.

In this circuit, it is the instant when the clock goes LOW that determines the sampling time, the falling edge of the clock. Any small disturbances to the amplitude of the clock have no effect because the switch is a binary device and distinguishes clearly the state HIGH from LOW even if it fluctuates a little in amplitude. But any timing disturbance has a direct effect on the value sampled and generates an error.

This error cannot be corrected later in the ADC because it is already attached into the sampling sequence being processed for digitization and will impact the overall performance of the ADC.

Therefore, clock jitter is critical to the performance of an ADC and must be specified appropriately. How much of it is acceptable? How do timing errors translate into the overall performance? To answer these questions is the purpose of this Tutorial.

II. Why Jitter Matters

As data converters have evolved to always-higher sampling frequencies and higher resolutions, they become more sensitive to the external conditions. Clock timing quality is one of them.

Nyquist Sampling Theorem assumes periodic sampling. Any deviation to the ideal sampling instant is defined as "jitter". Fig. 2 illustrates how jitter generates an error.

Assuming a jitter value of Δt on the sampling instant, the error produced is proportional to the derivative of the input signal [1], [2]:

$$v_{\text{error}} = \Delta t \frac{dv_{\text{in}}}{dt}. \tag{1}$$

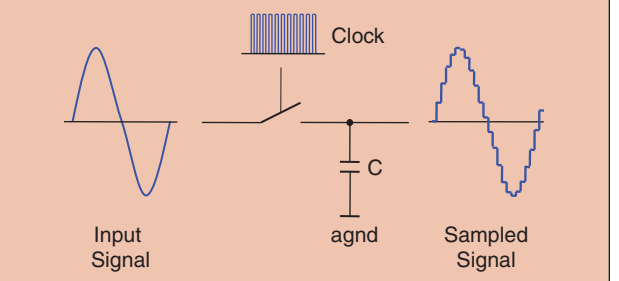

Figure 1. Sampling operation.

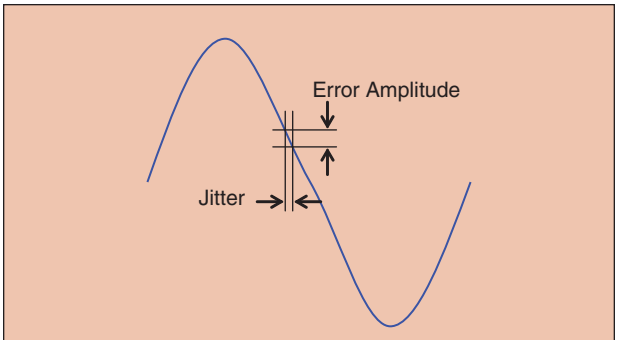

Figure 2. Sampled value uncertainty vs. sampling time uncertainty (jitter).

For a sinewave of frequency f_{in} and amplitude A_{in}, the maximum error is at the zero crossings:

$$v_{\text{error max}} = \Delta t\, A_{\text{in}}\, 2\pi f_{\text{in}}. \tag{2}$$

In order to have this error below 0.5 LSB in a N-bit data converter with input range $+/-A_{\text{in}}$, the maximum value of the jitter is

$$v_{\text{error}} < \frac{A_{\text{in}}}{2^N} \rightarrow \Delta t < \frac{1}{2\pi\, f_{\text{in}}\, 2^N}. \tag{3}$$

For example, for a 12 bit 100 MS/s ADC with maximum bandwidth of 50 MHz, the peak-to-peak jitter specification is 0.8 ps. This kind of jitter requires a very high performance clock generator.

The same analysis applies to Digital-to-Analog converters, DACs, where the relevant clock is the one at the last interface from the discrete-time domain, where the signal samples get sampled-and-held for further continuous-time processing.

III. Sampling Errors Due to Jitter

Jitter statistics are typically similar to random noise. Therefore, equation (3) is often exaggerated. Most relevant is to reflect the effect of jitter on SNR.

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The jitter sampling error is not affected by the actual clock frequency.

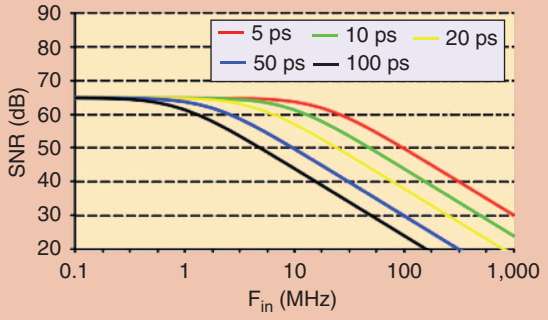

Figure 3. SNR degradation due to sampling clock jitter for a converter with SNR_{ADC} = 65 dB.

Let's denote Δt_{rms} as the standard deviation of clock jitter (or root mean square). We can then re-write the sampling error in (1) as:

$$\sigma(v_{\text{error}}) = \Delta t_{rms}\,\sigma\left(\frac{dv_{\text{in}}}{dt}\right) = \Delta t_{rms} \cdot 2\pi f_{\text{in}} \frac{A_{\text{in}}}{\sqrt{2}}, \qquad (4)$$

where $\sigma()$ is the root mean square operator.

The resulting SNR on the sampled sinewave is then [3]:

$$SNR_{\text{Jitter}} = 20\log\left(\frac{A_{\text{in}}/\sqrt{2}}{\Delta t_{rms} \cdot 2\pi f_{\text{in}} \frac{A_{\text{in}}}{\sqrt{2}}}\right)$$

$$= -20\log(\Delta t_{rms} \cdot 2\pi f_{\text{in}})\ [\text{dB}]. \qquad (5)$$

This SNR_{Jitter} limitation must be added to the intrinsic ADC SNR limitation, SNR_{ADC}. SNR_{ADC} is typically determined by quantization and thermal noise and is dependent on the ADC implementation. The overall SNR achieved, SNR_{Total}, that includes the intrinsic performance of the ADC and the effect of the clock jitter, can then be expressed as [4]:

$$SNR_{\text{Total}} = -20\log\sqrt{10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{\text{Jitter}}}{10}\right)}}\ [\text{dB}]. \qquad (6)$$

Fig. 3 illustrates this equation for an SNR_{ADC} of 65 dB. It shows the SNR_{Total} as a function of the sampling clock jitter (rms) and signal frequency (f_{in}).

Some key points can be derived from this analysis:

1) The jitter sampling error is not affected by the actual clock frequency
2) SNR performance at low frequency is not impacted by jitter
3) But at high frequency, jitter can be the dominant limiting factor on SNR performance

Tables 1 and 2 illustrate this for some concrete cases assuming an ADC with an intrinsic SNR of 65 dB.

As can be seen, for a 1 MHz signal, the SNR_{total} is close to the SNR_{ADC}, with little impact from jitter. However, for a 50 MHz signal, the SNR_{total} degrades strongly with the effect of jitter.

Table 1.

Maximum F_{in}	Jitter
1 MHz	13.15 ps rms
50 MHz	2.63 ps rms

Allowed clock jitter assuming SNR_{ADC} = 65 dB for achieving an SNR_{Total} of 60 dB

Table 2.

Maximum F_{in}	SNR_{Total}
1 MHz	64.9 dB
50 MHz	47.6 dB

Overall SNR assuming SNR_{ADC} = 65 dB and a jitter of 13.15 ps rms

IV. Jitter in the Frequency Domain

The traditional method presented above, based on equation (5) to obtain the SNR as a function of clock jitter and signal frequency, has some limitations.

Firstly, it assumes a very extreme situation of a full-scale sinewave input at the maximum frequency corner of the signal bandwidth. Although this situation may happen in some applications, most commonly the input signal energy is spread over some bandwidth much below the sampling frequency. On the other hand, in subsampling systems the signal band is actually above the sampling frequency.

Secondly, it attaches all the sampling error to the output signal even if part of it may lie out-of-band and, therefore, is removed by a later filter stage.

In order to take these situations into account, a spectrum representation of the sampling error is required. The voltage sampling error is given by the sampling time error, or jitter, multiplied by the time derivative of the input signal at the sampling time:

$$v_{\text{error}}(k) = \Delta t(kT_S) \cdot \left.\frac{dv_{\text{in}}(t)}{dt}\right|_{kT_S}. \qquad (7)$$

Taking the discrete-time Fourier transform (DTFT) [5],

$$\mathbb{F}(v_{\text{error}}(k)) = \mathbb{F}(\Delta t(kT_S)) * \mathbb{F}\left(\left.\frac{dv_{\text{in}}(t)}{dt}\right|_{kT_S}\right), \tag{8}$$

where $\mathbb{F}$ denotes the DTFT and * denotes convolution. Therefore, the spectrum of the sampling error is the convolution of the jitter spectrum with the spectrum of the *time-derivative* of the input signal at the sampling instants.

Assuming that the input signal and the clock are independent (for example, the signal is not disturbed by the clock and not already sampled), then (8) can be simplified to

$$V_{\text{error}}(f) = \Delta T(f) * j2\pi f \cdot V_{\text{in}}(f), \tag{9}$$

which relates directly the spectrum variables of, respectively, the sampling error, the jitter and the input signal.

Assuming a sinewave as the input, the jitter spectrum will be scaled by the value of the input frequency (in rad/s), and will be centered on its frequency by the convolution operation:

$$V_{\text{error}}(f) = 2\pi f_{\text{in}} \cdot \frac{A_{\text{in}}}{\sqrt{2}} \cdot \Delta T(f - f_{\text{in}}). \tag{10}$$

The clock is often derived from a PLL using a ring or LC oscillator. Then, the spectrum of its jitter follows the shape illustrated in Fig. 4. It is reasonably flat within the loop bandwidth, and falls outside. Therefore, most of the jitter energy is at relatively low frequencies.

Fig. 5 illustrates the resulting spectrum for an input signal composed of several sinewaves of different frequencies. In the upper plot, there are three sinewaves at frequencies respectively f_1, f_2, and f_3 and the clock at frequency F_S. The clock jitter can be seen as side-lobes around its center frequency, corresponding to the jitter spectrum scaled by the clock frequency itself (or phase noise).

The bottom plot shows the spectrum of the sampled signal until half the sampling frequency. As expected, the sampling error shows as side-lobes around the respective center frequencies, with amplitude proportional to the radian frequency of the sampled sinewave. Most interesting is f_3 that is above the clock frequency and therefore is sub-sampled. Even if it is shifted to low frequency $f_3 - F_S$, its sampling error is the largest because it is proportional to the frequency of input signal that is sampled.

V. Phase Noise

The spectrum of jitter is very difficult to measure directly. But it is quite straightforward to measure the phase noise of a clock signal. A common spectrum analyzer can be used, if the clock amplitude is reasonably free

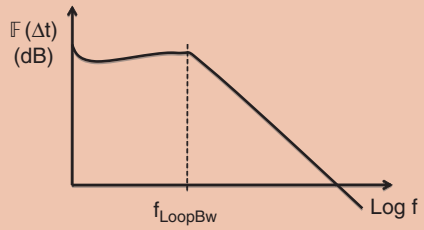

Figure 4. Typical spectrum shape of the clock jitter produced by a PLL.

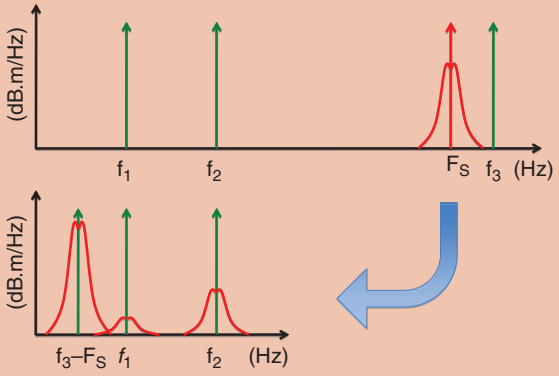

Figure 5. Illustration of the jitter spectrum on sinewave inputs.

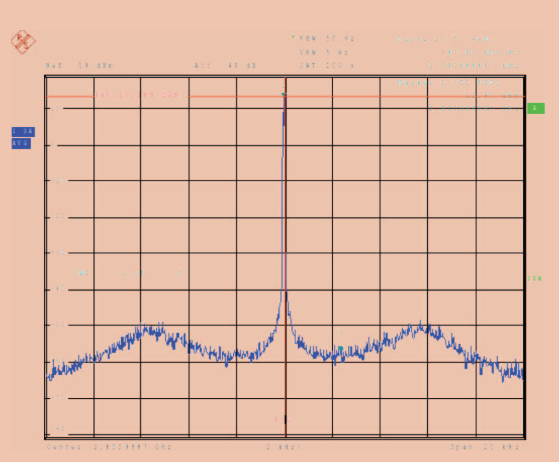

Figure 6. Plot of the phase noise on a spectrum analyzer.

of noise. Fig. 6 illustrates a plot of the spectrum around the clock frequency. The phase noise is clearly visible as sidelobes around the clock frequency.

Some spectrum analyzers with a phase noise module allow plotting the frequency axis relative to the clock center frequency. This allows obtaining a single-sideband spectrum plot in logarithmic scale as shown in Fig. 7.

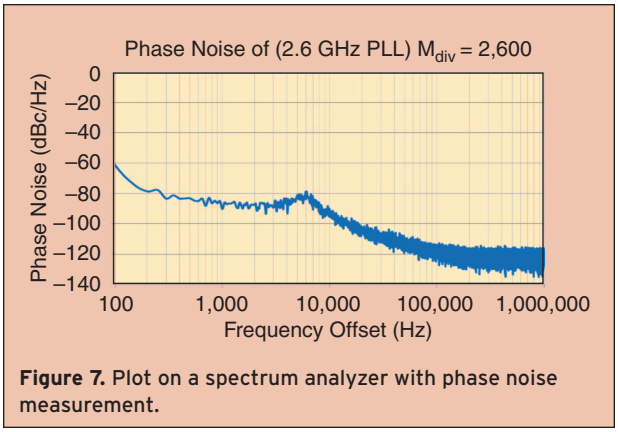

Figure 7. Plot on a spectrum analyzer with phase noise measurement.

The phase noise of a clock signal is its phase modulation due to the time-domain instabilities, or jitter. For simplicity, let's represent the clock as a sinewave of frequency F_S [6]:

$$\begin{aligned} v_{\text{clock}} &= A\sin(2\pi F_S(t+\Delta t(t))) \\ &= A\sin(2\pi F_S t + \phi(t)), \end{aligned} \tag{11}$$

where $\phi(t)$ is the phase noise in the time domain. Assuming $\phi(t)$ small,

$$v_{\text{clock}} \cong A\sin(2\pi F_S t) + A\cos(2\pi F_S t)\,\phi(t). \tag{12}$$

The second term of this expression is the additive noise due to the phase modulation. The phase noise appears multiplied by a cosine at the clock frequency. It follows that in the frequency domain the spectrum of the phase noise, $\Phi(f)$, is convolved with the noise-free clock and appears as sidebands around its center frequency, as seen in Fig. 6.

It is often represented as $L(f)$, or single-sideband phase noise power spectrum, and is equal to the noise power spectral density per Hertz at the frequency $F_s + f$ divided by the clock signal power $A^2/2$. It is called single-sideband because only one side of the noise power is taken into account, so it includes only half the noise energy. Therefore, it is related to $\Phi(f)$ as

$$L(f) = 10\log\left(\frac{1}{2}\Phi^2(f)\right)$$

$$\Phi(f) = \sqrt{2\cdot 10^{\frac{L(f)}{10}}}. \tag{13}$$

$L(f)$ is normally represented in dBc/Hz and corresponds to what is presented in a spectrum analyzer at offset frequencies from the clock center frequency (Fig. 7).

A. Phase Noise to Jitter Conversion

From (11) $\phi(t)$ has the following relationship with jitter [7]:

$$\phi(kT_S) = 2\pi F_S \cdot \Delta t(kT_S), \tag{14}$$

which shows that the clock phase noise is the same as the clock jitter scaled by its own radian frequency, $2\pi F_S$. That is equivalent to referencing jitter to the clock period. For example, a 100 MHz clock with a jitter of 10 ps, has a phase noise of 0.00628 rad, or 0.36 deg, or 0.1% of the clock period.

In the frequency domain, where the clock phase noise is most commonly represented, it is then equal to the clock jitter scaled by $2\pi F_S$:

$$\Phi_S(f) = 2\pi F_S \cdot \Delta T(f). \tag{15}$$

To obtain the total jitter from phase noise, the phase noise scaled by $1/2\pi F_S$ is integrated over frequency in power density [1]:

$$\Delta t_{rms} = \frac{1}{2\pi F_S}\sqrt{\int_0^\infty \Phi^2(f)df} = \frac{1}{2\pi F_S}\sqrt{2\int_0^\infty 10^{L(f)/10}df}. \tag{16}$$

B. Derivation of SNR from Phase Noise

Substituting (15) in (10), we obtain the spectrum of the sampling error on a sinewave as a function of the clock phase noise:

$$V_{\text{error}}(f) = \frac{f_{\text{in}}}{F_S}\frac{A_{\text{in}}}{\sqrt{2}}\,\Phi(f-f_{\text{in}}). \tag{17}$$

As expected, it shows the phase noise spectrum scaled by the ratio of the input frequency to the clock frequency centered at the input frequency.

In order to obtain the in-band noise that will affect the SNR, (17) is integrated in power over the system passband $(F_{\min}, F_{\max})$. The resulting SNR is

$$\begin{aligned} SNR_J &= 10\log\left(\frac{A_{\text{in}}^2/2}{\int_{F_{\min}}^{F_{\max}} V_{\text{error}}^2(f)df}\right) \\ &= -20\log\left(\frac{f_{\text{in}}}{F_S}\sqrt{\int_{F_{\min}}^{F_{\max}} 10^{L(f-f_{\text{in}})/10}df}\right). \end{aligned} \tag{18}$$

Notice that there is no factor 2 because the integration is over both sidebands of $L(f)$ $-F_{\min}$ can be lower than F_{in}.

[1] In fact we are abusing language a little by using spectral representations. Since these are random variables, phase noise and jitter can only be expressed in power spectral density. We are further abusively assuming that $\Phi(f)$ is real. The power spectral density should be expressed as $\Phi^*(f)\cdot\Phi^*(f)$ instead of $\Phi^2(f)$.

In Section 7 this equation will be illustrated with several practical examples. But before, let's get some more insight into phase noise in typical clock sources.

VI. Phase Noise of Oscillators and PLLs

A. Oscillator Phase Noise

The phase noise of an oscillator is composed of two main regions as illustrated by Fig. 8. The larger region is due to thermal noise that has an effect like frequency modulation and therefore generates sidebands falling inversely proportional with frequency offset. In a log plot, they result in a slope of −20 dB/dec. At low frequency offsets, there is a region with a slope of −30 dB/dec due to upconversion of $1/f$ noise. The corner frequency between the two regions, f_{kp}, is at a lower frequency than the $1/f$ noise corner frequency, and dependent on the oscillator implementation [8], [9].

The flat curve is the amplitude noise of the oscillator. Contributions for the amplitude noise come mainly from buffers in the signal path, the oscillator itself has very low amplitude noise due to its own mechanisms for amplitude stabilization.

When observing the oscillator output in a spectrum analyzer, the resulting curve is the combination of both noises, as illustrated by the dashed curve.

Total Noise and Jitter

From (16), jitter is the integral of this curve from zero to infinite, divided by the clock frequency. But the total integrated noise or jitter with such a curve is infinite, which obviously cannot correspond to practical cases. At high frequency offsets, the flat amplitude noise rolls off at the system bandwidth.

At low frequencies, the integration is also unbounded due to the $1/f^2$ slope, and more so with the $1/f$ noise generating a $1/f^3$ slope. This reflects the effect of the oscillator frequency drifting with time due to noise. In fact, the phase will diverge without limit when the frequency drifts off. It is similar to the popular random-walk process that generates unbounded trajectories.

In practical situations, the jitter is defined relative to the observation period, taking the average clock frequency as the reference to measure the jitter against. That is equivalent to applying a highpass transfer function to the phase noise spectrum with cut-off frequency equal to the inverse of the averaging period used. In actual applications this limit is related to the signal processing being done. For example, in telecommunications, this lower limit often corresponds to the symbol rate. In audio, it corresponds to 20 Hz, the lower limit of human audibility. And in video it corresponds to the horizontal refresh rate because the signal is synchronized at the beginning of each horizontal frame.

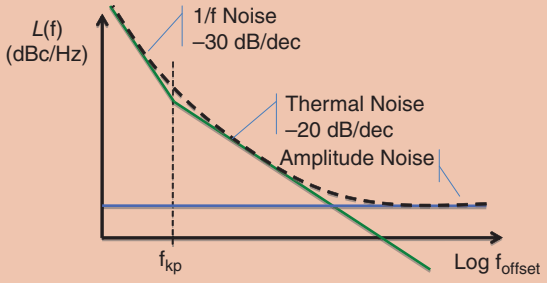

Figure 8. Phase noise of an oscillator.

B. PLL Phase Noise

A PLL, see Fig. 9, behaves as a lowpass filter for the phase noise of the input clock reference and as a highpass filter for that of the locked VCO. Most common implementations have a second order transfer function [10]. In the case of the input clock reference, the PLL also applies a gain, M, equal to the ratio of output frequency to input frequency. Considering $\Phi_{\text{in}}(f)$ the phase noise of the input clock reference and $\Phi_{VCO}(f)$ the phase noise of the locked VCO, the output phase noise is given by:

$$\Phi_{\text{out}}(f) = \frac{M}{\sqrt{1+\dfrac{f}{F_{\text{Loop}}}}}\Phi_{\text{in}}(f) + \sqrt{1+\frac{f}{F_{\text{Loop}}}}\,\Phi_{VCO}(f). \quad (19)$$

Typically, the input clock comes from a crystal oscillator and consequently, has very low phase noise, even after amplification by *M*. It will impact the output phase noise only at very low offset frequencies.

The locked VCO phase noise is often relatively large, especially if it is built as a ring oscillator. And most of its energy is at low frequencies, as illustrated in Fig. 8. The highpass transfer function of the PLL is therefore very convenient and effectively improves substantially the overall phase noise performance.

The PLL internal blocks, specially the phase detector, generate additional noise that is transferred to the

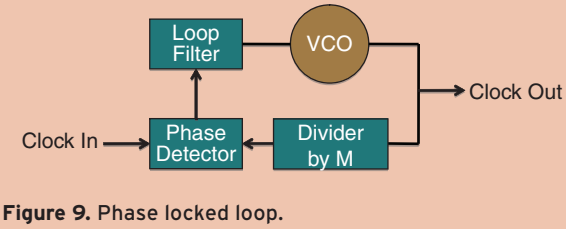

Figure 9. Phase locked loop.

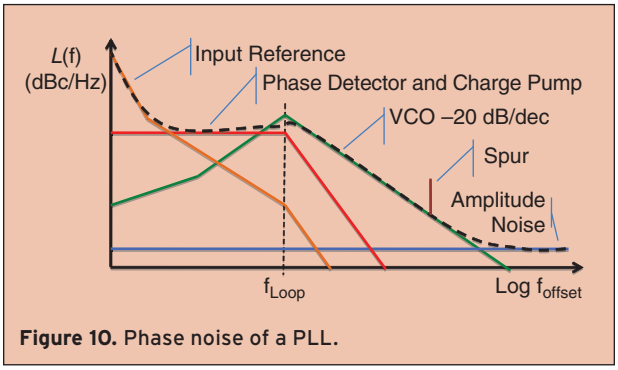

Figure 10. Phase noise of a PLL.

output with a lowpass transfer function similar to the input clock reference.

The resulting phase noise spectrum at the output is illustrated in Fig. 10. The curve for the locked VCO phase noise gets filtered down by a steep 40 dB/dec slope below the PLL loop bandwidth. Therefore, its −20 dB/dec slope is bent downward below f_{Loop}. Even the $1/f$ region is bent-down by the loop filter action.

The phase noise of the input reference clock is relevant only at very low offset frequencies.

The phase-detector and charge-pump noise may become the dominant phase noise contribution below the PLL loop bandwidth.

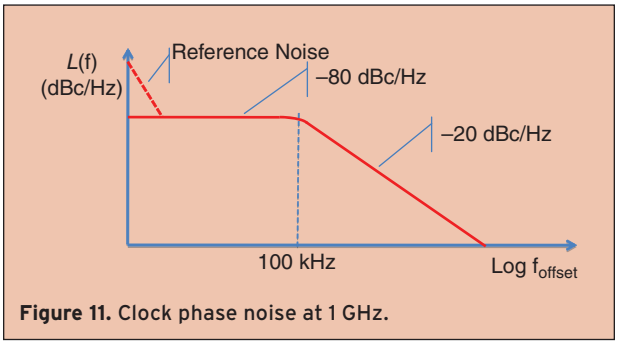

Figure 11. Clock phase noise at 1 GHz.

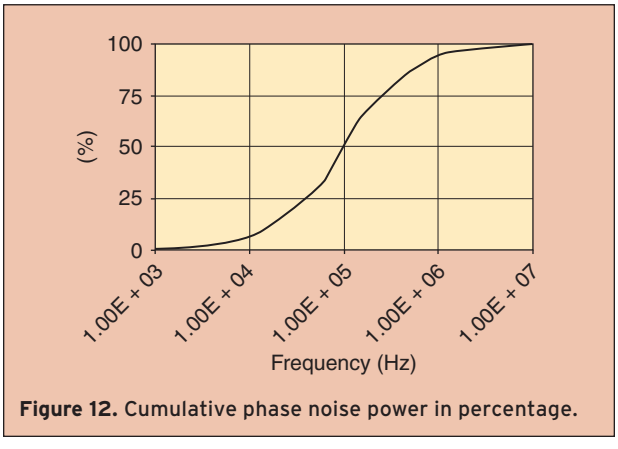

Figure 12. Cumulative phase noise power in percentage.

At high offset frequencies the amplitude noise dominates and generates a flat region visible on a spectrum analyzer plot.

The dashed curve shows the combined spectrum at the output of a PLL and can be compared with Fig. 7 that shows an actual measurement.

An oscillator also picks up noise from the supplies or the substrate. This noise is typically generated by the actual activity in the chip and can show up as spurs on the phase noise spectrum. An example is illustrated in Fig. 10 by the vertical line.

VII. Application Examples

In the following, several application examples will be studied. The master clock will be assumed to be produced by a PLL and have the phase noise spectrum as in Fig. 11 for a clock frequency of 1 GHz. For simplicity the noise density is flat within the band, corresponding to a situation of similar noise contributions by the VCO and the phase-detector/charge-pump. We neglect the reference clock phase noise (dashed line on the low frequency corner) because in many cases it is below the slowest relevant signal rates.

Integrating the area of the solid curve (multiplied by 2 for double-sideband) gives the total phase noise power. Taking the square root gives the rms phase noise:

$$\phi_{\text{Total}} = \sqrt{2\int_0^{\infty} \frac{10^{-80/10}}{1+\left(\frac{f}{100\cdot 10^3}\right)^2}\,df} = 0.056 \text{ rad rms.} \quad (20)$$

Jitter is then

$$\Delta t_{rms} = \frac{1}{\omega_S}\phi_{\text{Total}} = \frac{0.056}{2\pi 10^9} = 8.9 \text{ ps rms.} \quad (21)$$

Fig. 12 plots the cumulative noise power as a percentage of the total along frequency. It shows that half the phase noise power is within the loop band (100 kHz). And most of the remaining noise is still below 1 MHz. In the case of a phase noise spectrum mostly dominated by VCO noise, as in Fig. 7, the phase noise energy would be concentrated at the loop band corner frequency.

A. Sampling of Generic Sinusoidal Signals

Let's assume an ADC sampled at 100 MHz. We need to divide the 1 GHz master clock, generated with the PLL described above, by a factor of 10, see Fig. 13. This divider will add some flat phase noise as the horizontal line in Fig. 10. But we assume this is low enough so that we can neglect it. Let's further assume that the input signal bandwidth is limited at 25 MHz and a digital filter after the ADC removes all energy above that.

The 100 MHz clock will have the same jitter as the 1 GHz master clock. And its phase noise will have the same spectrum shape but scaled down by 10, or shifted down by 20 dB, resulting in a total phase noise of 0.0056 rad rms.

The worst case input signal is a sinewave with an amplitude equal to the ADC input range at a frequency just enough below 25 MHz such that most of the phase noise still stays within the passband of the digital filter. Let's then assume it is 24 MHz.

Using (18) we can now obtain the SNR limitation due to jitter:

$$SNR_J = -20\log\left(\frac{f_{\text{in}}}{F_s}\sqrt{\int_0^{25\text{ MHz}} 10^{L_{F_s}(f-f_{\text{in}})}df}\right)$$

$$= -20\log\left(\frac{f_{\text{in}}}{\frac{1}{10}F_{MCk}}\sqrt{\int_0^{25\text{ MHz}} \frac{1}{10}10^{L_{MCk}(f-f_{\text{in}})}df}\right),$$

where F_S is the actual sampling frequency, 100 MHz, equal to the master clock divided by 10. And the corresponding phase noise, L_{Fs}, is equal to the master clock phase noise scaled down by the same factor 10. The end result is the same as using the master clock phase noise and assuming 1 GHz for F_S, because the division factors cancel in the numerator with the denominator. It is independent of the actual sampling frequency. The SNR limitation due to jitter is only a function of the master clock phase noise and of the ratio of its frequency to the input signal frequency[2].

In this example, the integral limits include most of the phase noise energy because of the choice of signal frequency just enough below the passband limit.

We can then use the total phase noise of the master clock obtained in (20) and scale it by the ratio of the input frequency to the masterclock frequency:

$$SNR_J = -20\log\left(\frac{24\text{ MHz}}{1\text{ GHz}}0.056\,\text{rad}\right) = 57.4\text{ dB}. \quad (22)$$

In the situation that the maximum signal amplitude has some headroom below the ADC input range, this headroom would have to be added to the result. For example, in radio equipment some headroom margin must be allowed to allow for sudden changes in signal strength at the antenna that are not immediately compensated by the automatic gain control (AGC). Assuming such headroom to be 10 dB, the SNR limitation due to jitter on this ADC would be 67.4 dB.

[2] Or, using (21), it is a function of the master clock jitter and the input frequency solely.

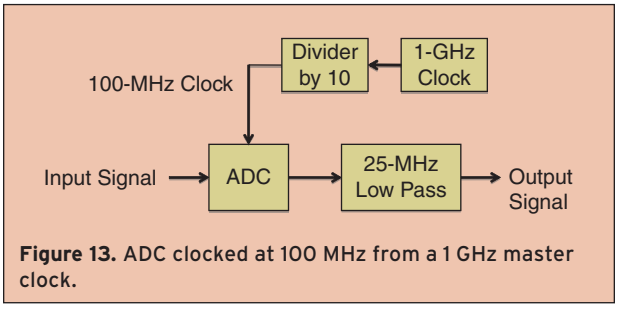

Figure 13. ADC clocked at 100 MHz from a 1 GHz master clock.

Key points:

1) The actual sampling frequency is not relevant. What is relevant is the master clock phase noise and its frequency ratio to the signal.
2) The worst-case situation is a maximum amplitude sinewave just enough below the passband limit so that most of the convoluted phase noise is in-band.
3) Any headroom will directly improve the SNR result.

B. Sub-Sampling

Some applications, such as direct IF sampling, use subsampling operation. In this situation the input signal is near one of the clock harmonics and after sampling it is shifted to baseband by aliasing.

For example, let's assume an input signal frequency of 302 MHz. After sampling it gets shifted to 2 MHz due to aliasing with the 3rd clock harmonic, see Fig. 14.
The resulting SNR limitation is now:

$$SNR_J = -20\log\left(\frac{302\text{ MHz}}{1\text{ GHz}}0.056\,\text{rad}\right) = 35.4\text{ dB}. \quad (23)$$

This clearly shows that systems operating in subsampling require very clean clock sources. In fact, the requirement is directly related to the input signal frequency and it is independent of the actual sampling frequency.

C. Interferer Situation

Let's now consider a situation in which the in-band received signal is very weak. For example, it is 60 dB below the ADC input range. The passband is the same 25 MHz.

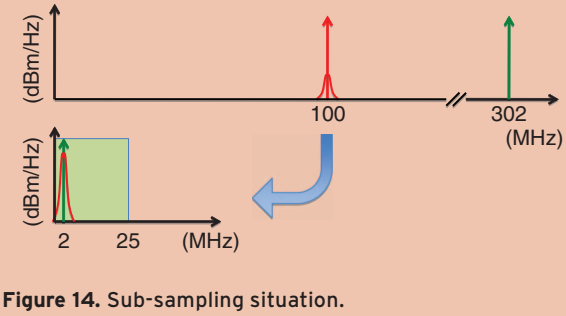

Figure 14. Sub-sampling situation.

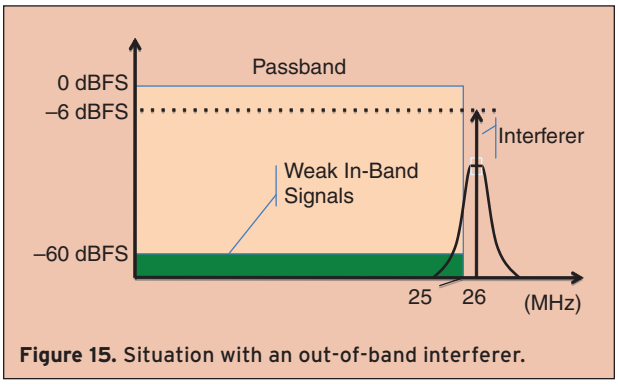

Figure 15. Situation with an out-of-band interferer.

But there are strong interferer signals out-of-band. These interferer signals can be as strong as −6 dBFS, meaning that there is 6 dB headroom to the ADC input range. Let's further assume that the closest interferer to the passband is at 26 MHz, see Fig. 15.

After the ADC this interferer is completely removed by the digital lowpass filter. But due to the phase noise convolution process, some of the sampling noise will fall in-band and will affect SNR. More specifically, the phase noise above 1 MHz offset frequency on the lower sideband. Integrating $L(f)$ for offset frequencies above 1 MHz:

$$\phi_{1\text{ MHz}} = \sqrt{\int_{10^6}^{\infty} \frac{10^{-80/10}}{1+\left(\frac{f}{100\cdot 10^3}\right)^2}\,df} = 0.01 \text{ rad rms.} \quad (24)$$

Note that this time there is no multiplication by two because only one sideband contributes.

The resulting SNR limitation, already including 6 dB for the headroom, is then:

$$SNR_J = -20\log\left(\frac{26\text{ MHz}}{1\text{ GHz}}\,0.01\text{ rad}\right) + 6 = 78\text{ dB}, \quad (25)$$

which results on a SNR on the weak input signal of just 18 dB.

D. OFDM Modulated Signals

In telecommunications, many systems use modulation techniques that generate a broad flat spectrum. An example is OFDM, consisting of multiple sub-bands (often above 1000 sub-bands) tightly packed side-by-side such that they fill completely the available channel band. Therefore, these systems are very efficient in band occupation. And they are also very robust to interference because only the sub-band masked by the interferer is lost and it is easily recovered by forward error correction. Similarly for multipath nulls. Examples of systems using OFDM are WLAN, WIMAX, Digital TV, UMTS and LTE.

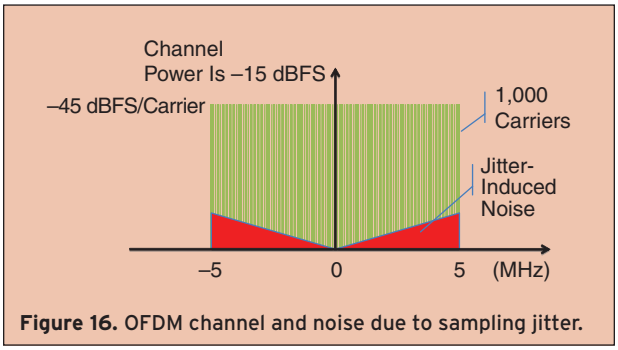

Figure 16. OFDM channel and noise due to sampling jitter.

Such a system is not straightforward to analyze for the effect of jitter on the sampling clock, because there is no single sinewave carrier to convolve with the clock phase noise. Instead, it is a multi-carrier signal, one carrier for each sub-band.

One characteristic of OFDM modulation is its large peak-to-rms ratio, or crest factor – typically 15 dB. That means that it needs relatively large headroom from the ADC input range. The SNR derivations used a sinewave that has a peak-to-average ratio of 3 dB. Therefore, additional headroom of 12 dB must be considered for such OFDM modulated signals.

Phase noise at frequency offsets below the carrier separation produce a common rotation to all the carriers and can be compensated with signal processing. That is why some pilot tones are normally included in the constellation. Therefore, only the phase noise at offset frequencies above the carrier separation is relevant.

For simplicity, we can consider an OFDM signal as multiple sinewaves, one for each carrier. Let's assume 1000 sub-bands in a 10 MHz channel at baseband (between −5 MHz and +5 MHz). The power of each carrier is 1/1000th of the signal power (−30 dB) because they are uncorrelated with each other. And the signal power is 15 dB below the ADC input range. Therefore, each carrier is at −45 dBFS. This is illustrated in Fig 16. Let's further assume that for proper demodulation of this signal the SNR must be better that 35 dB (enough for QAM-256 on each carrier).

The clock phase noise will be convolved with each carrier scaled by the carrier frequency. Normally, the carriers' separation is small and below the PLL loop bandwidth. And the channel width is much larger than the PLL bandwidth.

Then, assuming a clock phase noise spectrum like in Fig. 11, most of the convolved noise energy for each carrier stays within the channel, scaled by the carrier frequency from 0 to 5 MHz. The average noise power per carrier occurs for the carrier at 5 MHz / $\sqrt{3}$ = 2.88 MHz[3]. Adding over the 1000 carriers cancels with the −30 dB factor of the carrier power.

[3] Calculated as $\sqrt{(\int_0^{5\text{ MHz}} f^2\,df)/(5\text{ MHz})} = (5\text{ MHz})/(\sqrt{3})$. This is valid also for any uniform rectangular power spectrum signals, not only multi-carrier based.

The SNR limitation due to jitter is, then, given by:

$$SNR_J = -20\log\left(\frac{2.89\ \text{MHz}}{1\ \text{GHz}}0.056\ \text{rad}\right) + 12 = 88\ \text{dB}. \quad (26)$$

Two conclusions are evident. One is that the SNR is independent of the number of carriers. Second, the resulting SNR is much above the required 35 dB, showing that OFDM modulation is very robust to sampling jitter, being limited instead by nearby interferer situations as described above.

E. Broadband Phase Noise

Imagine a situation in which the clock signal is routed through a large digital core with insufficient isolation precautions. This can happen in a large SOC with not careful enough planning of the clock distribution. Then, the clock signal will be corrupted with broadband noise from the several gates crossed, crosstalk from neighboring lines and supply/substrate noise. The bandwidth of this noise extends well above the clock frequency as seen in Fig. 17, limited by the digital gates speed. After sampling, the high frequency components of the phase noise fold back into the Nyquist band 0-to-F_S due to aliasing and can become the dominant source of phase noise compared with the low frequency components.

In our example system, only the band from 0 to 25 MHz will be captured due to the digital lowpass filter following the ADC, as shown by the box in Fig. 17. Therefore, half the broadband noise is removed due to the oversampling used in this ADC. In Sigma-delta ADCs, the oversampling is much higher, of the order of 100. In these systems, the robustness of the ADC to broadband phase noise is very good because about 99% of the noise is removed in the decimating digital filters.

F. Clock Divider

We concluded before that by dividing, the phase noise is simply affected by the division factor (assuming the divider is ideal and adds no noise).

However, that does not include the effect of aliasing. In fact, the noise above the divided clock frequency is aliased and it is folded down. Therefore, the high frequency flat portion of the phase noise (flat line in Fig. 18) is scaled with the square root of the division ratio.

VIII. Clock Spurs

Spurs like the vertical line in Fig. 10 represent deterministic jitter. They can arise through many possible mechanisms. If the loop filter of a PLL is improperly designed, a residual leakage of the reference input clock appears on the VCO control voltage, generating a frequency modulation of the output clock. That results in spurs on both sides of the clock with frequency offsets equal to the reference input clock frequency. Additionally, any spurs on the supply or substrate easily leak into the clock distribution network, modulating the phase and appearing as dual spurs on the phase noise plot, one at each side of the clock frequency. These are very difficult to track and correct on a large SOC, even with very good isolation practices.

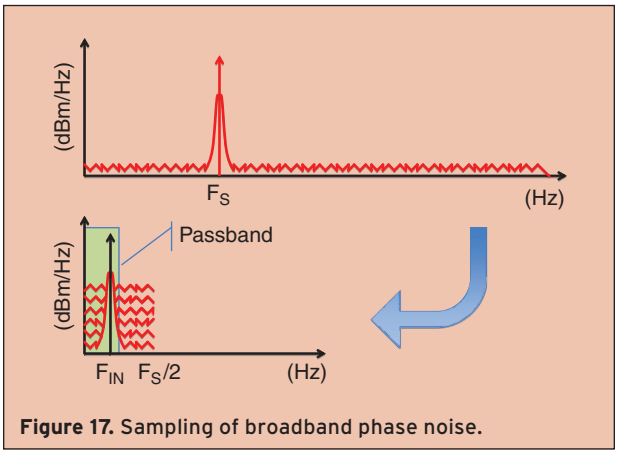

Figure 17. Sampling of broadband phase noise.

Often, clock spurs have insufficient energy to significantly contribute to the total phase noise or SNR of the sampled signal. But the corresponding spurs on the sampled signal can limit the resulting SFDR performance of a system. Modern systems are very sensitive to SFDR because this parameter determines the systems ability to resolve weak signals in a crowded spectrum with unwanted and strong nearby interferers.

Spurs on the clock phase noise spectrum are transferred to the sampled signal by the same mechanism as phase noise [4], [11]. They are convolved with the signal and scaled by the ratio of the signal frequency to the clock frequency.

For example, let's assume a 100 MHz clock with a spur at ±1 MHz offset with amplitude −50 dBc, and an input sinewave of 20 MHz. The spurs on the sampled signal would be at 19 and 21 MHz and with amplitude −64 dBc.

In many cases, the spurs are at quite large frequency offsets. In these cases, they normally generate spurs on the sampled signal outside the signal band. Then, these spurs may either:

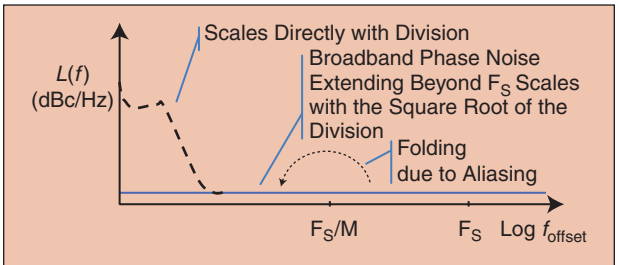

Figure 18. Phase noise scaling with clock division.

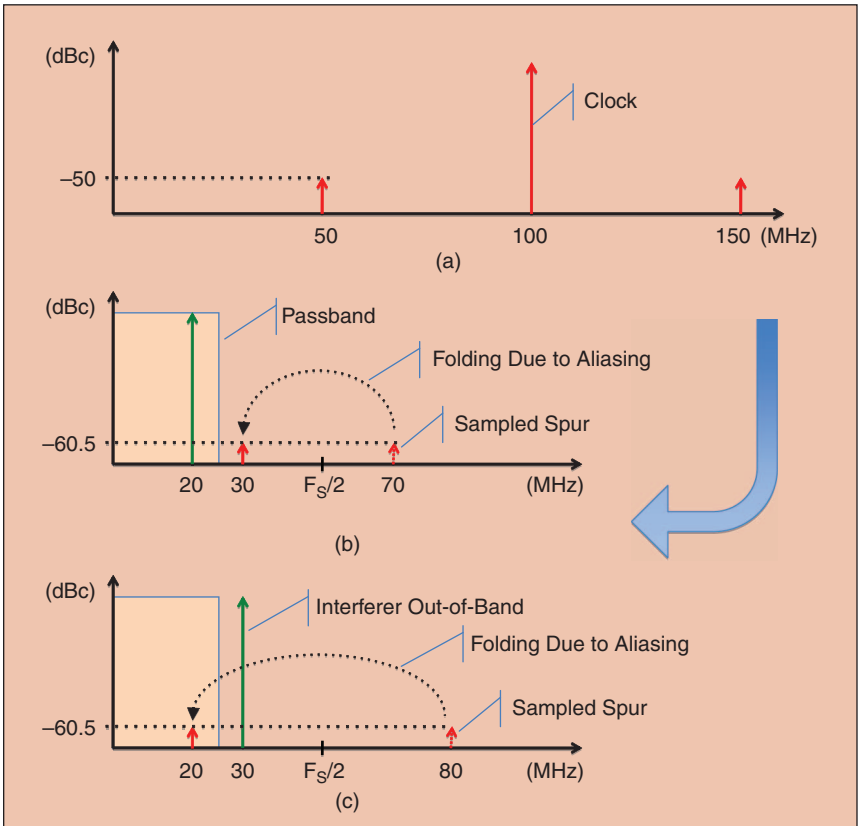

Figure 19. Examples of spurs aliasing.

1) Fold down into the signal band due to aliasing
2) Get removed by the system filters if they fall in a rejection band
3) Fall back into the signal band by sampling of an out-of-band interferer

Considering the example above but with the spurs at frequency offsets of ±50 MHz, the spur of the sampled signal would fall in the aliasing band at 70 MHz. It would then be folded down to 30 MHz, see Fig. 19b.

Now, if the system included a 25 MHz lowpass filter after the ADC, the above spur would fall outside its passband and would then be removed.

But if there was an interferer at 30 MHz, it would generate a spur at 80 MHz that would fall back in band at 20 MHz due to aliasing, see Fig. 19c.

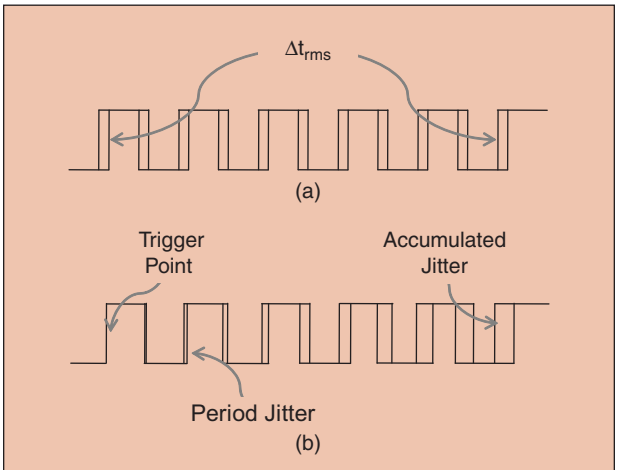

Figure 20. Measurement of accumulated jitter: (a) clock with jitter and (b) clock triggered on an edge showing the accumulated jitter with time.

IX. Jitter Measurement

It is quite difficult to measure jitter directly. The jitter definition is the time error of the clock edges relative to the ideal position. But how to know the ideal position? Normally, the jitter-free clock signal is not available.

In practice, a self-referenced measurement is often used [12], [13]. Different definitions exist.

The jitter itself is also denoted tracking jitter, timing jitter or absolute jitter. We will now proceed to relate it to the self-referenced measurements.

A. Period Jitter

Period jitter, also known as edge-to-edge or cycle-to-cycle jitter[4], is the variation of the clock period. It can be easily measured on an oscilloscope triggering on one rising edge of the clock and looking at the time variations of the next rising edge.

This measurement gives an important specification for digital circuits timing, because it shows the time available for the signals settling within a clock period.

Analytically, it is the discrete time difference of jitter:

$$\Delta t_{\text{Period}}(kT) = \Delta t(kT) - \Delta t((k-1)T) \qquad (27)$$

corresponding to a transfer function $(1-z^{-1})$, or $2\sin(\pi f/F_s)$ in the frequency domain.

It can then be related to phase noise as:

$$\Delta t_{\text{Period}} = \frac{1}{2\pi F_S}\sqrt{\int_0^\infty 2\cdot 10^{\frac{L(f)}{10}}\left(2\sin\left(\frac{\pi f}{F_S}\right)\right)^2 df}. \qquad (28)$$

[4] The term cycle-to-cycle jitter is also sometimes used to refer adjacent period jitter, which is the difference between two consecutive periods. We will not cover this definition in this work.

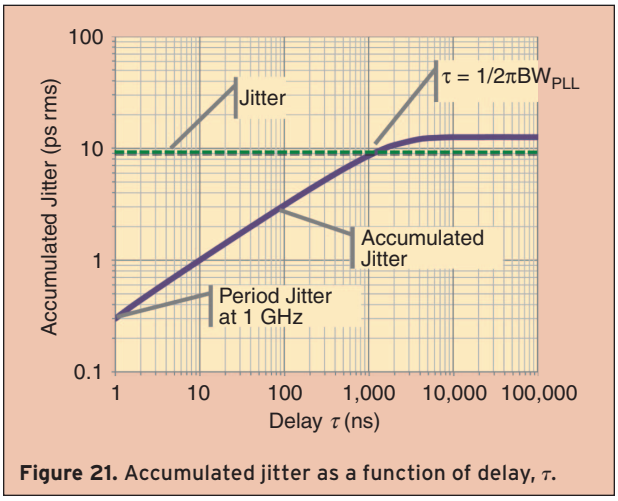

Figure 21. Accumulated jitter as a function of delay, τ.

B. Accumulated Jitter

Accumulated jitter is similarly measured as period jitter, but taking a later clock edge (Fig. 20). It is a function of the number of clock periods between the triggered edge and the measurement edge.

Analytically, it is also a discrete time difference of jitter:

$$\Delta t_{Acc}(kT, M) = \Delta t(kT) - \Delta t((k-M)T) \qquad (29)$$

corresponding to a transfer function $(1-z^{-M})$, or $2\sin(\pi f MT_s)$ in the frequency domain.

It can then be related to phase noise as:

$$\Delta t_{Acc}(\tau) = \frac{1}{2\pi F_S}\sqrt{\int_0^\infty 2\cdot 10^{\frac{L(f)}{10}}(2\sin(\pi f\tau))^2 df}, \qquad (30)$$

where $\tau = MT_S$.

Fig. 21 shows the accumulated jitter as a function of τ, assuming the phase noise of Fig. 11, on the 1 GHz clock.

The accumulated jitter increases with τ, starting at 0.3 ps_{rms} for $t = 1$ ns (the clock period). It stabilizes for large τ at 12.6 ps_{rms}, which is $\sqrt{2}\,\Delta t_{rms}$. This is expected because at large τ, there is no correlation between the jitter on both edges and the jitter is added in variance [14]. Another interesting observation is that the start of the curve stabilization is for τ around the value of the PLL loop time constant $(1/2\pi BW_{PLL})$. This observation shows that a good estimation of jitter is to measure the accumulated jitter for longer than the loop time constant, and divide it by $\sqrt{2}$.

X. Conclusions

Jitter is a critical specification for accurate and fast data converters. Not only is the total jitter of relevance, but also its spectrum distribution needs consideration. Clocks from open loop oscillators and from phase locked loops have quite different jitter spectrum characteristics. Some application examples were used to demonstrate situations of sub-sampling, presence of out-of-band interferers, broadband signals, broadband jitter and spurs. Jitter is often measured by self-referenced methodologies, which must be carefully interpreted to obtain the actual jitter value affecting sampling.

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