Circuit Theory in Circuit Simulation

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Abstract

This paper stresses the importance of applying circuit theory in circuit simulation. Circuit simulation is a combination of circuit theory and numerical analysis. Both the theoretical basis and the numerical algorithms should be robust and accurate to produce reliable and correct results. This communication focuses on the theoretical and practical aspects of circuit equation formulation in the simulation of circuits containing nanodevices.

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I. Introduction

Professor Ernie Kuh was one of the giants in circuit theory. His book with Charles Desoer [1] and later with Leon Chua and Charles Desoer [2] are classic in the field of circuit theory. I first got introduced to circuit theory in a formal way when I enrolled at the University of California at Berkeley in the late sixties to study for my Ph.D. degree. Ernie was my Ph.D. advisor.

In the late sixties the number of transistors in integrated circuits was relatively small, but increasing fast. Integrated circuit designs were increasing in complexity according to Moore's Law. There was a pressing need to have a circuit simulator to help analyze integrated circuit designs before fabrication. Ron Rohrer was teaching students in his class how to write a circuit simulator based

on nodal formulation rather than on state equations. The class project evolved later to become SPICE [3].

In our first research meeting, Ernie gave me a copy of Gary Hachtel's Ph.D. thesis that listed various transistor interconnection structures that resulted in multistable circuits. I was tasked to find the theory behind multistability of these structures. That led to the theory of circuits with multiple equilibrium points, and the development of computational methods for finding these multiple solutions based on piecewise-linear approximation. Writing a computer program that worked according to the theory established my interest in computer-aided simulation and design [4].

So, what is the relationship between circuit theory and circuit simulation? Circuit theory is applied in all aspects of circuit simulation. It is used in deriving efficient algorithms for circuit equation formulation to ensure that the equations are complete and solvable. It is applied to understand the existence of solutions and circuit stability in relation to numerical stability, especially when applying integration formulas to compute time-domain solutions. Circuit theory is used in partitioning algorithms for parallel processing to ensure that the equations of partitioned subcircuits are solvable [5]. It is applied in large-change [6] and small-change sensitivity analysis, reduced-order modeling, power estimation, reliability analysis, and other applications.

The contributions of Ernie Kuh to circuit simulation are many. In addition, the list of circuit theorists who contributed to circuit simulation is long. To list their names, at the risk of missing some names, and summarize their contributions in this short paper is not possible. In this short paper the focus is on the application of circuit theory to circuit equation formulation, with special attention given to circuits containing nanodevices. Equation formulation is the first step in circuit simulation. Errors in constructing the equations will produce inaccurate results, even if the numerical methods used to solve the equations are accurate.

II. Circuit Equation Formulation

Nodal analysis is the simplest method to implement in a computer program to formulate circuit equations, provided the element characteristic equations are of the form:

$$\mathbf{i}_b = \mathbf{G}\mathbf{v}_b + \mathbf{s} \tag{1}$$

where $\mathbf{G}$ in (1) could be complex, such as in sinusoidal steady-state analysis, or real as in the case of linear resistive circuits, linearized models at an iteration point in nonlinear DC analysis, or discretized and linearized circuit models at a time point and iteration point in time-domain analysis [7]. However, equation (1) does not include current-controlled elements and voltage sources, both independent and dependent.

In 1975 Ho, Branin, and Ruehli proposed a modified nodal analysis (MNA) method by appending the nodal equations with the characteristic equations of the current-controlled elements that do not fit into nodal formulation [8]. The element characteristics are classified into two types: elements in which the currents are the dependent variables (2), and elements in which the voltages are the dependent variables (3).

$$\mathbf{i}_1 = \mathbf{G}_1\mathbf{v}_1 + \mathbf{H}_1\mathbf{i}_2 + \mathbf{s}_1 \tag{2}$$

$$\mathbf{v}_2 = \mathbf{H}_2\mathbf{v}_1 + \mathbf{Z}_2\mathbf{i}_2 + \mathbf{s}_2 \tag{3}$$

$$\text{where} \quad \mathbf{i}_b = \begin{bmatrix}\mathbf{i}_1\\ \mathbf{i}_2\end{bmatrix}, \quad \mathbf{v}_b = \begin{bmatrix}\mathbf{v}_1\\ \mathbf{v}_2\end{bmatrix}$$

The MNA formulation method is used in current versions SPICE and its derivatives. Although the MNA formulation method is more general than nodal formulation, it does not accommodate all possible circuit element models. Ideal mem-devices [9] and mem-systems [10], which contain internal device variables, cannot be readily incorporated into the MNA formulation without transforming the characteristic equations into functions of only terminal voltages and currents that SPICE accepts. For example, in modeling the memristor for SPICE circuit simulation, the differential operator is modeled as a capacitor driven by a controlled source [11]. In modeling field-effect transistors (FETs), the surface-potential, which is an internal device variable that is nonlinearly dependent on the terminal voltages, is eliminated using analytical or numerical techniques to obtain a circuit model in terms of terminal currents and voltages only [12], [13]. In modeling carbon-nanotube [14] and graphene nano-ribbon FETs [15], additional circuitry is introduced to solve for the surface-potential, which is then coupled to the main device model by adding a voltage-controlled voltage source. The added controlled source adds an extra terminal to the original device, which introduces errors in the KCL equations. In addition, multiterminal device charge equations are modeled as interconnections of two-terminal capacitors, which ignores the capacitive coupling within the device. Moreover, the added circuitry in the circuit device models may result in overestimating the power computation in the device.

To accommodate such general characteristics, the MNA formulation method has been extended to

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incorporate general models that include variables other than voltages and currents [16]. The extended formulation is referred to as the Extended Nodal Analysis (ENA) formulation method. The element characteristics in ENA are assumed to be of the form:

$$\mathbf{i}_1 = \mathbf{G}_1\mathbf{v}_1 + \mathbf{H}_1\mathbf{i}_2 + \mathbf{N}_1\mathbf{z} + \mathbf{s}_1 \tag{4}$$

$$\mathbf{M}_2\mathbf{v}_2 = \mathbf{H}_2\mathbf{v}_1 + \mathbf{Z}_2\mathbf{i}_2 + \mathbf{N}_2\mathbf{z} + \mathbf{s}_2 \tag{5}$$

where $\mathbf{z}$ includes variables other than terminal currents and voltages, such as charge, flux, temperature, and any other internal physical parameters, such as the surface potential in FET models [12], the thickness of the doped region in memristors [17], the concentrations of potassium and sodium in the model of a neuron [18]. These internal variables are usually functions of voltages and currents in the circuit.

Earlier in 1971 G. D. Hachtel, R. K. Brayton and F. G. Gustavson proposed the Tableau approach to circuit equation formulation [19]. The tableau equations allow all types of elements without restrictions, but the resulting equations are very large compared to the number of equations in nodal, MNA and ENA formulation methods. The nodal, MNA and ENA equations can be derived from the tableau equations as follows. The Tableau equations consist of *topological equations*, KCL (6) and KVL (7):

$$\text{(KCL)}\quad \mathbf{A}\mathbf{i}_b = \mathbf{0} \tag{6}$$

$$\text{(KVL)}\quad \mathbf{v}_b = \mathbf{A}^{\mathrm{T}}\mathbf{v}_n \tag{7}$$

together with the *element characteristics* (4) and (5).

Partitioning the incidence matrix $\mathbf{A}$ according to the partition in the element characteristics shown in (4) and (5), one gets:

$$\text{KCL}\quad [\mathbf{A}_1\ \ \mathbf{A}_2]\begin{bmatrix}\mathbf{i}_1\\ \mathbf{i}_2\end{bmatrix} = \mathbf{0} \tag{8}$$

$$\text{KVL}\quad \begin{bmatrix}\mathbf{v}_1\\ \mathbf{v}_2\end{bmatrix} = \begin{bmatrix}\mathbf{A}_1^T\\ \mathbf{A}_2^T\end{bmatrix}\mathbf{v}_n \tag{9}$$

Eliminating $\mathbf{v}_1$, $\mathbf{v}_2$, and $\mathbf{i}_1$ in the Tableau Equations, one gets:

$$\begin{bmatrix}\mathbf{A}_1\mathbf{G}_1\mathbf{A}_1^T & (\mathbf{A}_1\mathbf{H}_1 + \mathbf{A}_2) & \mathbf{A}_1\mathbf{N}_1\\ (\mathbf{M}_2\mathbf{A}_2^T - \mathbf{H}_2\mathbf{A}_1^T) & -\mathbf{Z}_2 & -\mathbf{N}_2\end{bmatrix}\begin{bmatrix}\mathbf{v}_n\\ \mathbf{i}_2\\ \mathbf{z}\end{bmatrix} = \begin{bmatrix}-\mathbf{A}_1\mathbf{s}_1\\ \mathbf{s}_2\end{bmatrix} \tag{10}$$

which are the ENA equations. Note that if $\mathbf{z}$ is empty, one gets the MNA equations. If, in addition, $\mathbf{i}_2$ is empty, one gets the nodal equations. In practice, the ENA equations in (10) are assembled one circuit element at a time using the *stamp approach*, similar to assembling the MNA and nodal equations. The equations are assembled one element at a time using a template or a stamp based on its characteristics and connectivity. The element could be two-terminal or multiterminal.

III. Examples

In the following we derive, as illustration, the stamps of an ideal memristor, a memristive system, and a compact model of a FET that fit naturally into the ENA formulation, but require modification and transformation, at the risk of introducing errors, to fit into MNA formulation.

(1) *Ideal charge-controlled memristor* [9]: The characteristic equations of a two-terminal ideal charge-controlled memristor are given by:

$$\phi_M = f(q_M),\quad i_M = dq_M/dt,\quad v_M = d\phi_M/dt \tag{11}$$

Applying the Backward Euler (B.E.) formula [19] to the differential operators in (11), one gets

$$i_{M,n} = \frac{1}{h}(q_{M,n} - q_{M,n-1}) \tag{12}$$

$$v_{M,n} = \frac{1}{h}(\phi_{M,n} - \phi_{M,n-1}) \tag{13}$$

Substituting $\phi_M(t) = f_M(q_M)$ in (13), assuming $f_M(q_M)$ is differentiable at $q_{M,n}^{(k)}$, and linearizing at $q_{M,n}^{(k)}$, one gets

$$v_{M,n} = \frac{1}{h}(a_n^{(k)}q_{M,n} + b_n^{(k)} - \phi_{M,n-1}) \tag{14}$$

where $a_n^{(k)} = df_M/dq_M$ is evaluated at $q_{M,n}^{(k)}$, and $b_n^{(k)} = f_M(q_{M,n}^{(k)}) - a_n^{(k)}q_{M,n}^{(k)}$. Equations (12) and (14) constitute the linearized companion model of the charge-controlled ideal memristor. The corresponding stamp is shown in (15). Note that ENA formulation is used and q_M is declared as a circuit variable.

$$\begin{bmatrix} \vdots & \vdots & +\frac{1}{h}\\ \vdots & \vdots & -\frac{1}{h}\\ +1 & -1 & -\frac{a_n^{(k)}}{h}\end{bmatrix}\begin{bmatrix}v_{n_1}\\ v_{n_2}\\ q_M\end{bmatrix},\quad \begin{bmatrix}+\frac{q_{M,n-1}}{h}\\ -\frac{q_{M,n-1}}{h}\\ \frac{b_n^{(k)} - \phi_{M,n-1}}{h}\end{bmatrix} \tag{15}$$

Integration formulas other than the B.E. formula [21] can also be applied to derive a stamp.

(2) *Voltage-controlled memristive system* [10]: Consider a 2-terminal voltage-controlled memristive system connected between nodes n_1 and n_2 with characteristic equations given in (16) and (17), and with scalar x.

$$i_M(t) = G_M(v_M, x, t)\,v_M(t) \tag{16}$$

$$\dot{x} = f_2(v_M, x, t) \tag{17}$$

It is assumed that $G_M(v_M, x, t)$ in (16) is a nonlinear conductance function, which is the derivative of a nonlinear function relating i_M and v_M. Applying the B.E. formula to $\dot{x}$ in (17), one gets

$$\frac{1}{h}(x_n - x_{n-1}) = f_2(v_{M,n}, x_n, t_n) \tag{18}$$

Assuming that Newton method is applied to compute $v_{M,n}$, $i_{M,n}$, and x_n at t_n, and $f_2(x, i_M, t)$ is differentiable at $v_{M,n}^{(k)}$ and $x_n^{(k)}$, and linearizing (18) at $v_{M,n}^{(k)}$ and $x_n^{(k)}$, one gets:

$$\begin{aligned} i_{M,n} &= a_{11}^{(k)} v_{M,n} \\ \frac{1}{h}(x_n - x_{n-1}) &= a_{21}^{(k)} v_{M,n} + a_{22}^{(k)} x_n + s_2^{(k)} \end{aligned}$$

where $a_{11}^{(k)} = G_M(v_{M,n}^{(k)}, x_n^{(k)}, t_n)$, $a_{21}^{(k)} = \partial f_2/\partial v_M$, $a_{22}^{(k)} = \partial f_2/\partial x$, where $\partial f_2/\partial v_M$ and $\partial f_2/\partial x$ are evaluated at $v_{M,n}^{(k)}$ and $x_n^{(k)}$, and $s_2^{(k)} = f_2(v_{M,n}^{(k)}, x_n^{(k)}, t_n) - a_{21}^{(k)} v_{M,n}^{(k)} - a_{22}^{(k)} x_n^{(k)}$.

The corresponding stamp in an ENA formulation is given in (19).

$$\begin{bmatrix} +a_{11}^{(k)} & -a_{11}^{(k)} & \\ -a_{11}^{(k)} & +a_{11}^{(k)} & \\ +a_{21}^{(k)} & -a_{21}^{(k)} & a_{33}^{(k)} \end{bmatrix} \begin{bmatrix} v_{n_1} \\ v_{n_2} \\ x \end{bmatrix}, \begin{bmatrix} \\ \\ a_{33}^{(k)} \end{bmatrix} \tag{19}$$

where $a_{33}^{(k)} = +a_{22}^{(k)} - (1/h)$ and $a_{33}^{(k)} = -s_2^{(k)} - (1/h)\, x_{n-1}$. Note that x is declared as a circuit variable.

(3) *Compact model of a four-terminal carbon nanotube (CN) [14] or graphene nano-ribbon (GNR) FET [15]:* The characteristic equations of a CNFET or GNRFET are given as:

$$i_{DS} = f_{DS}(v_{DS}, \Psi_S) \tag{20}$$

$$q_G = C_G(v_{GS} - \Psi_S), \quad i_G = dq_G/dt \tag{21}$$

$$q_B = C_B(v_{BS} - \Psi_S), \quad i_B = dq_B/dt \tag{22}$$

$$q_D = f_D(v_{DS}, \Psi_S), \quad i_D = dq_D/dt \tag{23}$$

$$q_S = f_S(v_{DS}, \Psi_S), \quad i_S = dq_S/dt \tag{24}$$

$$q_G + q_B + q_D + q_S = 0 \tag{25}$$

where the *quantum* charge in the channel is $q_{CH} = q_D + q_S = f_{CH}(v_{DS}, \Psi_S)$. Equation (25) can be written as

$$C_G(v_{GS} - \Psi_S) + C_B(v_{BS} - \Psi_S) + f_{CH}(v_{DS}, \Psi_S) = 0 \tag{26}$$

In performing transient analysis and assuming B.E. formula is applied to (21), (22), (23), and (26) at time t_n, and linearizing the equations at iteration point $\mathbf{x}_{(n)}^{(k)}$, yields linearized equations of the form:

$$i_{DS(n)} = g_{DS}^{(k)} v_{DS(n)} + g_{\Psi}^{(k)} \Psi_{S(n)} + r_{DS}^{(k)} \tag{27}$$

$$i_{G(n)} = \frac{1}{h}[C_G(v_{GS(n)} - \Psi_{S(n)}) - q_{G(n-1)}] \tag{28}$$

$$i_{B(n)} = \frac{1}{h}[C_B(v_{BS(n)} - \Psi_{S(n)}) - q_{B(n-1)}] \tag{29}$$

$$i_{D(n)} = \frac{1}{h}[(c_D^{(k)} v_{DS(n)} + e_D^{(k)} \Psi_{S(n)} + r_{D(n)}^{(k)}) - q_{D(n-1)}] \tag{30}$$

$$i_{S(n)} = \frac{1}{h}[(c_S^{(k)} v_{DS(n)} + e_S^{(k)} \Psi_{S(n)} + r_{S(n)}^{(k)}) - q_{S(n-1)}] \tag{31}$$

$$\begin{aligned} C_G(v_{GS(n)} - \Psi_{S(n)}) + C_B(v_{BS(n)} - \Psi_{S(n)}) + c_{DS}^{(k)} v_{DS(n)} \\ + c_{\Psi}^{(k)} \Psi_{S(n)} + r_{CH}^{(k)} = 0 \end{aligned} \tag{32}$$

where the coefficients are found by linearizing the nonlinear functions at $\mathbf{x}_{(n)}^{(k)}$.

The corresponding stamp in an ENA formulation is of the form [20]:

$$\left[G + \frac{1}{h}C\right] \mathbf{v}, \mathbf{b} \tag{33}$$

where $\mathbf{v} = [v_G, v_B, v_D, v_S, \Psi_S]$, and

$$\mathrm{G} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & +g_{DS}^{(k)} & -g_{DS}^{(k)} & +g_{\Psi}^{(k)} \\ 0 & 0 & -g_{DS}^{(k)} & +g_{DS}^{(k)} & -g_{\Psi}^{(k)} \\ +C_G & +C_B & +c_{DS}^{(k)} & -d_S^{(k)} & +d_{\Psi}^{(k)} \end{bmatrix}$$

$$\mathrm{C} = \begin{bmatrix} +C_G & 0 & 0 & -C_G & -C_G \\ 0 & +C_B & 0 & -C_B & -C_B \\ 0 & 0 & +c_D^{(k)} & -c_D^{(k)} & +e_D^{(k)} \\ 0 & 0 & +c_S^{(k)} & -c_S^{(k)} & +e_S^{(k)} \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The contribution to the right-hand side vector is given by

$$\mathbf{b} = \begin{bmatrix} +\dfrac{q_{G(n-1)}}{h} \\ +\dfrac{q_{B(n-1)}}{h} \\ -r_{DS}^{(k)} + \dfrac{q_{D(n-1)}}{h} - \dfrac{r_D^{(k)}}{h} \\ +r_{DS}^{(k)} + \dfrac{q_{S(n-1)}}{h} - \dfrac{r_S^{(k)}}{h} \\ -r_{CH}^{(k)} \end{bmatrix}$$

Note that Ψ_S is declared as a circuit variable. Note also that the multiterminal nature of the charge equations is retained. Similar stamps can be derived for compact models of MOSFETS [12], including FINFETS [13].

IV. Conclusion

In summary, circuit simulation relies on circuit theory and numerical analysis. It is a combination of theory and practice. Both should be done correctly and accurately to produce reliable and trustworthy results. Ernie Kuh's many contributions to circuit theory and circuit simulation have been well documented since the 1960's. His influence exists in all circuit simulators that are in use today. In this short communication, we showed how circuit theory can be used to incorporate the complex models of devices into circuit equation simulation using the ENA formulation method that preserves the device physical parameters in the equations. This shortens the gap between device modeling and circuit simulation, and helps designers track the effects of the device internal physical parameters on circuit behavior, as well as the effects of circuit operating conditions on the device parameters. The formulation method allows electrical and nonelectrical parameters to be included in circuit simulation in a natural way.

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