Switched-Capacitor Power Electronics Circuits

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Abstract—*One of the main orientations in power electronics in the last decade has been the development of switching-mode converters without inductors and transformers. Light weight, small size and high power density are the result of using only switches and capacitors in the power stage of these converters. Thus, they serve as ideal power supplies for mobile electronic systems (e.g. cellular phones, personal digital assistants, and so forth). Switched-capacitor (SC) converters, with their large voltage conversion ratio, promise to be a response to such challenges of the 21st century as high-efficiency converters with low EMI emissions and the ability to realize steep step-down of the voltage (to 3V or even a smaller supply voltage for integrated circuits) or steep step-up of the voltage for automotive industry or internet services in the telecom industry. This paper is a tutorial of the main results in SC-converter research and design.*

Switched-Capacitor Converters—A Typical Power Electronics Contribution of the CAS Society

From all of the research subjects in the Power Systems and Power Electronics Circuits Technical Committee—the stability of power systems, analysis of power electronics circuits (which are time-variable circuits with internally-controlled switches), chaos, modeling and simulation of converters, hard-switching and soft-switching converters, and so forth—the SC-converter is probably the most pertinent contribution of the CAS Society to power electronics. In fact, most of the researchers in this field belong to our Society's technical committee and most of the breakthrough contributions on this subject have appeared in CAS publications.

The reason for this is clear. Pursuing small size filters in the 1950's, the circuit theory community found a solution in the elimination of bulky inductors from the structure of a passive filter. Active and then switched-capacitor filters showed the possibility of implementing the filtering function without using magnetic devices. The power electronics designer faced a similar challenge: the request for miniaturization of the power supply. This could be achieved only by eliminating the inductors and transformers.

In a converter, the inductor serves the two purposes of processing energy and filtering the output voltage. The use of a switched-capacitor circuit for processing energy seemed doomed to failure because it is known that charging a capacitor from zero is achieved at a 50% efficiency. Ten years of research were needed to overcome the efficiency dilemma and to develop high-efficiency switched-capacitor energy-processing circuits.

First SC Converters and Basic Principles

The primary goal of any switching-mode power converter is to provide a constant (DC or AC) output voltage at its load, despite variations in the input voltage or load. A control element, therefore, has to be introduced in the process of transmitting energy so that the converter (power stage) changes its topology cyclically, and the durations of the switching topologies are adjusted for regulation purposes.

The first SC converters were developed by a group of researchers from Kumamoto, Japan, who processed a DC unregulated voltage toward a DC regulated voltage [1, 2, 4]. These DC-DC converters were soon followed by AC-DC converters [3], DC-AC inverters [5] and AC-AC transformers [6]. By avoiding magnetic elements, these circuits, realized in a hybrid technology, featured a high power density (23W/inch^3).

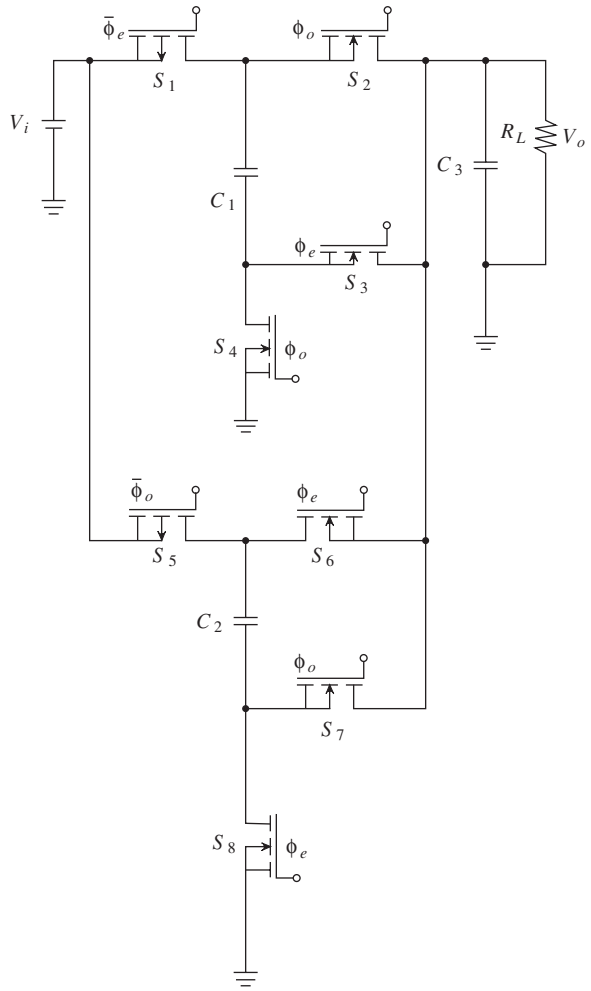

Figure 1(a). Basic SC step-down DC-DC converter.

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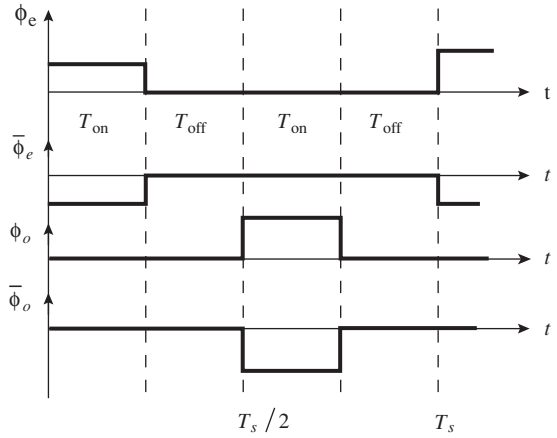

Figure 1(b). Its switching diagram.

A typical DC-DC power stage is given in Fig. 1(a); S_1 and S_5 are *p*-channel MOSFETs, the other switches are *n*-channel MOSFETs, and C_1, C_2, and C_3 are multilayer ceramic capacitors with a very low DC parasitic resistance—around 0.02 Ω for capacitances of tens of μF. The switches are operated according to the diagram of Fig. l(b). Accordingly, the converter goes through four topological stages in each switching cycle. $T_s = 1/f_s$ is the switching period, where f_s is the switching frequency. In the first topology, C_1 and C_2 are charged in series from the input voltage; concomitantly, C_2 and C_3 are discharged in parallel on the load R_L. The positions of C_1 and C_2 are inversed in the third topology. The second and the fourth topologies have a regulation role—the process of charging capacitors from the input is interrupted and a continuous output voltage is assured by capacitor C_3, which remains connected in parallel to the load. C_3, therefore, plays the role of a filter. Of course, the whole process takes place at a very high switching frequency in order to get an almost constant load voltage.

By analyzing the circuit and assuming equal capacitances C, one gets the relationship between the input and load voltages

$$V_o = \frac{V_i}{2} \cdot \frac{1}{1 + \frac{r_{on}}{2 R_L D}}$$

where r_{on} is the on-resistance of a *p*-type MOSFET in conduction, and D is called duty-ratio; in Fig. 1 (b), $D \triangleq Toff / T_s$.

Despite variation in line V_i or load R_L, the load voltage V_o can be kept constant either by controlling r_{on}, or D.

The output voltage exhibits a ripple during each switching cycle. In the first and third topology it increases from a minimum value $V_{o\,min}$ to a maximum value $V_{o\,max}$; in the even topologies, when C_3 is discharged exponentially on the load, the voltage decreases from its maximum value to its minimum one. The difference $\hat{V}_o$ between the two values results in

$$\hat{V}_o = V_{o\,min} \left(1 - \frac{1}{1 + \frac{0.5 - D}{R_L C f_s}} \right).$$

Of course, a high product (Cf_s) assures a small ripple. But for miniaturization's sake, one wants to use capacitors with low capacitance. This results in a need to operate the circuit at a very high switching frequency. The switching frequency cannot be increased as much as the technology permits, because each turn-on/off of a switch is accompanied by a switching loss, that negatively affects the efficiency.

One can operate the converter at a nominal duty-cycle close to 0.5, thus reducing the ripple. This means an r_{on}-control. From the efficiency point of view, however, it is preferable to ensure the minimum possible parasitic conduction resistance, for reducing the conduction losses, and to regulate the output voltage by means of the duty-cycle D.

As $r_{on} << R_L$, it is clear that the converter in Fig. 1 accomplishes a step-down of the input voltage; ideally, $V_o = V_i / 2$. An analogous structure has been designed for stepping-up the input voltage.

A similar principle was developed in [7] where a third control possibility was mentioned, the *p*-type MOSFET being operated as a controllable constant current source.

The first SC converters suffered from drawbacks. First, they had a limited line regulation; as $r_{on} << R_L$, changes in D had a limited influence on large changes in V_i; and so V_o almost follows V_i. Second, they showed disruptive input current; in the even-switching topologies, the input current is zero. This negatively influenced the EMI emission. Finally, a relatively large number of switches was required.

SC Converters with Improved Characteristics

In order to solve the above problems, a new configuration of the SC circuit was proposed in [8–11]; the SC block was divided into two symmetrical SC-subcircuits. For the first half-cycle the capacitors in the first SC cell are in a charging phase, and the capacitors in the second SC cell discharge on the load. The role of the two cells is interchanged in the second half-cycle.

Such a converter is shown in Fig. 2(a). It realizes a step-down function. The first SC sub-circuit is formed by C_1, C_2 (each of $47\mu F$ capacitance), S_1, S_2 (an IRF 9530 *p*-type MOSFET, and an IRF 540 *n*-type MOSFET, respectively), and D_1, D_2, and D_3 (Shottky diodes). Similar components form the

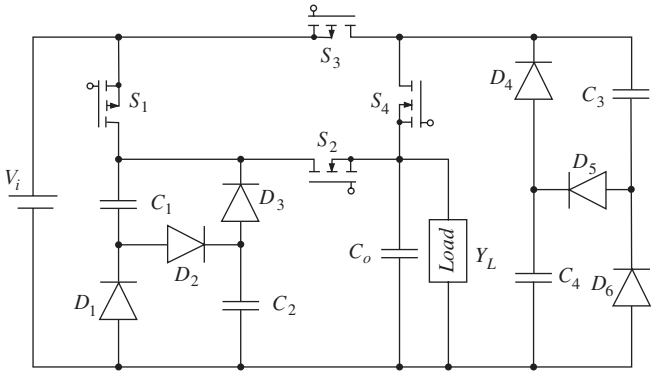

Figure 2(a). Step-down converter with two SC sub-circuits.

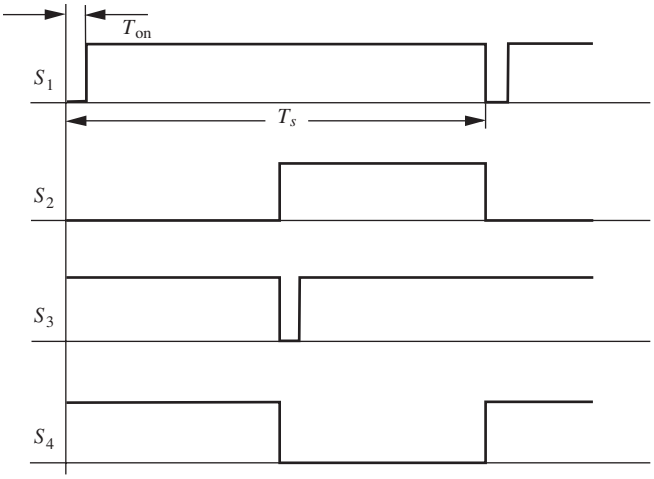

Figure 2(b). Switching diagram for Figure 2(a).

second SC sub-circuit. C_o (of 100μF capacitance) is placed all the time in parallel with the load. Its role is to minimize ripple in the load voltage. The timing diagram is given in Fig. 2(b). In the first switching topology, S_1 and S_4 are on, S_2 and S_3 are off. Capacitors C_1 and C_2 are charged in series from V_i. Due to losses in the charging circuit, the voltage on each capacitor at the end of this stage, of duration DT_s, will be a little less than $V_i / 2$. At the same time, capacitors C_3 and C_4, which were charged to almost $V_i / 2$ in the second half-cycle of the previous switching cycle, are discharged in parallel on the load. Because of losses, the voltage on the load is a little less than that on C_3 and C_4. The only difference in the second topology, of duration $T_s / 2 - DT_s$, is that S_1 is now switched-off. Thus, the charging process of C_1 and C_2 is interrupted; but C_3 and C_4 continue their discharging process on the load. If, for any reason, V_o has the tendency to drop, as for instance because of a drop in V_i, the duration of the first topology is increased, such that the voltage on capacitors at the end of the stage is the same as in the nominal case. If V_i increases over its nominal value, DT_s is reduced. For proper regulation, one needs to design D for nominal input and load such that the operating point at time DT_s is situated on the linear part of the charging characteristic of the capacitor, allowing for excursions in both directions when regulation is needed. In the third topology, S_3 and S_2 are on, S_1 and S_4 are off, and C_3 and C_4 are charged in series from V_i—the process is interrupted in the fourth topology—and C_1 and C_2 are discharged in parallel on the load—inclusive in the fourth topology. A steady-state analysis of the circuit gives

$$V_o = \frac{V_i - 3V_D}{2 + Y_L\left(\frac{1}{g_2} + \frac{1}{4g_1 D}\right)},$$

$$g_1 = \frac{1}{2r + r_1},\ g_2 = \frac{1}{2r_2 + r}$$

where V_D is the forward voltage of a diode in conduction, r is the ESR of a capacitor, and r_1 and r_2 are the on-resistances of the p-type and n-type transistors, respectively. The circuit is operated at $f_s = 87KHz$. Ideally, $V_o = V_i / 2$. It was designed for a 12 / 5 V converter of 12.5 W. If one requires another voltage ratio, he or she can use n capacitors instead of two in each sub-circuit, which results in $V_o \approx V_i / n$, if the losses are neglected.

A similar step-up converter can be designed by charging each group of capacitors in parallel from the input voltage in each of the odd topologies, while discharging the other group of capacitors in series with the load. By neglecting the losses, $V_o = n\ V_i$. In order to save one capacitor and to ensure an uninterrupted input current, it is possible to form the discharging circuit by a series of V_i, the $(n-1)$ capacitors in discharging phase, and the load.

The same structure can be used to build a DC-AC inverter [12]. A sinusoidal waveform (say of frequency 50 or 60 Hz) can be approximated by a stair-like waveform (Fig. 3). In the figure, sixteen steps of value V_o (9.69 V) have been used to get the peak voltage ($\sqrt{2} \cdot 110$ V). In order to realize a step of value kV_o ($k = 1, \ldots, 16$) the inverter is used as a step-up DC-DC converter with $k-1$ capacitors and $V_i = 12V$, operating at a switching frequency of almost 1000 times that of the AC output. Each SC sub-circuit has 15 capacitors. For example, to realize the first step, one uses only one capacitor of each SC sub-circuit, with all the other capacitors disconnected, that is, the inverter be-

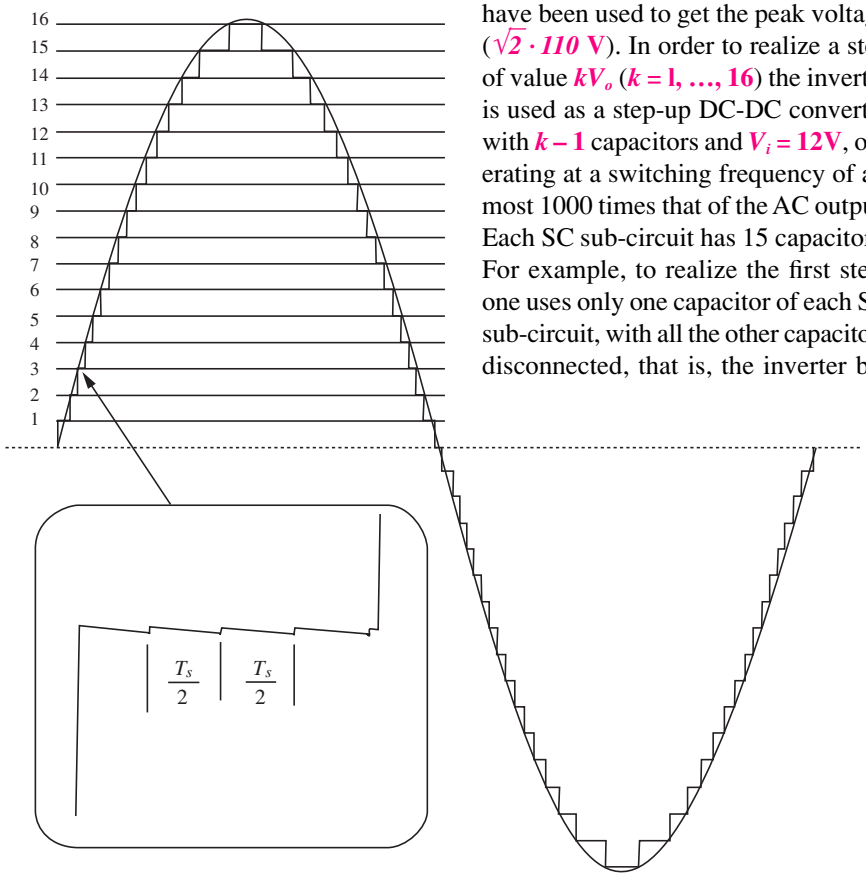

Figure 3. A sinusoidal waveform can be approximated by a stair waveform.

haves as a 12 / 9.69 V DC-DC converter. Only in step 16 are all the capacitors used. The negative part of the sinusoid is achieved simply by changing the direction of the current through the load.

A switched-capacitor circuit can also be used in the structure of a zero-current-switching (ZCS) converter—a converter in which the transistor turns off at the instant when the current through it reaches the value zero, implying zero-turn-off switching losses [13]. A ZCS condition is created by introducing a resonant block L_r, C_r into a classical converter as in Fig. 4. The input-to-output voltage ratio is equal to f_s / f_r, where $f_r = 1/(2\pi\sqrt{L_rC_r})$. Traditionally, changes in the input voltage were compensated by varying the switching frequency with a frequency-control method being used; but such a method has many disadvantages. An SC-circuit is used in the converter of Fig. 4 for varying the value of C_r. Capacitors C_1-C_8 have the values: 1*nF*, 1.5 *nF*, 2.5 *nF*, 5*nF*, 10*nF*, 20*nF*, 40*nF*, 80*nF*, and $C_o = 25nF$. According to the on/off positions of switches S_1-S_8, C_r can take 277 values between 26*nF* and 185*nF*, giving it, for all practical purposes, a continuous variation. V_o is kept constant at 12V despite a variation of the input voltage over the range [15, 35]V, or of the load current in the range [0.6, 4.1] A. Classically, the ZCS converter goes through four topological stages, where, in the fourth one, the voltage across C_r is zero. Only during the fourth stage, the zero-voltage-switching stage, do the switches S_1-S_8 turn on/off, according to the command of the feedback circuit, and thus zero-turn-on switching losses are assured for these switches.

The exact analysis performed in [17] pointed to losses due to the forward voltage on diodes in conduction, either in the charging or discharging circuit, to conduction losses in the parasitic resistances of the transistors (r_s) and capacitors (r_c), and to switching losses in the charging process of the capacitors (W_s). In a circuit with n capacitors per SC sub-circuit

$$W_s = \frac{nC}{2}\,\frac{1+e^{-DTs/\tau}}{1-e^{-DTs/\tau}}\,\hat{V}_o^{\,2}, \qquad \tau = (r_s + r_c)C$$

Even in an ideal converter with lossless elements, W_s is not zero. It depends mainly on $\hat{V}_o$. Therefore, from an efficiency point of view also, a designer will be interested in reducing the difference between the voltage on each capacitor at the end of, and beginning of, a discharging stage. A small difference will also help diminish the peak in the current at the beginning of charging process, thus limiting the EMI emission.

With all the methods the same result was found—regardless of the losses, the efficiency of a converter with n capacitors is

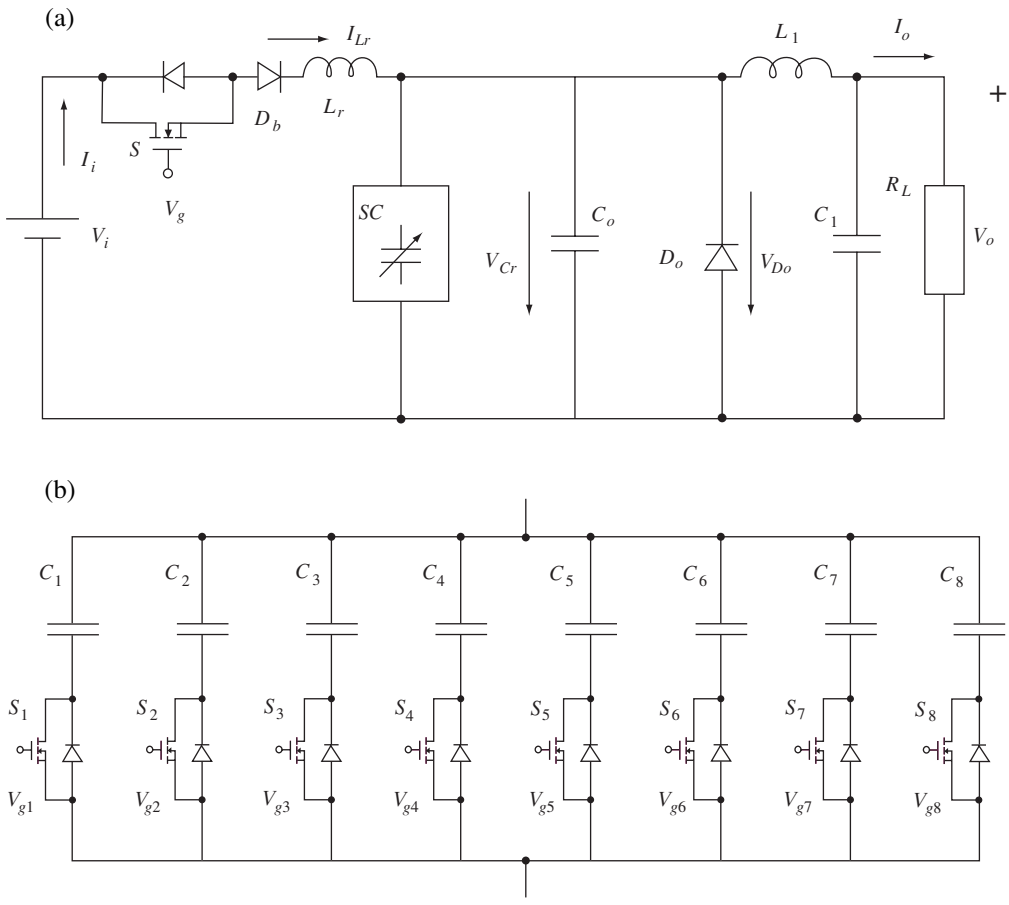

Figure 4. Zero-current-switching quasi-resonant converter with a switched-capacitor circuit as the resonant capacitance; (a) Power stage; (b) Structure of the SC-circuit.

Efficiency of the SC Converters and Optimization of Their Design

Transients and the steady-state of SC converters have been analyzed by methods [14–17] such as average state-space equations, algebraic modified nodal equations, or, more accurately, by integrating the exact differential equations written for each topological switching stage.

$$\eta = \frac{nV_o}{V_i}$$

for a step-down converter;

$$\eta = \frac{V_o}{(n+1)V_i}$$

for a step-up converter in which V_i is a part of the discharging circuit on the load.

This result might seem illogical because the efficiency depends only on the values of V_i, V_o and has nothing to do with the losses. The contradiction was later explained as follows. Let $V_{o\,obt}$ be the maximum voltage that can be obtained on the load in a given circuit, i.e. V_i / n in a step-down, or nV_i in a step-up converter, minus the voltage drops on the diodes and transistors in conduction, on ESRs of capacitors and wires. For example , in a typical 2 capacitor step-down converter with $V_i = 12$ V, $V_{o\,obt} = 5.3$ V. If the converter would be designed for a ratio 12 V / 5.3 V, then $\eta = 88\%$. But if the same converter is designed for a nominal ratio 12 V / 5V, then $\eta = 83\%$. Of course, with a given set of elements, it is not possible to get a V_o larger than $V_{o\,obt}$[†], therefore 88% is the maximum efficiency in this case. But as long as the converter is designed for a lower V_o than 5.3 V, the losses do not influence the efficiency, because in the formula of η appears the actual value of V_o and not $V_{o\,obt}$.

An optimum design, therefore,will be that in which the required V_o is close to $V_{o\,obt}$ for the respective circuit. For example, if one needs a ratio 12V / 4.5V, the design given in Fig. 2 would be a very bad one, as that converter would operate with a 75% efficiency. For such a ratio, another SC structure has to be chosen.

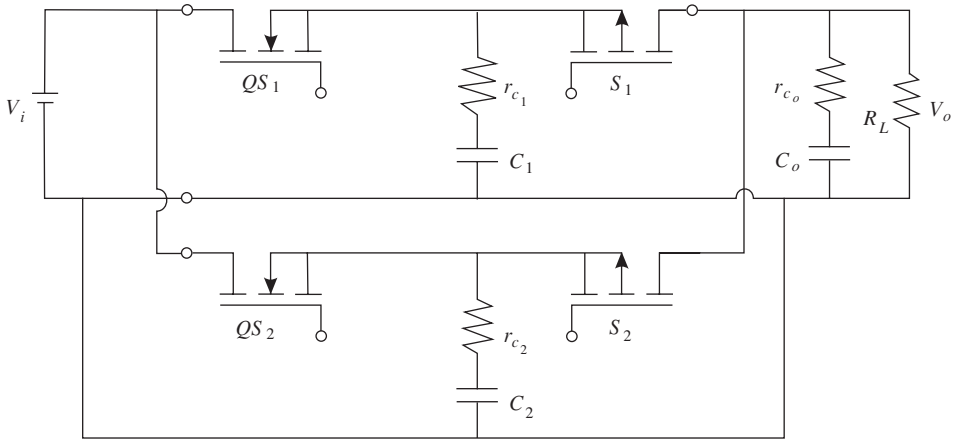

Figure 5. Step-down converter with current-control and continuous input current.

In [18] it was proved that the maximum attainable step-down/up voltage ratio M of a two-phase converter is given by the Fibonacci numbers $M(0) = 1$, $M(1) = 1$, and $M(n) = M(n-2) + M(n-1)$ where at least $(3n-2)$ switches are necessary. The Fibonacci converters are canonical designs, serving as terms of comparison for other designs. Unfortunately, these converters suffer from the drawback that the voltages on the capacitors are not equal, but follow a Fibonacci series.

Recent Developments in SC Converters

Research in the last three years [19–26] has resulted in converters with improved regulation [19], in new configurations of the capacitors and switches in the charging stage [20], in use of bi-directional switches for getting a bi-directional power flow (and thus the potential of both voltage step-down and step-up for a given DC-DC converter) [22–24], and in converters with continuous input current [25].

A current-controlled scheme is proposed in [25]. A simple step-down converter is shown in Fig. 5. It is formed by two basic cells (two switches QS and S, and a capacitor C) operating in antiphase. In the first topology, QS_1 and S_2 are in conduction, QS_2 and S_1 are in the off-position. Thus C_1 is charged from line V_i, and C_2 provides energy to the load R_L. In the second topology, QS_2 and S_1 are in conduction, and QS_1 and S_2 are in the off-position; so C_2 is charged from V_i and C_1 provides energy to the load. The durations of the two topologies are each equal to $T_s / 2$. The regulation is realized by varying the input current I_{ch}. The transistors QS_1 and QS_2 are operated between saturation and cut-off regions. In the first mode, the drain current is

$$I_D = \frac{1}{2} K_1 K_2 (V_{GS} - V_T)^2$$

where K_1 and K_2 are fabrication characteristics, and V_T is the threshold voltage of the MOSFET channel. Thus, the saturated MOSFET behaves as an ideal current source, whose value is controlled by the applied gate-source voltage V_{GS}. The capacitor (C_1 or C_2) is charged at a constant current I_{ch} (= I_D). Any variation in V_i or load will alter the level of V_{GS} through the feedback circuit, thus ensuring a constant output voltage. As in any steady-state cycle, the input current is constant for the entire switching period, and the EMI emission of the previous SC converters is suppressed. For larger power applications, two converters have been connected in parallel and operated in antiphase [26].

[†] It would be necessary to use devices with less losses, if available at a reasonable cost.

Perspectives

Switched-capacitor converters today are manufactured by industry: the MAX 828/829 voltage inverter by Maxim, and the LM 3351 voltage converter by National Semiconductor. With their high power density and IC implementation potential (all elements but capacitors of an SC regulator are realized as IC), SC power electronics are a preferable solution for low power supplies where no DC-DC isolation is necessary, as in portable electronic equipment.

With their steep voltage ratio (theoretically, by increasing the number of capacitors, any ratio is achievable), this type of power electronic circuit may serve as an answer to new challenges of technologies in the new millennium.

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