CSEE 4280: Lab 5:
Designing the Toy Processor Datapath

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Contributions: Please list contributions (in estimated percentages) of each member in the following categories.

- Pre-lab design and analysis:
  Habilou - 50% Kingsley - 50%
- In-lab module and testbench design
  Habilou - 50% Kingsley - 50%
- In-lab testbench simulation and analysis
  Habilou - 50% Kingsley - 50%
- In-lab FPGA synthesis and analysis
  Habilou - 50% Kingsley - 50%
- Lab report writing
  Habilou - 50% Kingsley - 50%

ABSTRACT

Now we have built all the necessary components for the Toy Processor. We will connect the Datapath and the controller to finish the implementation. You will then validate our design by simulating the behavior of your Toy Processor for a simple program.

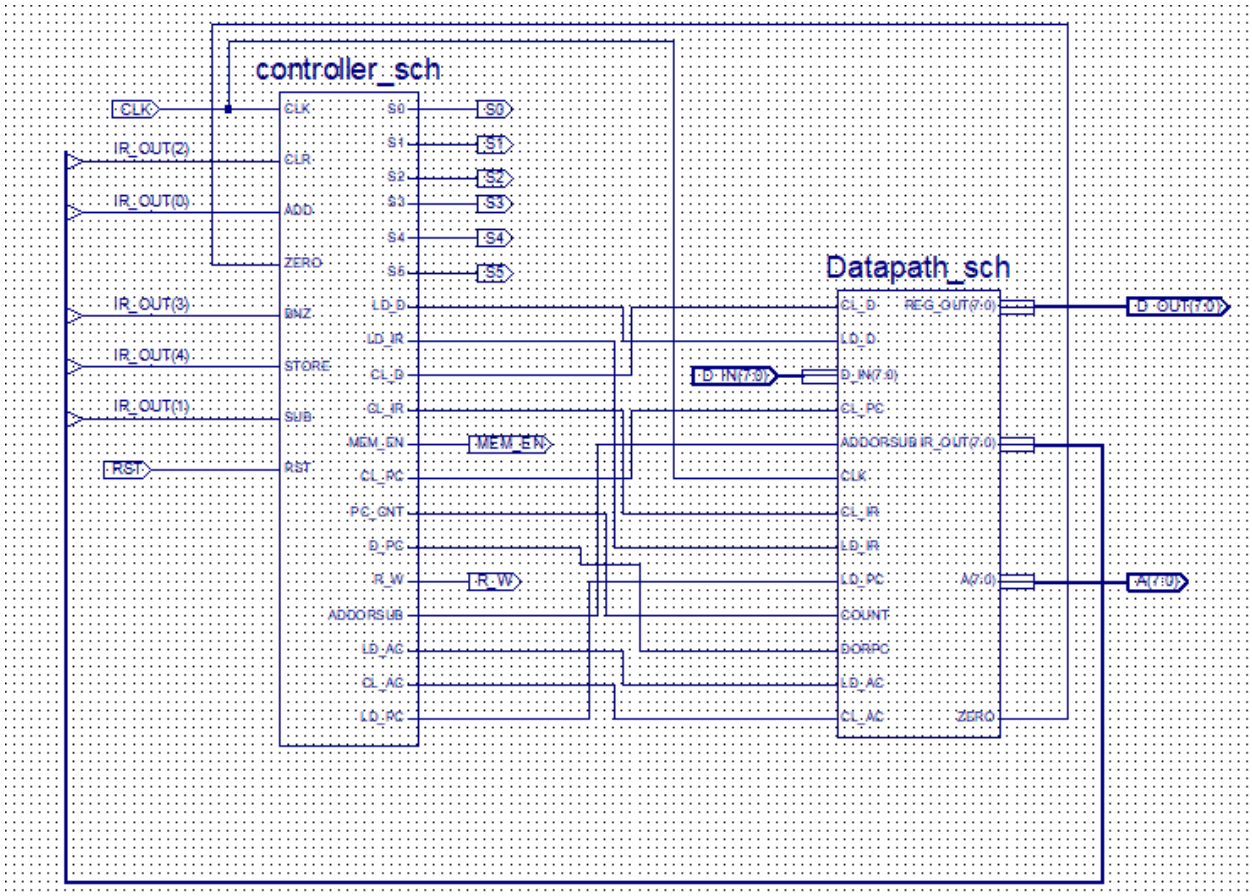
I. INTRODUCTION

A. Prelab

Instruction	Input	Memory Address
RESET	0000 0000	0000 0000
ADD	0000 0001	0000 0001
170	1010 1010	0000 0010
CLR	0000 0100	0000 0011
ADD	0000 0001	0000 0100
254	1111 1110	0000 0101
SUB	0000 0010	0000 0110
1	0000 0001	0000 0111
STORE	0001 0000	0000 1000
255	1111 1111	0000 1001
CLR	0000 0100	0000 1010
BNZ	0000 1000	0000 1011
254	1111 1110	0000 1100

II. IMPLEMENTATION DETAILS

A. Controller Schematic



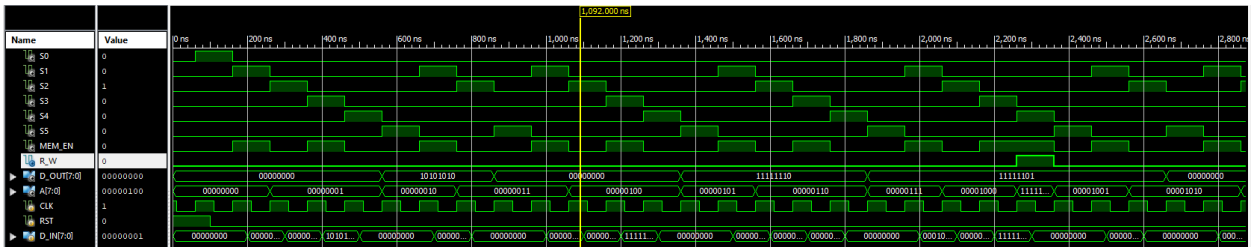
B. Controller Testbench

```
1  // Verilog test fixture created from schematic E:\Digital D
2
3  `timescale 1ns / 1ps
4
5  module toy_sch_toy_sch_sch_tb();
6
7     reg CLK = 1'b0;
8     reg RST = 1'b0;
9     reg [7:0] D_IN;
10    wire S0;
11    wire S1;
12    wire S2;
13    wire S3;
14    wire S4;
15    wire S5;
16    wire MEM_EN;
17    wire R_W;
18    wire [7:0] D_OUT;
19    wire [7:0] A;
20
21 // Instantiate the UUT
22    toy_sch UUT (
23       .CLK(CLK), .RST(RST), .D_IN(D_IN),
24       .S0(S0), .S1(S1), .S2(S2), .S3(S3),
25       .S4(S4), .S5(S5), .MEM_EN(MEM_EN),
26       .R_W(R_W), .D_OUT(D_OUT), .A(A)
27    );
28
29    initial begin
30       CLK = 1'b1;
31       RST = 1'b1;
32       D_IN = 8'b00000000;
33
34       #10;  //50ns
35       CLK = ~CLK;
36       #50;  //100ns
37       CLK = ~CLK;
38       #40;
39       RST = 1'b0;
40       #10;  //150
41       CLK = ~CLK;
42       #50;  //200
43       CLK = ~CLK;
44       #40;
45       D_IN = 8'b00000001;
46       #10;  //250
47       CLK = ~CLK;
```

```
19      wire [7:0] A;
20
21  // Instantiate the UUT
22      toy_sch UUT (
23          .CLK(CLK), .RST(RST), .D_IN(D_IN),
24          .S0(S0), .S1(S1), .S2(S2), .S3(S3),
25          .S4(S4), .S5(S5), .MEM_EN(MEM_EN),
26          .R_W(R_W), .D_OUT(D_OUT), .A(A)
27      );
28
29      initial begin
30          CLK = 1'b1;
31          RST = 1'b1;
32          D_IN = 8'b00000000;
33
34          #10;  //50ns
35          CLK = ~CLK;
36          #50;  //100ns
37          CLK = ~CLK;
38          #40;
39          RST = 1'b0;
40          #10;  //150
41          CLK = ~CLK;
42          #50;  //200
43          CLK = ~CLK;
44          #40;
45          D_IN = 8'b00000001;
46          #10;  //250
47          CLK = ~CLK;
48          #50;  //300
49          CLK = ~CLK;
50          #40;
51          D_IN = 8'b00000000;
52          #10;  //350
53          CLK = ~CLK;
54          #50;  //400
55          CLK = ~CLK;
56          #40;
57          D_IN = 8'b10101010;
58          #10;  //450
59          CLK = ~CLK;
60          #50;  //500
61          CLK = ~CLK;
62          #40;
63          D_IN = 8'b00000000;
64          #10;  //550
65          CLK = ~CLK;
```

III. Analysis Error

A. Waveform



The Waveform obtained confirms the correctness of our module because we were able to replicate the waveform given in the lab instruction.

IV. CONCLUSION

We were able to create a controller and confirmed its functionality by creating a testbench and obtaining a waveform identical to the one given in the lab instruction.