

Daisuke Otagiri

Professor Kurdahi

EECS 113

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Assignment 1: Screenshots

When N= 6

Data Memory:

System Clock (MHz) 12.0 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	B
0x00	0x00	0x00	0x00	0x00	0x03

R6	ACC
0x00	0x05

R5	PSW
0x00	0x00

R4	IP
0x00	0x00

R3	IE
0x00	0x00

R2	PCON
0x05	0x00

R1	DPH
0x03	0x00

R0	DPL
0x45	0x00

SP
0x07

pins bits TH1 TL1

P3	P2	P1	P0
0xFF	0xFF	0xFF	0xFF

PC 0x006A

PSW 0 0 0 0 0 0 0 0

Modify Code

addr 0x0000 0x80 value

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	80	3E	00	00	00	00	00	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	78	40	7F	06	79	00	76	00	08	76	01	7A	01	1F	08
50	E9	2A	F6	8A	F0	A9	F0	FA	DF	F5	00	00	00	00	00
60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

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Code Memory:

System Clock (MHz) 12.0 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	B
0x00	0x00	0x00	0x00	0x00	0x03

R6	ACC
0x00	0x05

R5	PSW
0x00	0x00

R4	IP
0x00	0x00

R3	IE
0x00	0x00

R2	PCON
0x05	0x00

R1	DPH
0x03	0x00

R0	DPL
0x45	0x00

SP
0x07

pins bits TH1 TL1

P3	P2	P1	P0
0xFF	0xFF	0xFF	0xFF

PC 0x006A

PSW 0 0 0 0 0 0 0 0

Modify RAM

addr 0x00 0x42 value

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	45	03	05	00	00	00	00	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	00	01	01	02	03	05	00	00	00	00	00	00	00	00	00
50	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

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When N=9

Data Memory:

System Clock (MHz) 12.0 1 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	0x00	B	0x0D
0x00	0x00	0x00	0x00	R6	0x00	ACC	0x15
RXD	TXD			R5	0x00	PSW	0x41
1	1	TMOD	0x00	R4	0x00	IP	0x00
SCON	0x00	TCON	0x00	R3	0x00	IE	0x00

pins bits TH1 TL1

0xFF	0xFF	P3	0x00	0x00	R2	0x15	PCON	0x00
0xFF	0xFF	P2			R1	0x0D	DPH	0x00
0xFF	0xFF	P1			R0	0x48	DPL	0x00
0xFF	0xFF	P0					SP	0x07

PC 0x006F

8051

PSW 0 1 0 0 0 0 0 1

Modify Code

addr	0x0000	0x80	value												
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	80	3E	00	00	00	00	00	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	78	40	7F	09	79	00	76	00	08	76	01	7A	01	1F	08
50	E9	2A	F6	8A	F0	A9	F0	FA	DF	F5	00	00	00	00	00
60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

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Code Memory:

System Clock (MHz) 12.0 1 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	0x00	B	0x0D
0x00	0x00	0x00	0x00	R6	0x00	ACC	0x15
RXD	TXD			R5	0x00	PSW	0x41
1	1	TMOD	0x00	R4	0x00	IP	0x00
SCON	0x00	TCON	0x00	R3	0x00	IE	0x00

pins bits TH1 TL1

0xFF	0xFF	P3	0x00	0x00	R2	0x15	PCON	0x00
0xFF	0xFF	P2			R1	0x0D	DPH	0x00
0xFF	0xFF	P1			R0	0x48	DPL	0x00
0xFF	0xFF	P0					SP	0x07

PC 0x006F

8051

PSW 0 1 0 0 0 0 0 1

Modify RAM

addr	0x00	0x43	value												
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	48	0D	15	00	00	00	00	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	00	01	01	02	03	05	08	0D	15	00	00	00	00	00	00
50	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

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When N=12:

Data Memory:

System Clock (MHz) 12.0 1 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	0x07	B	0x03
0x00	0x00	0x00	0x00	R6	0x00	ACC	0x05
RXD	TXD			R5	0x00	PSW	0x00
1	1	TMOD	0x00	R4	0x00	IP	0x00
SCON	0x00	TCON	0x00	R3	0x00	IE	0x00

pins bits TH1 TL1 R1 0x02 DPH 0x00

0xFF 0xFF P3 0x00 0x00 R0 0x45 DPL 0x00

0xFF 0xFF P2 PC 8051 SP 0x07

0xFF 0xFF P1 0x0055 PSW 0 0 0 0 0 0 0 0

0xFF 0xFF P0 0x0055 PSW 0 0 0 0 0 0 0 0

Modify Code

Code Memory

addr 0x0000 0x80 value

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	80	3E	00	00	00	00	00	00	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	78	40	7F	0C	79	00	76	00	08	76	01	7A	01	1F	1F	08
50	E9	2A	F6	8A	F0	A9	F0	FA	DF	F5	00	00	00	00	00	00
60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

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Code Memory:

System Clock (MHz) 12.0 1 Update Freq.

SBUF

R/O	W/O	TH0	TL0	R7	0x07	B	0x03
0x00	0x00	0x00	0x00	R6	0x00	ACC	0x05
RXD	TXD			R5	0x00	PSW	0x00
1	1	TMOD	0x00	R4	0x00	IP	0x00
SCON	0x00	TCON	0x00	R3	0x00	IE	0x00

pins bits TH1 TL1 R1 0x02 DPH 0x00

0xFF 0xFF P3 0x00 0x00 R0 0x45 DPL 0x00

0xFF 0xFF P2 PC 8051 SP 0x07

0xFF 0xFF P1 0x0055 PSW 0 0 0 0 0 0 0 0

0xFF 0xFF P0 0x0055 PSW 0 0 0 0 0 0 0 0

Modify RAM

Data Memory

addr 0x00 0x00 value

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	45	02	03	00	00	00	00	07	00	00	00	00	00	00	00	00
10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
30	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
40	00	01	01	02	03	05	08	0D	15	22	37	59	00	00	00	00
50	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
60	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
70	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

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RST Step Run New Load Save Copy Paste X

Time: 50us - Instructions: 39

```
0000| JMP MAIN
      ORG 40H
      MAIN:
0040| MOV R0, #40H ;start storing
0042| MOV R7, #12 ;number of fib to
0044| MOV R1, #00H
0046| MOV @R0, #0H;move first number
0048| INC R0
0049| MOV @R0,#01H ;move the second
004B| MOV R2, #01H
004D| DEC R7 ;match # of sequence
004E| DEC R7

      LABEL:
004F| INC R0 ;move to next open
0050| MOV A, R1
0051| ADD A, R2 ;add two numbers
0052| MOV @R0, A ;store total into
0053| MOV B, R2 ;store second number
0055| MOV R1, B ;second number in
```