Name (Pin Yin): _____ Assin. No.: _____

CQUPT EE310 2019 Fall Quiz 6a

(15min, 20pts)

1. (2pts) A memory block has 20-bit address bus, what is the maximum number of memory locations does this block support?

   Maximum 2^{20} =1Mb memory locations

2. (2pts) What is the full name of FIFO memory? What is the main benefit using a FIFO memory?

   First-in-first-out, to connect two systems with different data rate/clock frequency

3. (4pts) What is the full name of DRAM? What are the main advantage and disadvantage of DRAM compared to SRAM?
   Name-1pts, advantage-1pts, disadvantage-2pts

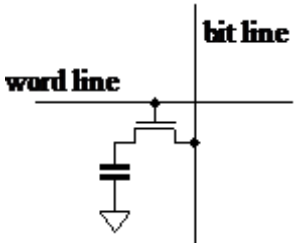
   Dynamic random access memory.

   Advantage: small size, simple circuit, high density, low cost

   Disadvantage: data need to be refreshed regularly

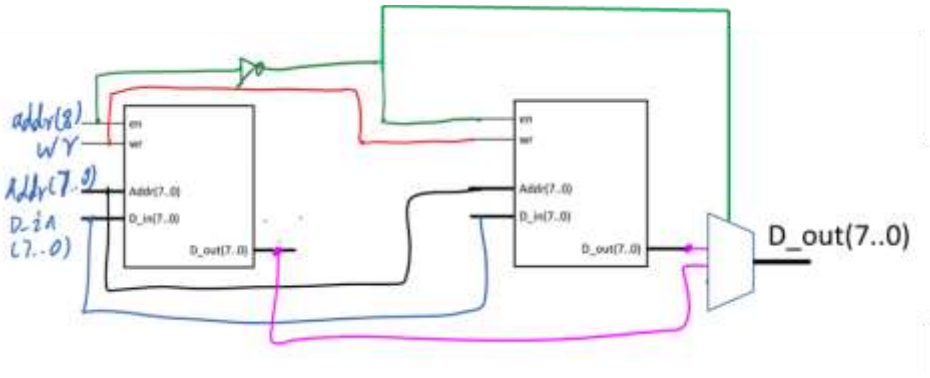
4. (4pts) Determine the following memory type: volatile or nonvolatile:
   a). ROM b). SRAM c). DRAM d). Flash RAM
   -1pt for each mistake.
   volatile: b) and c)
   nonvolatile: a) and d)

5. (4pts) Explain how you can configure the bit line and word line of the following DRAM cell to store a logic '1' on the capacitor. (give partial credit)



Set bit line to high (logic 1), and then set word line to high to turn on the MOSFET.

6. (4pts) Address decoding: Using two of the 8-bit memory block given below, expand the address lines to 9 bits while keep the data buses as 8 bits. Show your connections clearly.
   Inverter can be changed to a decoder



Name (Pin Yin): _____ Assin. No.: _____

CQUPT EE310 2019 Fall Quiz 6b

(15min, 20pts)

1. (2pts) A memory block has 30-bit address bus, what is the maximum number of memory locations does this block support?
   Maximum $2^{30} = 1Gb$ memory locations

2. (2pts) What are multiport memories? What is the benefit to have a dual-port RAM over a single-port RAM?

   Memories with more than 1 data/address buts and control lines.
   Can perform read and write at the same time

3. (4pts) What is the full name of SRAM? What is the difference between asynchronous and synchronous SRAM?
   Name-1pt, difference—3pts, give partial credit

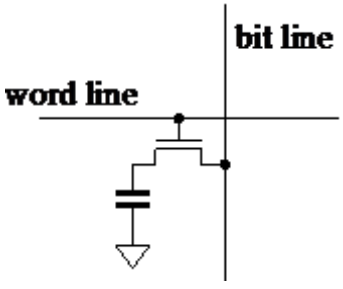
   Static random access memory

   Asynchronous SRAM is combinational and there is no clock signal

   Data in synchronous SRAM can only be accessed at clock edge

4. (4pts) Determine the following memory type: volatile or nonvolatile:
   a). ROM b). SRAM c). DRAM d). Flash RAM
   -1pt for each mistake
   volatile: b) and c)
   nonvolatile: a) and d)

5. (4pts) Explain how you can configure the bit line and word line of the following DRAM cell to read a logic '1' stored on the capacitor. (give partial credit)



Set bit line to intermediate voltage (between 0 and 1), and then set word line to high to turn on the MOSFET.

6. (4pts) Data bus expansion: Using two of the 8-bit memory block given below, expand the input/output data size to 16 bits. Show your connections and mark the lower and higher byte clearly.