Name (Pin Yin): _____ **Student ID**_____

CQUPT EE310 2020 Fall Quiz 2a

(15min, 20pts)

1. (5 pts) Finish the following SystemVerilog program to realize a 2-input OR gate.

   module or2in(input logic a, b, output logic y);

   y = a | b;

   endmodule

2. (10 pts) Write the states table (truth table) for a **falling**-edge triggered D flip-flop with asynchronous reset (active high) input

Reset	D	Clk	Q	Q*
1	X	X	X	0
0	0	H -> L	0	0
0	0	H -> L	1	0
0	1	H -> L	0	1
0	1	H -> L	1	1

3. (5 pts) How would you modify the following SystemVerilog code block to realize a **falling**-edge triggered D flip-flop

```
...
always_ff @(posedge clk, negedge reset)
   if (~reset) q <= 0;
   else q <= d;
  ...
```

Change posedge clk to negedge clk in the sensitivity list for the always_ff statement

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CQUPT EE310 2020 Fall Quiz 2b

(15min, 20pts)

1. (5 pts) Finish the following SystemVerilog program to realize a 2-input AND gate.

   module and2in(input logic a, b, output logic y);

   y = a & b; *//place your answer here*

   endmodule

2. (10 pts) Write the states table (truth table) for a rising-edge triggered JK flip-flop with asynchronous set (active low) input

Reset	J	K	Clk	Q	Q*
0	X	X	X	X	0
1	0	0	L -> H	0	0
1	0	0	L -> H	1	1
1	0	1	L -> H	0	0
1	0	1	L -> H	1	0
1	1	0	L -> H	0	1
1	1	0	L -> H	1	1
1	1	1	L -> H	0	1
1	1	1	L -> H	1	0

3. (5pts) what signals should be included in the sensitivity list?

```
always_ff @(sensitivity list)
   if(reset) q <= 0;
   else q <= d;
  ...
```

(posedge or negedge) clk , posedge reset ans.