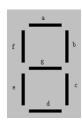
CQUPT EE310 2020 Fall Quiz 3a

(15min, 20pts)

- 1. (4pts) For a 7-seg LED display, all outputs are active HIGH.
 - a. Write the input binary code to display the hexadecimal number 'E'. 1110
 - b. What is the logic level for each output in order of abcdefg? 1001111



- 2. (6pts) Read the following System Verilog program and answer the questions.
 - a. How many input and output ports in the module named dec1?
 - 1 input port and 1 output port
 - b. How many input and output pins in this circuit?2 input pins, 4 output pins
 - c. Describe the function of the logic circuit. If possible, write down the official name of this circuit.

This circuit functions as an encoder whose output is the binary equivalent of a power of 2 specified by the input, I.

3. (6pts) Rewrite the always block in question 2 using if –else if – else statements.

```
always @(I)
begin

if(I == 2'b00) O = 4'b0001;

else if(I == 2'b01) O = 4'b0010;

else if(I == 2'b10) O = 4'b0100;

else if(I == 2'b11) O = 4'b1000;

else O = 4'bxxxx;
```

4. (4pts) A signal is defined as logic type, please explain what the following values mean.

'1': Logic level high or true or 1 '0': Logic level low or false or 0

'z': <u>High Impedence (no connection)</u> 'x': <u>Logic level unknown</u>

Name (Pin Yin):	Solution	
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CQUPT EE310 2020 Fall Quiz 3b (15min, 20pts)

- 1. (4pts) For a 7-seg LED display, all outputs are active LOW.
 - a. Write the input binary code to display the hexadecimal number 'C'. 1100
 - b. What is the logic level for each output in order of abcdefg? 1001110
- 2. (6pts) Read the following System Verilog program and answer the questions.
 - a. How many input and output ports in the module named mux4?

 Two input ports, One output port
 - b. How many input and output pins in this circuit? Six input pins, One output pin
 - c. Describe the function of the logic circuit. If possible, write down the official name of this circuit.

This is a 2 by 4 multiplexer that by way of the sel input, select one of four input lines to send to the output.

3. (6pts) Rewrite the always block in question 2 using if —else if- else statements.

```
always @(sel, d in)
begin
    if(sel == 2'b00) O = d_in[0];
     else if(sel == 2'b01) 0 = d in[1];
     else if(sel == 2'b10) O = d_in[2];
     else if(sel == 2'b11) 0 = d_in[3];
end
```

4. (4pts)A signal is defined as logic type, please explain what the following values mean.

'X': <u>Unknown logic level</u>

'1': Logic level high or true or 1

'0': Logic level low or false or 0 Z': High Impedence (no connection)