
Lecture25:

Digital CMOS circuits (3)

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NMOS inverter

- Passive “pull-up” device

- (a) Degradation of output level

Too small R_D , when $V_{in} = V_{DD}$.

In this case, large R_D is desirable.

- (b) Risetime limitation

Too small current for 1 \rightarrow 0 transition. ($V_{in} = 0$)

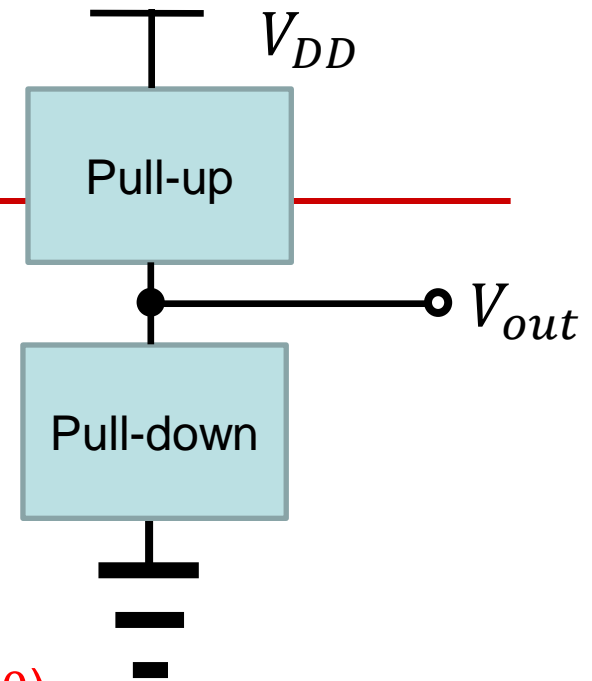
In this case, a better capability to charge the C_L is desirable.

- (c) Static power consumption

No ability to block the current, when $V_{in} = V_{DD}$.

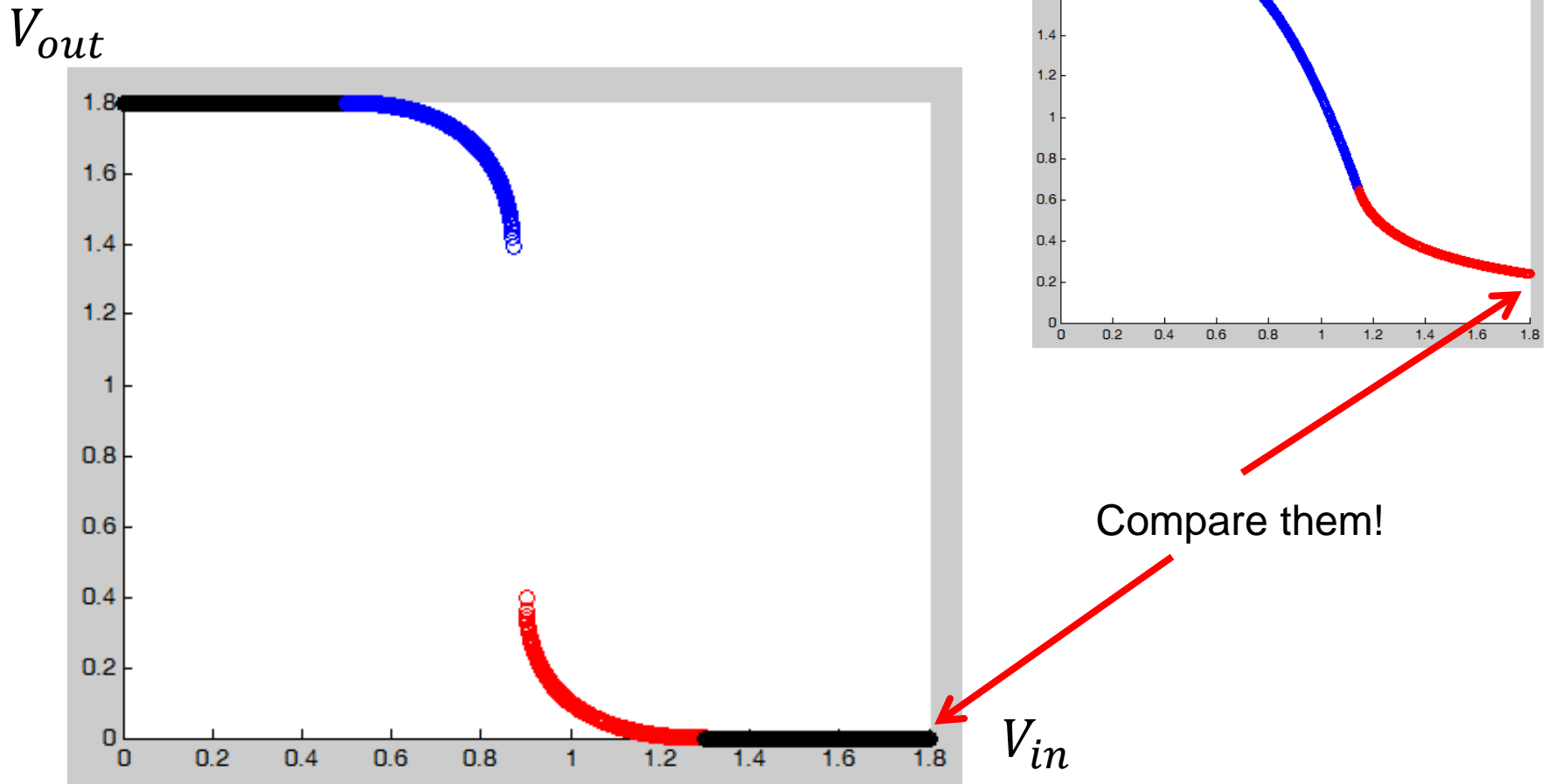
In this case, no current conduction is desirable.

- (a) & (c) \leftrightarrow (b)



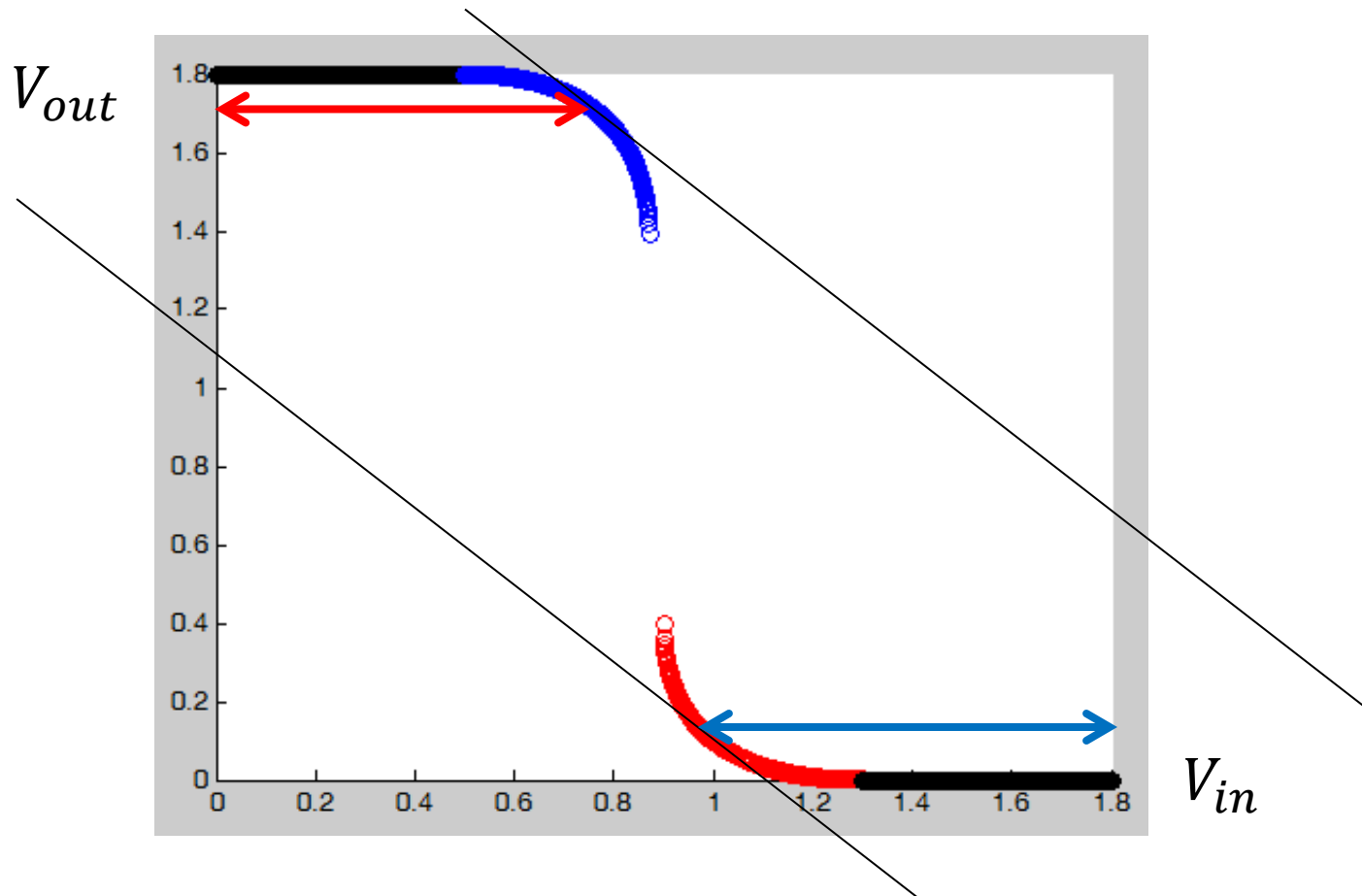
CMOS inverter

- Voltage transfer curve of a CMOS inverter
 - It is the answer of Homework#3.



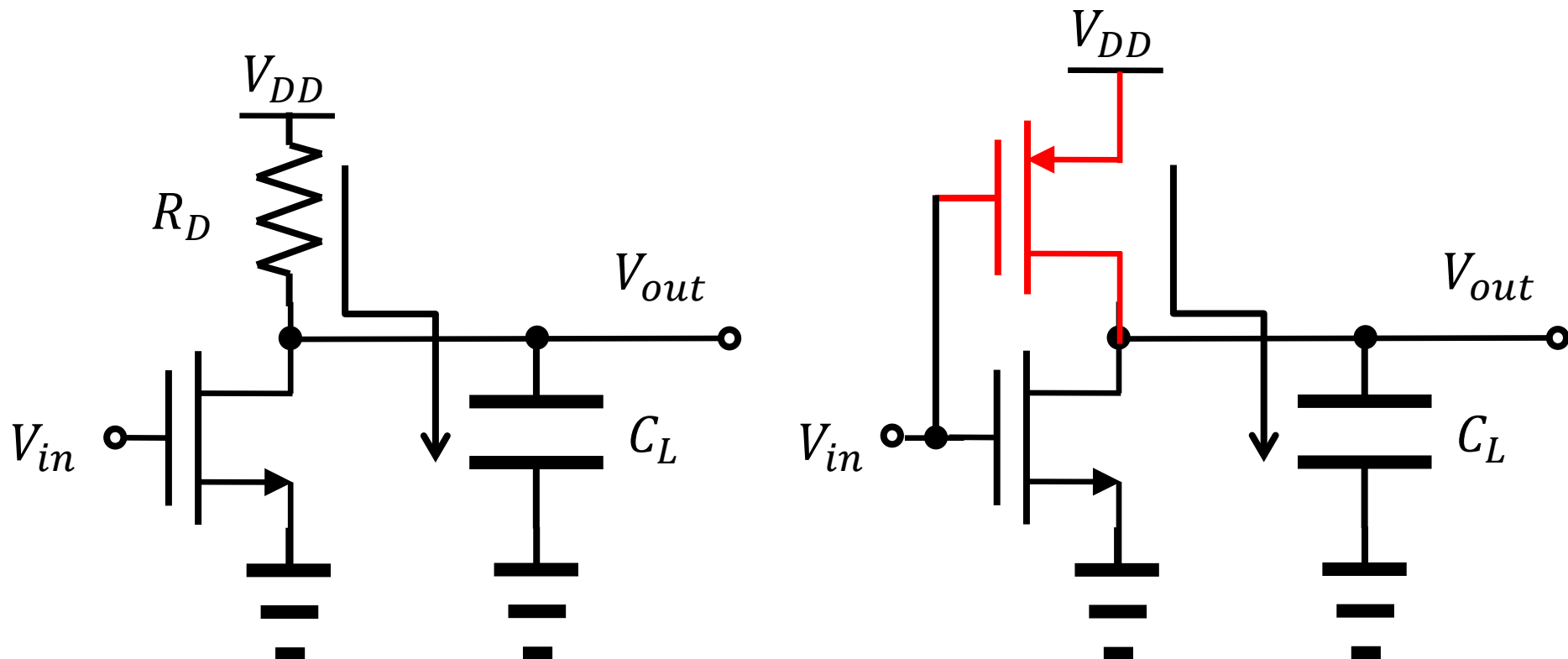
Noise margin?

- Noise margin is greatly improved.
 - Much better than the NMOS inverter



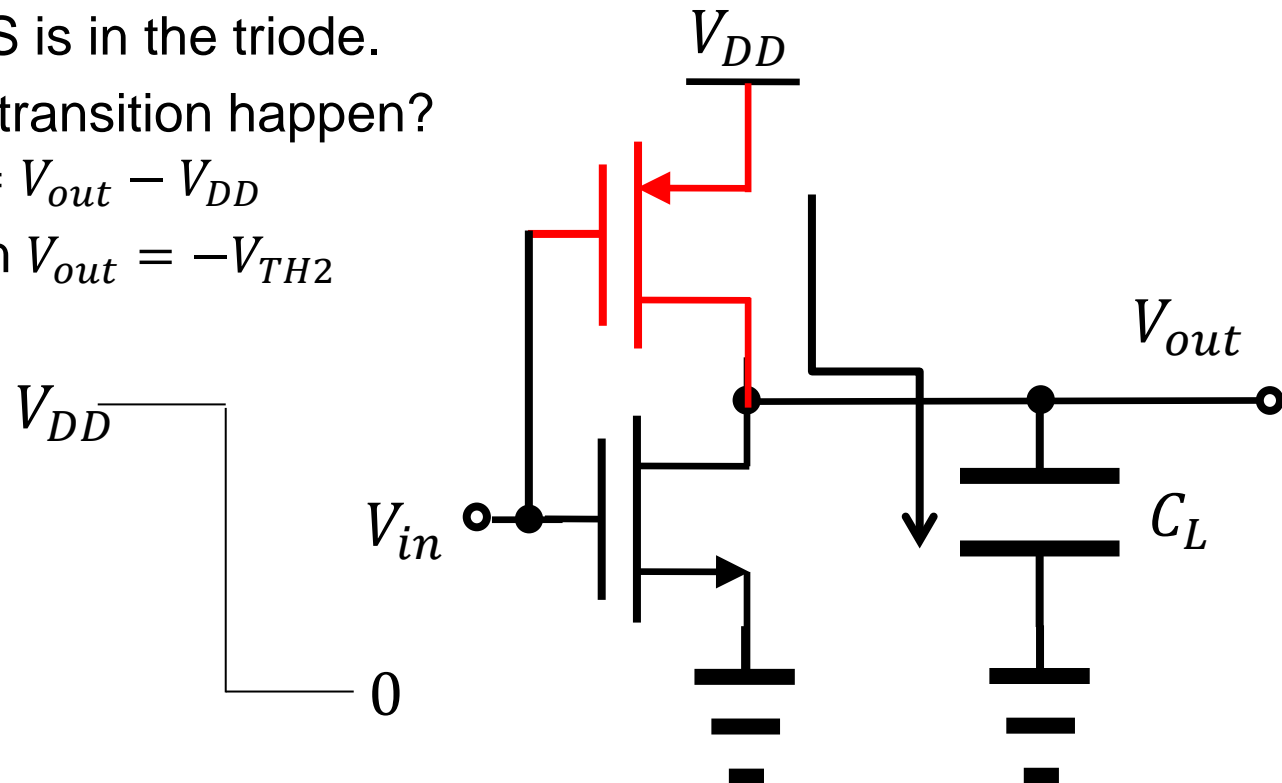
Speed of CMOS inverter (1/4)

- Consider the input transition from HIGH to LOW.
 - Instead of the resistor (R_D), now the PMOS pulls up the V_{out} .



Speed of CMOS inverter (2/4)

- Guess the charging speed.
 - In other words, the PMOS current ($I_{PMOS} = C_L \frac{dV_{out}}{dt}$)
 - At the beginning, the PMOS is in the saturation.
 - Later, the PMOS is in the triode.
 - When does the transition happen?
- $V_{in} - V_{DD} - V_{TH2} = V_{out} - V_{DD}$
- Therefore, when $V_{out} = -V_{TH2}$

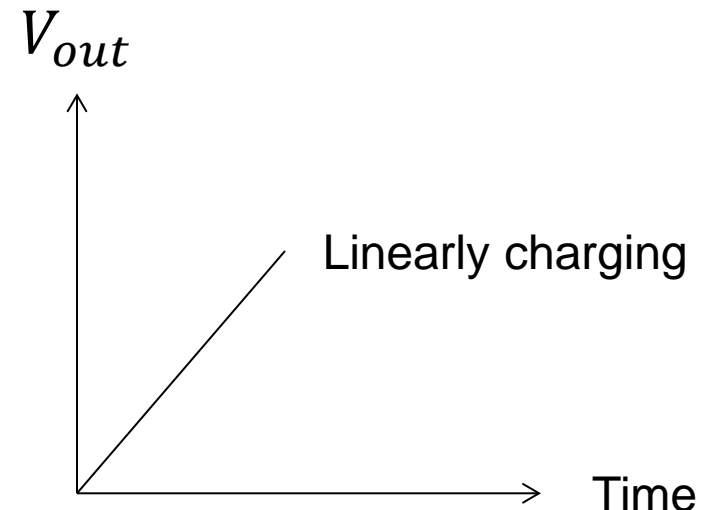


Speed of CMOS inverter (3/4)

- The first case (charge up to $-V_{TH2}$)
 - PMOS saturation current (constant)

$$T_{PLH1} = \frac{C_L |V_{TH2}|}{\frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{DD} - |V_{TH2}|)^2}$$

$$T_{PLH1} = R_{on2} C_L \frac{2|V_{TH2}|}{V_{DD} - |V_{TH2}|}$$



Speed of CMOS inverter (4/4)

- The second case (charge up to $\frac{V_{DD}}{2}$)
 - PMOS triode current
$$\frac{1}{2} \mu_p C_{ox} \frac{W}{L} [2(V_{DD} - |V_{TH2}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2] = C_L \frac{dV_{out}}{dt}$$
 - Time to reach $\frac{V_{DD}}{2}$
$$T_{PLH2} = R_{on2} C_L \ln \left(3 - 4 \frac{|V_{TH2}|}{V_{DD}} \right)$$
 - (Let's derive it together!)
- The overall propagation delay is
 - $T_{PLH} = R_{on2} C_L \left[\frac{2|V_{TH2}|}{V_{DD} - |V_{TH2}|} + \ln \left(3 - 4 \frac{|V_{TH2}|}{V_{DD}} \right) \right]$

Power consumption

- No static power dissipated!
 - Only the “dynamic” power dissipation is determined.
 - High → Low → High → ...
 - It involves charging and discharging the load capacitance.
 - The energy stored in the load capacitance
$$\frac{1}{2} C_L V_{DD}^2$$
 - The energy dissipated by the PMOS is also $\frac{1}{2} C_L V_{DD}^2$.
 - Therefore, $C_L V_{DD}^2$ is dissipated during T_{in} .

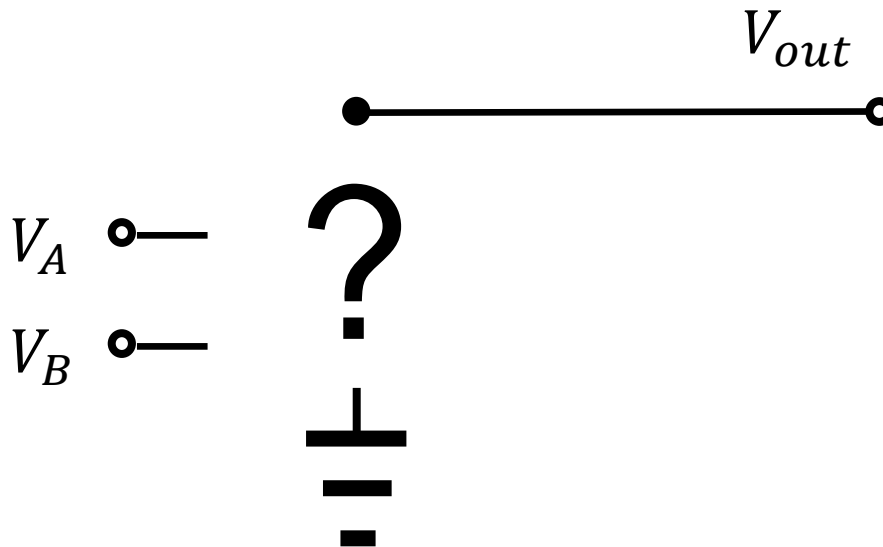
$$P_{av} = f_{in} C_L V_{DD}^2$$

NAND gate (1/4)

- Its truth table

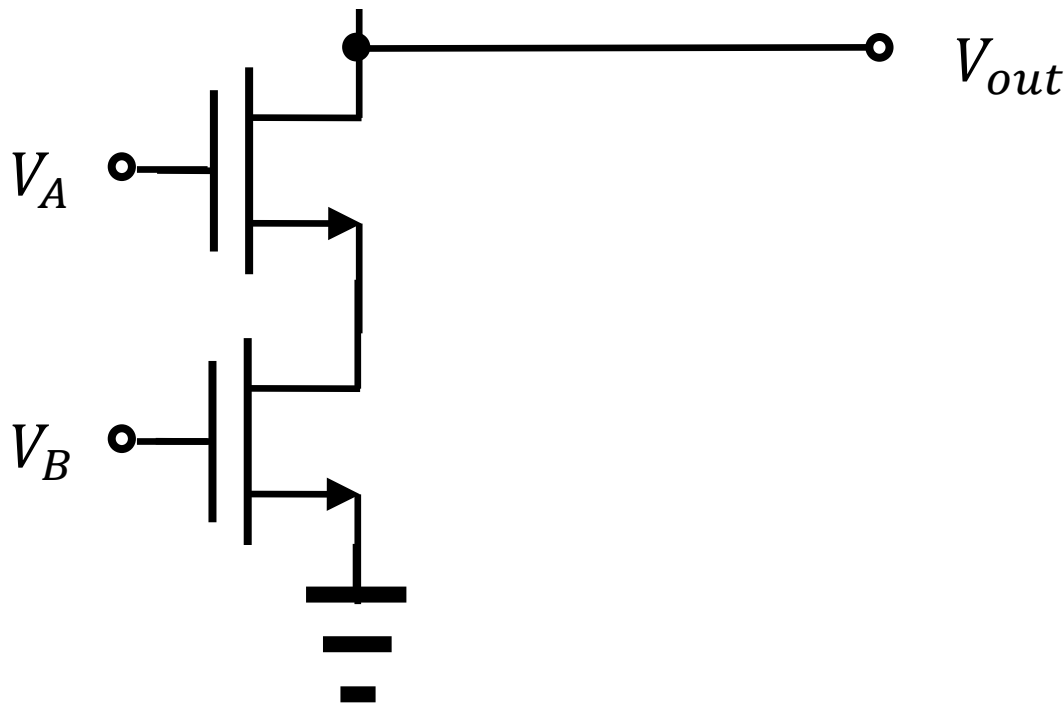
A	B	$A \text{ NAND } B$
0	0	1
0	1	1
1	0	1
1	1	0

- Only when two inputs are 1, the output node is connected to GND.



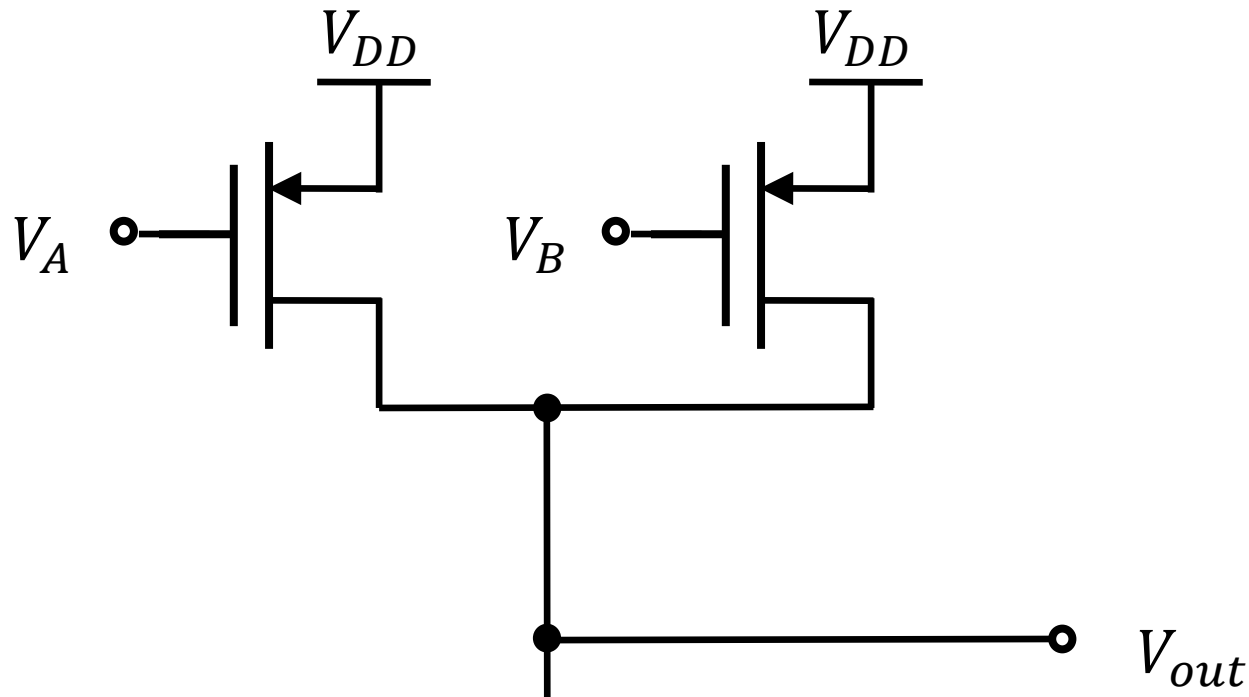
NAND gate (2/4)

- It is easy to realize that the serially connected NMOSFETs can do it.
 - When one of V_A or V_B is low, no electric connection between V_{out} and GND.



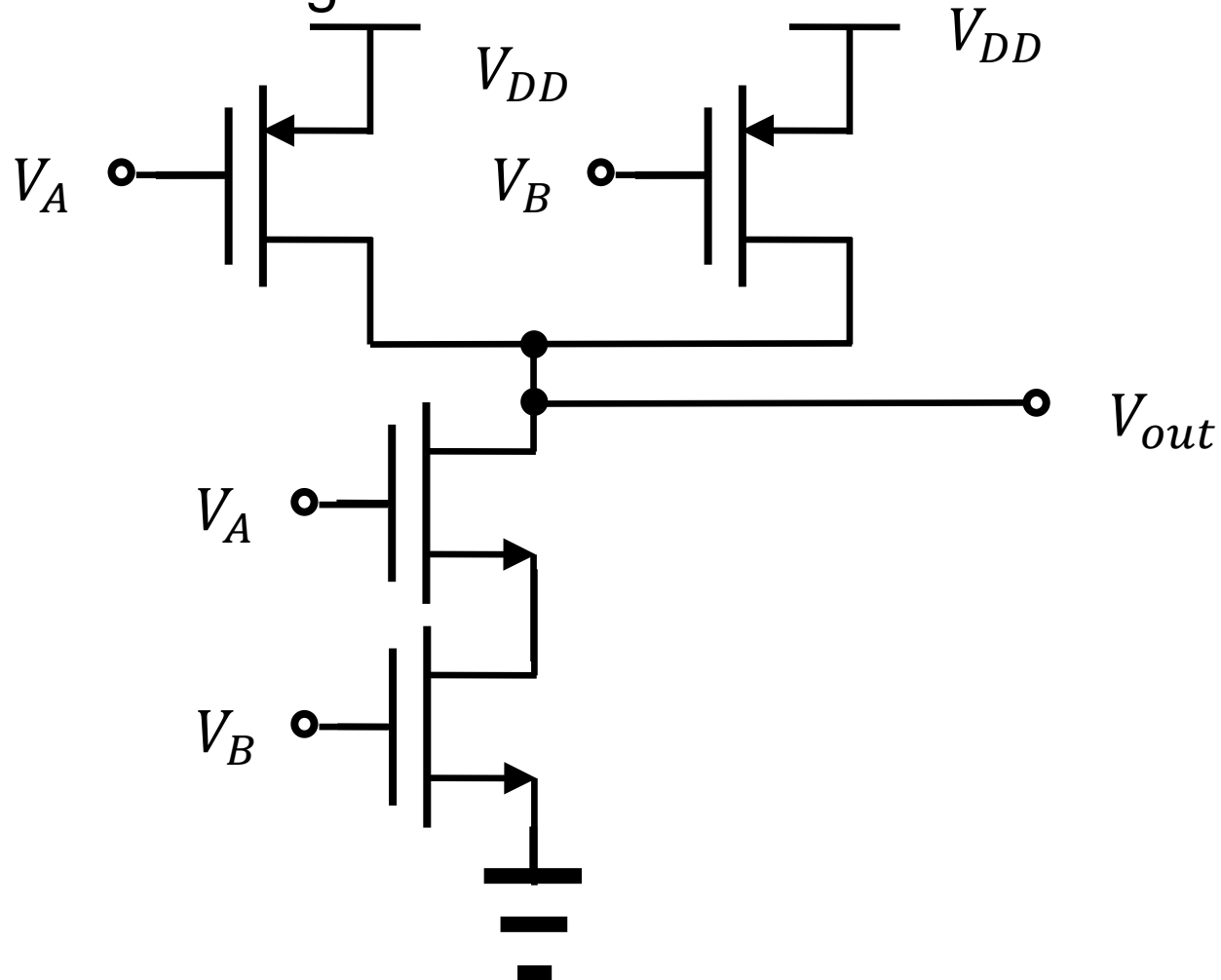
NAND gate (3/4)

- Similarly, the output node is not connected to V_{DD} , when two inputs are 1.
- It is easy to realize that the parallel connected NMOSFETs can do it.



NAND gate (4/4)

- Overall, the NAND gate looks like:



NOR gate

- Dual to the NAND gate
 - Serial PMOS
 - Parallel NMOS
- Which one is weaker?
 - Pull-up? Pull-down?