Lecture24:
Digital CMOS circuits (2)

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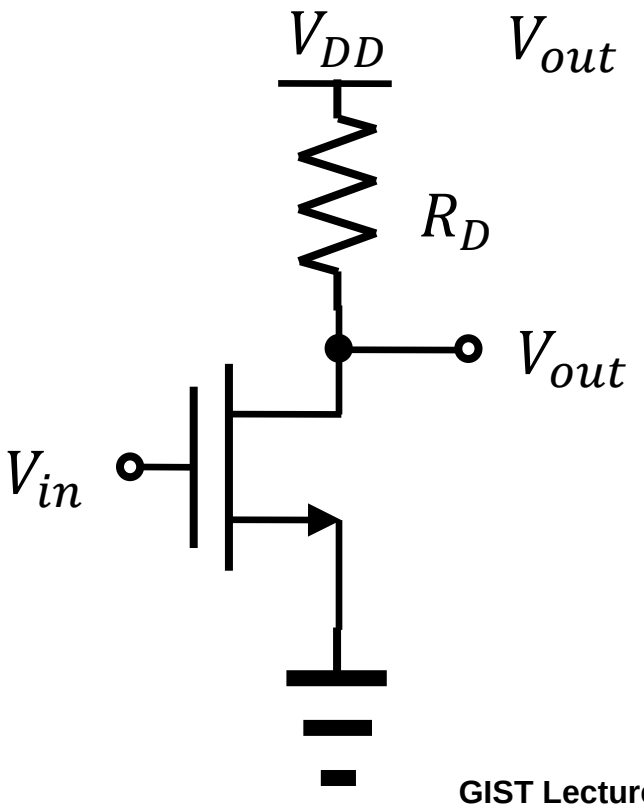
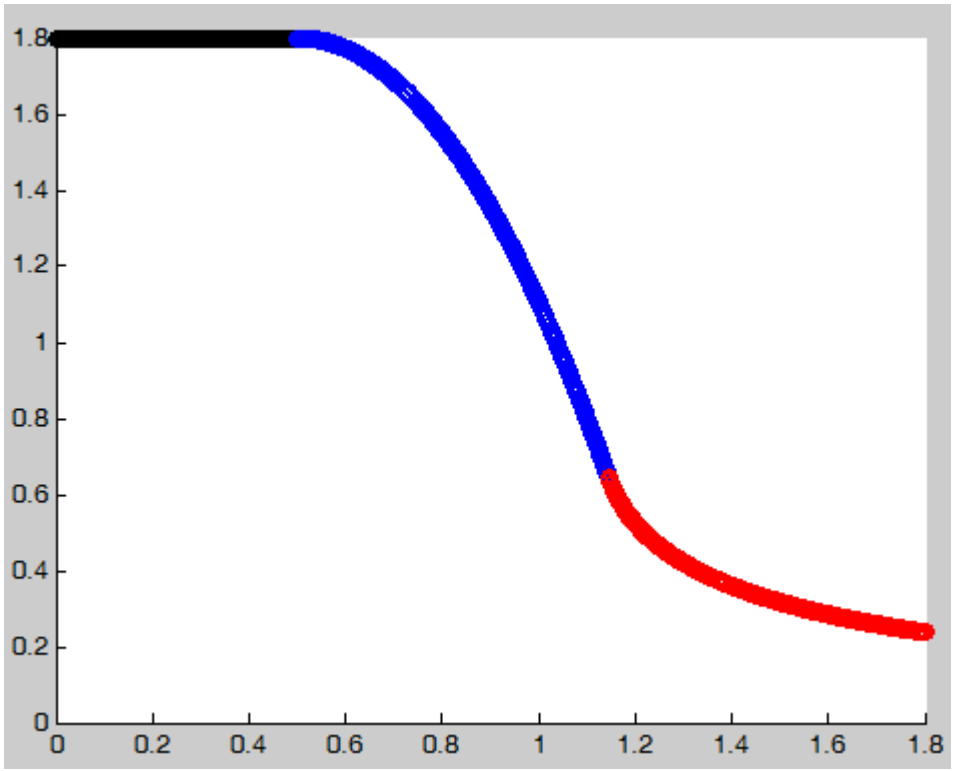
Review of last lecture

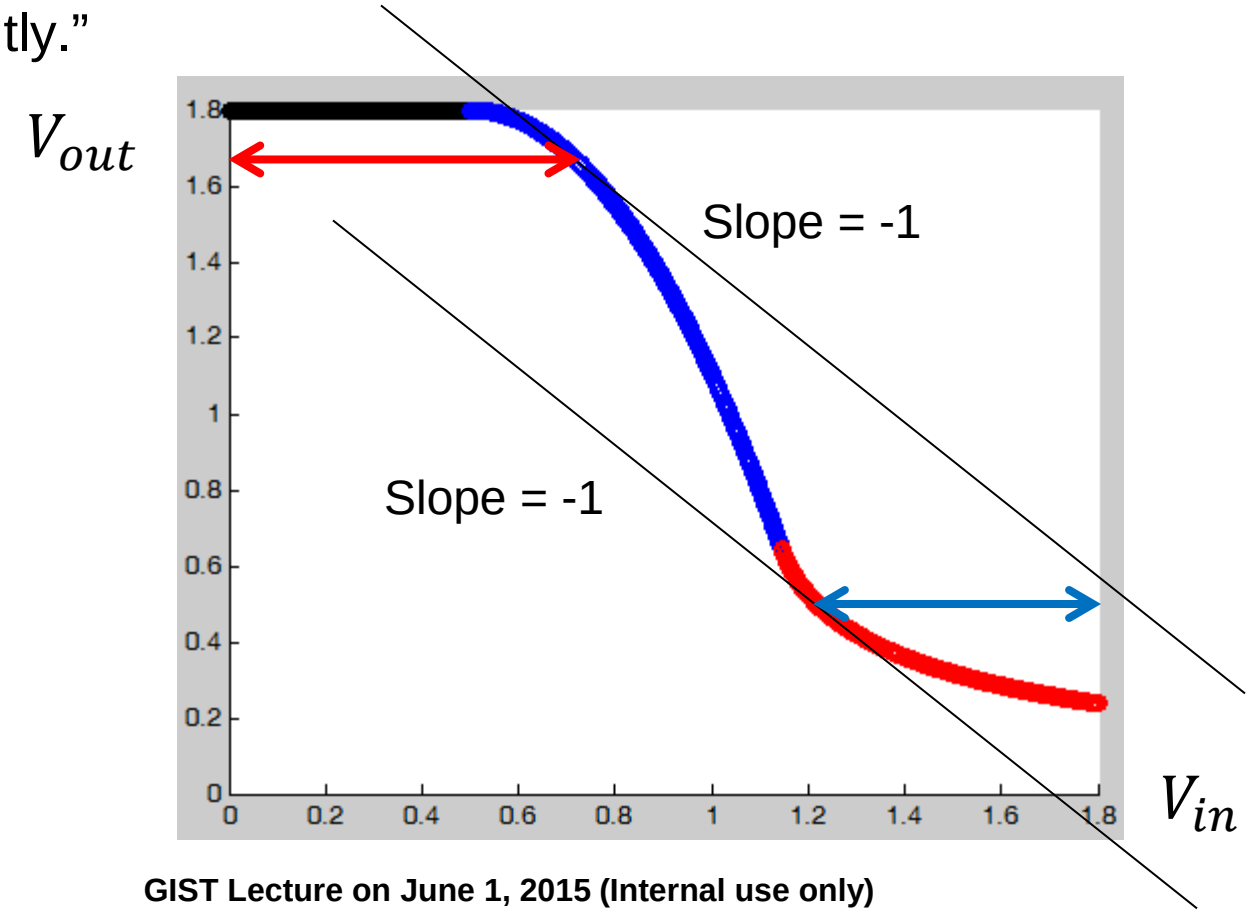
- Numeric calculation can be done with a binary system.
- Inverters and NAND gates are important.
- And, the NMOS inverter was introduced.





Noise margin

- Verbatim
  - “Noise margin is the maximum amount of degradation (noise) at the input that can be tolerated before the output is affected significantly.”



Noise margin of CS stage

- Let's calculate NM_L.
  - In this case,

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2$$

  - Taking the differentiation w. r. t. V_{in},

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})$$

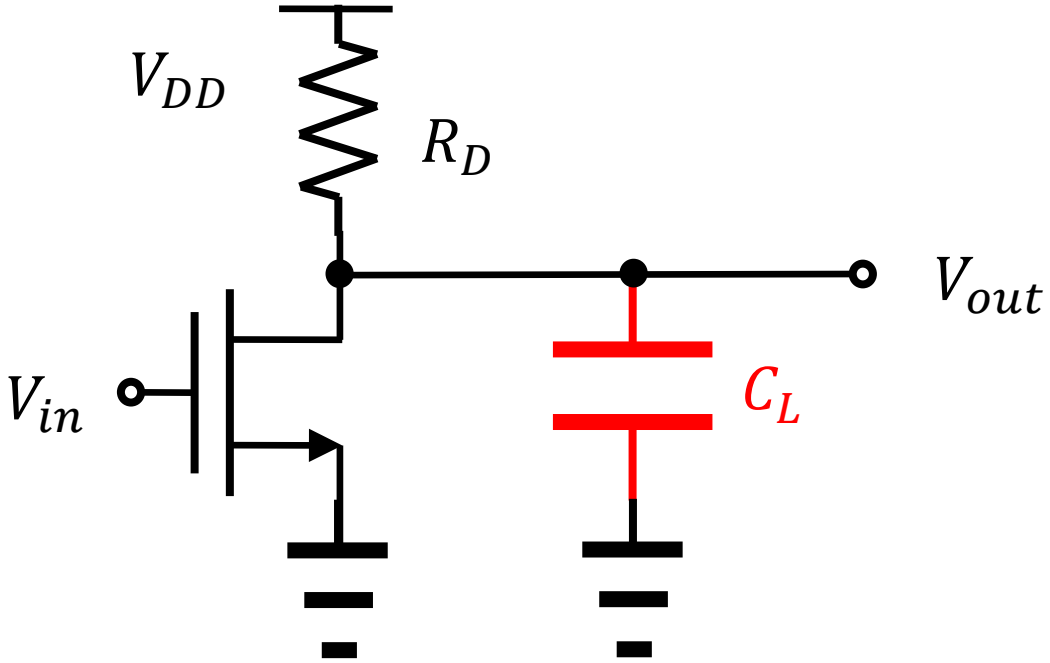
  - At $V_{in} = NM_L$, the slope becomes -1,

$$NM_L = \frac{1}{\mu_n C_{ox}\frac{W}{L}R_D} + V_{TH}$$

  - (Stronger NMOS yields a reduces NM_L.)

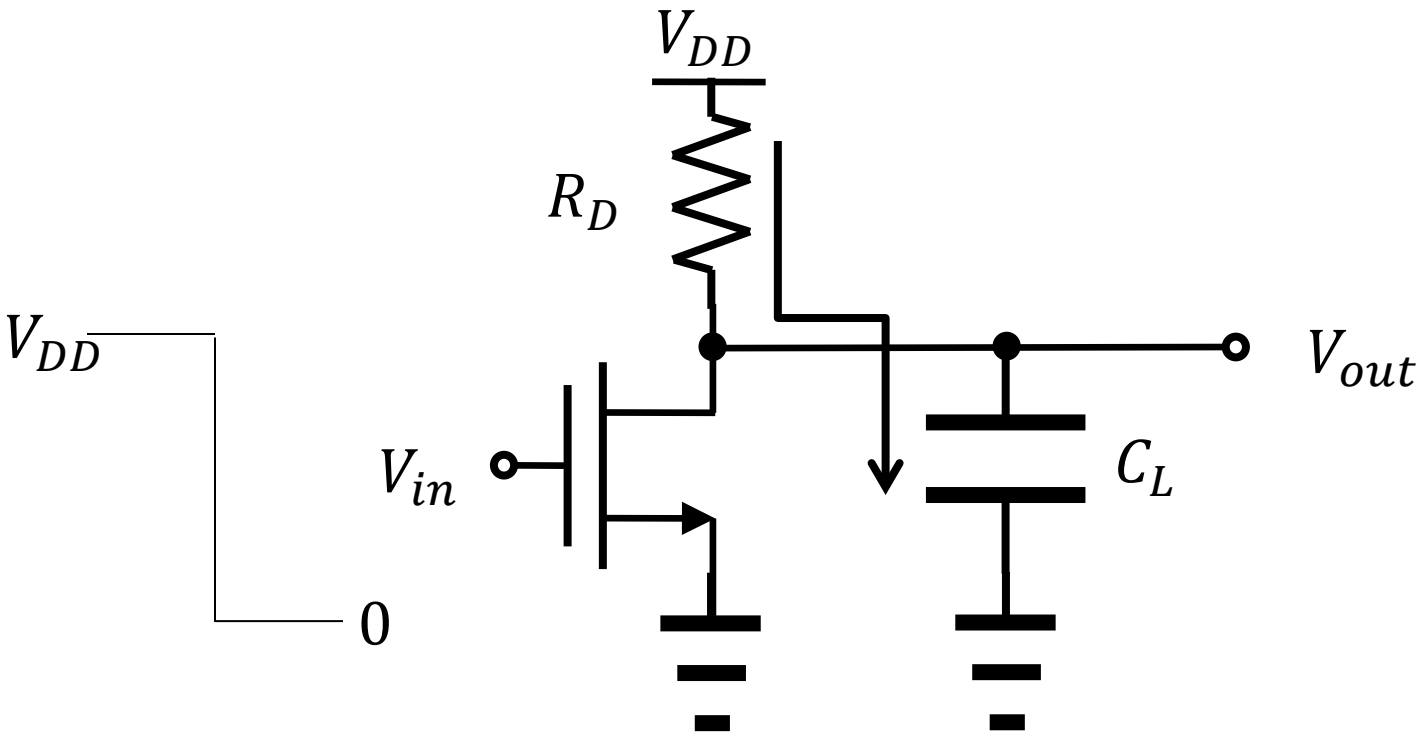
Speed of inverter (1/3)

- VTC merely describes the dc behavior.
  - Input voltages with different frequencies (1 kHz, 1 MHz, 1 GHz, 1 THz, …)
- Time-dependent behavior
  - Can a resistor introduce time-lagging effect?



Speed of inverter (2/3)

- A rapid transition of V_{in} from V_{DD} to 0
  - Then, the capacitor should be charged.
  - What is the electrical route to charge the capacitor?



Speed of inverter (3/3)

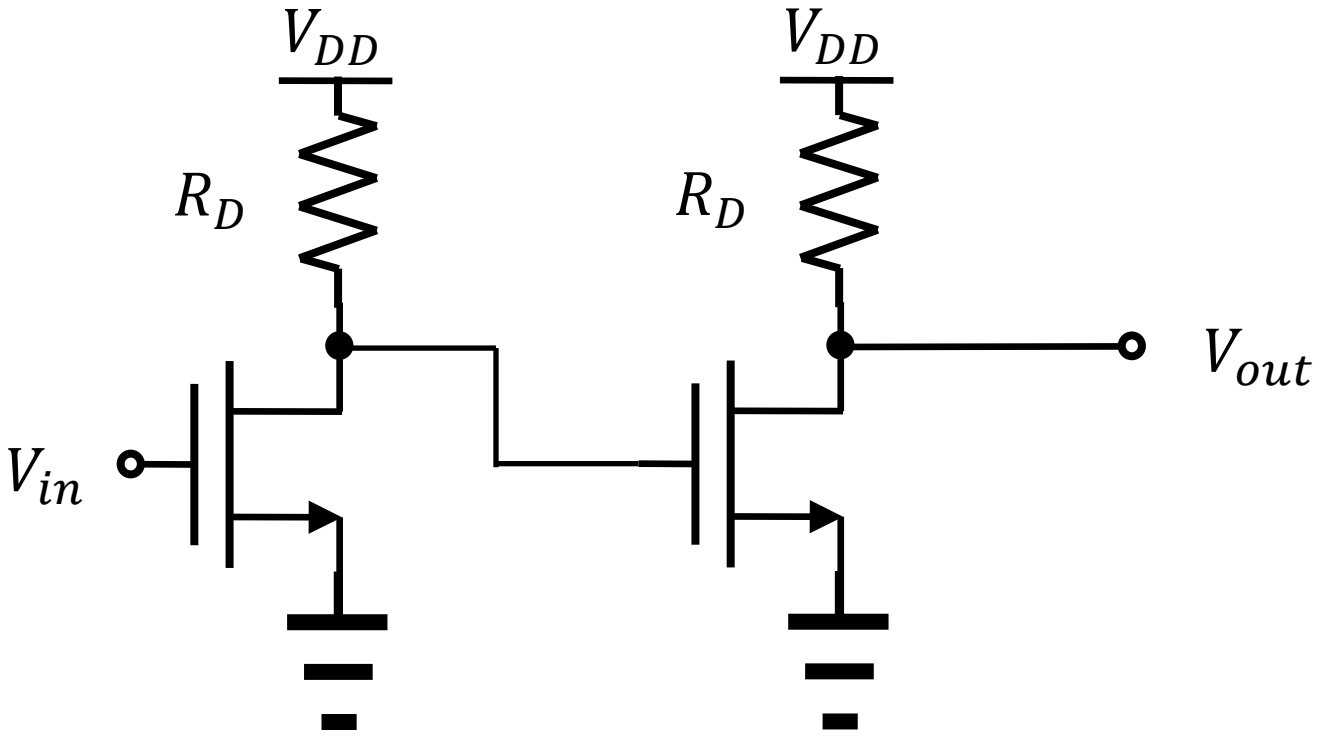
- Simply, it is a RC circuit.
  - Then, the solution is simply

$$V_{out}(t) = V_{out}(0^-) + [V_{DD} - V_{out}(0^-)]\left(1 - \exp\frac{-t}{R_D C_L}\right)$$

  - Since $\exp(-3) \approx 0.05$, after $3R_D C_L$, V_{out} reaches $0.95\ V_{DD}$.
  - Yes, it takes time to get the stable output voltage…

Origin of C_L?

- Consider an inverter chain.
  - Then, what is the load capacitance for the first stage?



- Another origin ➔ Interconnect

Standby(!) power

- The biggest problem in the NMOS inverter
  - When $V_{in} = 0$, no standby power
  - When $V_{in} = V_{DD}$, the power consumption is (approximately) $\frac{V_{DD}^2}{R_D}$.
  - If $V_{DD} = 1.8\ \mathrm{V}$ and $R_D = 10\ k\Omega$, 324 μW!

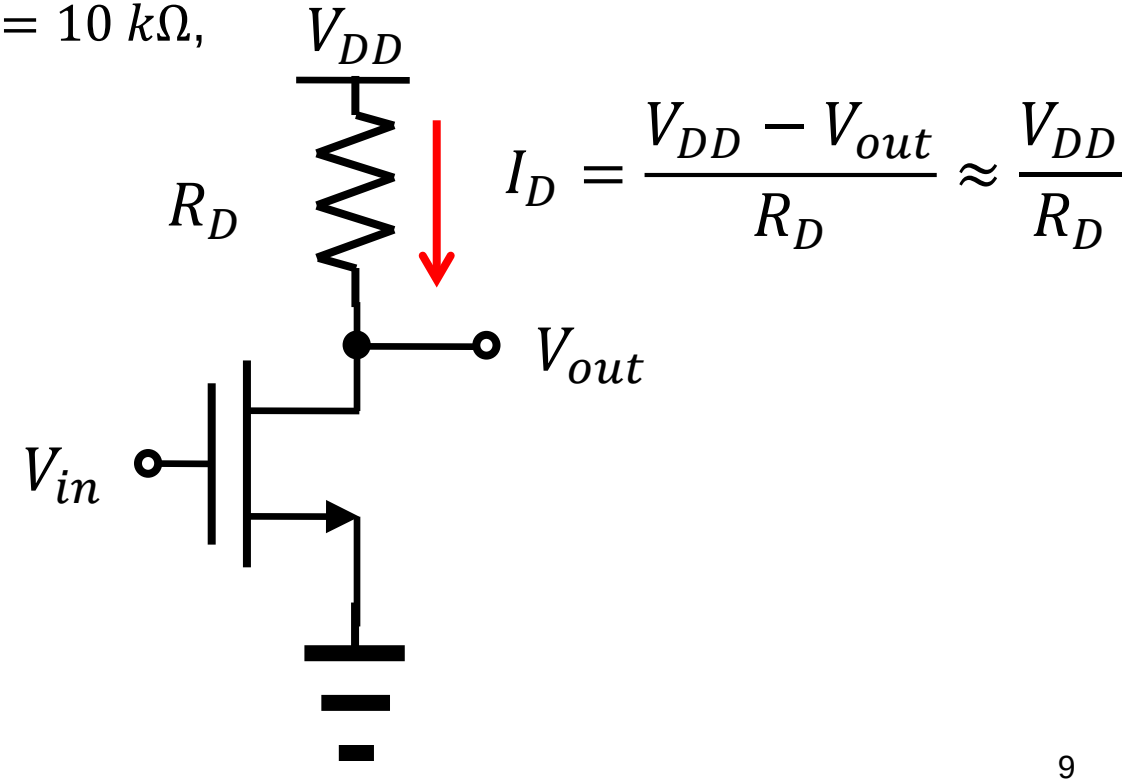


Figure 16.14

- Passive “pull-up” device
  - (a) Degradation of output level

    Too small R_D, when $V_{in} = V_{DD}$.

    In this case, large R_D is desirable.
  - (b) Risetime limitation

    Too small current for 1 ➔ 0 transition. ($V_{in} = 0$)

    In this case, a better capability to charge the C_L is desirable.
  - (c) Static power consumption

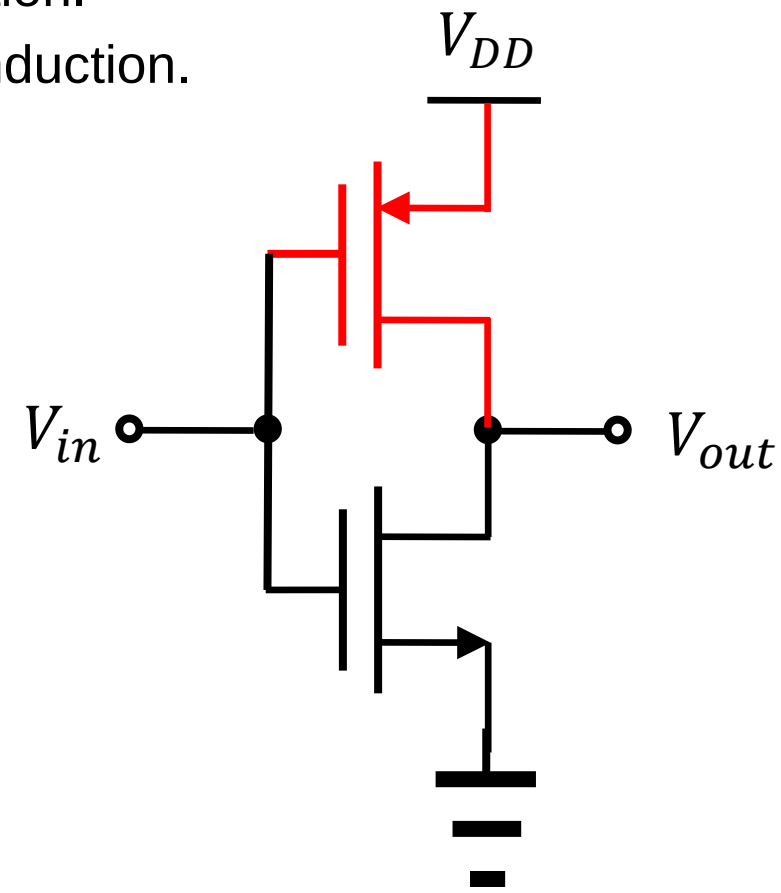
    No ability to block the current, when $V_{in} = V_{DD}$.

    In this case, no current conduction is desirable.
  - (a) & (c) ➔➔ (b)

CMOS inverter

- Ideal “pull-up” should have the following properties.
  - When $V_{in} = V_{DD}$, no current conduction.
  - When $V_{in} = 0$, improved current conduction.

- PMOS can do those jobs!



Draw it! (Homework#3)

- Only 1 problem
- Same parameters as before
  - $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$, $\mu_n C_{ox} = 75\ \mu\text{A/V}^2$, $V_{TH,n} = 0.5\ \text{V}$, $V_{TH,p} = -0.5\ \text{V}$, $\frac{W}{L} = \frac{10}{0.18}$, and $V_{DD} = 1.8\ \text{V}$
  - Using the computer, draw the voltage transfer curve.
- Due: June 3rd (This Wednesday!)