Mid-term examination

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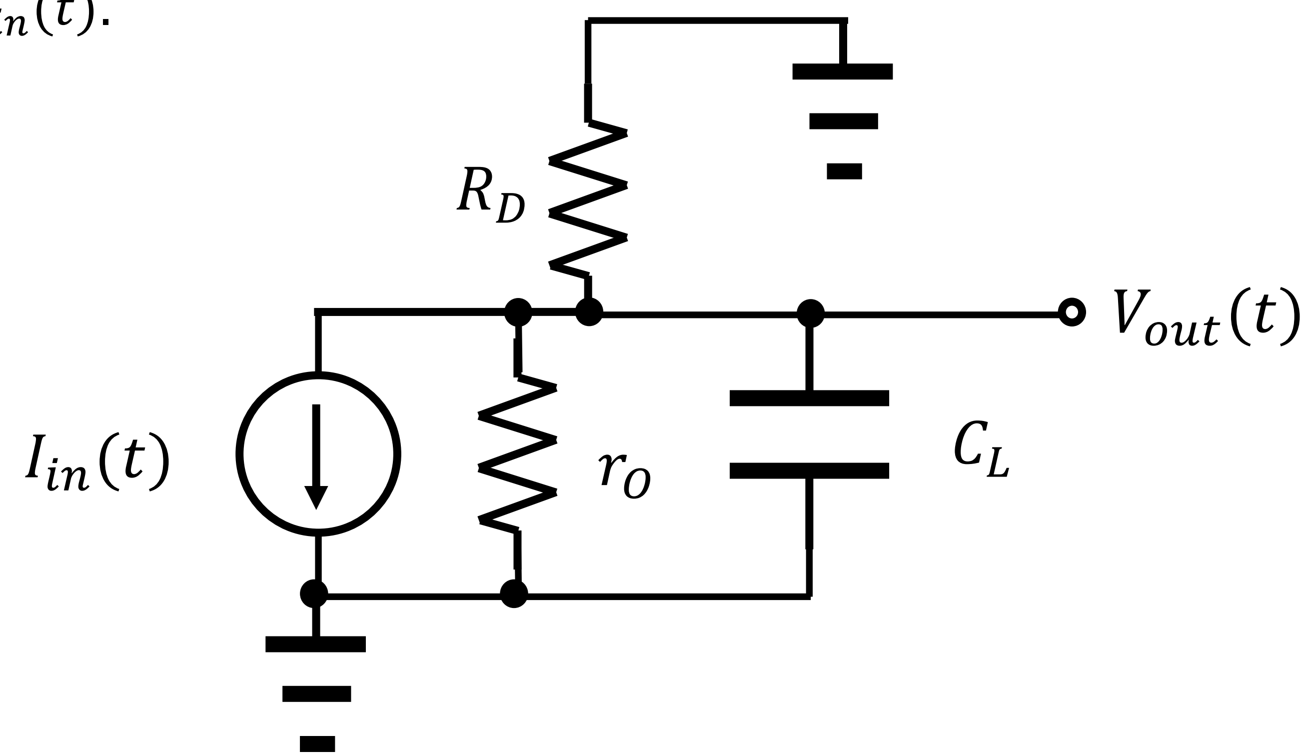
Problem1

- Circuit analysis:
  - Write down the Kirchhoff current law for the output node.
  - Solve the differential equation for the output voltage, $V_{out}(t)$.
  - Express the output voltage, $V_{out}(t)$, as a function of the input current, $I_{in}(t)$.



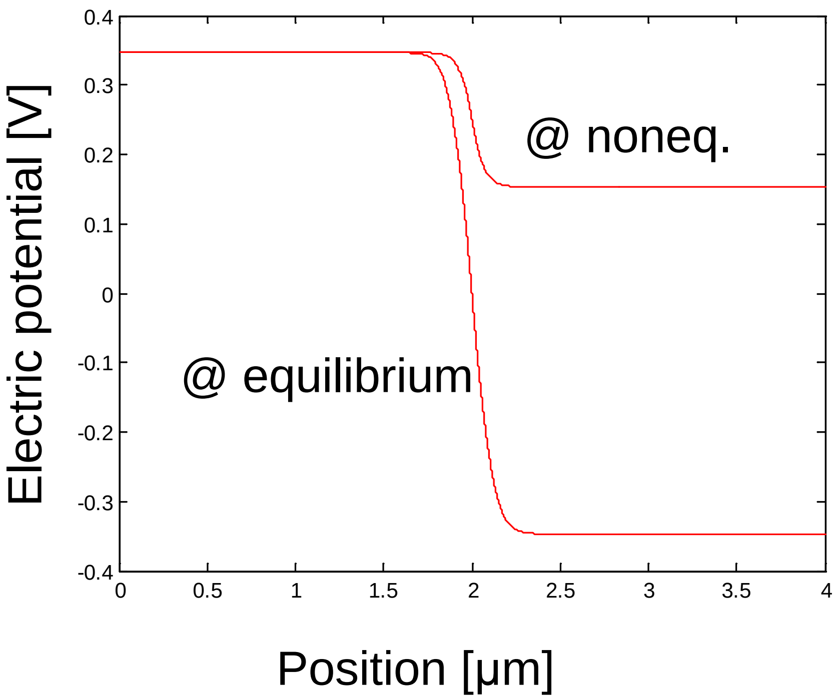
Problem2

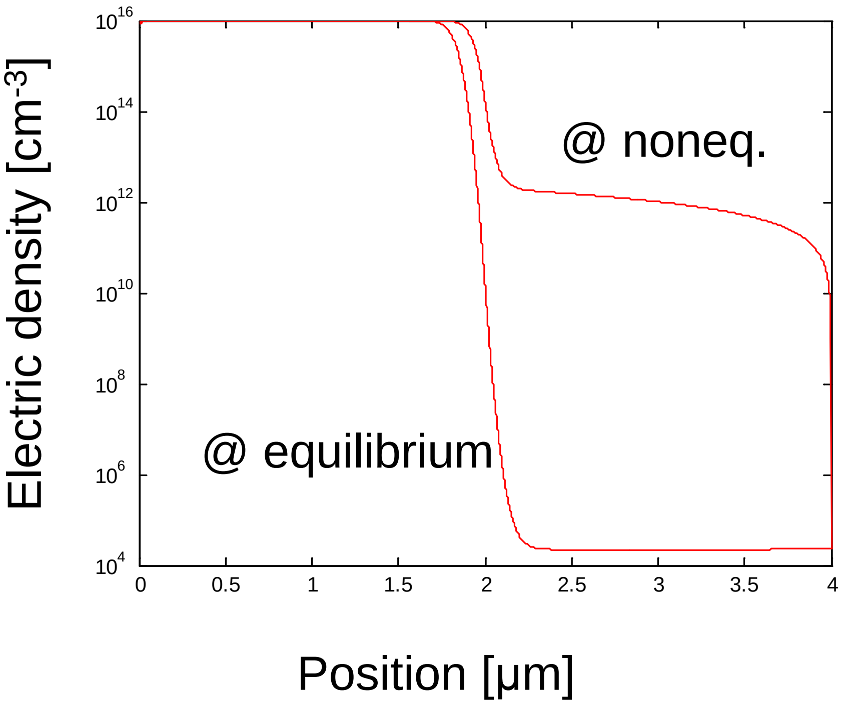
- Properties of semiconductors
  - Answer “Yes” or “No” for the following five statements.

  - 1. Only semiconductors have the band gap.
  - 2. The intrinsic carrier density of silicon increases exponentially as the temperature increases.
  - 3. The relation of $np = n_i^2$ must be valid everywhere for a pn junction at equilibrium.
  - 4. A doping density of 10^{10} cm^{-3} is a relatively high doping density.
  - 5. The Einstein relation between the mobility and the diffusion constant holds only at equilibrium, in a rigoruous sense.

Problem3

- Biased pn junction
  - 1. Where is the p-type region? Where is the n-type region?
  - 2. From two figures below, estimate the bias condition. Is it forward-biased or reverse-biased? What is the applied bias?





Problem4

- Forward-biased pn junction
  - The electron density at the boundary between the p-type region and the depletion region is given by

$$n_p = n_{p0} \exp \frac{V}{k_B T/q}$$

  - Also, at the end of the p-type region, $n_p = n_{p0}$. (n_{p0} is a constant.)
  - The hole density at the boundary between the n-type region and the depletion region is given by

$$p_n = p_{n0} \exp \frac{V}{k_B T/q}$$

  - Also, at the end of the n-type region, $p_n = p_{n0}$. (p_{n0} is a constant.)
  - Length of p-type region and n-type region is L_p and L_n, respectively.
  - Assuming linear variation of n_p and p_n, calculate the diffusion current density.

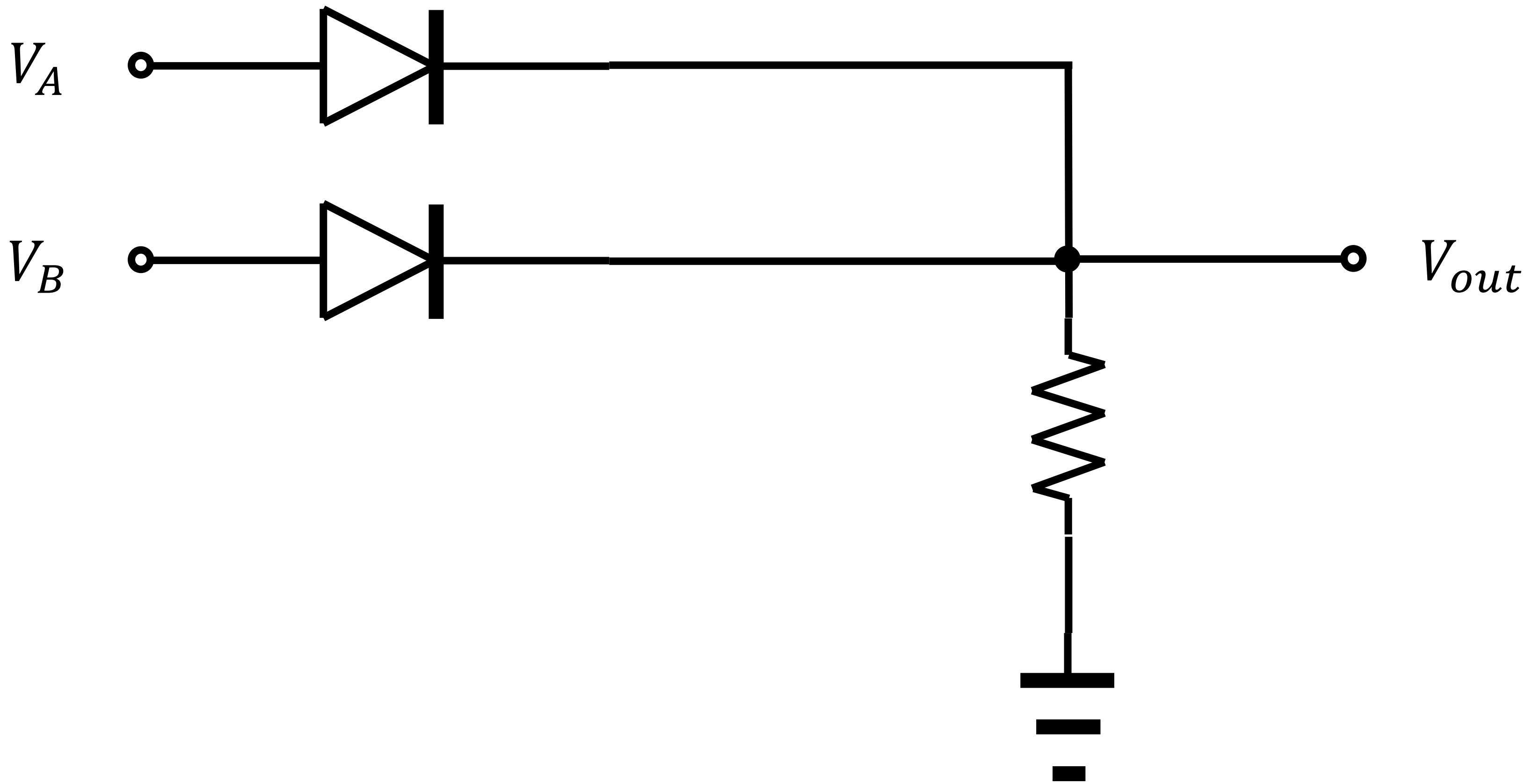
Problem5

- Constant voltage model
  - 1. Show explicitly that:
  - For a forward-biased diode, only a small change of the diode voltage is required for increasing the diode current by a factor of 10.
  - (You may use $\log 10 \approx 2.3$)

  - 2. When we increase the diode voltage by 0.3 V, what is the increaing ratio of the diode current?

Problem6

- OR gate
  - 1. Explain that the following circuit can be seen as an OR gate (approximately).
  - 2. Write down expected drawbacks of the circuit.



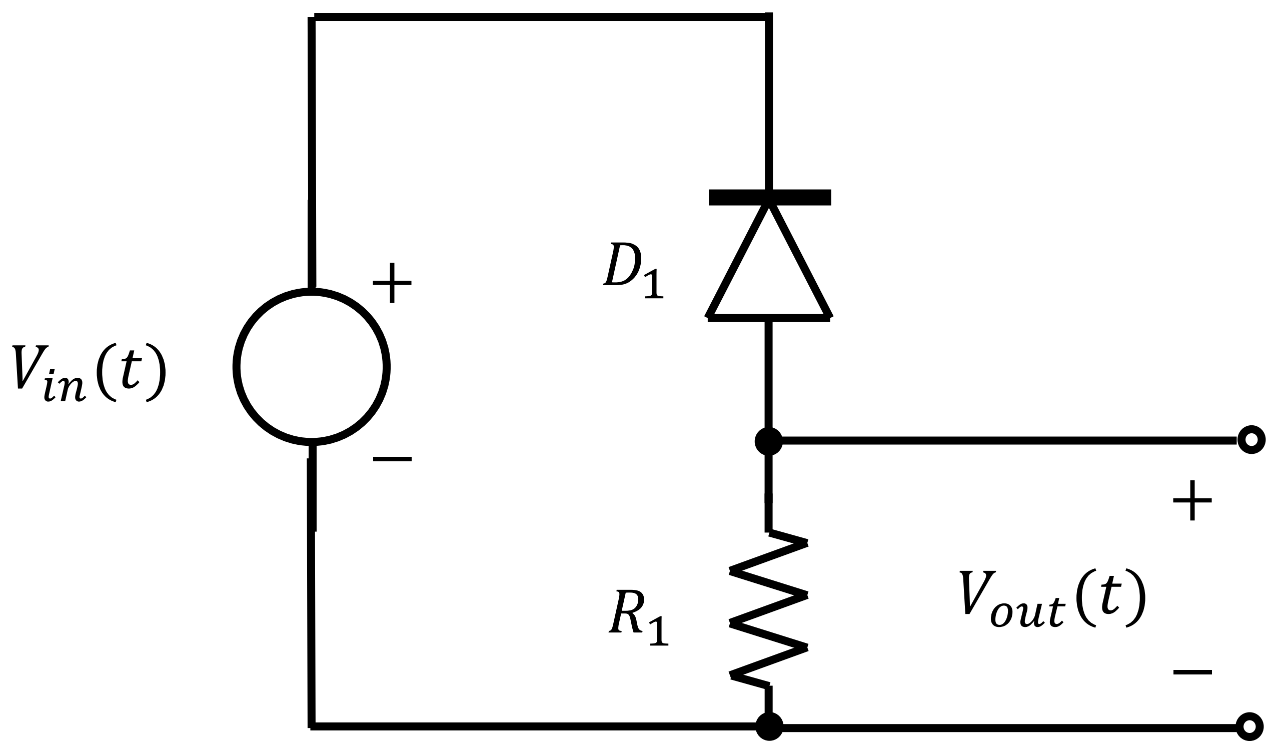
Problem7

- Small-signal model
  - 1. Les us describe the IV characteristic of a pn diode as $I = I_s\left(\exp\frac{V}{k_B T/q} - 1\right)$. A dc bias voltage, V_{dc}, is applied. Then, calculate the equivalent small-signal resistance.

  - 2. Now, consdider a device whose IV charactierstic is given as $I = K(V_0 V - \frac{1}{2}V^2)$. Here, K and V_0 are constants. A dc bias voltage, V_{dc}, is applied. Then, calculate the equivalent small-signal resistance.

Problem8

- A diode-resistor circuit, $V_{in}(t) = +3 + 0.001 \sin \omega t$
  - 1. Qualitatively explain its inout-output charactersitic.
  - 2. When the (angular) frequency becomes higher, qualitatively describe the behavior of $V_{out}(t)$.



Problem9

- A circuit
  - 1. Qualitatively explain its inout-output charactersitic.
  - 2. Solve the system exactly. (You may use $I = I_s \exp \frac{V}{k_B T/q}$.)