Lecture10: MOSFET

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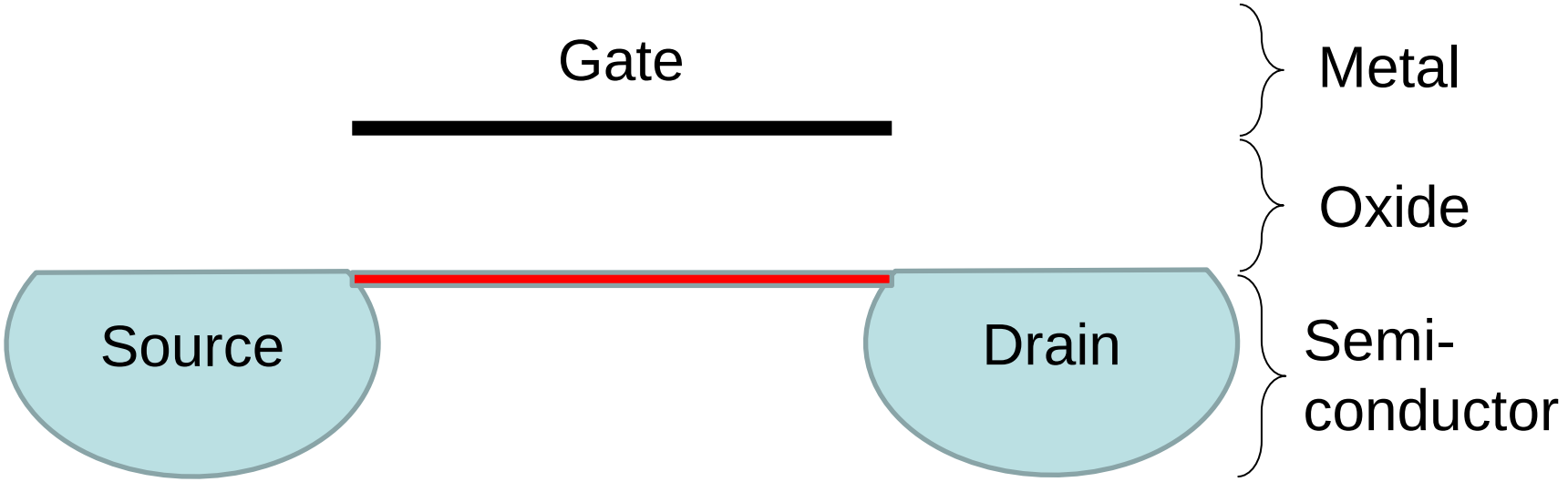
MOS? MOSFET?

- MOS (Metal-Oxide-Semiconductor)
  - By changing the gate voltage, the charge density can be controlled.
- MOSFET (MOS Field-Effect Transistor)
  - Current conduction

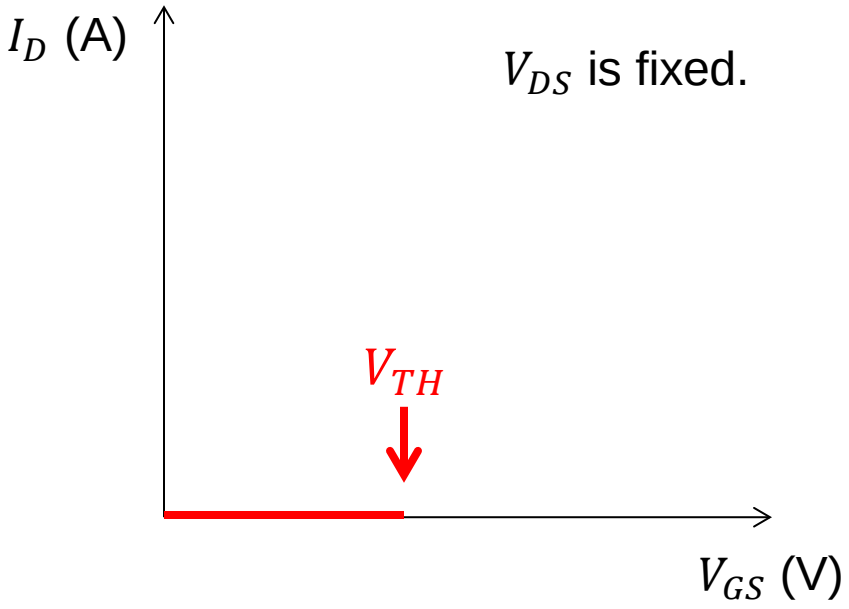


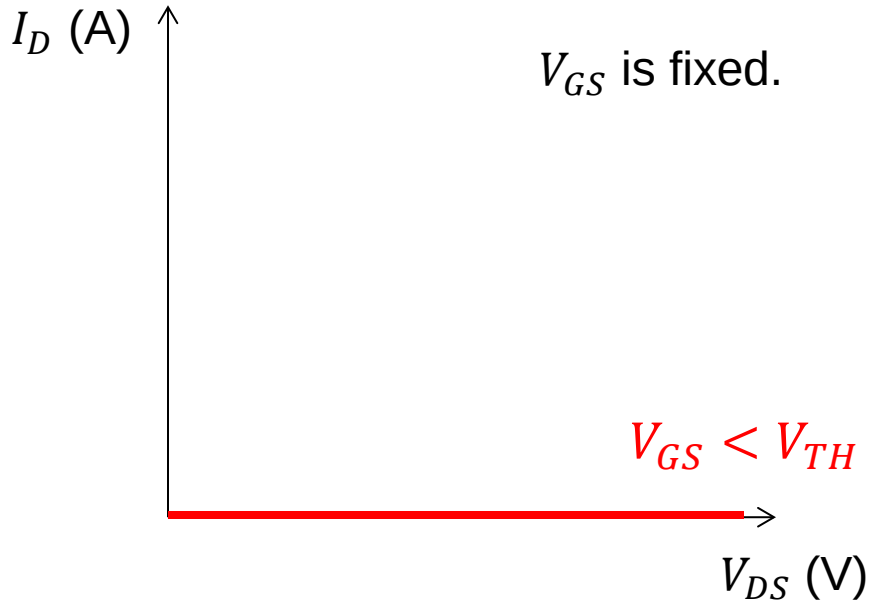
Its operation

- The MOSFET has three terminals.
  - Source, drain, and gate
  - We always have
$$I_S(t) + I_D(t) + I_G(t) = 0.$$
- At low frequencies, the gate current is zero.
  - Source current + drain current = 0, $I_S + I_D = 0$
  - Source is regarded as the reference contact.
  - Gate voltage (V_{GS}) and drain voltage (V_{DS}) are variables.
- We are interested with $I_D(V_{GS}, V_{DS})$.

IV characteristics

- We will draw the two graphs.
  - $I_D(V_{GS})$ with fixed V_{DS} & $I_D(V_{DS})$ with fixed V_{GS}





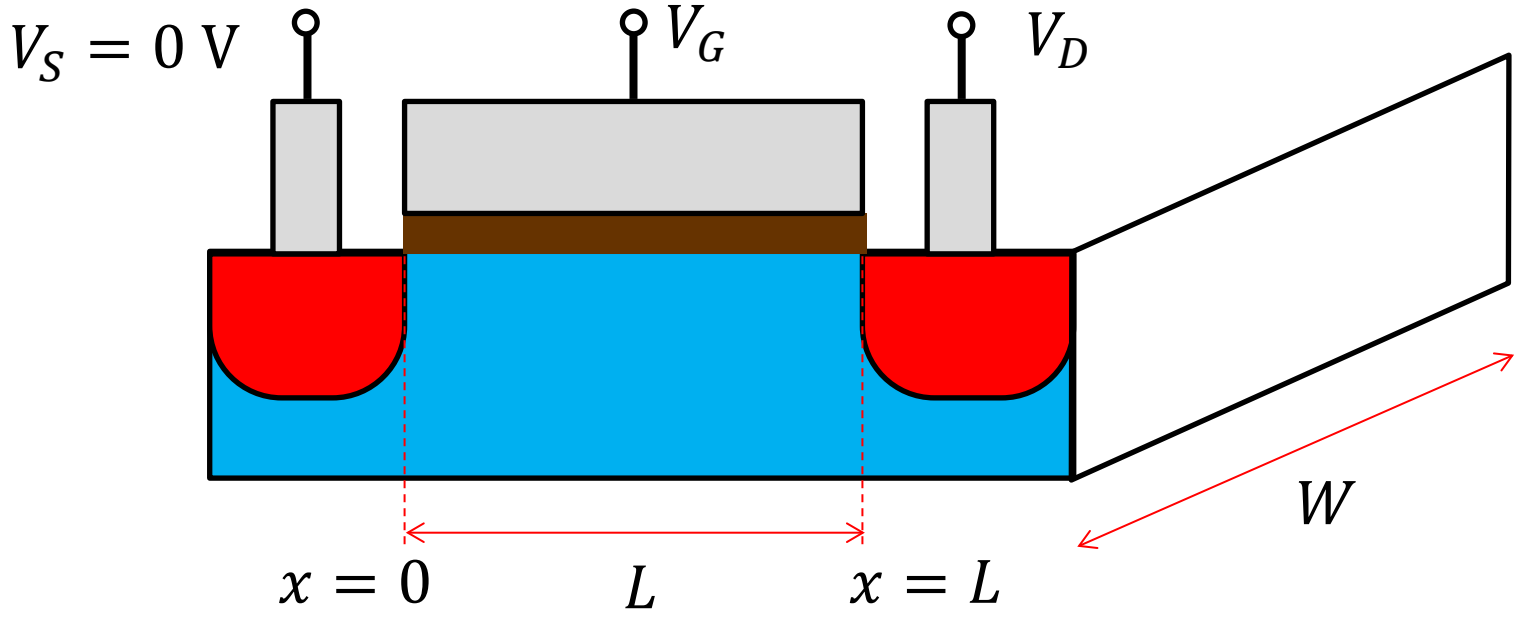
Drain current

- It is easy to guess that
  - When $V_{GS} < V_{TH}$, no drain current is allowed.
$$I_D = 0$$
  - When $V_{GS} > V_{TH}$,
$$I_D \propto C_{ox}(V_{GS} - V_{TH})$$

- In this lecture, we derive an appropriate expression for I_D.

Device structure

- Two-dimensional cross-section
  - "Potential" can be dependent on the position, $V(x)$.



Derivation of IV (1)

- Drain current
  - Q_{elec} is the electron charge density *per unit length*.
  - It follows

$$Q_{elec} = W C_{ox}[V_G - V(x) - V_{TH}] \qquad \text{(Razavi 6.3)}$$

  - At a certain position of x, the current is given by

$$I(x) = Q_{elec}(x)\, v(x) \qquad \text{(Razavi 6.4)}$$

  - Also v is the electron velocity.

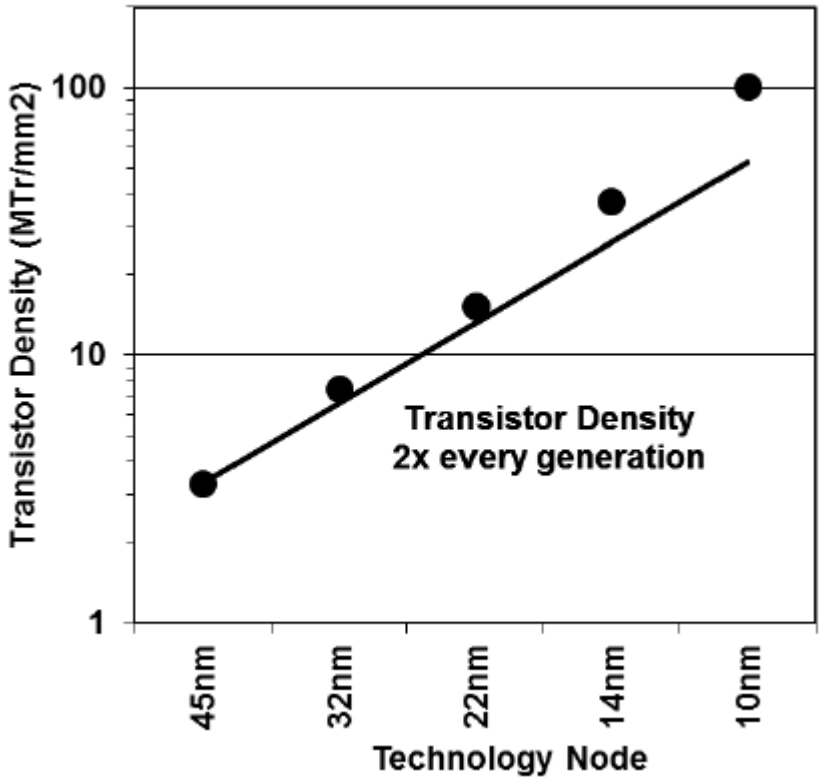
$$v = -\mu_n E = +\mu_n \frac{dV}{dx} \qquad \text{(Razavi 6.5 and 6.6)}$$

Homework#5 (1)

- Due: 09:00, April 8 (Mon)
- (Many problems in the previous mid-term are your own exercise. Not for HW)
- In HW#5, an IEDM paper by C. Auth et al. is studied.
  - All graphs are taken from that paper.

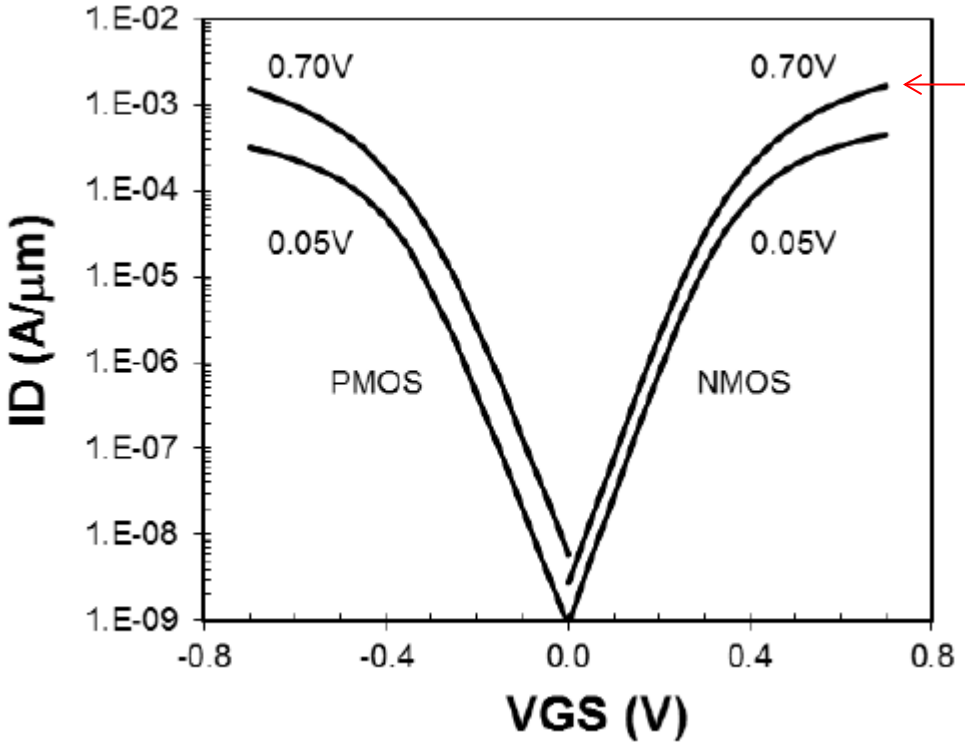
Homework#5 (2)

- P1
  - The graph shows the logic transistor density.
  - Compared with the 45nm node, how much is the 10 nm improved, in terms of the transistor density?



Homework#5 (3)

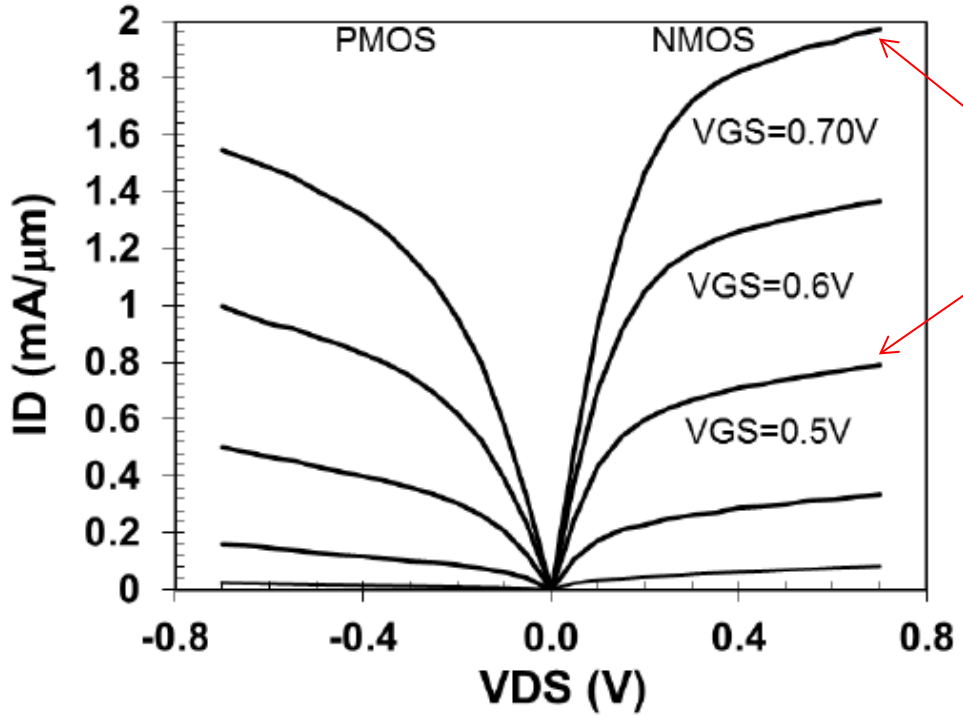
- P2
  - The graph shows the $I_D - V_{GS}$ curve in the semi-log scale.
  - Estimate the ratio between $I_D(V_{GS} = 0.7\ \mathrm{V}, V_{DS} = 0.7\ \mathrm{V})$ and $I_D(V_{GS} = 0.0\ \mathrm{V}, V_{DS} = 0.7\ \mathrm{V})$.



Use this curve.

Homework#5 (4)

- P3
  - The graph shows the $I_D - V_{DS}$ curve. (I_D is normalized with W.)
  - Consider a device with $W = 100\ \mathrm{nm}$.
  - Calculate the drain currents, $I_D(V_{GS} = 0.7\ \mathrm{V}, V_{DS} = 0.7\ \mathrm{V})$ and $I_D(V_{GS} = 0.5\ \mathrm{V}, V_{DS} = 0.7\ \mathrm{V})$.



Use these curves.