Final examination

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Information and Communications
Gwangju Institute of Science and Technology

Welcome!

- Total nineteen (15) problems
  - Five (5) minutes for each problem
  - 75 minutes long

- Policy
  - No cellphone!
  - No calculator!
  - No question!

- Recommendation
  - Prepare your answer sheets. (Write down your name.)

Problem1

- Saturation current of an NMOSFET is shown below.
  - Using the MOSFET IV model studied in the course, specify the following parameters: V_{TH} and $\mu_n C_{ox} \frac{W}{L}$
  - Neglect the channel-length modulation.

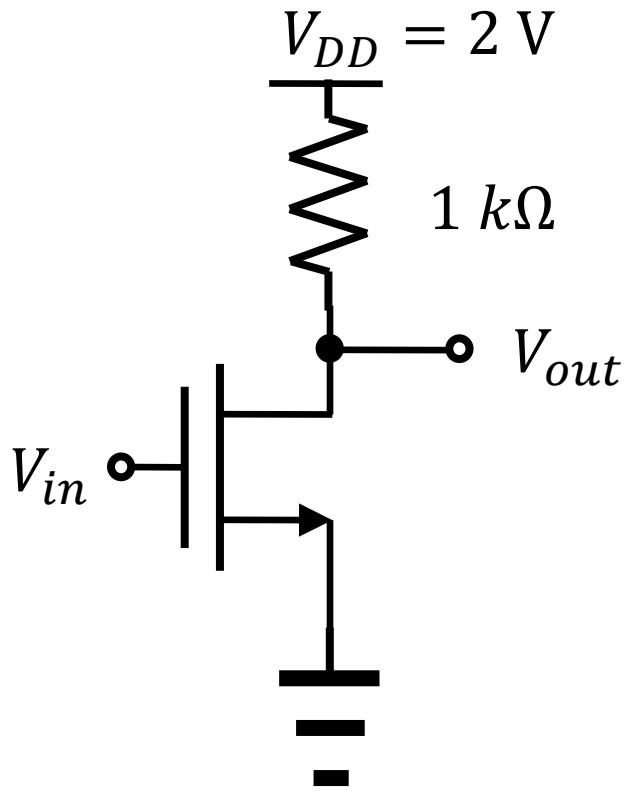
V_{GS} [V]	I_D [mA]
0.5	0.05
1.0	1.8
1.5	6.05
2	12.8

Problem2

- Use the IV curve shown in Problem1.
  - When we set the dc bias point as $V_{GS} = 1.0\ \mathrm{V}$ and $V_{DS} = 1.0\ \mathrm{V}$, draw the small-signal model with the numerical values. Neglect the channel-length modulation.

Problem3

- The same MOSFET is used in the CS amplifier.
  - Assume the dc gate voltage is $0.8\ \mathrm{V}$.
  - Calculate the voltage gain for a load resistance of $1\ \mathrm{k\Omega}$.
  - Repeat it with a load resistance of $1\ \mathrm{M\Omega}$.

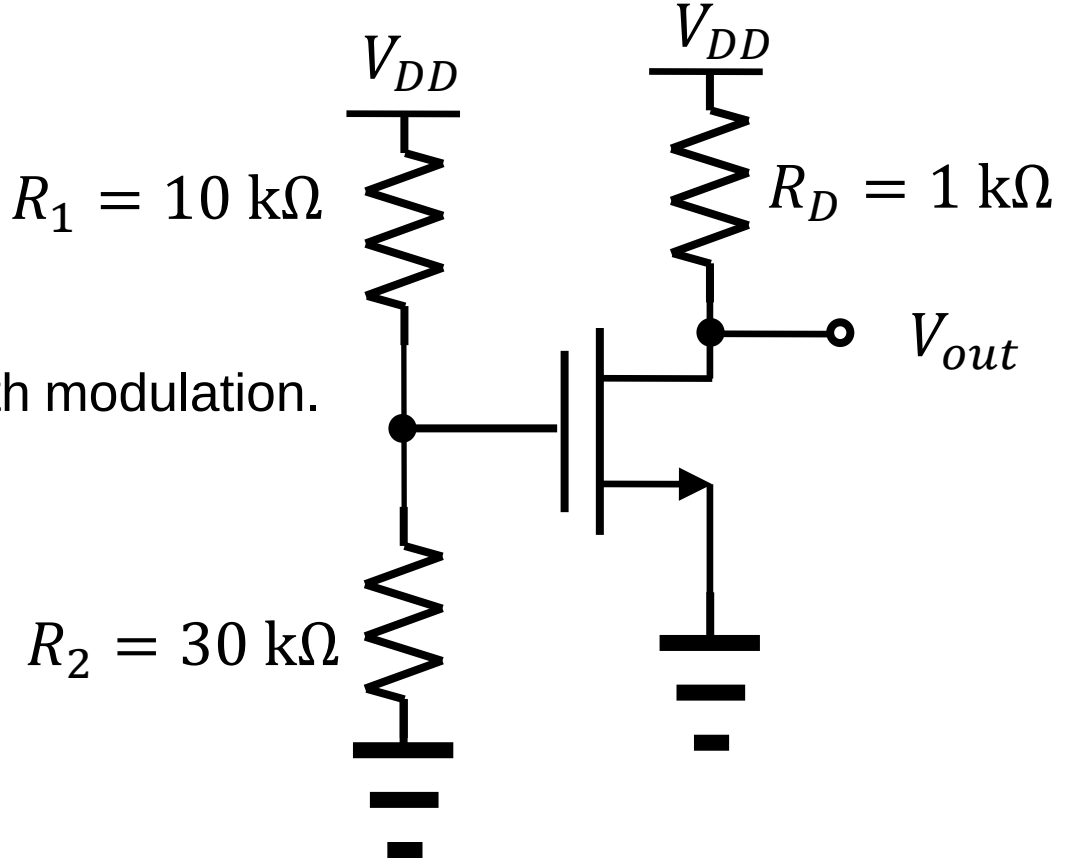


Problem4

- Calculate the dc V_{out} of the following circuit.
  - For the calculation, use the following parameters:

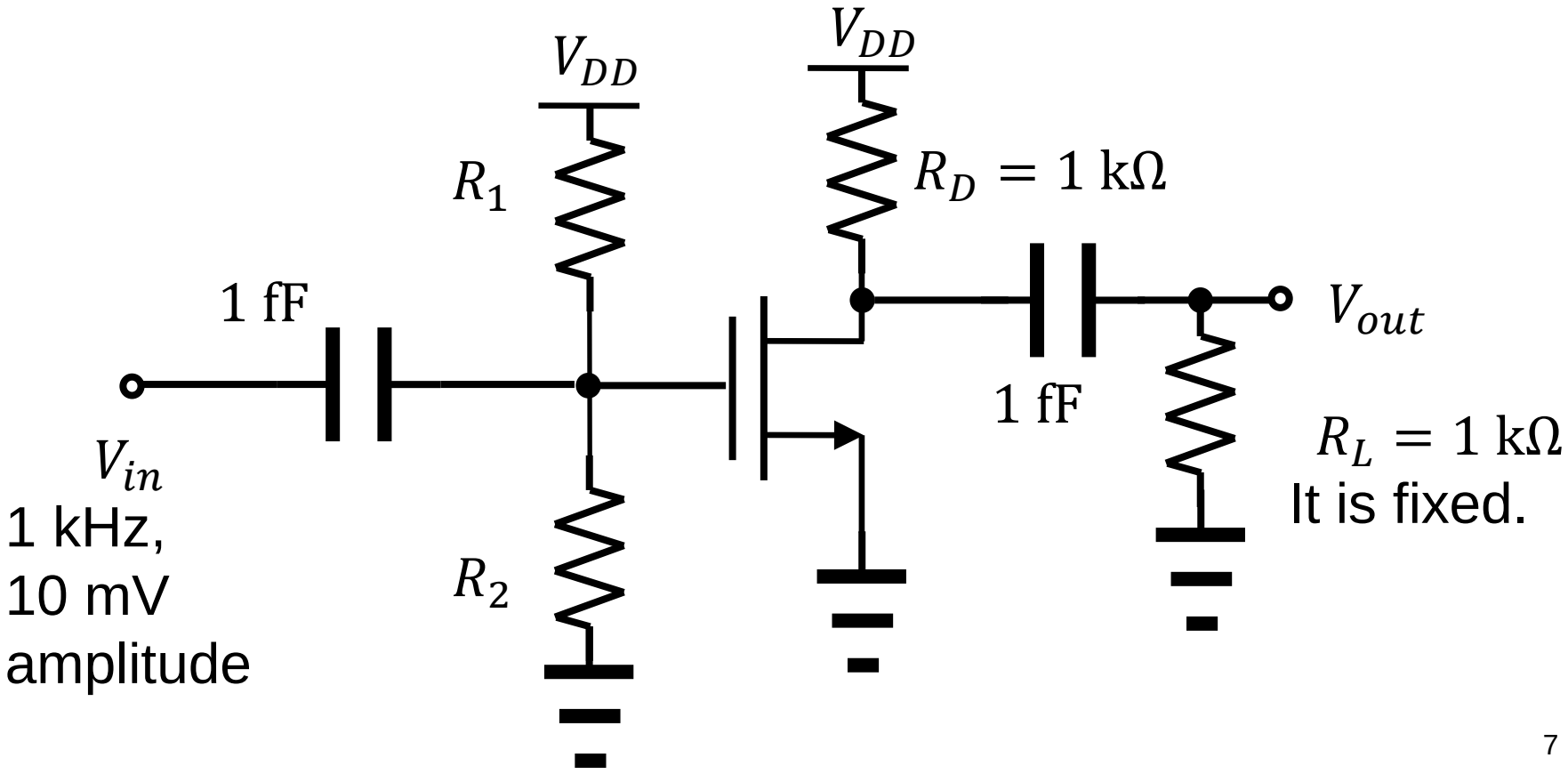
$V_{DD} = 2\ \mathrm{V}$
$\mu_n C_{ox} = 100\ \mu\mathrm{A/V^2}$
$V_{TH} = 0.5\ \mathrm{V}$
$\frac{W}{L} = \frac{10}{0.5}$

  - Neglect the channel-length modulation.



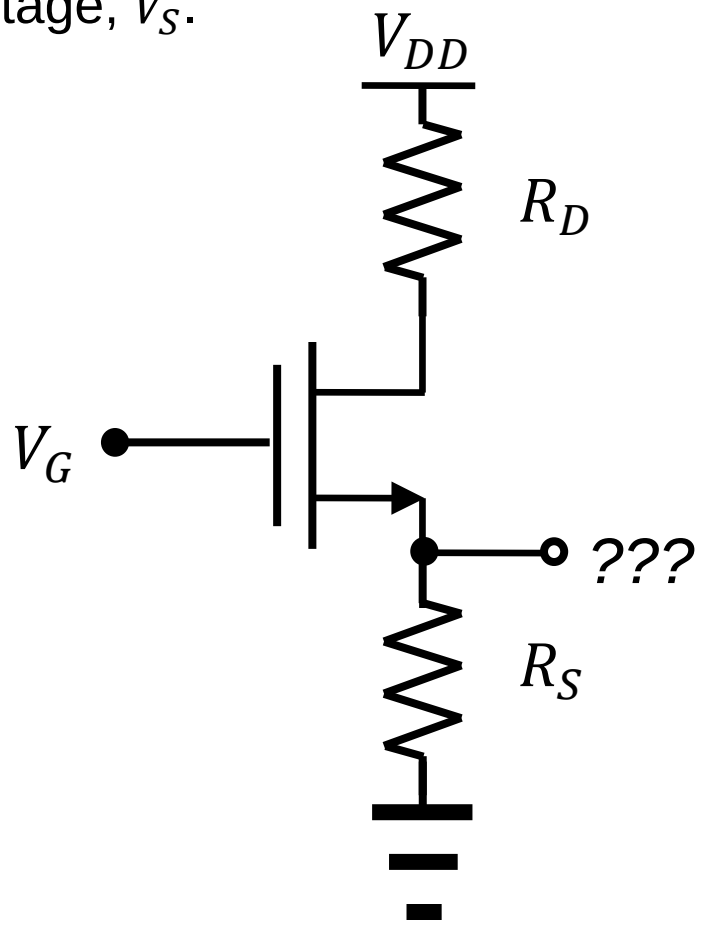
Problem5

- For the same circuit, an input signal with 1 kHz is applied.
  - Unfortunately, the following circuit does not work properly.
  - Fix the problem, and calculate the output amplitude.



Problem6

- Consider a source-degenerated CS stage.
  - Derive the expression of the source voltage, V_S.
  - Neglect the channel-length modulation



Problem7

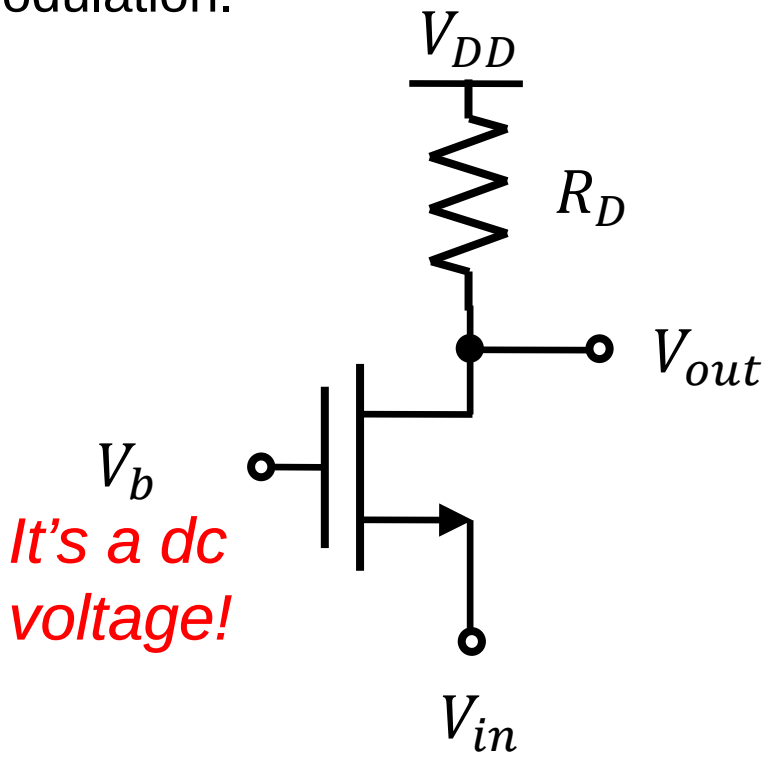
- Consider a source-degenerated circuit.
  - In the lecture, we have studied the voltage gain of the source-degenerated CS amplifier, $A_v = -\frac{g_m R_D}{1+g_m R_S}$.
  - In this problem, derive the voltage gain with the channel-length modulation.

Problem8

- Draw the small-signal model of a source-degenerated CS stage.
  - Derive the output resistance.
  - Include the channel-length modulation.

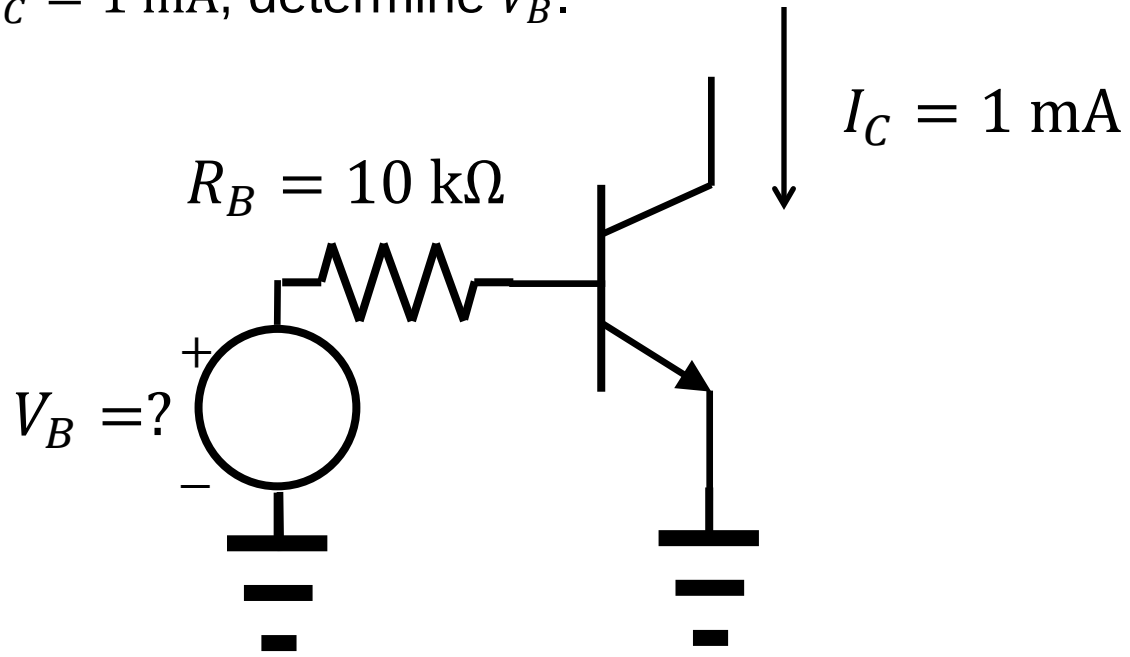
Problem9

- The common-gate stage shown below must provide a voltage gain of 4 and an input impedance of $50\ k\Omega$.
  - Determine the values of g_m and R_D.
  - Neglect the channel-length modulation.



Problem10

- Consider a circuit shown below.
  - Assume $\beta = 100$.
  - In the BJT, $I_S = 10^{-15}$ A. Also use the approximate relation, $\exp\frac{60\text{ mV}}{V_T} \approx 10$.
  - When $I_C = 1$ mA, determine V_B.

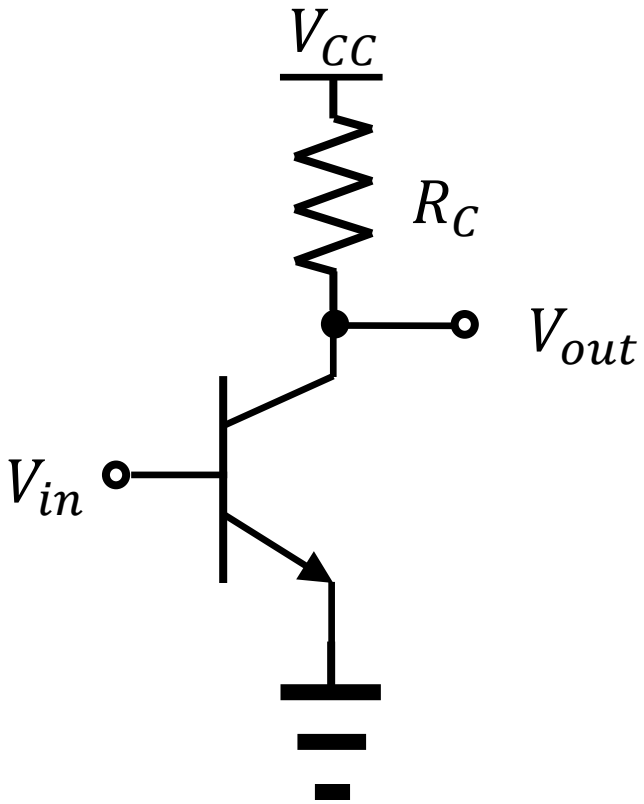


Problem11

- Compare the channel-length modulation (MOSFET) and the Early effect (BJT).
  - Explain the physical mechanisms to give such effects.

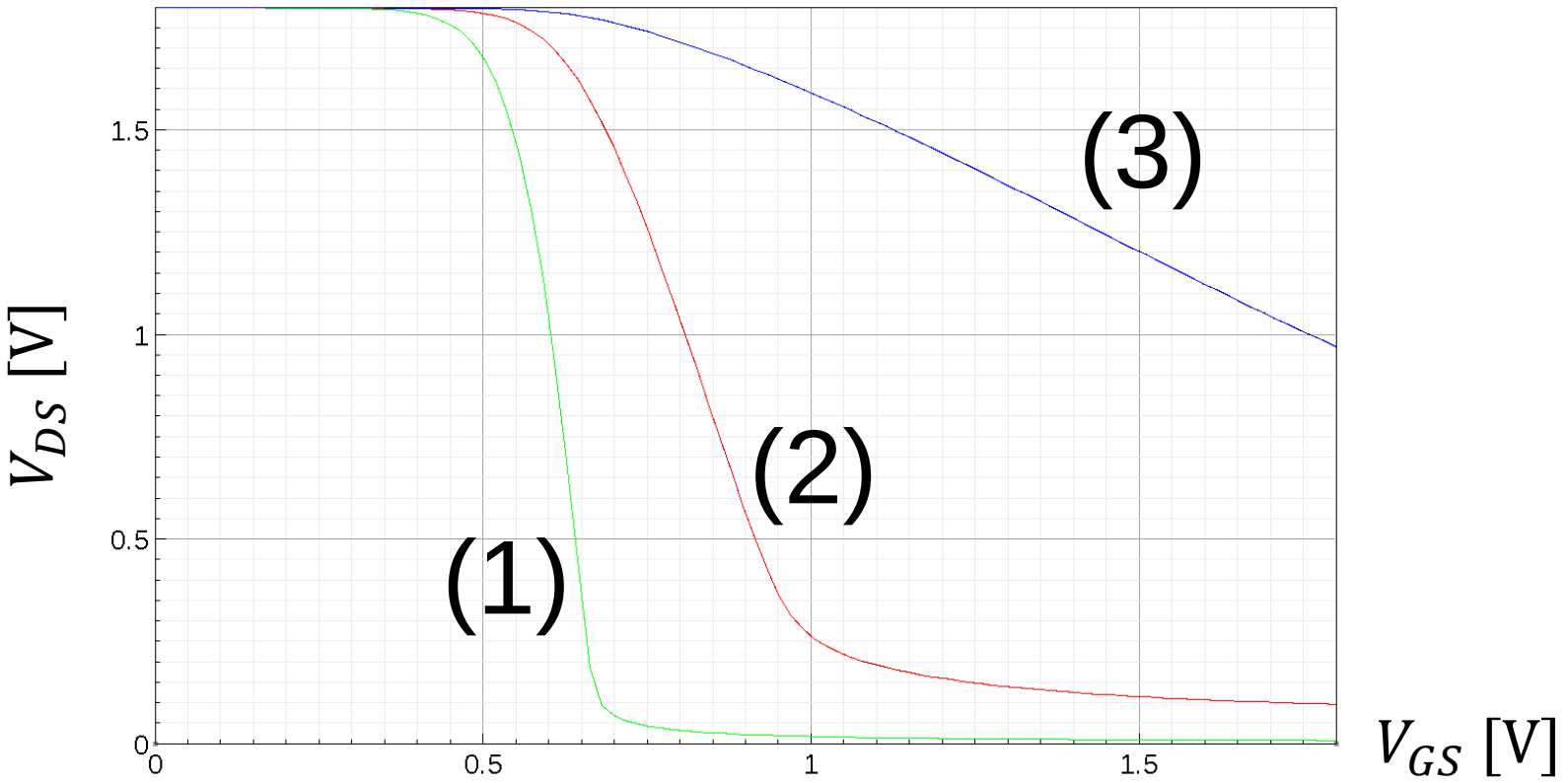
Problem12

- Consider a common-emitter amplifier.
  - Draw the small-signal model.
  - Show that the voltage gain becomes insensitive to I_C, when we have a very large R_C.



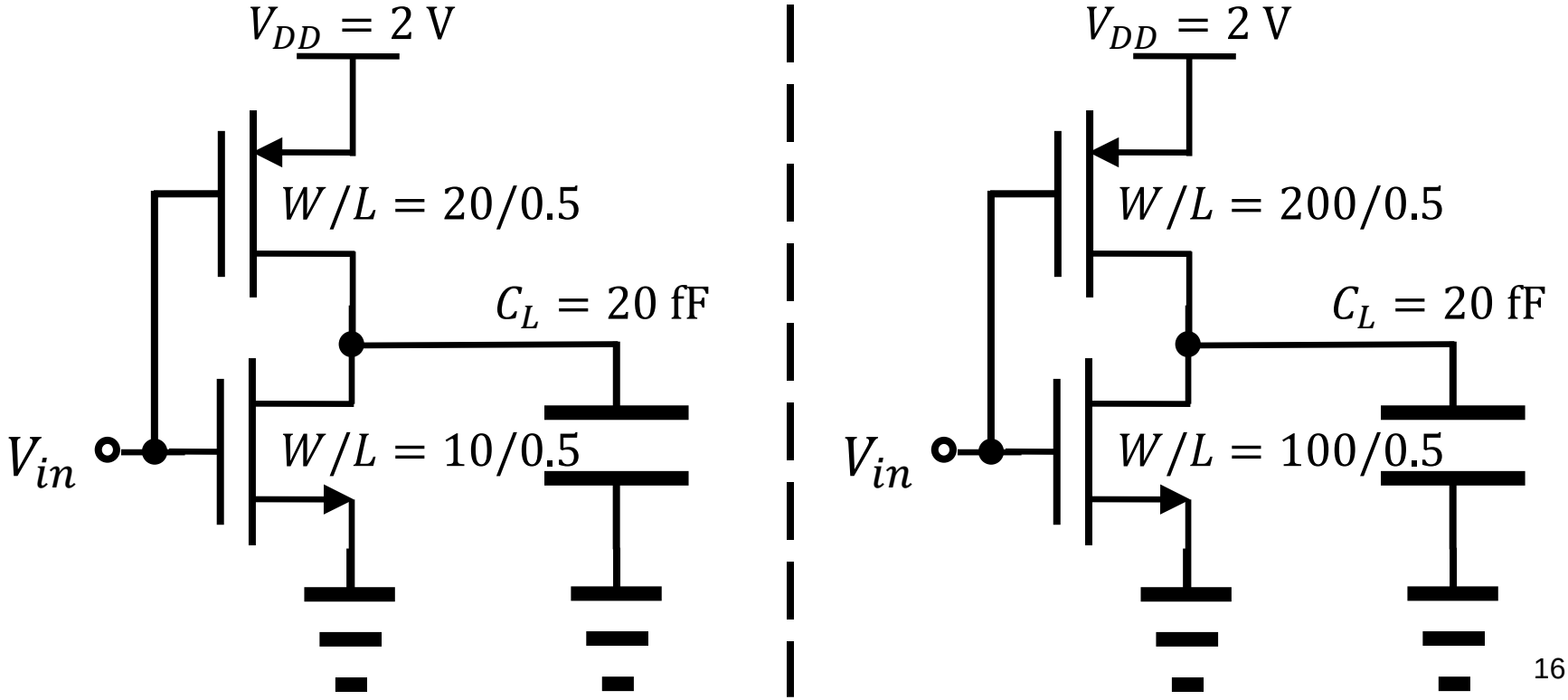
Problem13

- Voltage transfer curves of NMOS inverters are shown.
  - Three different drain resistances are used.
  - Select the curve with the highest drain resistance.
  - Explain the reason.



Problem14

- Two CMOS inverters are operated under the periodic input clock signal. They differ only in the device size.
  - The clock frequency is very low, just $1\ \mathrm{kHz}$.
  - Calculate the dynamic power dissipation of two inverters.



Problem15

- Consider CMOS NOR and NAND gates.
  - For simplicity, each of them has only two input variables.
  - Assume that the size of each MOSFET is the same for both gates. Which gate is faster? Explain the reason.