Lecture25:
Bipolar junction transistors (3)

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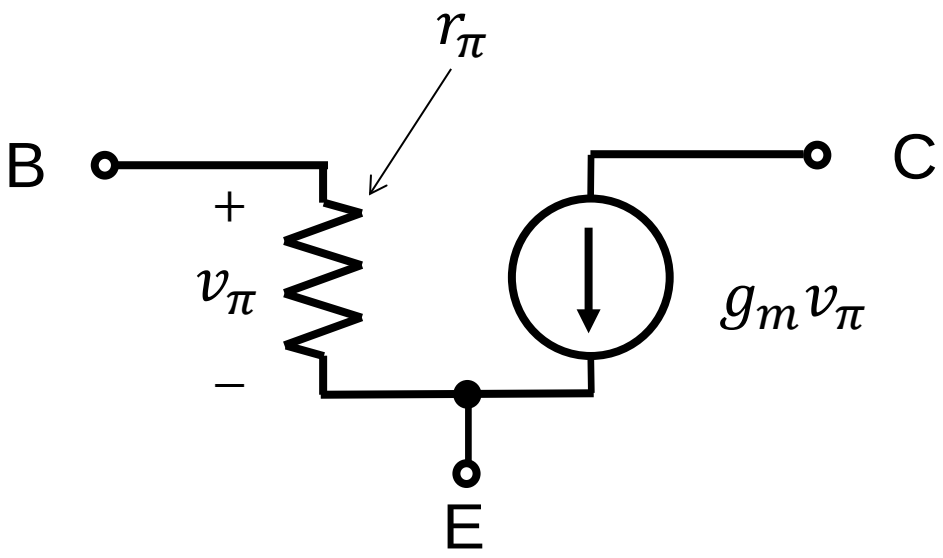
Small-signal model

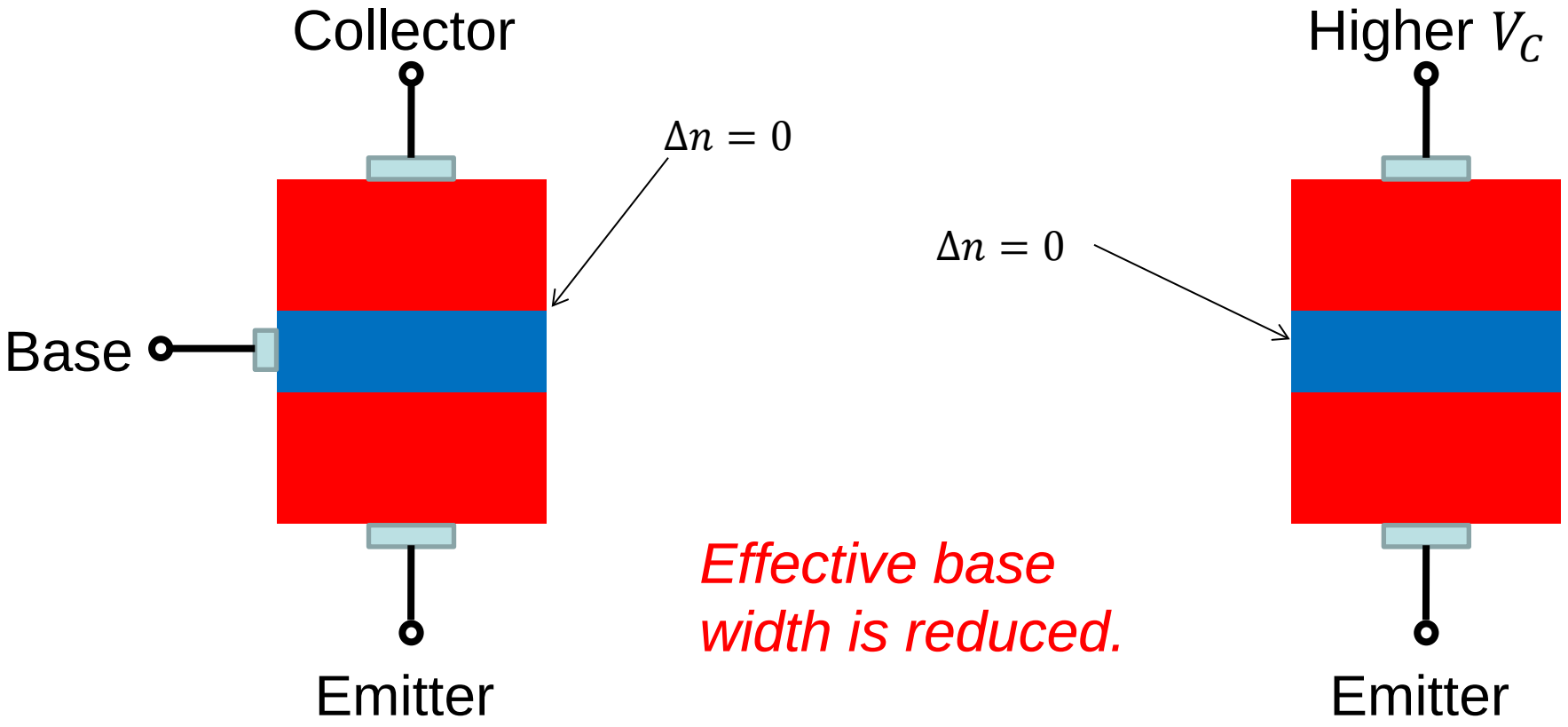
- Quite similar with the MOSFET model
  - Finite resistance between the base and emitter

$$r_\pi = \frac{\beta}{g_m}$$



Early effect (1/2)

- For higher V_{CE},
  - The depletion region between the base and collector is widened.

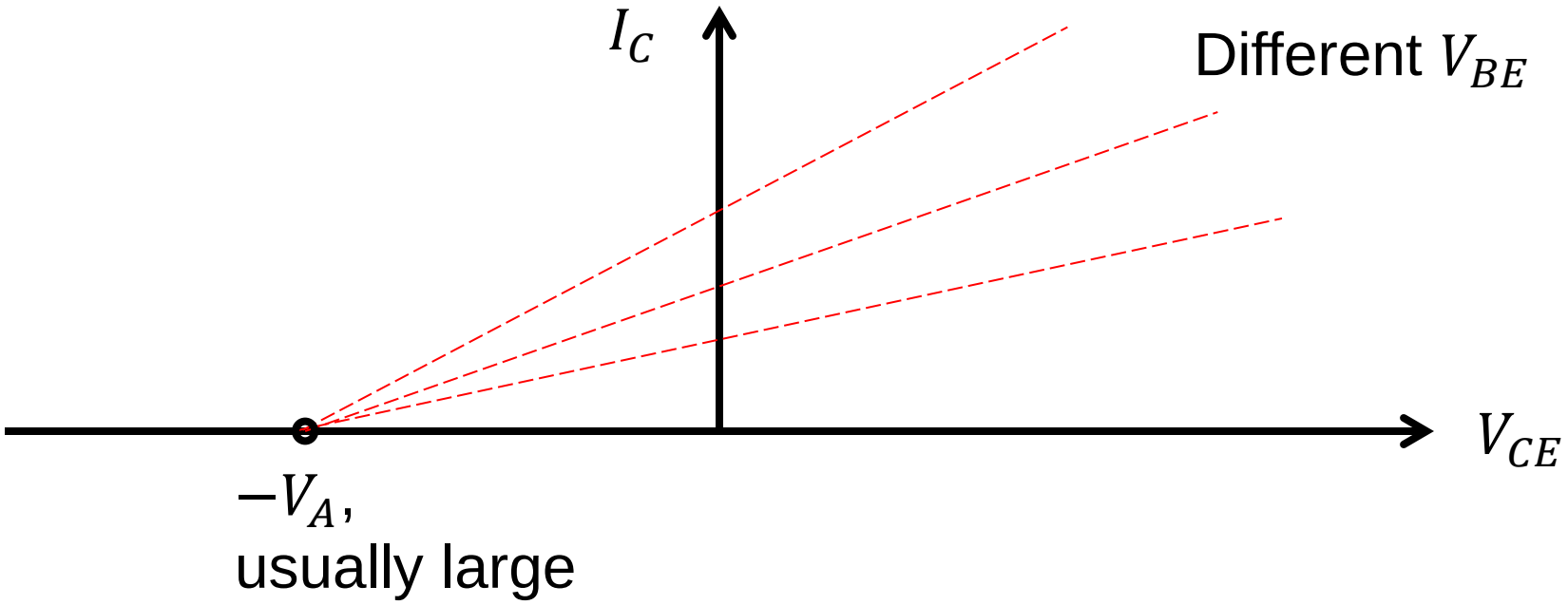


Effective base width is reduced.

Early effect (2/2)

- Its modeling
  - The IV characteristics is now modified:

$$I_C = \left(I_S \exp \frac{V_{BE}}{V_T} \right) \left(1 + \frac{V_{CE}}{V_A} \right)$$

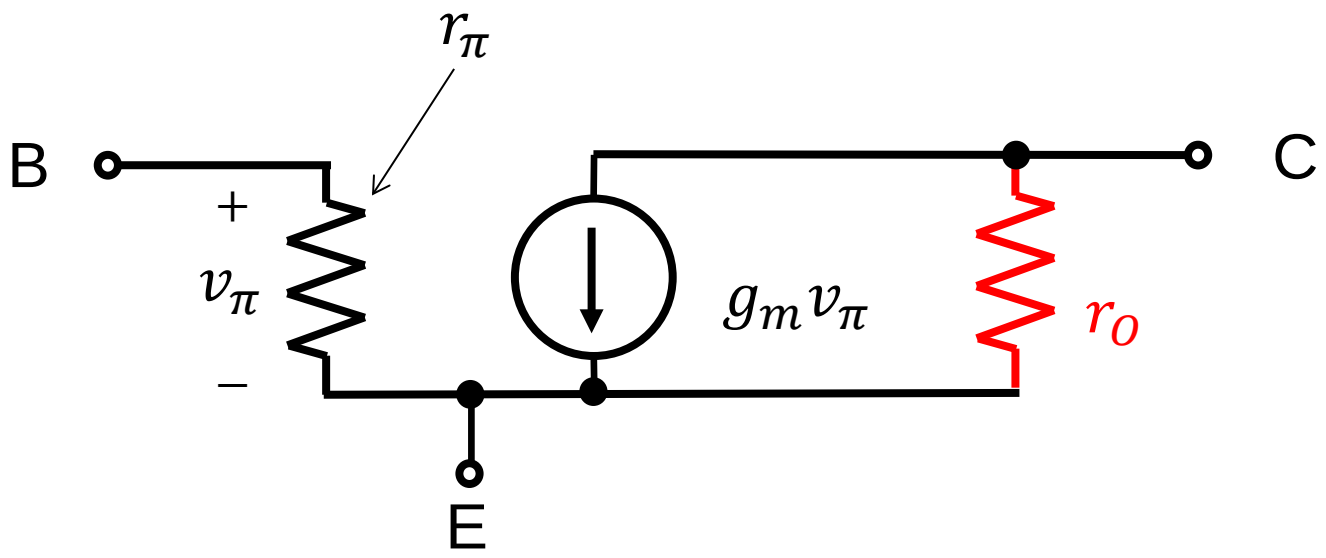


Output resistance

- It is easy to show that

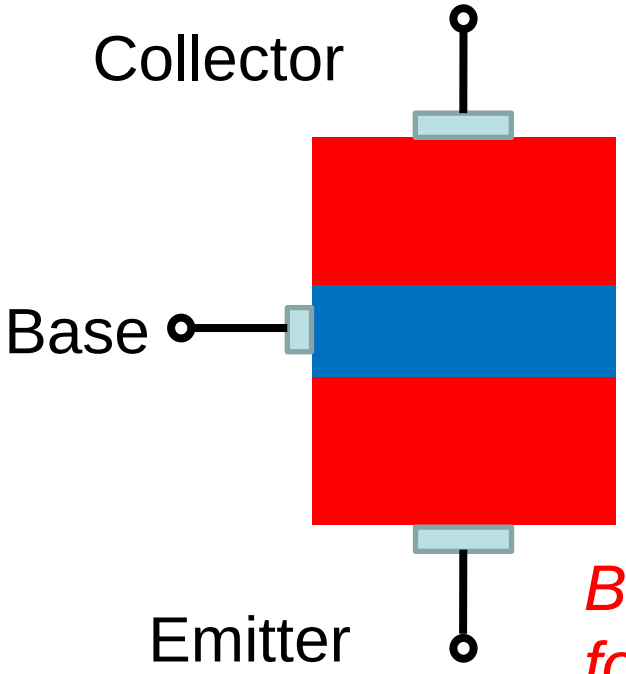
$$\frac{dI_C}{dV_{CE}} = \left(I_S \exp\frac{V_{BE}}{V_T}\right)\frac{1}{V_A}$$

$$r_O \approx \frac{V_A}{I_C}$$

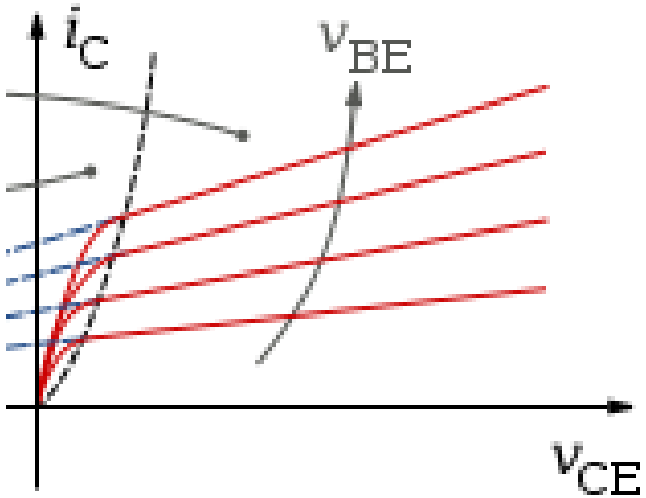


Saturation?

- What was the saturation in the MOSFET?
  - Saturation of the drain current, as the drain voltage increases.
- What is the saturation in the BJT?
  - Saturation of the collector current, as the base current increases.



Both junctions are forward biased.



Typical output characteristics (Taken from Wikipedia)

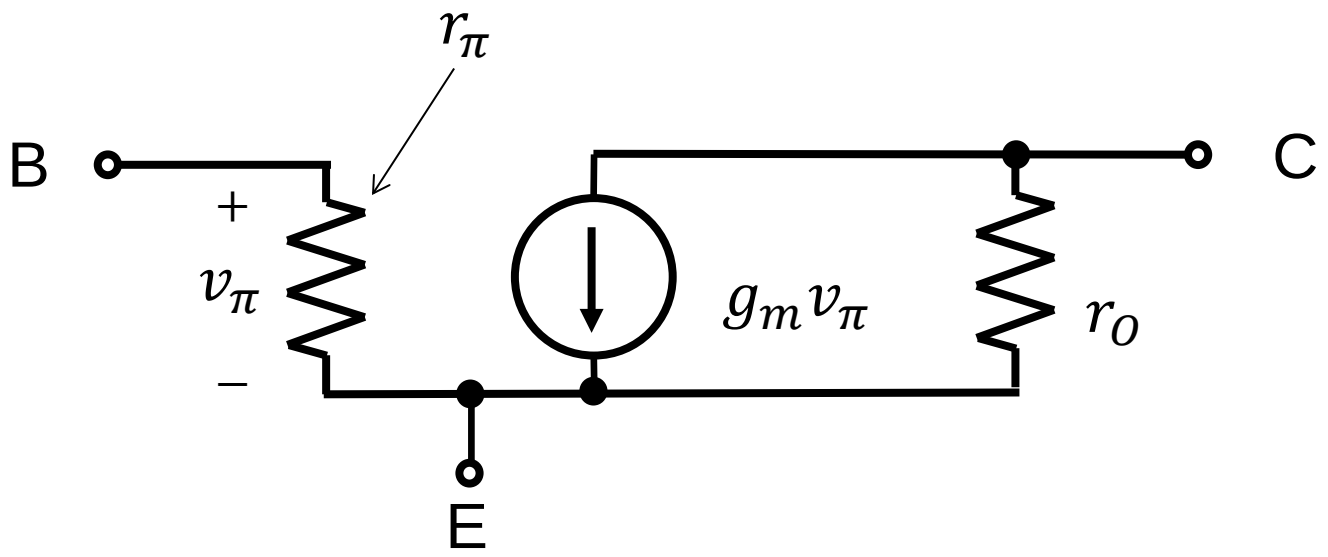
Small-signal model

- Useful expressions

$$g_m = \frac{I_C}{V_T}$$

$$r_\pi = \frac{\beta}{g_m}$$

$$r_O \approx \frac{V_A}{I_C}$$

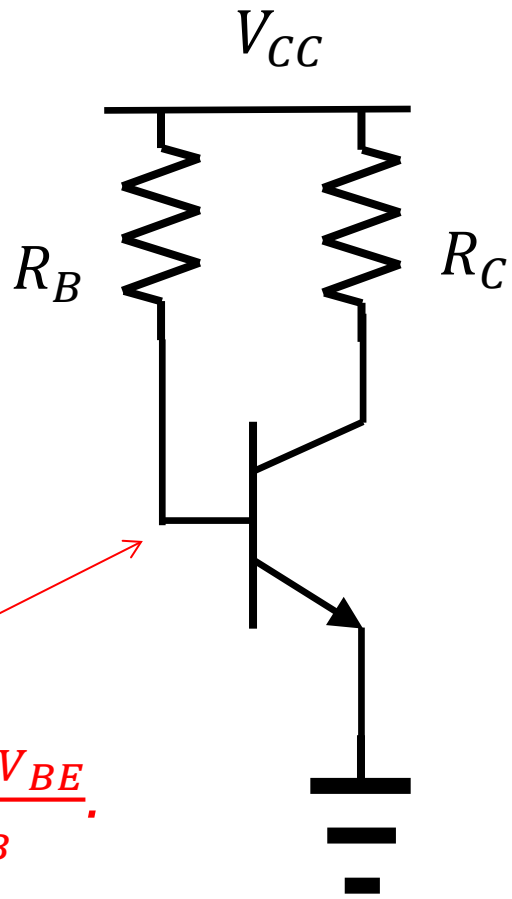


Biasing

- Example 5.7
  - DC analysis?
  - (Recall its MOS counterpart.)

  - Specific values

$V_{CC} = 2.5\ \text{V}$
$R_B = 100\ k\Omega$
$R_C = 1\ k\Omega$



Current?

It would be $\frac{V_{CC}-V_{BE}}{R_B}$.

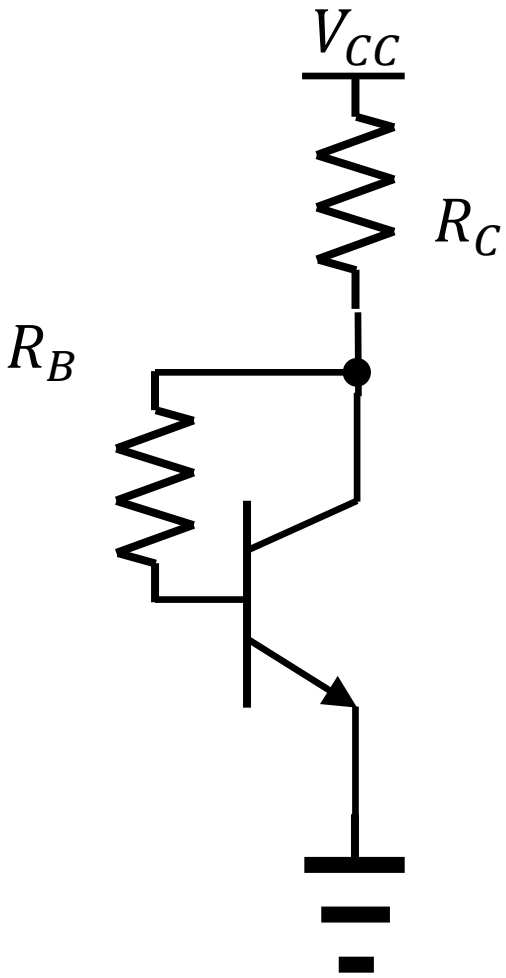
Self-biased stage

- Which one is higher?
  - Collector voltage or base voltage?
  - In the forward active region!

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta}}$$ ← *Why?*

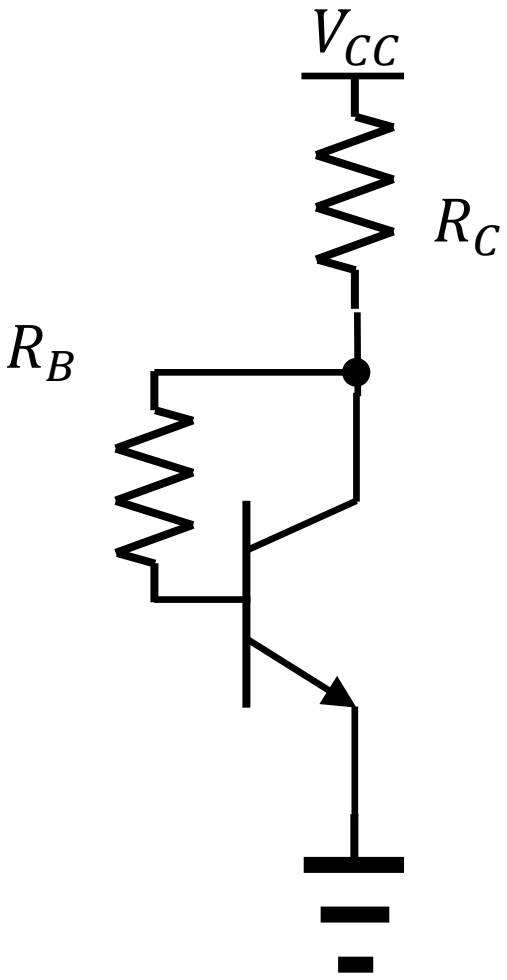
  - Uncertain V_{BE} and β
  - What can we do?

$$R_C \gg \frac{R_B}{\beta}$$



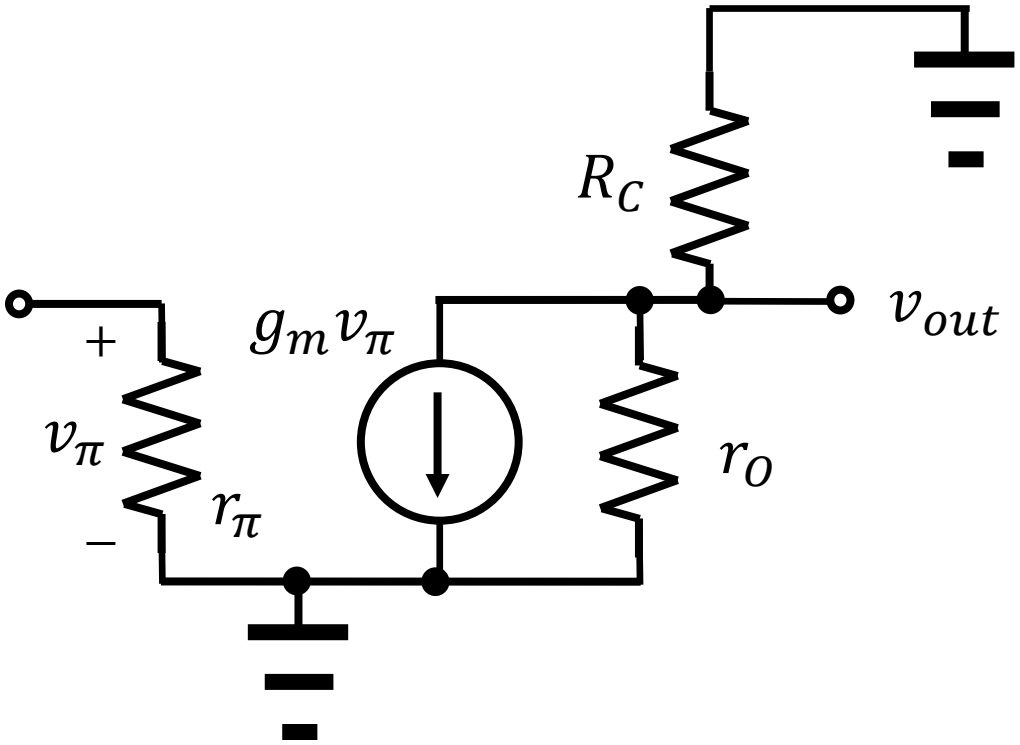
Example 5.14

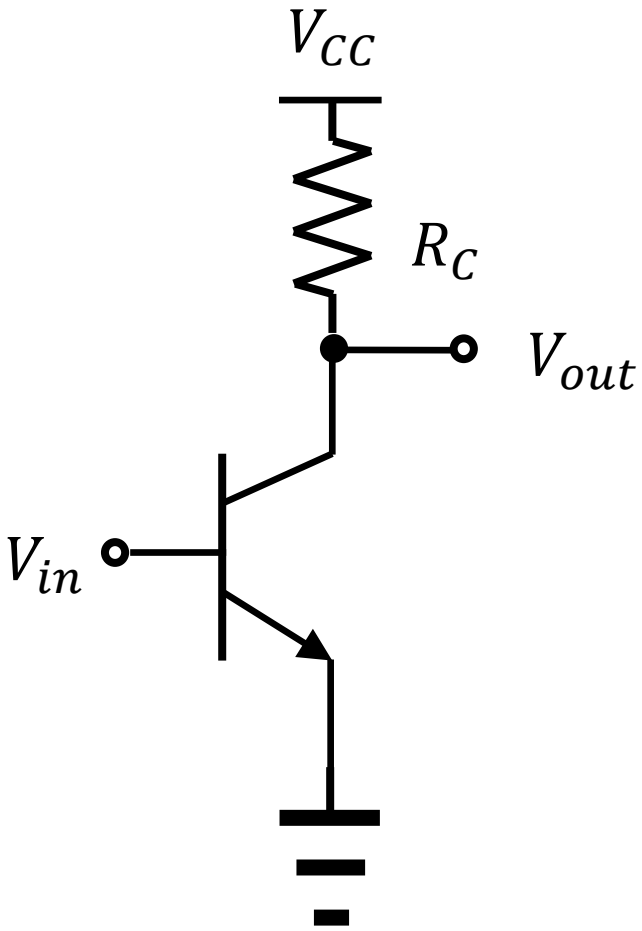
- Design the self-biased stage.
  - In this example, we assume
$$R_C \approx 10\frac{R_B}{\beta}$$
  - It means $I_C = \frac{V_{CC}-V_{BE}}{1.1R_C}$.
  - We want to have g_m of $\frac{1}{13\ \Omega}$ in this example.
  - For BJTs, $g_m = \frac{I_C}{V_T}$. Therefore, $I_C = 2\ \mathrm{mA}$.
  - Then,
$$R_C \approx \frac{V_{CC} - V_{BE}}{1.1\ I_C} = 475\ \Omega$$



Common-emitter (1/2)

- You can easily imagine that
  - There is a common-emitter configuration.





Common-emitter (2/2)

- Voltage gain?
  - Same with the CS stage:

$$A_v = -g_m(R_C||r_O)$$

- Impedances?
  - Input impedance

$$R_{in} = r_\pi = \frac{\beta}{g_m}$$

  - Output impedance

$$R_{out} = R_C||r_O$$

Common-emitter (2/2)

- Voltage gain?
  - Same with the CS stage:
$$A_v = -g_m(R_C||r_O)$$
  - When we have a very large R_C, $A_v \rightarrow -g_m r_O$.
  - For BJTs, $g_m = \frac{I_C}{V_T}$ and $r_O = \frac{V_A}{I_C}$.

- Impedances?
  - Input impedance
$$R_{in} = r_\pi = \frac{\beta}{g_m}$$
  - Output impedance
$$R_{out} = R_C||r_O$$

Example 5.21

- Collector current of 1 mA and $R_C = 1\ k\Omega$.
  - Then, g_m is readily available.

$$g_m = \frac{1}{26\ \Omega}$$

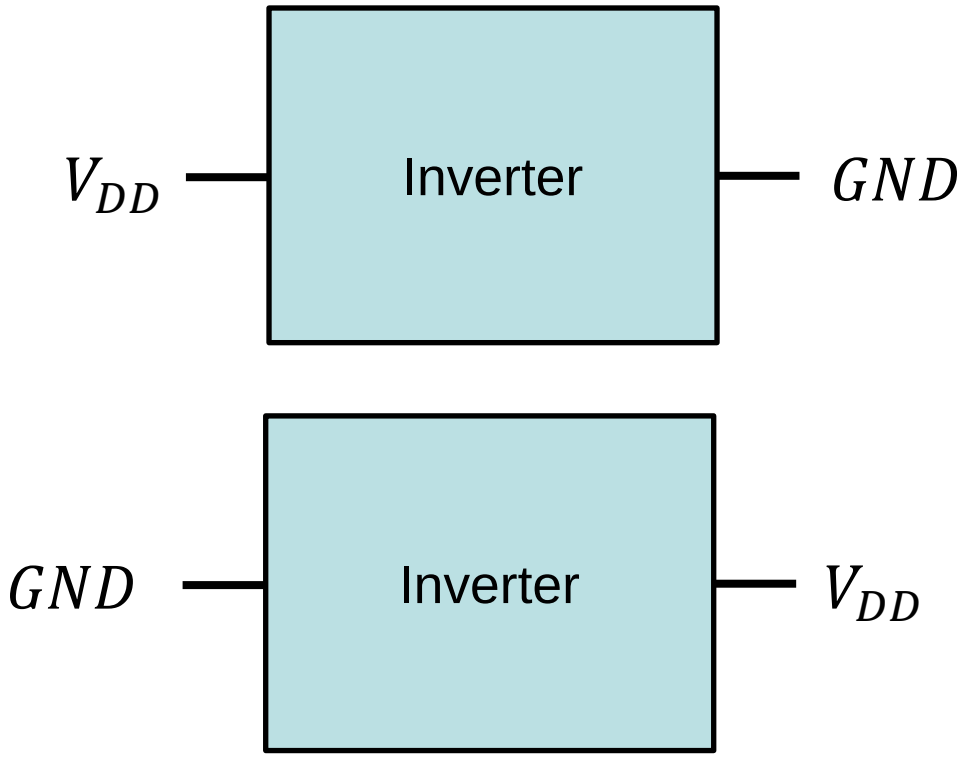
  - When the Early voltage is 10 V, $r_O = \frac{10\ \text{V}}{1\ \text{mA}} = 10k\Omega$.
  - Overall, $R_C || r_O = \frac{1}{1.1} k\Omega \approx 0.91\ k\Omega$.

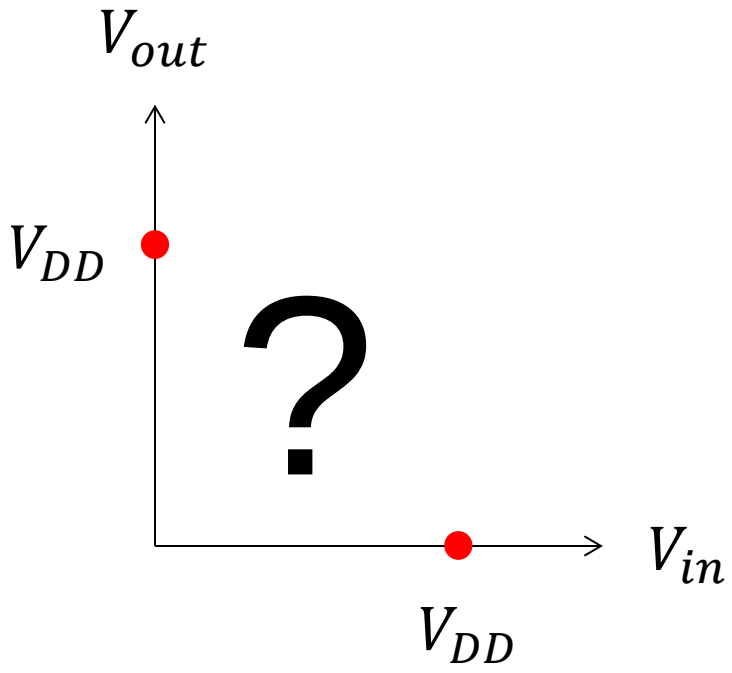
Special topic

DIGITAL CMOS CIRCUITS

In circuit,

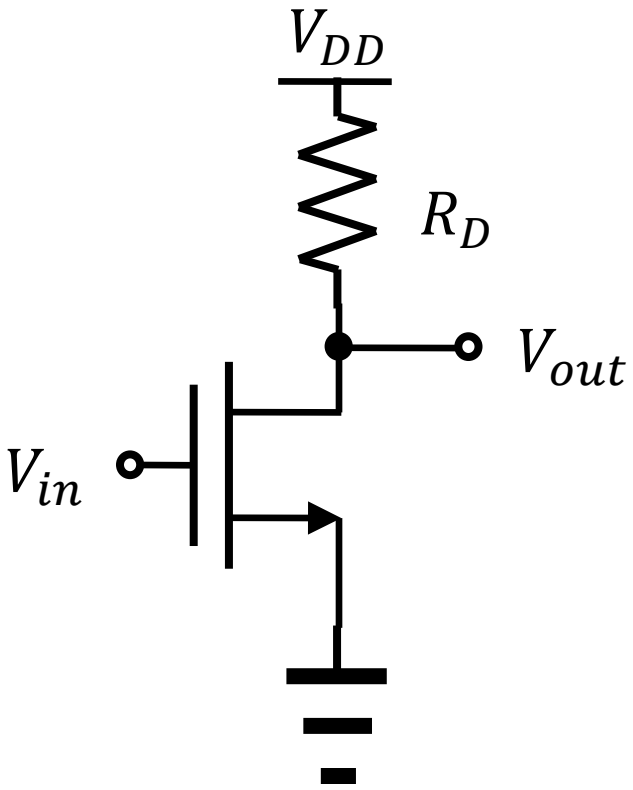
- How can we represent 0 and 1?
  - V_{DD} is assigned to the logical value, 1.
  - GND is assigned to the logical value, 0.





Inverter

- When the output becomes 0?
  - Only when the input is high.
  - *You have seen it before!*



Vin	Vout
0	1
1	0

Voltage transfer

- When $V_{in} < V_{TH}$,
  - Trivially, $V_{out} = V_{DD}$.
- When V_{in} is slightly larger than V_{TH}, the NMOSFET is in the saturation region.

$$V_{out} = V_{DD} - I_D R_D$$

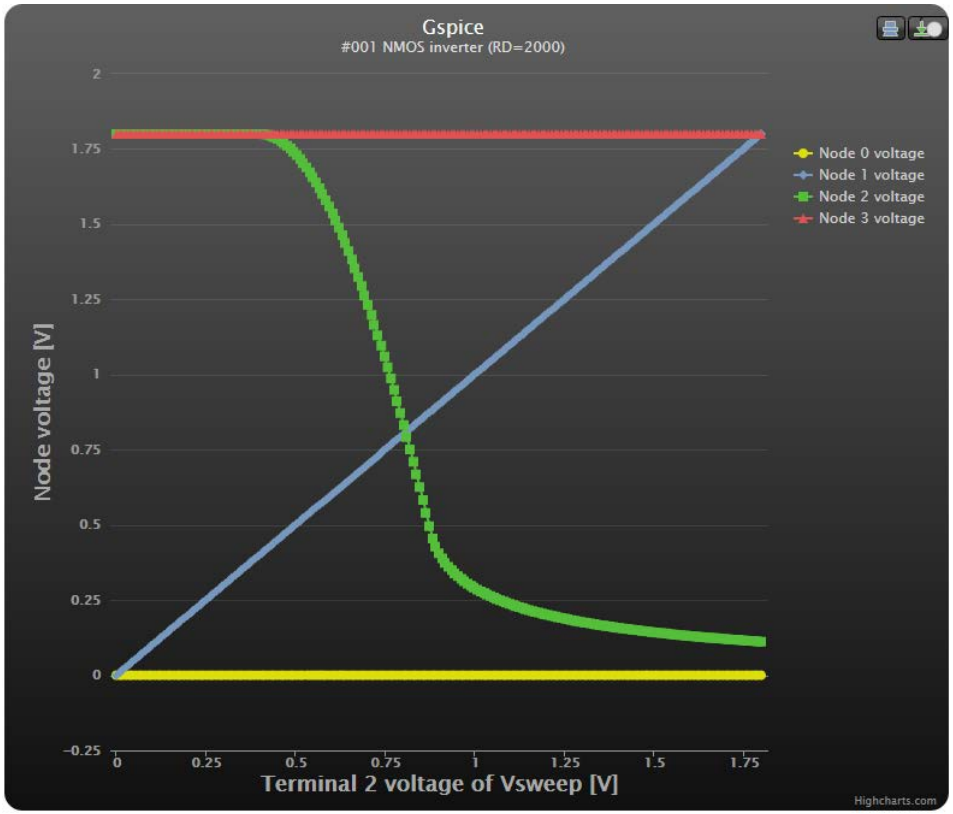
$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2$$

- When V_{in} is further increased, the NMOSFET is in the triode region.

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D[2(V_{in} - V_{TH})V_{out} - V_{out}^2]$$

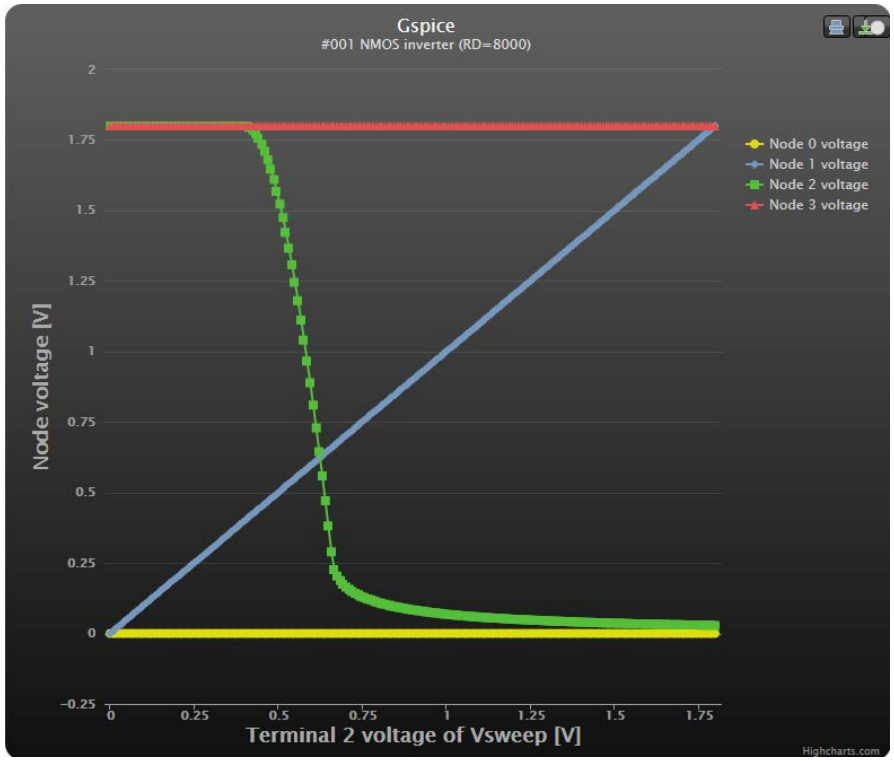
G-SPICE example (1)

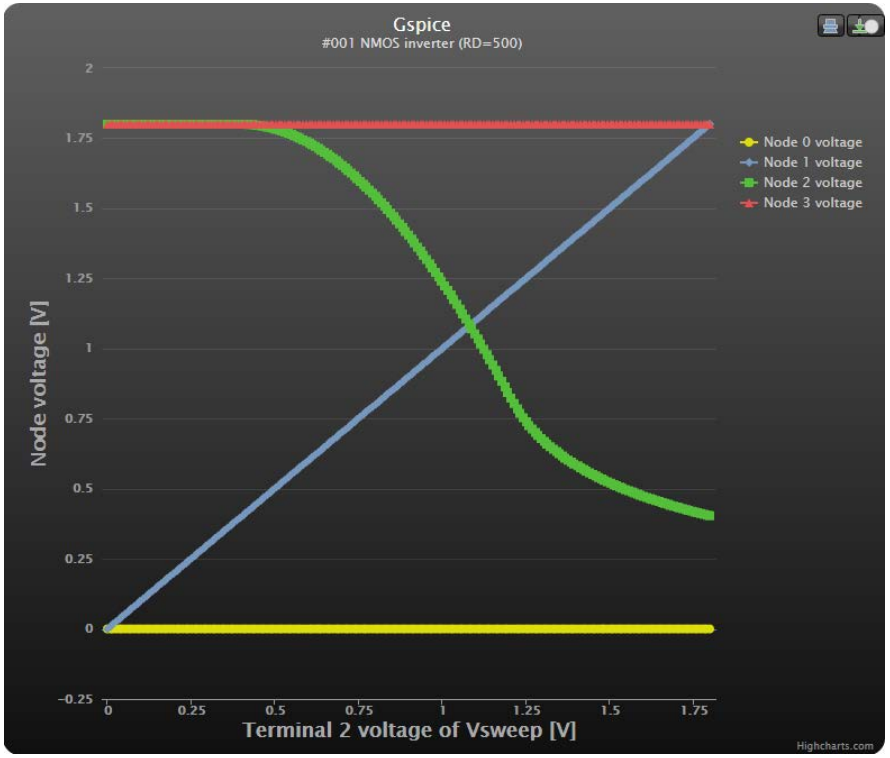
- Following parameters are used.
  - $\mu_n C_{ox} = 200\ \mu\text{A/V}^2$, $V_{TH} = 0.4\ \text{V}$, $\frac{W}{L} = \frac{5}{0.18}$, $\lambda = 0.1\ \text{V}^{-1}$, $R_D = 2k\Omega$ and $V_{DD} = 1.8\ \text{V}$



G-SPICE example (2)

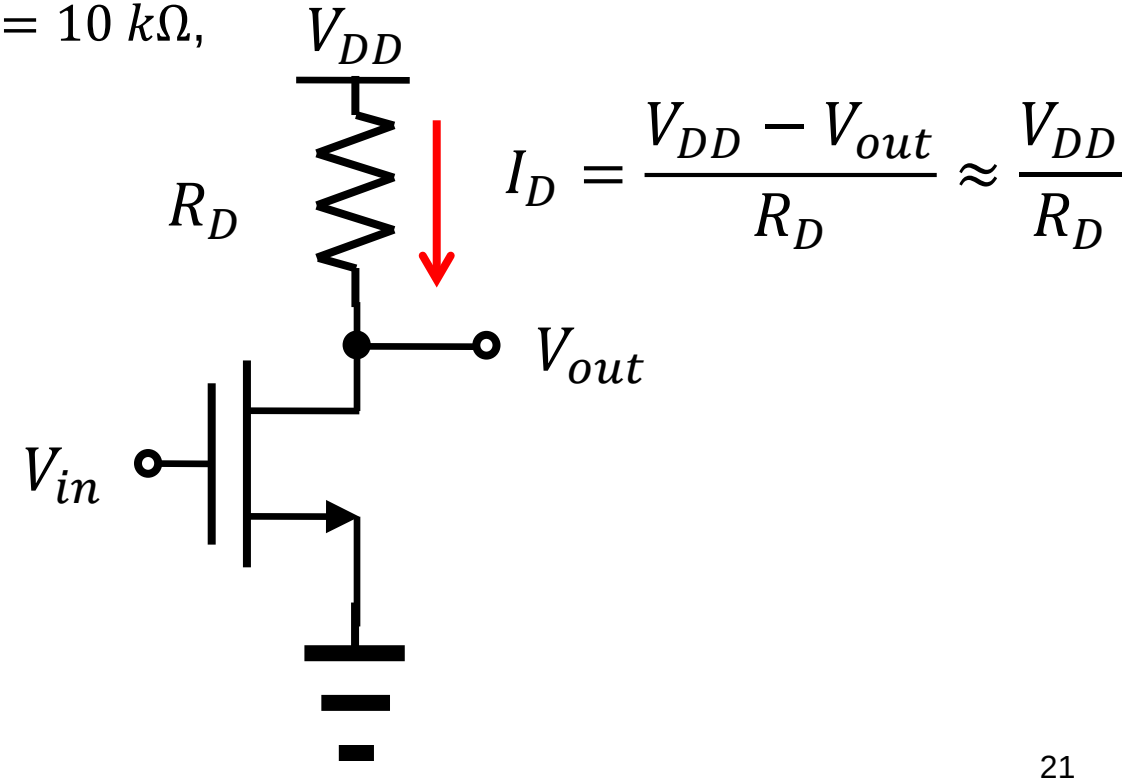
- Different values of R_D (8000 Ohm and 500 Ohm)
  - 0➔1 is always good, but, 1➔0 depends on the situation.
  - Relative “strength” determines the VTC.





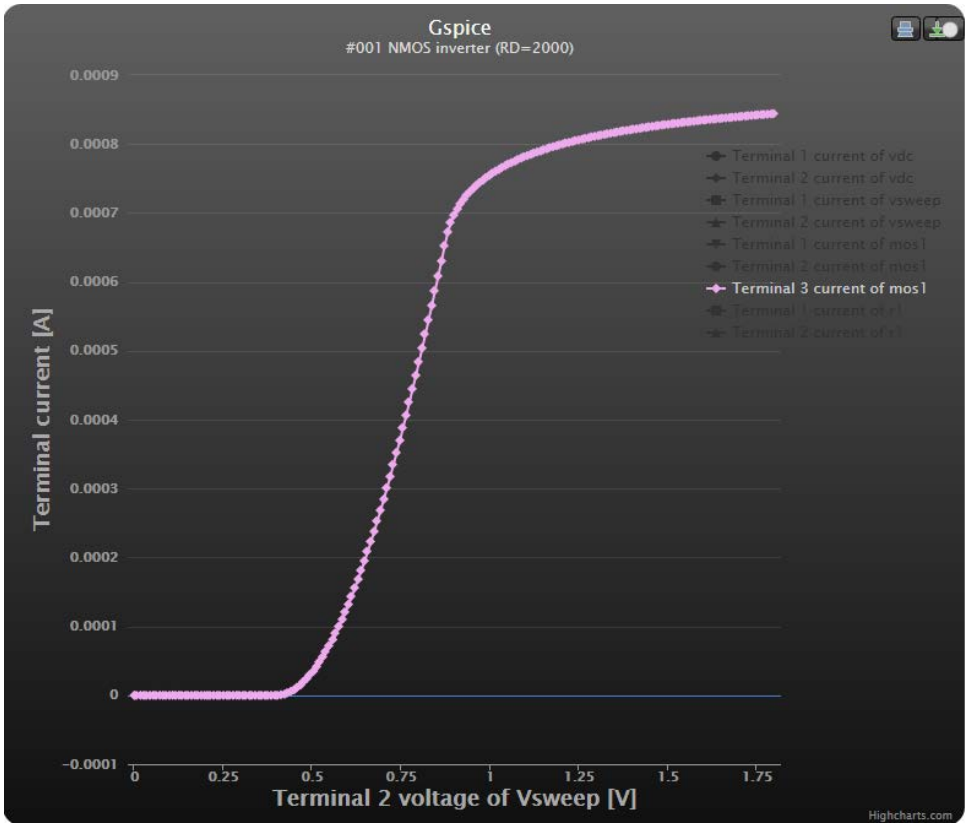
Standby(!) power

- The biggest problem in the NMOS inverter
  - When $V_{in} = 0$, no standby power
  - When $V_{in} = V_{DD}$, the power consumption is (approximately) $\frac{V_{DD}^2}{R_D}$.
  - If $V_{DD} = 1.8\ \mathrm{V}$ and $R_D = 10\ k\Omega$, 324 μW!



G-SPICE example (3)

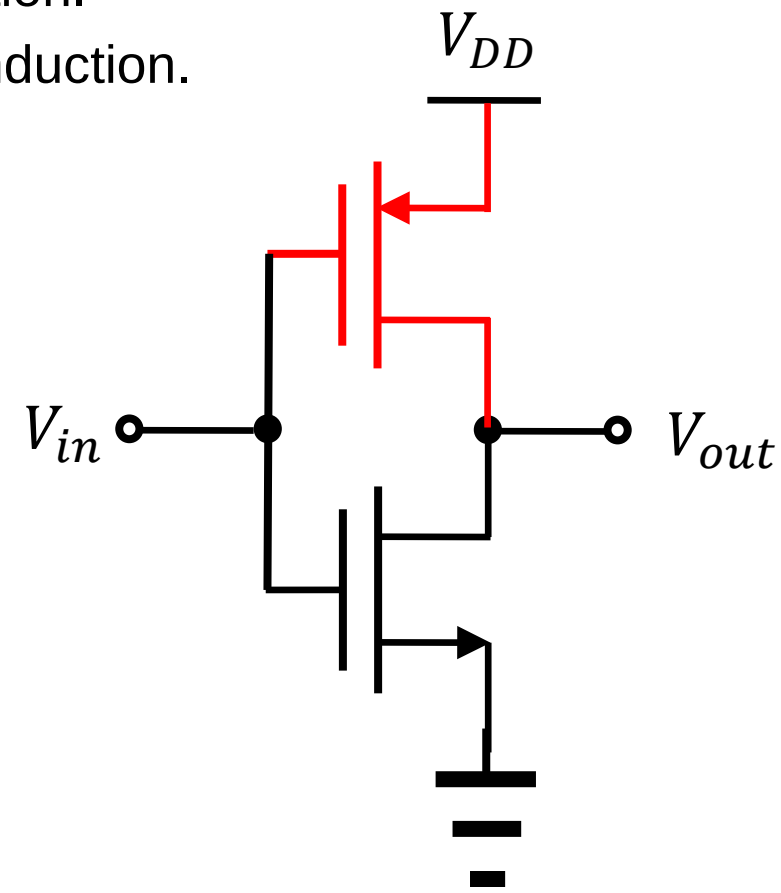
- Current as a function of input voltage
  - Estimate the power consumption…



CMOS inverter

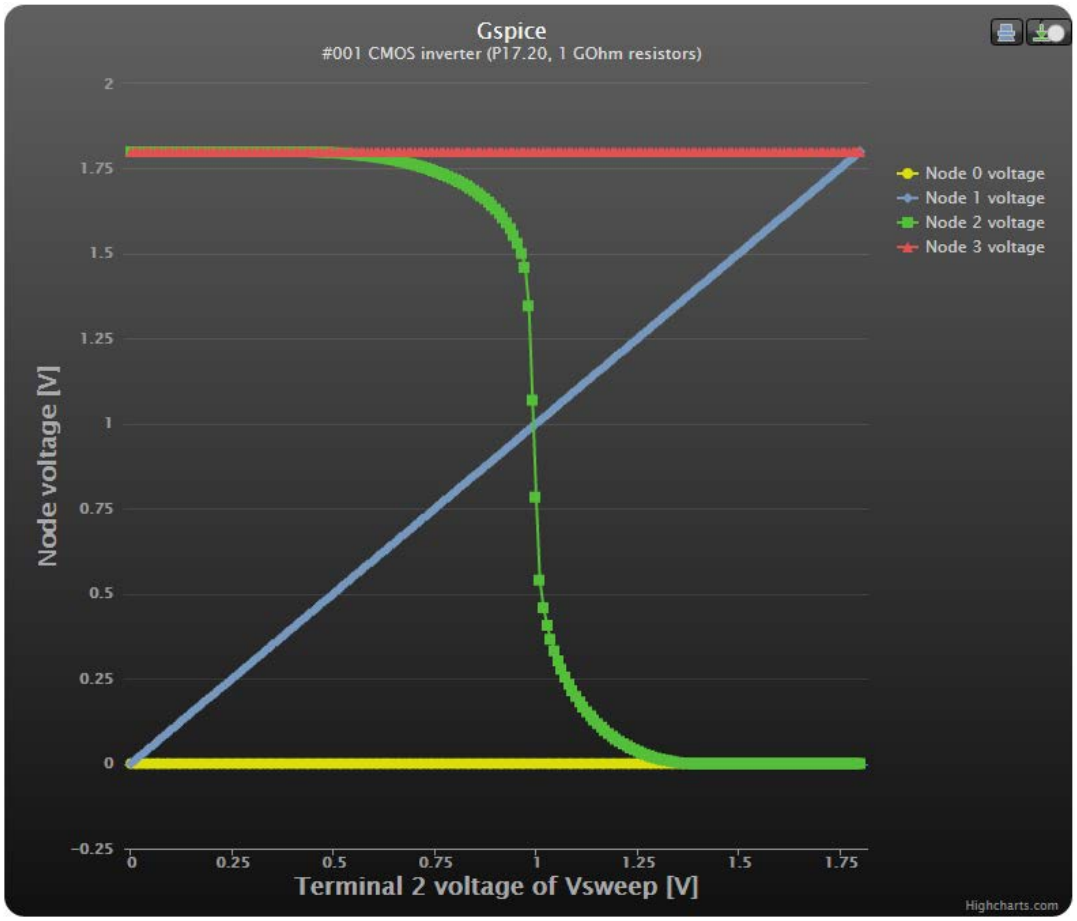
- Ideal “pull-up” should have the following properties.
  - When $V_{in} = V_{DD}$, no current conduction.
  - When $V_{in} = 0$, improved current conduction.

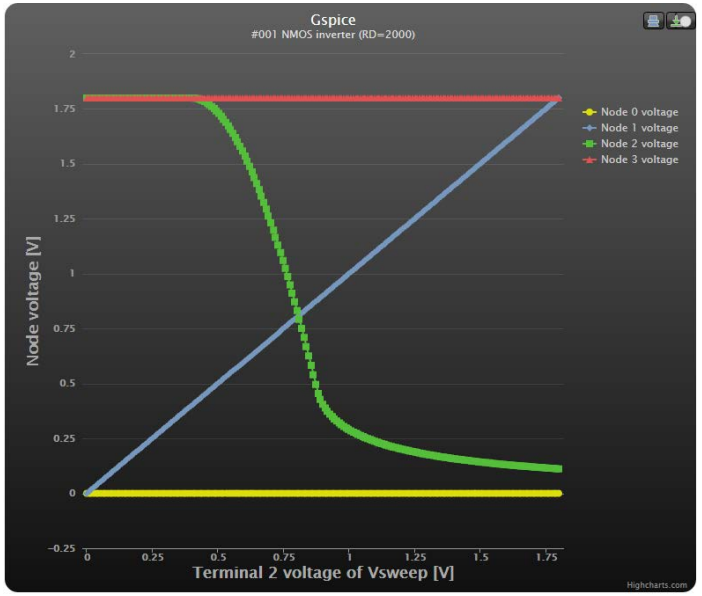
- PMOS can do those jobs!



G-SPICE example (4)

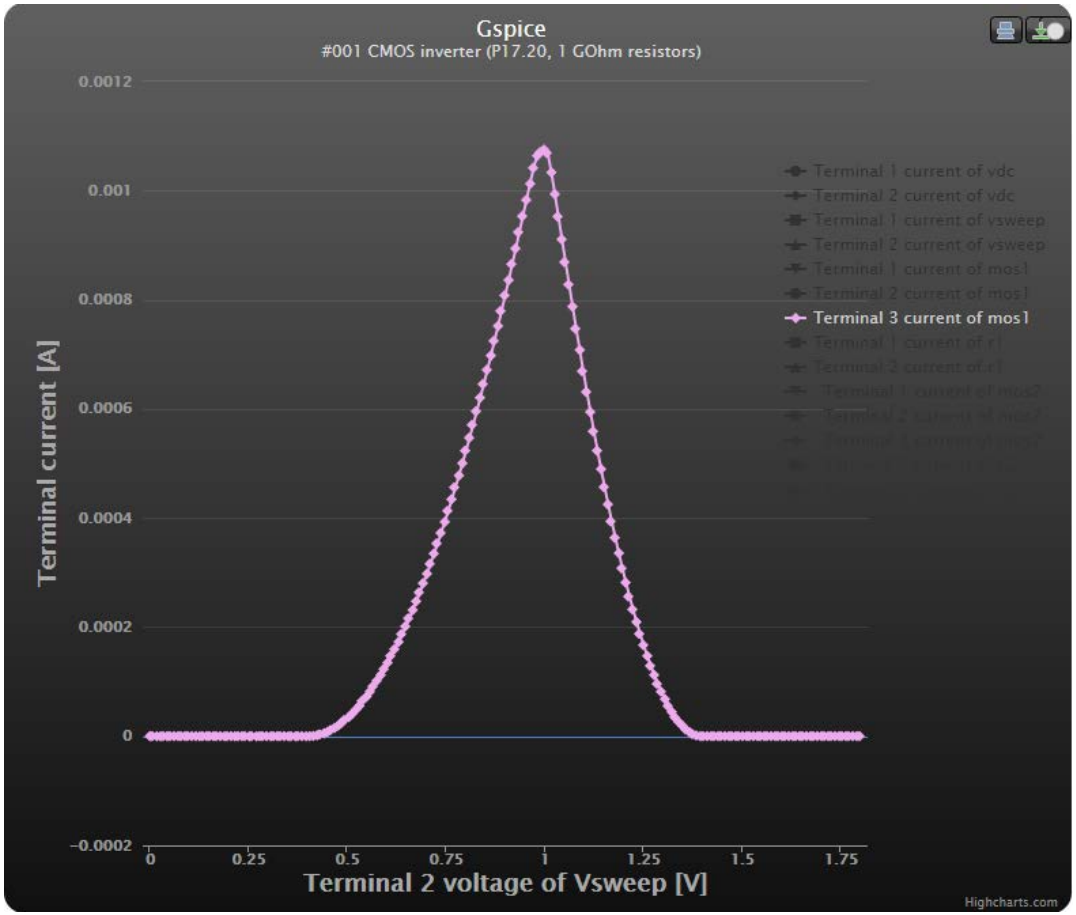
- Parameters of P17.20
  - (Two large resistors are introduced.)

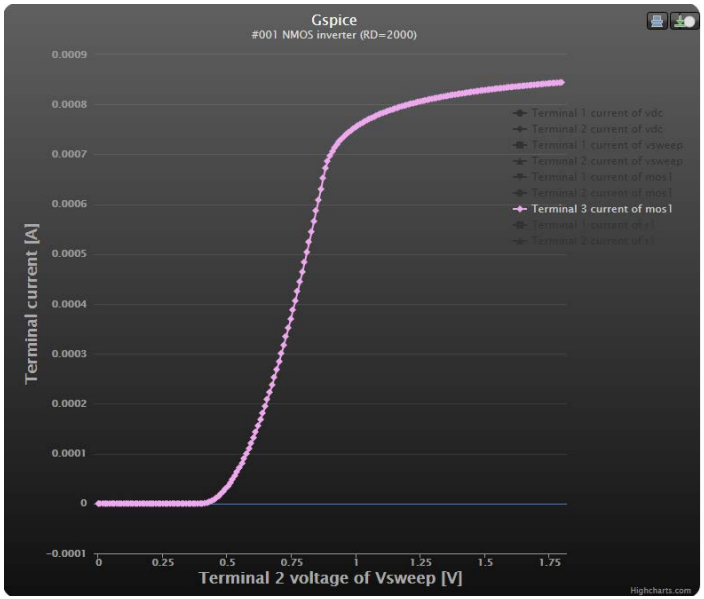




G-SPICE example (5)

- Even better news
  - No standby power is dissipated.





CLOSING REMARKS