Lecture20:
Digital CMOS circuits (3)

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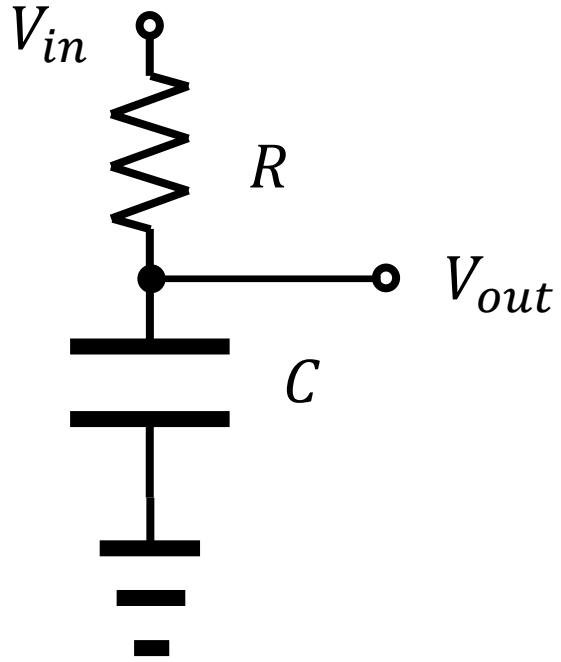
RC circuit

- Consider a serial RC circuit.
  - The KCL states

$$\frac{V_{out} - V_{in}}{R} + C\frac{dV_{out}}{dt} = 0$$

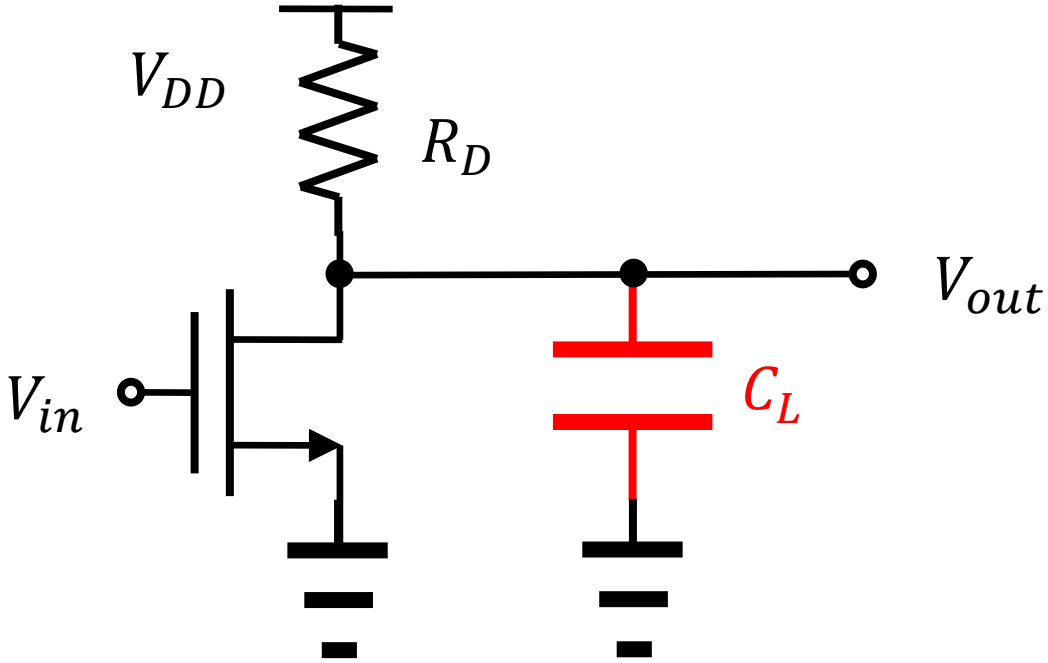
  - Assume a step-wise change of V_{in} at $t = 0$. It becomes V_{DD}.
  - Initial output voltage is V_0.
  - Its solution is given by

$$V_{out}(t) = V_{DD} + (V_0 - V_{DD})\exp\left(-\frac{t}{RC}\right)$$



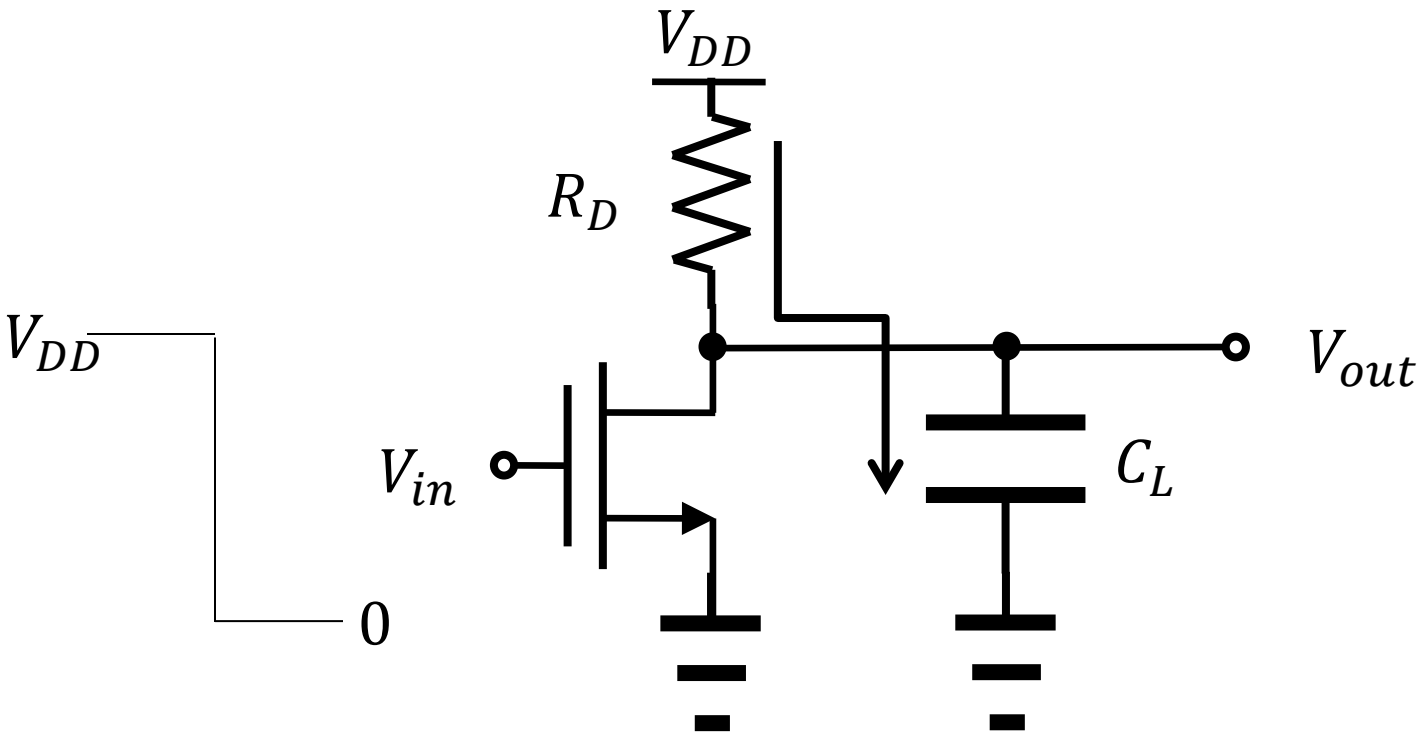
Speed of inverter (1/4)

- VTC merely describes the dc behavior.
  - Input voltages with different frequencies (1 kHz, 1 MHz, 1 GHz, 1 THz, …)
- Time-dependent behavior
  - Can a resistor introduce time-lagging effect? No.



Speed of inverter (2/4)

- A rapid transition of V_{in} from V_{DD} to 0
  - Then, the capacitor should be charged.
  - What is the electrical route to charge the capacitor?



Speed of inverter (3/4)

- Simply, it is a RC circuit.
  - Then, the solution is simply

$$V_{out}(t) = V_{out}(0^-) + [V_{DD} - V_{out}(0^-)]\left(1 - \exp\frac{-t}{R_D C_L}\right)$$

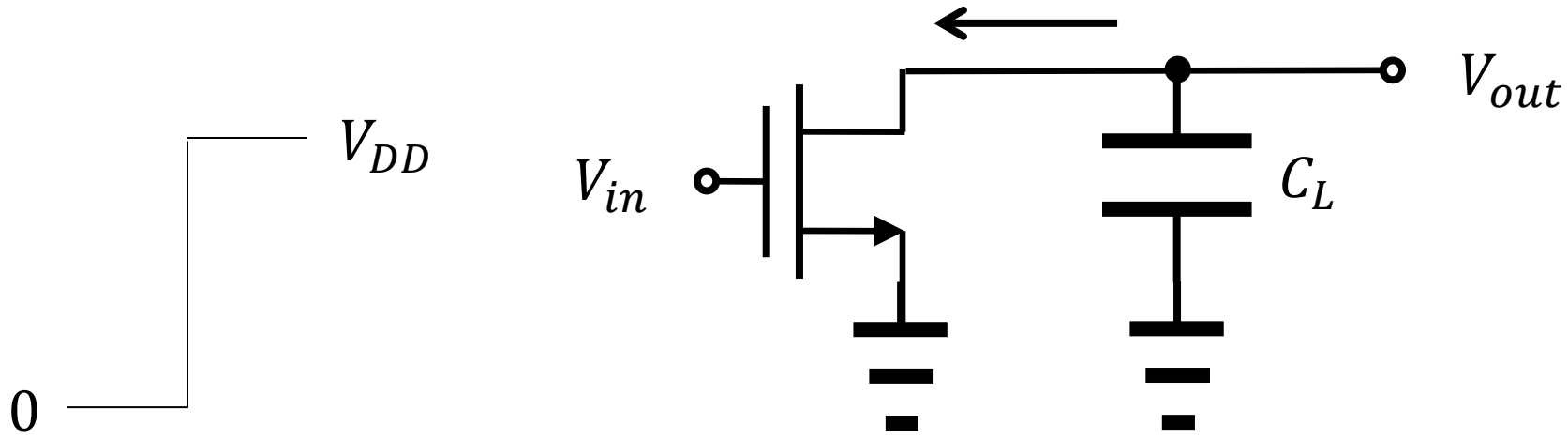
  - Since $\exp(-3) \approx 0.05$, after $3R_D C_L$, V_{out} reaches $0.95\ V_{DD}$.

  - Yes, it takes time to get the stable output voltage…
  - The delayt restricts the maximum signal frequency.

Speed of inverter (4/4)

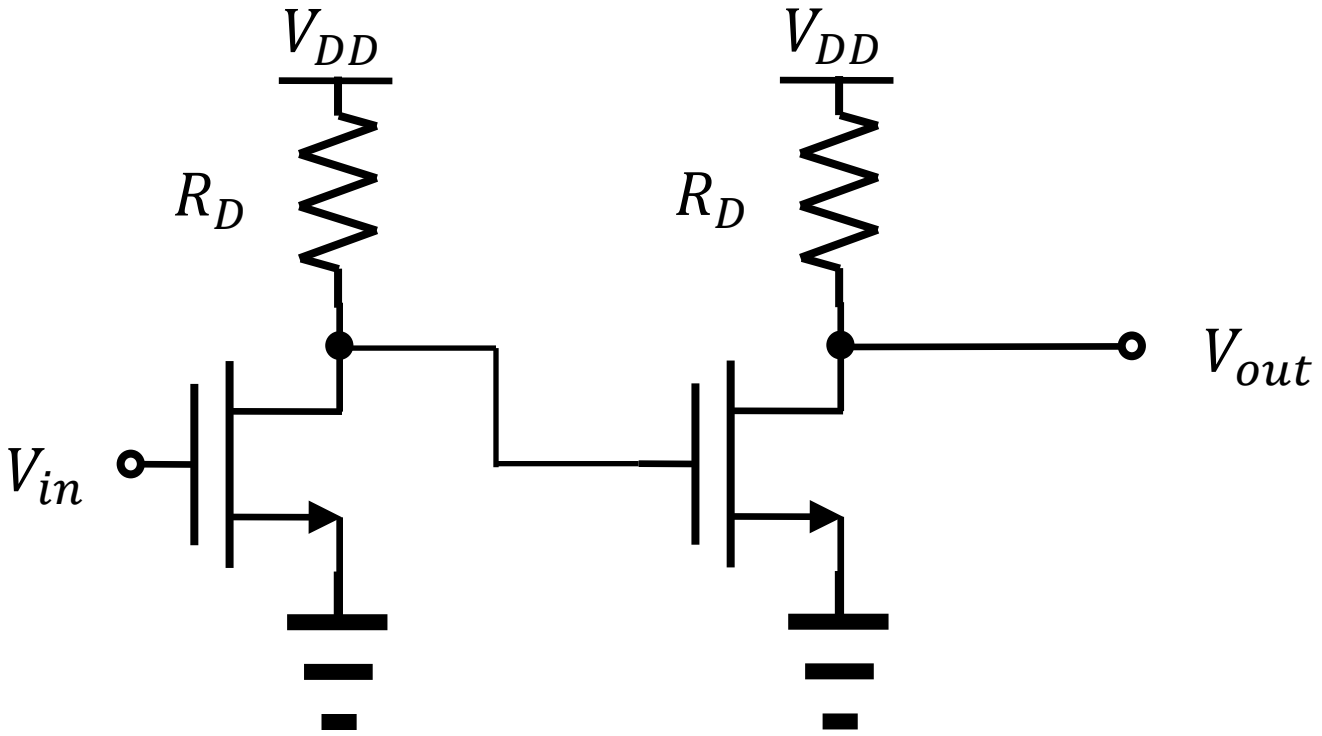
- A rapid transition of V_{in} from 0 to V_{DD} to 0
  - At the initial phase, the resistor does not conduct.
  - Also the MOSFET is operated in its saturation mode.
  - Then,

$$I_{D,sat} + C_L \frac{dV_{out}}{dt} = 0$$



Origin of C_L?

- Consider an inverter chain.
  - Then, what is the load capacitance for the first stage?



- Another origin ➔ Interconnect

Fan-out

- (It is not “Pan out” written in the lecture. Sorry!)
- The fan-out of a logic gate output is the number of gate inputs it can drive.
  - In order to minimize the delay, a large fan-out should be avoided.

Homework#9

- Due: 09:00, May 28
- Solve the following problems of the final exam in 2017.
  - P35
  - P36
  - P37
  - P38
  - P39
  - P41
  - P42
  - P43