Lecture23: CMOS inverter

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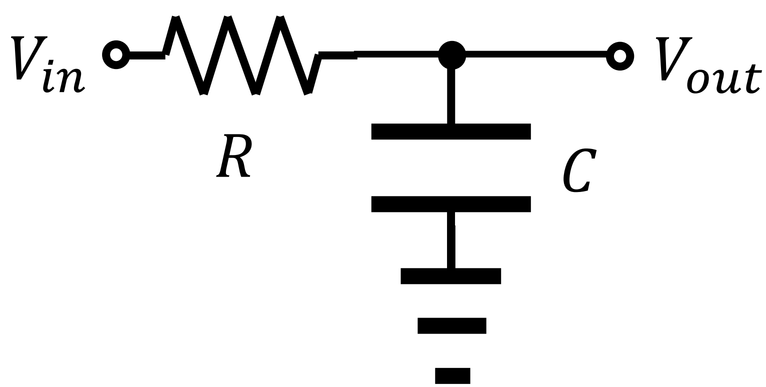
RC circuit

- Consider a serial RC circuit.
  - The KCL states

$$\frac{V_{out} - V_{in}}{R} + C\frac{dV_{out}}{dt} = 0$$

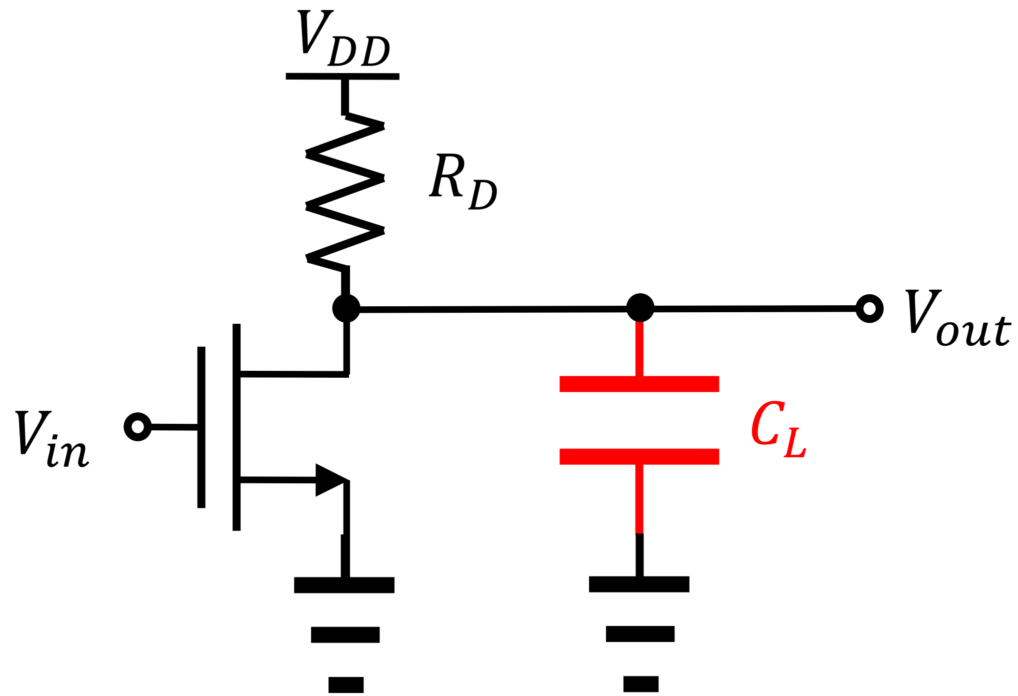
  - Assume a step-wise change of V_{in} at $t = 0$. It becomes V_{DD}.
  - Initial output voltage is V_0.
  - Its solution is given by

$$V_{out}(t) = V_{DD} + (V_0 - V_{DD})\exp\left(-\frac{t}{RC}\right)$$



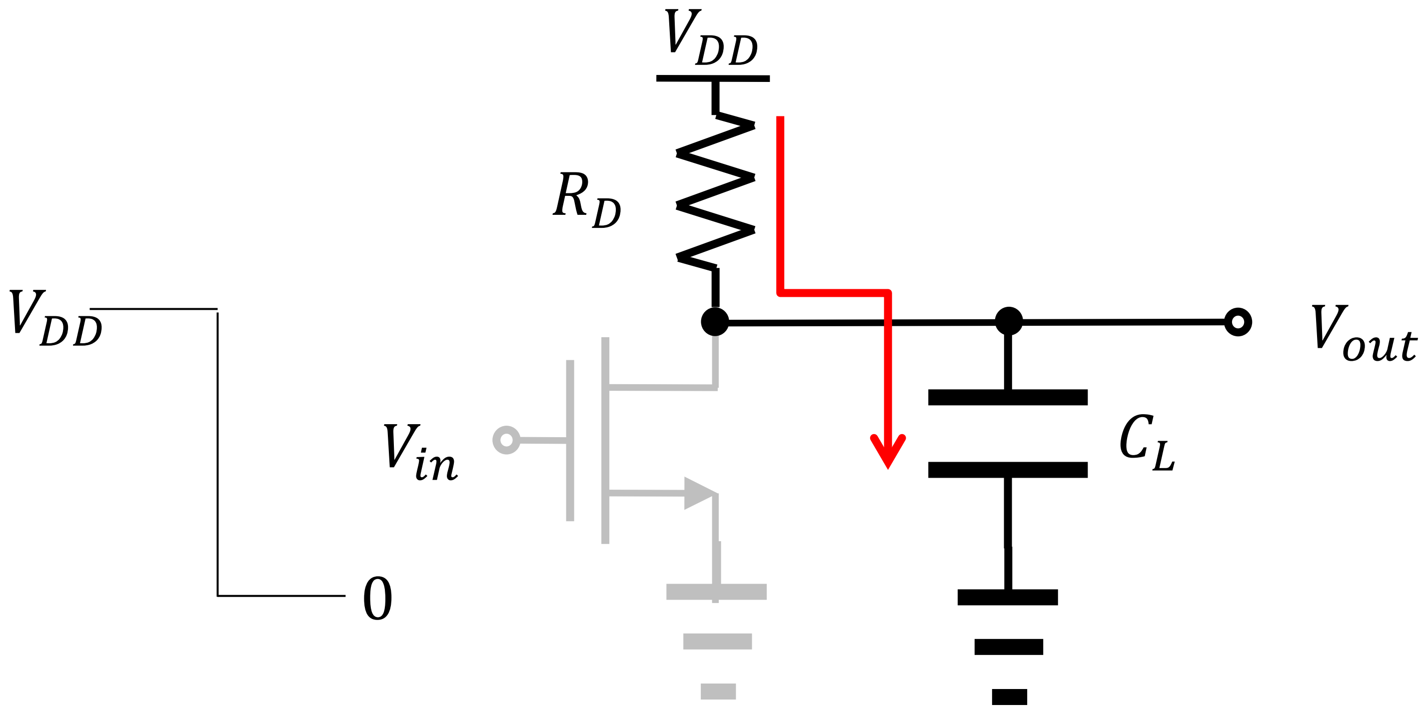
Speed of inverter (1/4)

- VTC merely describes the DC behavior.
  - Input voltages with different frequencies (1 kHz, 1 MHz, 1 GHz, …)
  - Time-dependent behavior



Speed of inverter (2/4)

- A rapid transition of V_{in} from V_{DD} to 0
  - The capacitor should be charged.



Speed of inverter (3/4)

- Simply, it is a RC circuit.
  - Then, the solution is simply

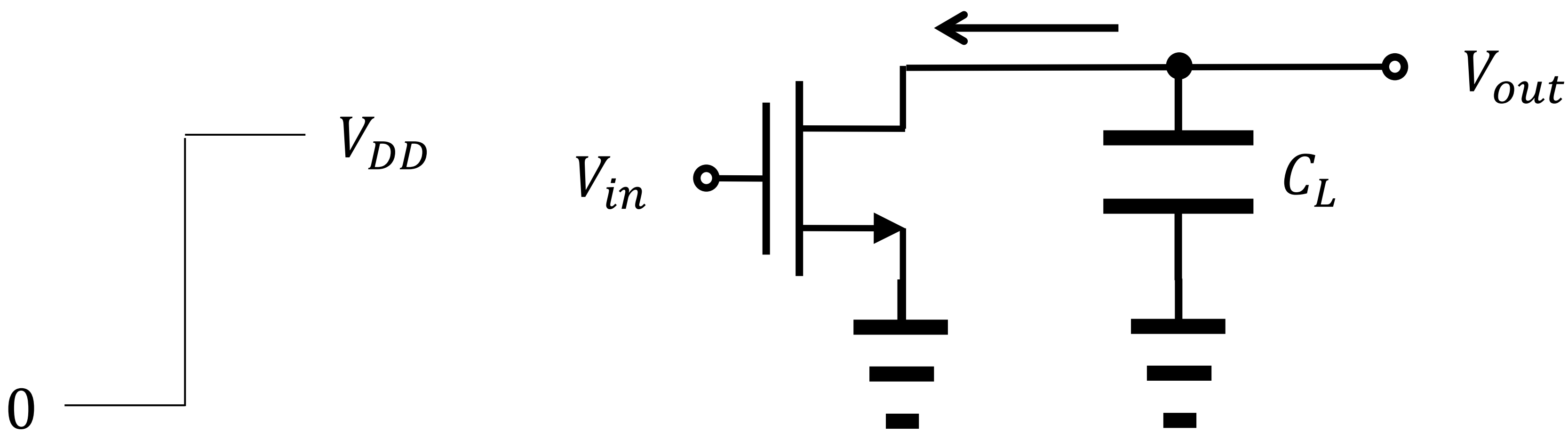
$$V_{out}(t) = V_{out}(0^-) + [V_{DD} - V_{out}(0^-)]\left(1 - \exp\frac{-t}{R_D C_L}\right)$$

  - Since $\exp(-3) \approx 0.05$, after $3R_D C_L$, V_{out} reaches $0.95\,V_{DD}$.
  - Yes, it takes time to get the stable output voltage…
  - The delay restricts the maximum signal frequency.

Speed of inverter (4/4)

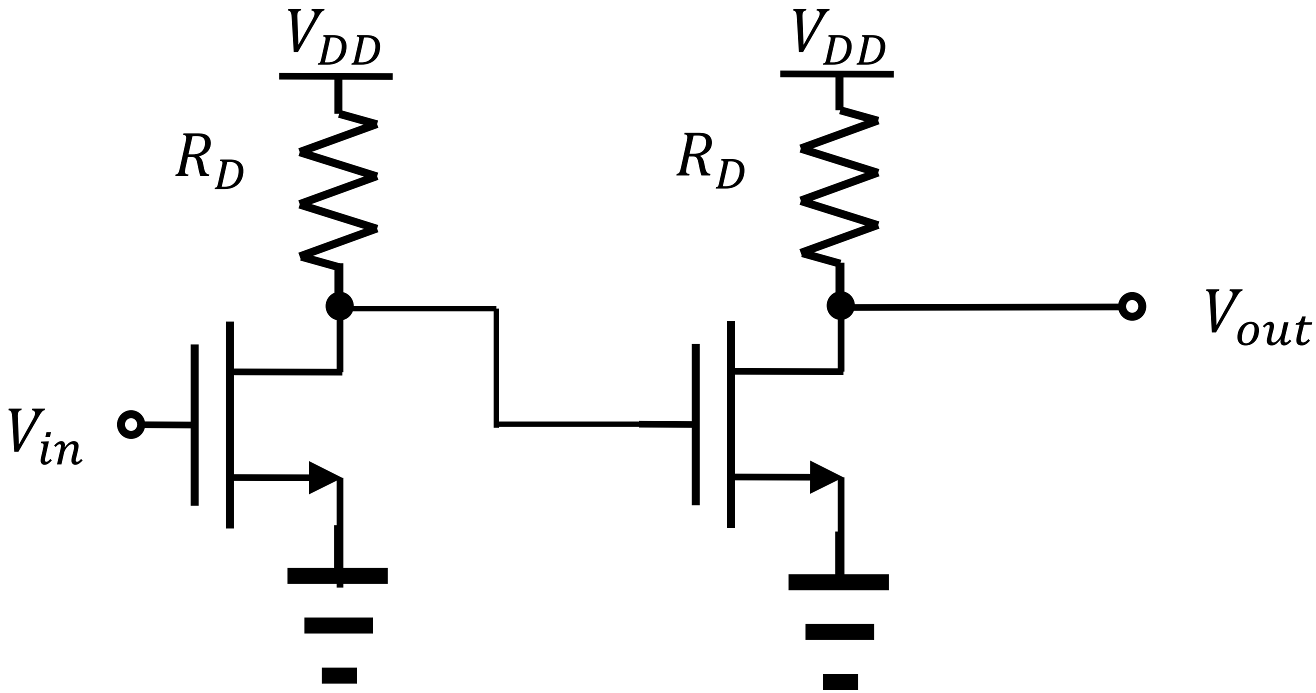
- A rapid transition of V_{in} from 0 to V_{DD} to 0
  - At the initial phase, the resistor does not conduct.
  - Also the MOSFET is operated in its saturation mode. Then,

$$I_{D,sat} + C_L \frac{dV_{out}}{dt} = 0$$



Origin of C_L?

- Consider an inverter chain.
  - Then, what is the load capacitance for the first stage?

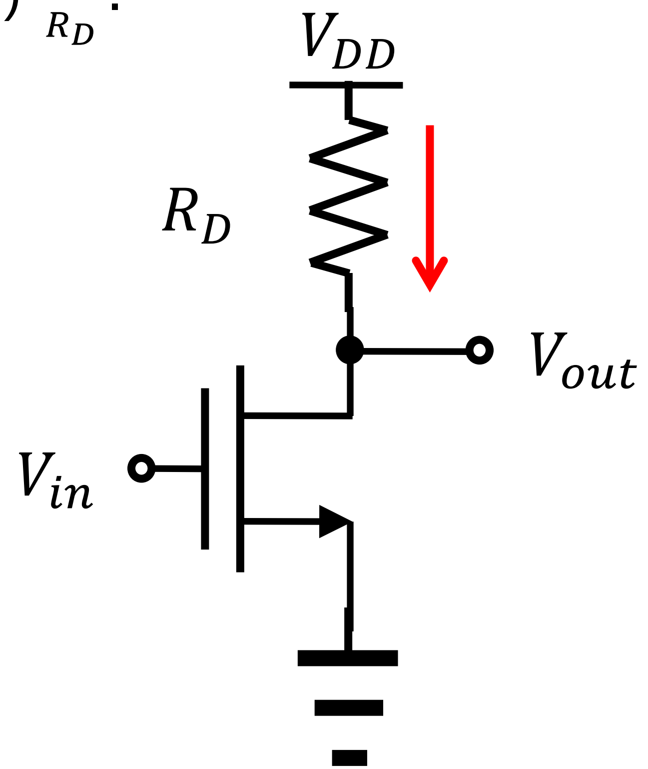


- Interconnect

Standby(!) power

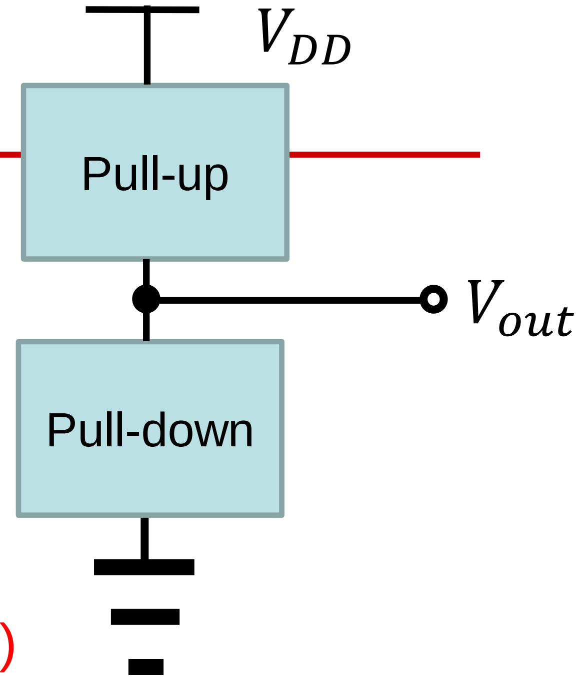
- The biggest problem in the NMOS inverter
  - When $V_{in} = 0$, no standby power
  - When $V_{in} = V_{DD}$?
  - The power consumption is (approximately) $\frac{V_{DD}^2}{R_D}$.
  - If $V_{DD} = 1.8\ \mathrm{V}$ and $R_D = 10\ k\Omega$,

  324 μW!



$$I_D = \frac{V_{DD} - V_{out}}{R_D} \approx \frac{V_{DD}}{R_D}$$

NMOS inverter



- Passive "pull-up" device
  - (a) Degradation of output level

Too small R_D, when $V_{in} = V_{DD}$.

In this case, large R_D is desirable.

  - (b) Risetime limitation

Too small current for 1 ➔ 0 transition. ($V_{in} = 0$)

In this case, a better capability to charge the C_L is desirable.

  - (c) Static power consumption

No ability to block the current, when $V_{in} = V_{DD}$.

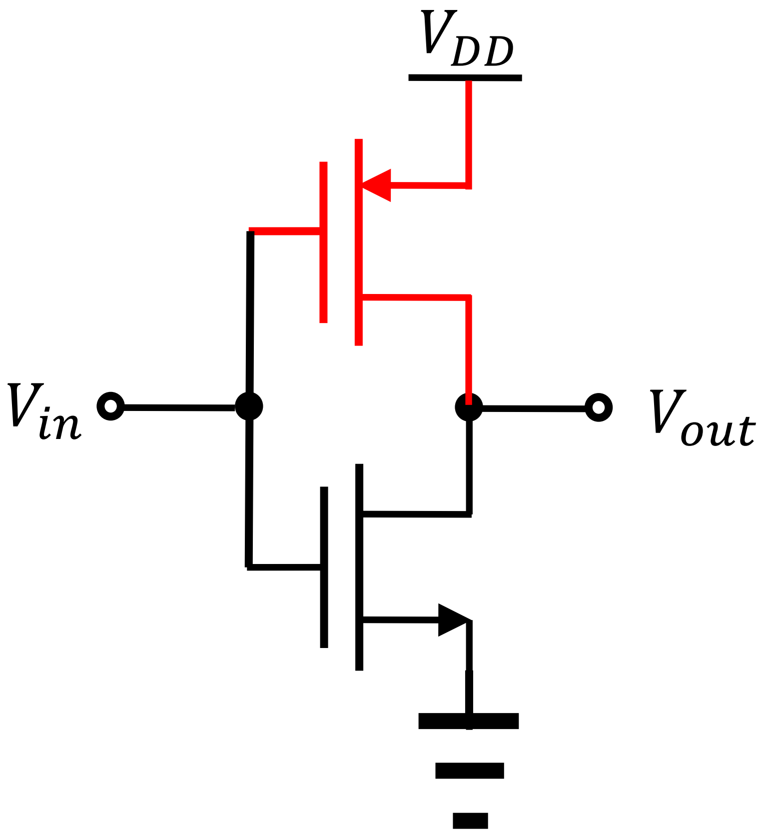
In this case, no current conduction is desirable.

  - (a) & (c) ←➔ (b)

CMOS inverter

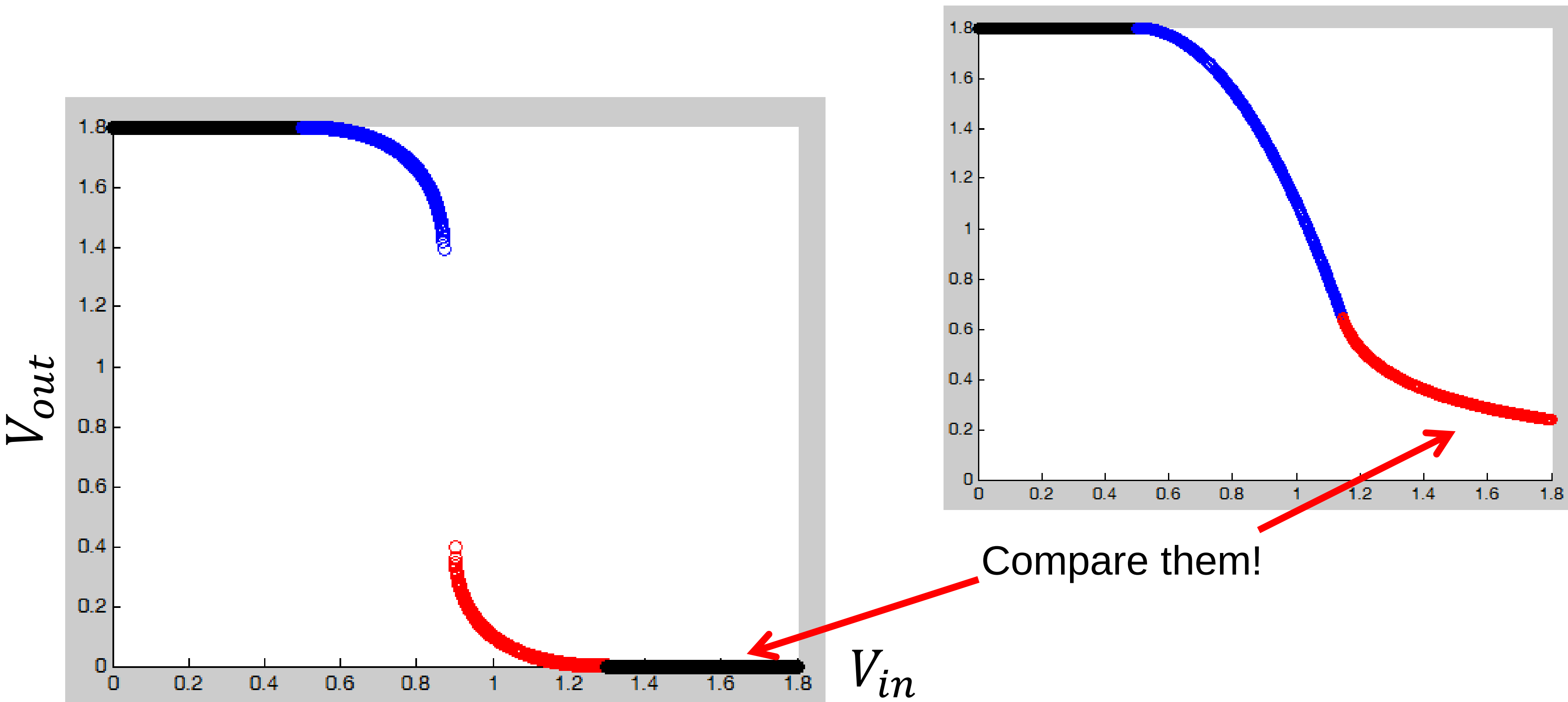
- Ideal "pull-up" should have the following properties.
  - When $V_{in} = V_{DD}$, no current conduction.
  - When $V_{in} = 0$, improved current conduction.

- PMOS can do those jobs!



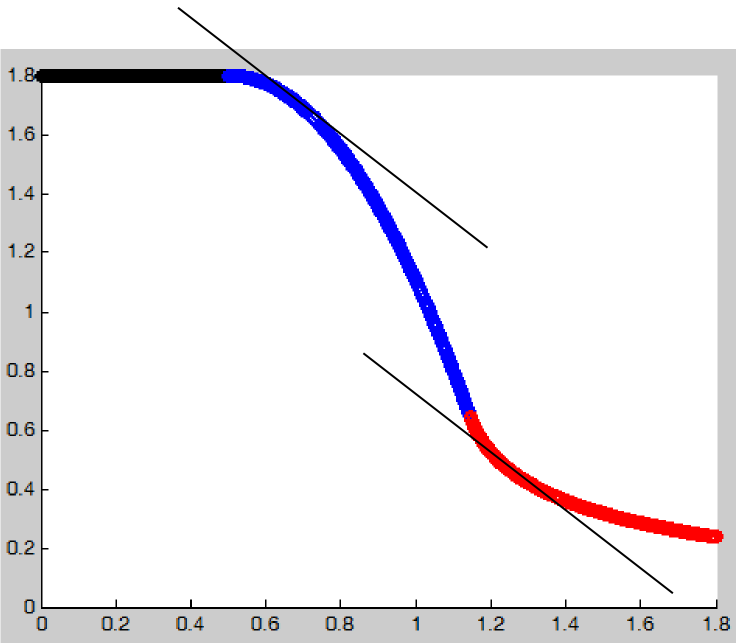
CMOS inverter

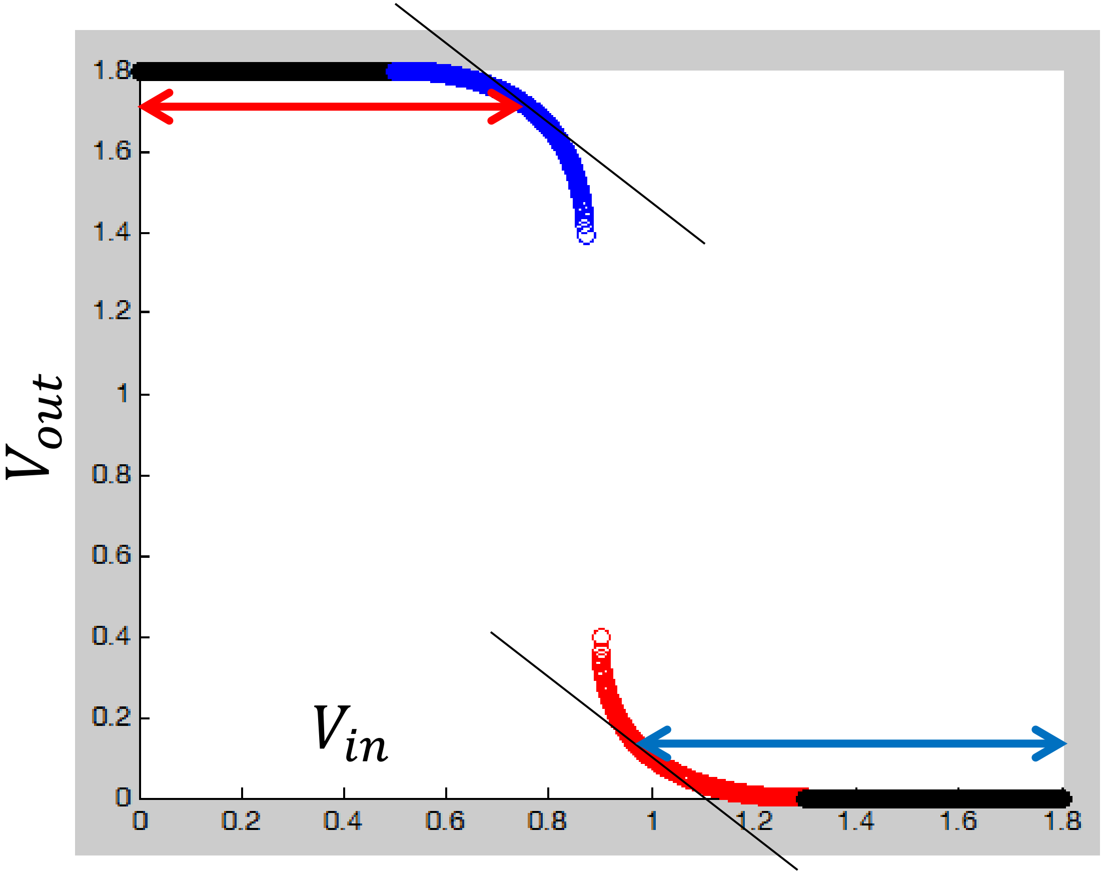
- Voltage transfer curve of a CMOS inverter



Noise margin?

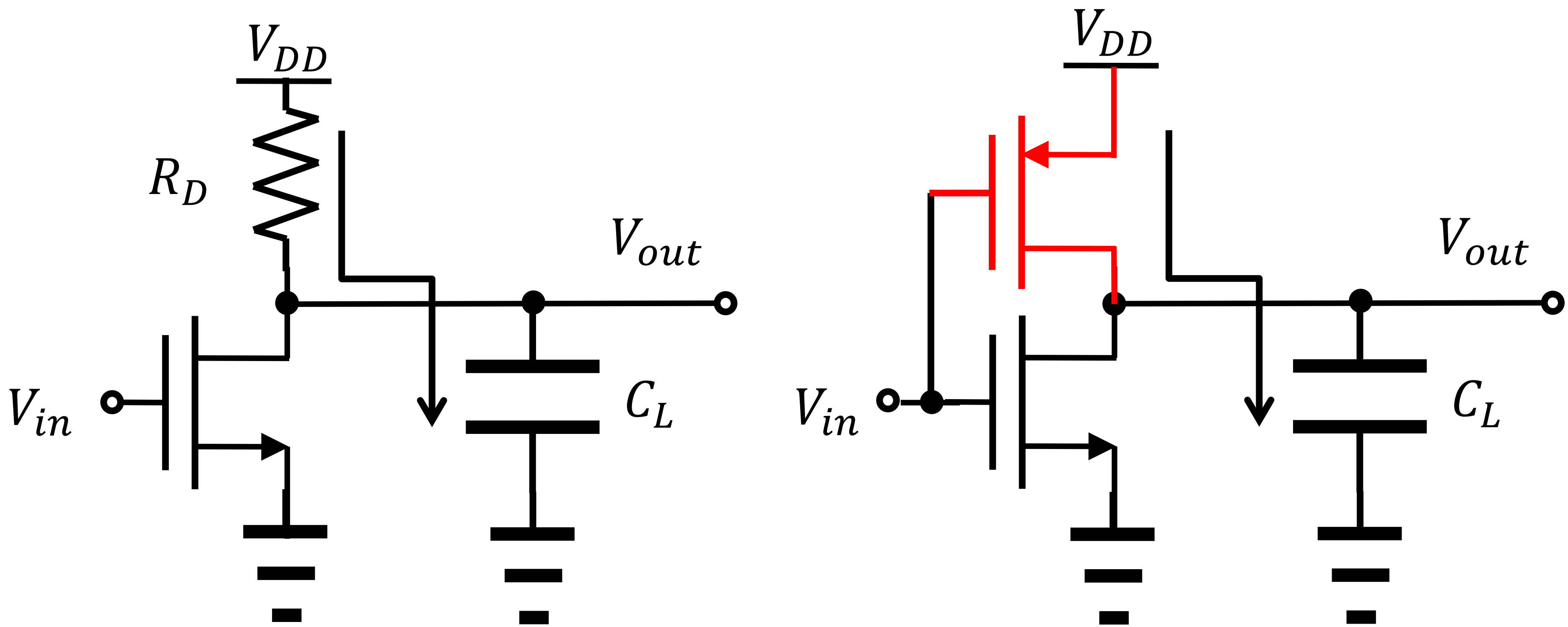
- Greatly improved!
  - Steeper transition





Speed of CMOS inverter (1/4)

- Consider the input transition from HIGH to LOW.
  - Instead of the resistor (R_D), now the PMOS pulls up the V_{out}.

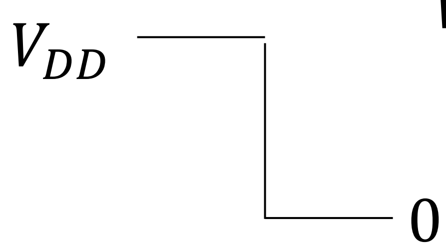


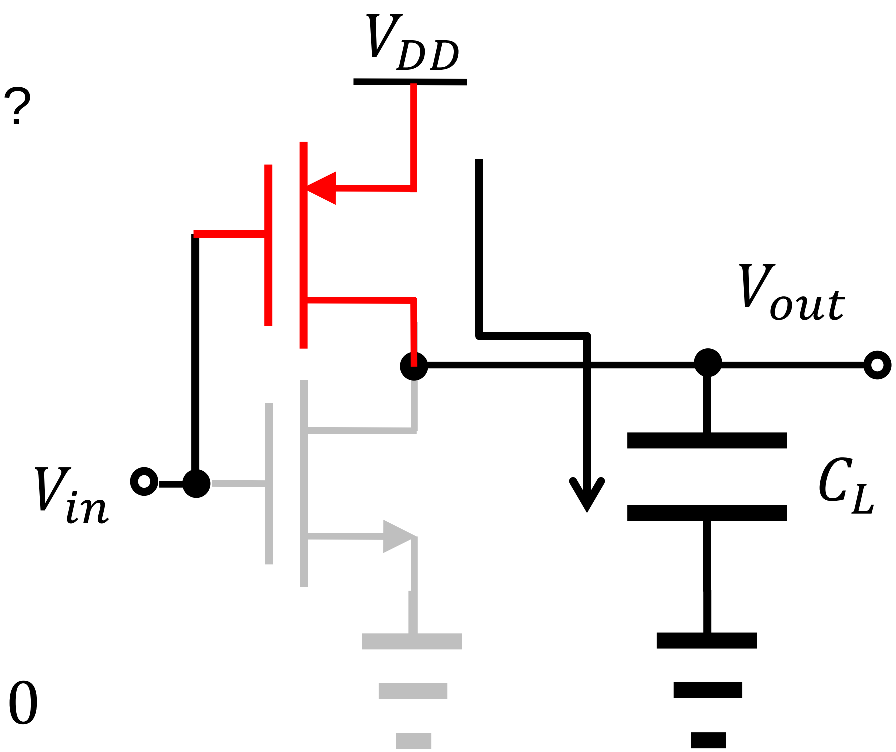
Speed of CMOS inverter (2/4)

- Guess the charging speed.
  - The PMOS current matters. ($I_{PMOS} = C_L \frac{dV_{out}}{dt}$)
  - Initially, the PMOS is in the saturation.
  - Later, the PMOS is in the triode.
  - When does the transition happen?

$V_{in} - V_{DD} - V_{TH2} = V_{out} - V_{DD}$

  - Therefore, when $V_{out} = -V_{TH2}$



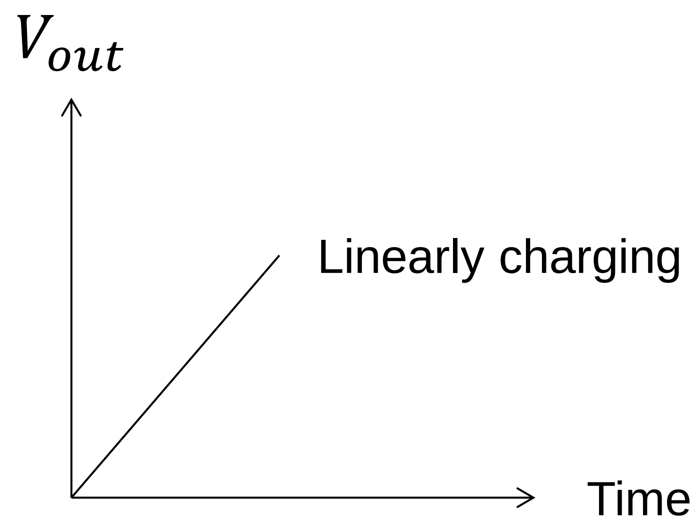


Speed of CMOS inverter (3/4)

- The first case (charge up to $-V_{TH2}$)
  - PMOS saturation current (constant)
  - Time to reach $|V_{TH2}|$

$$T_{PLH1} = \frac{C_L|V_{TH2}|}{\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{DD} - |V_{TH2}|)^2}$$

$$T_{PLH1} = R_{on2}C_L\frac{2|V_{TH2}|}{V_{DD} - |V_{TH2}|}$$



Speed of CMOS inverter (4/4)

- The second case (charge up to $\frac{V_{DD}}{2}$)
  - PMOS triode current

$$\frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(V_{DD}-|V_{TH2}|)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2]=C_L\frac{dV_{out}}{dt}$$

  - Time to reach $\frac{V_{DD}}{2}$

$$T_{PLH2}=R_{on2}C_L\ln\left(3-4\frac{|V_{TH2}|}{V_{DD}}\right)$$

- The overall propagation delay is
  - $T_{PLH}=R_{on2}C_L\left[\frac{2|V_{TH2}|}{V_{DD}-|V_{TH2}|}+\ln\left(3-4\frac{|V_{TH2}|}{V_{DD}}\right)\right]$

Power consumption

- No static power dissipated!
  - Only the “dynamic” power dissipation is determined.
  - High ➔ Low ➔ High ➔ …
  - It involves charging and discharging the load capacitance.
  - The energy stored in the load capacitance

$$\frac{1}{2}C_L V_{DD}^2$$

  - The energy dissipated by the PMOS is also $\frac{1}{2}C_L V_{DD}^2$.
  - Therefore, $C_L V_{DD}^2$ is dissipated during T_{in}.

$$P_{av} = f_{in} C_L V_{DD}^2$$

Homework#10, the final

- Due: 09:00, **June 3 (Mon)**
- Solve the following problems of the final exam in <u>2018</u>.
  - P26
  - P27
  - P28
  - P29
  - P30