Final exam, Electronic Circuits, Spring semester, 2018

June 11, 2018

We have 40 questions. The exam ends at AM 10:40. Write down your answers on the answer sheets. Explicitly show the unit of your answer. For each question, use the designated answer slot.

In the final exam, no partial credit will be given.

When the numbers are provided, just answer a numerical value and a correct unit.

If not stated otherwise, use the long-channel IV characteristics of MOSFETs. (Neglect the channel length modulation.)

If not stated otherwise, include the output resistance in the small-signal MOSFET model.

Some useful facts are summarized below:

For a resistor, $V = IR$. For a capacitor, $I = C\,dV/dt$. For an inductor, $V = L\,dI/dt$.

A good value for the thermal voltage, V_T, at room temperature is 0.02585 V. You may use an approximate value.

Approximately, $\ln 10 \approx 2.3$. Moreover, $e^{-0.7} \approx 0.5$.

The vacuum permittivity is approximately $8.85 \times 10^{-12}\ \mathrm{F/m}$.

The (absolute) elementary charge is approximately $1.6 \times 10^{-19}\ \mathrm{C}$.

At a given time, the power dissipation is defined by $P(t) = I(t)V(t)$.

At room temperature, the intrinsic carrier density of silicon, n_i, is 10^{10} /cm^3.

The built-in potential in a pn junction is given by $V_0 = V_T \ln \frac{N_A N_D}{n_i^2}$.

1. A PMOSFET with a threshold voltage of -0.7 V has its source connected to ground. When the gate voltage is -1.2 V, what is the highest voltage allowed at the drain while the device operates in the saturation region?

2. The drain current in Problem 1 (the saturation current) is known to be -1 mA. Then, what would the drain current be for the drain voltage of -50 mV?

3. Consider a circuit. The threshold voltage of the NMOSFET is 1.5 V. $\mu_n C_{ox} \frac{W}{L} = 0.25\ \mathrm{mA/V^2}$. Calculate the gate voltage.

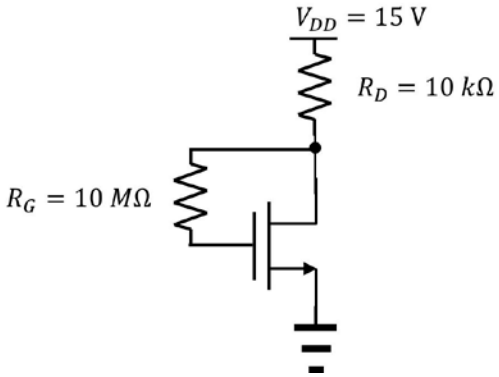

Fig. P3

4. The circuit in Fig. P3 is used for the common-source amplifier. A resistive load of 10 $\mathrm{k\Omega}$ is used. The output resistance of the NMOSFET is $47\ k\Omega$. Calculate the voltage gain.

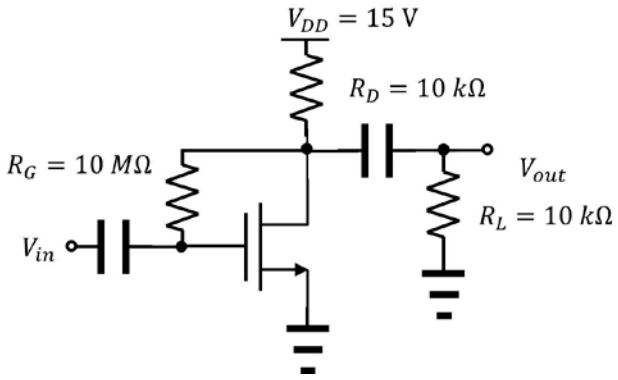

Fig. P4

5. A common-source amplifier utilizes a NMOSFET biased at 0.25 mA with $V_{GS} - V_{TH} = 0.25$ V. The NMOSFET is in the saturation region. The output resistance of the MOSFET is $200\ k\Omega$. The drain resistance is $20\ k\Omega$. Calculate the voltage gain with a correct sign.

6. Consider the same amplifier in Problem 5. A load resistance of $20\,k\Omega$ is additionally connected to the output. (Of course, a large capacitor is also used.) Calculate the voltage gain with a correct sign.

7. A common-source amplifier with a source-degeneration resistance, R_S, utilizes a NMOSFET biased at 0.25 mA with $V_{GS} - V_{TH} = 0.25\,\text{V}$. The NMOSFET is in the saturation region. Ignore the output resistance of the MOSFET. The drain resistance is $20\,k\Omega$ and a load resistance is also $20\,k\Omega$. Assume that $R_S = 1.5\,k\Omega$. Calculate the voltage gain with a correct sign.

8. Consider the following circuit. The threshold voltage of the MOSFET is 1.0 V. Its $\mu_n C_{ox}\frac{W}{L}$ is $1\,\text{mA/V}^2$. What is the gate voltage?

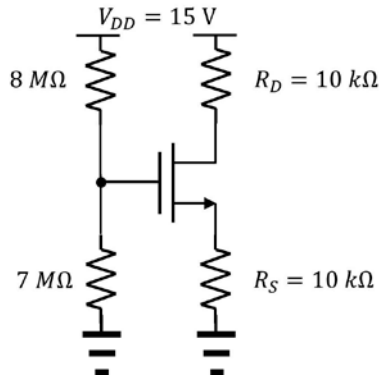

Fig. P8

9. Consider the same circuit in Problem 8. Calculate the drain current.

10. Consider the following circuit. The threshold voltage of the NMOSFET is 1.0 V and $\mu_n C_{ox}\frac{W}{L}$ is $1\,\text{mA/V}^2$. Find out the value for R_D to have a dc drain current of 0.5 mA.

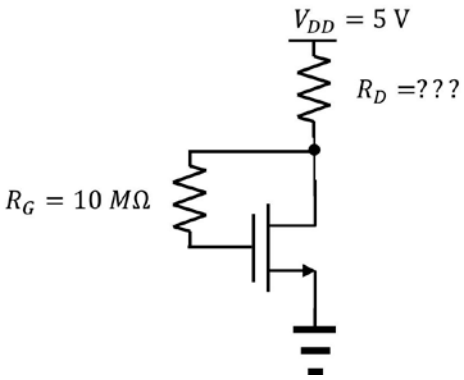

Fig. P10

11. Consider the following circuit. The threshold voltage of the NMOSFET is 1.5 V and $\mu_n C_{ox} \frac{W}{L}$ is $1\ \mathrm{mA/V^2}$. Calculate the source voltage.

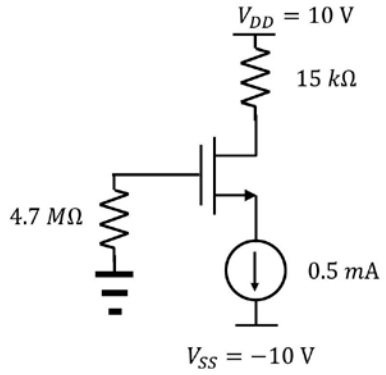

Fig. P11

12. Consider the following circuit. $\mu_n C_{ox} = 20\ \mu\mathrm{A/V^2}$ and $\mu_p C_{ox} = 8\ \mu\mathrm{A/V^2}$. The threshold voltage of the NMOSFET and the PMOSFET are +1.0 V and -1.0 V, respectively. Two MOSFETs have the same length, $10\ \mu\mathrm{m}$. The width of the NMOSFET is $30\ \mu\mathrm{m}$, while that of the PMOSFET is $75\ \mu\mathrm{m}$. Calculate the node voltage of the shared drain.

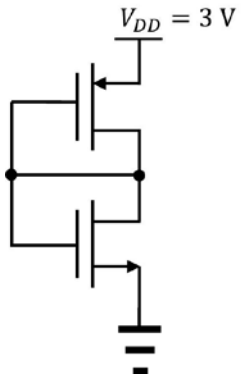

Fig. P12

13. Consider the following circuit. The threshold voltage of the NMOSFET is 0.7 V. $\mu_n C_{ox} = 200\,\mu\text{A}/V^2$. The length and width of the transistor are $1\,\mu\text{m}$ and $10\,\mu\text{m}$, respectively. Calculate the drain current.

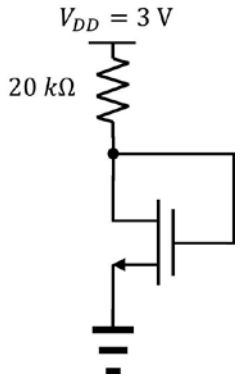

Fig. P13

14. The circuit in Problem 13 is expanded. The left part is taken from Fig. P13. The size of the left NMOSFET is the same as before. The right NMOSET has the same parameters, except for the width of $50\,\mu\text{m}$. Calculate the drain current of the right NMOSFET.

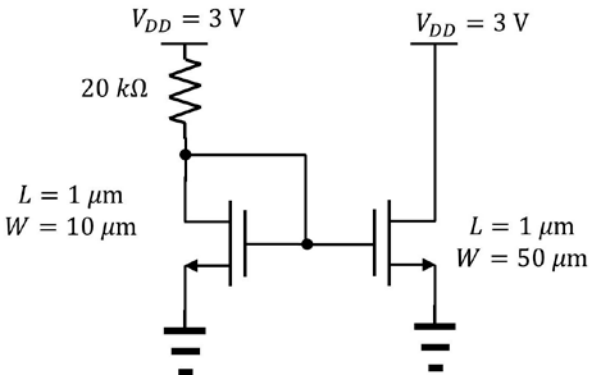

Fig. P14

15. Consider a NMOSFET in the saturation region. Neglect the output resistance of the transistor, as usual. Assume that the gate voltage varies with $V_{GS}(t) = V_{GS,DC} + v\cos\omega t$. When v is not zero, the time-averaged drain current is increased. Express such an incremental drain current in terms of usual device parameters and v.

16. You have a NMOSFET and a resistor. Implement a NOT logic gate with them. (In other words, draw the circuit schematic.) Identify your input bits and output bit.

17. You have two NMOSFETs and a resistor. Implement a NAND logic gate with them. Identify your input bits and output bit.

18. You have two NMOSFETs and a resistor. Implement a NOR logic gate with them. Identify your input bits and output bit. Remember that the NOR is the inverted OR.

19. The NAND gate is a universal logic gate. You have two input bits, x and y. Implement an AND gate with the NAND gates. Draw the circuit schematic.

20. The NAND gate is a universal logic gate. You have two input bits, x and y. Implement an XOR (exclusive OR) gate with the NAND gates. Draw the circuit schematic.

21. A CMOS inverter is shown. The threshold voltage of the NMOSFET is 0.5 V. The threshold voltage of the PMOSFET is -0.5 V. The input voltage is 0.0 V. Calculate the output voltage.

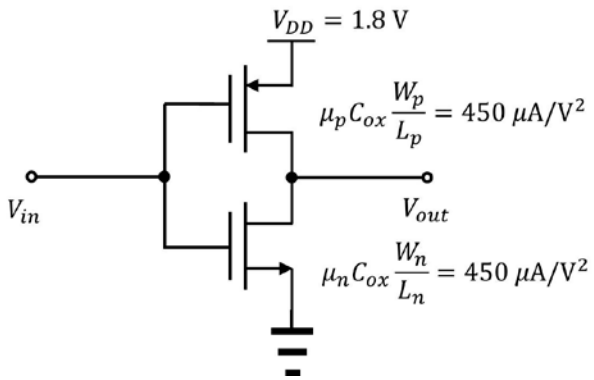

Fig. P21

22. Repeat Problem 21 for an input voltage of 0.8 V.

23. Repeat Problem 21 for an input voltage of 0.9 V.

24. Calculate the noise margin for low input, NM_L.

25. Using the same NMOSFET and PMOSFET used in Problem 21, a common-source amplifier with a PMOS load has been designed. We want to use it for a certain voltage range where the (absolute value of the) voltage gain is larger than 1. Calculate the width of such a voltage range.

26. A NMOS inverter is shown below. The threshold voltage of the NMOSFET is 0.5 V. $V_{DD} = 1.8\,\text{V}$, $\mu_n C_{ox} = 300\,\mu\text{A}/V^2$, and $\frac{W}{L} = 1.5$. Assume that $R_D = 25\,k\Omega$. When the input voltage is equal to 1.8 V, calculate the output voltage.

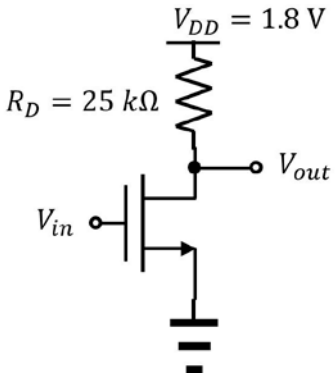

Fig. P26

27. Consider the same situation in Problem 26. Calculate the power dissipated by the inverter (both of the NMOSFET and the resistor).

28. Consider the very similar situation in Problem 26. The same NMOSFET is used. Also the initial input voltage is 1.8 V. However, we have a load capacitor, whose capacitance is $10\,f\text{F}$. At $t = 0$, the input voltage is suddenly decreased to zero. Calculate the capacitor voltage at $t = 173$ psec.

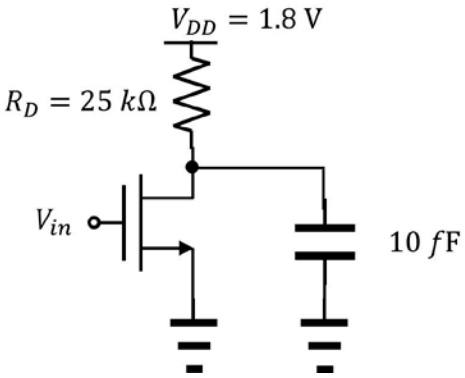

Fig. P28

29. Instead of the resistive load, a NMOSFET is used as an active load. $V_{DD} = 1.8\,\text{V}$. For every NMOSFET, the threshold voltage of the NMOSFET is 0.5 V, $\mu_n C_{ox} = 300\,\mu\text{A}/V^2$, and $\frac{W}{L} = 1.5$. When the input voltage is equal to 1.8 V, calculate the output voltage.

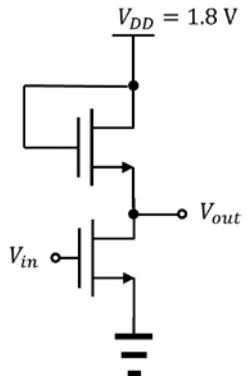

Fig. P29

30. Consider the same situation in Problem 29. Calculate the power dissipated by the inverter.

31. An ideal op amp has some properties. Describe an ideal op amp in terms of its gain, input impedance, output impedance, and speed.

32. The unit gain buffer is shown. Assume a finite open-loop gain, A_0. Express the voltage gain as a function of A_0 with a correct sign.

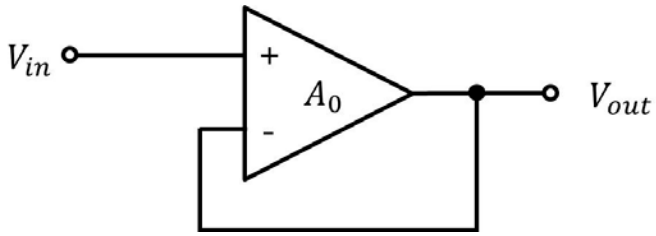

Fig. P32

33. Consider the following circuit. A source whose voltage is 1 V and resistance is $1\,\mathrm{M}\Omega$ is connected to the unit gain buffer. The open-loop gain is 100. The output impedance of the op amp is $75\,\Omega$. A load resistance of $1\,k\Omega$ is used. Calculate the output voltage in the mV unit.

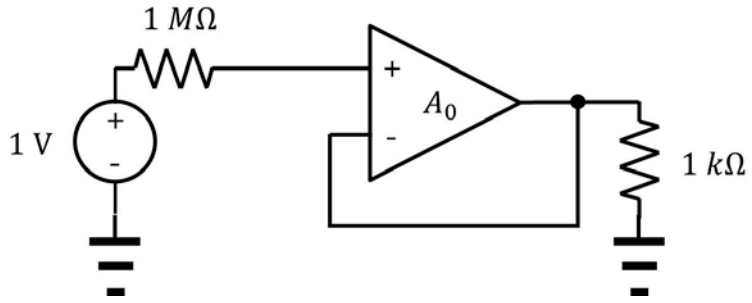

Fig. P33

34. Repeat Problem 33 with a smaller load resistance of $75\,\Omega$. Calculate the output voltage in the mV unit.

35. A noninverting amplifier is shown. Assume a finite open-loop gain, A_0. Express the closed-loop gain as a function of A_0, R_1, and R_2.

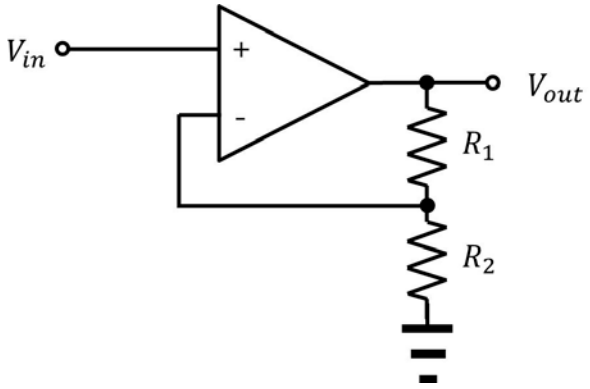

Fig. P35

36. Consider the same noninverting amplifier. In addition to the open-loop gain, consider the input resistance, R_{in}, and the output resistance, R_{out}. Express the closed-loop gain as a function of A_0, R_1, R_2, R_{in}, and R_{out}.

37. Assume an ideal op amp. Express the output voltage as a function of two input voltages.

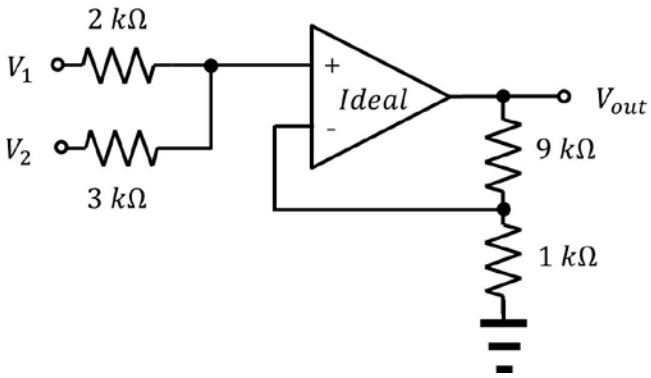

Fig. P37

38. Assume an ideal op amp. Express the voltage gain in terms of four resistances.

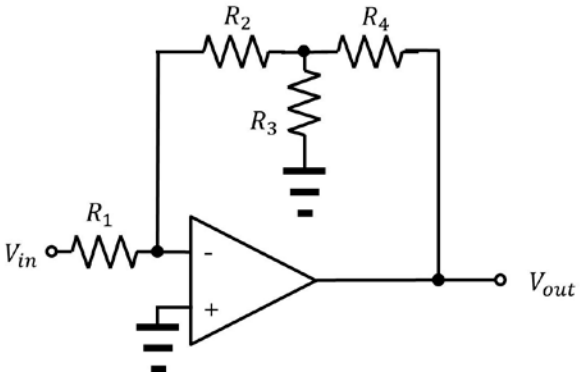

Fig. P38

39. Consider the RC circuit shown below. The input voltage has been kept as zero. At $t = 0$, the voltage is suddenly increased to 5 V. Calculate the output voltage at $t = 0.7$ msec.

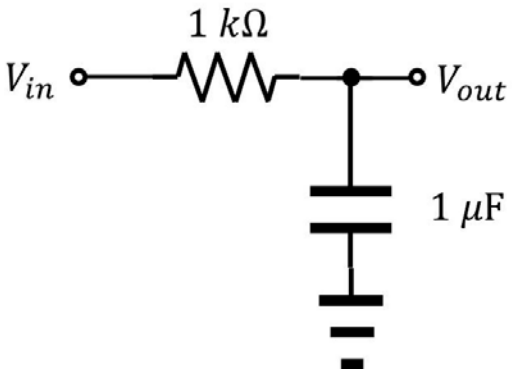

Fig. P39

40. Consider an op amp circuit shown below. Assume an ideal op amp. Initially, the output voltage was zero. At $t = 0$, the voltage is suddenly increased to 5 V. Calculate the output voltage at $t = 0.7$ msec.

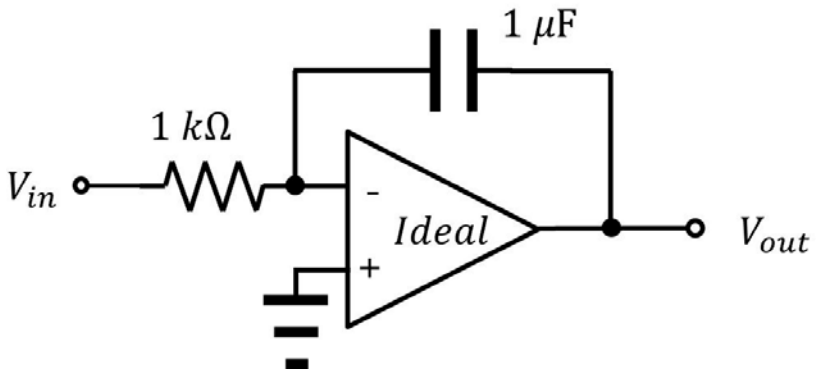

Fig. P40