Lecture25:
NAND gate

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Electrical Engineering and Computer Science
Gwangju Institute of Science and Technology

Power consumption

- No static power dissipated!
  - Only the “dynamic” power dissipation is determined.
  - High ➔ Low ➔ High ➔ …
  - It involves charging and discharging the load capacitance.
  - The energy stored in the load capacitance

$$\frac{1}{2} C_L V_{DD}^2$$

  - The energy dissipated by the PMOS is also $\frac{1}{2} C_L V_{DD}^2$.
  - Therefore, $C_L V_{DD}^2$ is dissipated during T_{in}.

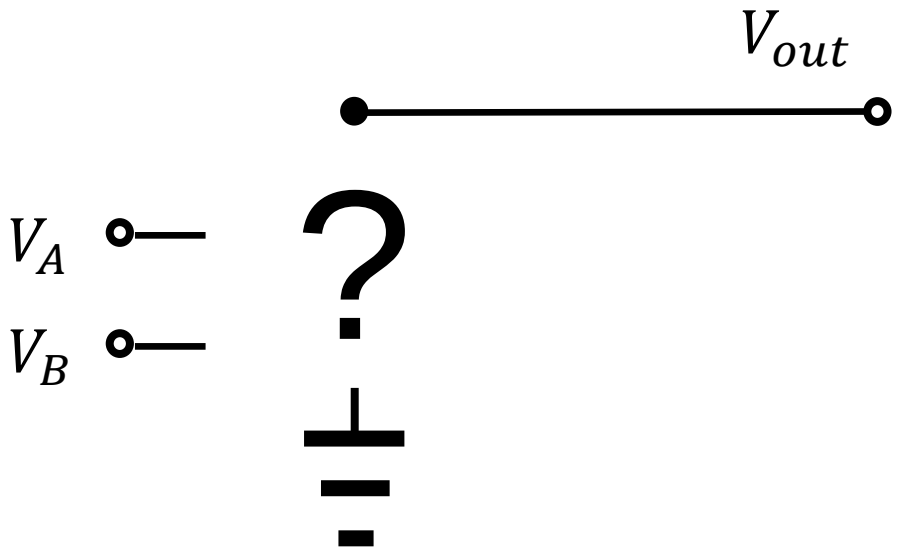
$$P_{av} = f_{in} C_L V_{DD}^2$$

NAND gate (1/4)

- Its truth table

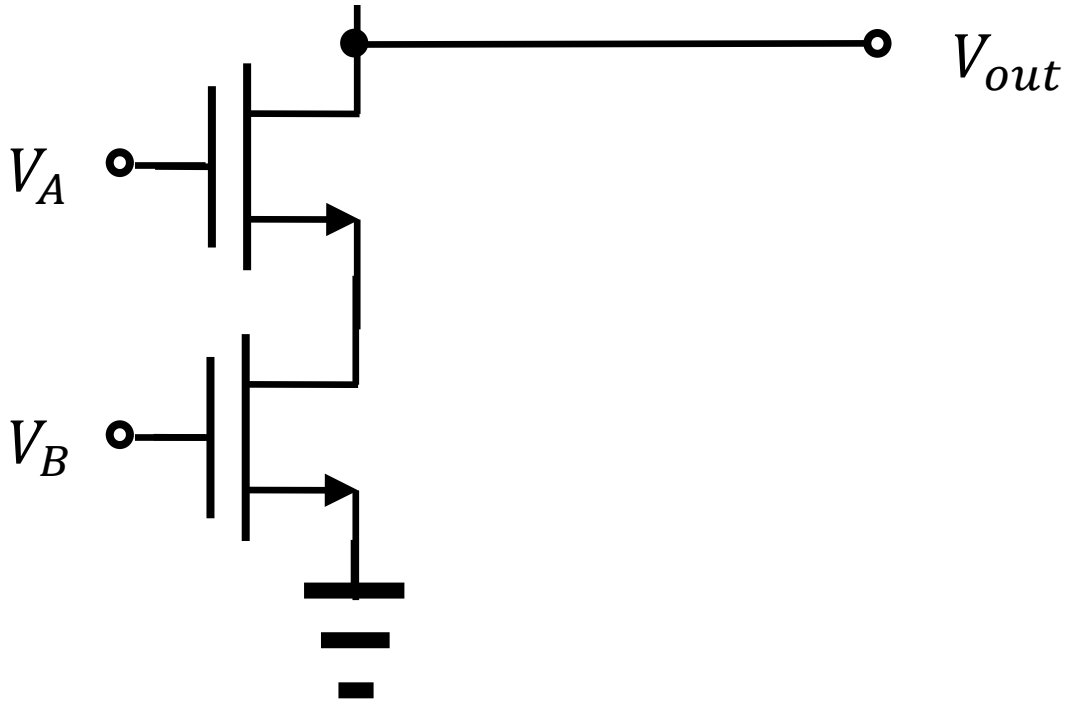
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

  - Only when two inputs are 1, the output node is connected to GND.



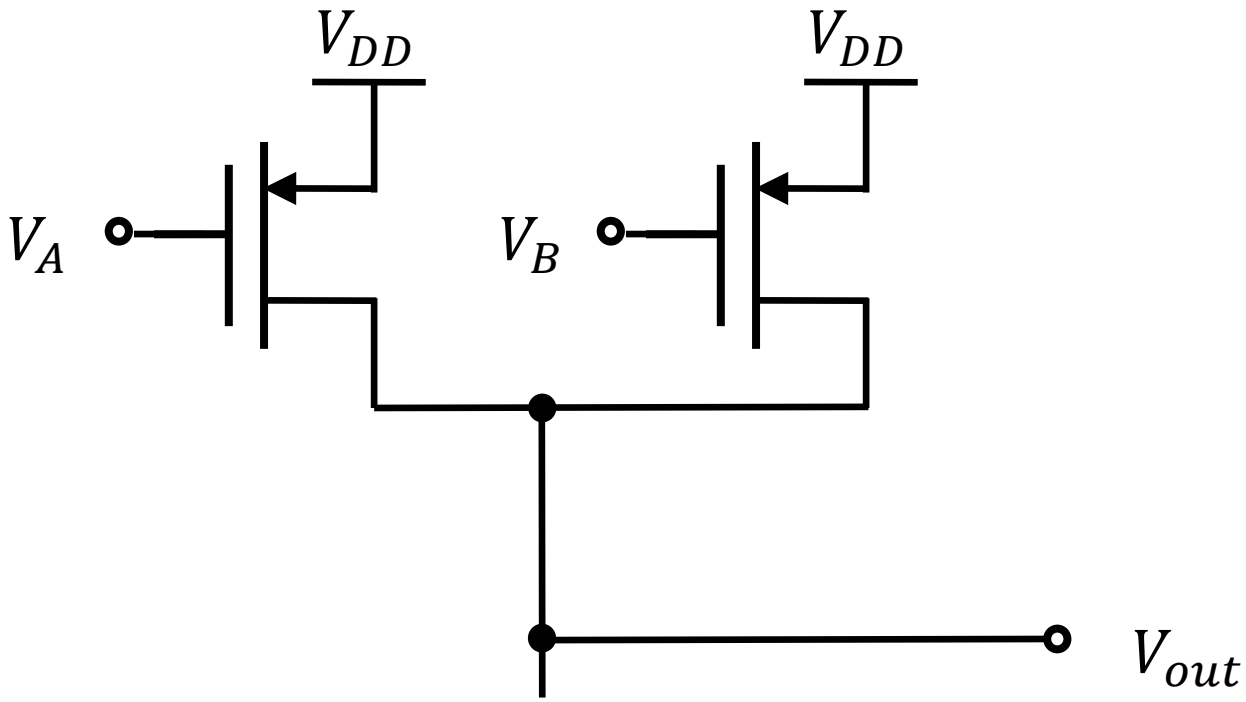
NAND gate (2/4)

- It is easy to realize that the serially connected NMOSFETs can do it.
  - When one of V_A or V_B is low, no electric connection between V_{out} and GND.



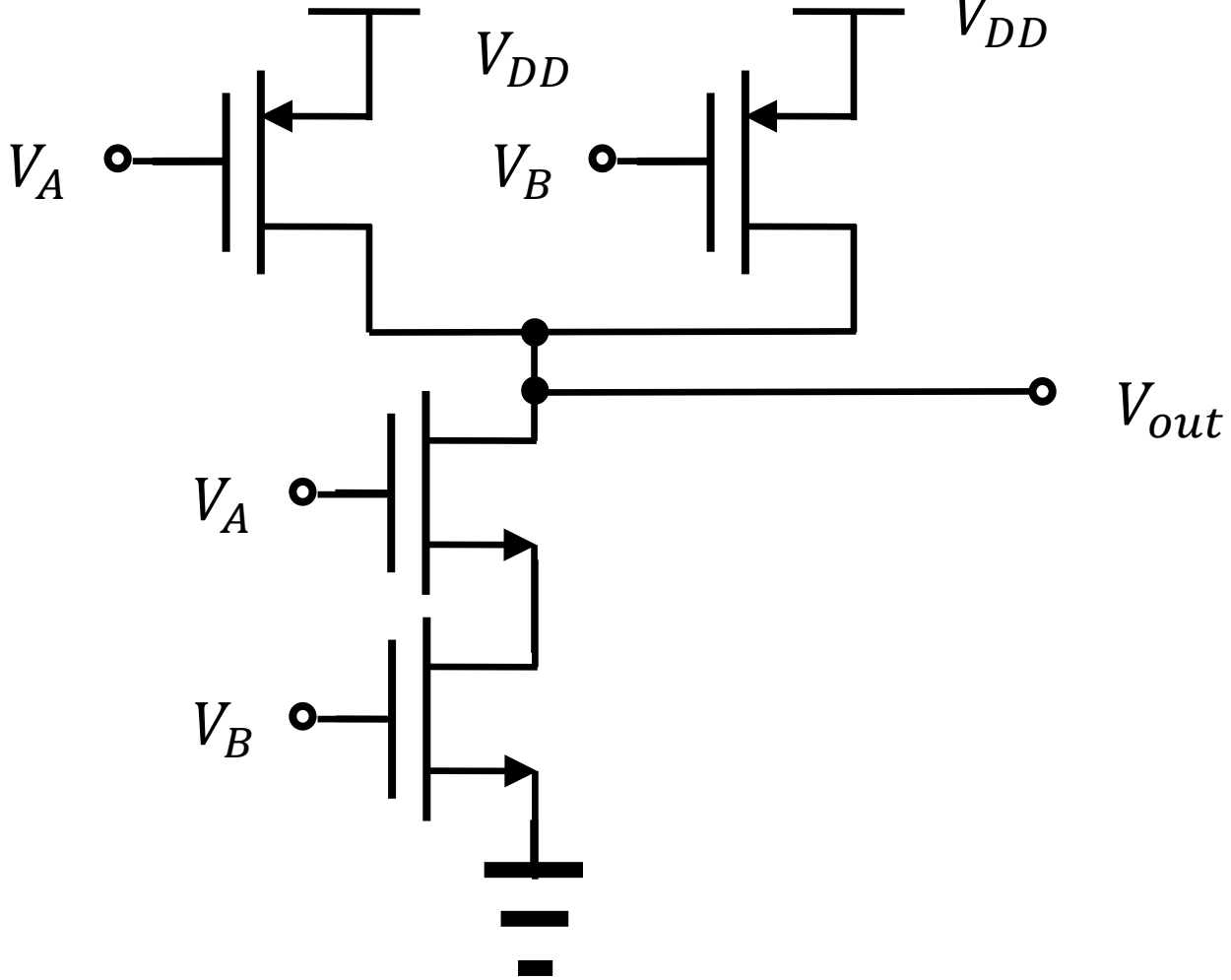
NAND gate (3/4)

- Similarly, the output node is not connected to V_{DD}, when two inputs are 1.
- It is easy to realize that the parallel connected NMOSFETs can do it.



NAND gate (4/4)

- Overall, the NAND gate looks like:



NOR gate

- Dual to the NAND gate
  - Serial PMOS
  - Parallel NMOS
- Which one is weaker?
  - Pull-up? Pull-down?