Lecture15:
CMOS amplifiers (2)

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Turning point

- We have only 12 lectures ahead!

🡐 Tsukuba Marathon 2011 turning point (from Wikimedia Commons)

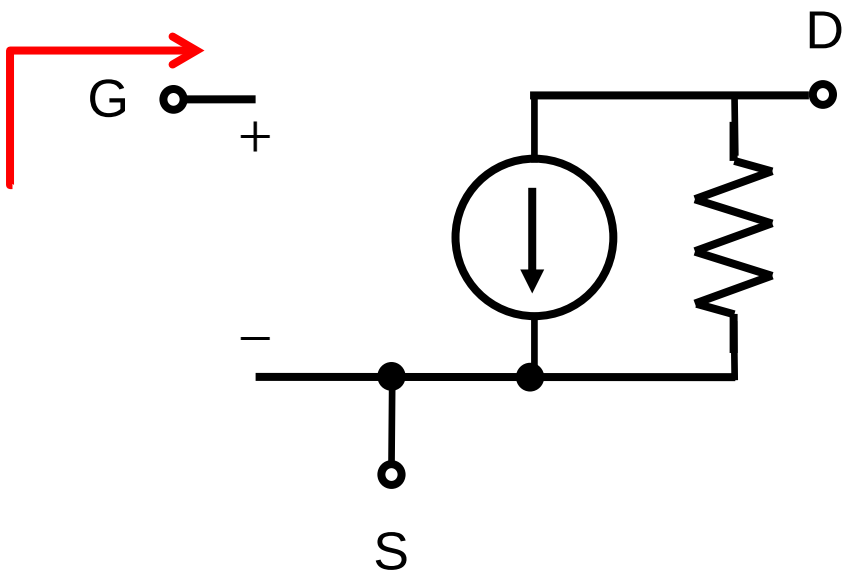
Things to be covered…

- We will cover:
  - Ch. 17
  - Ch. 4
  - Ch. 5
  - Ch. 8
  - Ch. 16 (It depends on the lecture progress.)

Mon	Tue	Wed	Thu	Fri	Sat	Sun
L15(4.27)		L16(4.29)				
L17(5.4)		L18(5.6)				
L19(5.11)		L20(5.13)				
L21(5.18)		L22(5.20)				
		L23(5.27)				
L24(6.1)		L25(6.3)				
L26(6.8)		**Final**				

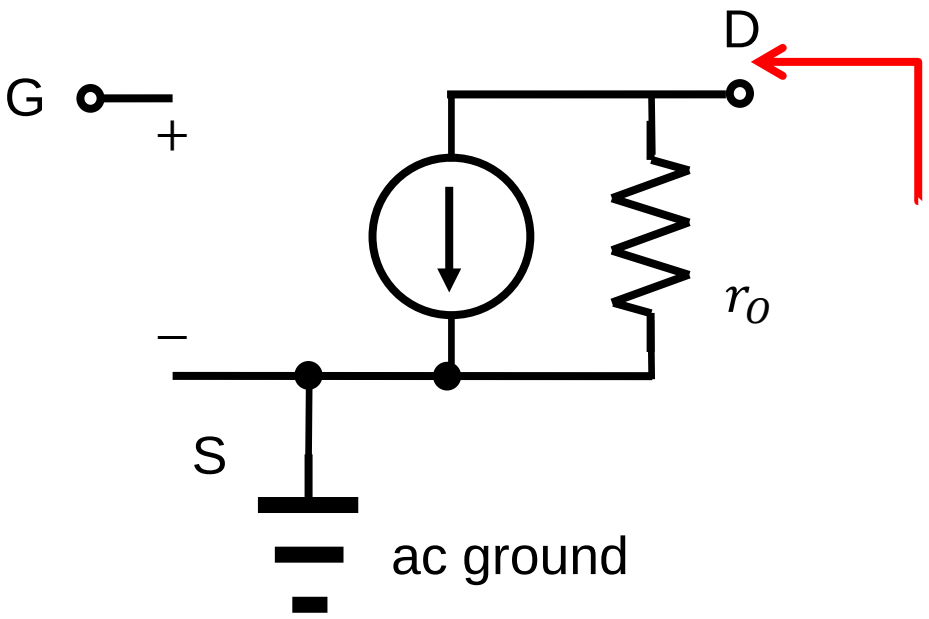
Impedances (1/3)

- A MOSFET with three terminals
  - Looking into the gate, we see the infinite impedance.
  - (Strictly valid at the low-frequency range)



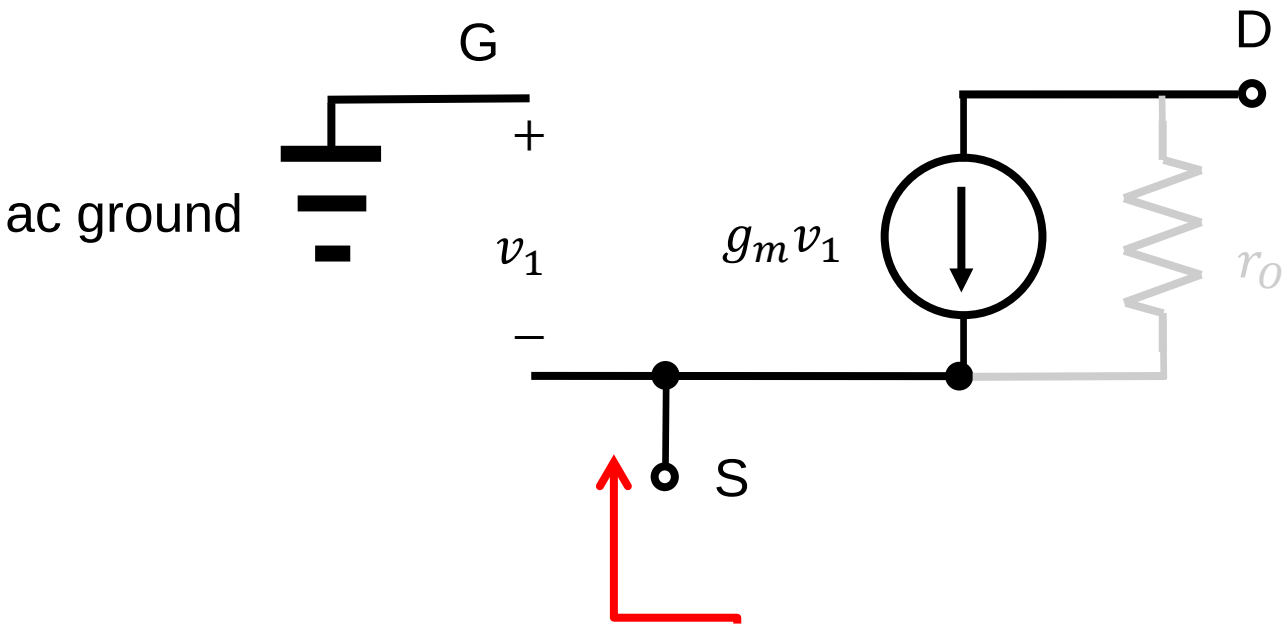
Impedances (2/3)

- A MOSFET with three terminals
  - Looking into the drain, we see r_O if the source is ac grounded.



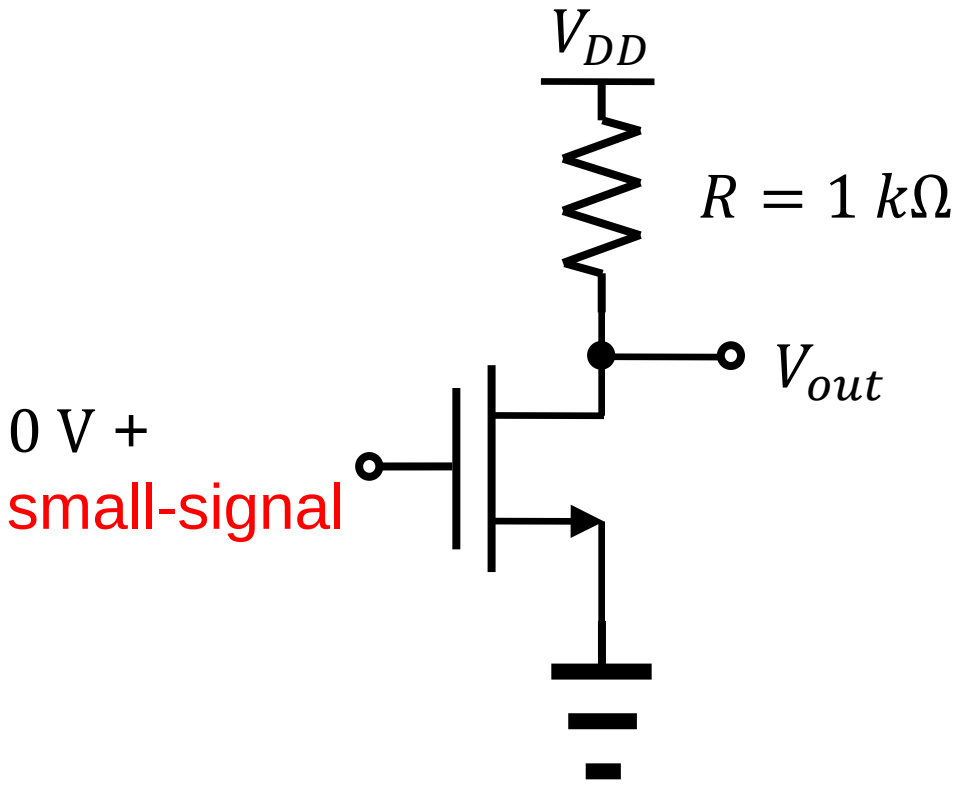
Impedances (3/3)

- A MOSFET with three terminals
  - Looking into the source, we see $1/g_m$ if the gate is ac grounded and channel-length modulation is neglected.



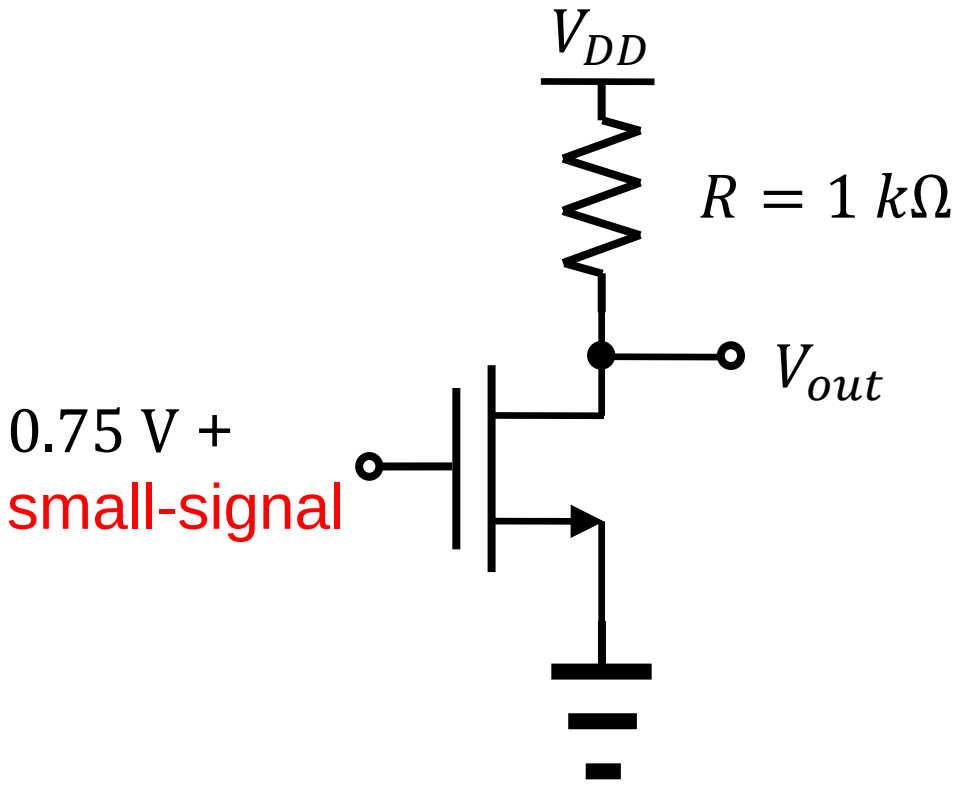
Transistor turned off

- The example 17.5 shows an amplifier circuit.
  - But, the transistor is not turned on.
  - The circuit generates no output signal.



This is a solution.

- The example 16.7 shows a revised circuit.
  - Then, how can we generate 0.75 V, for example?
  - Use of a separate battery can be a way.



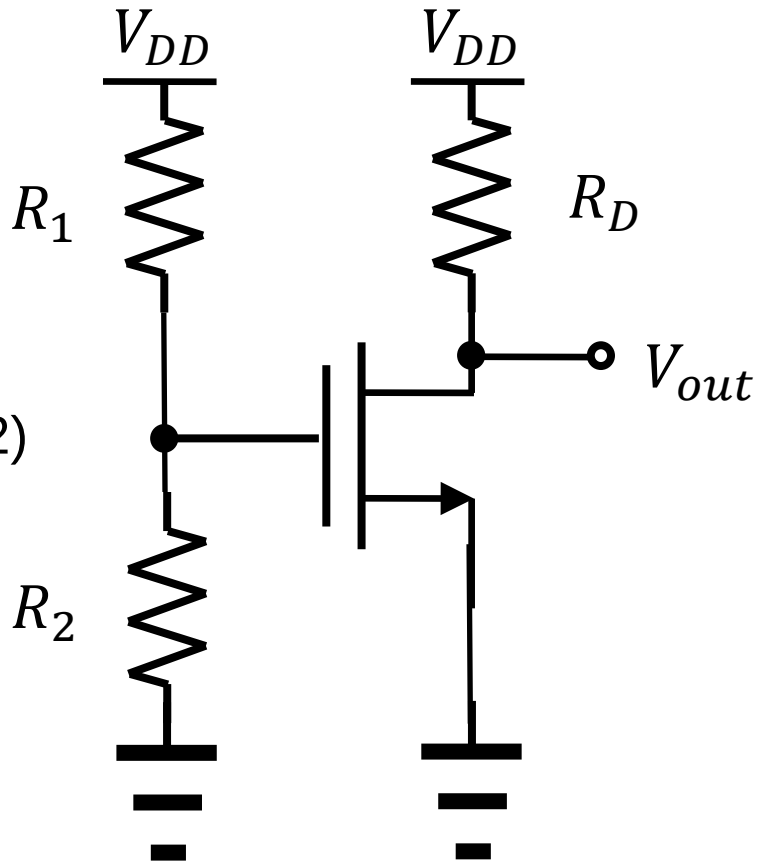
Simple biasing (1/2)

- A better way
  - The gate bias voltage is

$$V_{GS} = \frac{R_2}{R_1+R_2} V_{DD} \qquad (17.10)$$

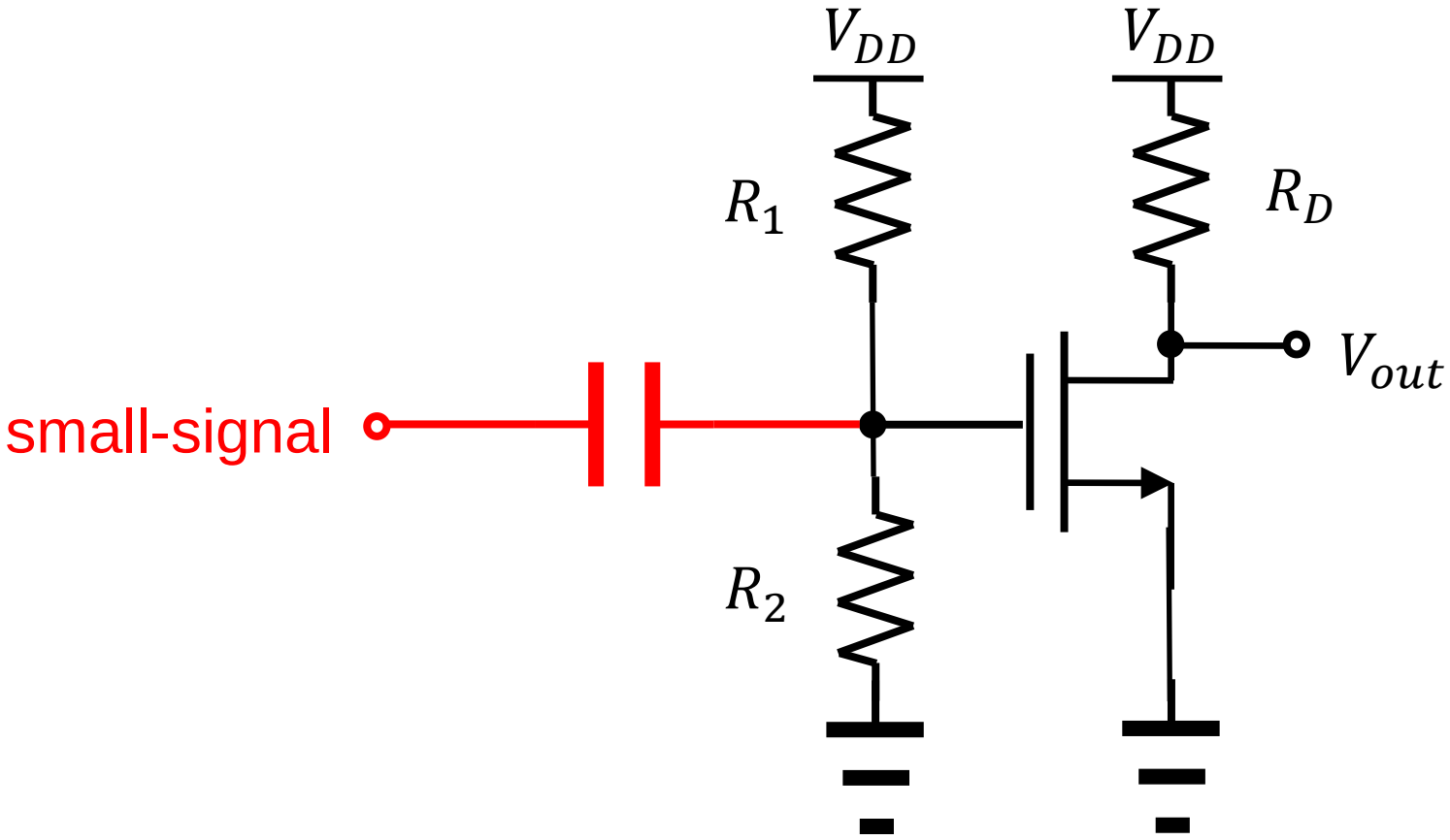
  - The drain current is

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(\frac{R_2}{R_1+R_2} V_{DD} - V_{TH}\right)^2 \qquad (17.12)$$



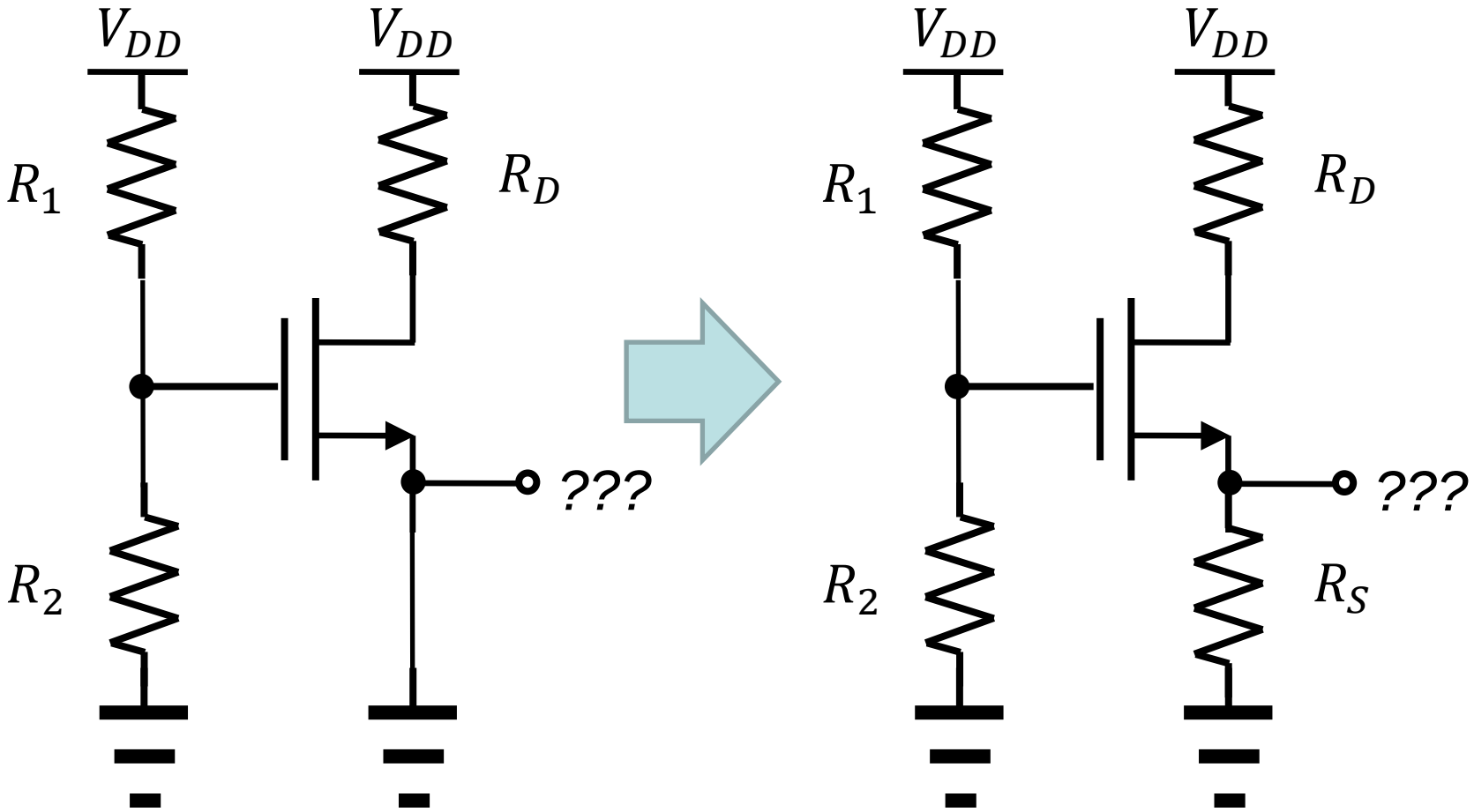
Simple biasing (2/2)

- How to apply the small-signal input
  - Use a capacitor!



Source degeneration (1/2)

- A resistor placed in series with the source terminal



Source degeneration (2/2)

- Now we have to find the source voltage.
  - (Saturation current of the MOSFET) = (Current flowing through R_S)
  - After a simple manipulation, we can find

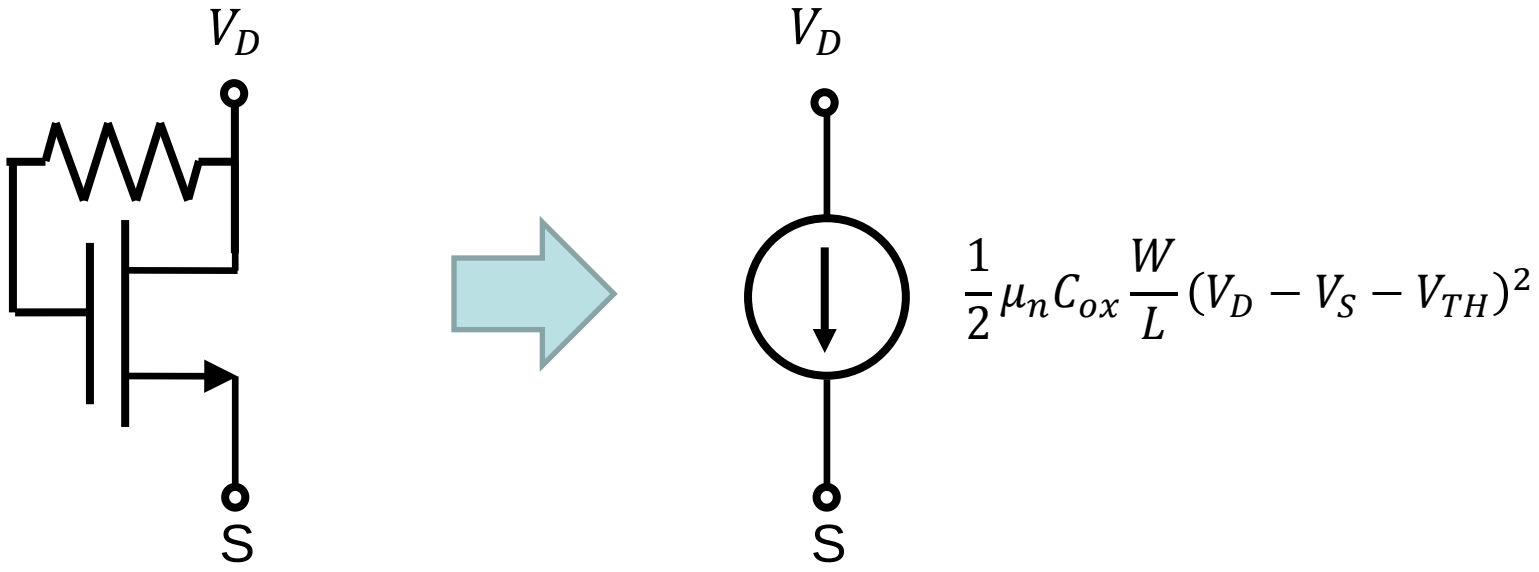
$$V_S = V_G + V_1 - V_{TH} - \sqrt{V_1^2 + 2(V_G - V_{TH})V_1}$$

  - Here,

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_s}$$

Self-biasing

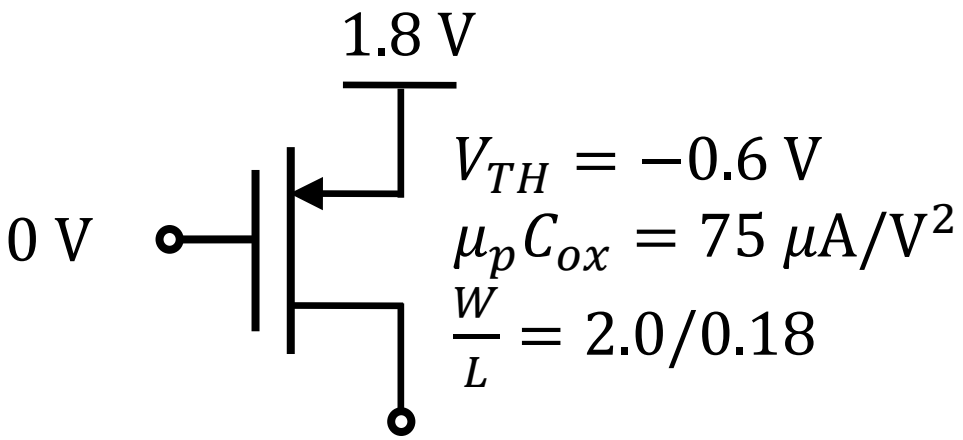
- Already covered in Example 6.13.
  - Always in the saturation region.



Gate and drain are tied.

Biasing of PMOS devices

- Let's recall the problem18 of our mid-term exam.
  - The amount of "gate overdrive" is $1.2\ \mathrm{V}$.
  - It is not $0.6\ \mathrm{V}$.



Read your textbook.

- You can find today's lecture contents in Sec. 17. 2.
  - Up to p. 759

- We will cover Sec. 17. 3 and Sec. 17. 4.
  - Common source
  - Up to p. 766