Lecture8:
Metal-Oxide-Semiconductor

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Parallel plates

- A problem from "General Physics" course.
  - Consider a dielectric layer (whose thickness is d and area is A) sandwiched by two parallel metal plates. Its permittivity is ϵ.
  - A voltage difference, V, is applied.
  - The charges are $+Q$ and $-Q$, respectively.
  - By applying the Gauss law,

$$Q = \epsilon|\mathbf{E}|A = \epsilon\frac{V}{d}A$$

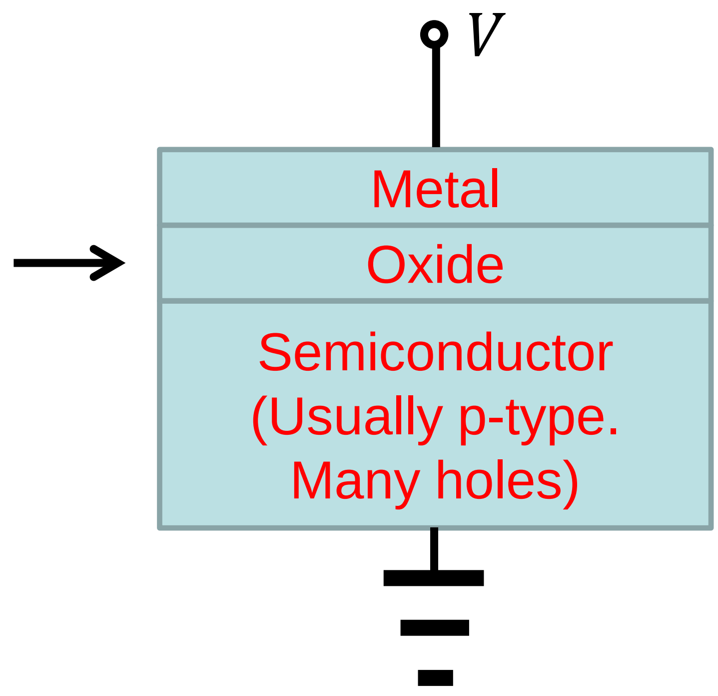
  - Therefore, the capacitance *per unit area* becomes

$$C = \frac{\epsilon}{d}$$

Metal-Oxide-Semiconductor

- The key structure in the microelectronics
  - Question: Is the MOS a capacitor with $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$?
  - Answer: No.

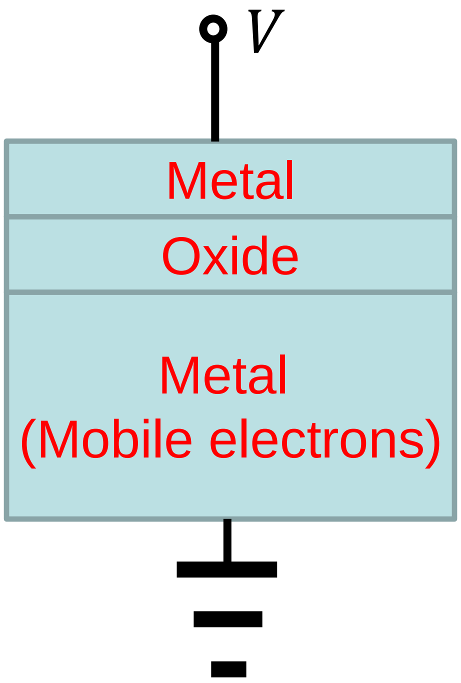
Its thickness, t_{ox}

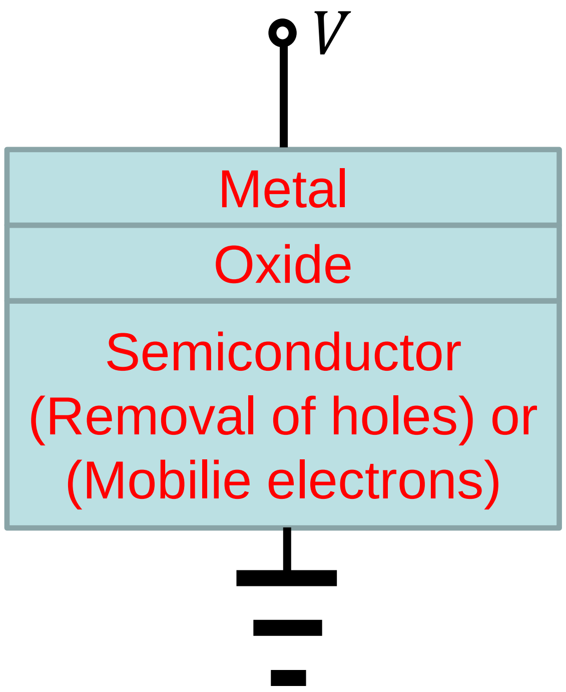


What is the difference?

- Threshold behavior
  - Two ways to provide negative charges
  - Removal of holes
  - Mobile electrons

- Threshold voltage
  - It is written as V_{TH}.
  - Most important!





Inversion?

- Remember that the substrate is doped with the p-type dopants.
  - We expect that the holes are found in the silicon substrate.
  - However, when a sufficiently large gate voltage is applied, the electrons are found, as if it is doped with the n-type dopants.
  - Those electrons are called as the “inversion electrons.”

Electron charge density

- When $V_G < V_{TH}$,
  - The electron charge density vanishes.

$$Q_{elec} = 0$$

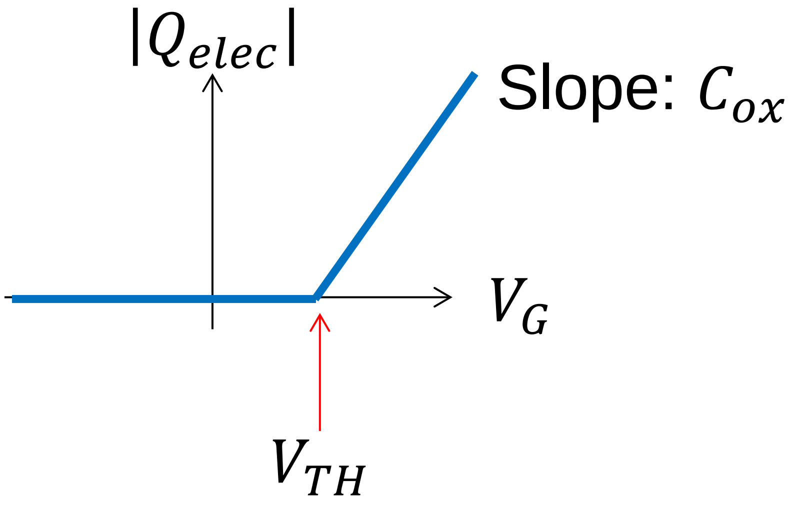
- When $V_G > V_{TH}$,
  - The electron charge density is proportional to $V_G - V_{TH}$.

$$|Q_{elec}| = C_{ox}(V_G - V_{TH})$$

  - (Here, Q_{elec} and C_{ox} are quantites *per area*.)

$|Q_{elec}|$ versus V_G

- It is piecewise linear. Therefore, it is nonlinear.
  - Digital application: ON ($V_G = V_{DD}$) / OFF ($V_G = 0$)
  - Analog application: Linear part

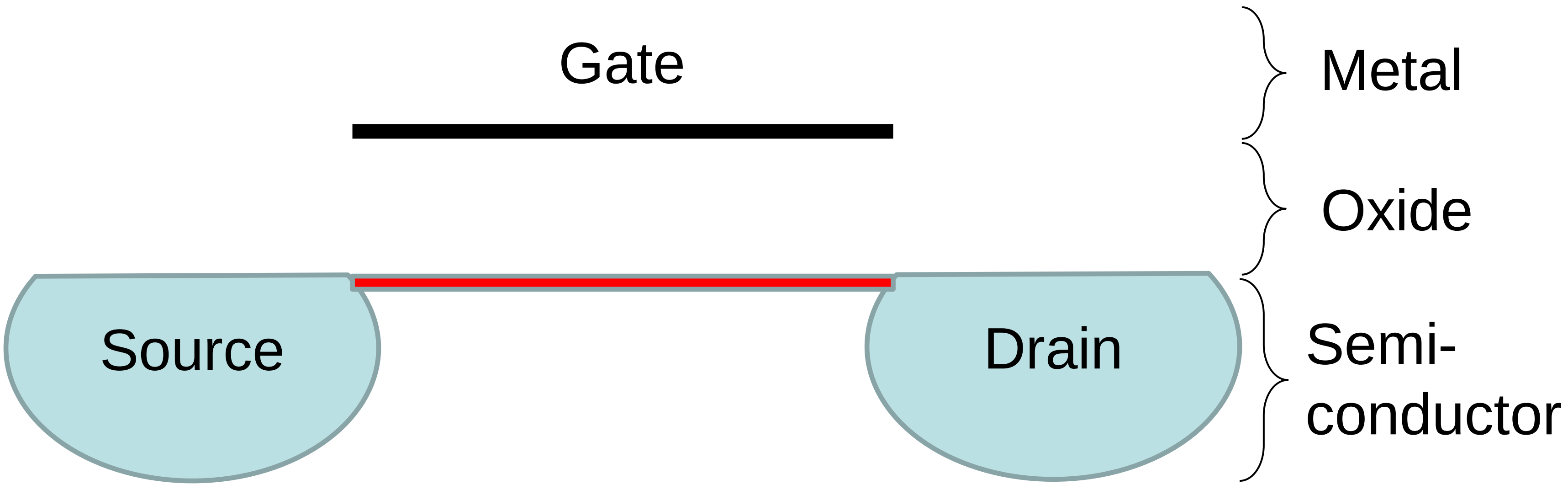


Engineering questions

- Which one is good?
  - Large C_{ox} or small C_{ox}?
  - High V_{TH} or low V_{TH}?

MOS? MOSFET?

- MOS (Metal-Oxide-Semiconductor)
  - By changing the gate voltage, the charge density can be controlled.
- MOSFET (MOS Field-Effect Transistor)
  - Current conduction



Its operation

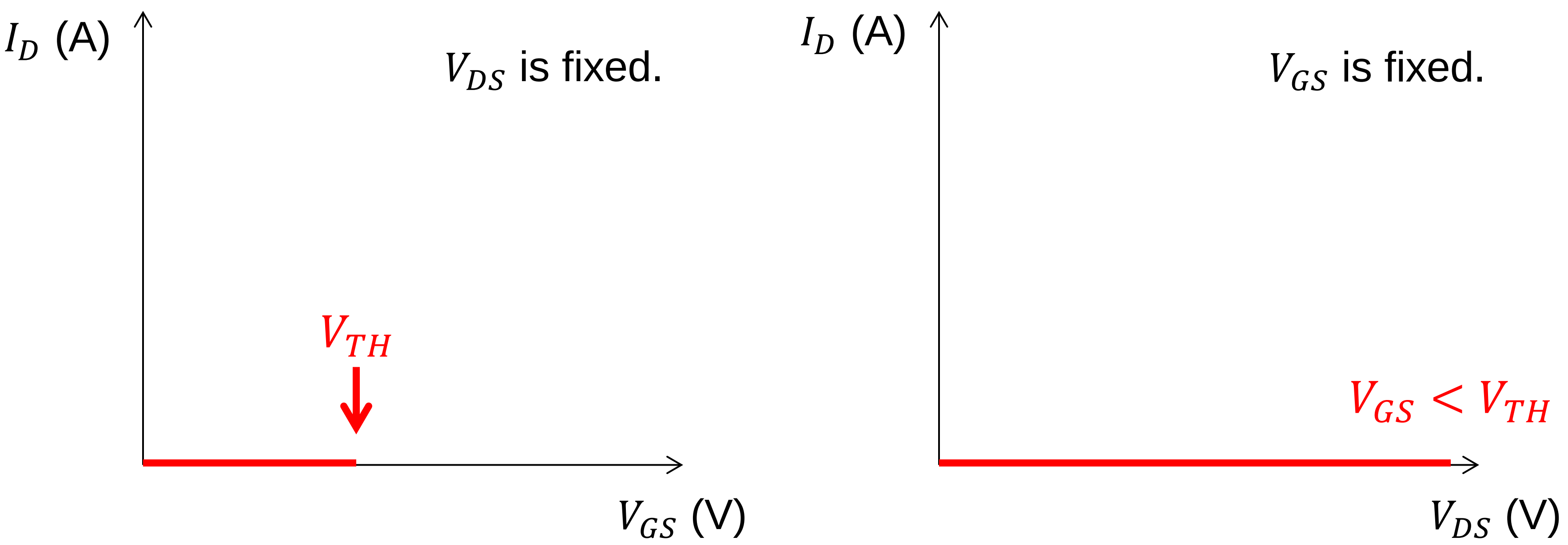
- The MOSFET has three terminals.
  - Source, drain, and gate
  - We always have

$$I_S(t) + I_D(t) + I_G(t) = 0.$$

- At low frequencies, the gate current is zero.
  - Source current + drain current = 0, $I_S + I_D = 0$
  - Source is regarded as the reference contact.
  - Gate voltage (V_{GS}) and drain voltage (V_{DS}) are variables.
- We are interested with $I_D(V_{GS}, V_{DS})$.

IV characteristics

- We will draw the two graphs.
  - $I_D(V_{GS})$ with fixed V_{DS} & $I_D(V_{DS})$ with fixed V_{GS}



Homework#4

- Due: 09:00, April 2
- Solve following problems of the 2018 mid-term exam.
  - P10
  - P16
  - P17
  - P18
  - P19
- Solve following problems of the 2017 mid-term exam.
  - P21
  - P22
  - (The remaining problems in the 2017 mid-term exam are your own exercise. Not for HW.)