Lecture18:
CMOS amplifiers (2)

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Summary

- MOS structure
  - Two different mechanisms to provide negative charges
  - Threshold voltage
  - Once the MOS is inverted, it is a capacitor.
- MOS IV
  - Current as a product of density and velocity
  - Triode region and saturation region
  - Concept of transconductance
  - Channel length modulation
  - Body effect
  - Velocity saturation
  - Subthreshold swing

Introduction to G-SPICE

- What is the SPICE?
  - Simulation Program with Intergrated Circuit Emphasis

- G-SPICE is a “SPICE-like” program.
  - It will be serviced through the EDISON website.
  - Today, (unfortunately) the off-line demonstration is made.

A resistor

- Biasing a resistor
  - Input file

```
tstep = 1e-9 ;
tnum = 1000 ;
vsweep = 1 ;
vsweep_value = 1.0 ;
vsweep_num = 100 ;
vsweep_node1 = 0 ;
vsweep_node2 = 1 ;
r[0] = 1 ;
r_value[0] = 1e3 ;
r_node1[0] = 0 ;
r_node2[0] = 1 ;
```

Two resistors

- Biasing two resistors
  - Input file

```
tstep = 1e-9 ;
tnum = 1000 ;
vsweep = 1 ;
vsweep_value = 1.0 ;
vsweep_num = 100 ;
vsweep_node1 = 0 ;
vsweep_node2 = 2 ;
r[0] = 1 ;
r_value[0] = 1e3 ;
r_node1[0] = 0 ;
r_node2[0] = 1 ;
r[1] = 1 ;
r_value[1] = 1e3 ;
r_node1[1] = 1 ;
r_node2[1] = 2 ;
```

MOSFET

- MOSFET Id-Vds
  - Input file
  - Change the gate voltage
  - Channel length modulation?

```
tstep = 1e-9 ;
tnum = 1000 ;
vdc = 1 ;
vdc_value = 1.8 ;
vdc_node1 = 0 ;
vdc_node2 = 1 ;
vsweep = 1 ;
vsweep_value = 1.8 ;
vsweep_num = 100 ;
vsweep_node1 = 0 ;
vsweep_node2 = 2 ;
mos[0] = 1 ;
mos_type[0] = 0 ;
mos_vt0[0] = 0.4 ;
mos_kp[0] = 200e-6 ;
mos_w[0] = 2.0 ;
mos_l[0] = 0.18 ;
mos_lambda[0] = 0.1 ;
mos_node1[0] = 0 ;
mos_node2[0] = 1 ;
mos_node3[0] = 2 ;
```

Amplifier

- Guess its schematic
  - Its input-output characteristic?

```
tstep = 1e-3 ;
tnum = 1000 ;
vdc = 1 ;
vdc_value = 1.8 ;
vdc_node1 = 0 ;
vdc_node2 = 3 ;
vsweep = 1 ;
vsweep_value = 1.8 ;
vsweep_num = 100 ;
vsweep_node1 = 0 ;
vsweep_node2 = 1 ;
mos[0] = 1 ;
mos_type[0] = 0 ;
mos_vt0[0] = 0.4 ;
mos_kp[0] = 100e-6 ;
mos_w[0] = 2.0 ;
mos_l[0] = 0.18 ;
mos_lambda[0] = 0.0 ;
mos_node1[0] = 0 ;
mos_node2[0] = 1 ;
mos_node3[0] = 2 ;
r[0] = 1 ;
r_value[0] = 5e3 ;
r_node1[0] = 2 ;
r_node2[0] = 3 ;
```

One more…

- Imposing a sinusoidal signal
  - How about the output voltage?

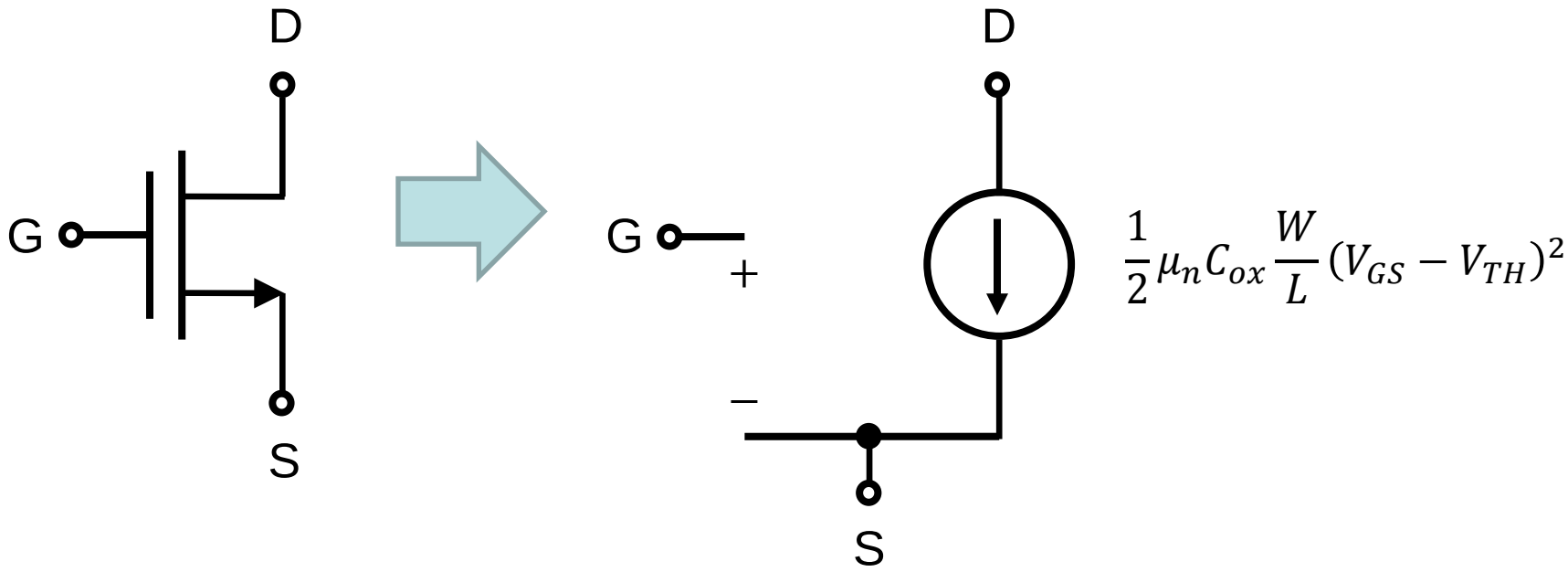
```
tstep = 1e-3 ;
tnum = 1000 ;
vdc = 1 ;
vdc_value = 1.8 ;
vdc_node1 = 0 ;
vdc_node2 = 4 ;
vsweep = 1 ;
vsweep_value = 1.0 ;
vsweep_num = 100 ;
vsweep_node1 = 0 ;
vsweep_node2 = 1 ;
vsin = 1;
vsin_amp = 0.01 ;
vsin_freq = 10 ;
vsin_node1 = 1 ;
vsin_node2 = 2 ;
mos[0] = 1 ;
mos_type[0] = 0 ;
mos_vt0[0] = 0.4 ;
mos_kp[0] = 100e-6 ;
mos_w[0] = 2.0 ;
mos_l[0] = 0.18 ;
mos_lambda[0] = 0.0 ;
mos_node1[0] = 0 ;
mos_node2[0] = 2 ;
mos_node3[0] = 3 ;
r[0] = 1 ;
r_value[0] = 5e3 ;
r_node1[0] = 3 ;
r_node2[0] = 4 ;
```

Large-signal model (1/2)

- Saturation region

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

  - Drain current is determined by gate voltage. (*voltage-controlled current source*)
  - *Channel-length modulation?*

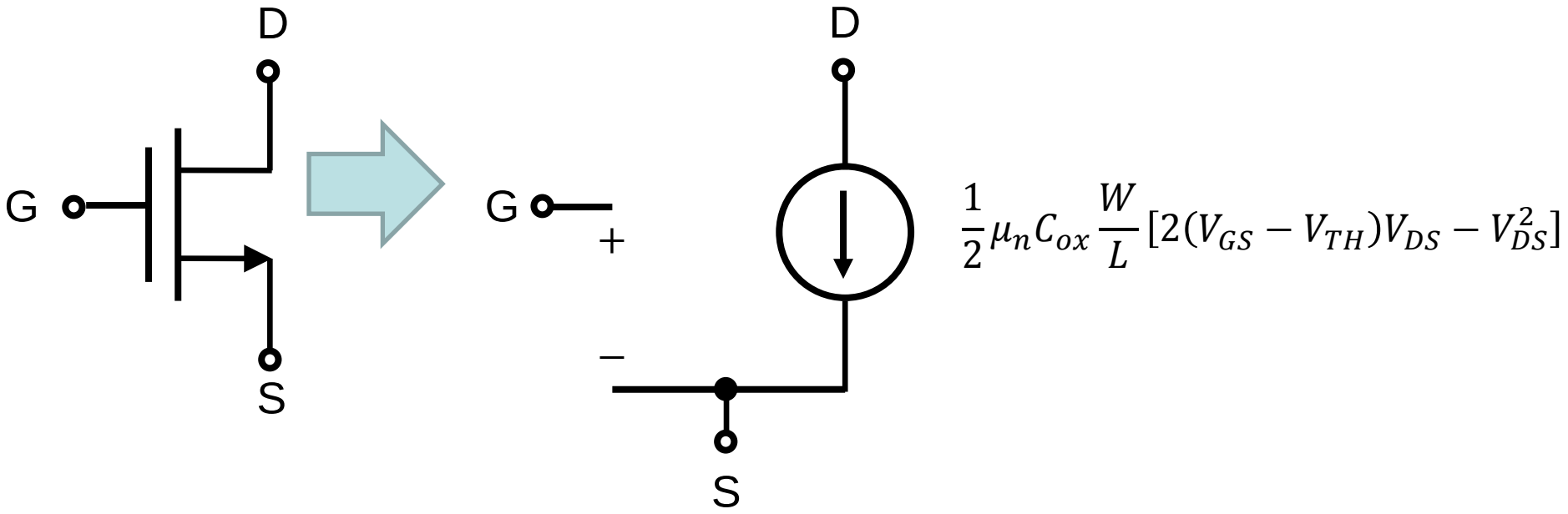


Large-signal model (2/2)

- Triode region

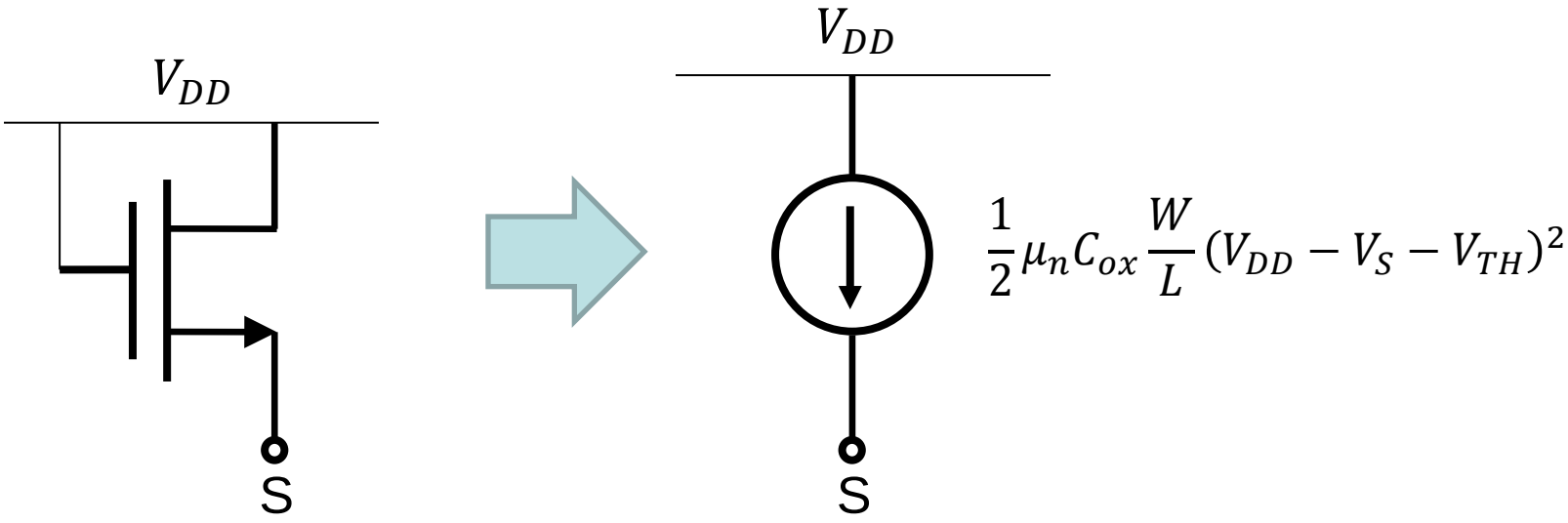
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$$

  - Still, it can be described by a *voltage-controlled current source*.



Example 6.13

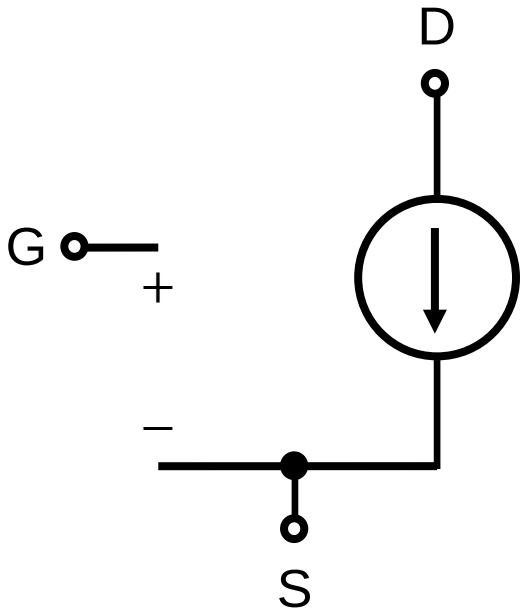
- Always in the saturation region!
  - Any necessary condition?

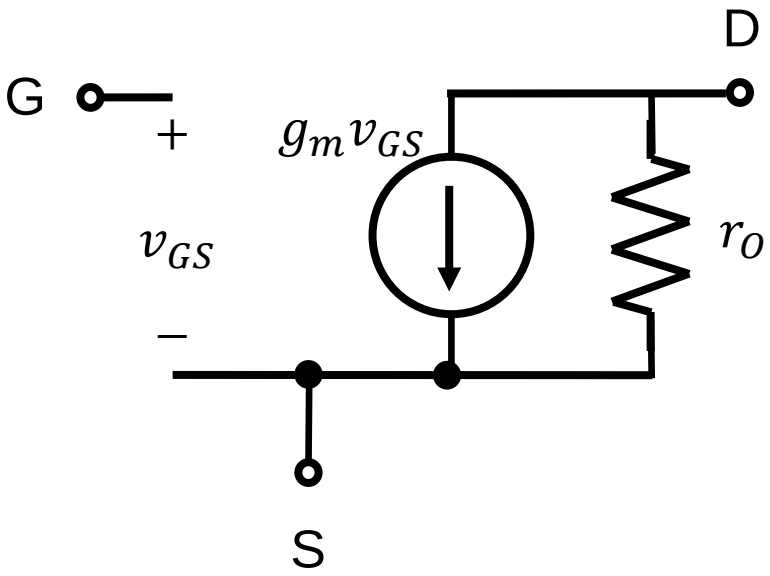


Gate and drain are tied.
They are connected to V_{DD}.

Small-signal model

- The large-signal model is complete (within its accuracy limitation).
  - But, for small-signal analysis, it is convenient to have the small-signal model.



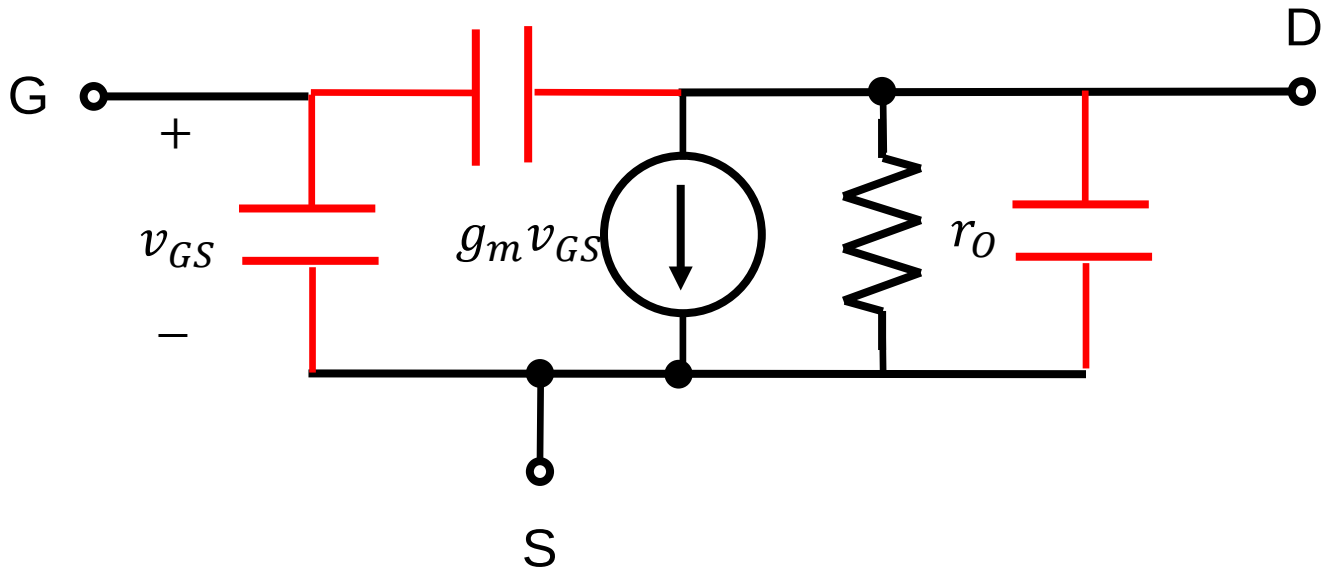


$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

What is g_m and r_O?

Time-dependent one?

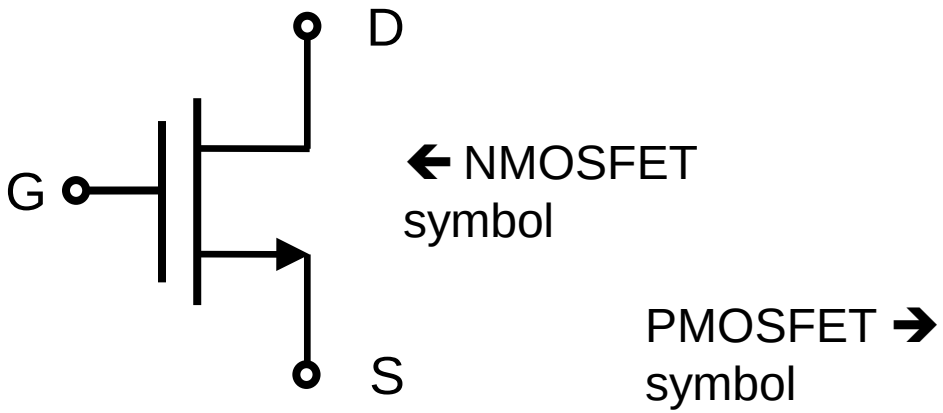
- Everything was in the dc steady-state…
  - How about the frequency-dependent case?
  - Capacitive components can be seen.
  - *Their physical origin?*

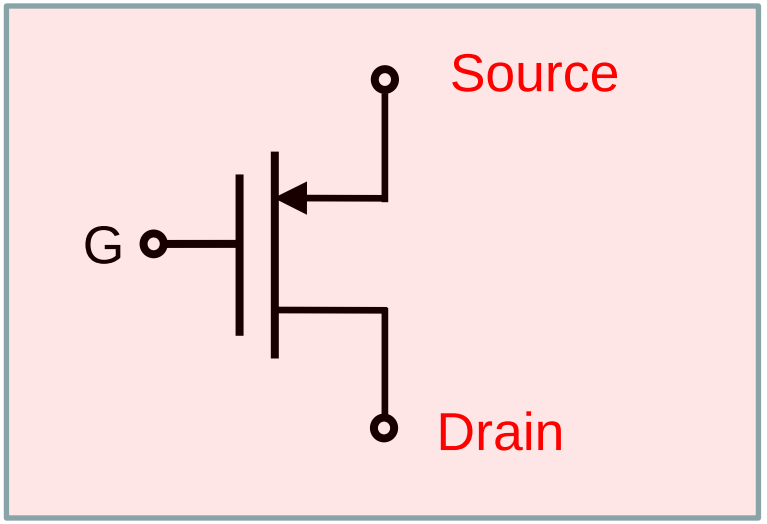


High-frequency, equivalent-circuit model for the case in which the source is connected to the substrate

CMOS

- 9's complementary of 123?
  - 876
- Complementary MOS
  - Here we have an NMOSFET.
  - A device where the transport is dominated by holes





- Why is it important?

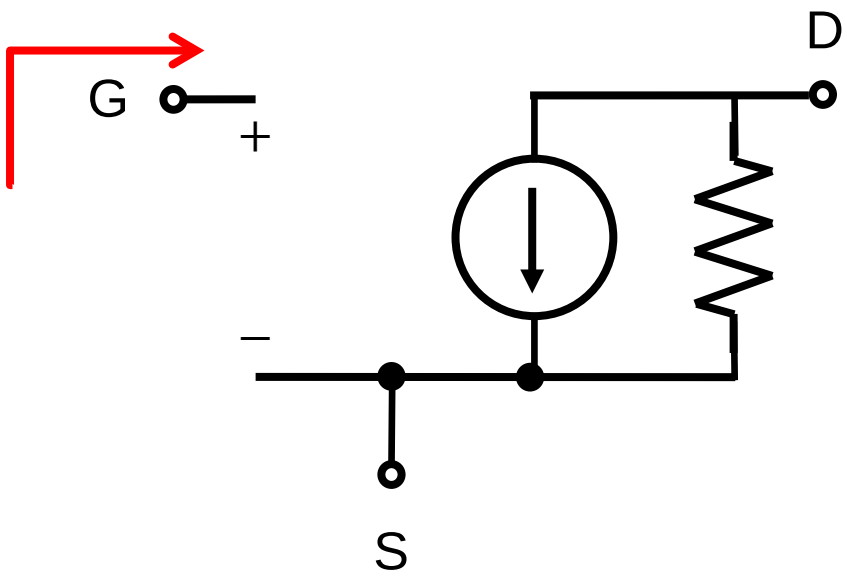
Why amplifiers?

- Signal amplification
  - Usually, signals are “weak.” (in the μV or mV range)
  - It is too small for reliable processing.
  - If the signal magnitude is made larger, processing is much easier.

- Desirable properties
  - Low power consumption
  - High speed operation
  - Low noise

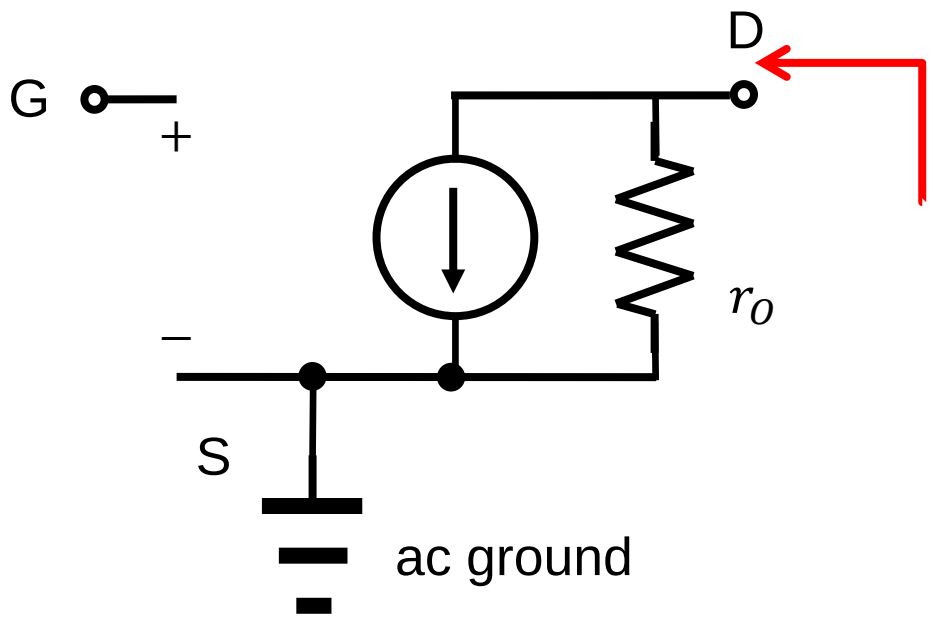
Impedances (1/3)

- A MOSFET with three terminals
  - Looking into the gate, we see the infinite impedance.
  - (Strictly valid at the low-frequency range)



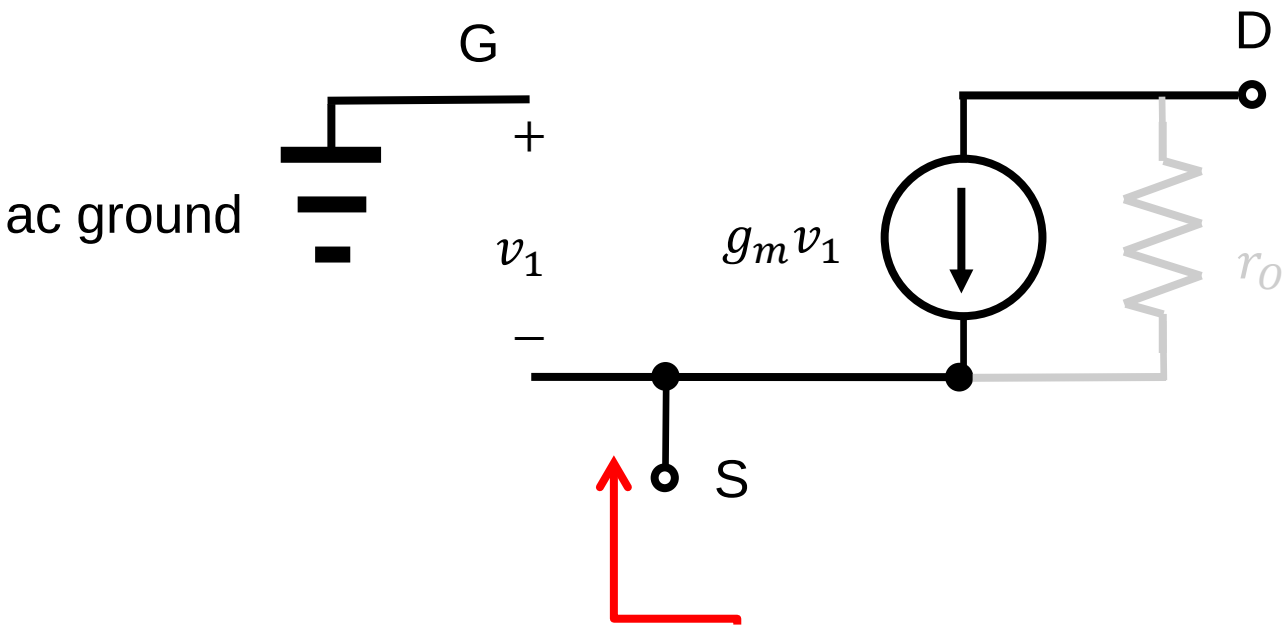
Impedances (2/3)

- A MOSFET with three terminals
  - Looking into the drain, we see r_O if the source is ac grounded.



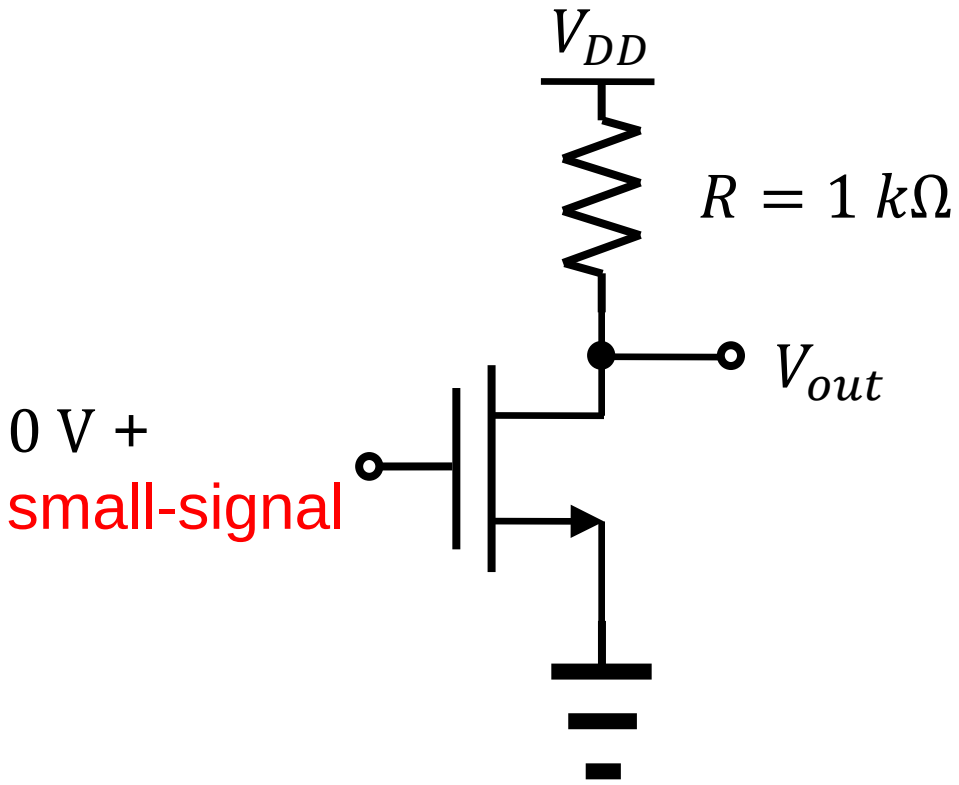
Impedances (3/3)

- A MOSFET with three terminals
  - Looking into the source, we see $1/g_m$ if the gate is ac grounded and channel-length modulation is neglected.



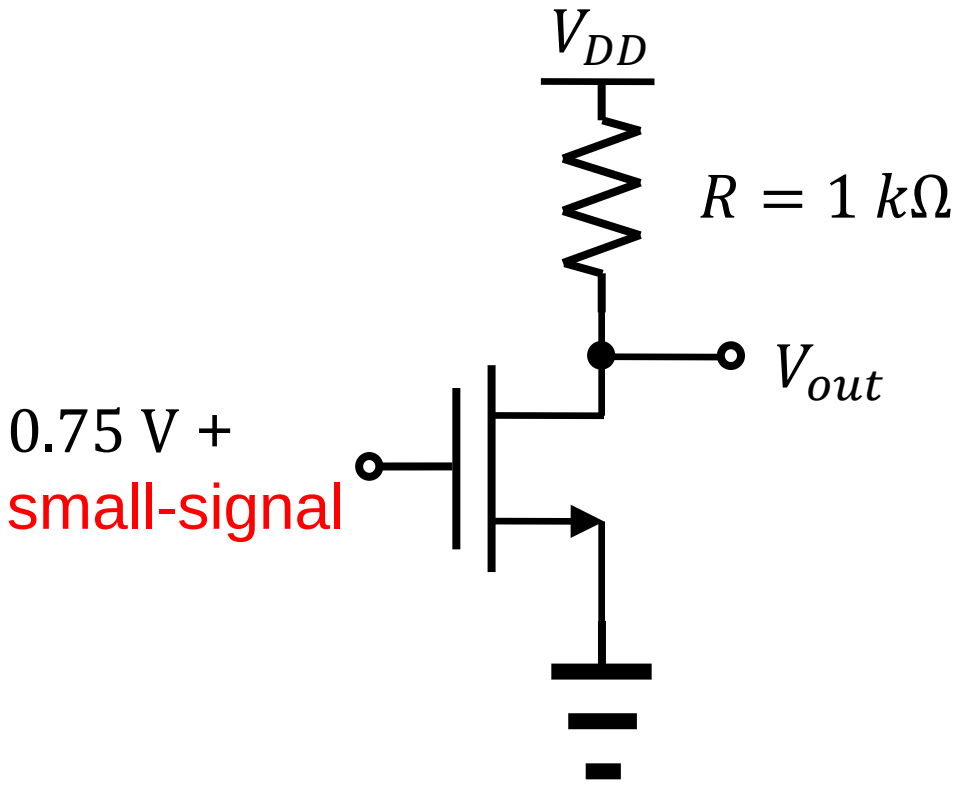
Transistor turned off

- The example 17.5 shows an amplifier circuit.
  - But, the transistor is not turned on.
  - The circuit generates no output signal.



This is a solution.

- The example 16.7 shows a revised circuit.
  - Then, how can we generate 0.75 V, for example?
  - Use of a separate battery can be a way.



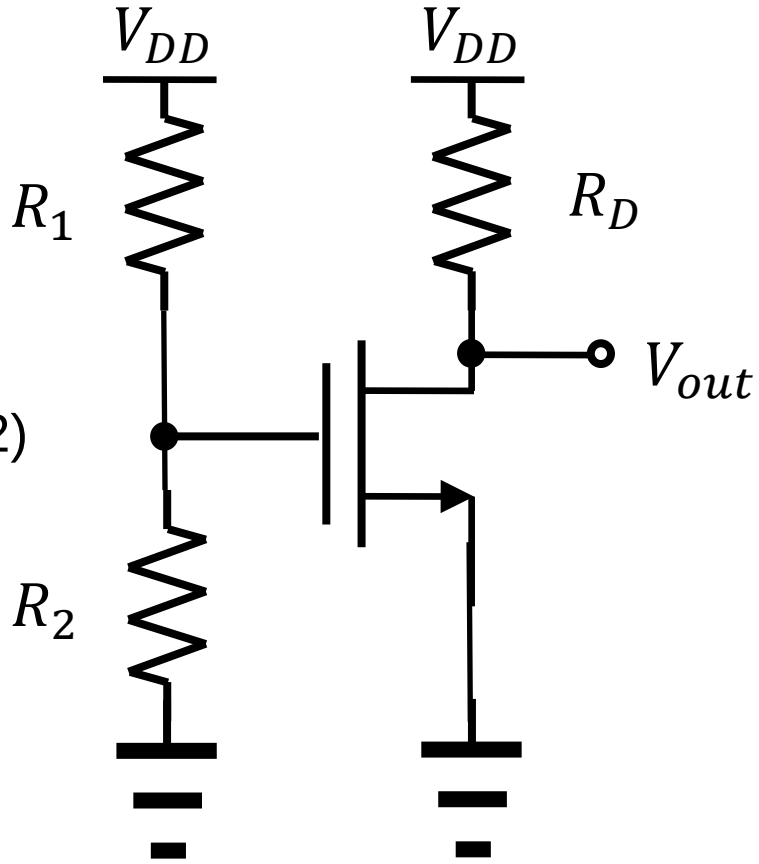
Simple biasing (1/2)

- A better way
  - The gate bias voltage is

$$V_{GS} = \frac{R_2}{R_1+R_2} V_{DD} \qquad (17.10)$$

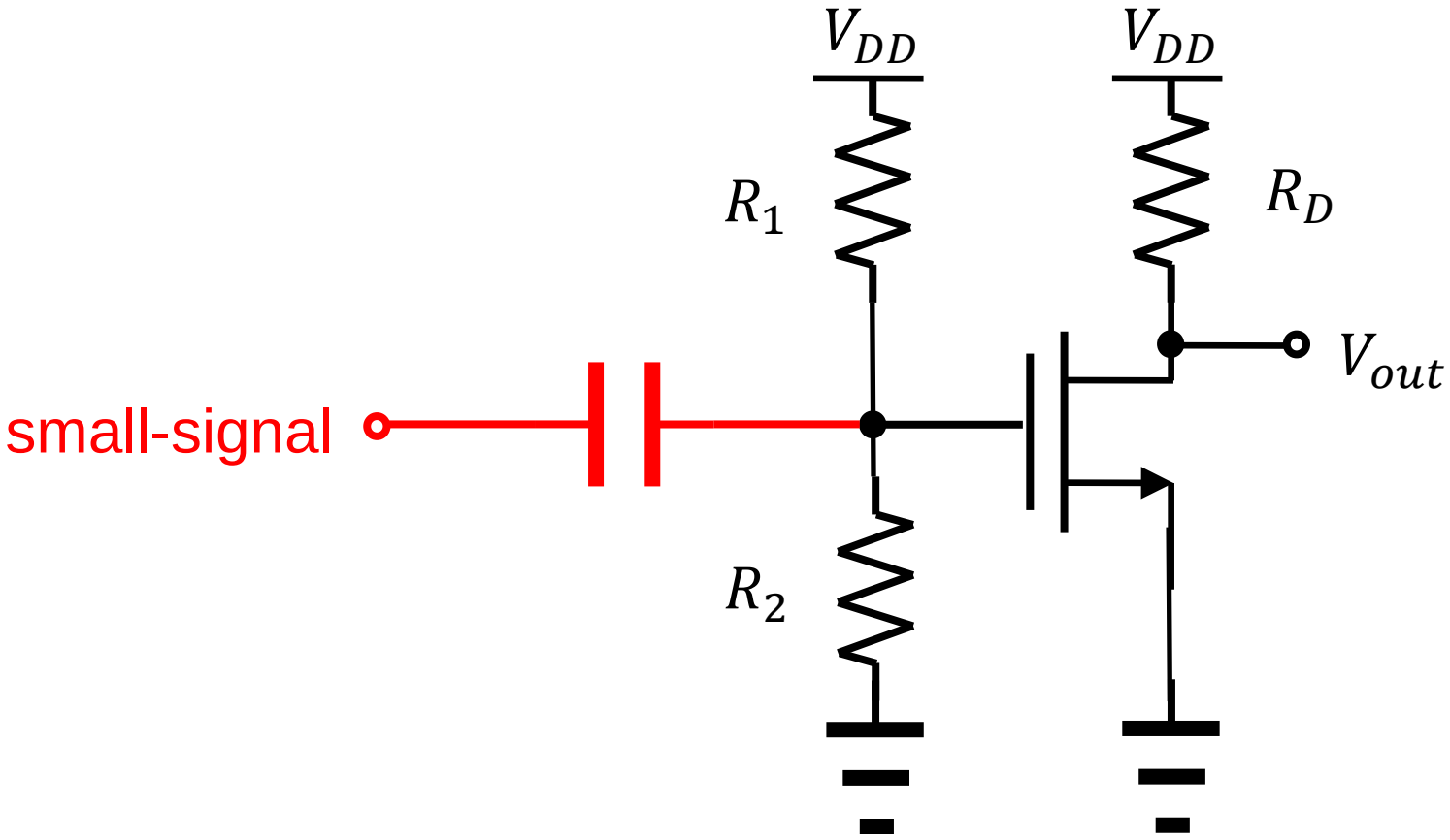
  - The drain current is

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(\frac{R_2}{R_1+R_2} V_{DD} - V_{TH}\right)^2 \qquad (17.12)$$



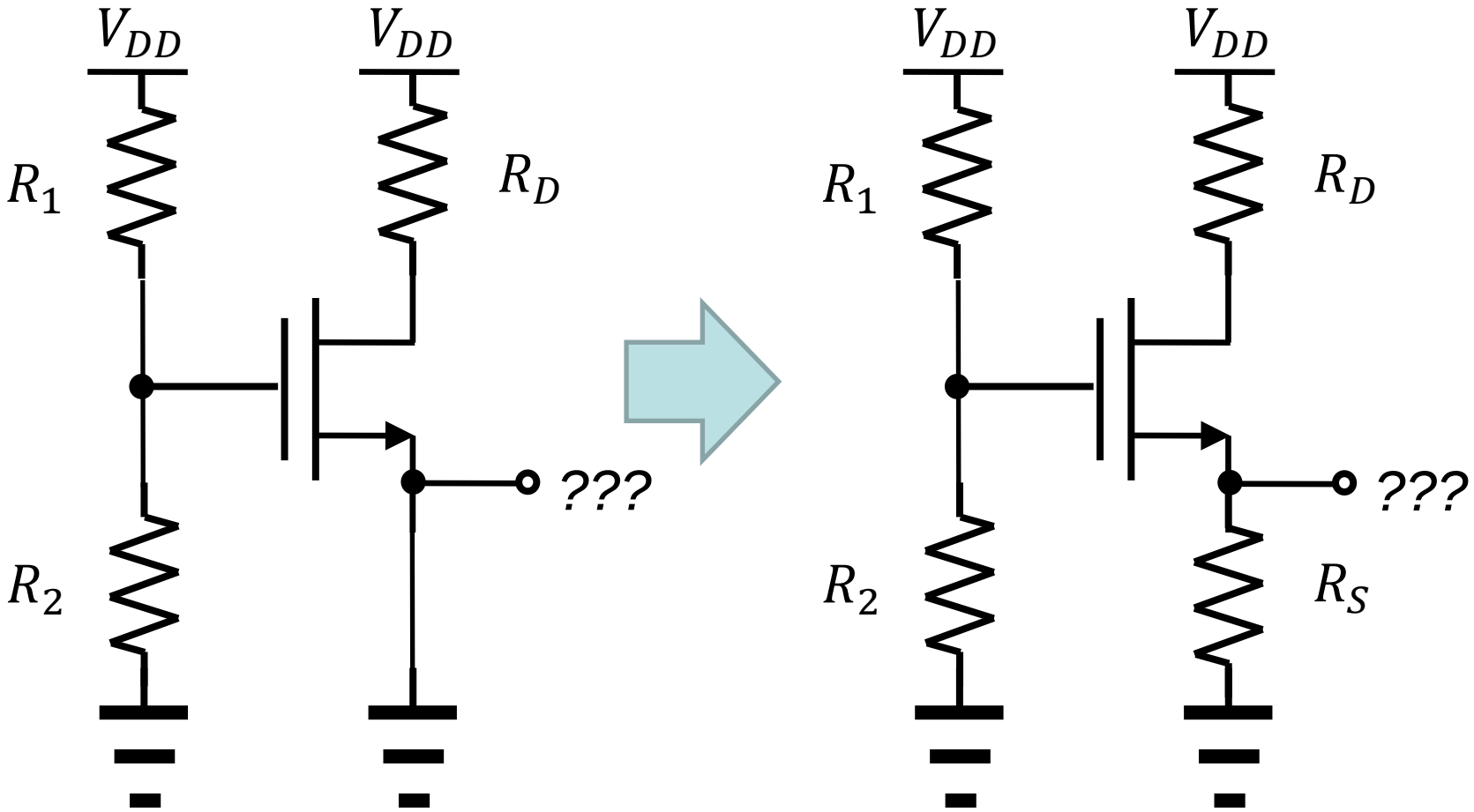
Simple biasing (2/2)

- How to apply the small-signal input
  - Use a capacitor!



Source degeneration (1/2)

- A resistor placed in series with the source terminal



Source degeneration (2/2)

- Now we have to find the source voltage.
  - (Saturation current of the MOSFET) = (Current flowing through R_S)
  - After a simple manipulation, we can find

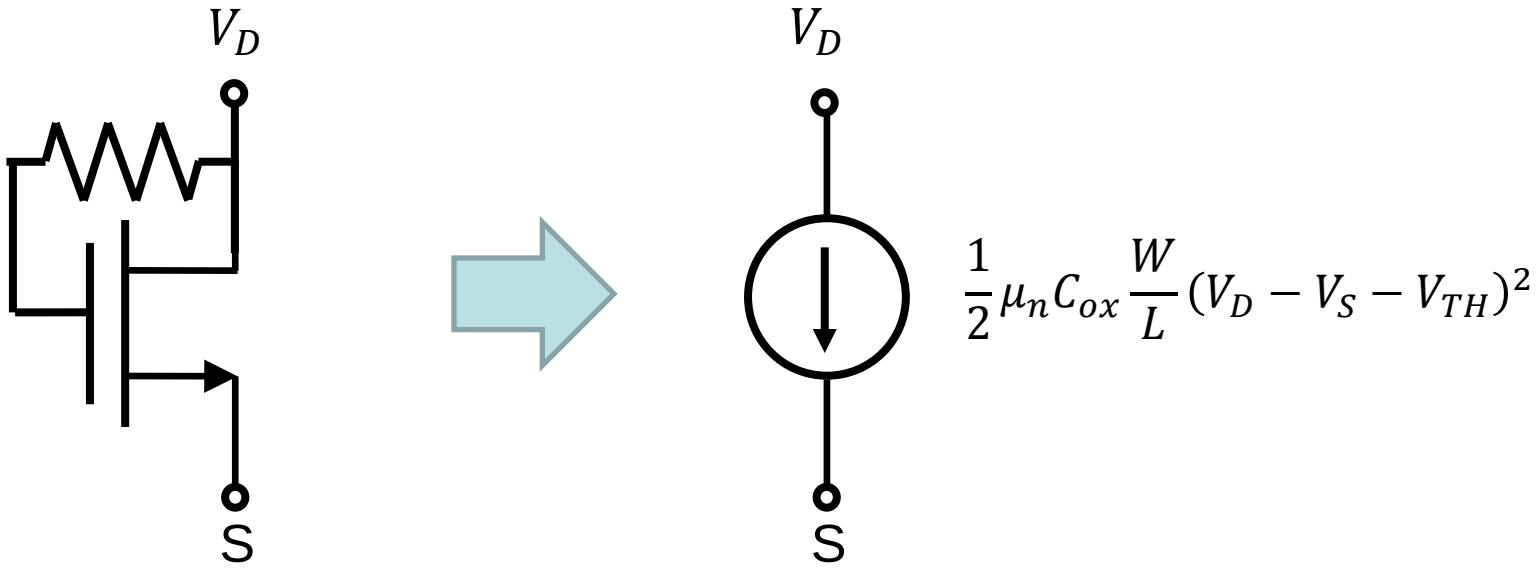
$$V_S = V_G + V_1 - V_{TH} - \sqrt{V_1^2 + 2(V_G - V_{TH})V_1}$$

  - Here,

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_s}$$

Self-biasing

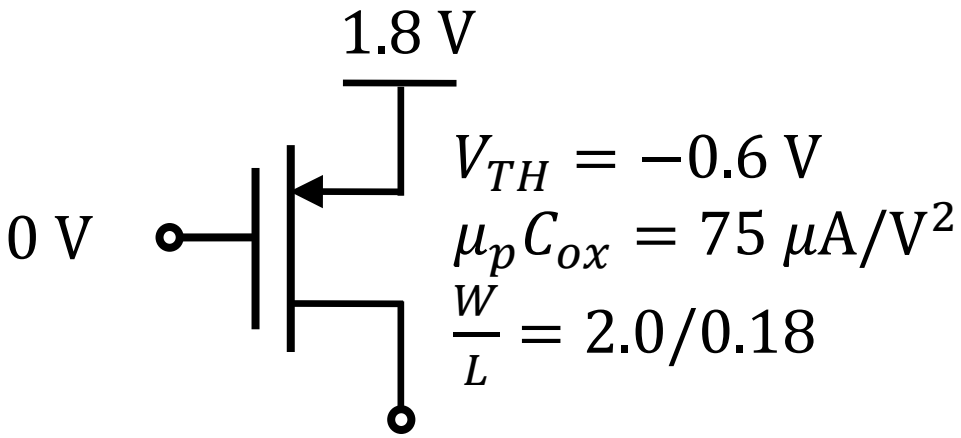
- Already covered in Example 6.13.
  - Always in the saturation region.



Gate and drain are tied.

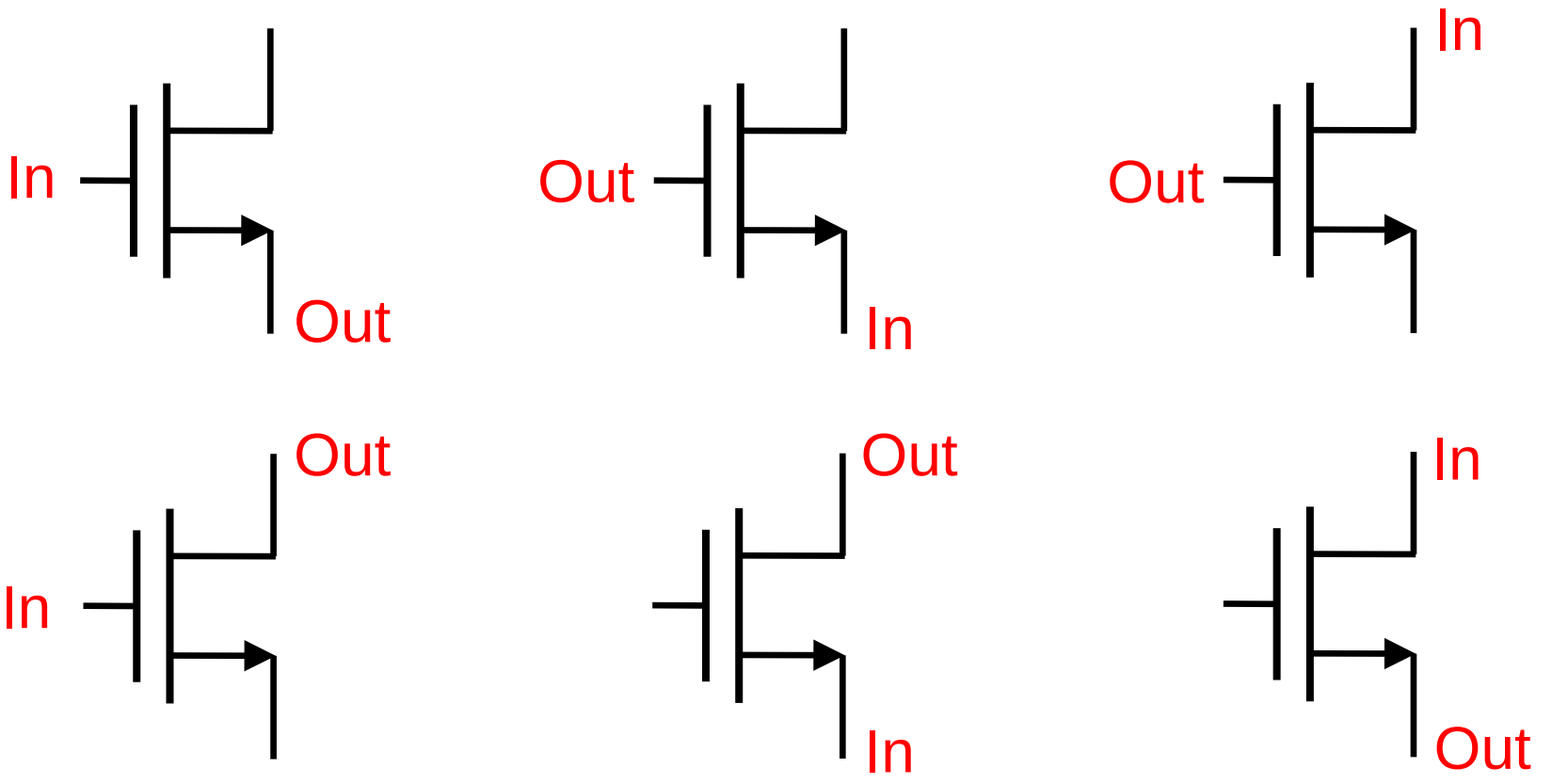
Biasing of PMOS devices

- Different polarity
  - The amount of “gate overdrive” is $1.2\ \mathrm{V}$.
  - It is not $0.6\ \mathrm{V}$.



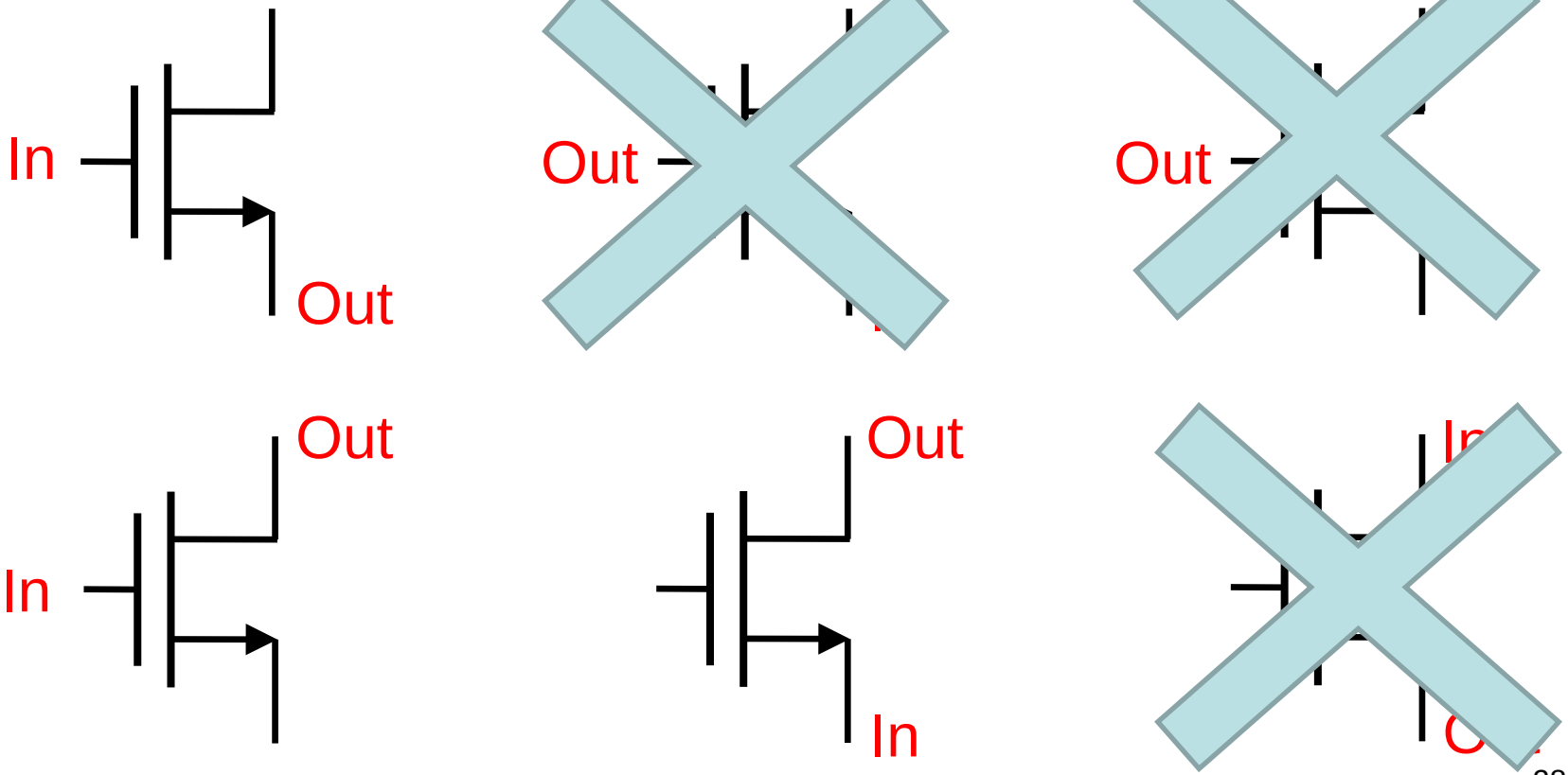
CMOS amplifiers (1/2)

- Select one input. Then, select one output.
  - What are possible topologies?



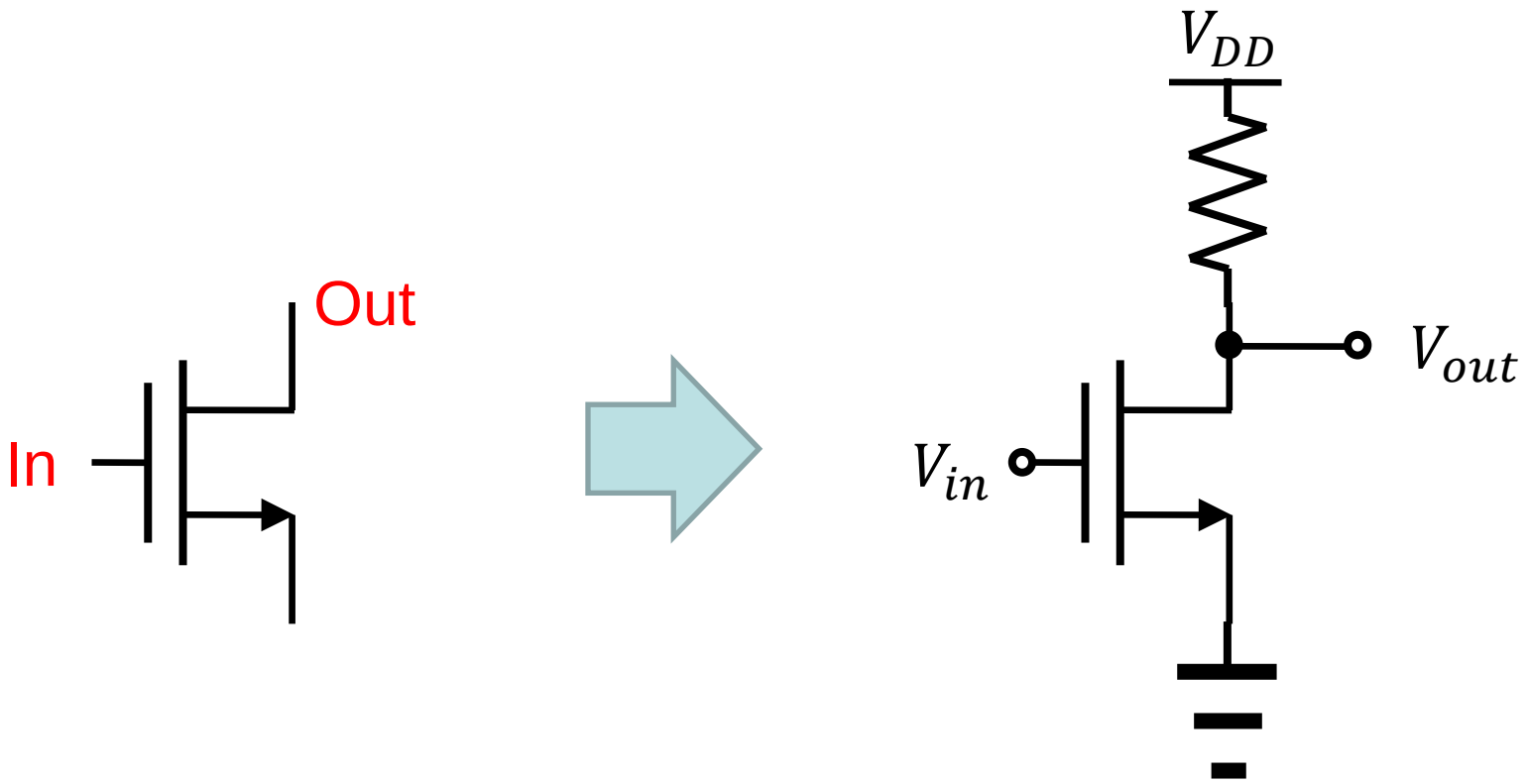
CMOS amplifiers (2/2)

- Only three are possible.
  - Each of them has own name.



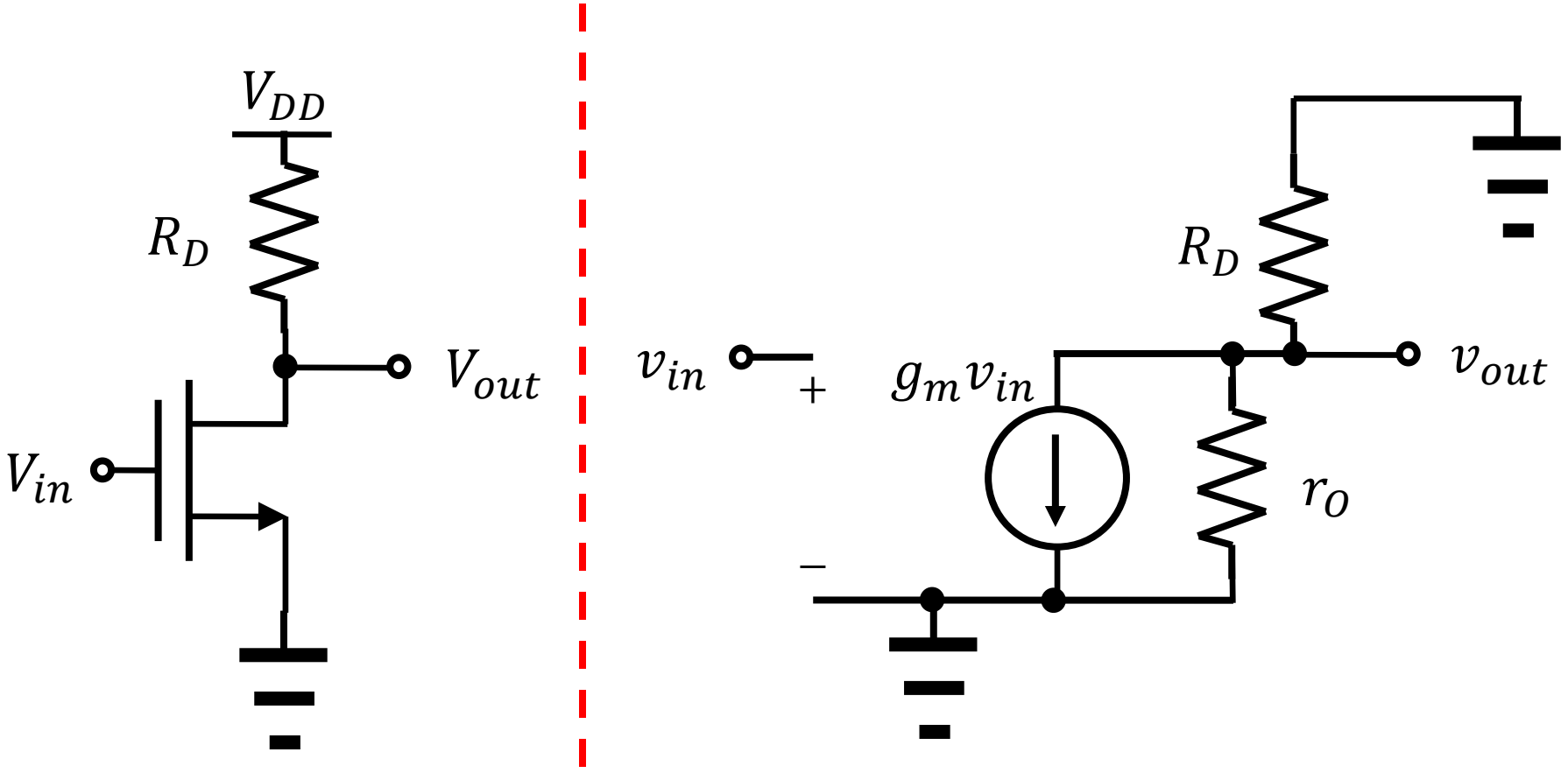
Common-source

- Source terminal is grounded.



Small-signal model

- Let's draw the small-signal model together!



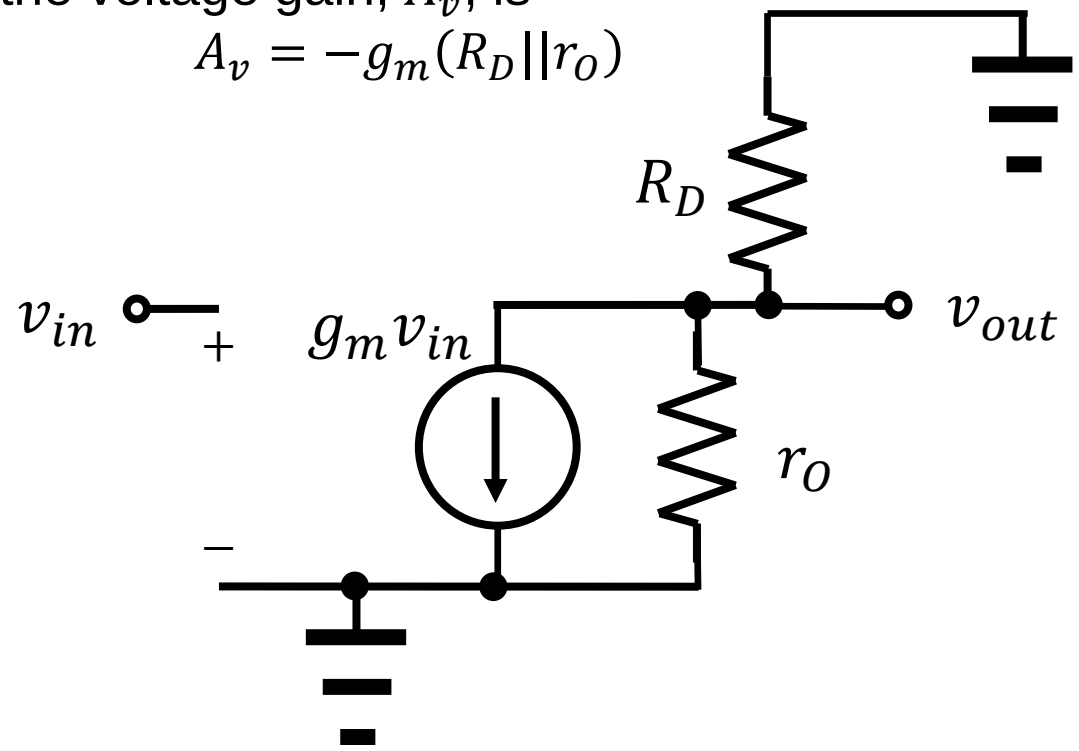
Gain

- Now, calculate the v_{out}.
  - KCL for the v_{out} node gives

$$v_{out} = -g_m(R_D||r_O)v_{in}$$

  - Therefore, the voltage gain, A_v, is

$$A_v = -g_m(R_D||r_O)$$



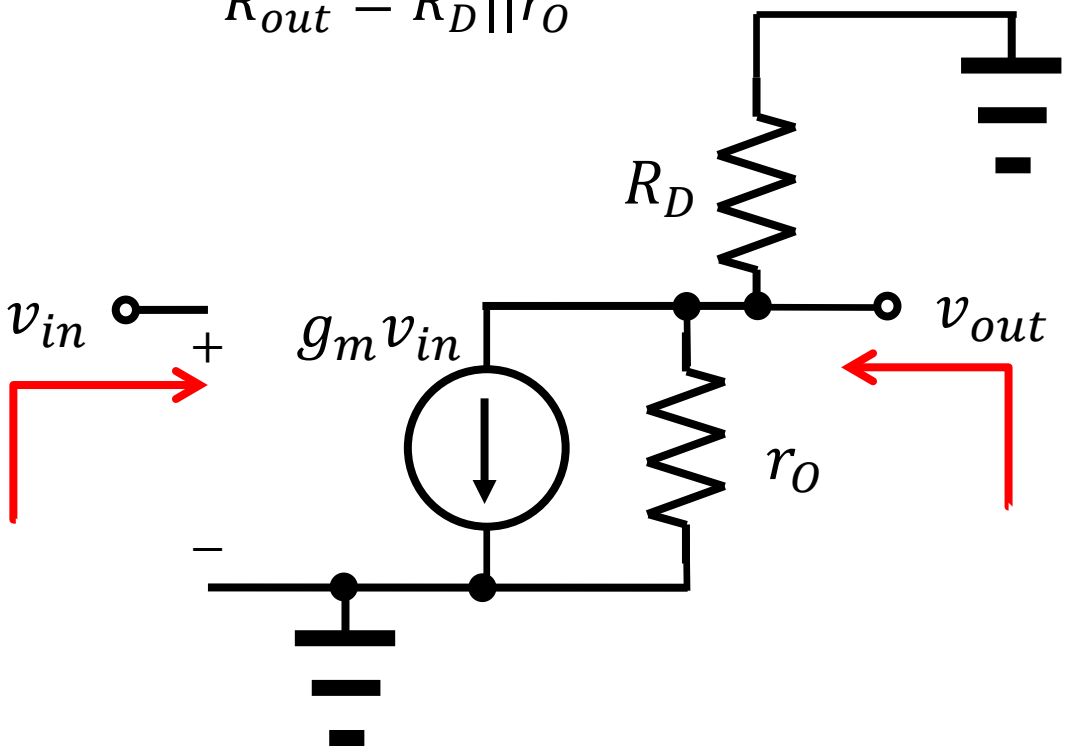
Input/output impedances

- Input impedance

$$R_{in} = \infty$$

- Output impedance

$$R_{out} = R_D || r_O$$



Current-source load

- When $R_D \rightarrow \infty$,
  - The gain can be maximized.