Lecture16:
CMOS amplifiers (3)

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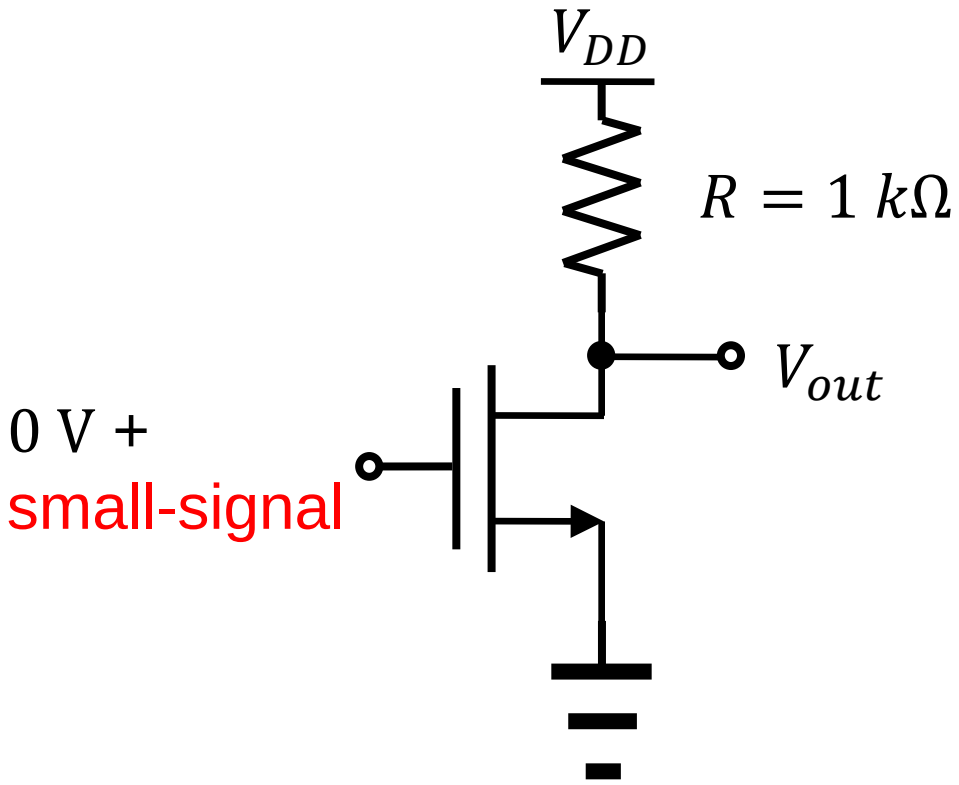
Read your textbook.

- Reading your textbook is important.

- Today, we will try to cover up to p. 764.
  - Just before 17. 4. 1.

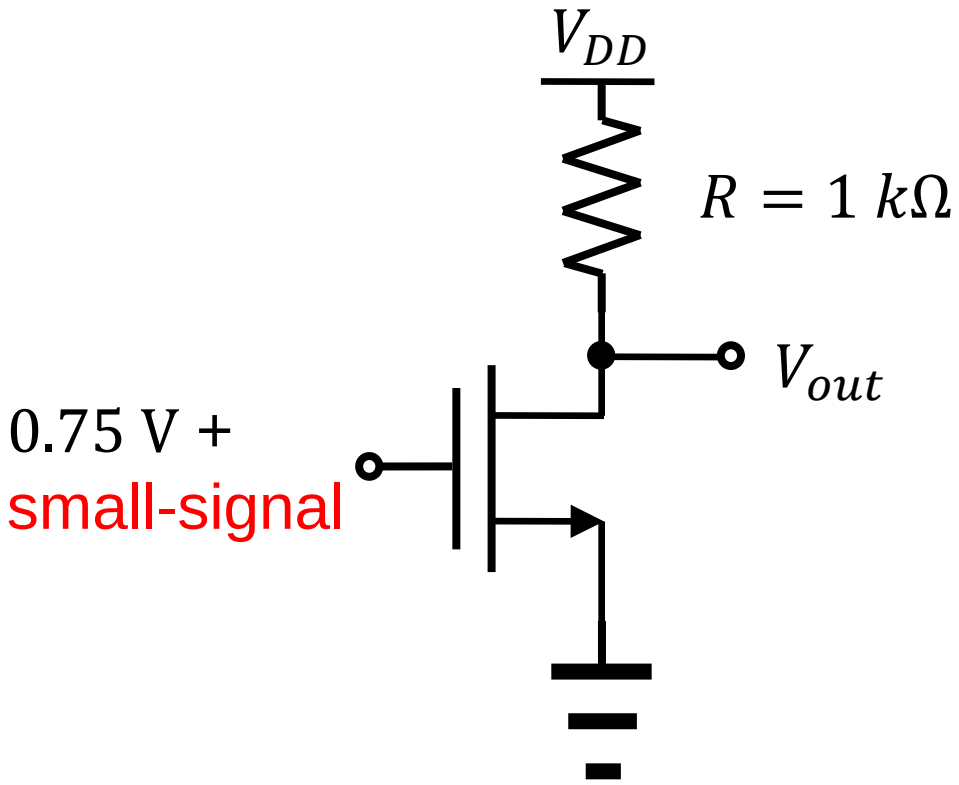
Transistor turned off

- The example 17.5 shows an amplifier circuit.
  - But, the transistor is not turned on.
  - The circuit generates no output signal.



This is a solution.

- The example 17.7 shows a revised circuit.
  - Then, how can we generate 0.75 V, for example?
  - Use of a separate battery can be a way.



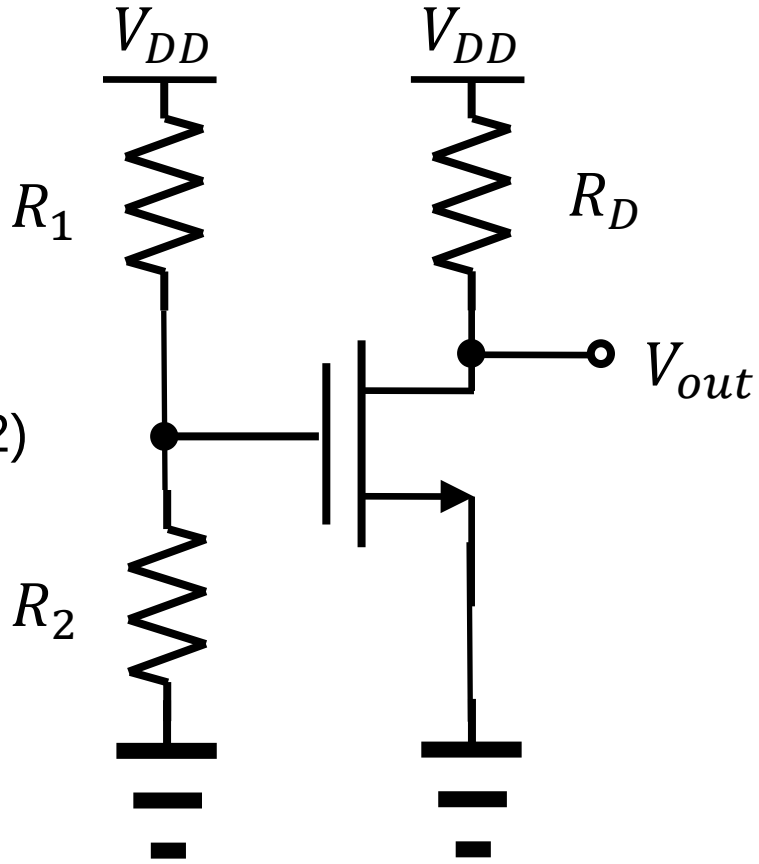
Simple biasing (1/2)

- A better way
  - The gate bias voltage is

$$V_{GS} = \frac{R_2}{R_1+R_2} V_{DD} \qquad (17.10)$$

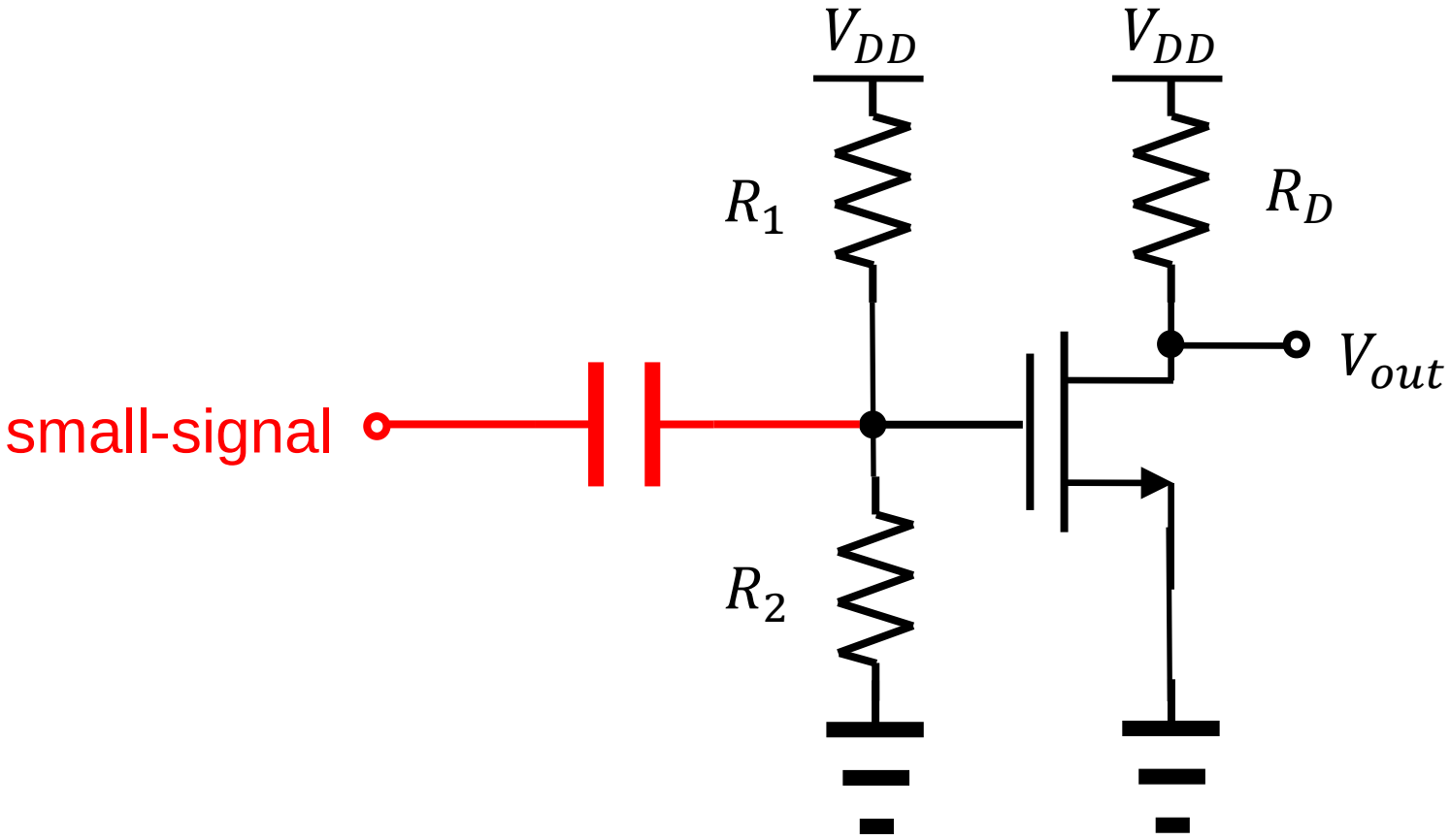
  - The drain current is

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(\frac{R_2}{R_1+R_2} V_{DD} - V_{TH}\right)^2 \qquad (17.12)$$



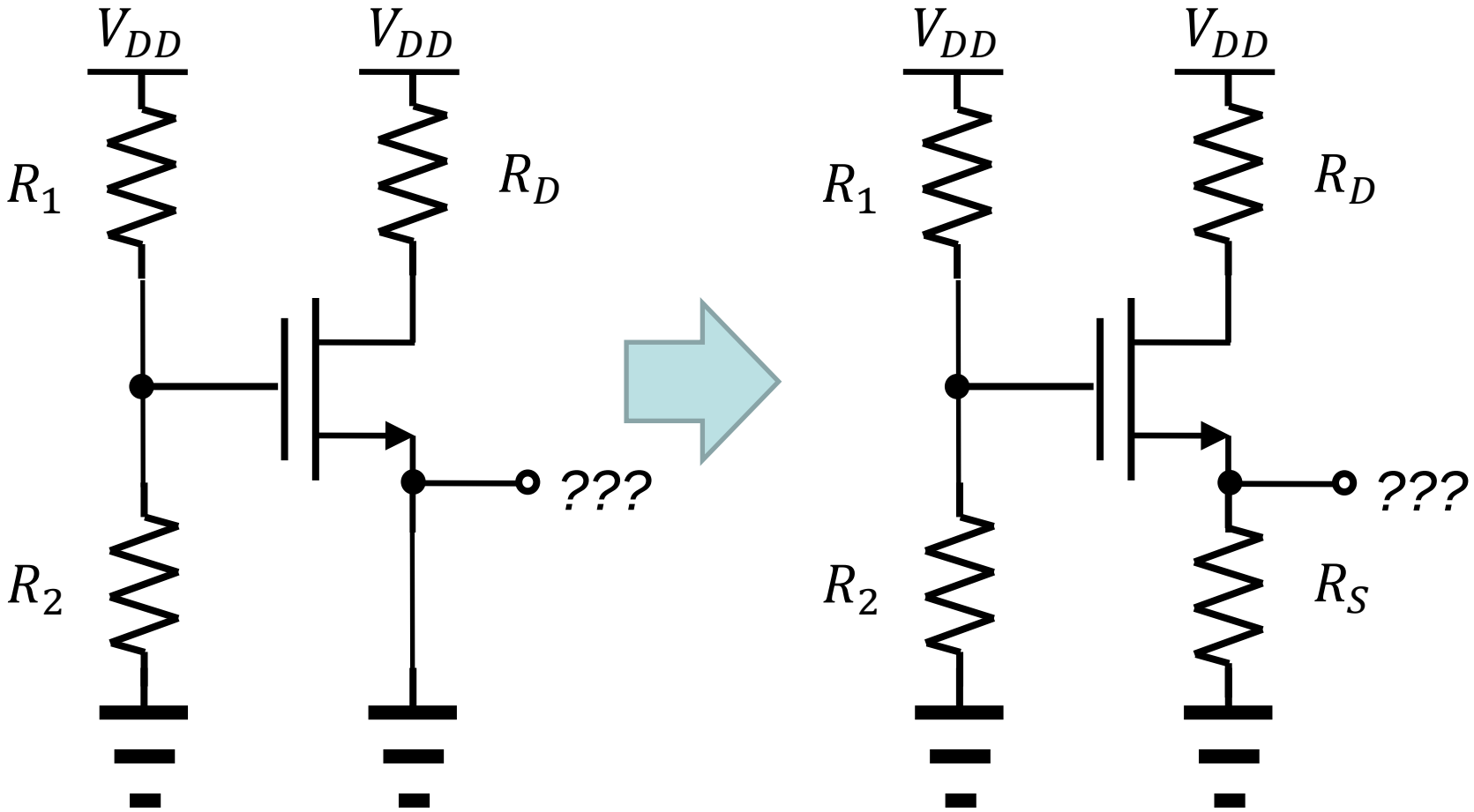
Simple biasing (2/2)

- How to apply the small-signal input
  - Use a capacitor!



Source degeneration (1/2)

- A resistor placed in series with the source terminal



Source degeneration (2/2)

- Now we have to find the source voltage.
  - (Saturation current of the MOSFET) = (Current flowing through R_S)
  - After a simple manipulation, we can find

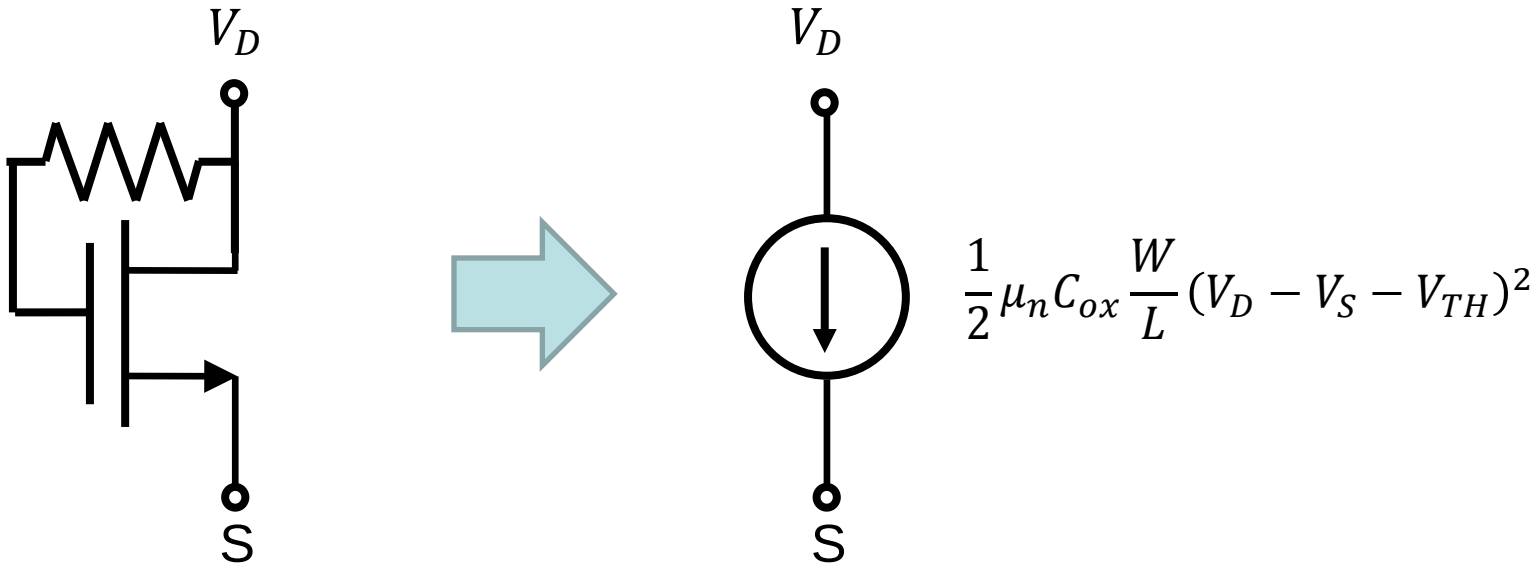
$$V_S = V_G + V_1 - V_{TH} - \sqrt{V_1^2 + 2(V_G - V_{TH})V_1}$$

  - Here,

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_s}$$

Self-biasing

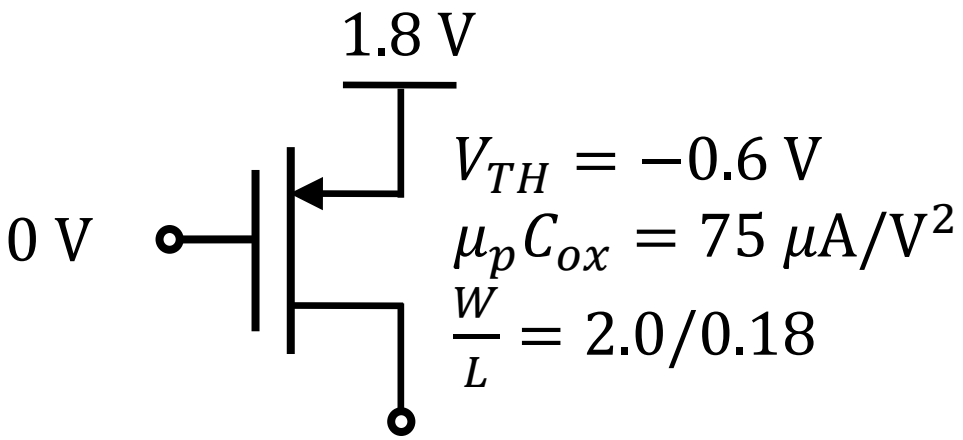
- Already covered in Example 6.13.
  - Always in the saturation region.



Gate and drain are tied.

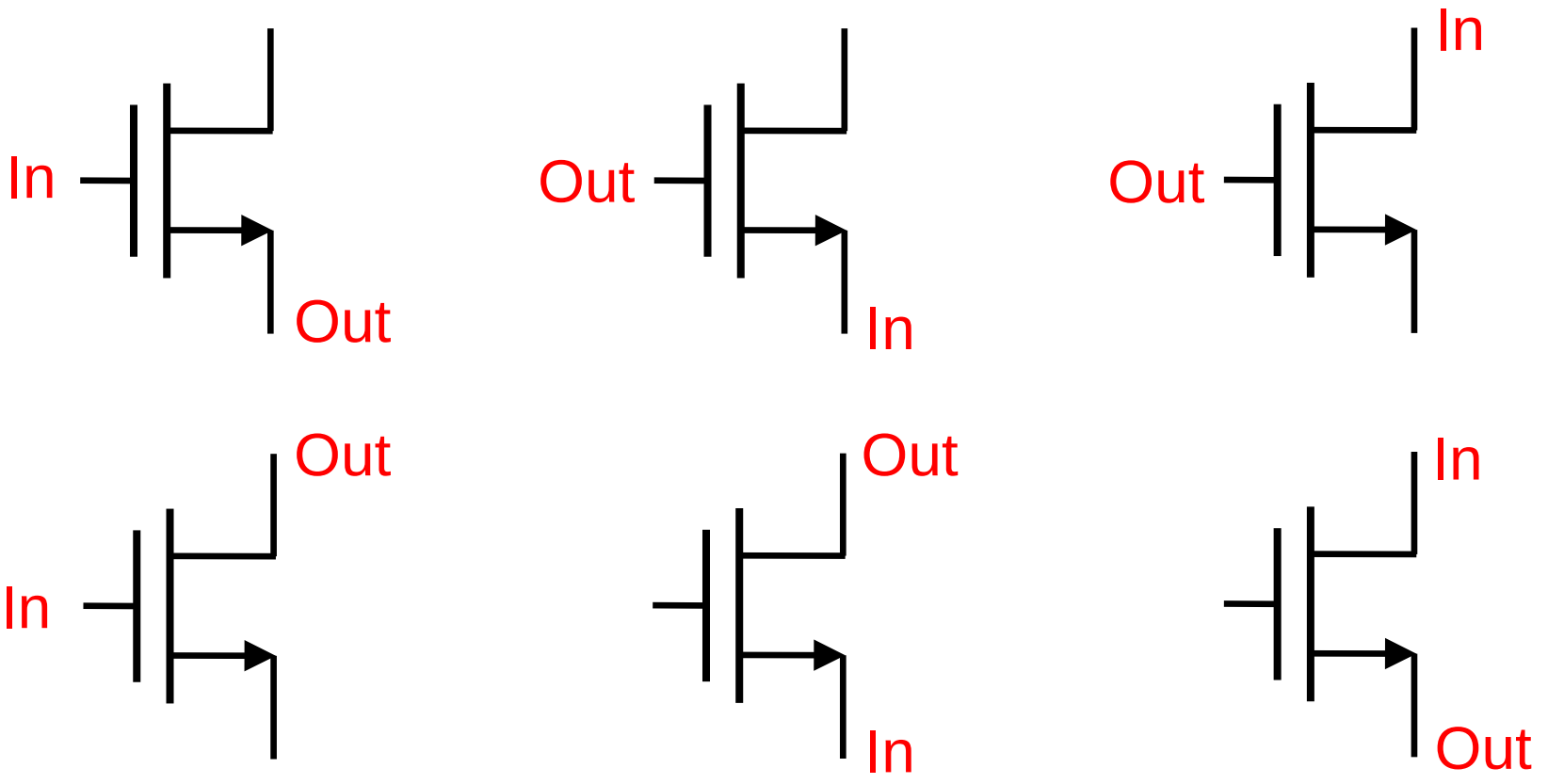
Biasing of PMOS devices

- Let's recall the problem18 of our mid-term exam.
  - The amount of "gate overdrive" is $1.2\ \mathrm{V}$.
  - It is not $0.6\ \mathrm{V}$.



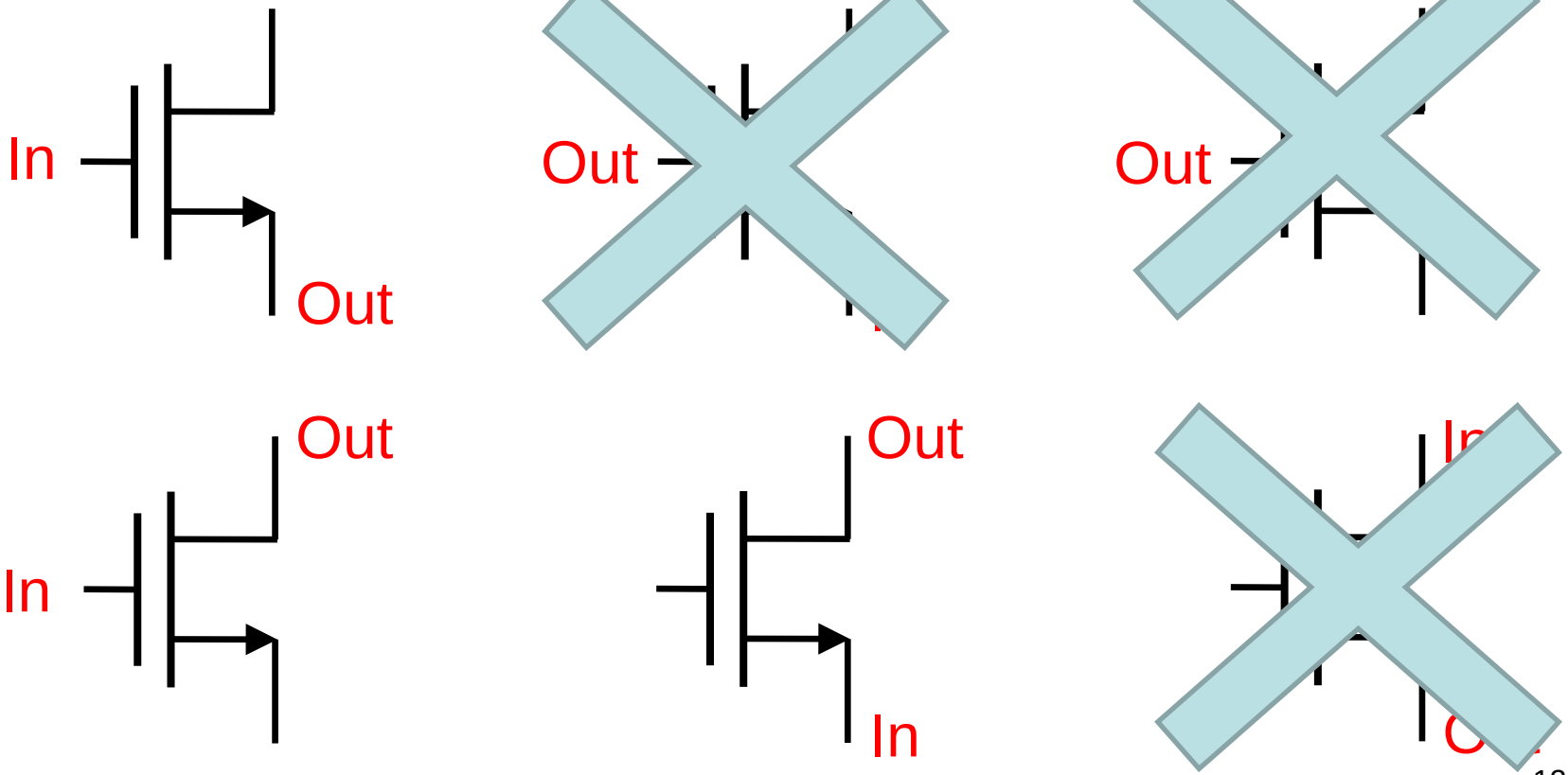
CMOS amplifiers (1/2)

- Select one input. Then, select one output.
  - What are possible topologies?



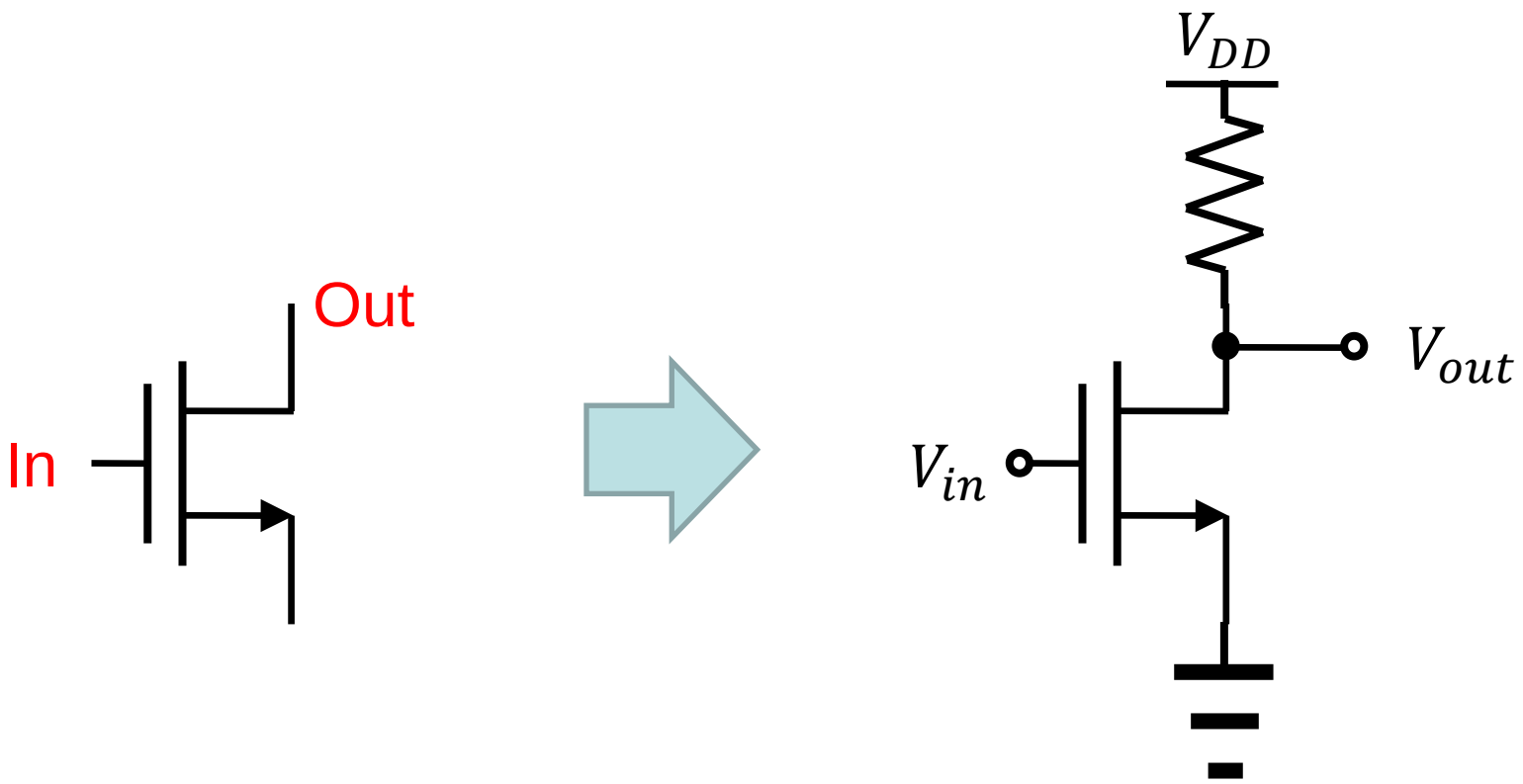
CMOS amplifiers (2/2)

- Only three are possible.
  - Each of them has own name.



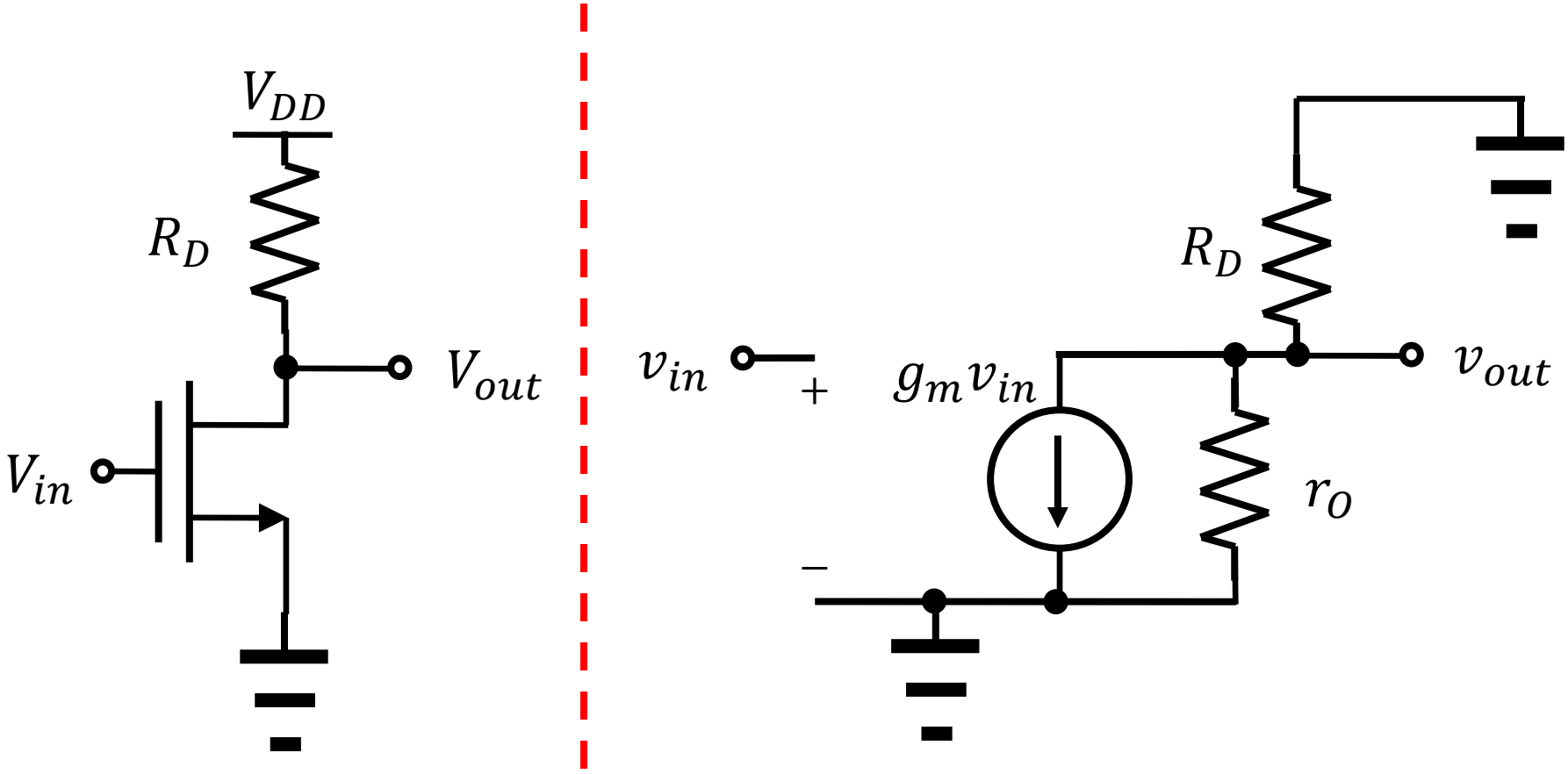
Common-source

- Source terminal is grounded.



Small-signal model

- Let's draw the small-signal model together!



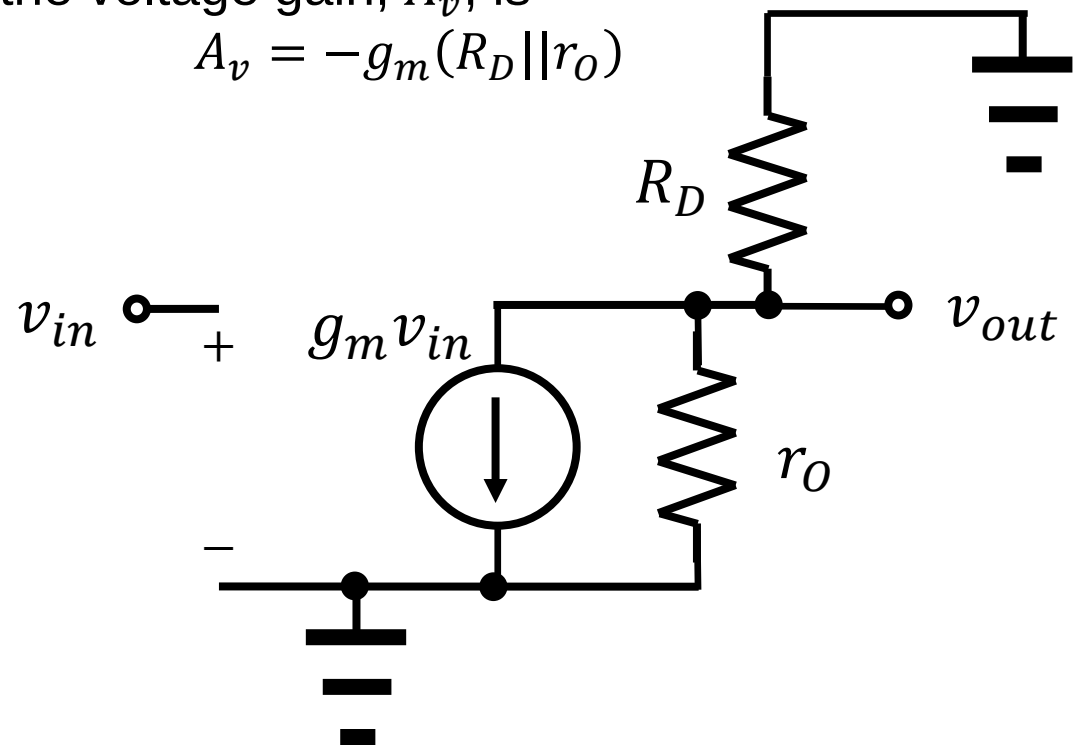
Gain

- Now, calculate the v_{out}.
  - KCL for the v_{out} node gives

$$v_{out} = -g_m(R_D||r_O)v_{in}$$

  - Therefore, the voltage gain, A_v, is

$$A_v = -g_m(R_D||r_O)$$



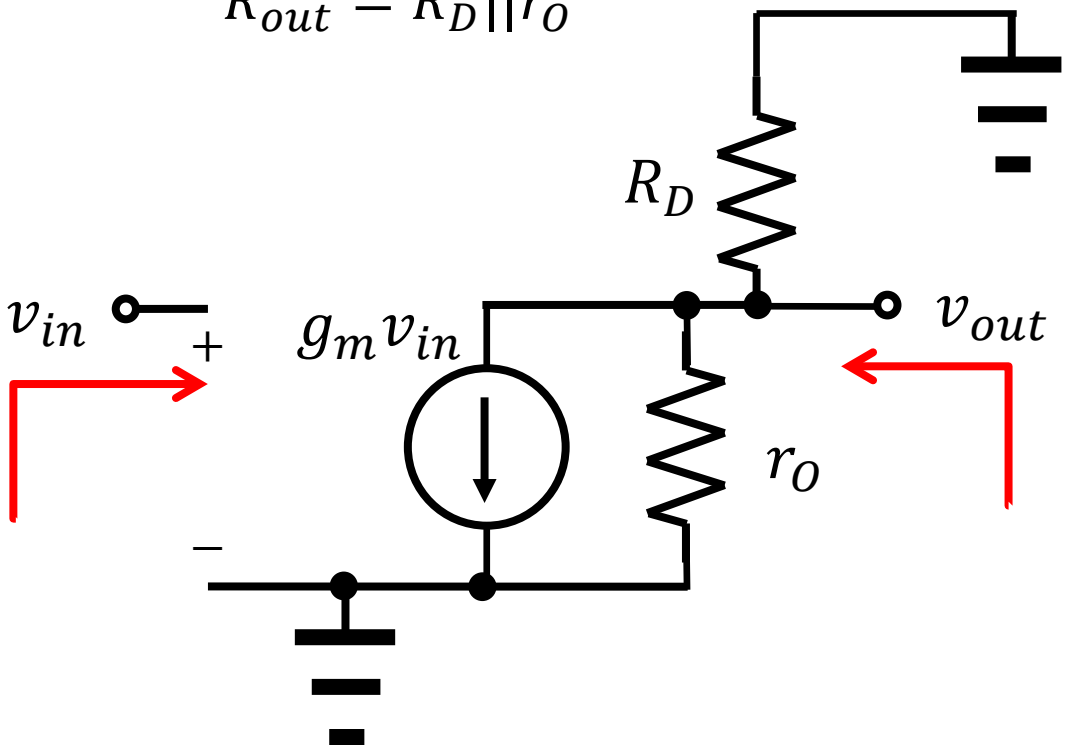
Input/output impedances

- Input impedance

$$R_{in} = \infty$$

- Output impedance

$$R_{out} = R_D || r_O$$



Current-source load

- When $R_D \rightarrow \infty$,
  - The gain can be maximized.