Final exam, Electronic Circuit, Spring semester, 2019

June 10, 2019

We have 40 questions. The exam ends at PM 12:00. Write down your answers on the answer sheets. Explicitly show the unit of your answer. For each question, use the designated answer slot.

In the final exam, no partial credit will be given.

When the numbers are provided, just answer a numerical value and a correct unit.

If not stated otherwise, use the long-channel IV characteristics of MOSFETs. With the channel-length modulation, the saturation current is given by

$$\mathrm{I_D} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

If not stated otherwise, set $\lambda = 0$.

Some useful facts are summarized below:

For a resistor, $V = IR$. For a capacitor, $I = C\,dV/dt$. For an inductor, $V = L\,dI/dt$.

A good value for the thermal voltage, V_T, at room temperature is 0.02585 V. You may use an approximate value.

Approximately, $\ln 10 \approx 2.3$. Moreover, $e^{-0.7} \approx 0.5$.

The vacuum permittivity is approximately $8.85 \times 10^{-12}\,\mathrm{F/m}$.

The (absolute) elementary charge is approximately $1.6 \times 10^{-19}\,\mathrm{C}$.

At a given time, the power dissipation is defined by $P(t) = I(t)V(t)$.

At room temperature, the intrinsic carrier density of silicon, n_i, is 10^{10} /cm^3.

The built-in potential in a pn junction is given by $V_0 = V_T \ln\frac{N_A N_D}{n_i^2}$.

1. Consider the crystalline silicon. The position vector of any silicon atom can be written as either $\left(\frac{j+k}{2}, \frac{i+k}{2}, \frac{i+j}{2}\right)a$ or $\left(\frac{j+k}{2}+\frac{1}{4}, \frac{i+k}{2}+\frac{1}{4}, \frac{i+j}{2}+\frac{1}{4}\right)a$ in the Cartesian coordinate system. In this problem, i, j, and k are arbitrary integers and a is 0.543 nm. The mass of each silicon atom is 4.66 X 10^{-23} g. Calculate the mass density of silicon. Your answer should have a unit of (g/cm3).

2. Assume that the intrinsic carrier density of silicon follows the following formula:

$$n_i = 5.2 \times 10^{15}\, T^{1.5} \exp\left(-\frac{E_g}{2k_B T}\right) (\#/\mathrm{cm}^3)$$

In this expression, T is the absolute temperature in K, $E_g = 1.12\,\mathrm{eV}$, and $k_B = 8.617 \times 10^{-5}\,\mathrm{eV/K}$. At 300 K, the intrinsic carrier density is about 1X10^{10} cm^{-3}. Estimate the intrinsic carrier density at 400 K.

3. In the lecture, it has been stressed that the diode current-voltage graph shows a slope of 60 mV/dec. (When it is drawn in the semi-log scale.) However, as we know, "60 mV" is a rough value valid only at room temperature. At 77 K (The boiling temperature of liquid nitrogen), what is the additional voltage required to increase the diode current by a factor of 10?

4. Assume a constant-voltage model for diodes. The turn-on voltage of the diode is V_{on}. Consider both of a positive V_{in} and a negative V_{in}. Draw V_{out} as a function of V_{in}. Also, write down $V_{out}(V_{in})$.

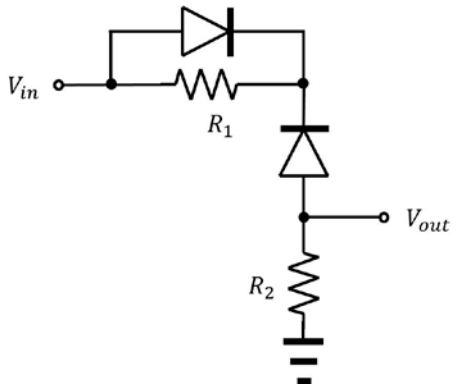

Fig. P4

5. Consider a circuit shown in Fig. P5. Express the voltage for the load resistor as a function of time.

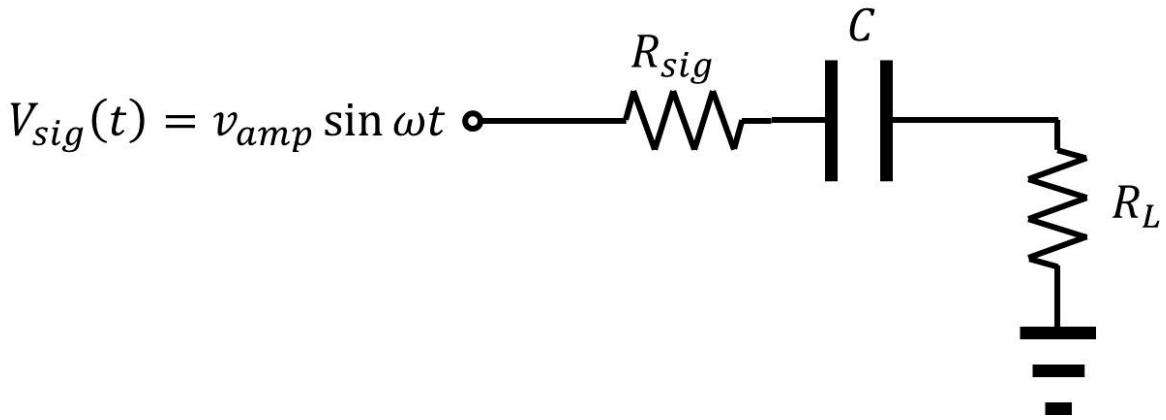

Fig. P5

6. For the circuit in P5, the (angular) frequency, ω, is fixed. Also the signal amplitude (v_{amp}) and the internal resistance (R_{sig}) are fixed. We can change only C and R_L. Describe how we can set C and R_L to maximize the power delivered to the load resistor.

7. For the circuit shown in Fig. P7, find the labeled node voltages, V_1, V_2, and V_3. The NMOS transistors have a threshold voltage of 1.0 V. $\mu_n C_{ox} \frac{W}{L} = 2\ \text{mA/V}^2$. Neglect the channel-length modulation.

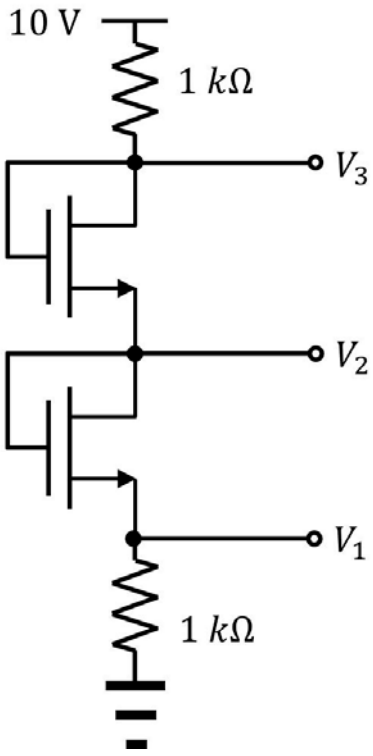

Fig. P7

8. In the lecture, we have studied the common-source amplifier. Write down the voltage gain (with a correct sign), the input impedance, and the output impedance. Consider the channel-length modulation with r_O. The load resistance is infinitely large.

9. In the lecture, we have studied the common-gate amplifier. Write down the voltage gain (with a correct sign), the input impedance, and the output impedance. Consider the channel-length modulation with r_O. The load resistance is infinitely large.

10. In the lecture, we have studied the source follower. Write down the voltage gain (with a correct sign), the input impedance, and the output impedance. Consider the channel-length modulation with r_O. The load resistance is infinitely large.

11. Calculate the small-signal voltage gain of a common-source amplifier with a correct sign. The threshold voltage of the transistor is 0.4 V. $\mu_n C_{ox} = 400\ \mu\text{A/V}^2$. Its width is ten-times wider than its length. Neglect the channel-length modulation. Also, let $V_{DD} = 1.8\ \text{V}$, $R_D = 17.5\ k\Omega$, and $V_{GS} = 0.6\ \text{V}$.

12. Calculate the dc power dissipation of the common-source amplifier in P11.

13. Consider the amplifier in P11. Estimate the maximum amplitude of a sinusoidal small-signal gate voltage to keep the MOSFET in the saturation region.

14. Calculate the (time-averaged) ac power dissipation by R_D in P11. Use the small-signal amplitude of the gate voltage, which is obtained in P13.

15. In Fig. P15, an equivalent small-signal circuit is shown. Calculate the resistance, r_X, defined as

$$r_X = \frac{v_X}{i_X}$$

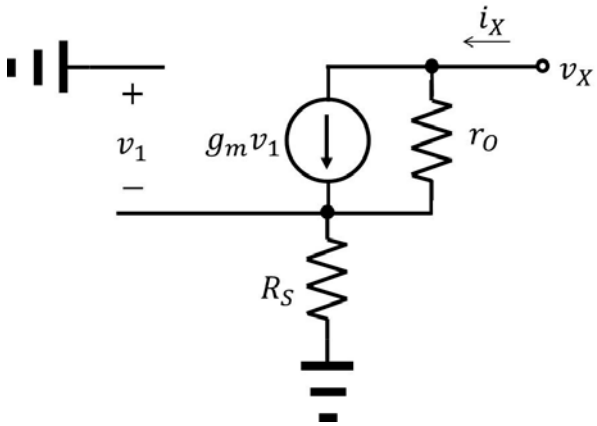

Fig. P15

16. Calculate r_X in P15. In this problem, $r_O = R_s = 20\ k\Omega$ and $g_m = 1.25$ mS.

17. In the lecture, we didn't consider a circuit topology wherein the input is applied to the drain and the output is sensed at the source. In this problem, we consider such a circuit topology. V_G is constant. Assume that the MOSFET has an output resistance of r_O. Also the transconductance is denoted as g_m. Express the voltage gain in terms of g_m, r_O, and R_s.

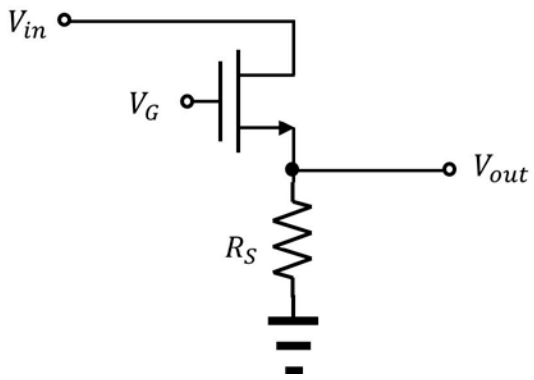

Fig. P17

18. Calculate the input impedance of the circuit in P17.

19. Calculate the output impedance of the circuit in P17.

20. A common-source amplifier utilizes a MOSFET with $\mu_n C_{ox} = 400\ \mu A/V^2$ and W/L = 10. In this problem, unlike many other problems, consider the channel-length modulation. $\lambda = \frac{1}{9}\ V^{-1}$. It is biased at a dc drain current of 0.2 mA and uses $R_D = 10\ k\Omega$. let $V_{DD} = 3.0$ V. Calculate the voltage gain with a correct sign.

21. Find the input/output impedances of the common-source amplifier in P20.

22. A common-gate amplifier using an NMOS transistor for which $g_m = 4$ mA/V has a 5 kΩ drain resistance and a 5 kΩ load resistance. The amplifier is driven by a voltage source having a 500 Ω resistance. What is the overall voltage gain? Note that the input signal voltage is different from the source terminal voltage in this problem.

23. A common-gate amplifier is required to match a signal source whose internal resistance is 100 Ω. (In other words, the input impedance of the common-gate amplifier should be 100 Ω.) It is operated at a gate overdrive voltage of 0.2 V. The drain resistance is 2 kΩ. Of course, the transistor is in the saturation model. Write the dc drain current and the overall voltage gain. Again, note the input signal voltage is different from the source terminal voltage in this problem.

24. Design a source follower. The output resistance of the source follower should be $200\,\Omega$. The MOSFET has $\mu_n C_{ox} = 400\,\mu\text{A/V}^2$ and is operated at $V_{GS} - V_{TH} = 0.25\,\text{V}$. Find the required W/L ratio. Also specify the dc bias current.

25. Consider the source follower in P24. If the amplifier load resistance varies over the range $1\,k\Omega$ to $10\,k\Omega$, what is the range of the voltage gain of the source follower? Write your answer with a correct sign.

26. Design an NMOS inverter. The power supply $V_{DD} = 2.5\,\text{V}$. When the input voltage is V_{DD}, the output voltage is 0.1 V and the current is 50 μA. Let the transistor be specified to have V_{TH} = 0.5 V and $\mu_n C_{ox} = 125\,\mu\text{A/V}^2$. Neglect the channel-length modulation. Specify the required values of W/L and R_D.

27. Consider the NMOS inverter in P26. A load capacitor is 30 fF. Initially, the input voltage is V_{DD}. At t=0, the input voltage suddenly becomes 0 V. Calculate the time required for the output voltage to be 1.3 V.

28. Find the dynamic power dissipation of an inverter operated from a 1.8-V supply and having a load capacitance of 100 fF. Let the inverter be switched at 100 MHz.

29. Initially, the capacitor (80 fF) was charged up to V_{DD} = 1.8 V. The NMOSFET was turned off. At t=0, the input voltage suddenly becomes V_{DD}. The stored charges in the capacitor are discharged. Calculate the time required for the NMOSFET to enter into the triode mode. Assume that $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.4\,\text{V}$, $W = 1.0\,\mu\text{m}$, and $L = 0.18\,\mu\text{m}$.

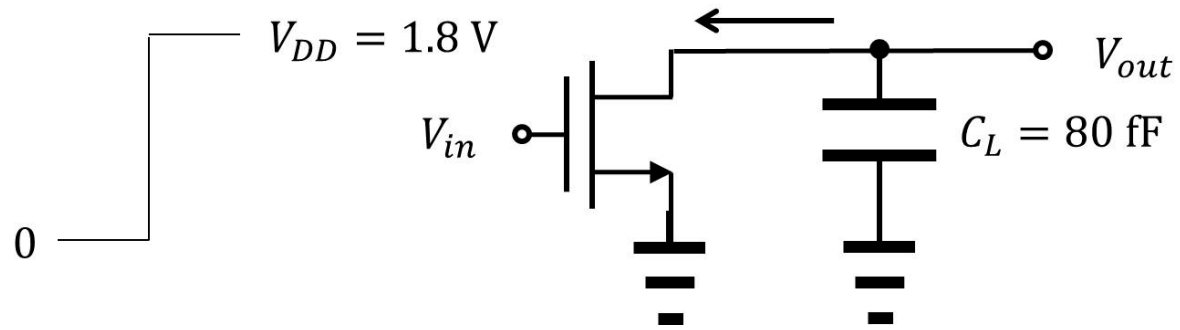

Fig. P29

30. Consider the situation in P29. Now the NMOSFET is in the triode mode. Calculate the additional time required for the capacitor voltage to become $\frac{V_{DD}}{2}$, 0.9 V.

31. Repeat P29 with V_{DD} = 0.9 V.

32. Repeat P30 with V_{DD} = 0.9 V.

33. Consider a CMOS inverter fabricated in a 0.18-μm process for which V_{DD} = 1.8 V, $V_{TH,N}$ = 0.5 V, $V_{TH,P}$ = -0.5 V, $\mu_n = 4\mu_p$, and $\mu_n C_{ox} = 300\ \mu A/V^2$. In addition, both MOSFETs have $L = 0.18\ \mu m$. The width of the NMOSFET is $W_n = 0.27\ \mu m$. When the input voltage is 0.9 V, the output voltage is also 0.9 V. Find the width of the PMOSFET, W_p. .

34. For the matched case in P33, two noise margins for high/low inputs are the same. Calculate the nose margin. Your answer should have a unit of (mV).

35. We have studied the concept of the output impedance. For the matched case of P33, calculate the output impedance. Of course, no small-signal is applied in the input terminal.

36. Instead of the matched case, consider a case of $W_p = W_n$. Since it is not matched, two noise margins are different. The smaller one is taken as the noise margin. Calculate the noise margin. Your answer should have a unit of (mV).

37. Repeat P36 with $W_p = 2W_n$.

38. In P34, P36, and P37, three different CMOS inverters have been considered. For these three cases, calculate $L(W_n + W_p)$.

39. You have two NMOSFETs and two PMOSFETs. Using those elements, implement Y = A NOR B. Draw the circuit schematic in your answer sheet. Clearly identify your NMOSFETs and PMOSFETs.

40. You have three NMOSFETs and three PMOSFETs. Using those elements, implement Y = NOT (A OR (B AND C)). Draw the circuit schematic in your answer sheet. Clearly identify your NMOSFETs and PMOSFETs.