Lecture19:
Digital CMOS circuits (2)

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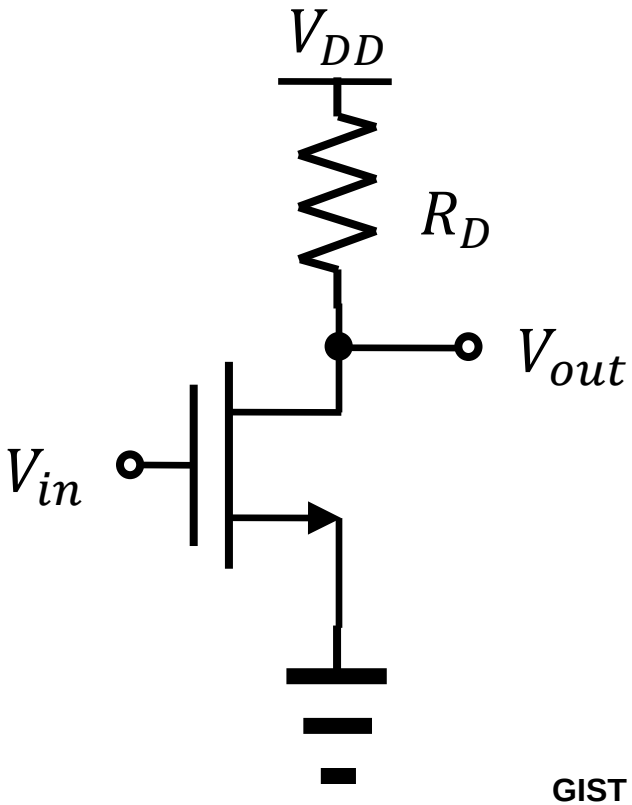
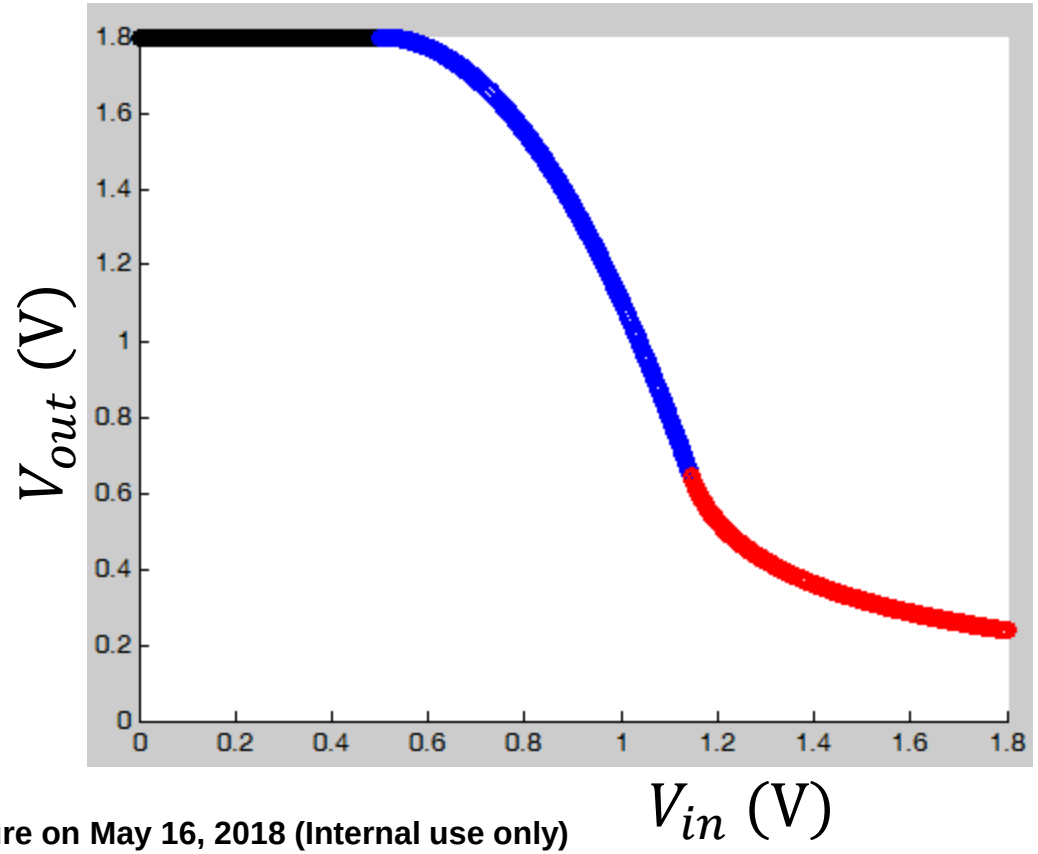
Review of last lecture

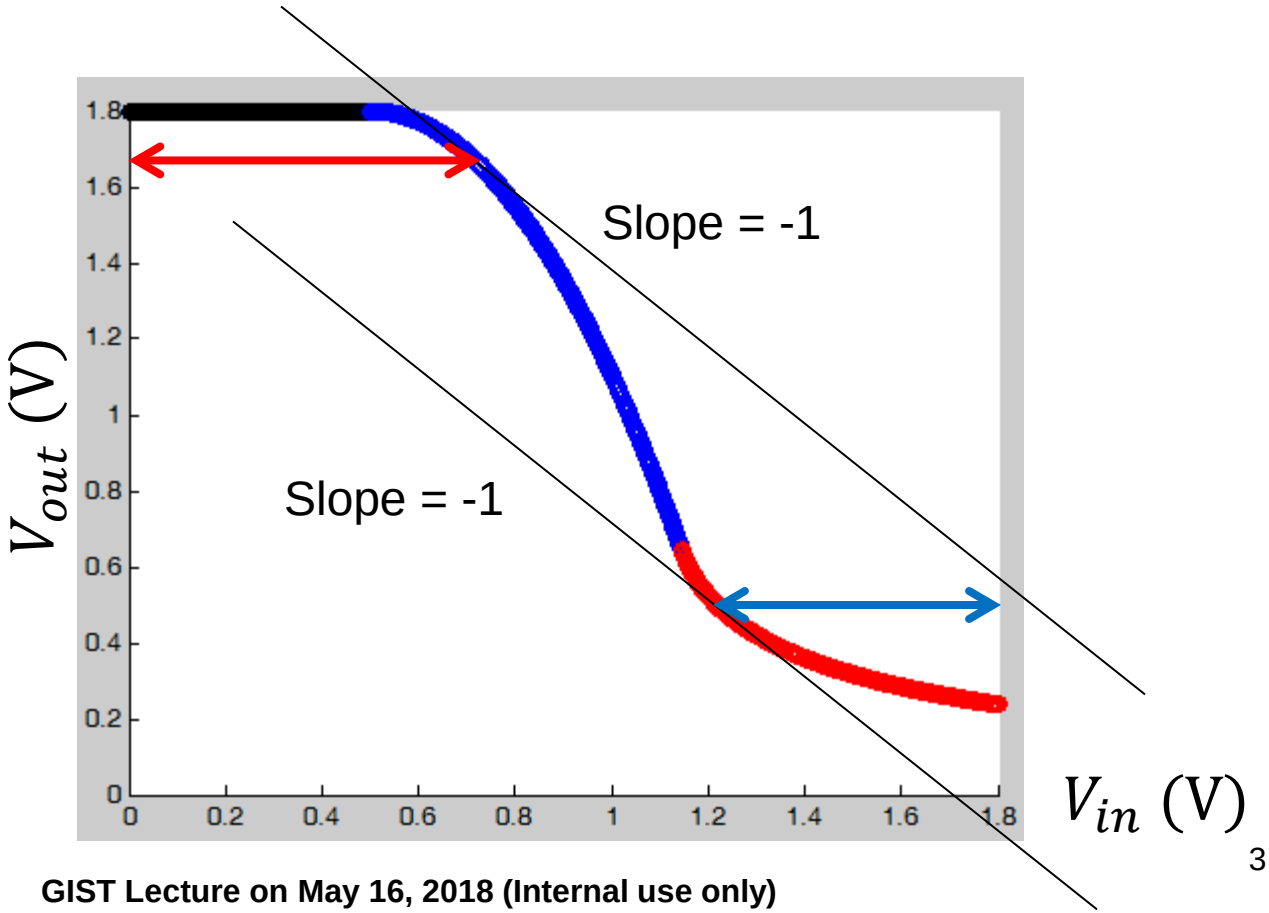
- Numeric calculation can be done with a binary system.
- Inverters and NAND gates are important.
- And, the NMOS inverter was introduced.





Noise margin

- Verbatim
  - “Noise margin is the maximum amount of degradation (noise) at the input that can be tolerated before the output is affected significantly.”



Noise margin of CS stage

- Let's calculate NM_L.
  - In this case, (blue curve)

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})^2$$

  - Taking the differentiation w. r. t. V_{in},

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}R_D(V_{in} - V_{TH})$$

  - At $V_{in} = NM_L$, the slope becomes -1,

$$NM_L = \frac{1}{\mu_n C_{ox}\frac{W}{L}R_D} + V_{TH}$$

  - (Stronger NMOS yields a reduces NM_L.)

Common-source

- Common-source configuration
  - It can be used as an amplifier. The slope, $\frac{dV_{out}}{dV_{in}}$, is the voltage gain.
  - It can be also used as an inverter.