
Lecture24: CMOS inverter

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NMOS inverter

- Passive “pull-up” device

- (a) Degradation of output level

Too small R_D , when $V_{in} = V_{DD}$.

In this case, large R_D is desirable.

- (b) Risetime limitation

Too small current for 1 \rightarrow 0 transition. ($V_{in} = 0$)

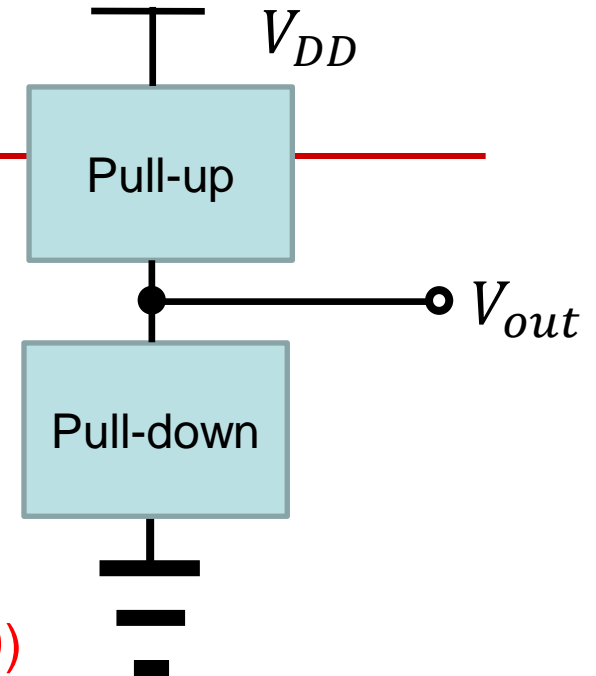
In this case, a better capability to charge the C_L is desirable.

- (c) Static power consumption

No ability to block the current, when $V_{in} = V_{DD}$.

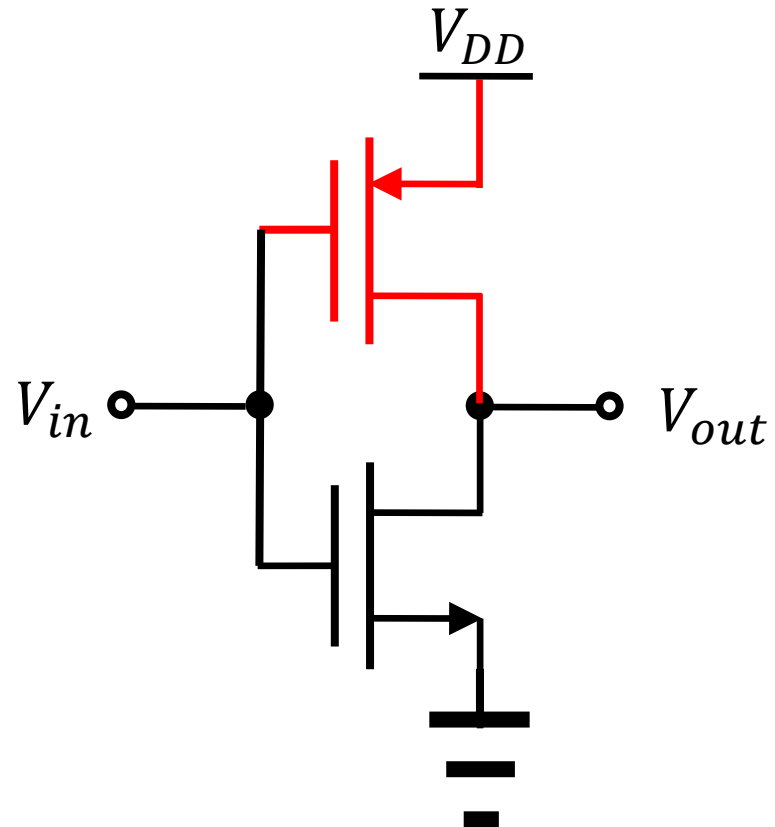
In this case, no current conduction is desirable.

- (a) & (c) \leftrightarrow (b)



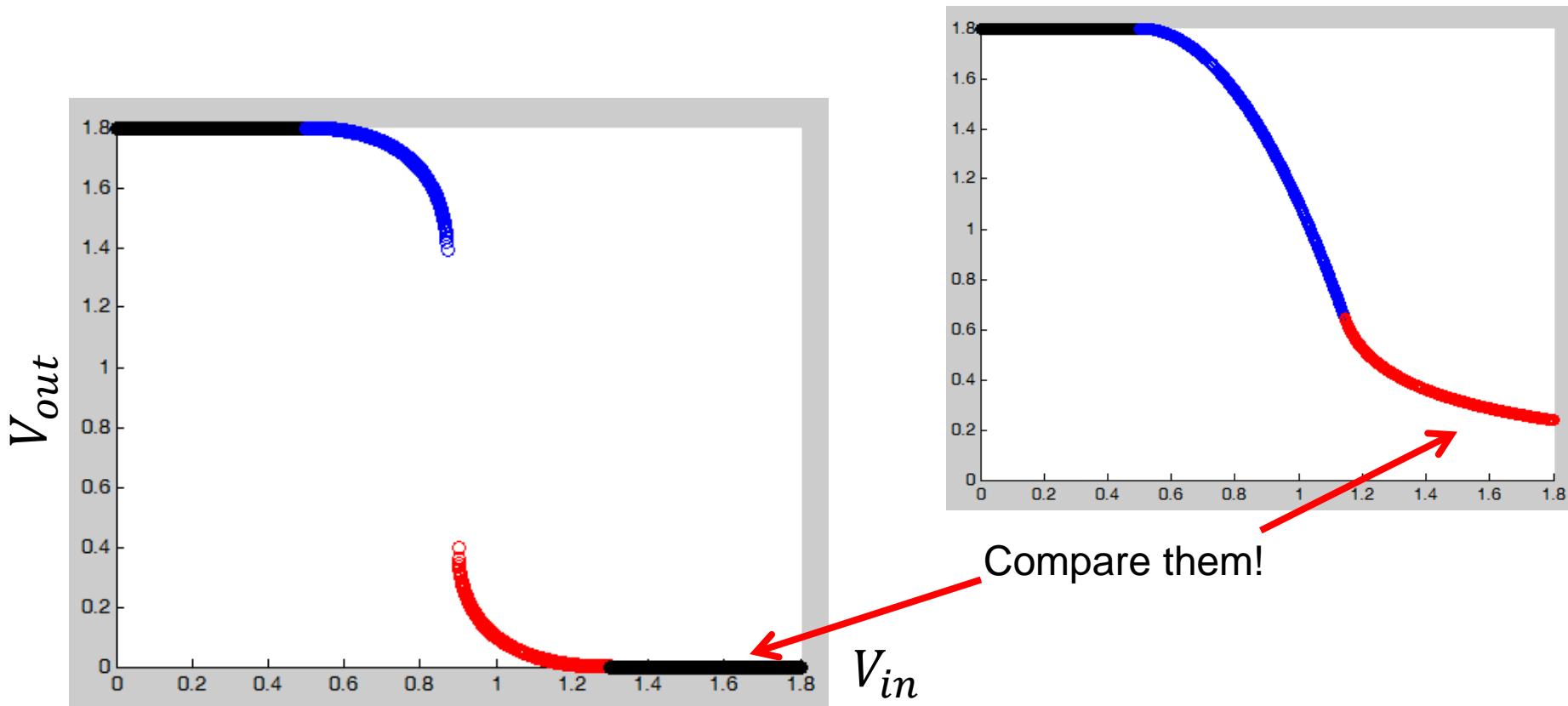
CMOS inverter

- Ideal “pull-up” should have the following properties.
 - When $V_{in} = V_{DD}$, no current conduction.
 - When $V_{in} = 0$, improved current conduction.
- PMOS can do those jobs!



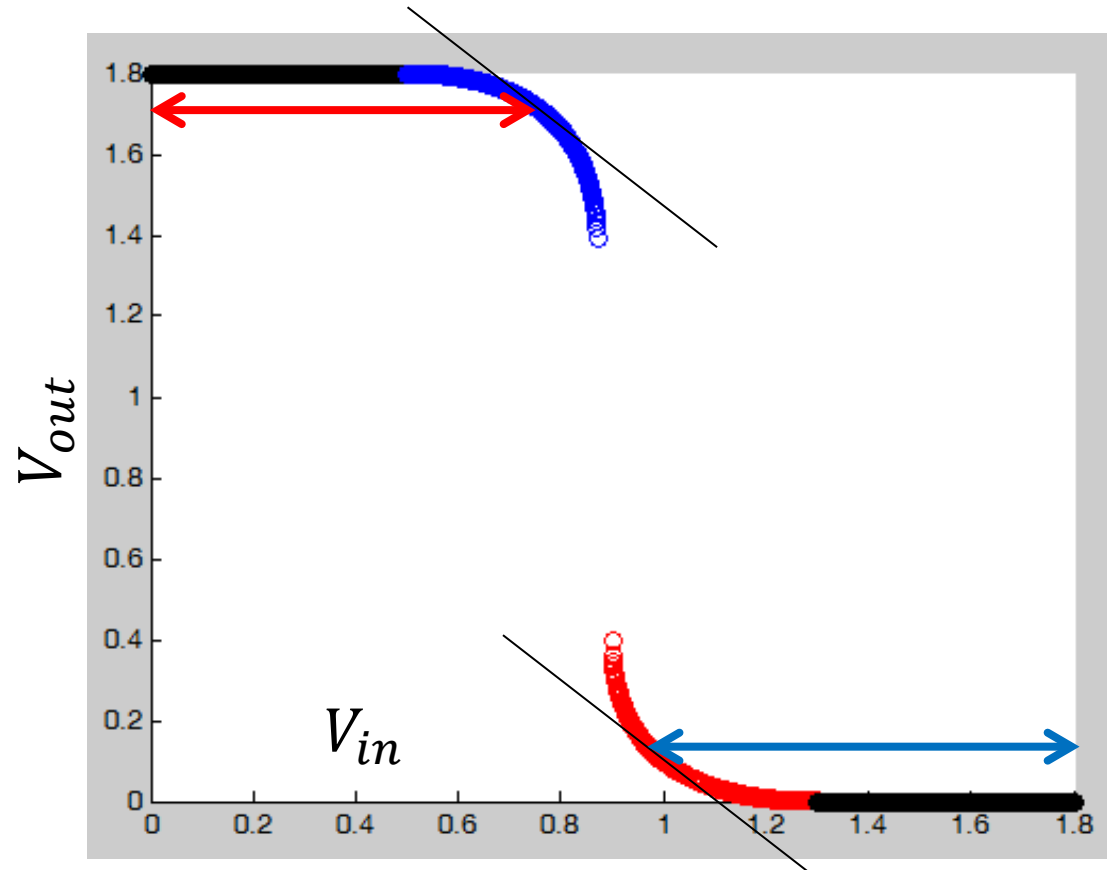
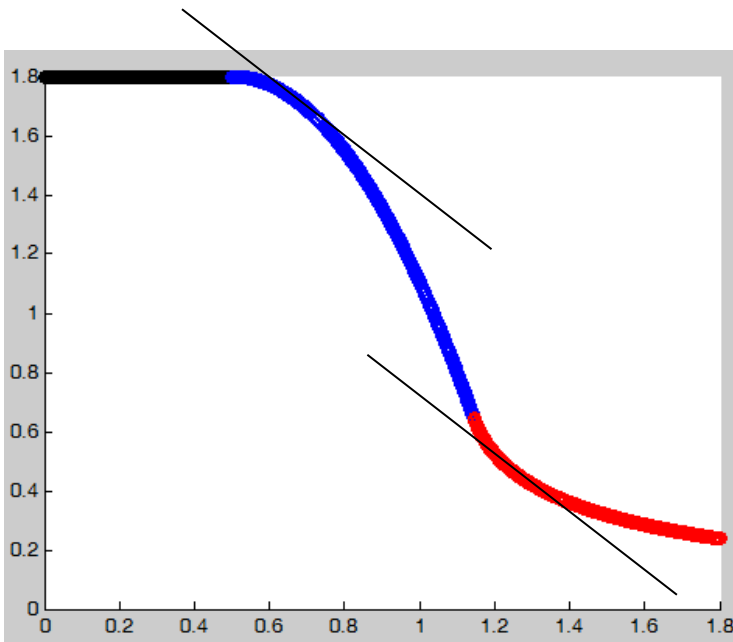
CMOS inverter

- Voltage transfer curve of a CMOS inverter



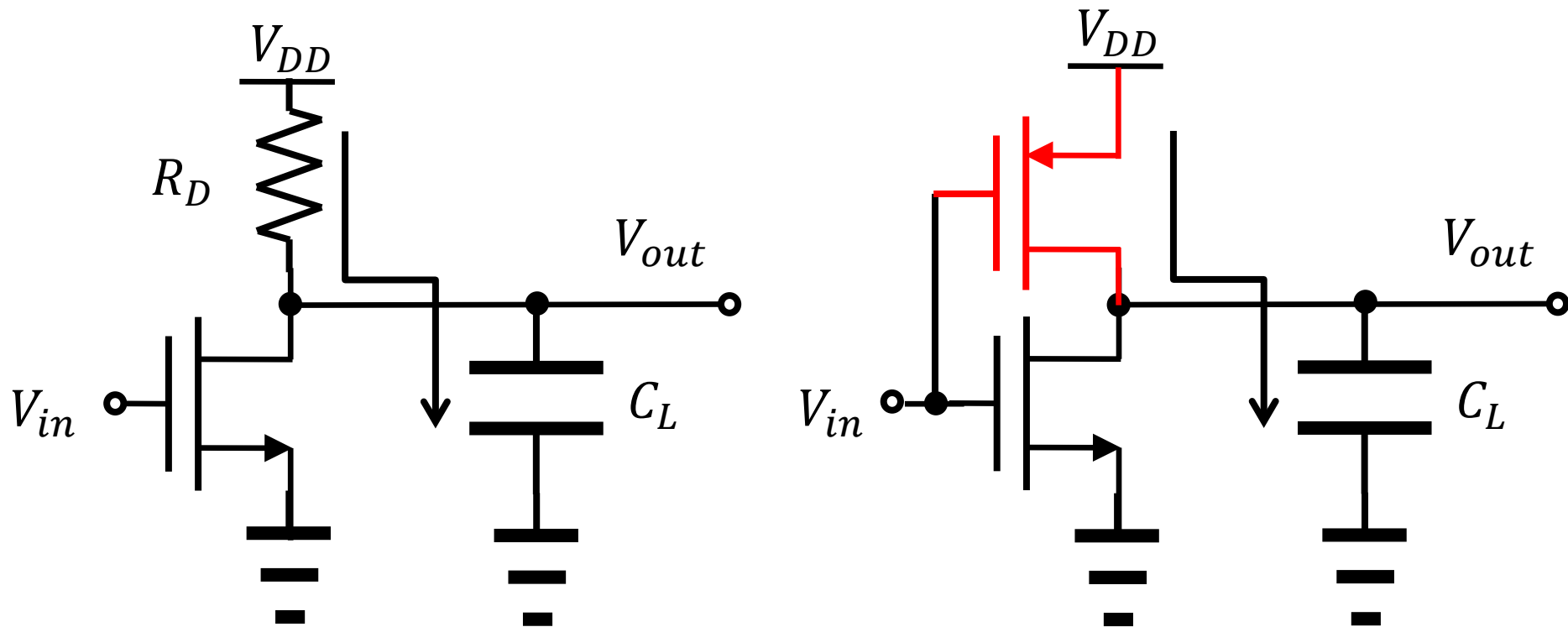
Noise margin?

- Greatly improved!
 - Steeper transition



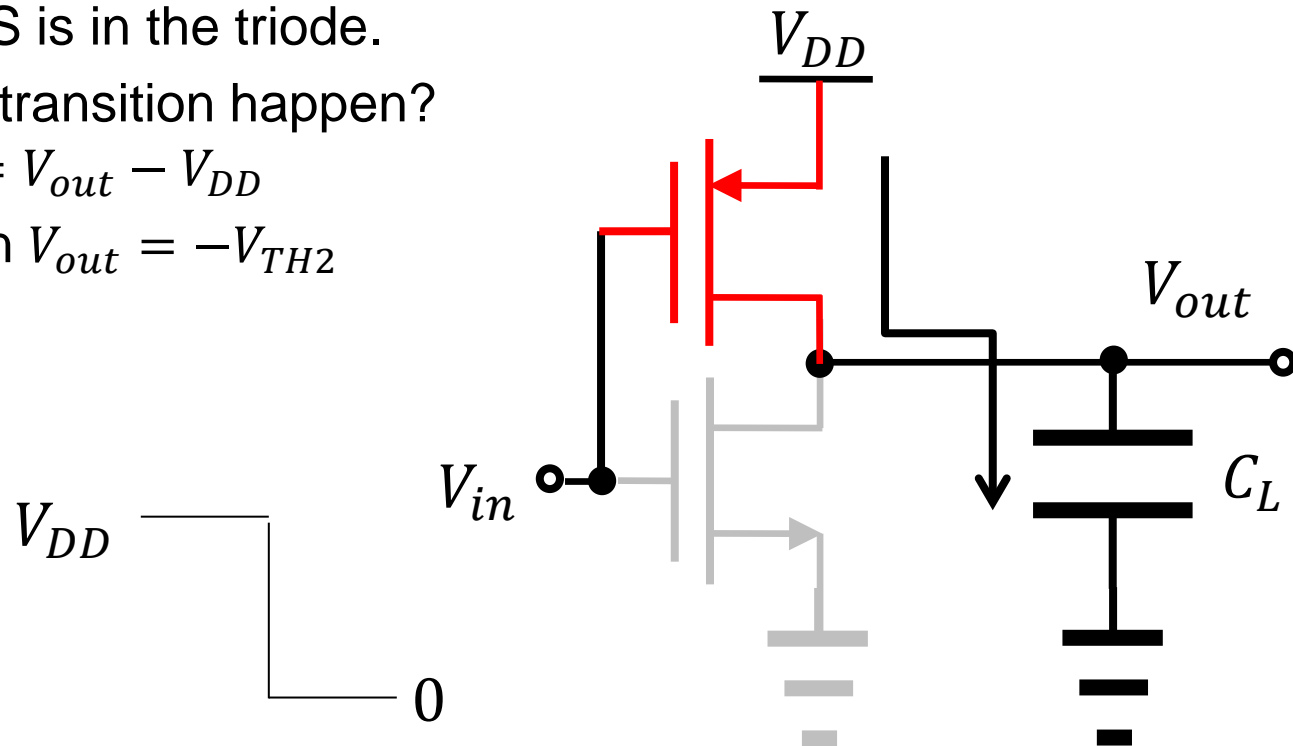
Speed of CMOS inverter (1/4)

- Consider the input transition from HIGH to LOW.
 - Instead of the resistor (R_D), now the PMOS pulls up the V_{out} .



Speed of CMOS inverter (2/4)

- Guess the charging speed.
 - The PMOS current matters. ($I_{PMOS} = C_L \frac{dV_{out}}{dt}$)
 - Initially, the PMOS is in the saturation.
 - Later, the PMOS is in the triode.
 - When does the transition happen?
- $V_{in} - V_{DD} - V_{TH2} = V_{out} - V_{DD}$
- Therefore, when $V_{out} = -V_{TH2}$

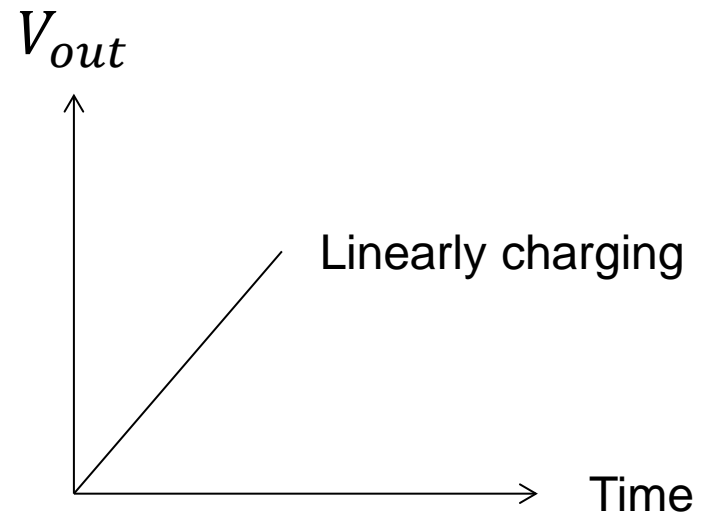


Speed of CMOS inverter (3/4)

- The first case (charge up to $-V_{TH2}$)
 - PMOS saturation current (constant)

$$T_{PLH1} = \frac{C_L |V_{TH2}|}{\frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{DD} - |V_{TH2}|)^2}$$

$$T_{PLH1} = R_{on2} C_L \frac{2|V_{TH2}|}{V_{DD} - |V_{TH2}|}$$



Speed of CMOS inverter (4/4)

- The second case (charge up to $\frac{V_{DD}}{2}$)

- PMOS triode current

$$\frac{1}{2} \mu_p C_{ox} \frac{W}{L} [2(V_{DD} - |V_{TH2}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2] = C_L \frac{dV_{out}}{dt}$$

- Time to reach $\frac{V_{DD}}{2}$

$$T_{PLH2} = R_{on2} C_L \ln \left(3 - 4 \frac{|V_{TH2}|}{V_{DD}} \right)$$

- The overall propagation delay is

- $T_{PLH} = R_{on2} C_L \left[\frac{2|V_{TH2}|}{V_{DD} - |V_{TH2}|} + \ln \left(3 - 4 \frac{|V_{TH2}|}{V_{DD}} \right) \right]$

Power consumption

- No static power dissipated!
 - Only the “dynamic” power dissipation is determined.
 - High → Low → High → ...
 - It involves charging and discharging the load capacitance.
 - The energy stored in the load capacitance

$$\frac{1}{2} C_L V_{DD}^2$$

- The energy dissipated by the PMOS is also $\frac{1}{2} C_L V_{DD}^2$.
- Therefore, $C_L V_{DD}^2$ is dissipated during T_{in} .

$$P_{av} = f_{in} C_L V_{DD}^2$$