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# Lecture21: NMOS inverter

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# Why digital?

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- You know the answer.
  - And you know what it actually is. (Binary)
- Today, we will consider the following questions:
  - How can we treat the arithmetic operations (Addition, subtraction, multiplication, ...)
  - What is the elemental operation?
  - Then, what are the essential circuits to build such a system?
  - (It will be a short review on Digital Design.)
- Inverter and NAND gates

# Addition

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- Once you can add two numbers,  $x$  and  $y$ , you can do
  - Addition,  $x + y$  (of course)
  - Subtraction,  $x - y = x + (-y)$ 
    - A simple example) 4-digit binary numbers,  $a = 0110$  and  $b = 0011$ .
    - The 1's complement of  $b$  is 1100.
    - The 2's complement of  $b$  is 1101.
    - Sum of 0110 and 1101 is 10011.
    - Discarding the end carry gives us the correct answer, 0011.
  - Multiplication,  $x \times y$

# Even in addition,

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- You can recognize that
  - Addition of two 1-bit binary numbers is the core operation!
  - There are only four possible cases!

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10 \leftarrow \text{Carry}$$

# Inclusion of carry-bit

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- We introduce a separate bit for representing the carry.

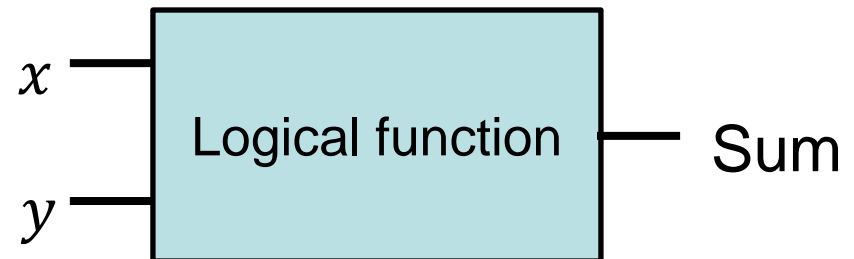
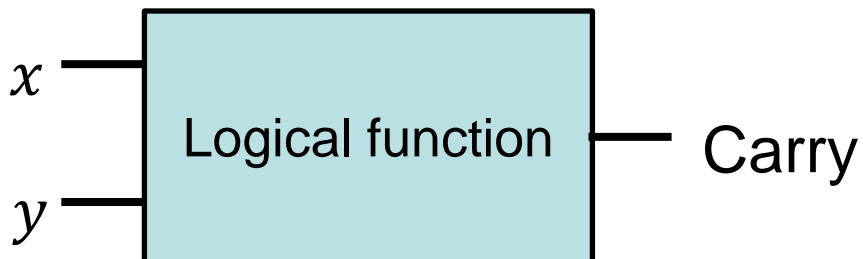
- Carry-bit & sum-bit

$$\begin{array}{rcl} 0 + 0 & = & 00 \\ 0 + 1 & = & 01 \\ 1 + 0 & = & 01 \\ 1 + 1 & = & 10 \end{array}$$

Carry

Sum

- Treat them separately!



# Relation btw $x$ , $y$ , and sum

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- Concentrate on the sum-bit.
  - A table can be made.
  - It is called a **truth table**.

$x$	$y$	sum
0	0	0
0	1	1
1	0	1
1	1	0

- Yes, it is the exclusive OR,  $x \text{ XOR } y$ .

# Relation btw $x$ , $y$ , and carry

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- Concentrate on the carry-bit.
  - A table can be made, again.

$x$	$y$	carry
0	0	0
0	1	0
1	0	0
1	1	1

- Yes, it is the AND operation,  $x$  AND  $y$

# After all,

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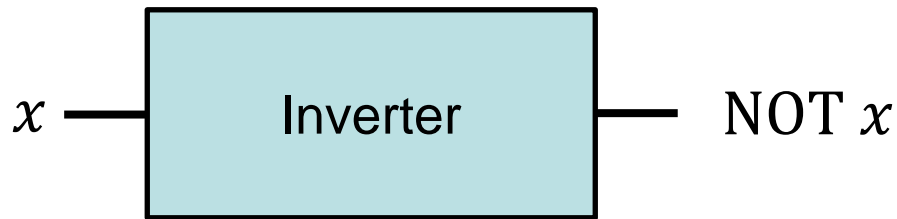
- As much as we have AND, OR, and NOT gates, we can implement any Boolean function.
  - For example,
$$x \text{ XOR } y = (x \text{ AND } (\text{NOT } y)) \text{ OR } ((\text{NOT } x) \text{ AND } y)$$
  - With NAND, NOR, and NOT gates, we can, too.



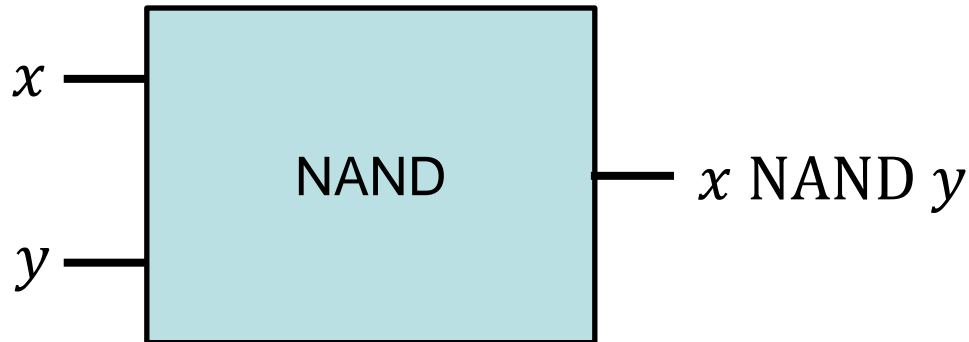
# Inverter and NAND

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- NOR can be implemented similarly.



$x$	NOT
0	1
1	0

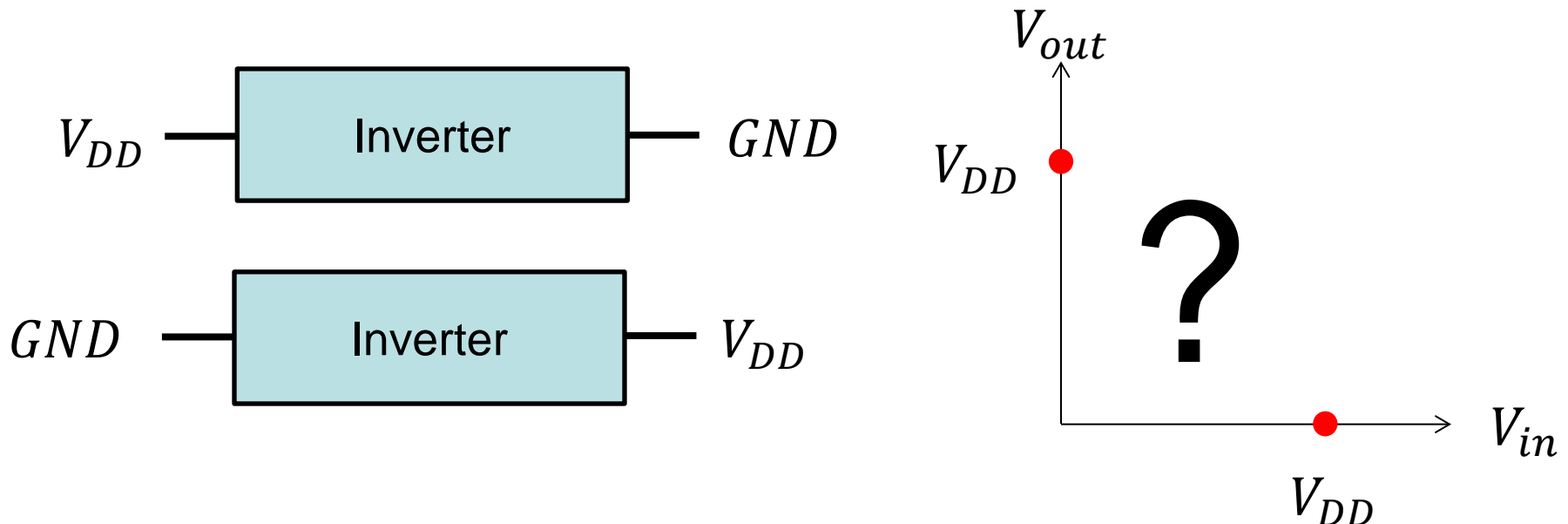


$x$	$y$	NAND
0	0	1
0	1	1
1	0	1
1	1	0

# In circuit,

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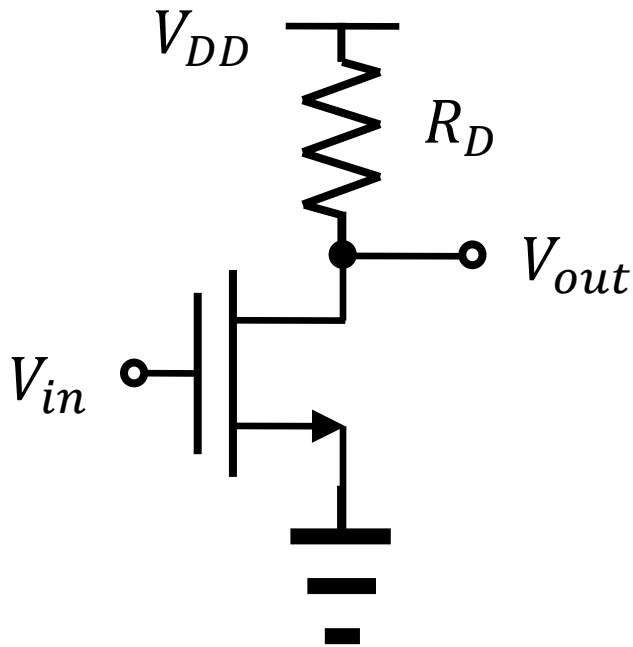
- How can we represent 0 and 1?
  - $V_{DD}$  is assigned to the logical value, 1.
  - $GND$  is assigned to the logical value, 0.



# NMOS inverter

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- How can we have an output, 0?
  - Only when the input is high. *You have seen it before!*



Vin	Vout
0	1
1	0

# Voltage transfer

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- When  $V_{in} < V_{TH}$ , trivially,  $V_{out} = V_{DD}$ .
- When  $V_{in}$  is slightly larger than  $V_{TH}$ , the NMOSFET is in the saturation region.

$$V_{out} = V_{DD} - I_D R_D$$
$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})^2$$

- When  $V_{in}$  is further increased, the NMOSFET is in the triode region.

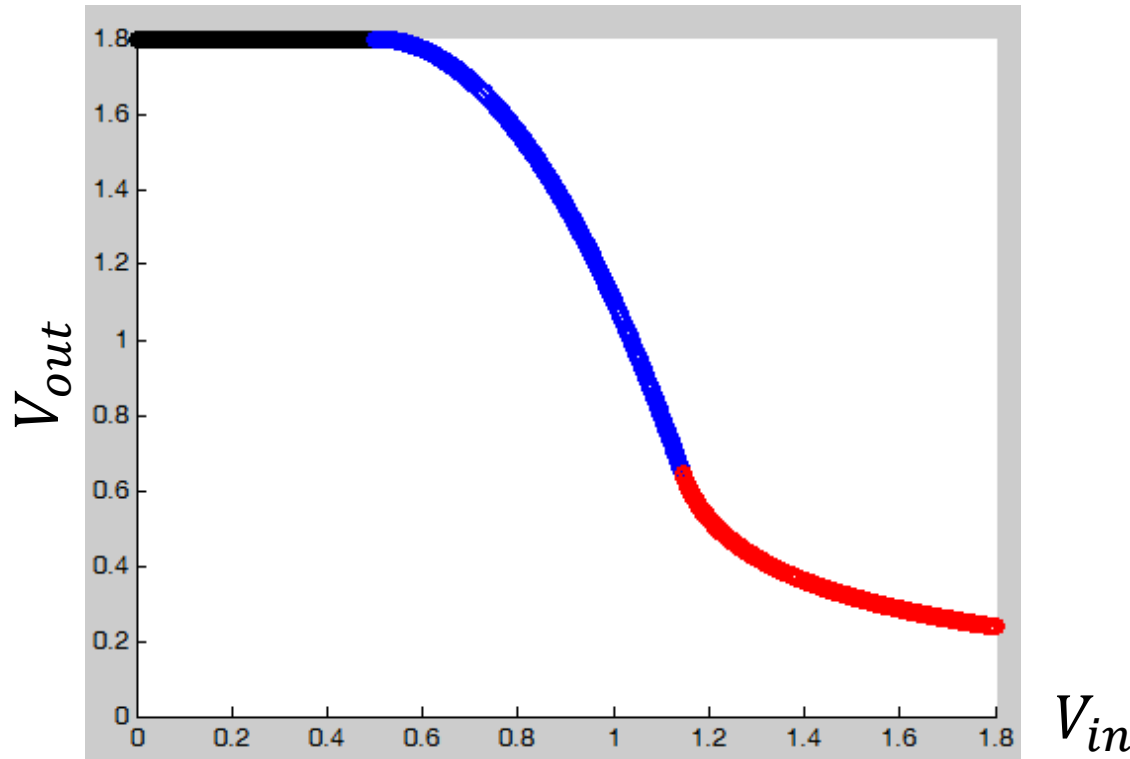
$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} R_D [2(V_{in} - V_{TH})V_{out} - V_{out}^2]$$

# Draw it! (1/2)

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- Parameters in Example 17. 14 (Razavi) w/o modification.

$$\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2, V_{TH} = 0.5 \text{ V}, \frac{W}{L} = \frac{10}{0.18}, R_D = 1\text{k}\Omega \text{ and } V_{DD} = 1.8 \text{ V}$$

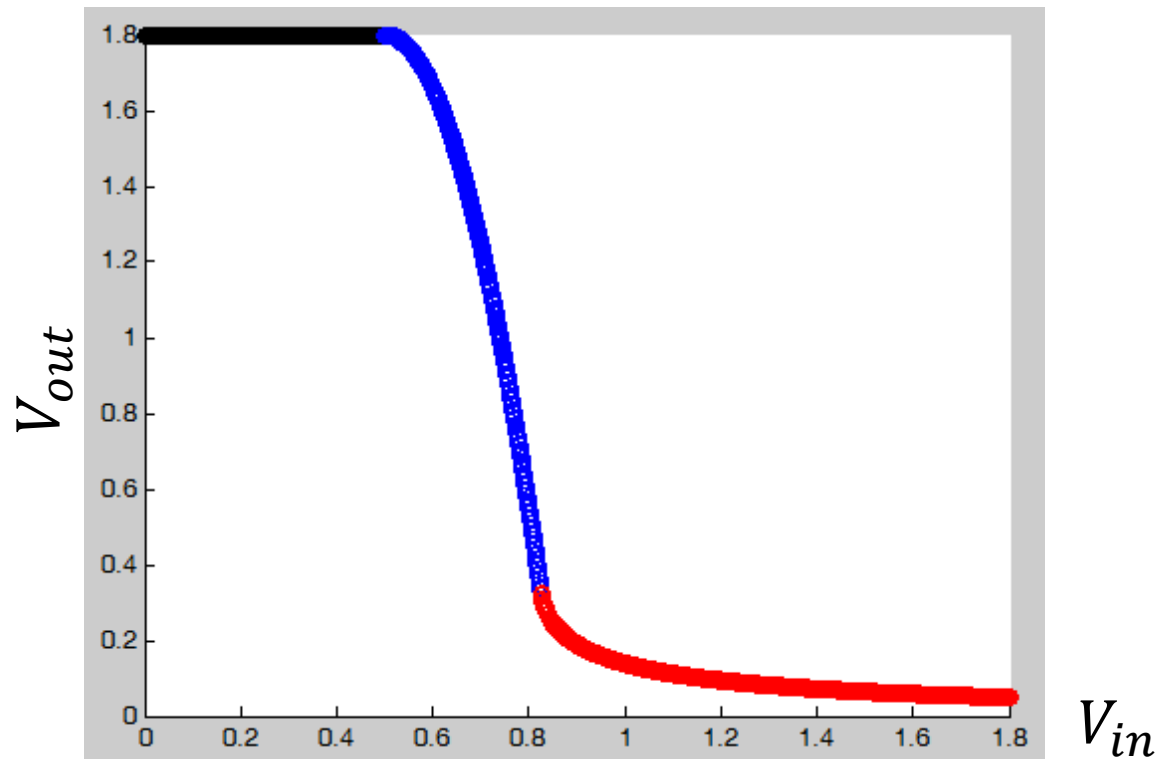


# Draw it! (2/2)

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- With a wider NMOSFET

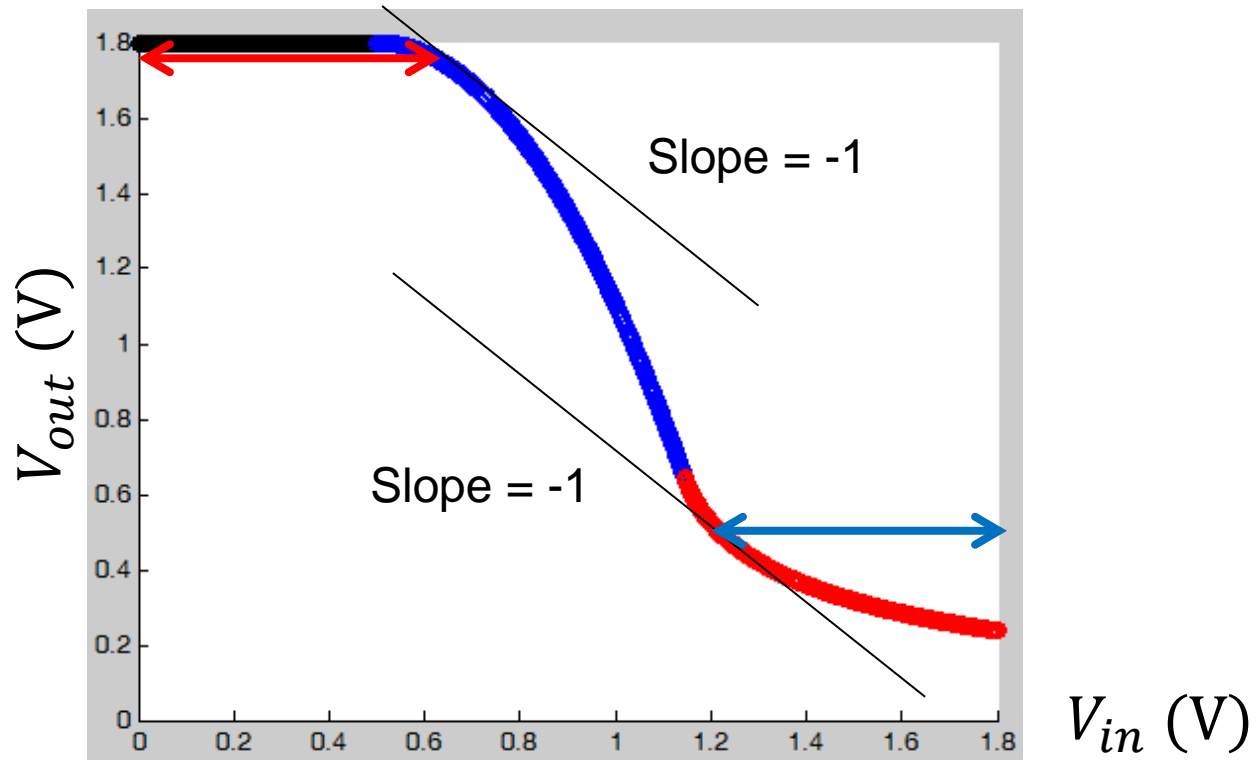
$$\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2, V_{TH} = 0.5 \text{ V}, \frac{W}{L} = \frac{50}{0.18}, R_D = 1\text{k}\Omega \text{ and } V_{DD} = 1.8 \text{ V}$$



# Noise margin

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- Verbatim
  - “(It) is the maximum amount of degradation (noise) at the input that can be tolerated before the output is affected significantly.”



# Noise margin of CS stage

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- Let's calculate  $NM_L = V_{IL}$ .

- In this case, (blue curve)

$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})^2$$

- Taking the differentiation w. r. t.  $V_{in}$ ,

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})$$

- At  $V_{in} = V_{IL}$ , the slope becomes -1,

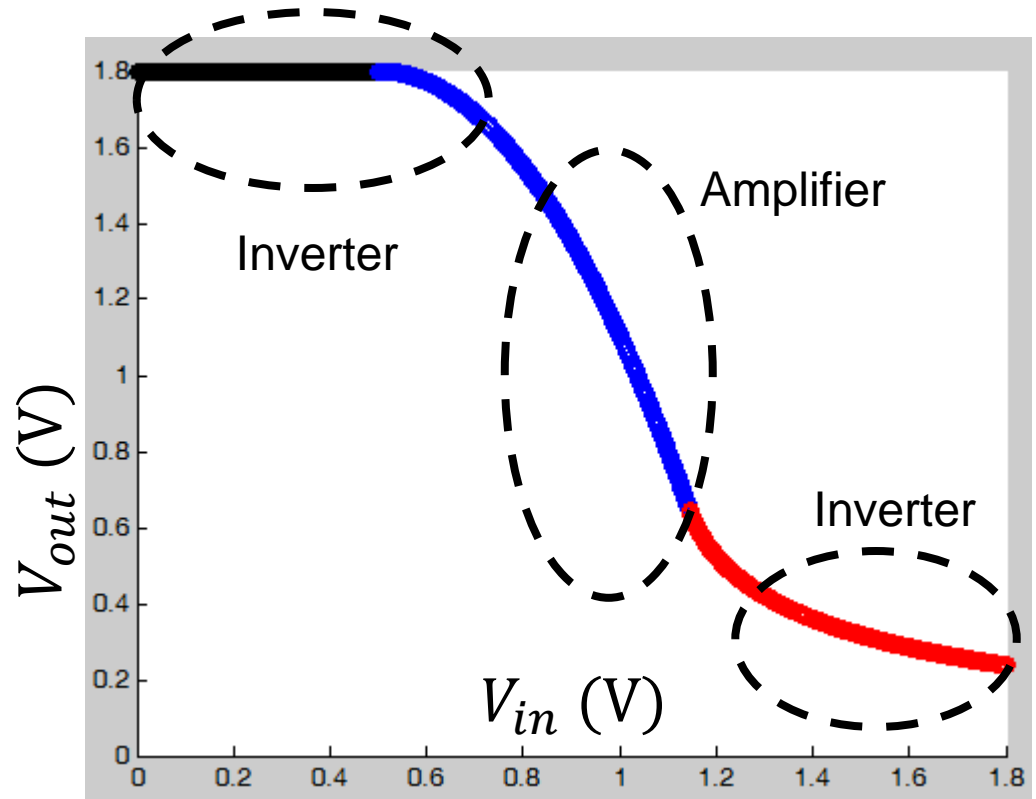
$$NM_L = V_{IL} = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_D} + V_{TH}$$

- (Stronger NMOS yields a reduces  $NM_L$ .)



# Common-source

- Common-source configuration
  - It can be used as an inverter.
  - It can be used as an amplifier.
  - $\frac{dV_{out}}{dV_{in}}$  is the voltage gain.



# Homework#9

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- Due: 09:00, **May 27 (Mon)**
- Solve the following problems of the final exam in 2018.
  - P9
  - P10
  - P11
  - P12
  - P13
  - P14