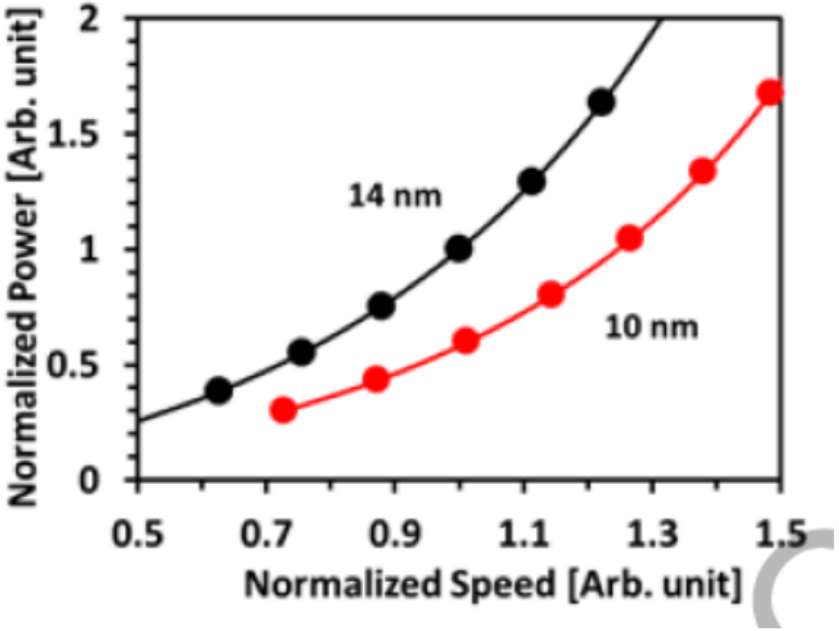
VLSI Symposium 2016

Samsung Electronics will present a 10nm logic technology developed using 3rd generation Si FinFETs for low power, high performance applications, demonstrating a speed improvement of 27% with a 40% reduction in power compared to 14nm process, achieved with multi-threshold voltage devices and reduced contact resistance.

Overcoming process challenges such as multiple patterning, high aspect ratio etching, niche gate replacements, and advanced isolation, the authors demonstrated yield analysis of a 0.04μm^2 SRAM with 128Mb cell size and observed a static noise margin of 190mV at 0.75V.



Paper T2.1, Figure 7 – "Si FinFET-based 10nm Technology with Multi V_t Gate Stack for Low Power and High Performance Applications," Cho et al., Samsung Electronics

Next Wednesday

- Bring your own PC. (Of course, with internect connection!)
  - Check your accesibility to the EDISON website.

Lecture14:
Physics of MOS transistors (2)

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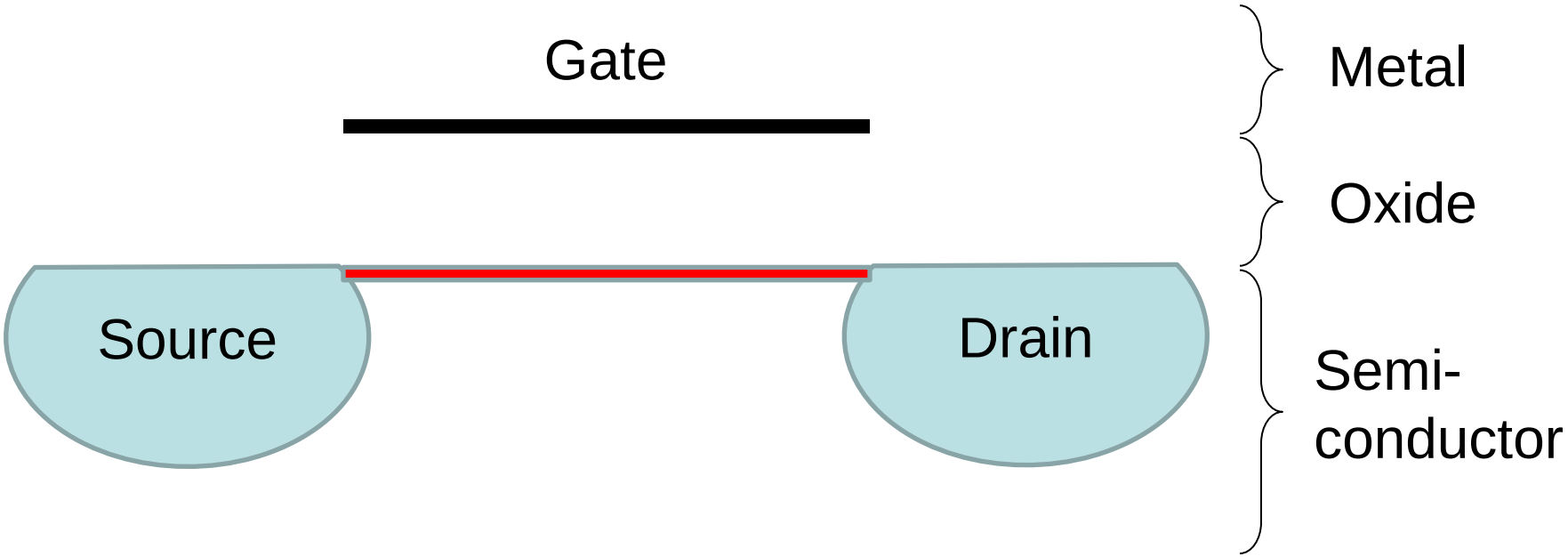
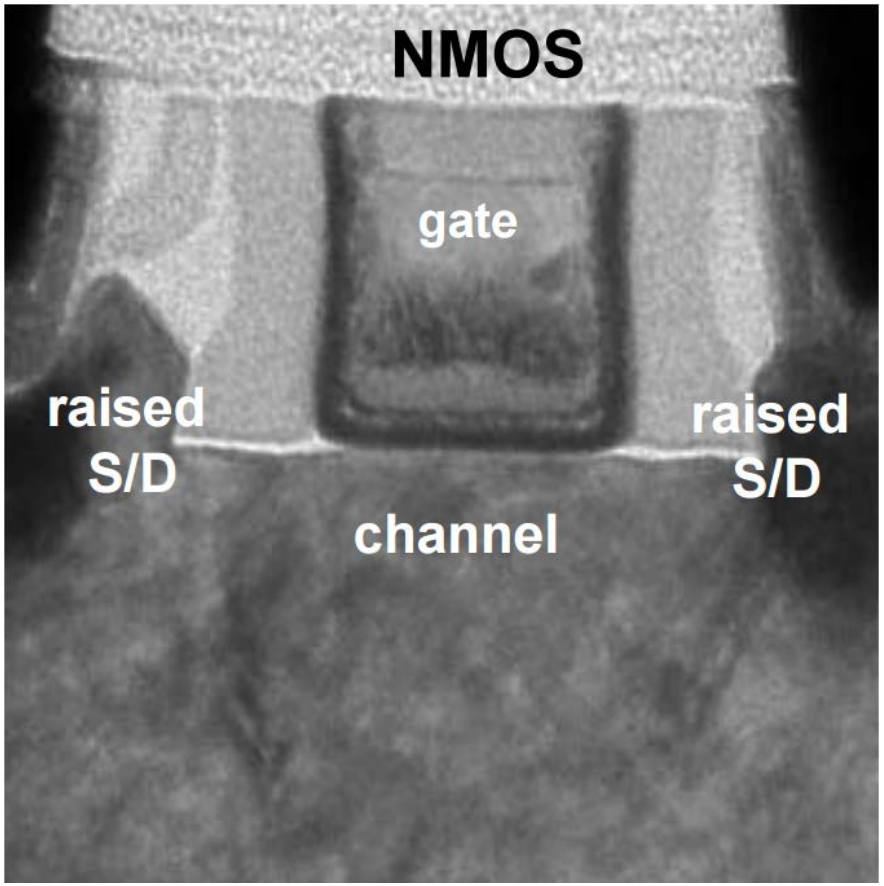
MOSFET

- Vertical structure
  - Metal-Oxide-Semiconductor
- Terminals
  - Gate, Source, Drain, (and substrate)



Actual device

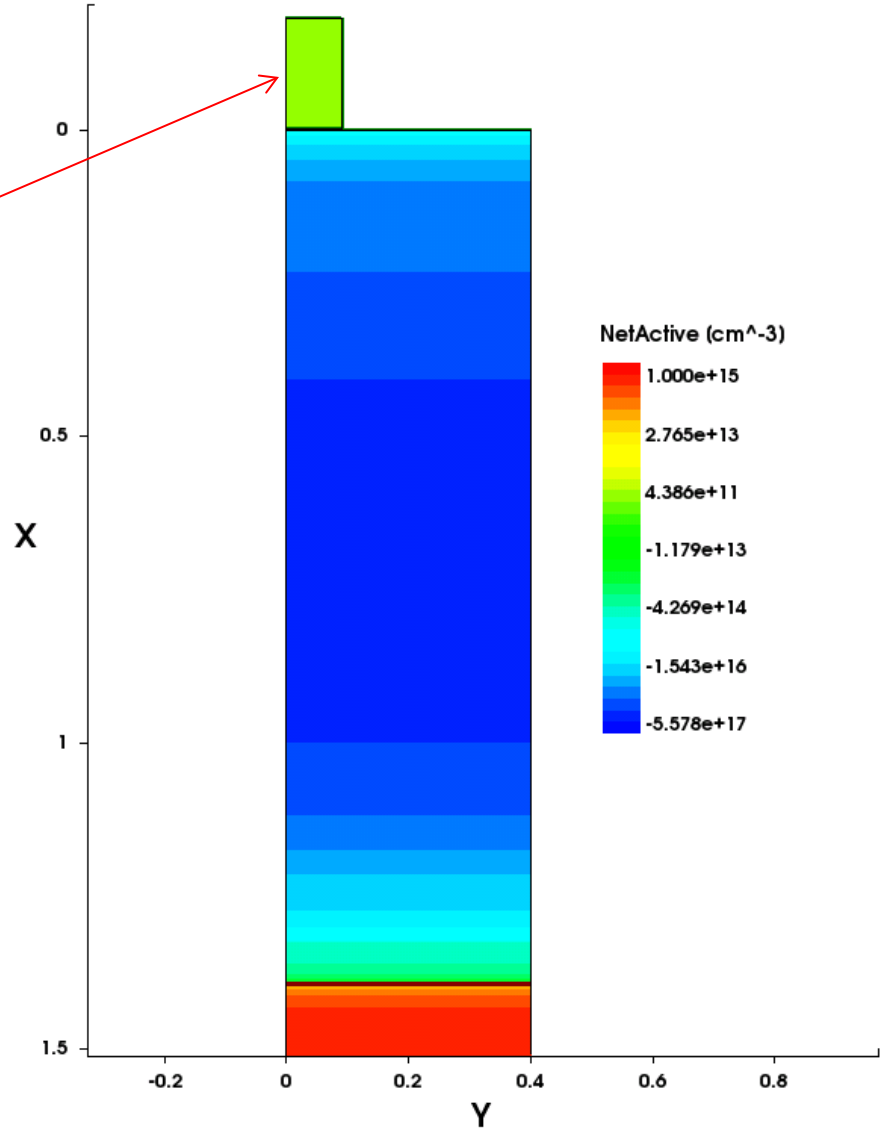
- TEM image of a MOSFET
  - 32nm node
  - (somewhat old…)



(Packan et al., IEDM 2009)

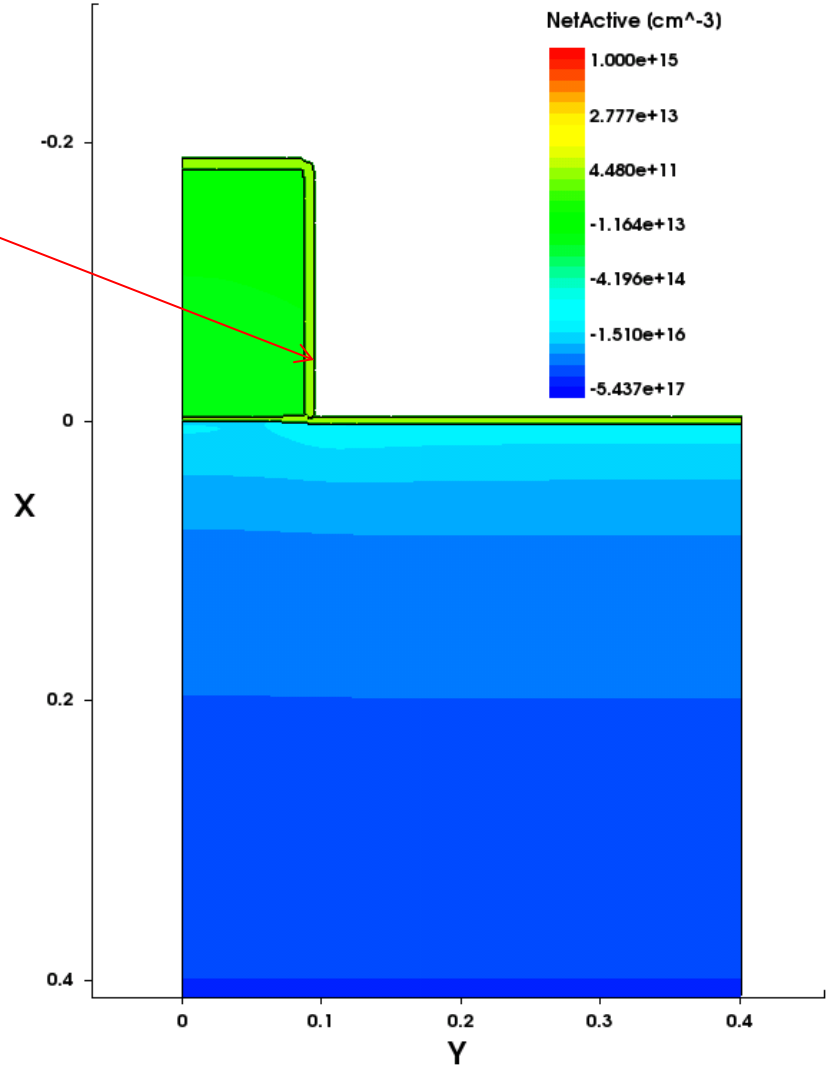
How to fabricate it (1/6)

- 0.18 μm NMOSFET
  - P-well formation
  - Gate oxidation
  - Gate definition
  - (Half structure is shown.)



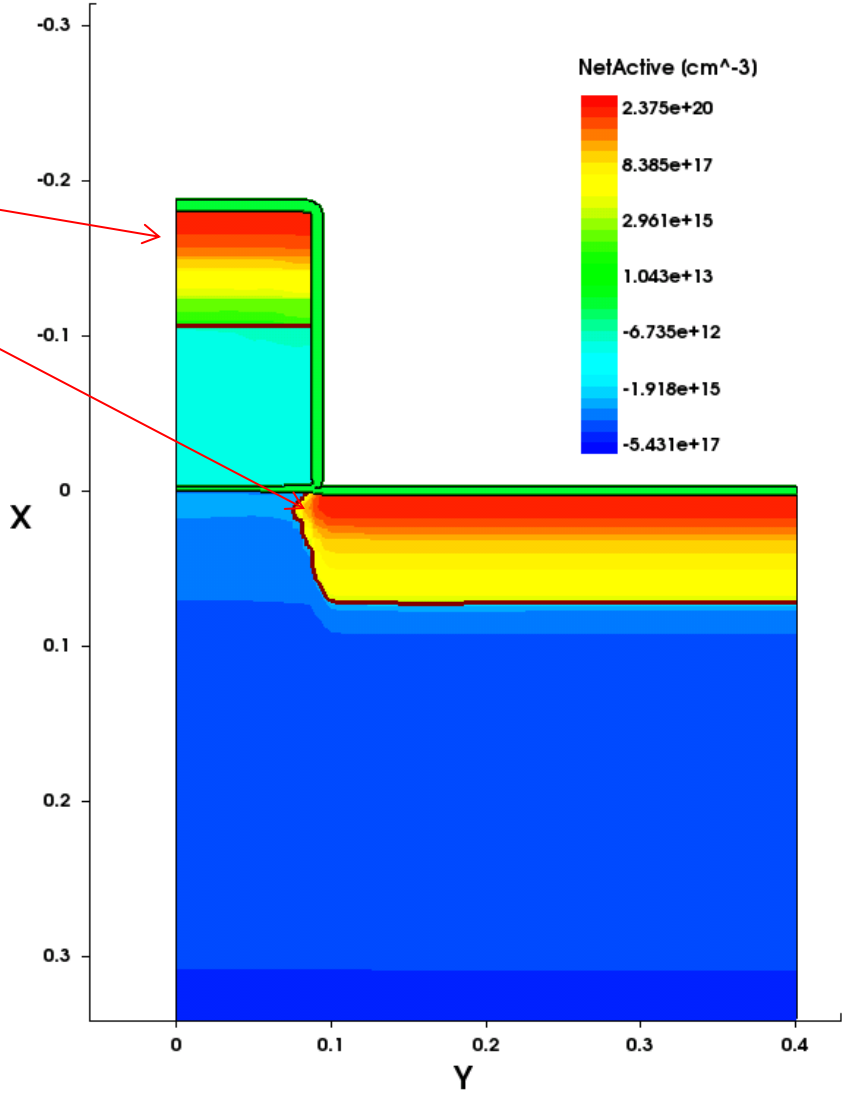
How to fabricate it (2/6)

- 0.18 μm NMOSFET
  - Gate re-oxidation



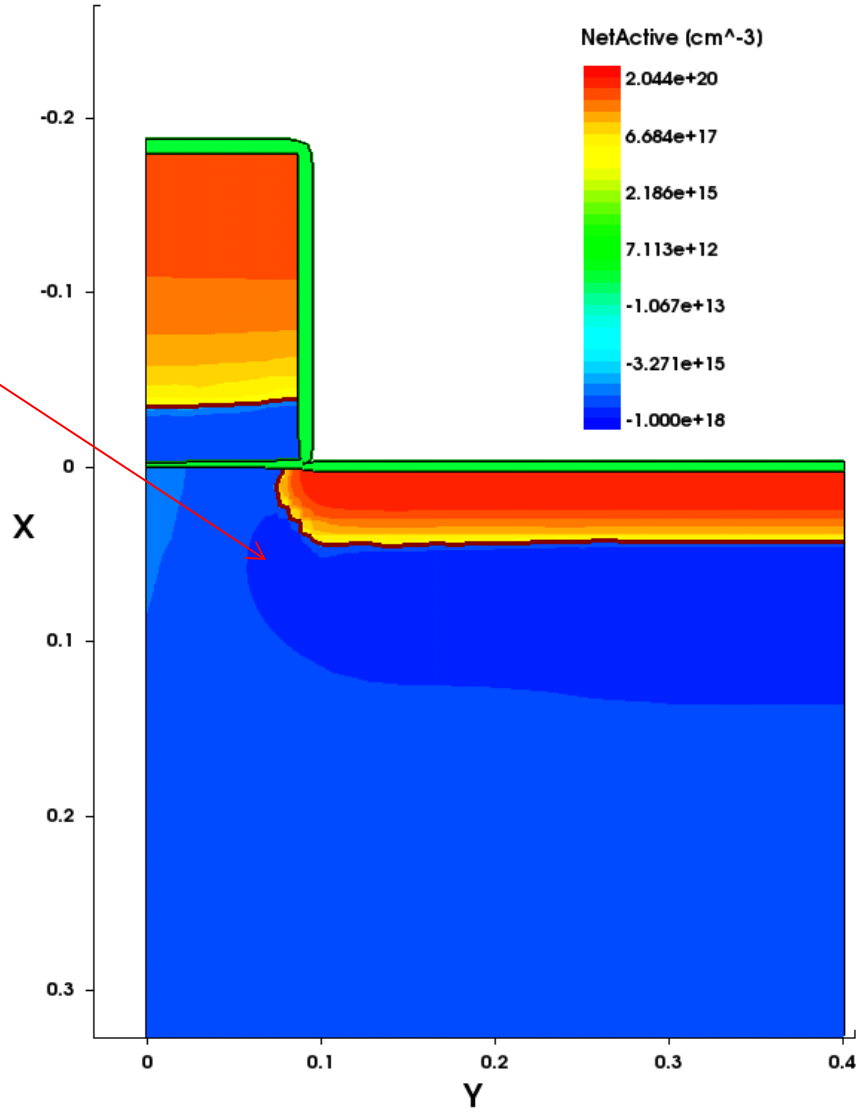
How to fabricate it (3/6)

- 0.18 μm NMOSFET
  - LDD implant



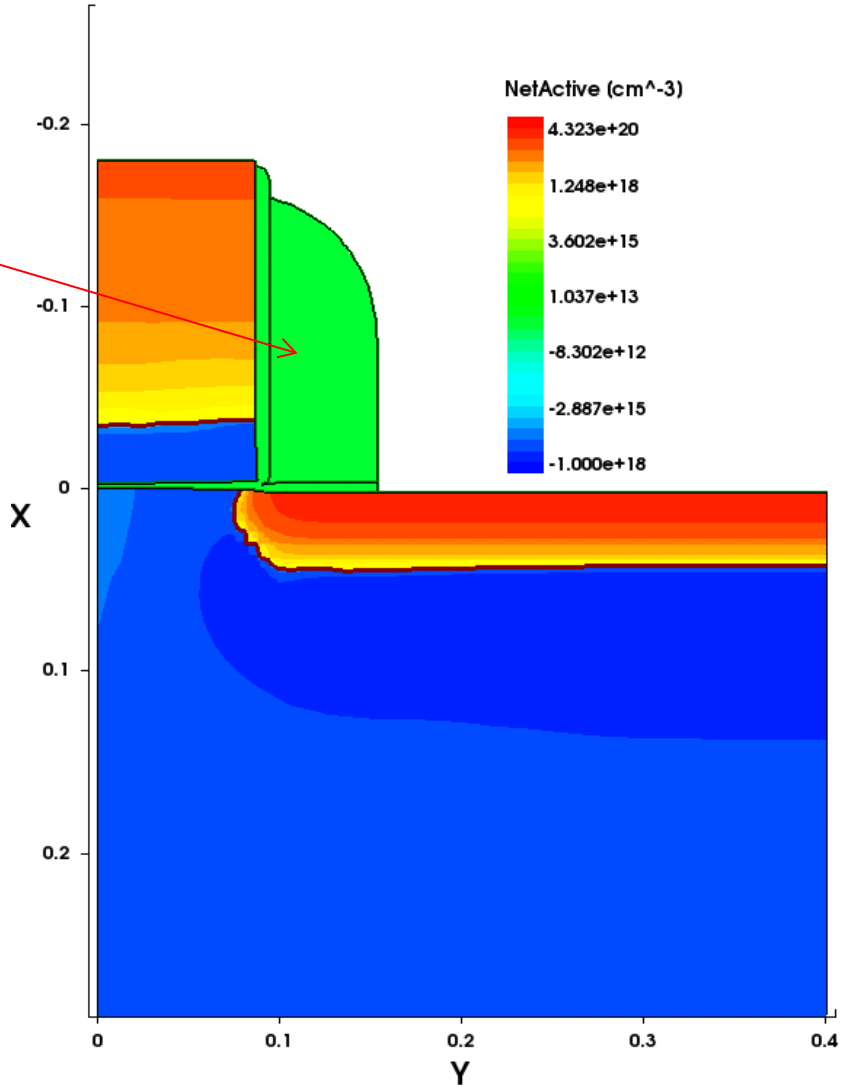
How to fabricate it (4/6)

- 0.18 μm NMOSFET
  - Halo implant



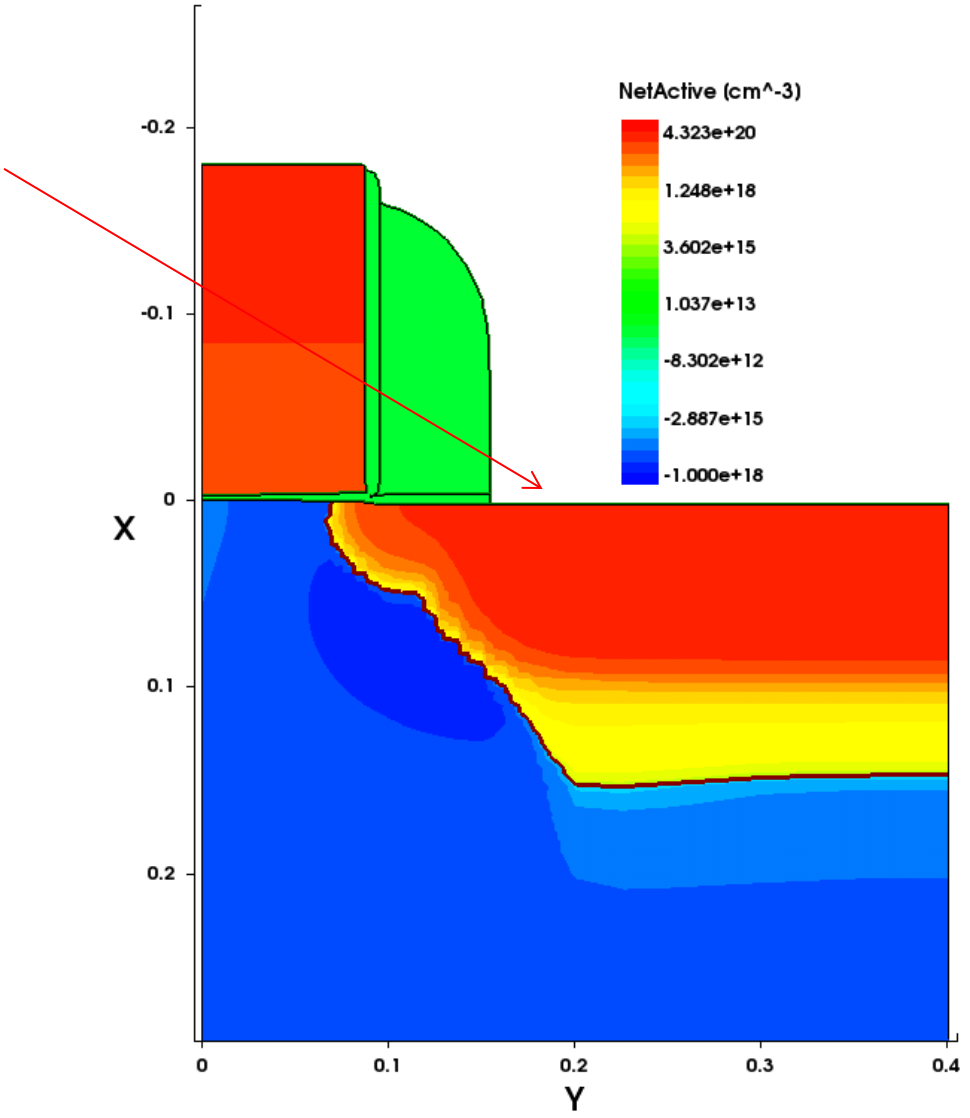
How to fabricate it (5/6)

- 0.18 μm NMOSFET
  - Nitride spacer



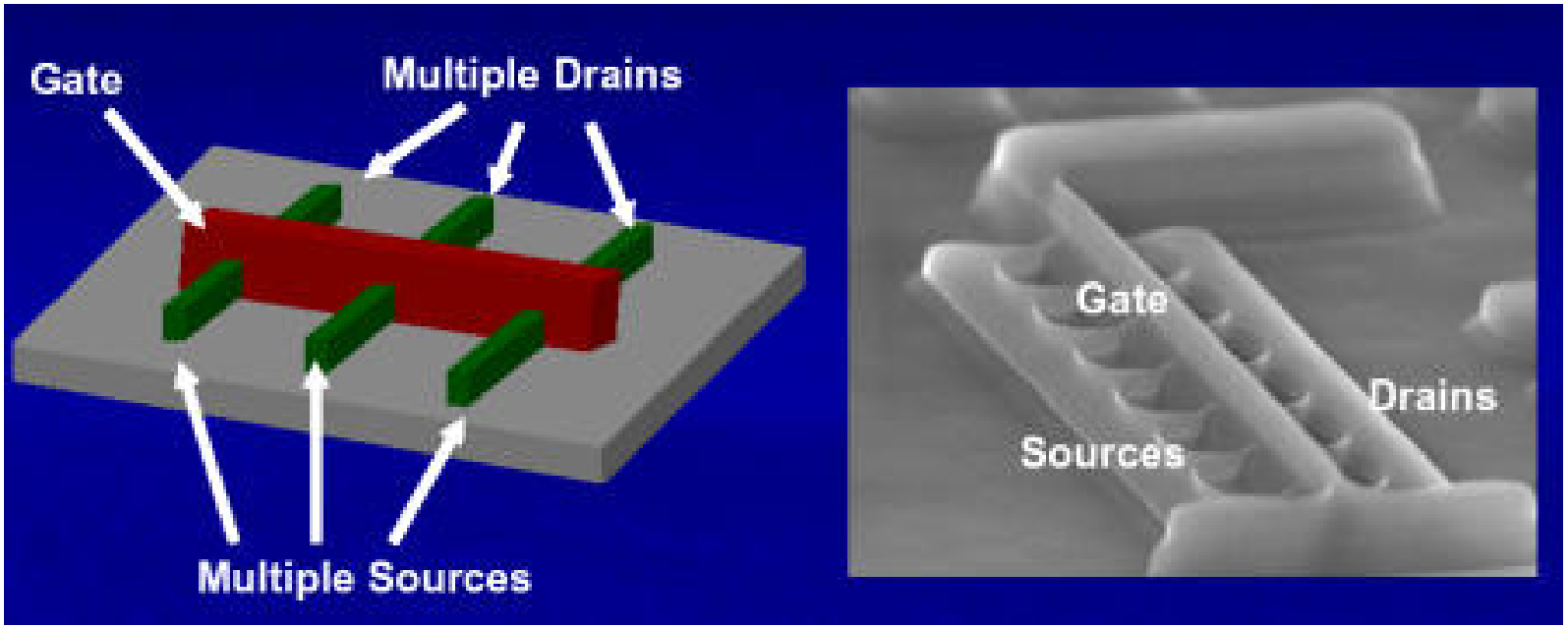
How to fabricate it (6/6)

- 0.18 μm NMOSFET
  - Source/drain implant



Top view

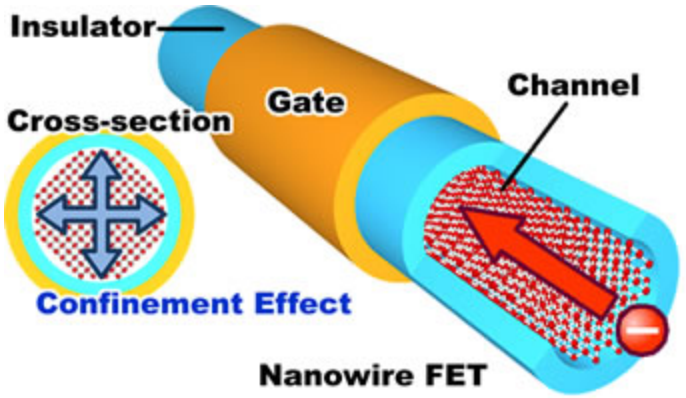
- TEM image of a MOSFET
  - 22nm node
  - (a few years ago…)



(Wikipedia)

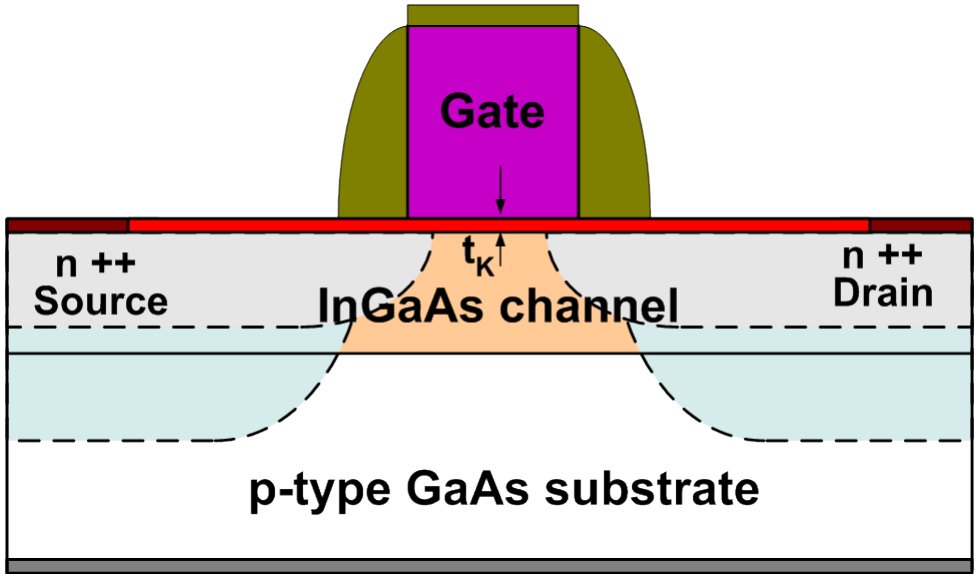
Future

- Nanowire?



(Google images)

- III-V?



(Google images)

Other application

- Up to now, we have seen the MOSFET used for the logic application.
  - CMOS RF

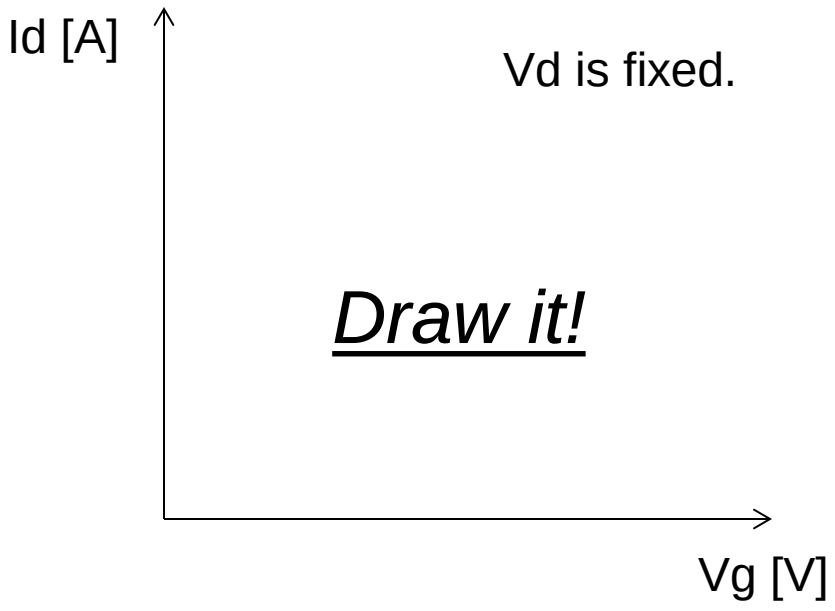
- However,
  - NAND Flash memory
  - Power device
  - Various sensors

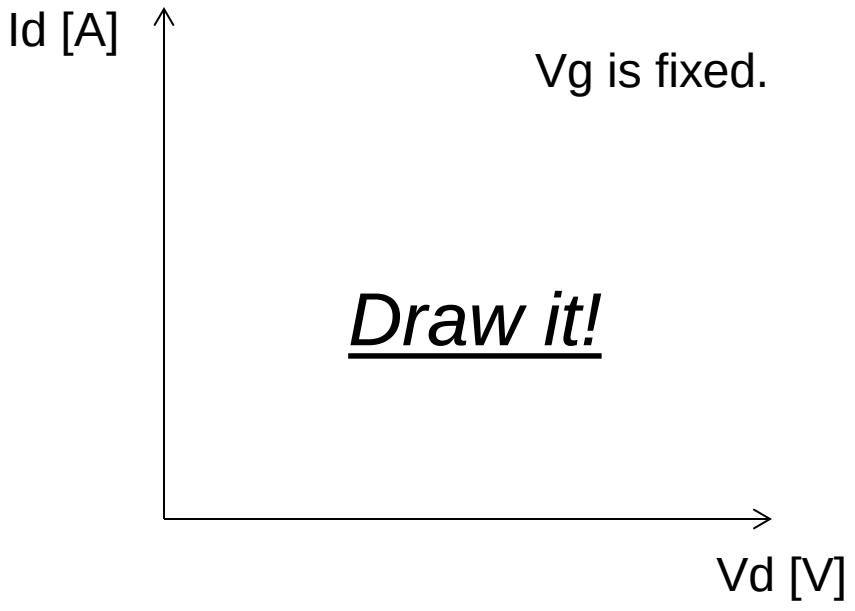
Review (1/2)

- The MOSFET has three terminals.
  - (Low-frequency) gate current is zero. (Isolated by the dielectric material)
  - Source current + drain current = 0
  - Source is connected to the GND.
  - Gate voltage and drain voltage are variables.

Review (2/2)

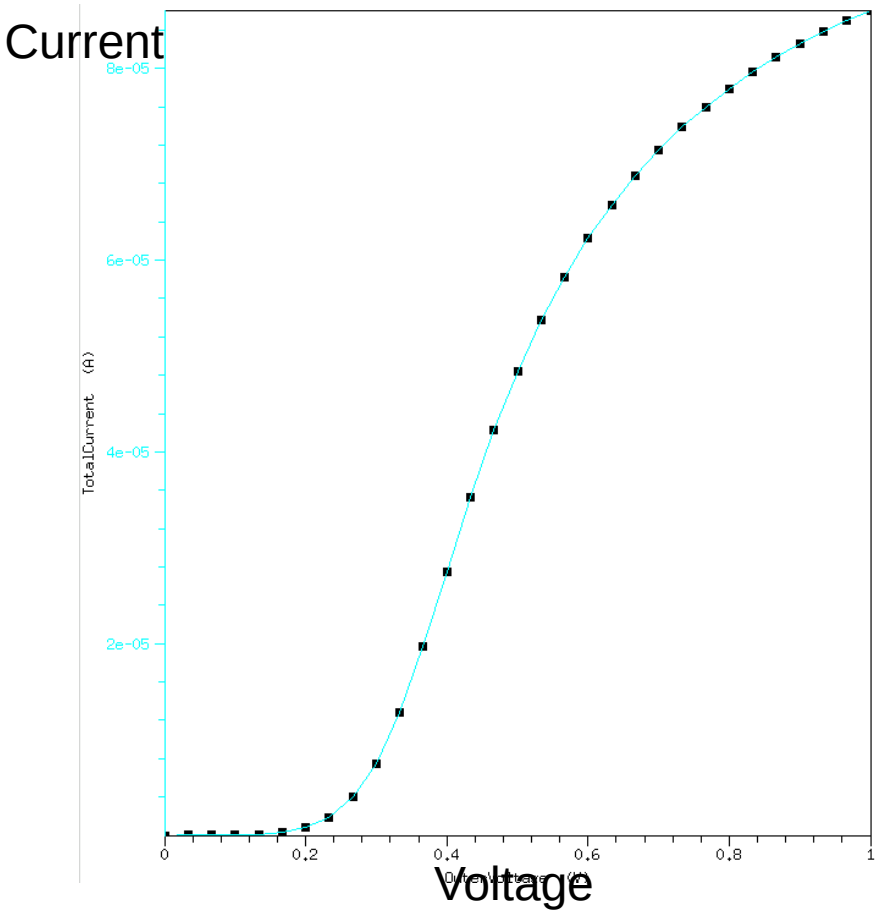
- Typical graphs
  - Id-Vg for given Vd values
  - Id-Vd for given Vg values





Threshold voltage

- Threshold behavior
  - Physical reason? (*See p. 248*)



A door threshold and a dog (Google images)

🡸 A typical Id-Vg curve

Derivation of IV (1/2)

- Drain current
  - First of all, the current is given by

$$I = Q\,v \tag{6.4}$$

  - Here, Q is the charge density *per unit length*.
  - It follows

$$Q = WC_{ox}[V_G - V(x) - V_{TH}] \tag{6.3}$$

  - Also v is the electron velocity.

$$v = -\mu_n E = +\mu_n \frac{dV}{dx} \tag{6.5 and 6.6}$$

  - The drain current is

$$I_D = WC_{ox}[V_G - V(x) - V_{TH}]\mu_n \frac{dV}{dx} \tag{6.7}$$

Derivation of IV (2/2)

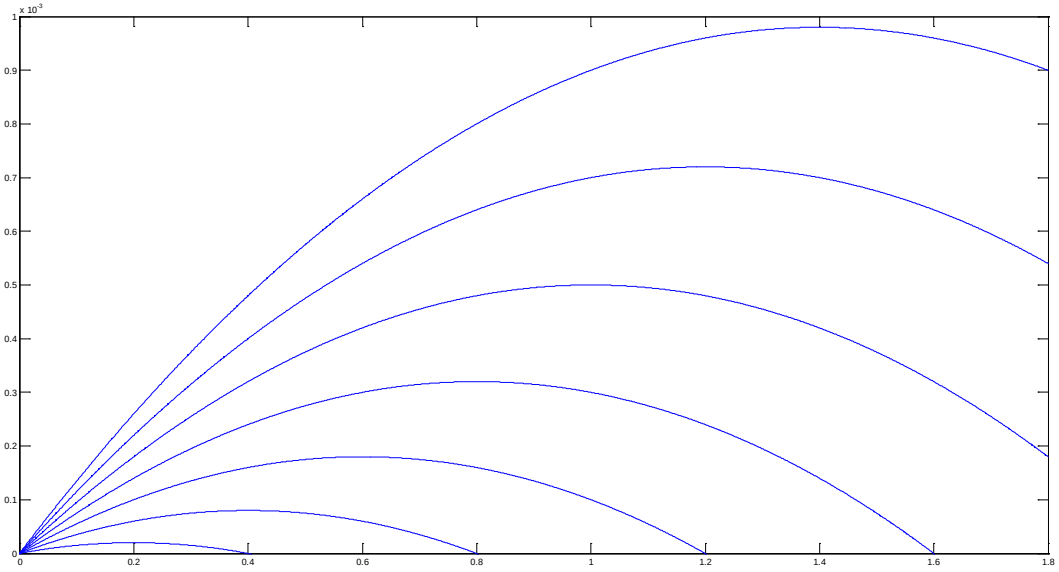
- Integration over the channel
  - Simply re-arranging,

$$I_D dx = \mu_n C_{ox} W [V_G - V(x) - V_{TH}] dV$$

  - When integrated,

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_G - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Current



← Is it acceptable?

Voltage

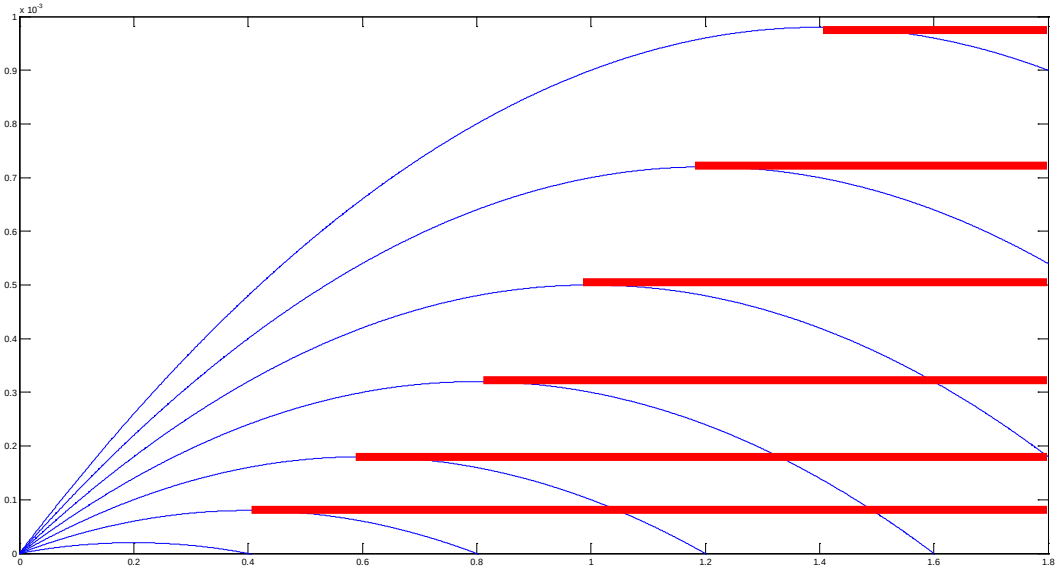
Of course, not!

- Current usually increases as the voltage increases…
- Recall (6.3).

$$Q = WC_{ox}[V_G - V(x) - V_{TH}] \qquad (6.3)$$

  - What happens when $V(x) = V_G - V_{TH}$?
  - "Saturation region"

Current

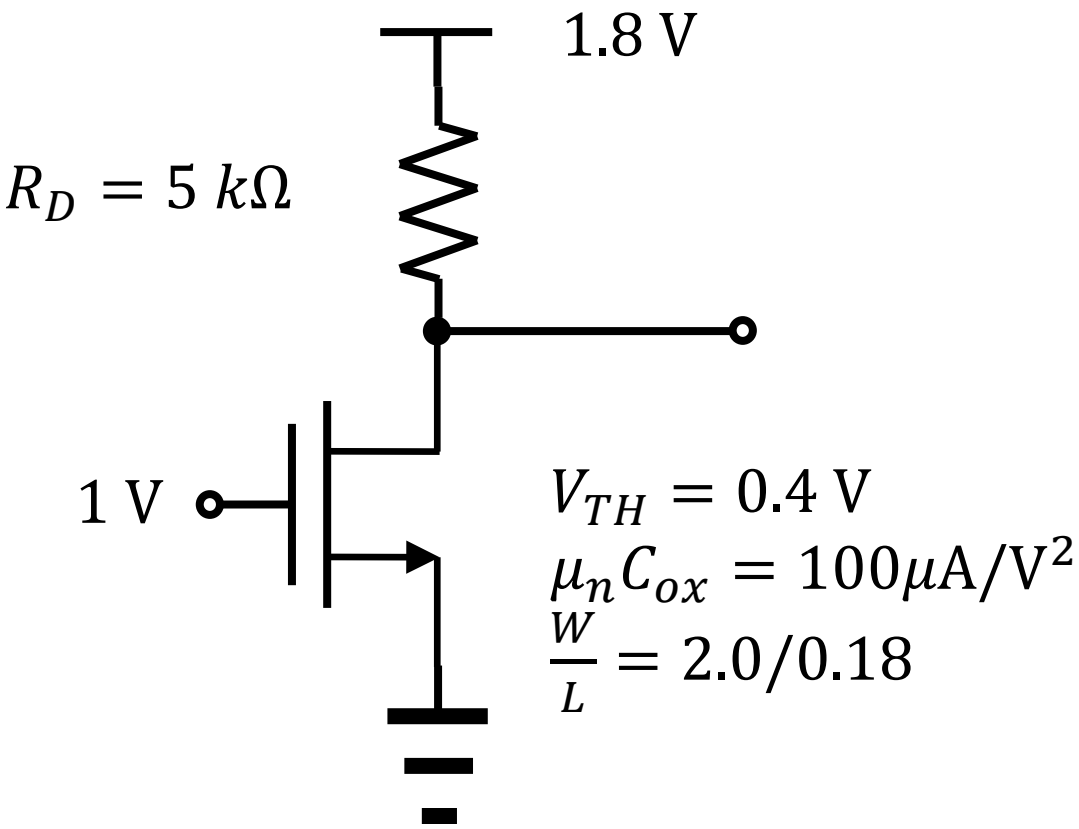


Voltage

🡸 Instead, the current is saturated. (Red lines)

Example 6.6

- Assume the saturation region.
  - Then, the saturation current becomes $200\ \mu\text{A}$.

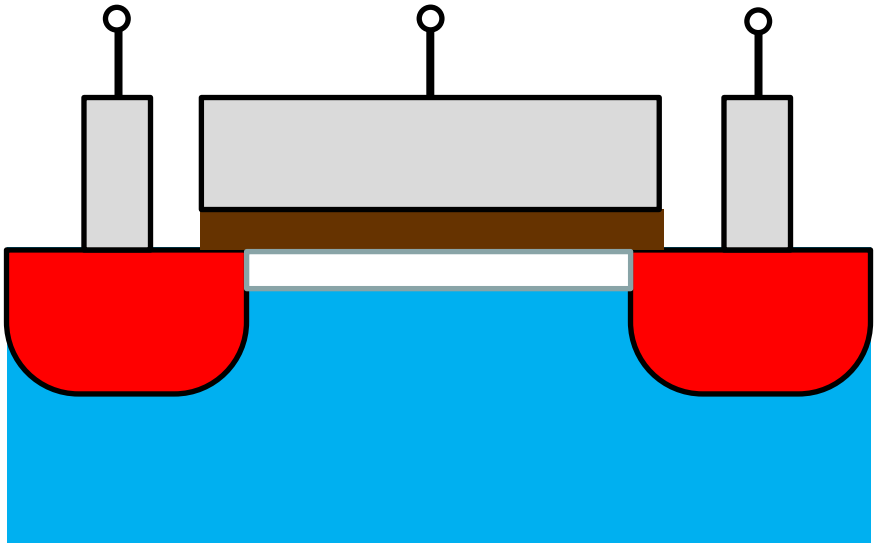


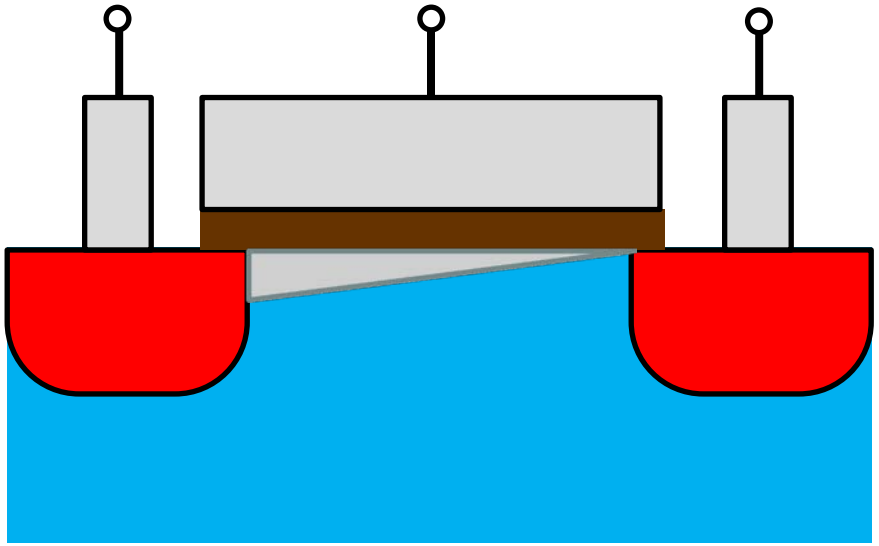
Long vs. short

- Long channel device
  - “Long”?
  - It depends on the situation.
- Short channel device
  - “Short”?
  - Again, it depends on the situation.
- Channel-length modulation
- Velocity saturation
- Body effect

Channel length modulation

- Channel length modulation





- Output resistance?

$$r_O = \frac{\Delta V_{DS}}{\Delta I_D}$$

MOS transconductance

- "conductance" of a simple resistor
  - It means $\frac{I}{V}$.
- "trans" + "conductance"
  - Between different terminals

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{6.44}$$

  - For the saturation region,

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

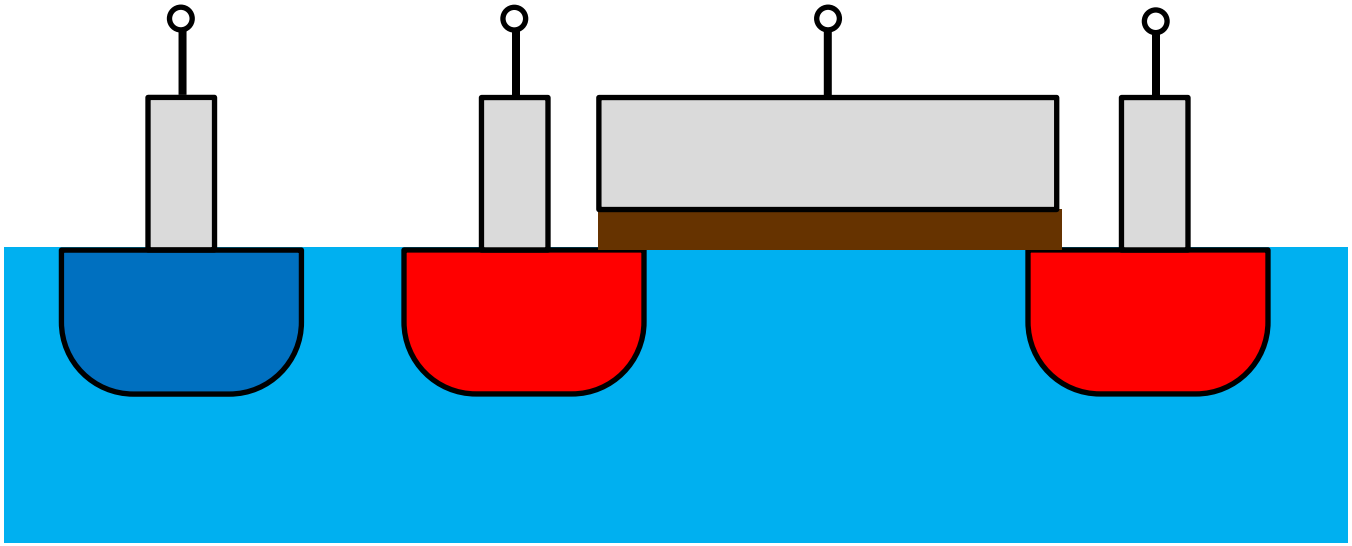
← Why?

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

Body effect

- Actually, a MOSFET is a four-terminal device.
  - Substrate (or bulk)
  - Threshold voltage, V_{TH}, varies. (In which direction?)



Two more issues

- Velocity saturation
  - Once again, the current is given by

$$I = Q\ v \tag{6.4}$$

  - How did we have the saturation?

- Subthreshold conduction
  - Although not covered, it's the critical issue!

Summary

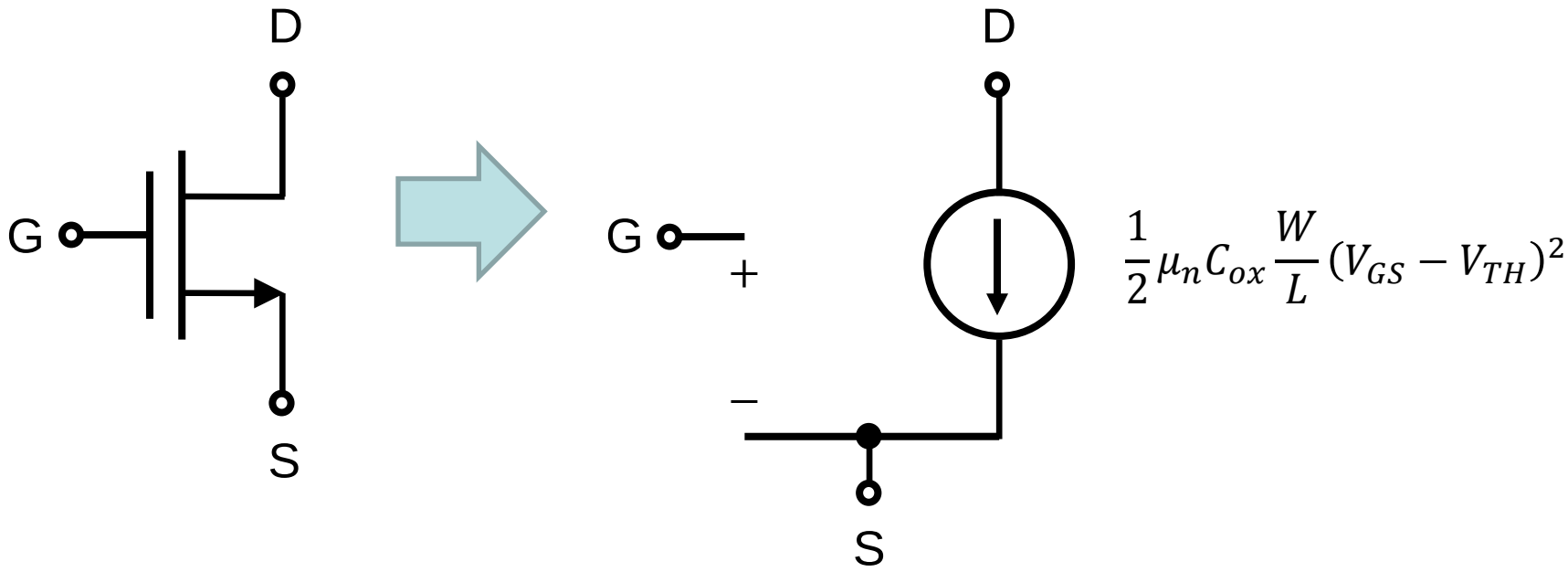
- MOS structure
  - Two different mechanisms to provide negative charges
  - Threshold voltage
  - Once the MOS is inverted, it is a capacitor.
- MOS IV
  - Current as a product of density and velocity
  - Triode region and saturation region
  - Concept of transconductance
  - Channel length modulation
  - Body effect
  - Velocity saturation
  - Subthreshold swing

Large-signal model (1/2)

- Saturation region

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

  - Drain current is determined by gate voltage. (*voltage-controlled current source*)
  - *Channel-length modulation?*

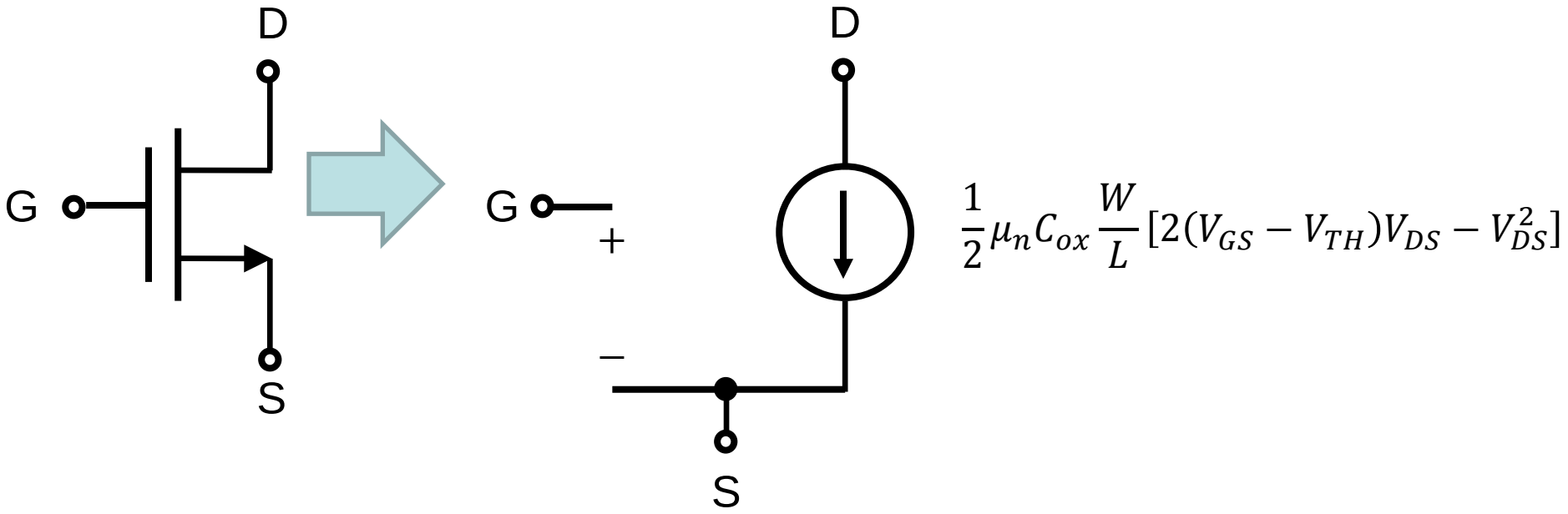


Large-signal model (2/2)

- Triode region

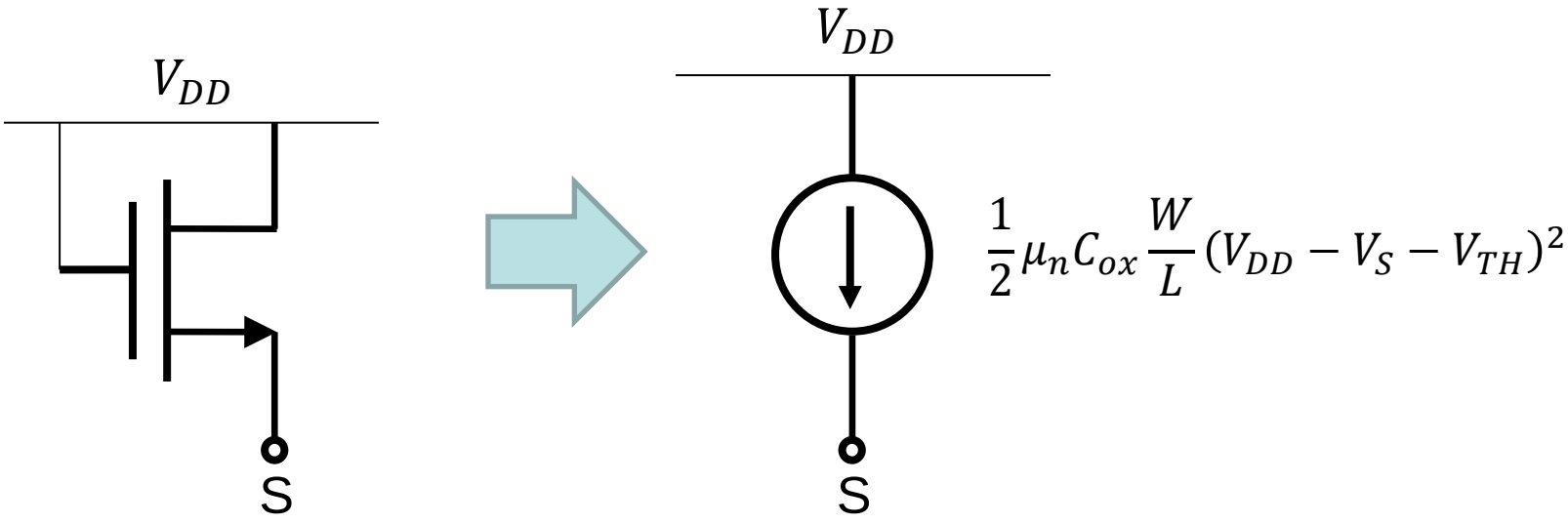
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$$

  - Still, it can be described by a *voltage-controlled current source*.



Example 6.13

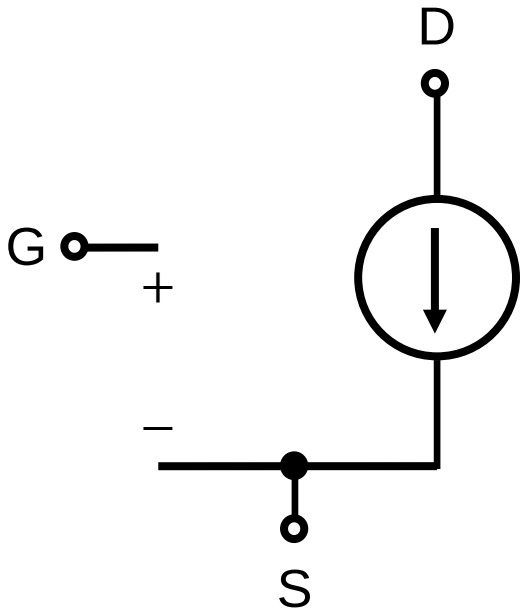
- Always in the saturation region!
  - Any necessary condition?

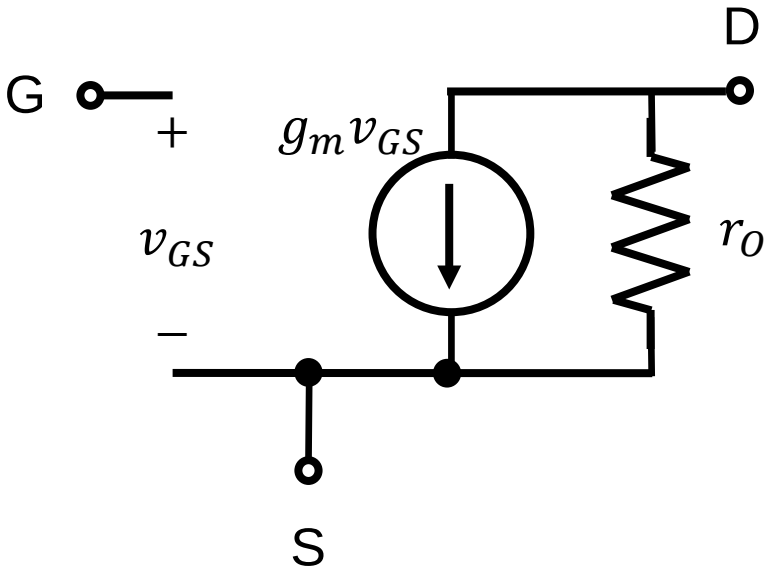


Gate and drain are tied.
They are connected to V_{DD}.

Small-signal model

- The large-signal model is complete (within its accuracy limitation).
  - But, for small-signal analysis, it is convenient to have the small-signal model.



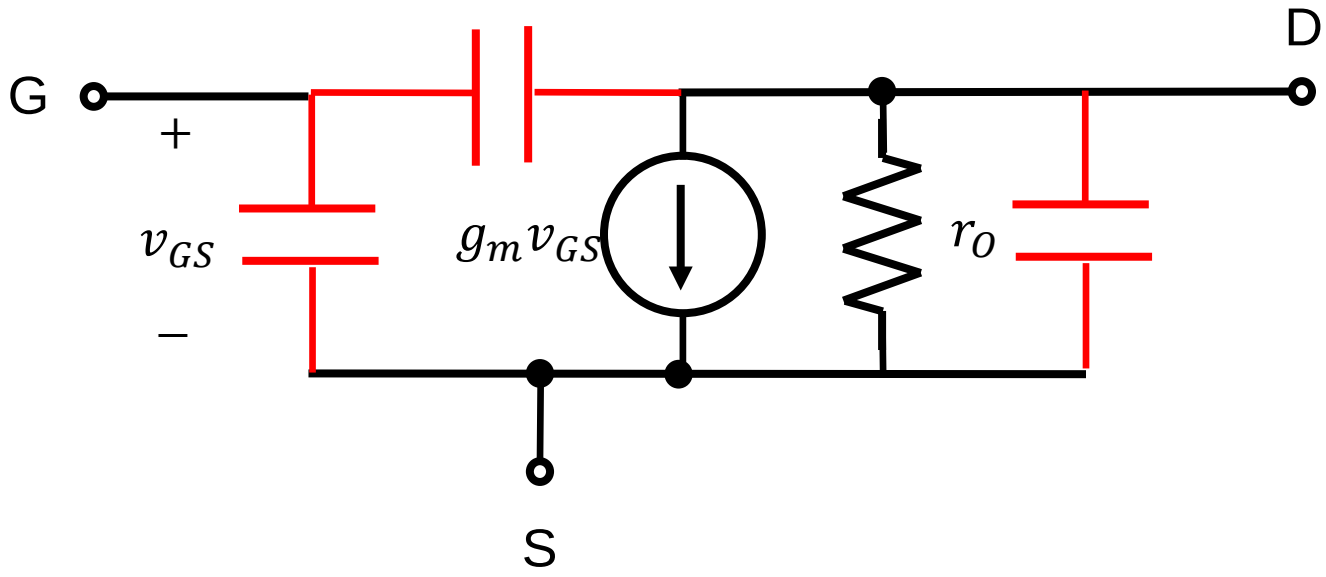


$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

What is g_m and r_O?

Time-dependent one?

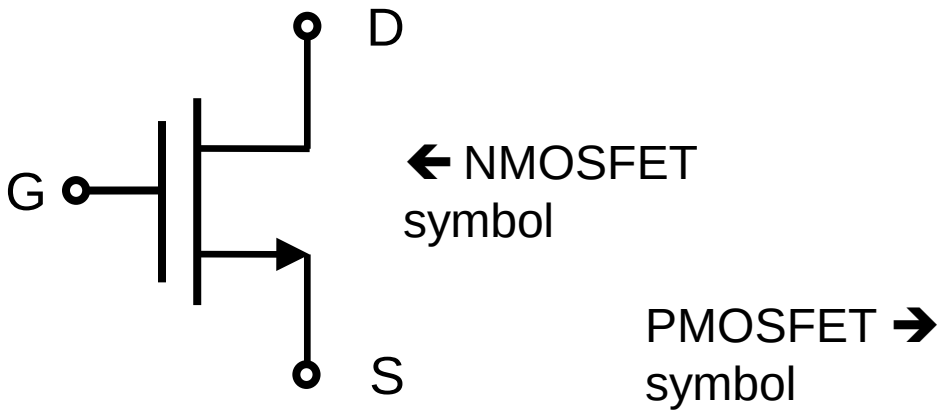
- Everything was in the dc steady-state…
  - How about the frequency-dependent case?
  - Capacitive components can be seen.
  - *Their physical origin?*

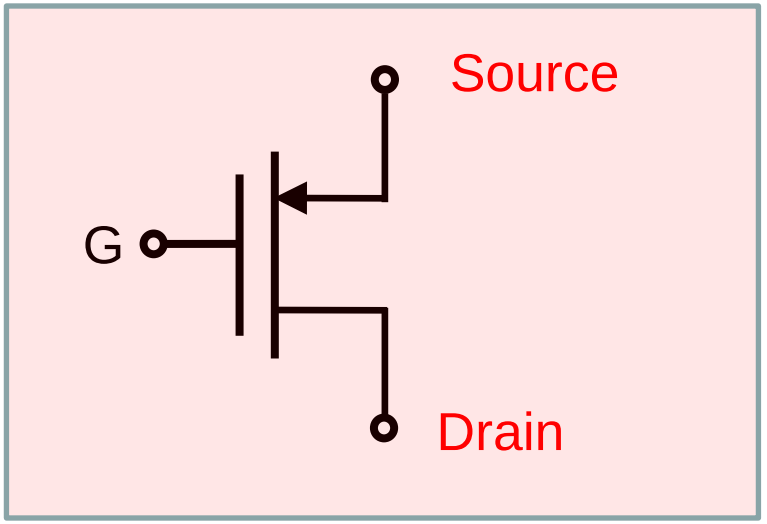


High-frequency, equivalent-circuit model for the case in which the source is connected to the substrate

CMOS

- 9's complementary of 123?
  - 876
- Complementary MOS
  - Here we have an NMOSFET.
  - A device where the transport is dominated by holes





- Why is it important?