Lecture6: MOSFET, its structure and history

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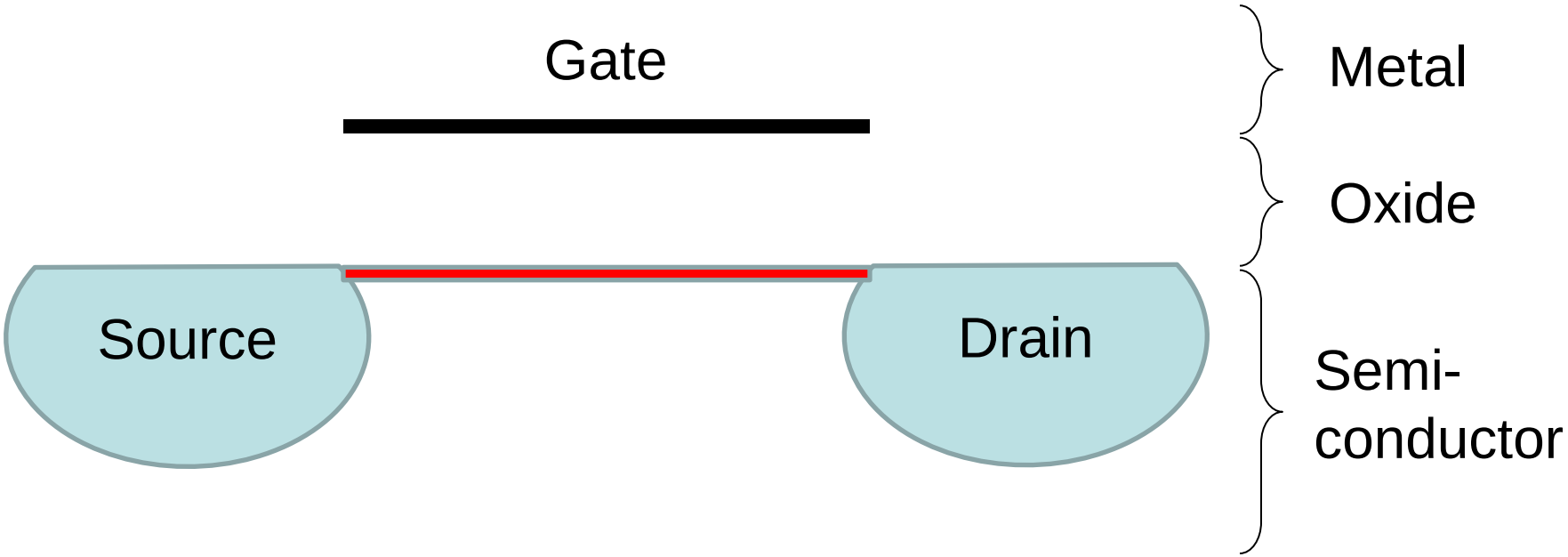
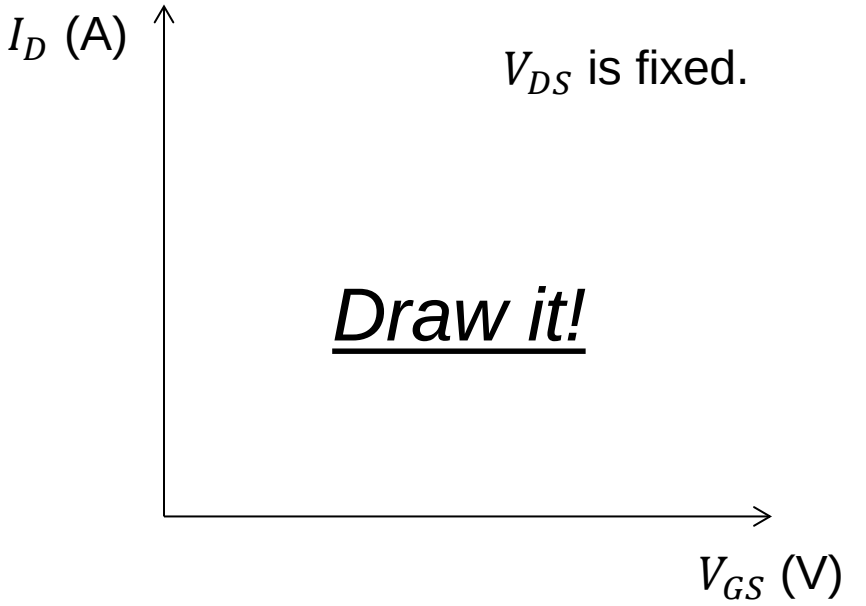
MOSFET

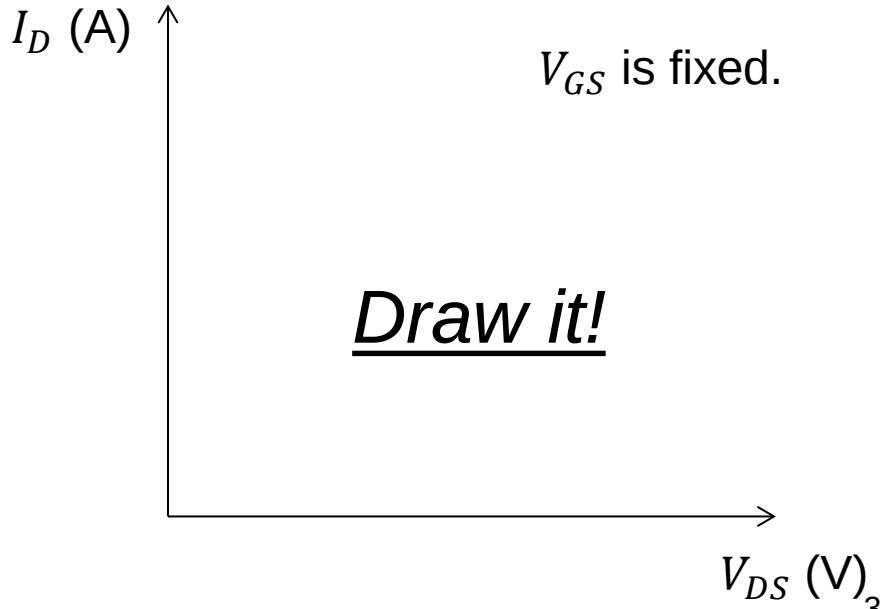
- Metal-Oxide-Semiconductor Field Effect Transistor
- Vertical structure
  - Metal-Oxide-Semiconductor
- Terminals
  - Gate, Source, Drain, (and substrate)



Its operation

- The MOSFET has three terminals.
  - At low frequencies, the gate current is zero.
  - Source current + drain current = 0, $I_S + I_D = 0$
  - Source is connected to the GND.
  - Gate voltage (V_{GS}) and drain voltage (V_{DS}) are variables.





Recent history

- If not stated otherwise, the figures are taken from…
  - M. Bohr, International Electron Device Meeting (IEDM) 2011
  - Other Intel's IEDM (or VLSI) papers

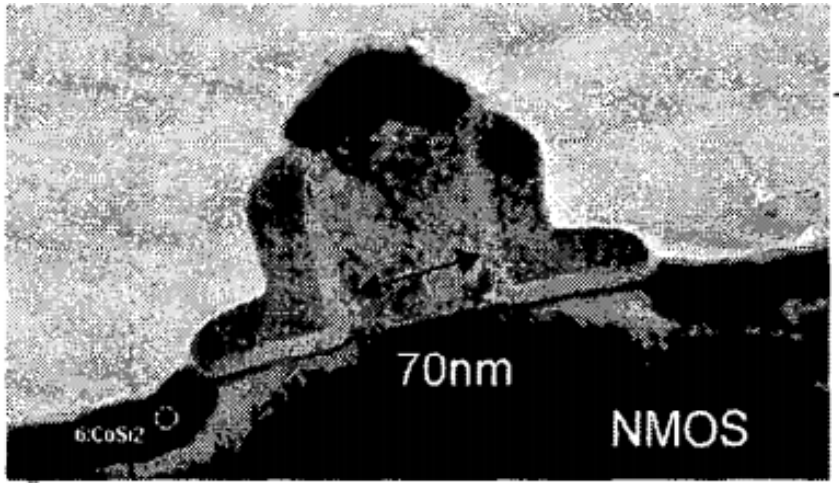
- It's a "logic-centric" history
  - Memory devices have their own history.
  - Two representative memory devices are:
  - DRAM
  - NAND

Chronicles

- IEDM papers presented by Intel
  - 130nm: 2000
  - 90nm: 2003
  - 65nm: 2004
  - 45nm: 2007
  - 32nm: 2008
  - 22nm: 2012 (VLSI, not IEDM) (FinFET)
  - 14nm: 2014
  - 10nm: 2017 (IEDM)
  - 7nm: 2017 (VLSI, not IEDM) (Nanowire) (IBM-Samsung-Global Foundries, not Intel)

Prehistoric(?) MOSFET

- 130-nm MOSFET
  - Major issue: Cu interconnection (Previously, Al)
  - Operation voltage: 1.3 V
  - Oxide thickness: 1.5 nm
  - Poly-silicon gate

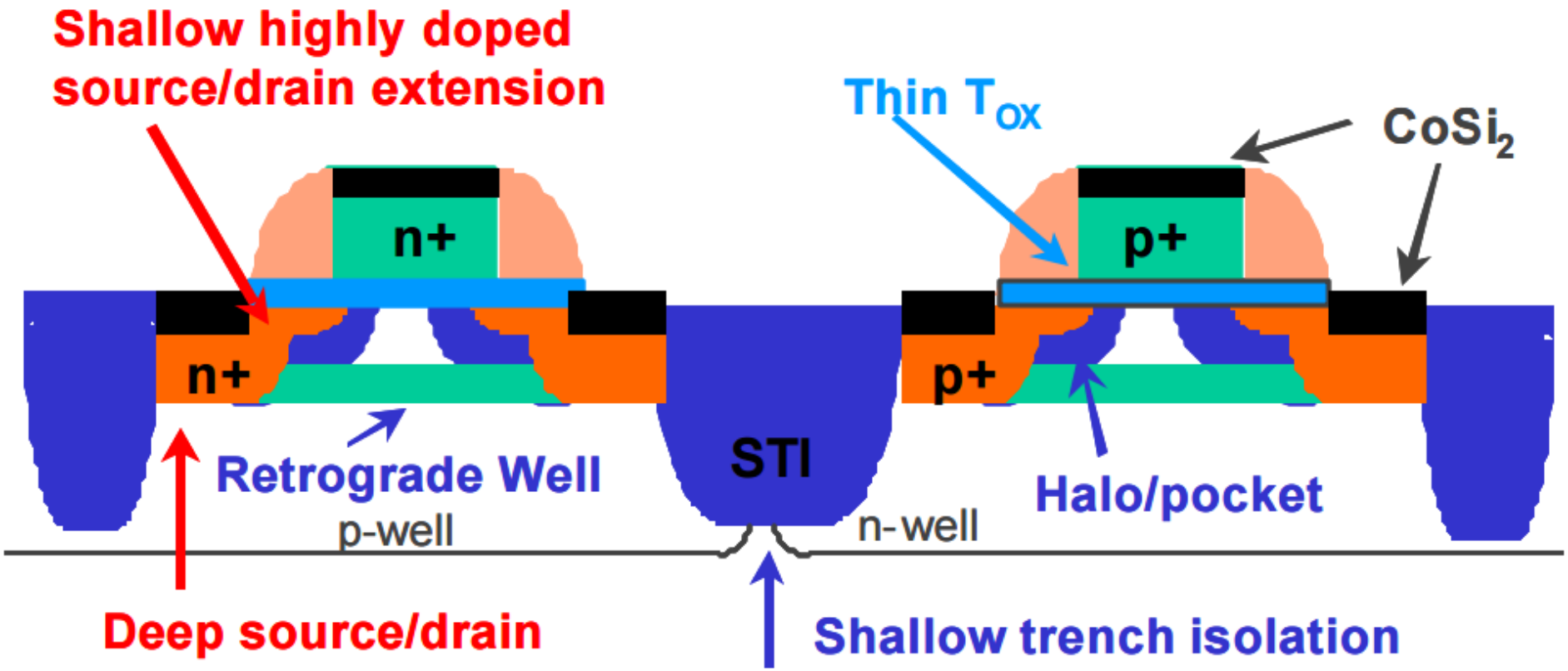


SUMMARY OF TRANSISTOR CHARACTERISTICS

Parameter		180 nm Generation [1]	This Work
V_{DD}	[V]	1.5	1.3
L_{GATE}	[nm]	130	70
T_{OX}	[nm]	2.0	1.5
I_{OFF}	[nA/μm]	3	10
I_{DSAT}(n)	[mA/μm]	1.04	1.02
I_{DSAT} (p)	[mA/μm]	0.46	0.5
Low Vt I_{OFF}	[nA/μm]	-	100
Low Vt I_{DSAT}(n)	[mA/μm]	-	1.17
Low Vt I_{DSAT} (p)	[mA/μm]	-	0.6

Cross-section drawing

- Many features…



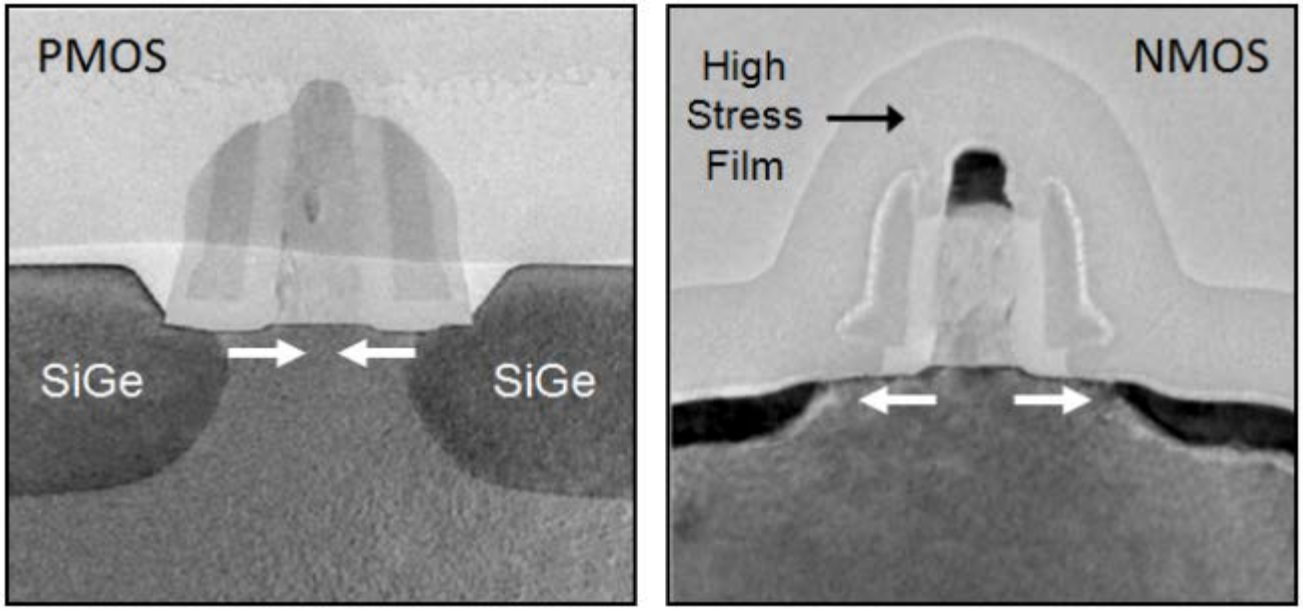
(www.intel.com)

Leakage problem

- Why?
  - The SiO_2 gate oxide had scaled to ~1.2 nm at the 90 nm generation. ➔ The gate oxide leakage was increasing exponentially and had become a noticeable percentage of total chip power.
  - Deceasing supply voltage ➔ decreasing threshold voltage ➔ ever-higher subthreshold leakage current
- Increasing transistor leakage
  - Was against the market preferences.
  - The 1980s and 1990s were the era of the home PC.
  - The 2000s was the “mobile” era.

90-nm node

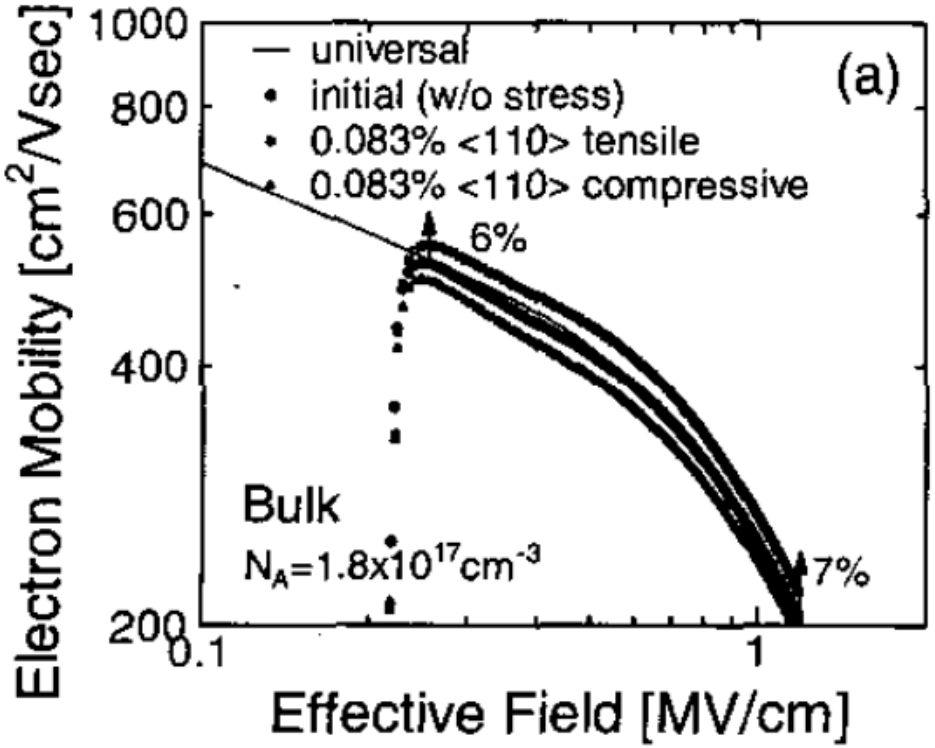
- Oxide thickness: 1.2nm ($\times$ 0.8 scaling, not $\times$ 0.7)
  - SiGe was selectively deposited in PMOS source-drain regions to provide compressive channel strain.
  - A tensile SiN cap layer was deposited over NMOS transistors to provide tensile channel strain.

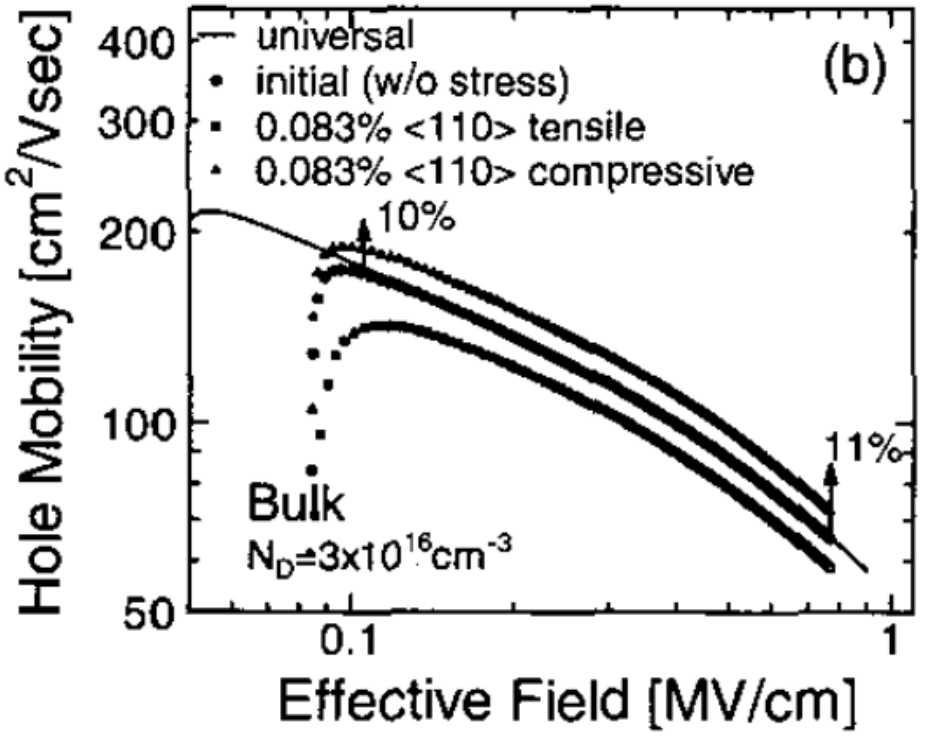


90nm uniaxial strained silicon transistors

Its impact

- Mobility enhancement
  - For electrons, tensile strain
  - For holes, compressive strain

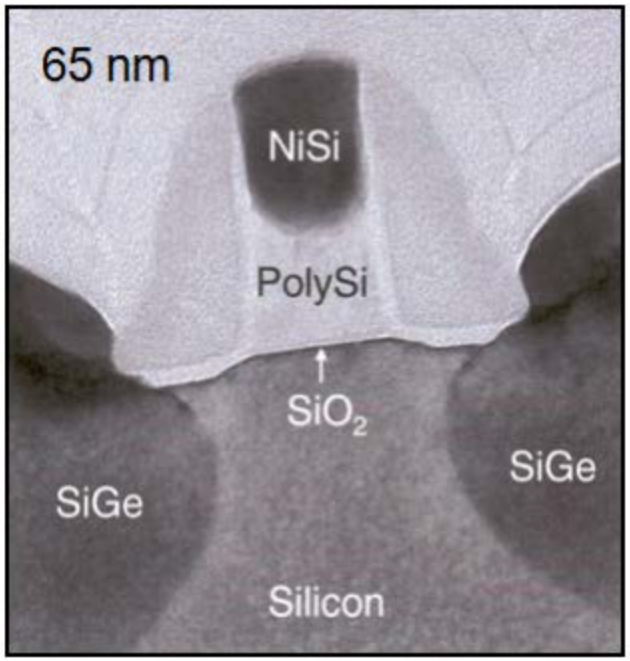


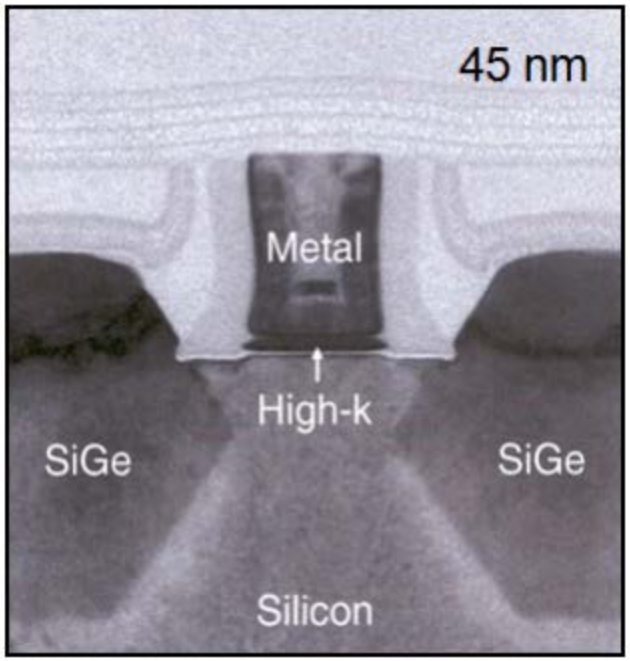


Mobility characteristics under <110> uniaxial strain (K. Uchida, IEDM 2004)

“High-k + metal” gate

- We need to scale the “effective” oxide thickness.
  - Keeping the physical thickness
  - Increasing the oxide capacitance
- Poly depletion effect is now removed.



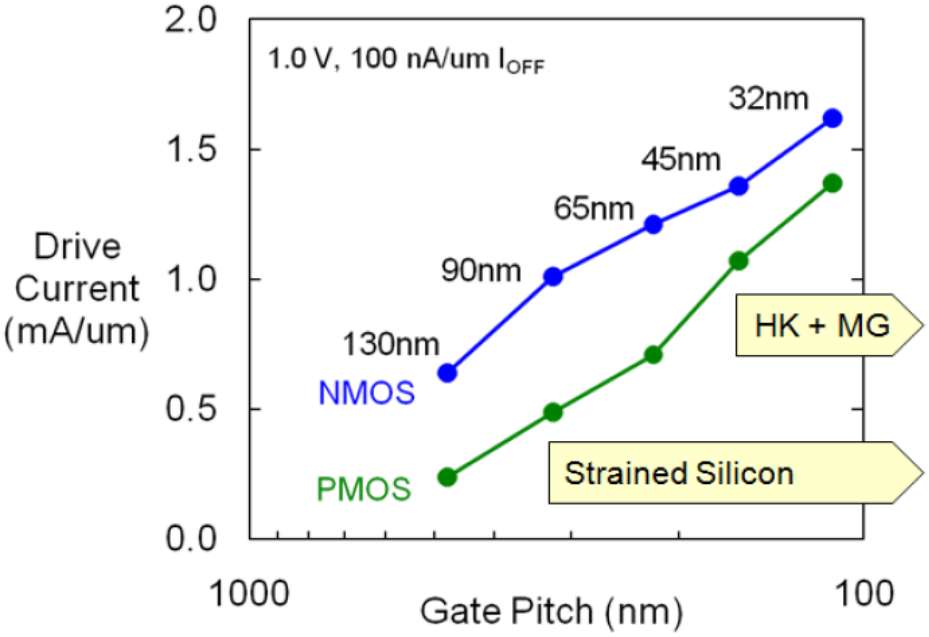


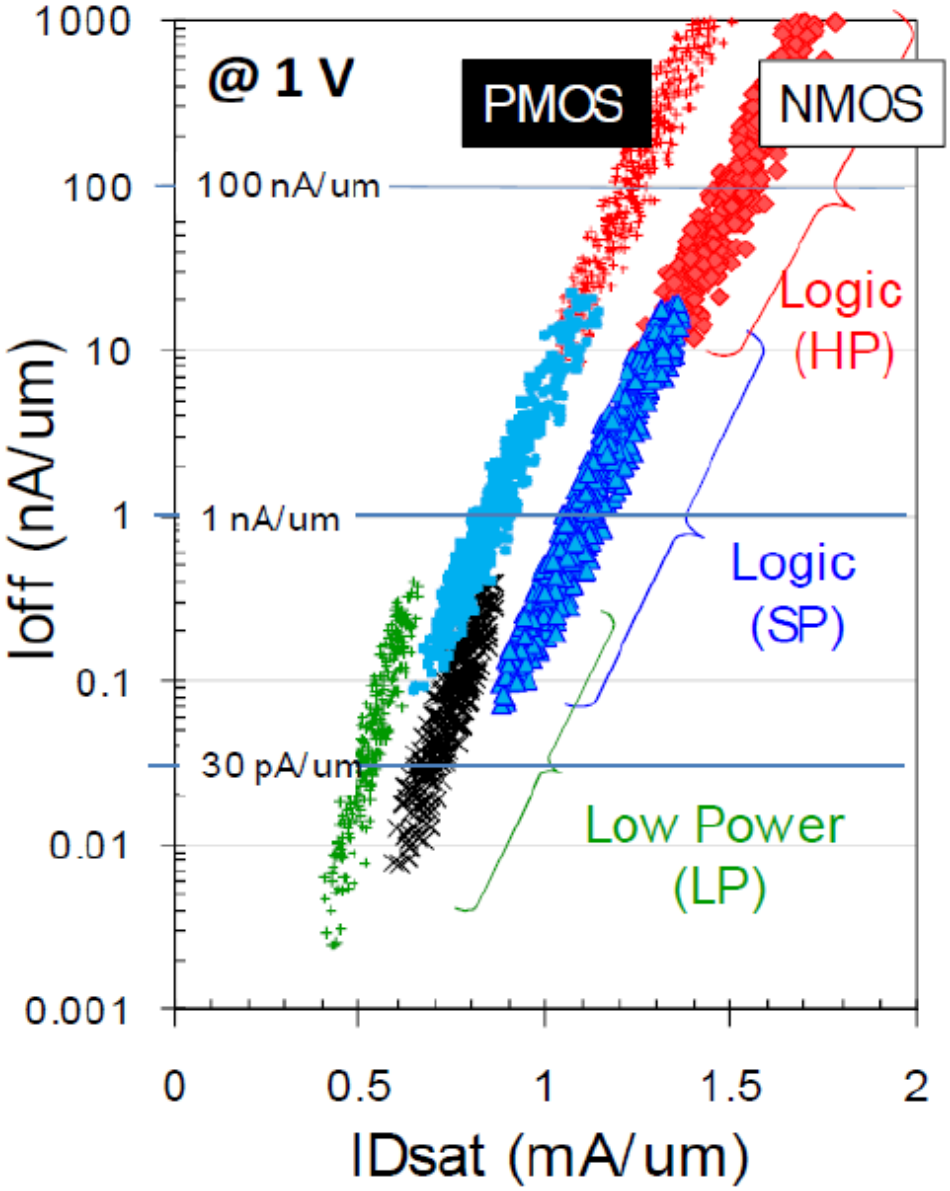
65nm

45nm high-k metal gate transistor

Performance

- Drive current improvement
  - Strain engineering
  - High-k + metal gate

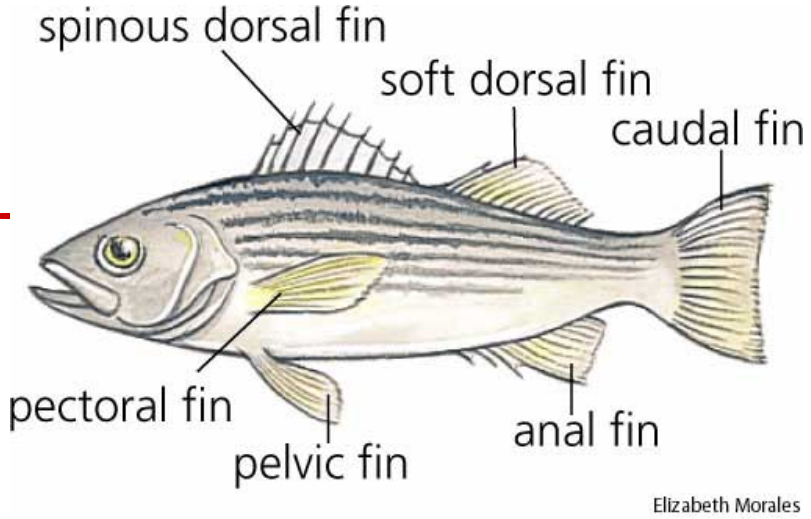




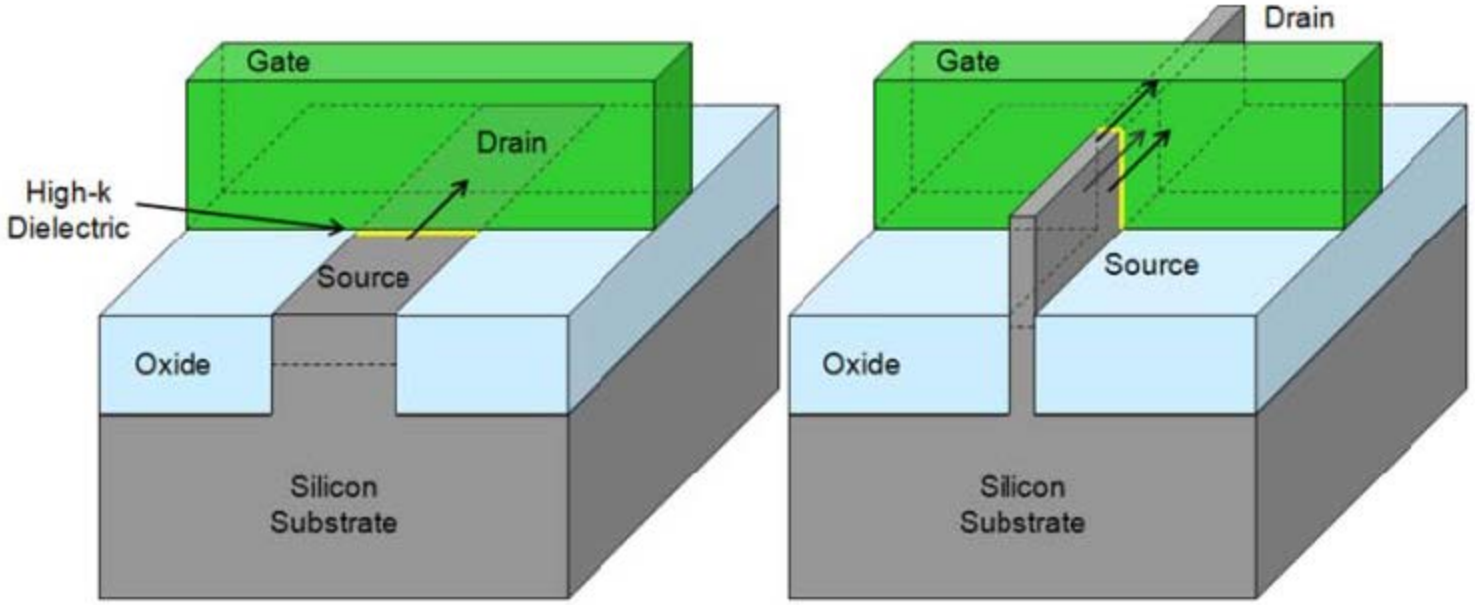
32nm transistor performance and leakage options

FinFET

- FinFET
  - So named after its shape
  - Initially proposed as a SOI FinFET
  - Later, a bulk FinFET



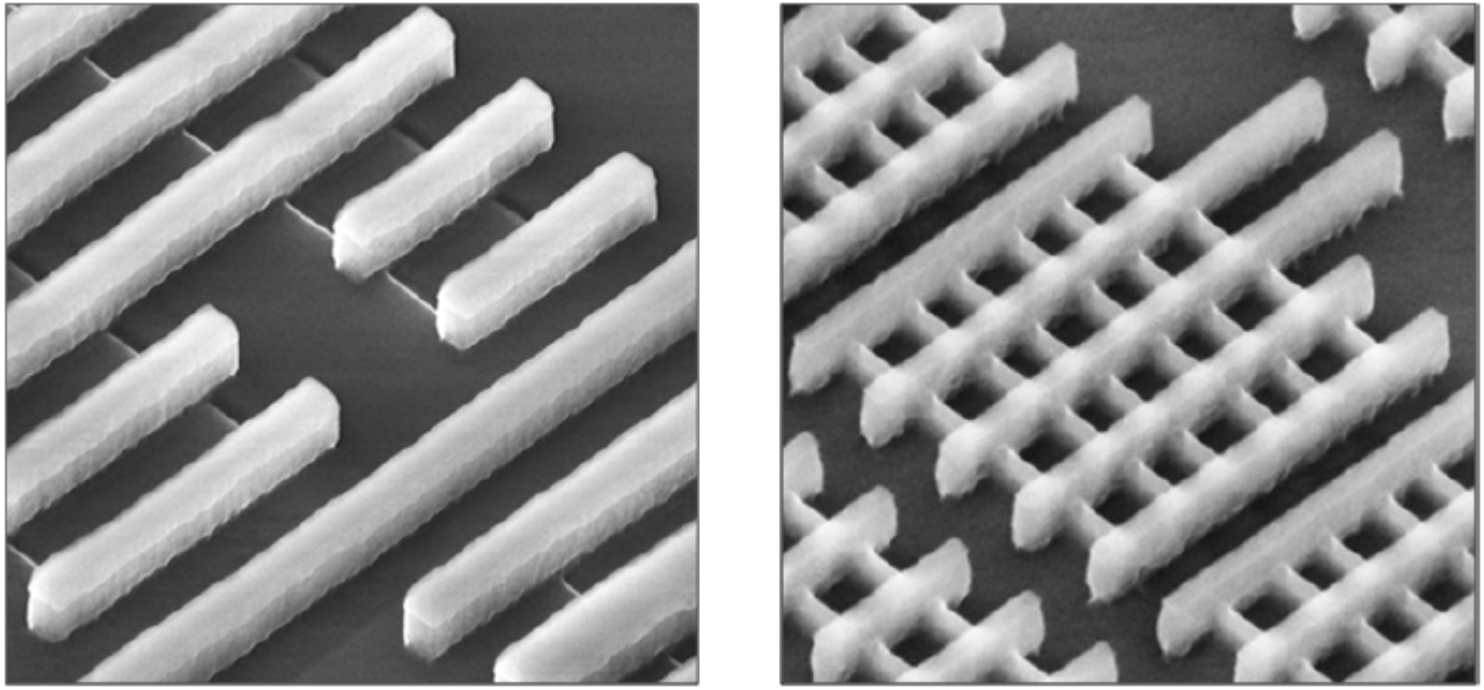
Fins (Google images)



Planar transistor structure (left) and FinFET structure (right)

SEM image

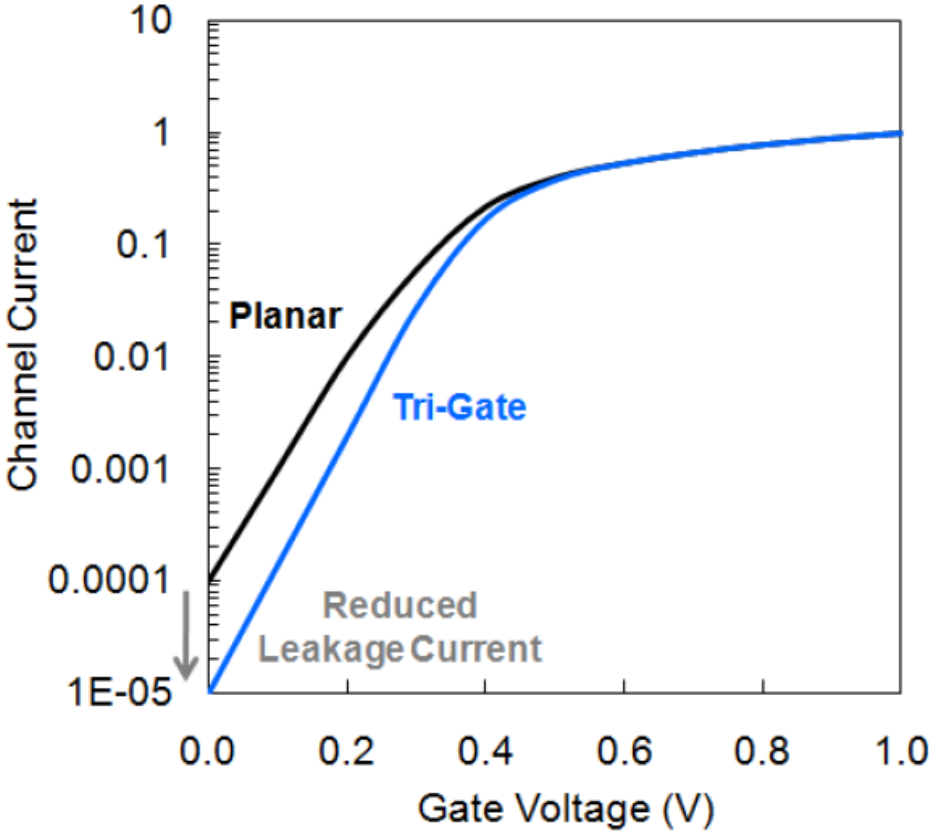
- FinFET
  - Improved electrostatic control of the channel region

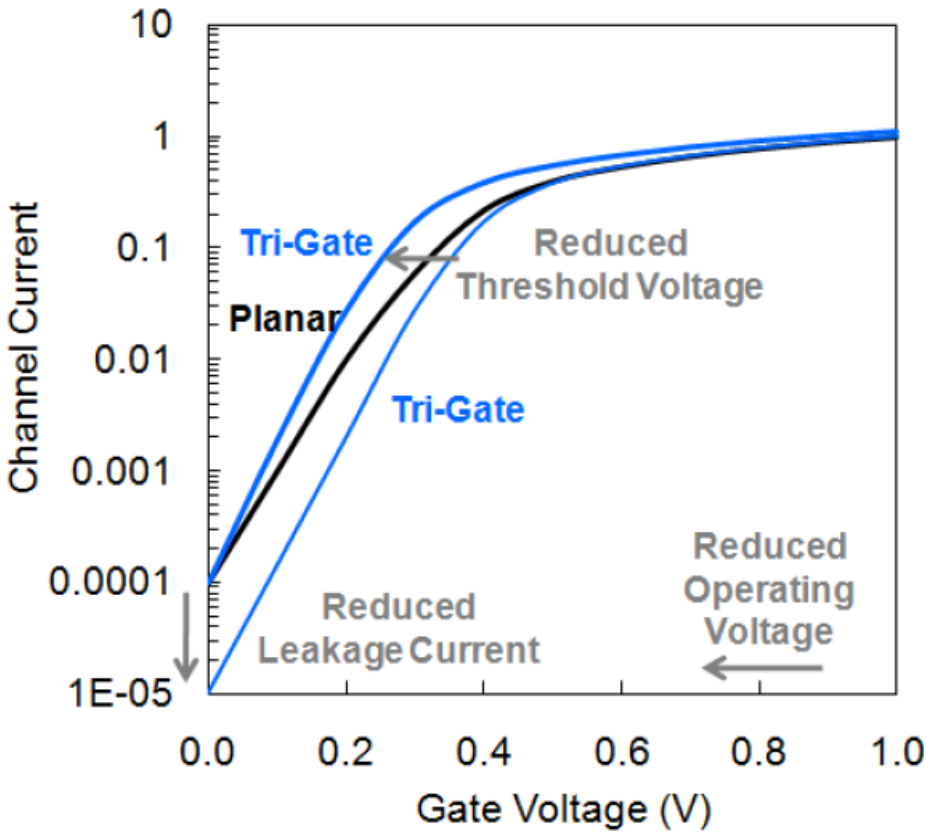


32nm planar transistors (left) and 22nm FinFETs (right)

Performance

- Steeper sub-threshold slope
  - $\times 10$ off-state leakage reduction

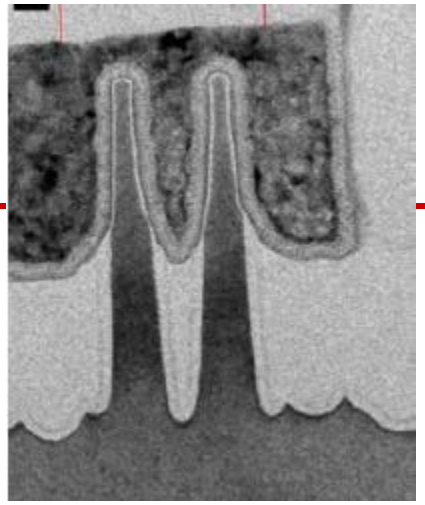


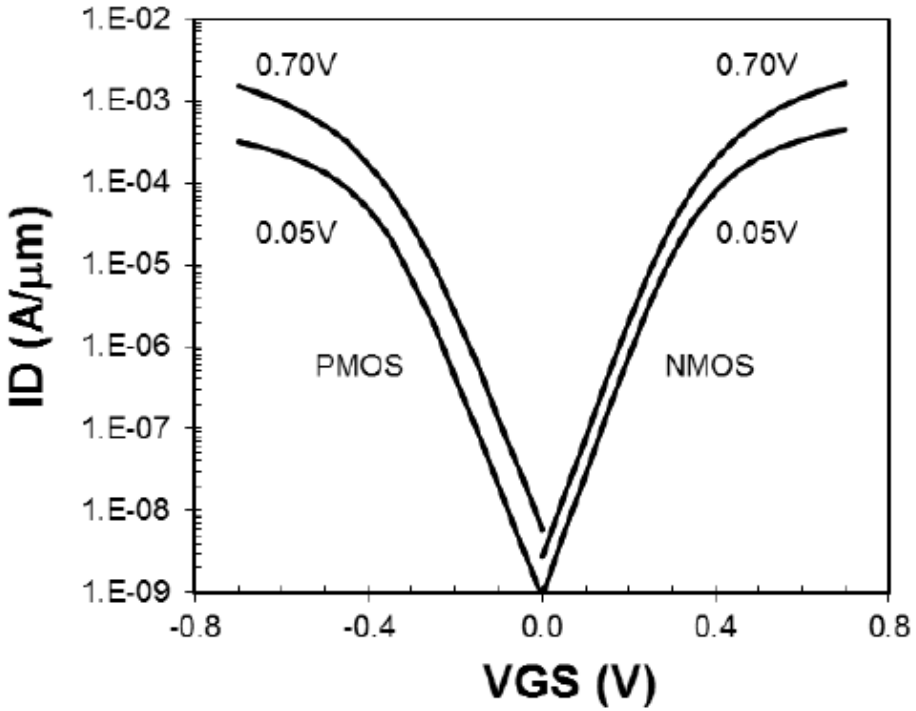


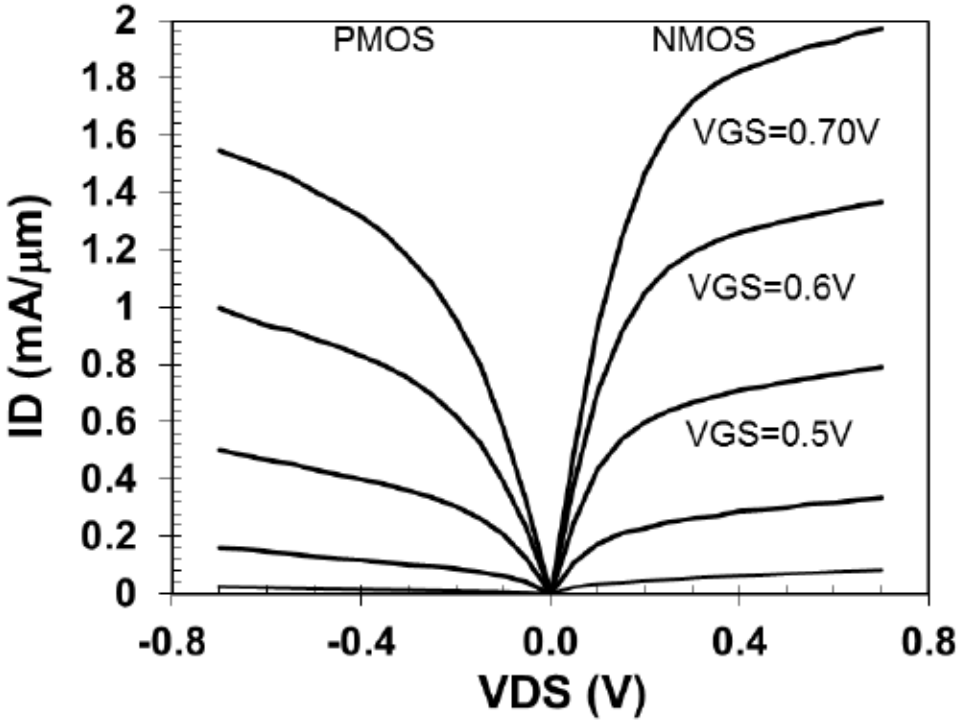
Transistor IV characteristics

IEDM 2017

- State-of-the-art FinFET technology







Nanosheet

- Proposed as an viable option at 5nm node and beyond
  - Gate-All-Around (GAA) transistor

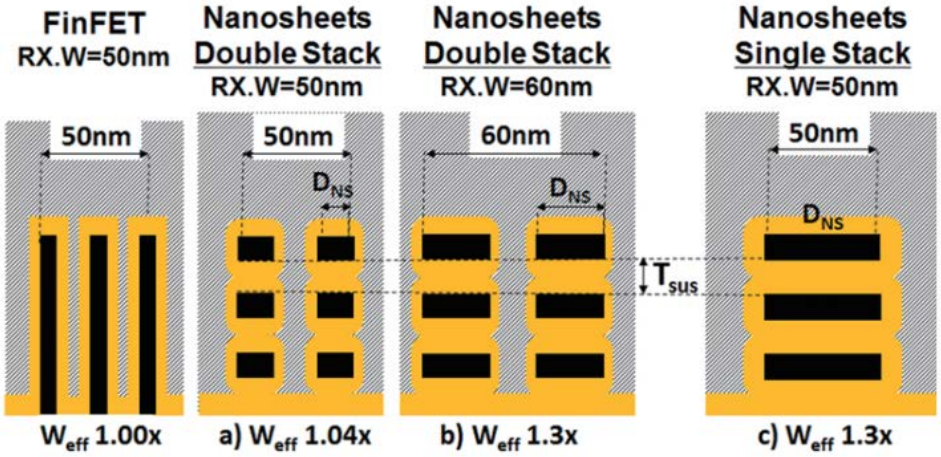


Fig. 2: Increase in W_{eff} going from aggressively scaled FinFET to double and single stack Nanosheets structures. Best improvement is obtained using a single wide Nanosheet stack at constant active width (RX.W).