

---

# Final examination

Sung-Min Hong ([smhong@gist.ac.kr](mailto:smhong@gist.ac.kr))

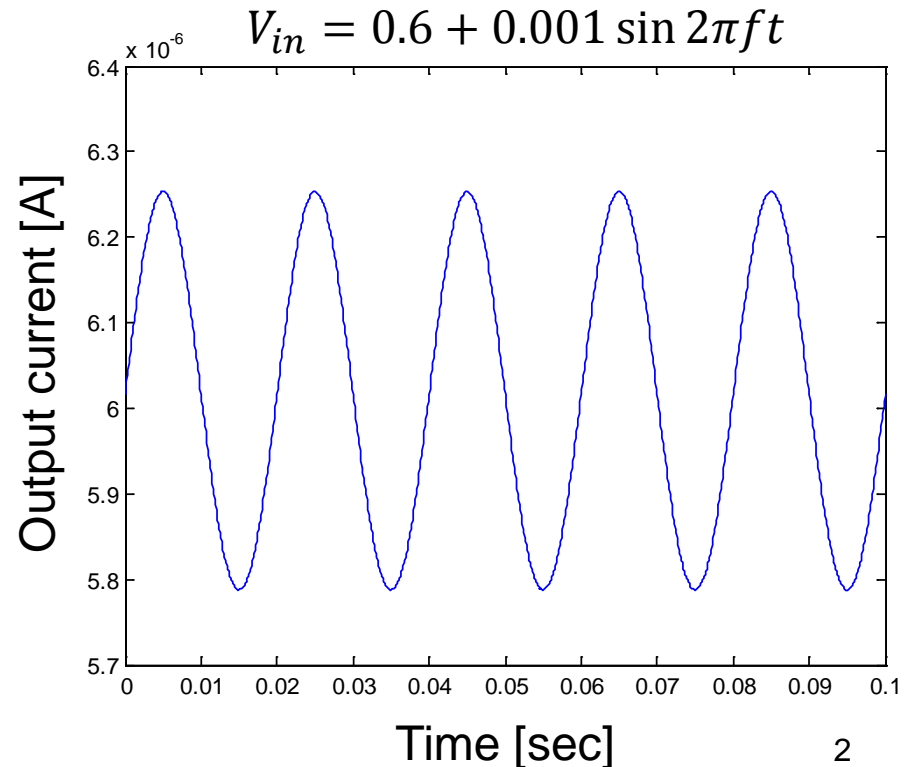
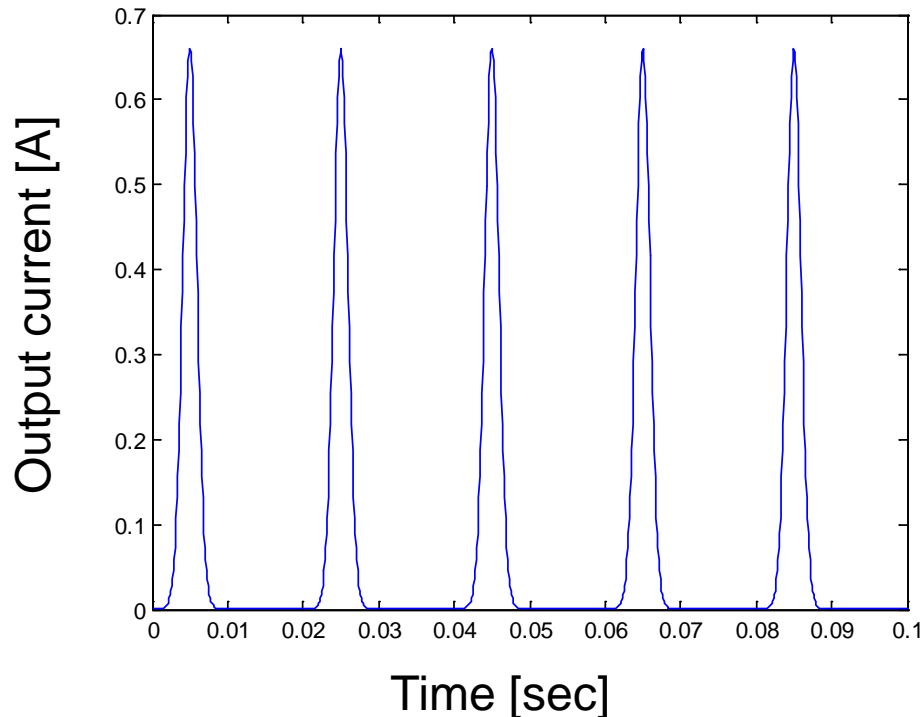
Semiconductor Device Simulation Lab.  
School of Electrical Engineering and Computer Science  
Gwangju Institute of Science and Technology

# Problem1

---

- A nonlinear system,  $I_{out} = I_s \exp \frac{V_{in}}{V_T}$ , is considered.
  - Two cases (0.3 V swing and 1 mV swing) are shown below.
  - Describe those output currents in the frequency domain.

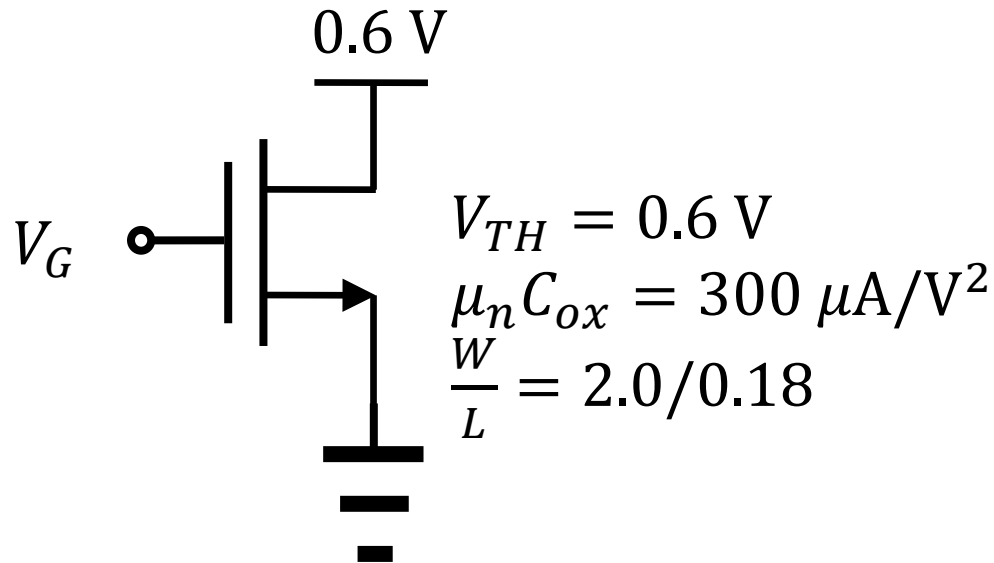
$$V_{in} = 0.6 + 0.3 \sin 2\pi f t$$



# Problem2

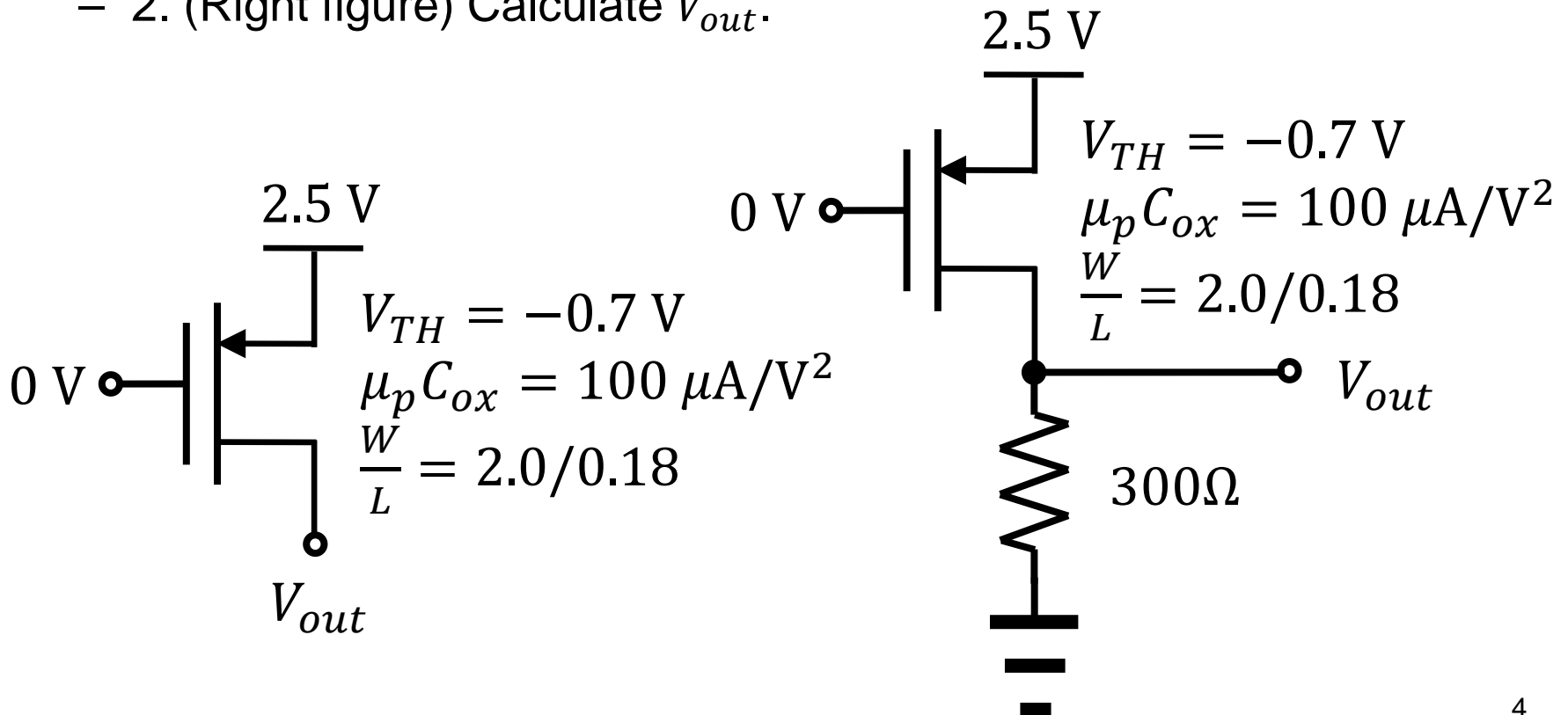
---

- Consider a NMOSFET.
  - Neglect the channel length modulation.
  - 1. Draw its transconductance up to  $V_{GS} = 1.8$  V. Use the IV model studied in the class room.
  - 2. The above answer is not fully consistent with the realistic results. Especially, it goes wrong for high  $V_{GS}$  values. Explain why.



# Problem3

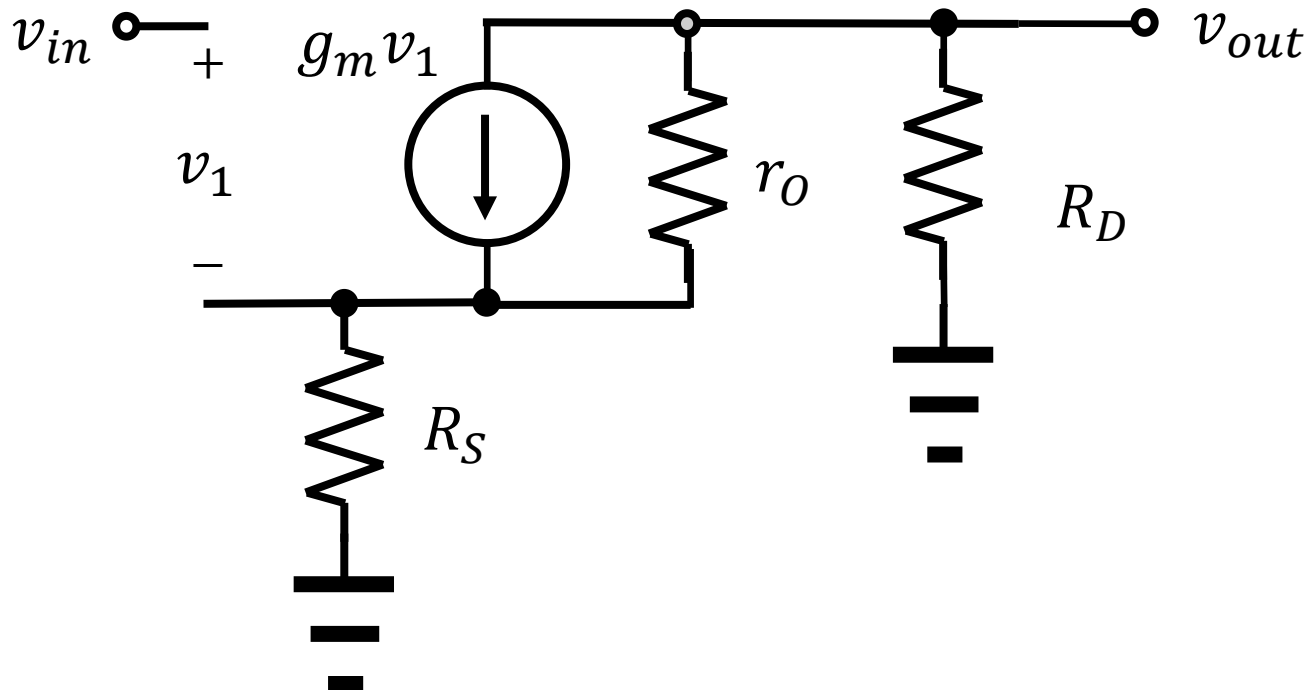
- Consider the following circuit. (Neglect the channel length modulation.)
  - 1. (Left figure) Draw the source current as a function of  $V_{out}$ .
  - 2. (Right figure) Calculate  $V_{out}$ .



# Problem4

---

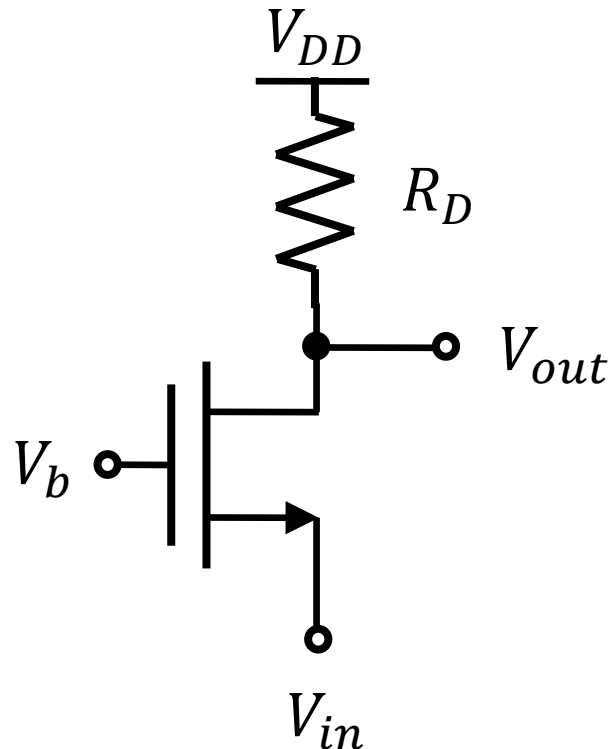
- A small-signal model of the source-degenerated CS amplifier is shown.
  - Derive the voltage gain with the channel length modulation.
  - (If it is difficult, you may try without the channel length modulation for partial credit.)



# Problem5

---

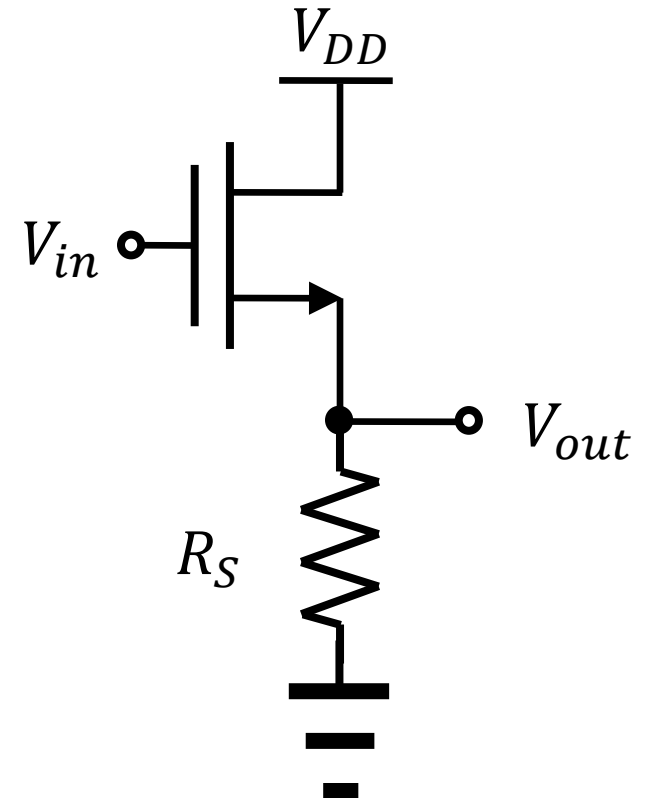
- Consider a common-gate amplifier.
  - 1. Calculate the input impedance, when the channel length modulation is neglected.
  - 2. Repeat again with the channel length modulation.



# Problem6

---

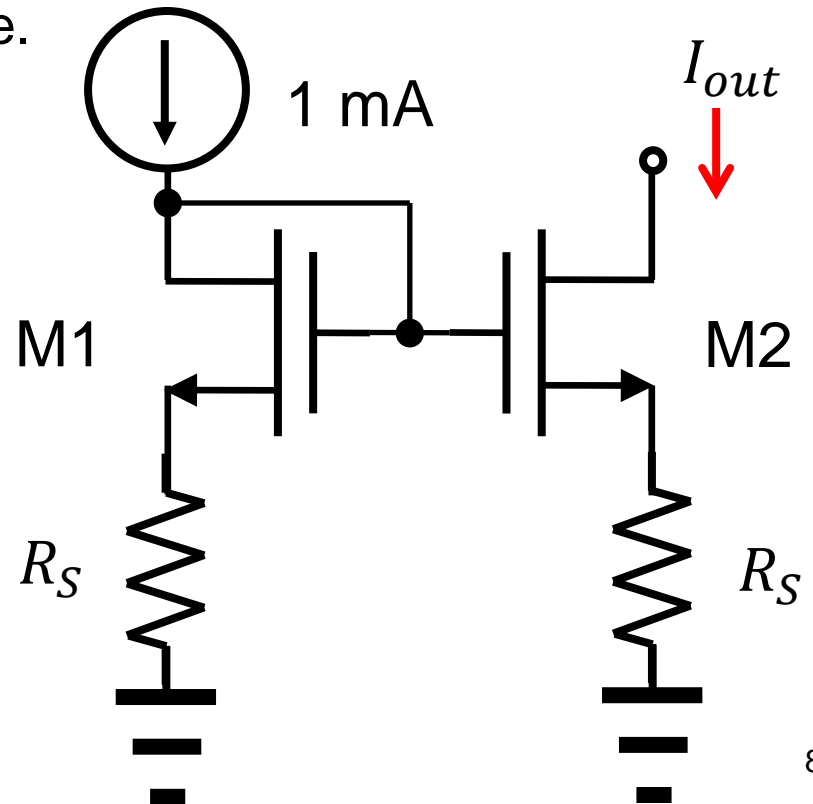
- A source follower is shown.
  - Consider the channel length modulation.
  - 1. Calculate the voltage gain.
  - 2. Calculate the output resistance.



# Problem7

---

- Consider the following circuit.
  - Two transistors, M1 and M2, are identical.
  - 1. What is the output current, approximately? (Assume that M2 is in the saturation mode.)
  - 2. Express the output impedance.





# Problem8

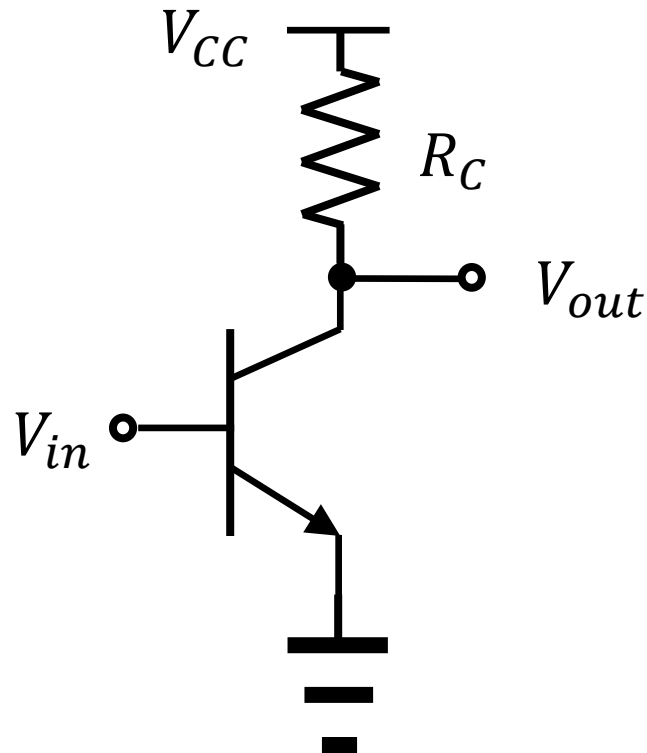
---

- Consider a bipolar junction transistor.
  - In the BJT,  $I_S = 10^{-15}$  A.
  - The Early voltage is 100 V.
  - Also use the approximate relation,  $\exp \frac{60 \text{ mV}}{V_T} \approx 10$ .
  - Draw the collector current as a function of the collector-emitter voltage for  $V_{BE} = 0.72$  V.
  - Explicitly show the current values as much as you can.  
(Approximate graph is allowed.)

# Problem9

---

- Consider a common-emitter amplifier.
  - 1. Express  $g_m$  and  $r_o$  of the bipolar junction transistor as a function of the collector current.
  - 2. Show that the voltage gain becomes insensitive to  $I_C$ , when we have a very large  $R_C$ .



# Problem10

---

- G-SPICE input file for a circuit is shown.
  - 1. Draw the circuit diagram.
  - 2. Calculate the voltage of node#2.(Approximate solutions are allowed.)

```
tstep = 1e-3 ;
tnum = 1000 ;
vdc = 1 ;
vdc_value = 1.8 ;
vdc_node1 = 0 ;
vdc_node2 = 3 ;
vsweep = 1 ;
vsweep_value = 1.8 ;
vsweep_num = 100 ;
vsweep_node1 = 0 ;
vsweep_node2 = 1 ;
mos[0] = 1 ; (NMOS)
mos_type[0] = 0 ;
mos_vt0[0] = 0.4 ;
mos_kp[0] = 100e-6 ;
mos_w[0] = 2.0 ;
mos_l[0] = 0.18 ;
mos_lambda[0] = 0.0 ;
mos_node1[0] = 0 ; (S)
mos_node2[0] = 1 ; (G)
mos_node3[0] = 2 ; (D)
r[0] = 1 ;
r_value[0] = 5e3 ;
r_node1[0] = 2 ;
r_node2[0] = 3 ;
```

# Problem11

---

- NMOS inverter vs. CMOS inverter
  - 1. For each inverter, sketch the drain current as a function of the input voltage.
  - 2. Compare the results from the viewpoint of the standby power.

