Final exam, Electronic Circuits, Spring semester, 2017

June 12, 2017

We have 50 questions. The exam ends at noon. Write down your answers on the answer sheets. For each question, use the designated answer slot.

In the final exam, no partial credit will be given.

When the numbers are provided, just answer a numerical value and a correct unit.

Some useful facts are summarized below:

For a resistor, $V = IR$. For a capacitor, $I = C\, dV/dt$. For an inductor, $V = L\, dI/dt$.

A good value for the thermal voltage, V_T, at room temperature is 0.02585 V. You may use an approximate value.

Approximately, $\ln 10 \approx 2.3$. Moreover, $e^{-0.7} \approx 0.5$.

The vacuum permittivity is approximately 8.85×10^{-12} F/m.

The (absolute) elementary charge is approximately 1.6×10^{-19} C.

At a given time, the power dissipation is defined by $P(t) = I(t)V(t)$.

At room temperature, the intrinsic carrier density of silicon, n_i, is 10^{10} /cm^3.

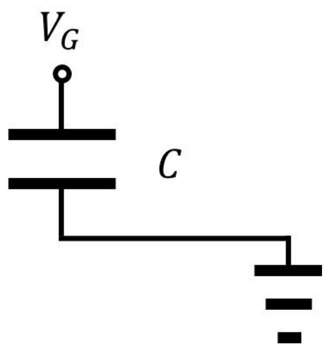
The built-in potential in a pn junction is given by $V_0 = V_T \ln \frac{N_A N_D}{n_i^2}$.

1. Consider a resistor whose resistance is $1\,\mathrm{k\Omega}$. The voltage across the resistor is given by $3 + 0.1 \sin 2\pi t$ V. Calculate the resistor current as a function of time

2. Consider a capacitor whose capacitance is $1\,\mathrm{pF}\ (= 10^{-12}\,\mathrm{F})$. The voltage across the capacitor is given by $3 + 0.1 \sin 2\pi t$ V. Calculate the capacitor current as a function of time.

3. Consider a capacitor whose capacitance is $1\,\mathrm{pF}\ (= 10^{-12}\,\mathrm{F})$. At 1 MHz, calculate its impedance. Note that $e^{j\omega t}$ is the assumed time-dependence. Here, j is the imaginary unit. You may use $\pi \approx 3.14$.

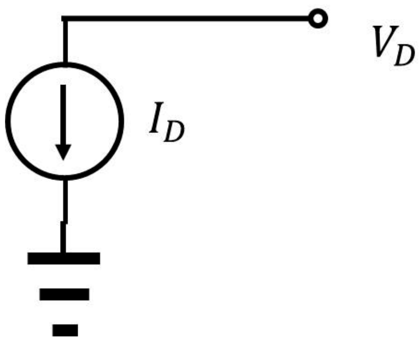
4. Calculate the impedance seen from the "G" node at a very low frequency.



Problem 4.

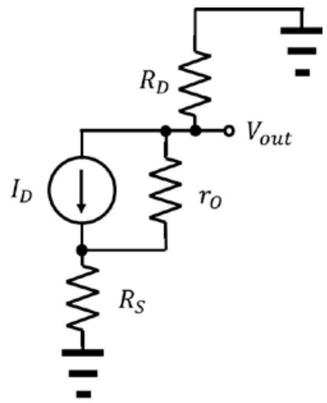
5. Repeat Problem 4 at a finite frequency of f.

6. Calculate the impedance seen from the "D" node at a very low frequency. Here, I_D is fixed.



Problem 6.

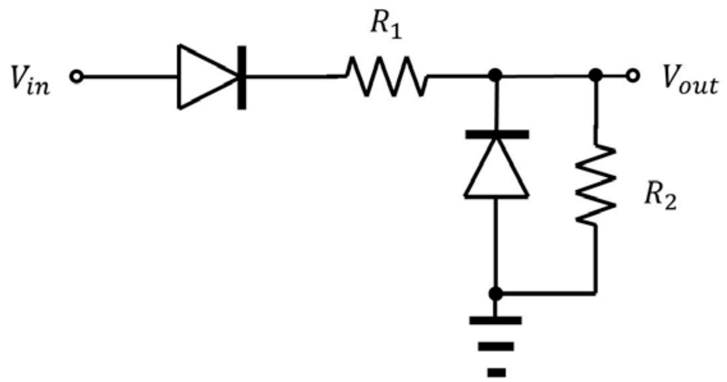
7. By using the Kirchhoff current law, express the output voltage as a function of I_D.



Problem 7.

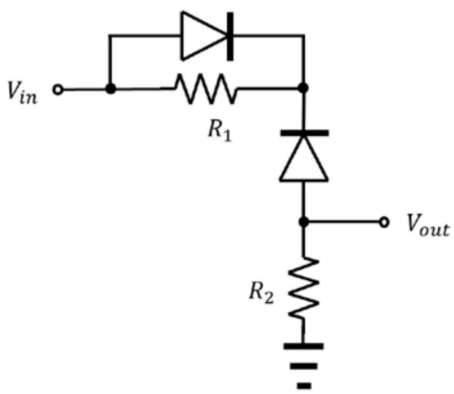
8. When a pn junction is reverse-biased, the (absolute) magnitude of the terminal current is 10^{-15} A. We want to have 1 mA in the forward mode. What is the required forward bias voltage?

9. Assume a constant-voltage model for diodes. The turn-on voltage of the diode is V_{on}. For a positive V_{in}, draw V_{out} as a function of V_{in}.



Problem 9.

10. Assume a constant-voltage model for diodes. The turn-on voltage of the diode is V_{on}. Consider both of a positive V_{in} and a negative V_{in}. Draw V_{out} as a function of V_{in}.

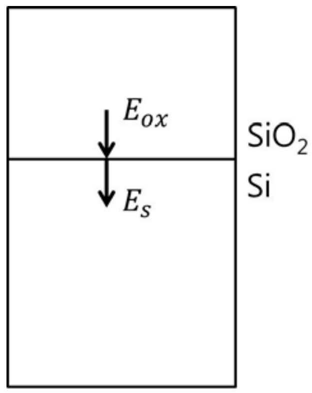


Problem 10.

11. The oxide thickness is 2 nm. Use 4.0 as the relative permittivity of SiO_2. Calculate the gate capacitance per unit area. (Write down the numerical value.)

12. Consider the gate stack in Problem 11. The gate area is $10\,\mathrm{nm} \times 10\,\mathrm{nm}$. Initially, the transistor was biased with $V_{GS} = 0.5\,\mathrm{V}$, which is slightly larger than the threshold voltage. Later, the gate bias is increased to $V_{GS} = 1.5\,\mathrm{V}$. Then, how many electrons are additionally collected in the Si/SiO_2 interface? (Your answer should be a number.)

13. Consider a Si/SiO_2 interface. In this problem, the relative permittivity of Si and SiO_2 are 11.7 and 3.9, respectively. The vertical field components at the interface are denoted as E_s (Si side) and E_{ox} (SiO_2 side). When E_s is 1 MV/cm, calculate E_{ox}.



Problem 13.

14. In a Si/SiO_2 interface, the magnitude of the surface electric field (in the Si side) is given by E_s. The field is heading toward the Si substrate. The Si substrate is p-type doped with an acceptor doping concentration of N_A. Under the depletion approximation, express the depletion width (W_d) as a function of E_s. In this problem, ignore the electron density.

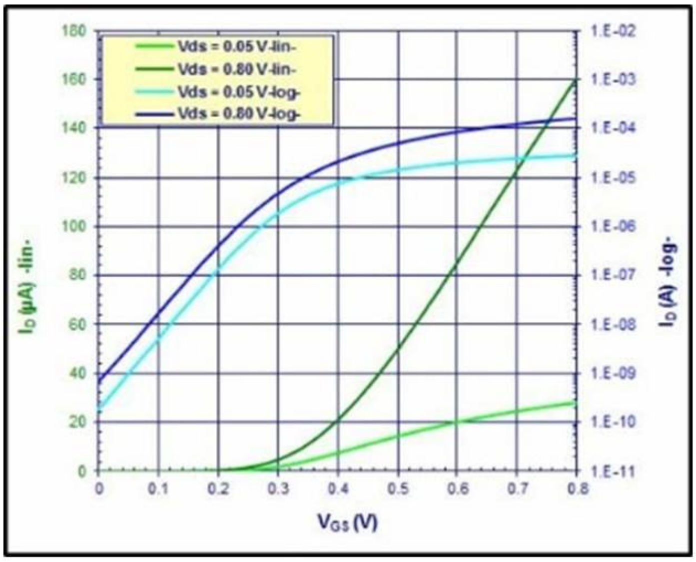
15. Consider the structure in Problem 14. We can define the potential difference between the interface and a point located deep in the substrate. Let's call this quantity ϕ_s. Express ϕ_s as a function of E_s.

16. Using the answers of Problems 14 and 15, express the net depletion charge density (charge per unit area) as a function of ϕ_s. Be careful about the sign.

17. Let us assume that we want to fabricate a 1-nm-thick silicon dioxide (whose relative permittivity is 3.9) layer for the insulating layer of the MOSFET. However, it is not very easy to fabricate it, simply because it is too thin. Instead, we want to obtain the same gate capacitance using a different material. For example, a hafnium oxide (whose relative permittivity is assumed to

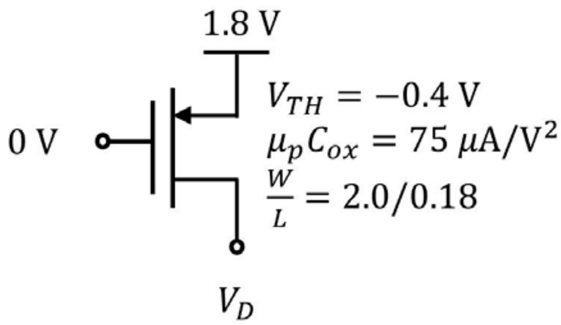
be 23.4) layer is introduced. Then, calculate the thickness of the hafnium oxide layer to get the required gate capacitance.

18. The real $I_D - V_{GS}$ curves of Intel's 14 nm NMOSFET are shown. (The graph is taken from Techinsights.) Since green curves are shown in the linear scale, concentrate on them. Estimate the threshold voltage.



Problem 18. (From Techsights)

19. Consider a PMOSFET. What is the gate overdrive voltage? Write down the absolute value.



Problem 19.

20. Consider the PMOSFET in Problem 19. When the drain voltage is 1.6 V, calculate the source current. Be careful about the sign.

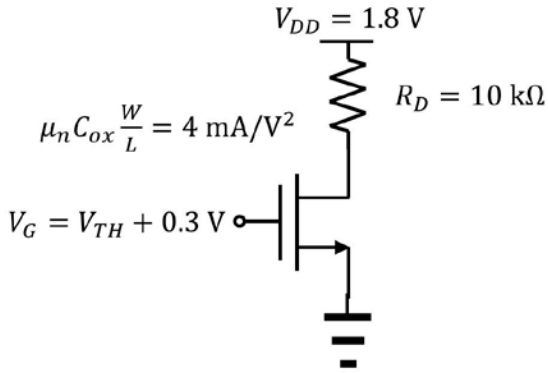
21. The drain current of a NMOSFET is 1 mA. Another MOSFET has the exactly same structure

with ten times larger channel width. When the same bias voltages are applied to this MOSFET, what is the expected drain current?

22. The gate overdrive voltage of a NMOSFET is 0.3 V. Moreover, $\mu_n C_{ox}\frac{W}{L}$ is $4\ \mathrm{mA/V^2}$. When the drain current is $100\ \mu\mathrm{A}$, what is the drain voltage?

23. Consider the same NMOSFET in Problem 22. The gate bias voltage is the same as before. Only the drain voltage is doubled. Calculate the drain current.

24. Consider the same NMOSFET in Problem 22. The gate bias voltage is the same as before. A resistor, whose resistance is $10\ \mathrm{k\Omega}$, is connected to the drain terminal. The resistor is also connected to $V_{DD}(= 1.8\ \mathrm{V})$. Calculate the drain voltage.



Problem 24.

25. Consider the same circuit in Problem 24. However, the gate overdrive voltage is now 0.1 V. Calculate the drain voltage.

26. In a realistic model, the drain current of a MOSFET in the triode mode is described as

$$I_D = \frac{\mu_n C_{ox} W\left\{(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right\}}{L\left(1 + \frac{V_{DS}}{E_{sat}L}\right)},$$

where all parameters except for V_{GS} and V_{DS} are assumed to be constant. Using this model, explicitly show the transconductance.

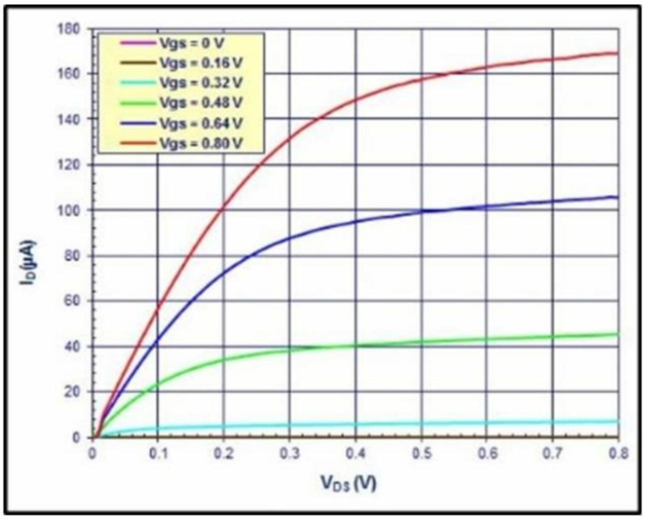
27. Consider the same model in Problem 26. Explicitly show the output resistance.

28. Let's assume that the mobility is a function of V_{GS} such as

$$\mu_n(V_{GS}) = \frac{\mu_0}{1 + \left(\frac{V_{GS} + V_{TH}}{6 \cdot TOXE \cdot E_0}\right)^2},$$

where $TOXE$ and E_0 are constant. A very long channel NMOSFET in the saturation mode is assumed, therefore, the channel length modulation is neglected. Using the above mobility model, express the transconductance as a function of V_{GS} explicitly.

29. The real $I_D - V_{DS}$ curves of Intel's 14 nm NMOSFET are shown. (The graph is taken from Techinsights.) The blue curve is obtained with $V_{GS} = 0.64\ \mathrm{V}$. When $V_{DS} \approx 0.5\ \mathrm{V}$, the drain current is around $100\ \mu\mathrm{A}$. Using the curves, estimate the transconductance at $V_{GS} = 0.64\ \mathrm{V}$ and $V_{DS} = 0.5\ \mathrm{V}$. (Write down a numerical value with a correct unit.)

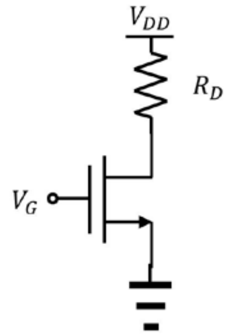


Problem 29. (From Techsights)

30. Using the graph in Problem 29, estimate the output resistance, r_O. Consider the same bias condition, $V_{GS} = 0.64\ \mathrm{V}$ and $V_{DS} = 0.5\ \mathrm{V}$. (Write down a numerical value with a correct unit.)

31. Consider the following DC circuit. Assume that the MOSFET is working in the saturation mode. Express the DC power dissipated by the MOSFET and the resistor as a function of V_G, V_{DD}, and other device parameters. (Neglect the channel length modulation.)

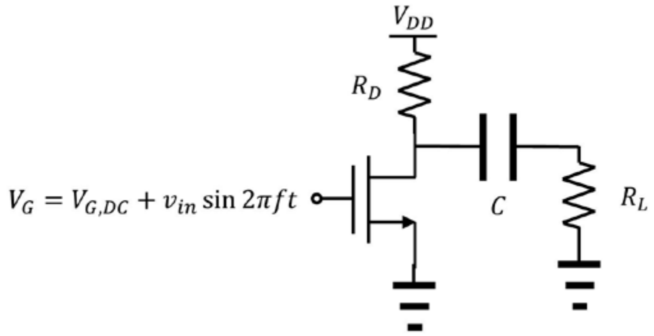
$\mu_n C_{ox}$, V_{TH}, and W/L are given.



Problem 31.

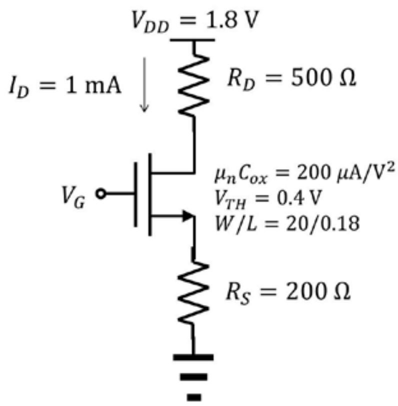
32. Consider the following common-source amplifier. Assume that the MOSFET is working in the saturation mode. Express the average power dissipated by the load resistor as a function of v_{in}, $V_{G,DC}$, V_{DD}, R_L, and other device parameters. (Neglect the channel length modulation.) Note that we consider a nonzero frequency, f.

$\mu_n C_{ox}$, V_{TH}, and W/L are given. $2\pi f C \gg 1$.



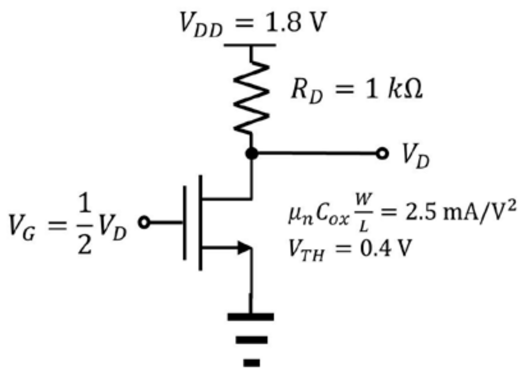
Problem 32.

33. Calculate the gate voltage.



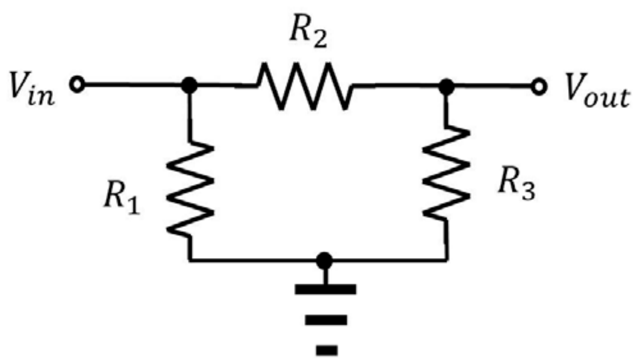
Problem 33.

34. Calculate the drain voltage.



Problem 34.

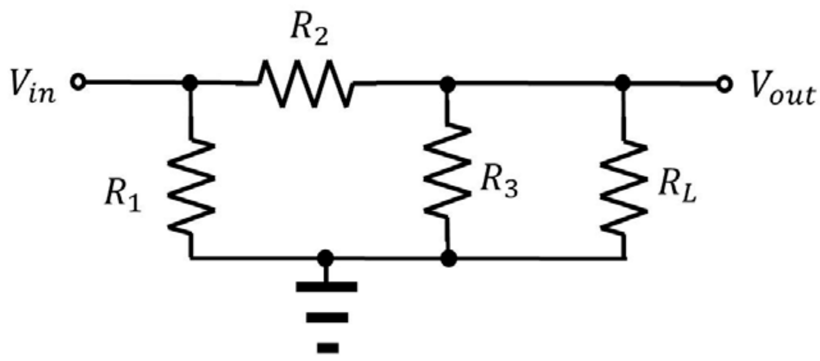
35. Consider a network of resistors. Although it is not an amplifier, we can define the voltage gain (A_v) as a ratio, $\frac{V_{out}}{V_{in}}$, anyway. Express A_v as a function of R_1, R_2, and R_3.



Problem 35.

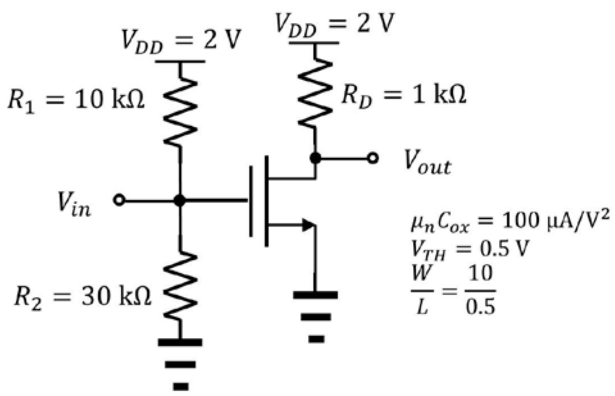
36. Consider the network in Problem 35. Express the input and output resistances (R_{in} and R_{out}) as a function of R_1, R_2, and R_3.

37. Consider a resistor network. Express the output voltage, V_{out}, using V_{in}, A_v, R_{in}, R_{out}, and R_L. (Do not use R_1, R_2, and R_3.)



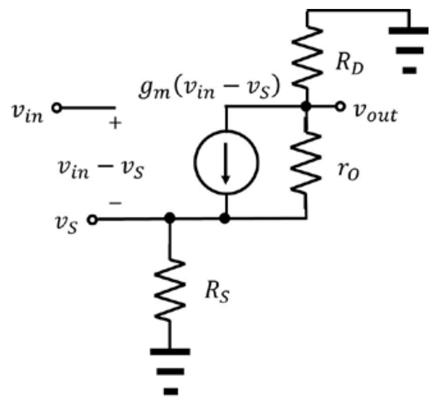
Problem 37.

38. Consider the common-source amplifier. Calculate the (small-signal) voltage gain.



Problem 38.

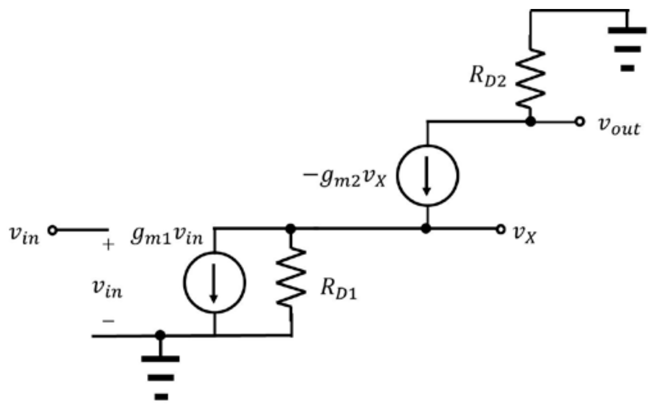
39. Consider a small-signal circuit. Calculate the voltage gain. (Here, v_S is introduced for notational simplicity. The voltage gain is defined between v_{in} and v_{out}.)



Problem 39.

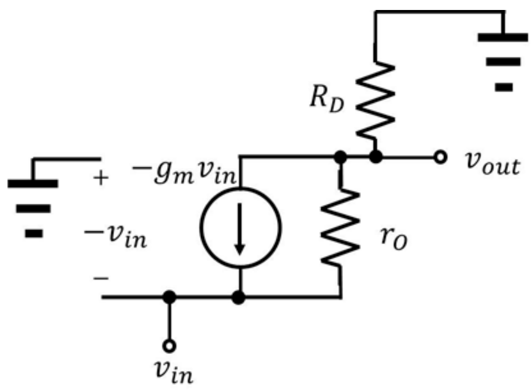
40. Consider the same small-signal circuit in Problem 39. Calculate the input and output resistances.

41. Consider a small-signal circuit. Calculate the voltage gain.



Problem 41.

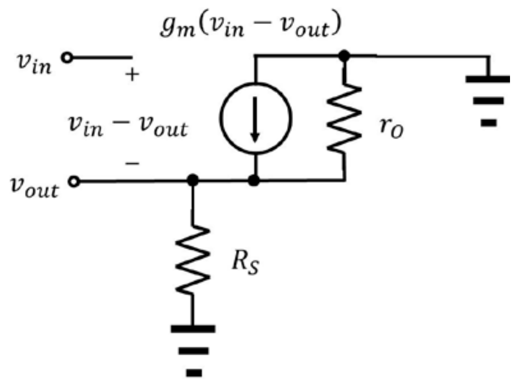
42. Consider a small-signal circuit. Calculate the voltage gain.



Problem 42.

43. Consider the same small-signal circuit in Problem 42. Calculate the input and output resistances.

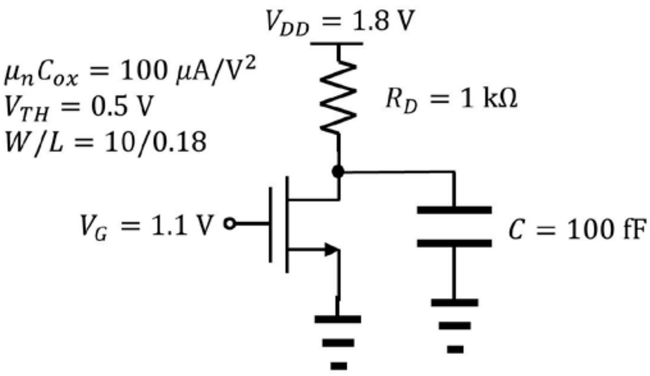
44. Consider a small-signal circuit. Calculate the voltage gain.



Problem 44.

45. Consider the same small-signal circuit in Problem 44. Calculate the input and output resistances.

46. Calculate the DC voltage of the drain terminal.

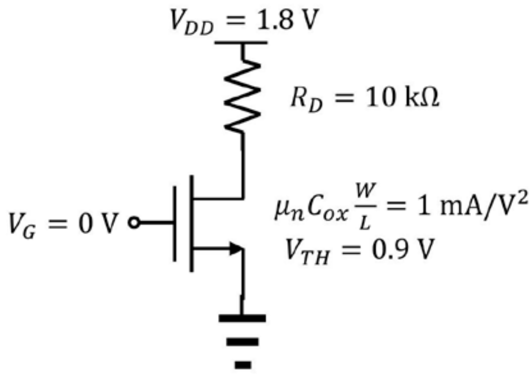


Problem 46.

47. Now assume that the gate voltage is suddenly changed to 0 V. After 70 psec, what is the drain voltage? (Write down the numerical value.)

48. Repeat Problem 47. After several minutes, what is the drain voltage?

49. Calculate the drain voltage.



Problem 49.

50. Repeat Problem 49 with $V_G = V_{DD}$.