
Lecture23:

Dynamic characteristics

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RC circuit

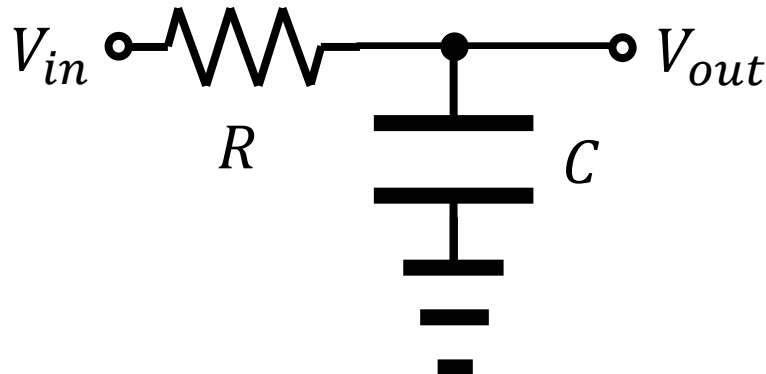
- Consider a serial RC circuit.

- The KCL states

$$\frac{V_{out} - V_{in}}{R} + C \frac{dV_{out}}{dt} = 0$$

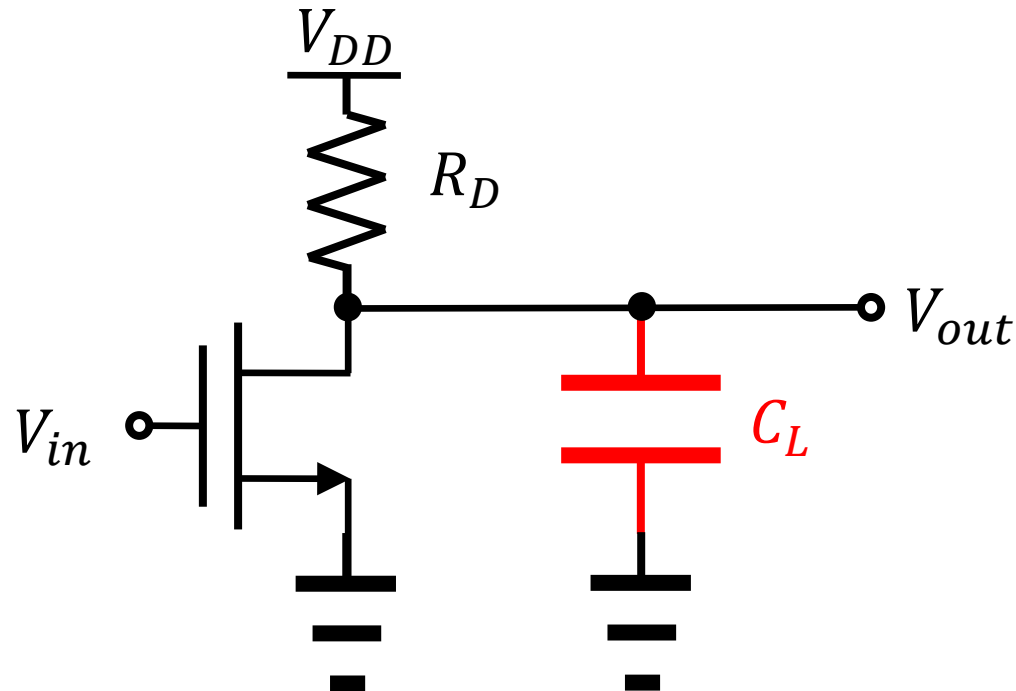
- Assume a step-wise change of V_{in} at $t = 0$. It becomes V_{DD} .
- Initial output voltage is V_0 .
- Its solution is given by

$$V_{out}(t) = V_{DD} + (V_0 - V_{DD}) \exp\left(-\frac{t}{RC}\right)$$



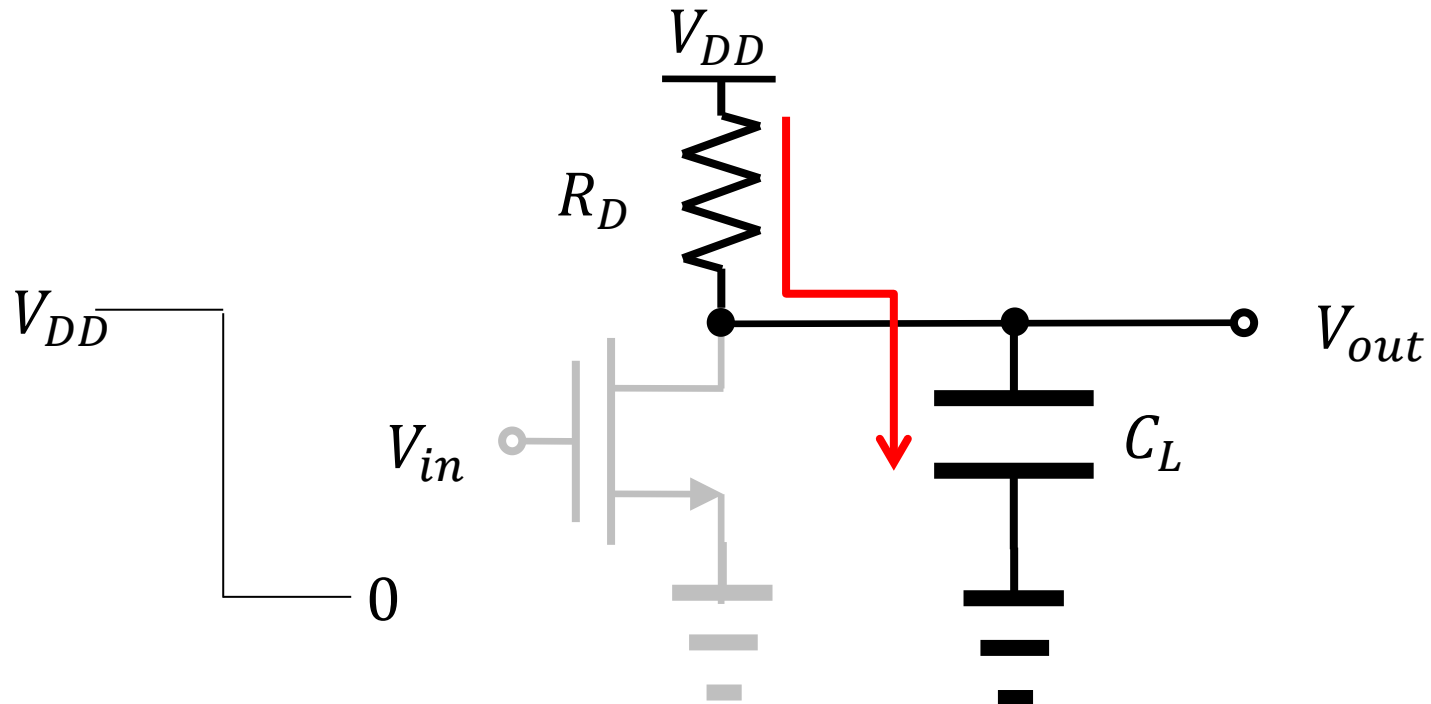
Speed of inverter (1/4)

- VTC merely describes the DC behavior.
 - Input voltages with different frequencies (1 kHz, 1 MHz, 1 GHz, ...)
 - Time-dependent behavior



Speed of inverter (2/4)

- A rapid transition of V_{in} from V_{DD} to 0
 - The capacitor should be charged.



Speed of inverter (3/4)

- Simply, it is a RC circuit.

- Then, the solution is simply

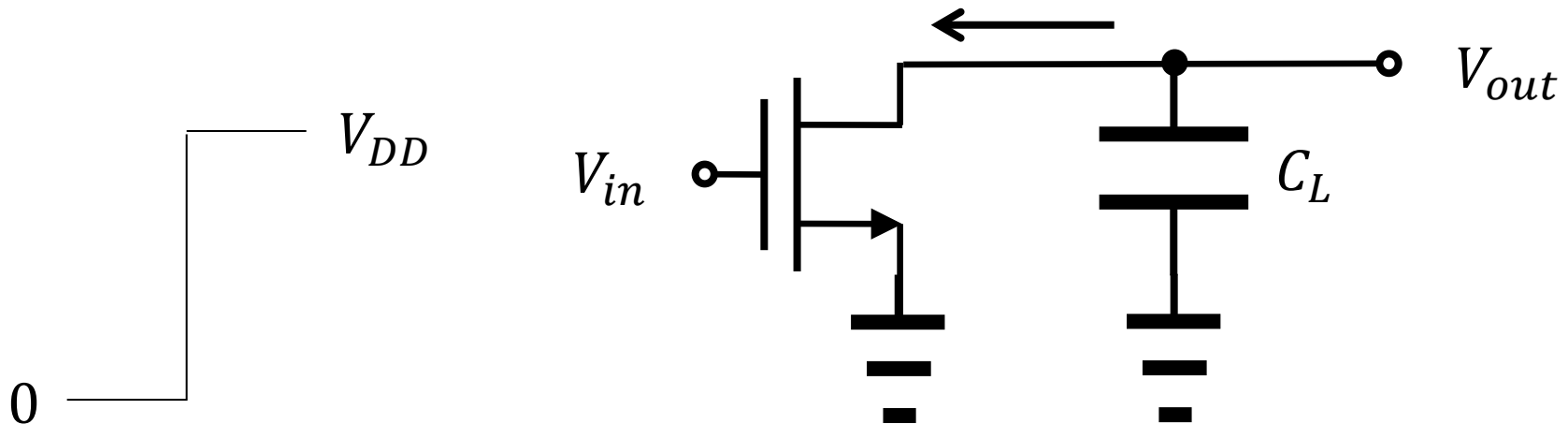
$$V_{out}(t) = V_{out}(0^-) + [V_{DD} - V_{out}(0^-)] \left(1 - \exp \frac{-t}{R_D C_L} \right)$$

- Since $\exp(-3) \approx 0.05$, after $3R_D C_L$, V_{out} reaches $0.95 V_{DD}$.
 - Yes, it takes time to get the stable output voltage...
 - The delay restricts the maximum signal frequency.

Speed of inverter (4/4)

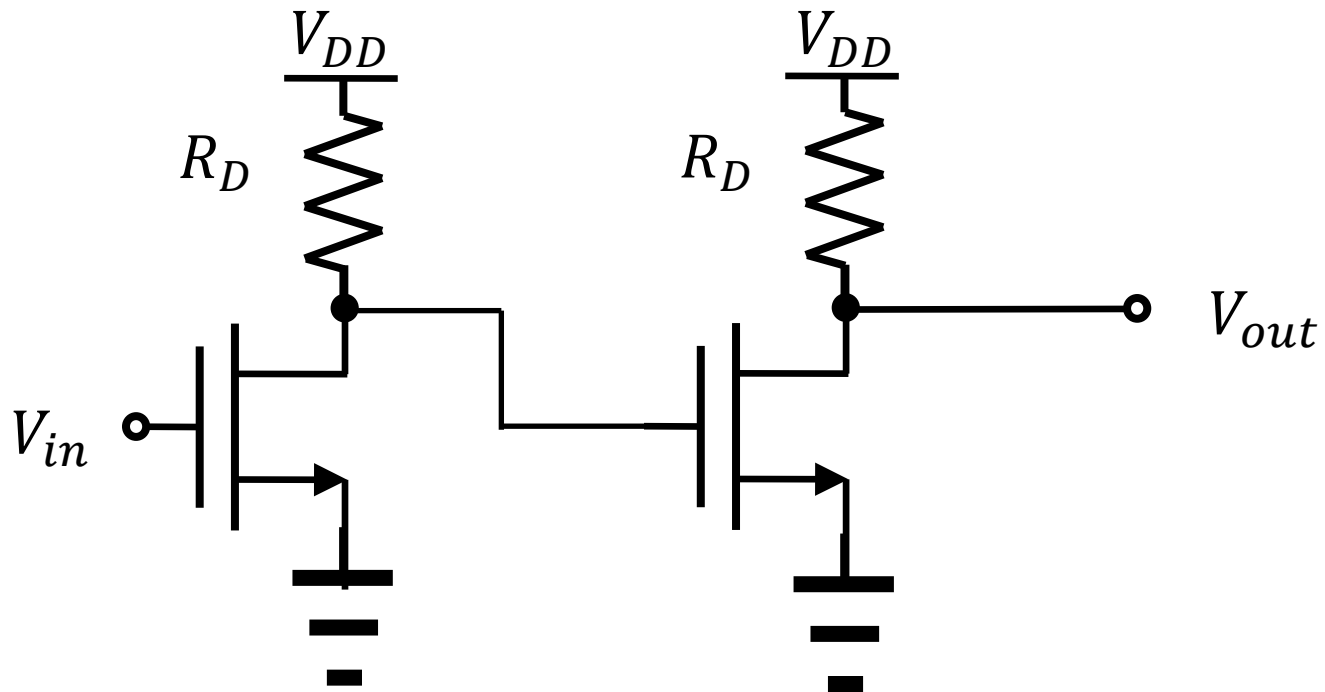
- A rapid transition of V_{in} from 0 to V_{DD} to 0
 - At the initial phase, the resistor does not conduct.
 - Also the MOSFET is operated in its saturation mode. Then,

$$I_{D,sat} + C_L \frac{dV_{out}}{dt} = 0$$



Origin of C_L ?

- Consider an inverter chain.
 - Then, what is the load capacitance for the first stage?

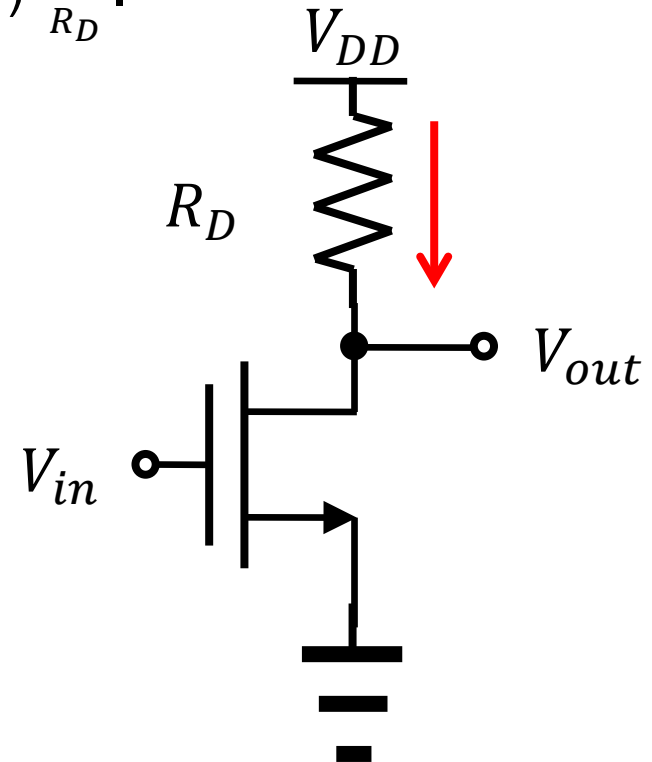


- Interconnect

Standby(!) power

- The biggest problem in the NMOS inverter
 - When $V_{in} = 0$, no standby power
 - When $V_{in} = V_{DD}$?
 - The power consumption is (approximately) $\frac{V_{DD}^2}{R_D}$.
 - If $V_{DD} = 1.8\text{ V}$ and $R_D = 10\text{ k}\Omega$,
324 μW !

$$I_D = \frac{V_{DD} - V_{out}}{R_D} \approx \frac{V_{DD}}{R_D}$$



Homework#10, the final

- Due: 09:00, **June 3 (Mon)**
- Solve the following problems of the final exam in 2018.
 - P26
 - P27
 - P28
 - P29
 - P30