
Lecture26: SPICE results

Sung-Min Hong (smhong@gist.ac.kr)

Semiconductor Device Simulation Lab.
School of Information and Communications
Gwangju Institute of Science and Technology

SPICE

- Simulation Program with Integrated Circuit Emphasis
 - Originally developed at UC Berkeley (first release in 1971)
 - It was a term project in a graduate course!



Is this SPICE? Not in this context...
(Google Images)



Larry Nagel, the main author
of SPICE
(Google Images)

MOS IV (1/3)

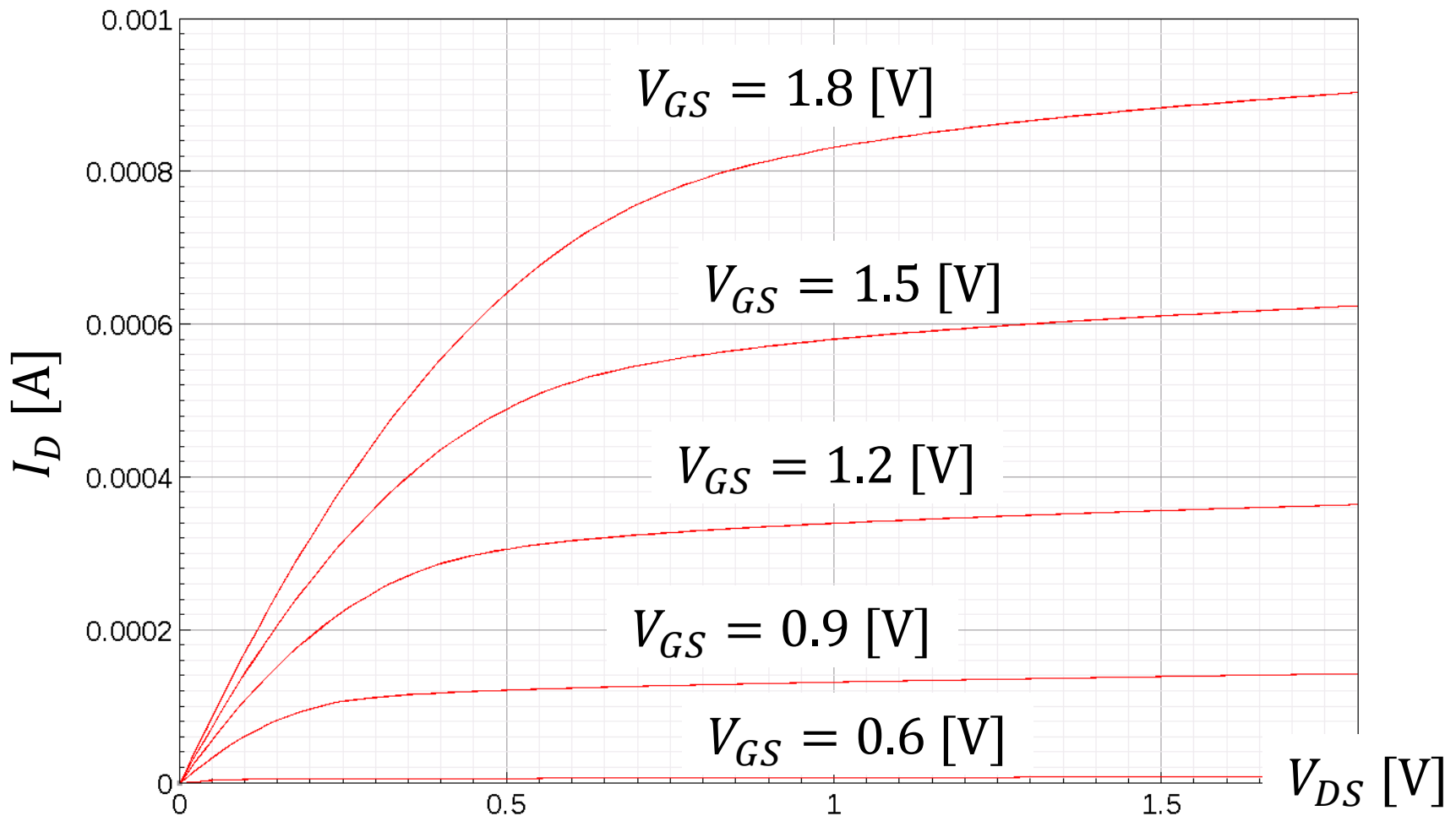
- BSIM3 model (NMOS)
 - $T_{ox} = 9$ [nm]
 - $V_{th0} = 0.6322$ [V] for long-channel devices
- BSIM3 model (PMOS)
 - $T_{ox} = 9$ [nm]
 - $V_{th0} = -0.6732829$ [V] for long-channel devices
- We will use 1.8 V as the V_{DD} .
- Note that these models also consider many parasitic effects.
 - Perfect agreement with our simple results cannot be expected!



Chenming Hu
(Google Images)

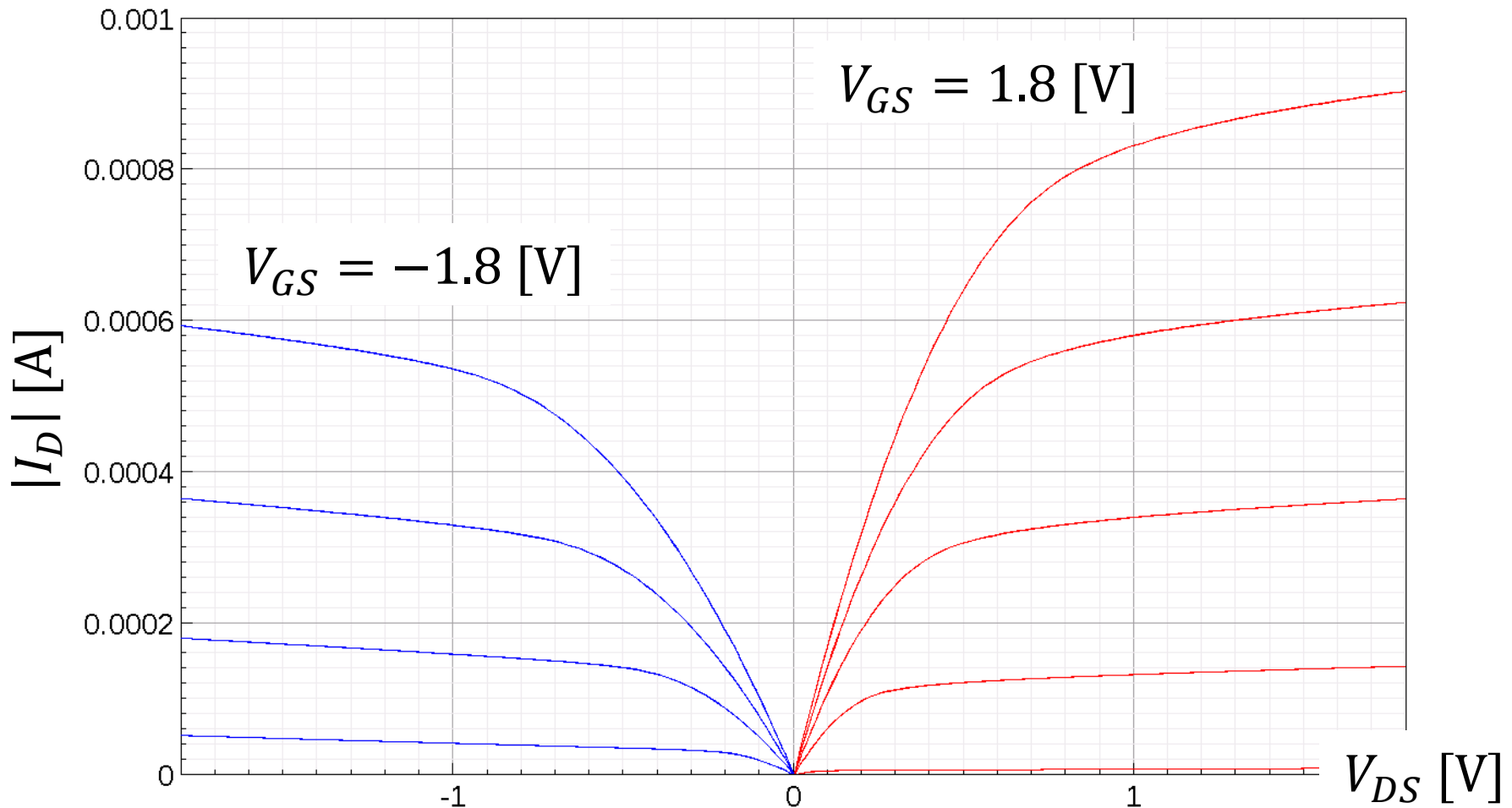
MOS IV (2/3)

- NMOS IV curve ($L = 0.5$ microns, $W = 10$ microns)
 - Channel-length modulation is visible.



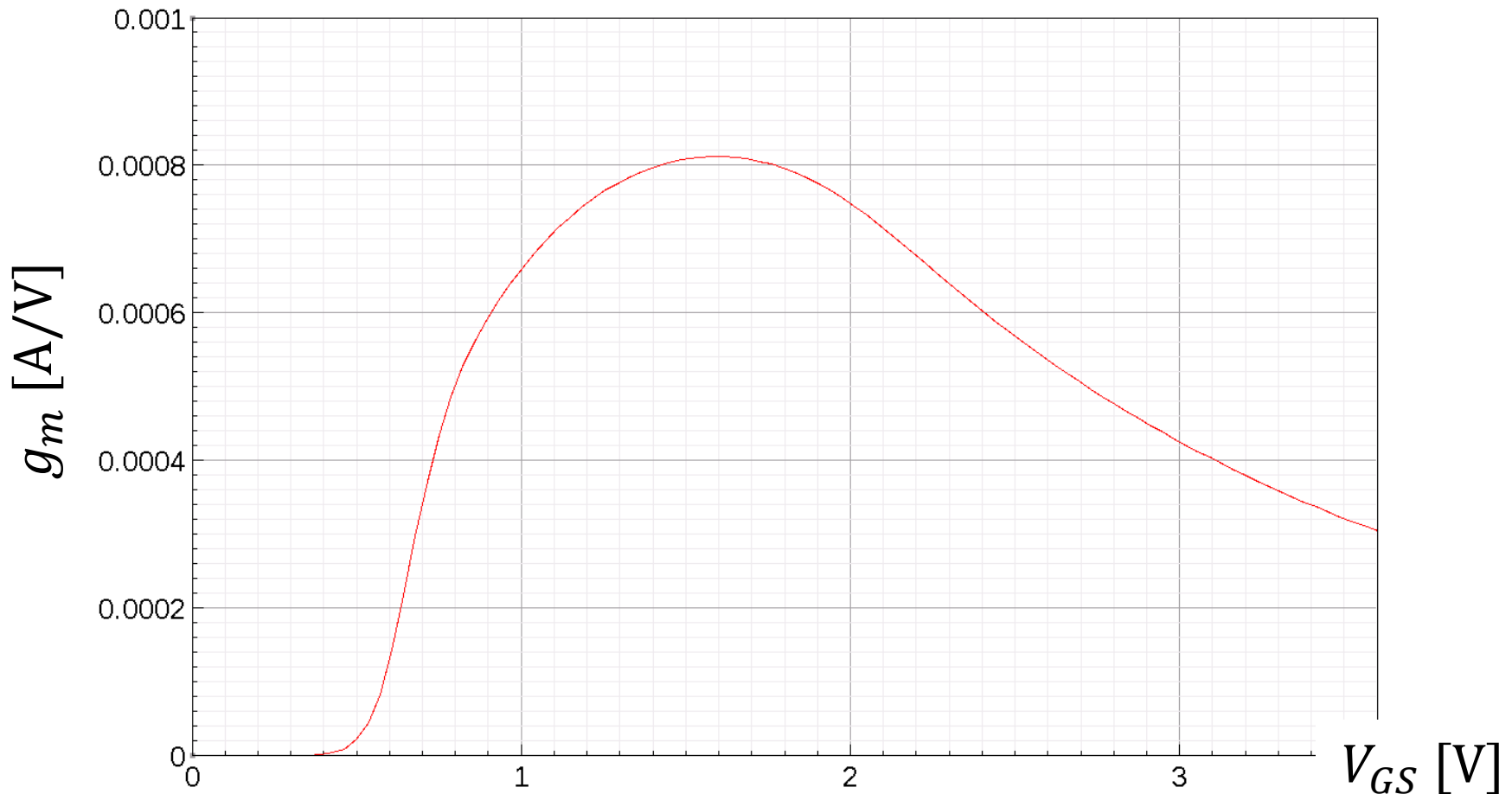
MOS IV (3/3)

- PMOS IV curve ($L = 0.5$ microns, $W = 10$ microns)
 - Certainly, its current level is smaller than the NMOS.



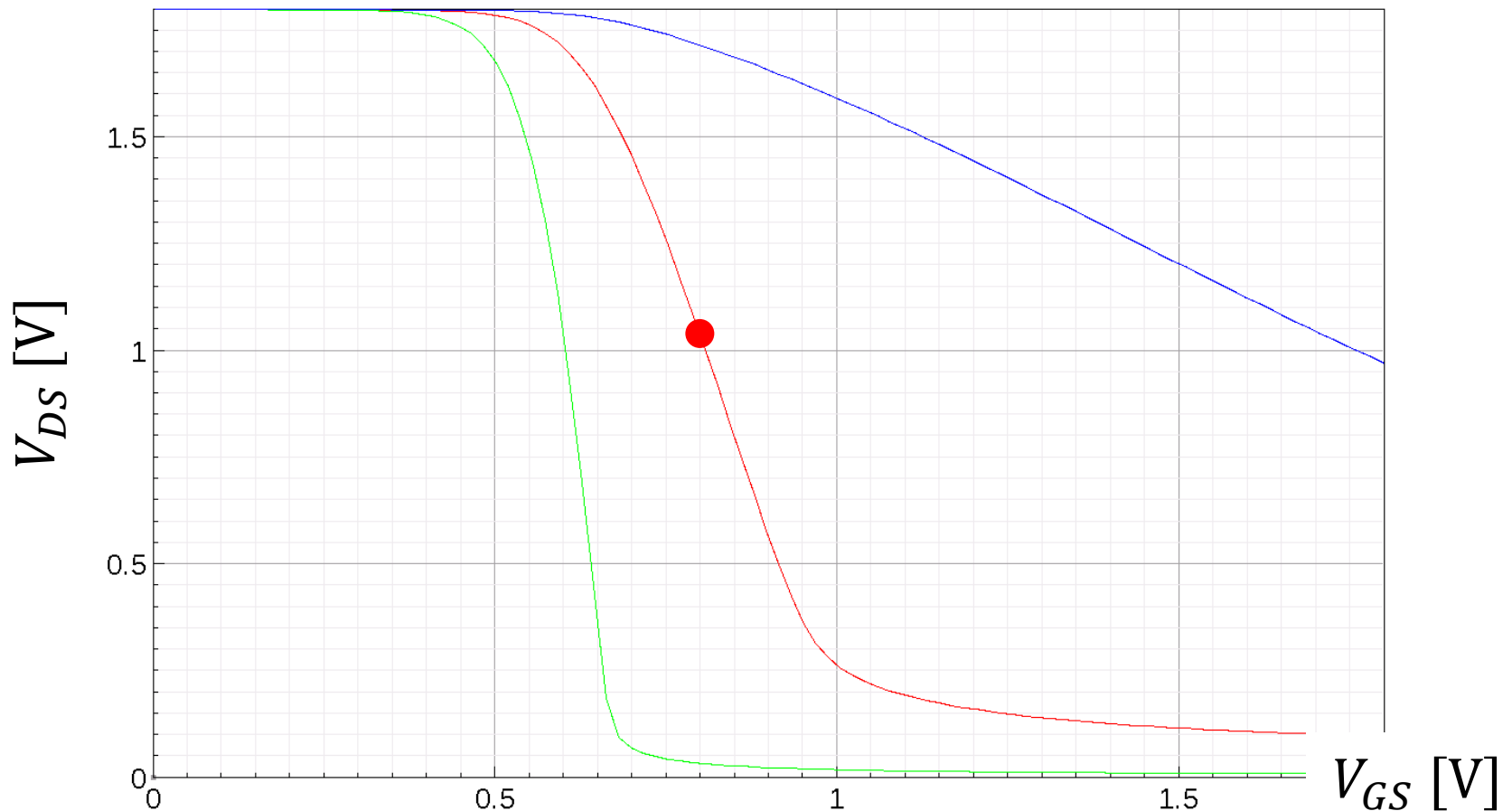
Transconductance

- NMOS g_m ($L = 0.5$ microns, $W = 10$ microns)
 - Curve at $V_{DS} = \frac{1}{2}V_{DD}$.



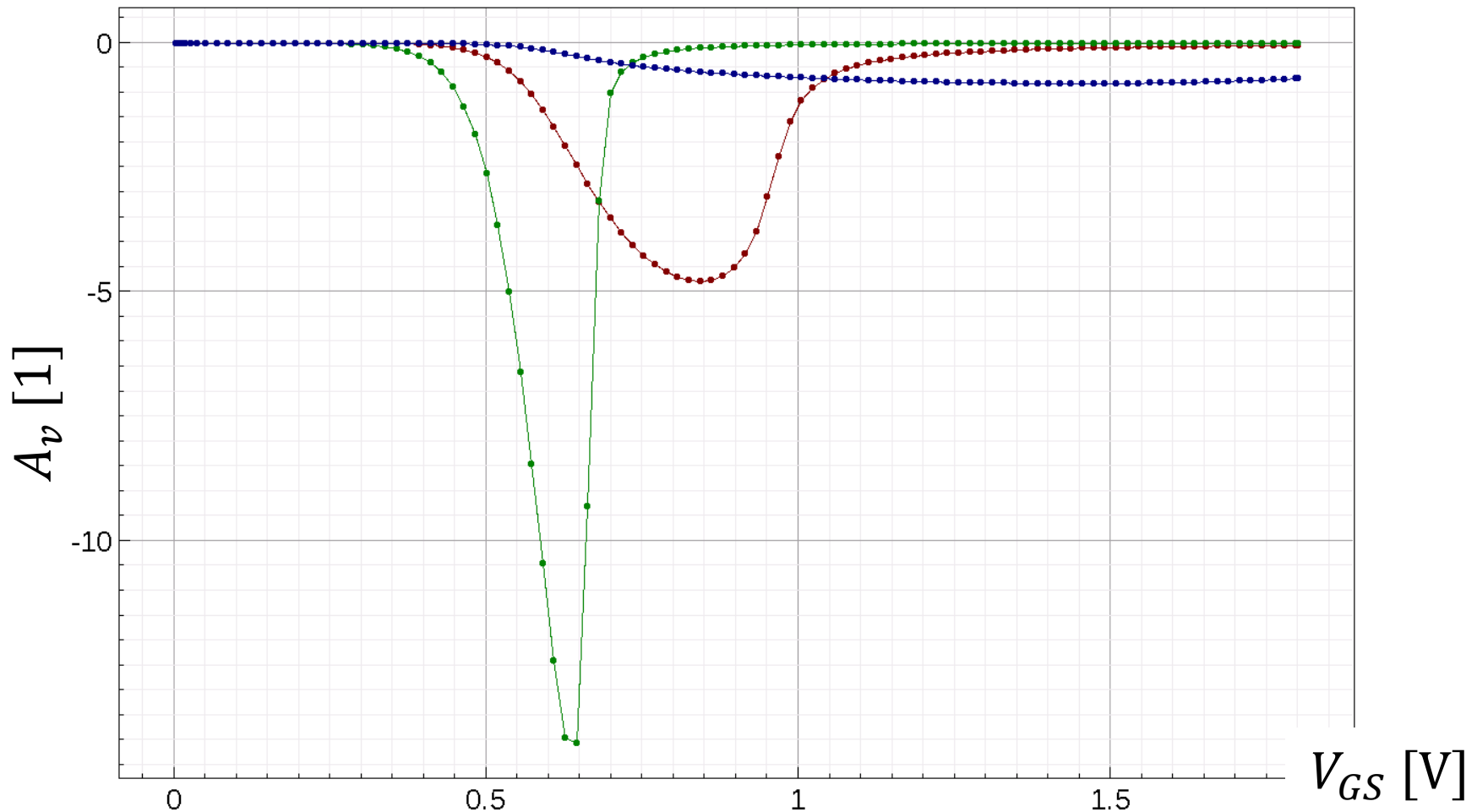
Common-source (1/3)

- Consider a CS stage ($L = 0.5$ microns, $W = 10$ microns)
 - The VTC is shown for different load resistances, $1\text{ k}\Omega$, $10\text{ k}\Omega$, and $100\text{ k}\Omega$.



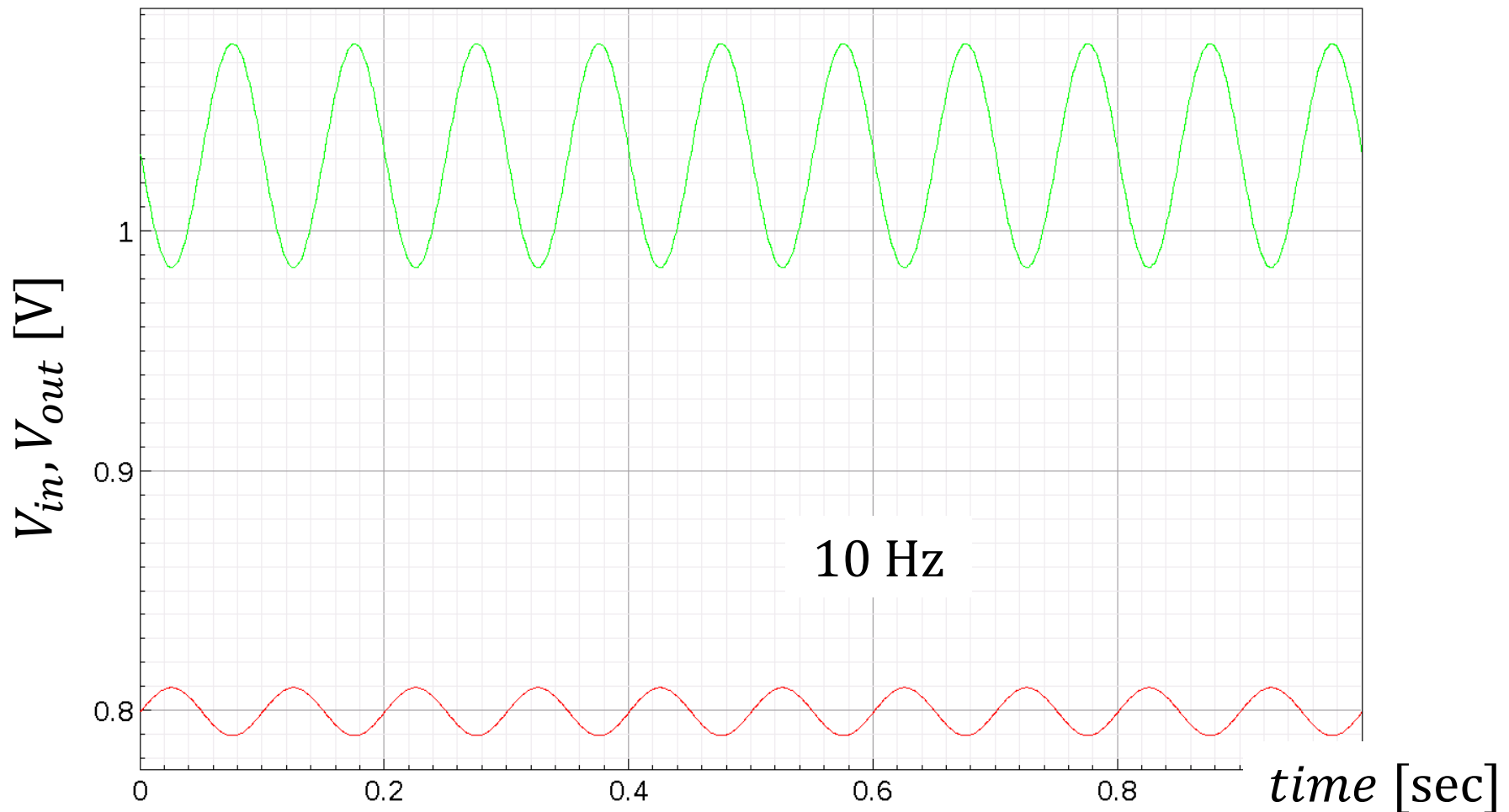
Common-source (2/3)

- From the previous curve,
 - We can calculate the voltage gain.



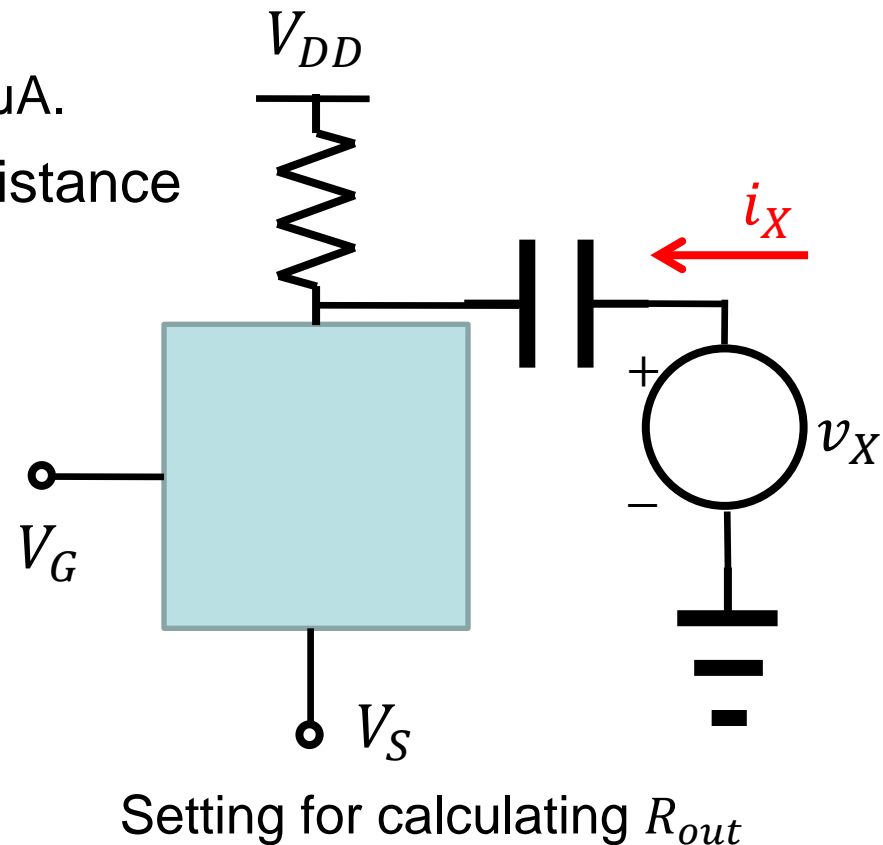
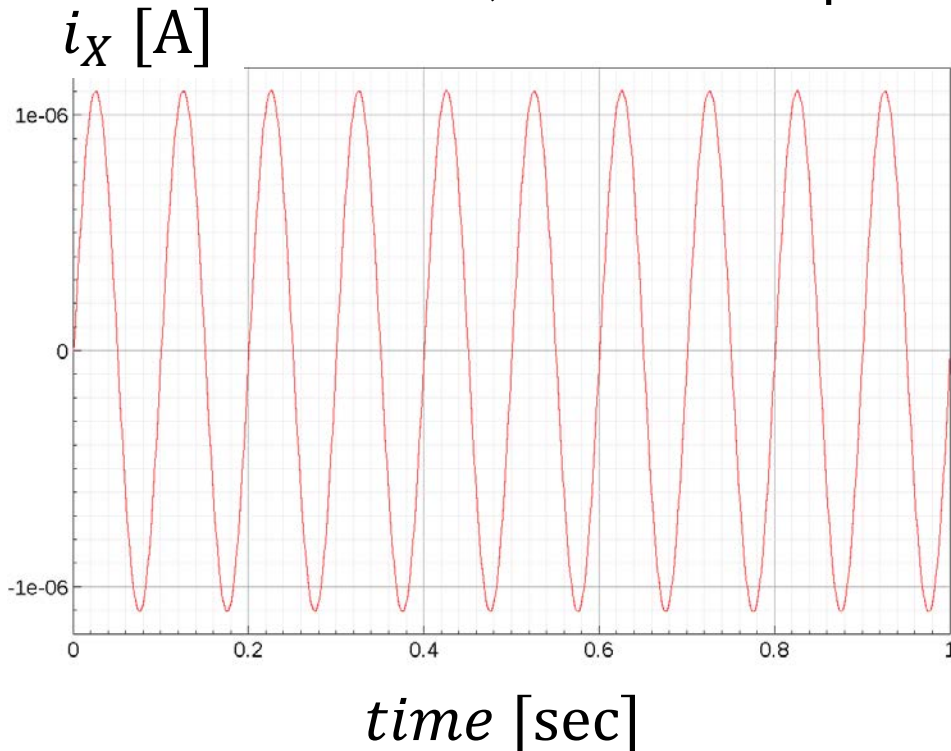
Common-source (3/3)

- Checking directly with transient simulation
 - Load resistance of $10\text{ k}\Omega$ is used. ($V_{GS} = 0.8\text{ V}$, amplitude of 10 mV)



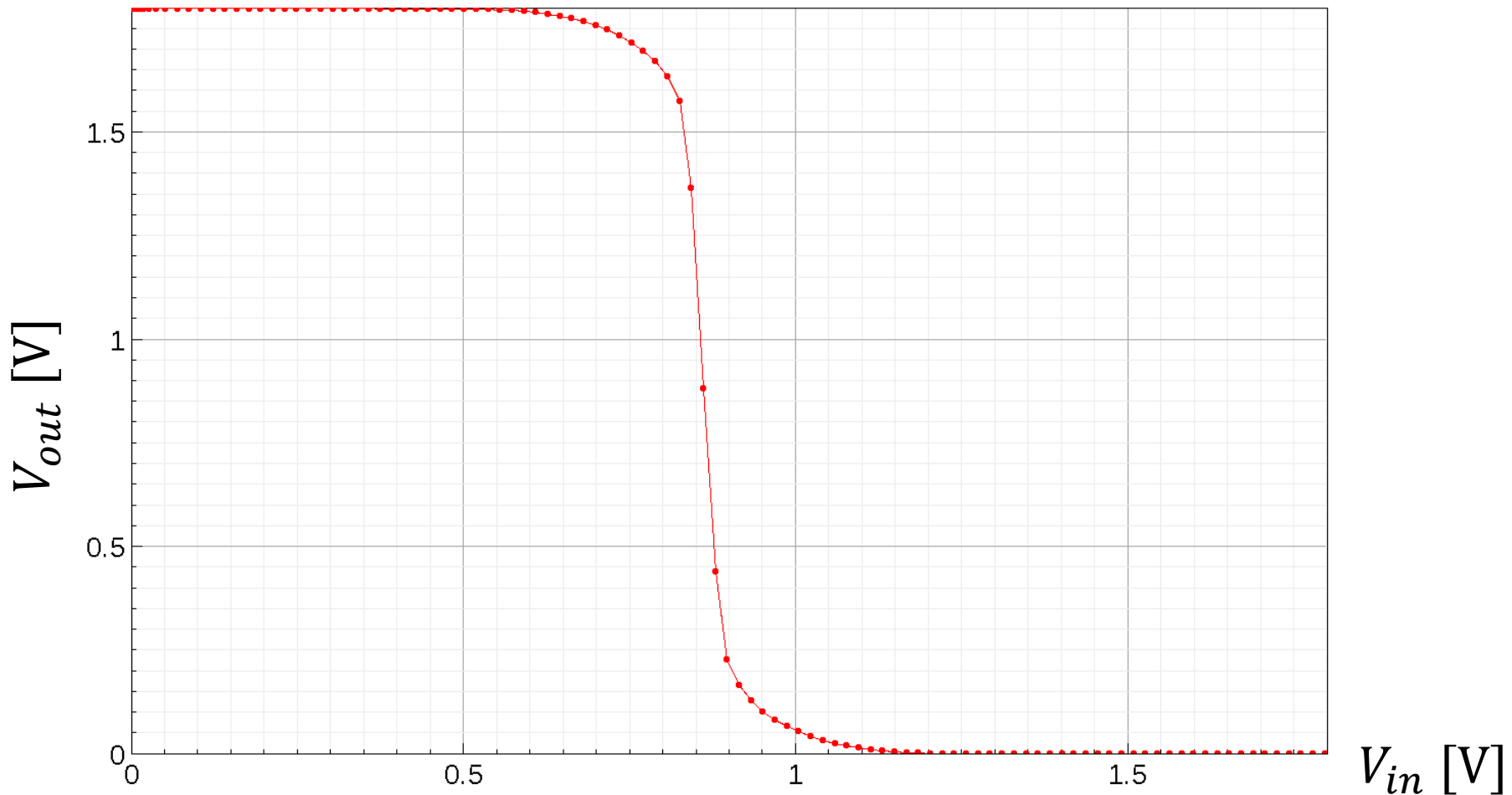
Measuring impedances

- Applying a small-signal voltage excitation
 - Amplitude was 10 mV.
 - Current has an amplitude of 1.1 μA .
 - Therefore, 9 k Ω of output resistance



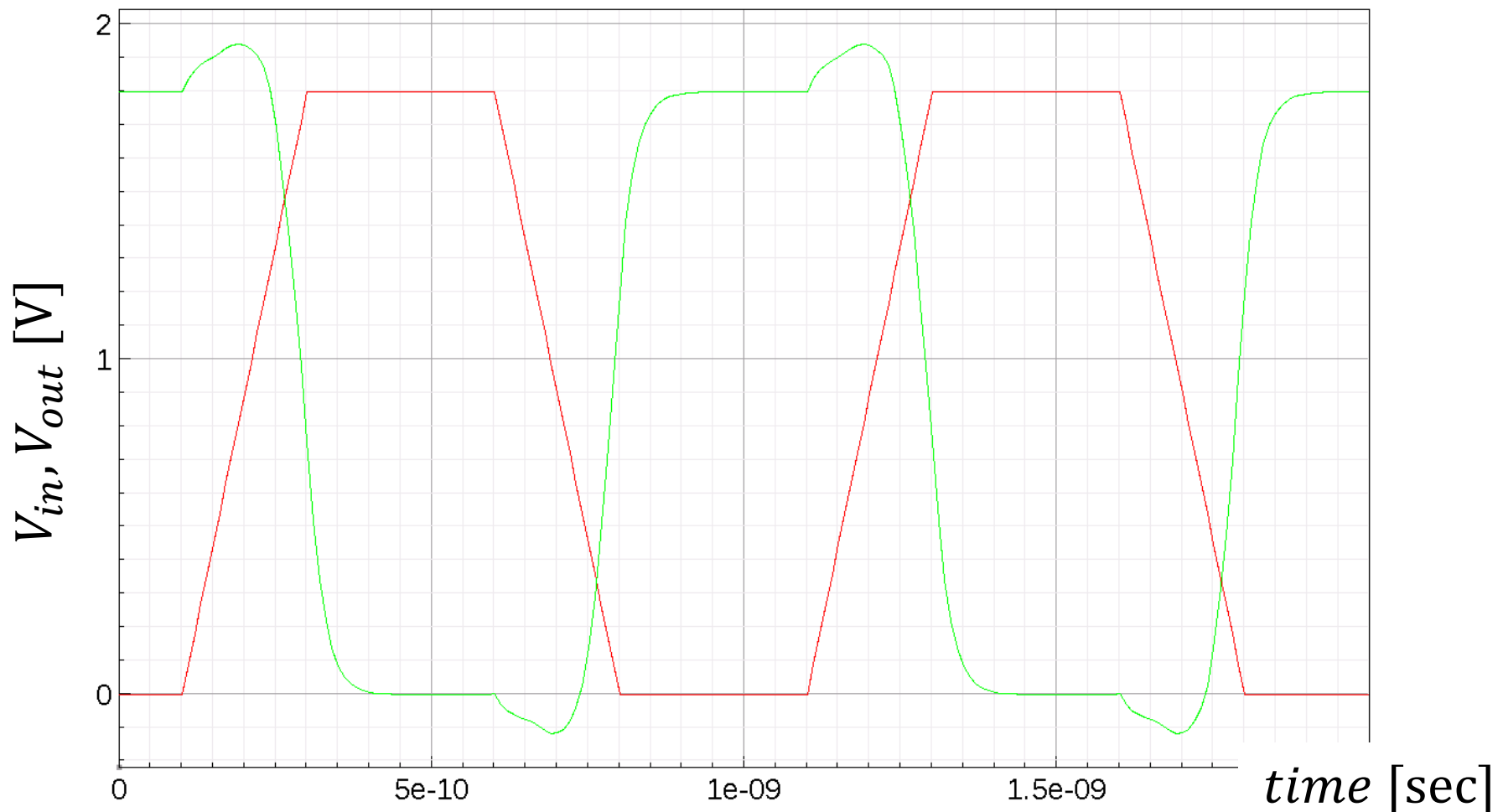
CMOS inverter

- Width ratio = 1:2 (NMOS:PMOS)
 - Improved VTC, as expected



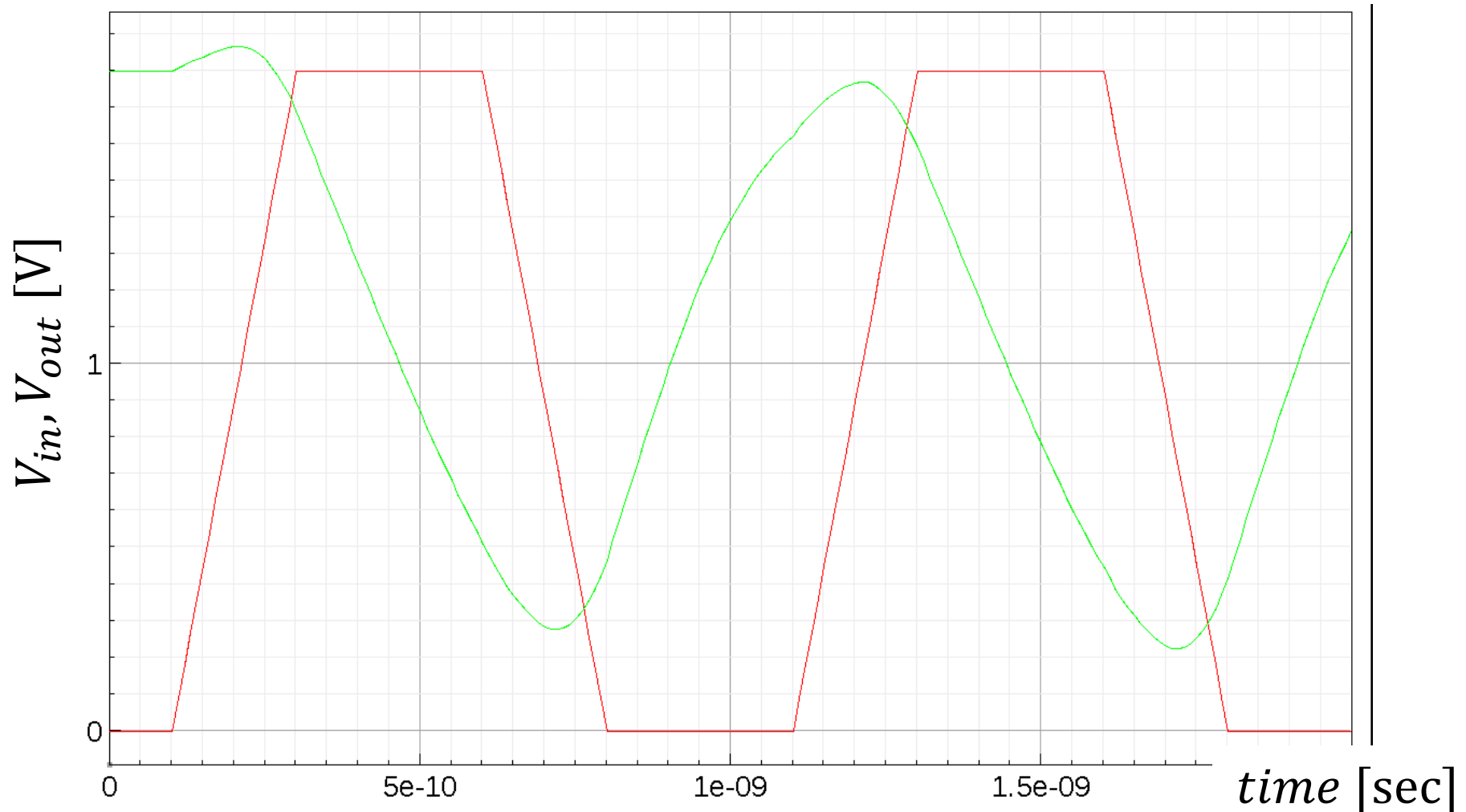
Transient simulation (1/2)

- Load capacitor of 20 fF
 - 1 GHz signal



Transient simulation (2/2)

- Higher value of load capacitance, 200 fF



Final exam.

- The day after tomorrow!
 - June 10 (Wed)
 - PM 01:00 ~ 02:15 (Class time)
 - In this time, we will have an ordinary paper exam.
 - Again, no calculator, no cell phone, ...