
Lecture23:

Digital CMOS circuits (1)

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Lecture schedule

- L23, L24, L25, and L26
 - L23 (Today): Digital circuits (1)
 - L24 (Mon): Digital circuits (2)
 - L25 (Wed), L26 (Mon): Operational amplifiers, SPICE, and review
- Final exam
 - June 10 (Wed)
 - PM 01:00 ~ 02:15 (Class time)

Why digital?

- You know the answer.
 - And you know what it actually is. (Binary)
- Today, we will consider the following questions:
 - How can we treat the arithmetic operations (Addition, subtraction, multiplication, ...)
 - What is the elemental operation?
 - Then, what are the essential circuits to build such a system?
 - (It will be a short review on Digital Design.)
- Inverter and NAND gates

Addition

- Once you can add two numbers, x and y , you can do
 - Addition, $x + y$ (of course)
 - Subtraction, $x - y = x + (-y)$
 - Multiplication, $x \times y$

Even in addition,

- You can recognize that
 - Addition of two 1-bit binary numbers is the core operation!
 - There are only four possible cases!

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10 \leftarrow \text{Carry}$$

Inclusion of carry-bit

- In order to unify the notation, we introduce a separate bit for representing the carry.

- Carry-bit & sum-bit

$$0 + 0 = 00$$

$$0 + 1 = 01$$

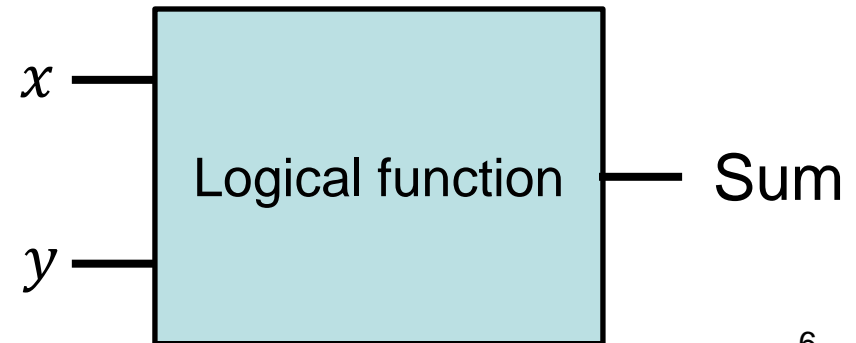
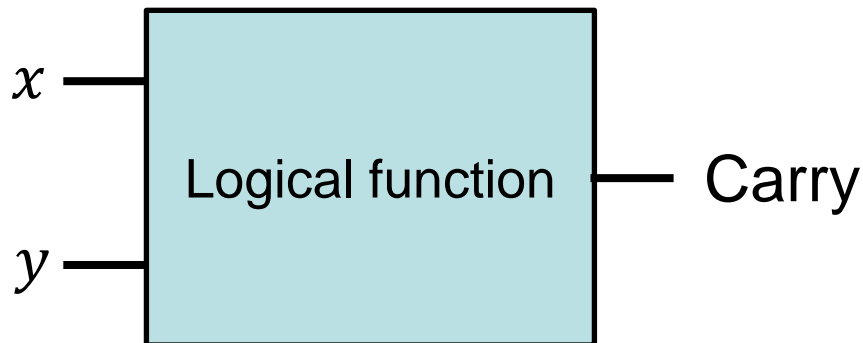
$$1 + 0 = 01$$

$$1 + 1 = 10$$

Carry

Sum

- Treat them separately!



Relation btw x , y , and sum

- Concentrate on the sum-bit.
 - A table can be made.
 - It is called a **truth table**.

x	y	sum
0	0	0
0	1	1
1	0	1
1	1	0

- Yes, it is the exclusive OR, $x \text{ XOR } y$.

Relation btw x , y , and carry

- Concentrate on the carry-bit.
 - A table can be made, again.

x	y	carry
0	0	0
0	1	0
1	0	0
1	1	1

- Yes, it is the AND operation, x AND y

After all,

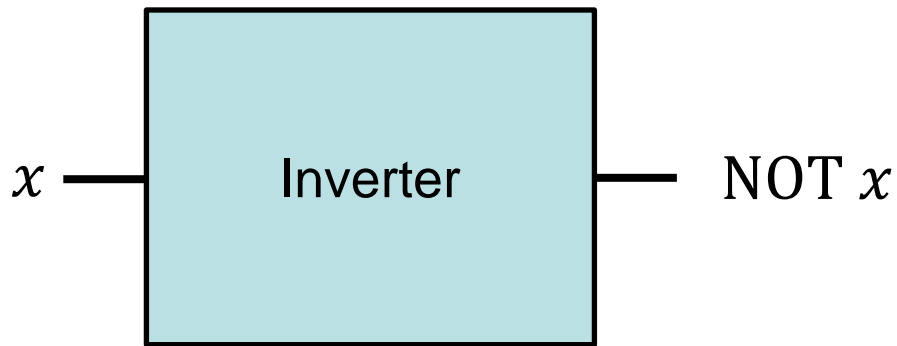
- As much as we have AND, OR, and NOT gates, we can implement any Boolean function.
 - With NAND, NOR, and NOT gates, we can, too.



(Google Images)

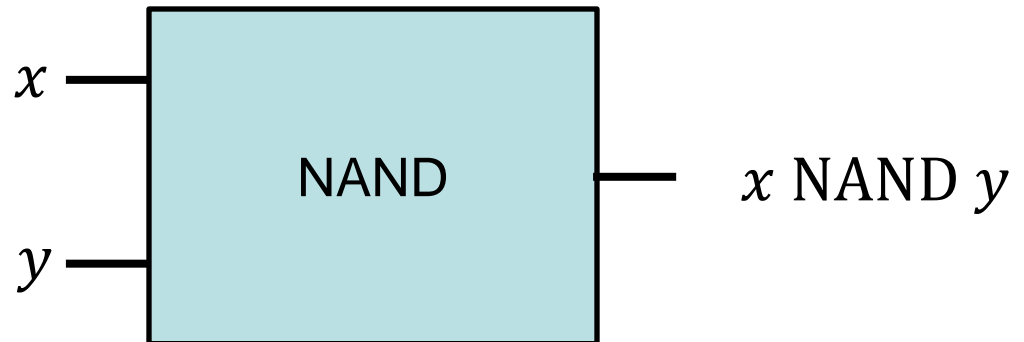
Inverter and NAND

- NOR can be implemented similarly.



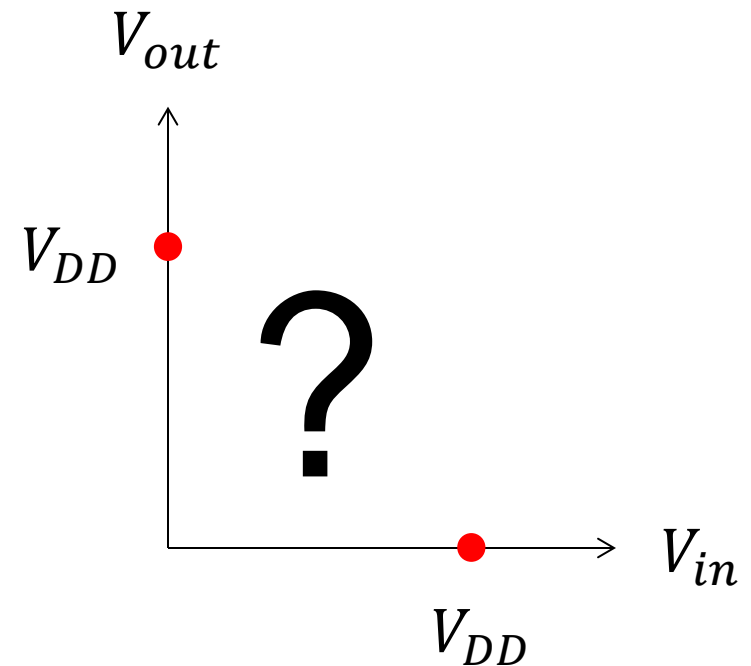
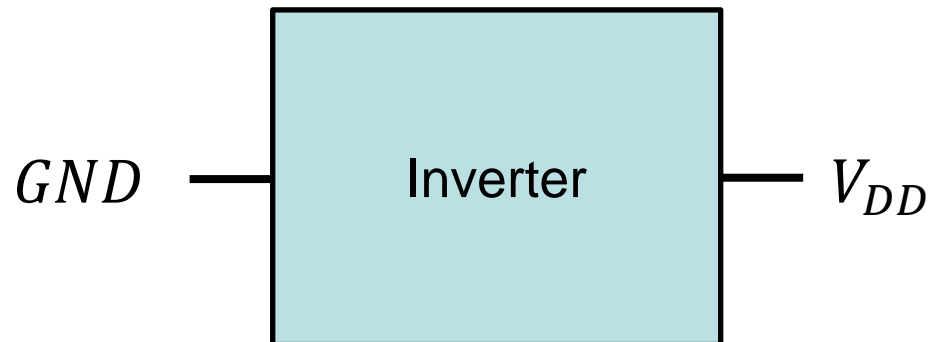
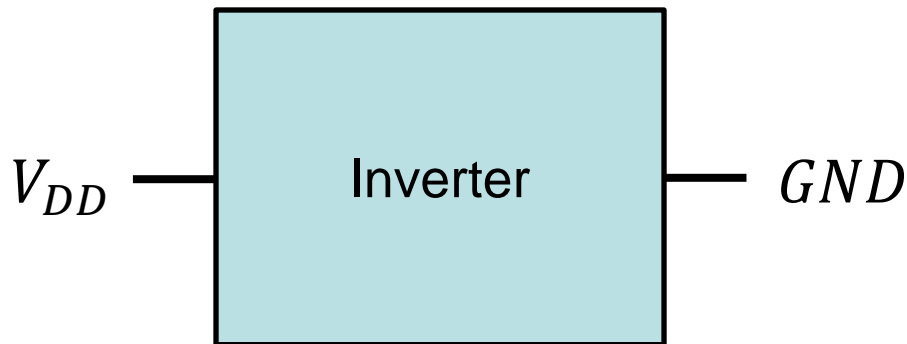
x	NOT
0	1
1	0

x	y	NAND
0	0	1
0	1	1
1	0	1
1	1	0



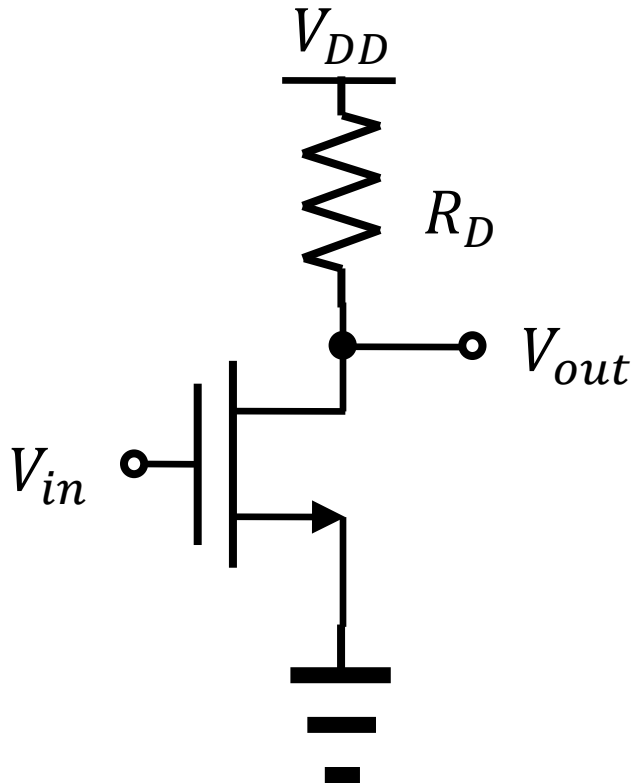
In circuit,

- How can we represent 0 and 1?
 - V_{DD} is assigned to the logical value, 1.
 - GND is assigned to the logical value, 0.



Inverter

- When the output becomes 0?
 - Only when the input is high.
 - *You have seen it before!*



V_{in}	V_{out}
0	1
1	0

Voltage transfer characteristic

- When $V_{in} < V_{TH}$,
 - Trivially, $V_{out} = V_{DD}$.
- When V_{in} is slightly larger than V_{TH} , the NMOSFET is in the saturation region.

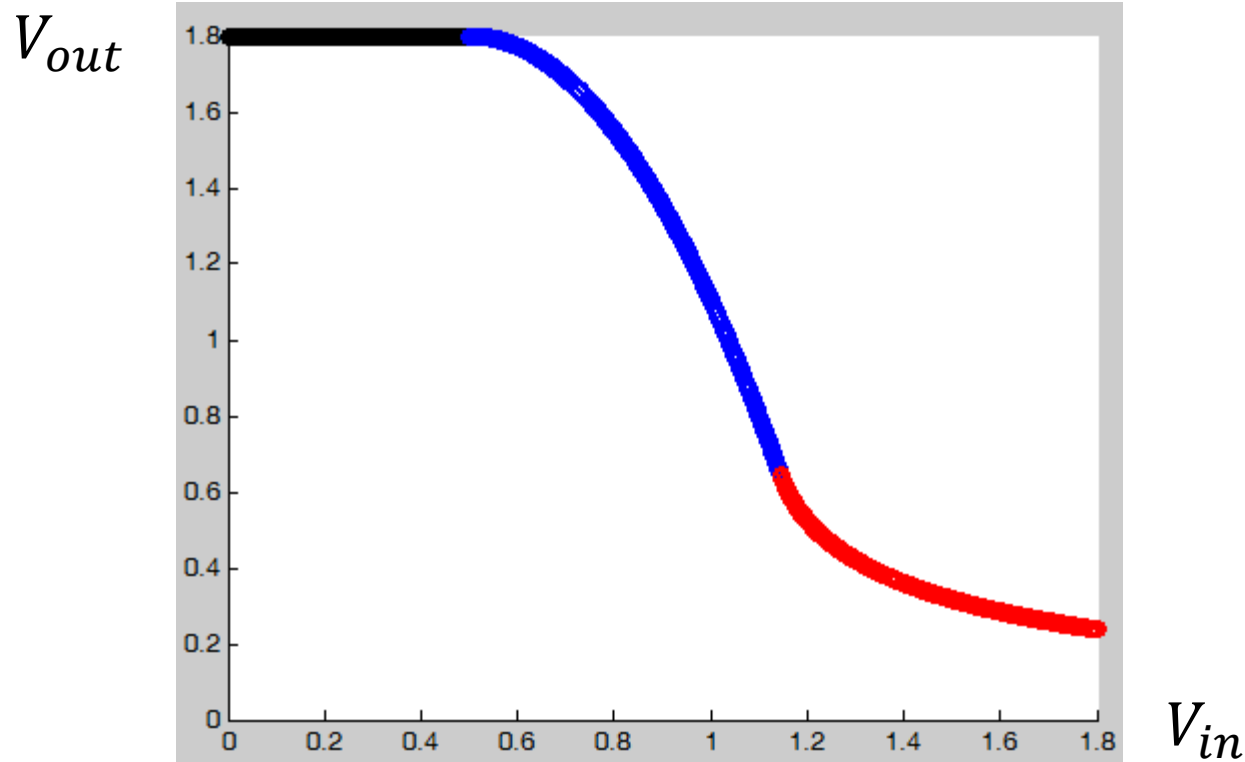
$$V_{out} = V_{DD} - I_D R_D$$
$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})^2$$

- When V_{in} is further increased, the NMOSFET is in the triode region.

$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} R_D [2(V_{in} - V_{TH})V_{out} - V_{out}^2]$$

Draw it! (1/2)

- The parameters used in Example 17. 14 without modification.
 - $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH} = 0.5 \text{ V}$, $\frac{W}{L} = \frac{10}{0.18}$, $R_D = 1\text{k}\Omega$ and $V_{DD} = 1.8 \text{ V}$



Draw it! (2/2)

- With a wider NMOSFET

– $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH} = 0.5 \text{ V}$, $\frac{W}{L} = \frac{50}{0.18}$, $R_D = 1\text{k}\Omega$ and $V_{DD} = 1.8 \text{ V}$

