Lecture1: Introduction

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Welcome!

- Electronic Circuits
  - Code: EC3207
  - Lecture 3, no experiment, credit 3
- Prerequisite
  - Electric Circuit Theory
- Instructor, Sung-Min Hong
  - School of Information and Communications (정보통신공학부)

Textbook

- Fundamentals of Microelectronics
  - An excellent book by B. Razavi
  - Second edition

- Coverage in this course
  - CMOS-oriented lecture!

Lecture

- Basic information
  - Mon/Wed 13:00-14:15, GIST SIC B, Room 206
  - Handwriting on blackboard(/chalkboard)
  - Supplemented by slides (Just like this!)

- G-Class will be actively used.
  - Please check your e-mail address!

Office hour

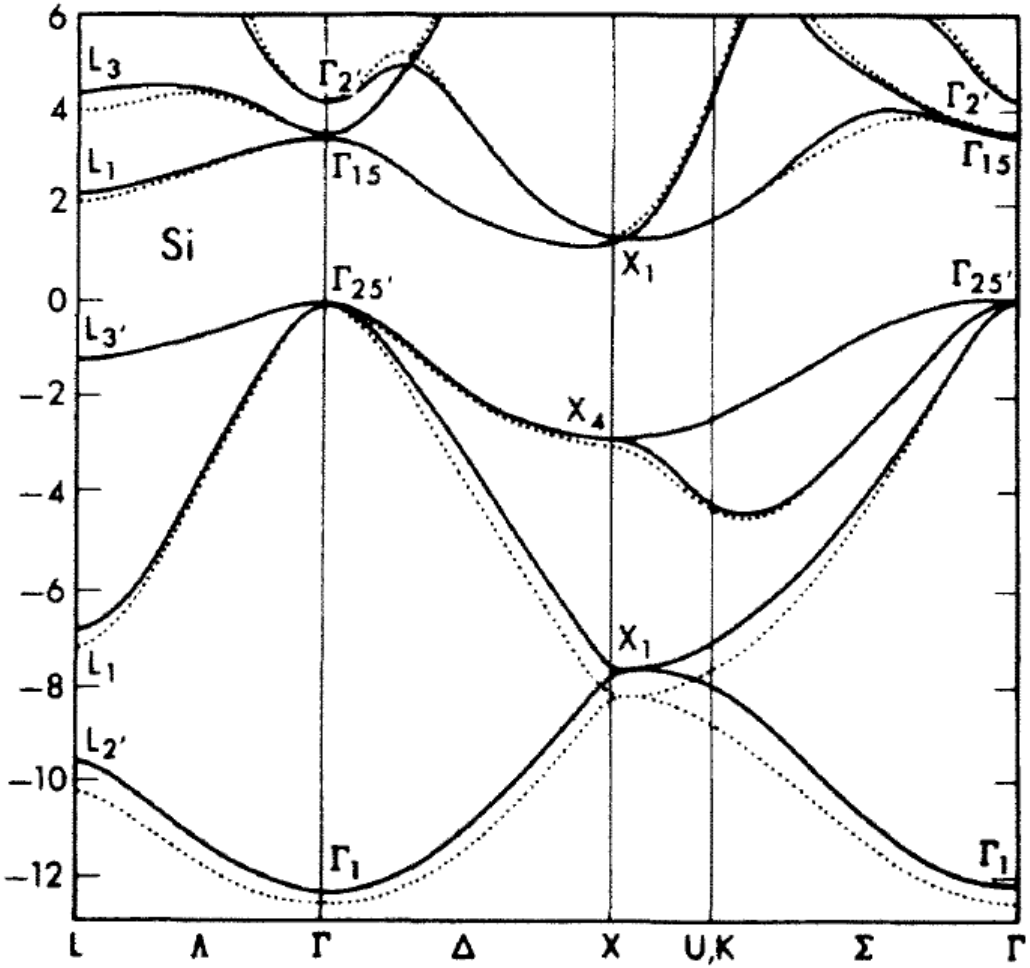
- Office hour
  - My office is located at Room 208, SIC Building A.
  - Special sessions are available by appointment.

Evaluation

- Attendance (10%)
  - In addition to 10%, there is the “2/3 rule”, dictated by the college.
- Homework (30%)
  - Every week (10 times?) & EDISON
- Midterm (30%)
- Final (30%)
  - Covering the whole semester
- For students from other concentrations
  - No S/U registration
  - No advantage/disadvantage rule

Highlights (1)

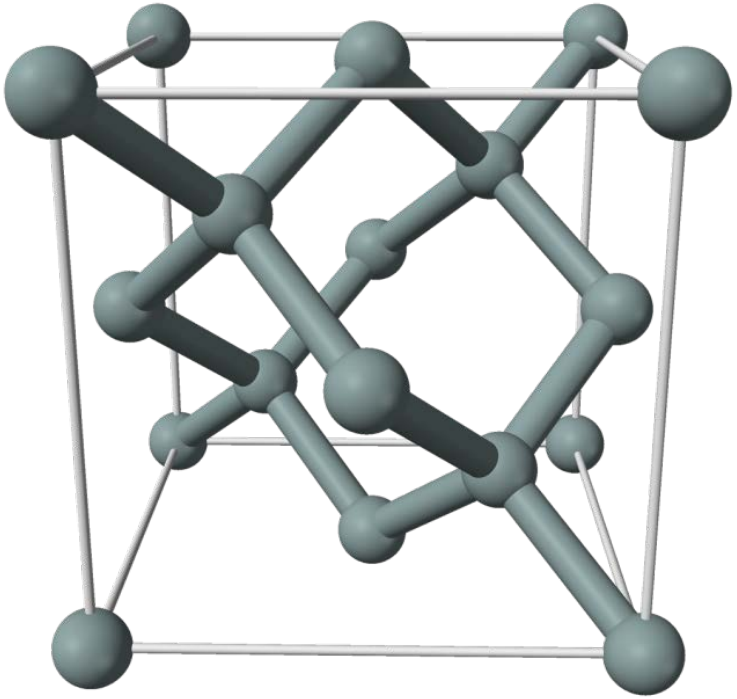
- Band structure of silicon (Band gap ~ 1.12eV)



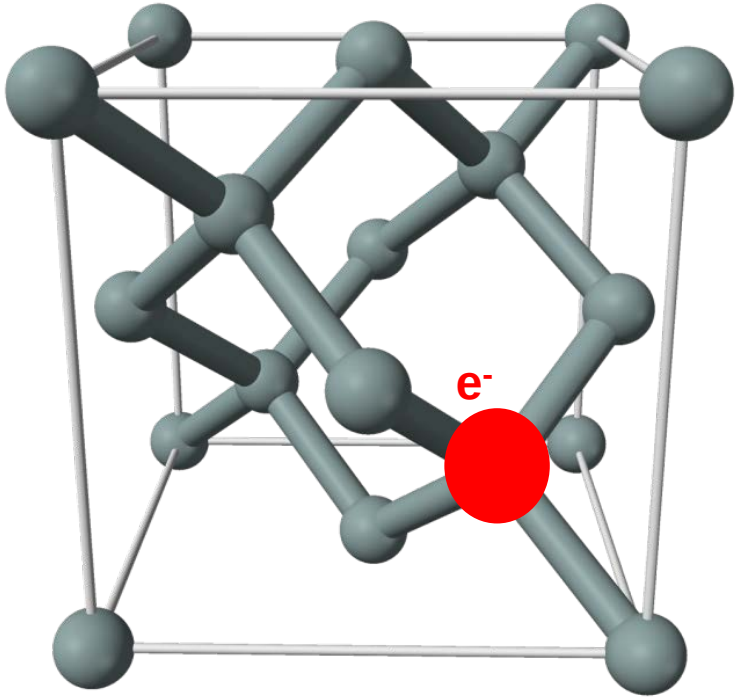
(J. R. Chelikowsky and M. L. Cohen,
PRB, vol. 14, p. 556, 1976)

Highlights (2)

- The phosphorus atom has 5 valence electrons.
  - Additional electron (e^- in the right figure) serves as a charge carrier.



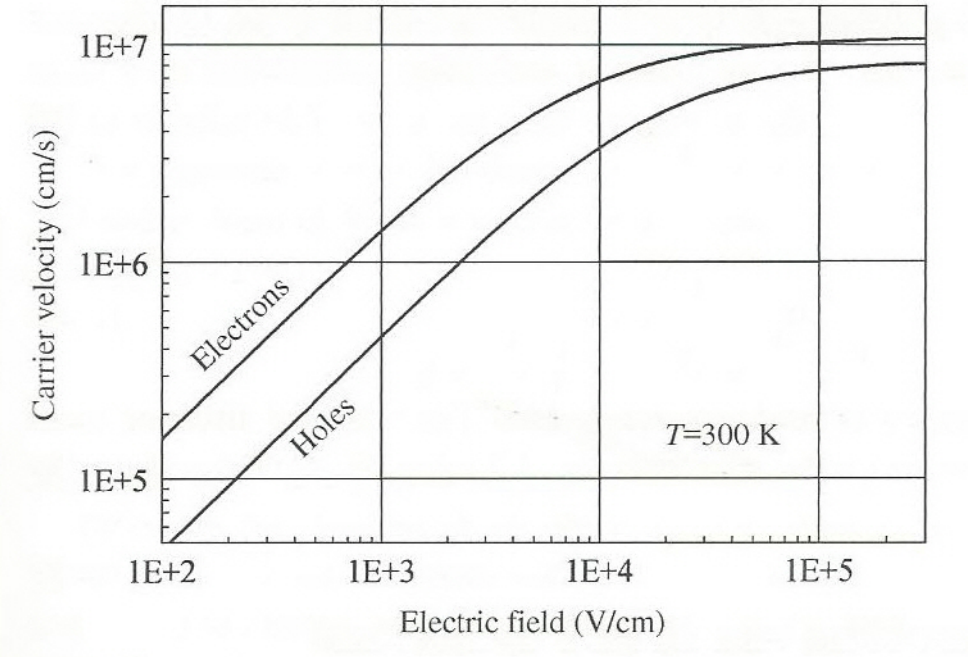
Pure silicon



Silicon with “impurity” atom
(For example, phosphorus)

Highlights (3)

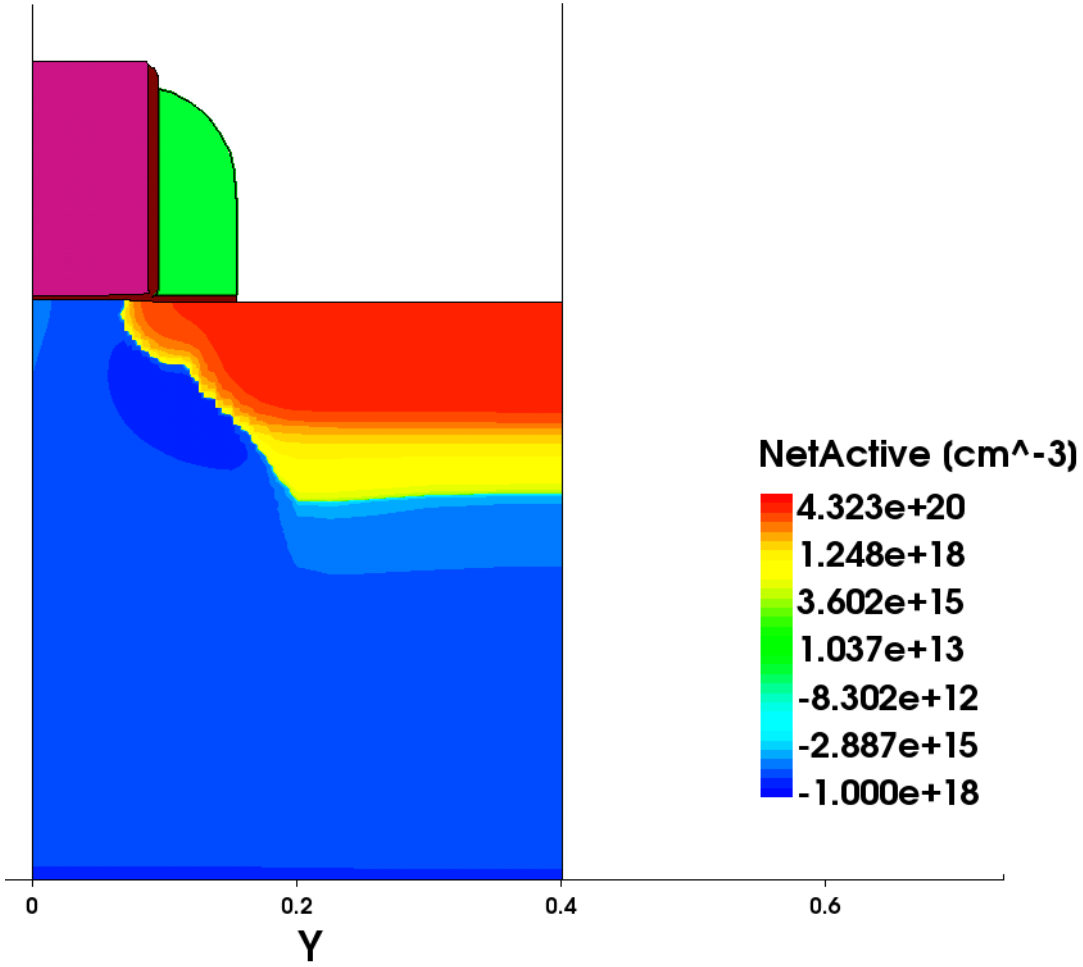
- Directly affects the DC current
  - At low electric fields, the linear relationship is valid.
  - At high electric fields, the velocity saturation starts to occur. The saturation velocity of Si is about 10^7 [cm/sec].



Velocity-field relationship in Si at 300K
(Y. Taur and T. H. Ning, Fundamentals of modern VLSI devices)

Highlights (4)

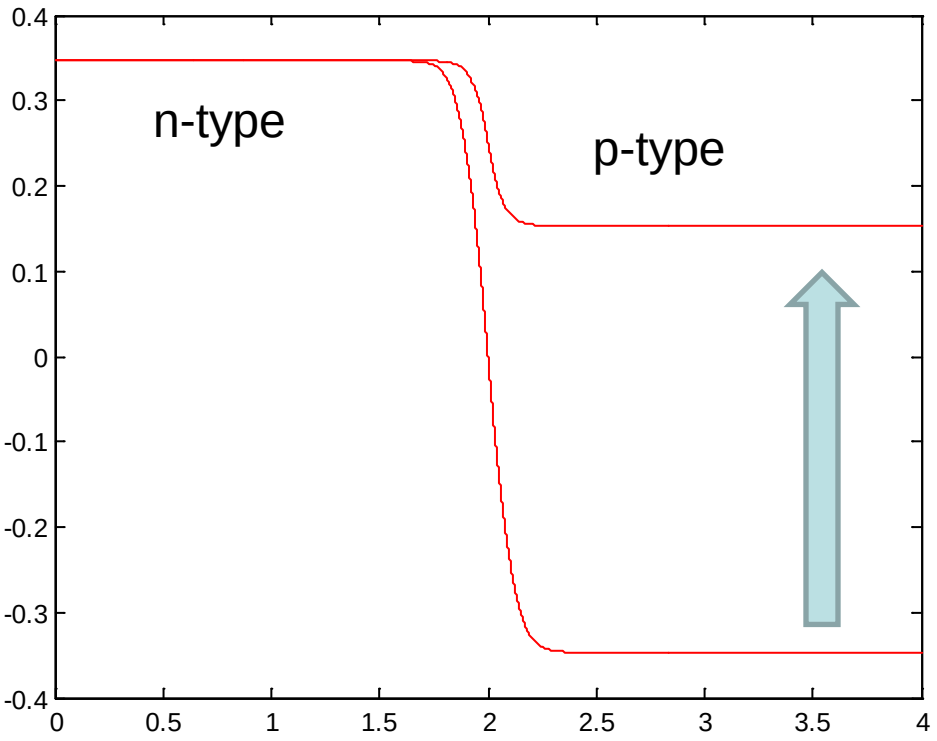
- Ion implantation for source/drain formation
  - Arsenic, dose=5e15<cm-2>, energy=<40keV>



Highlights (5)

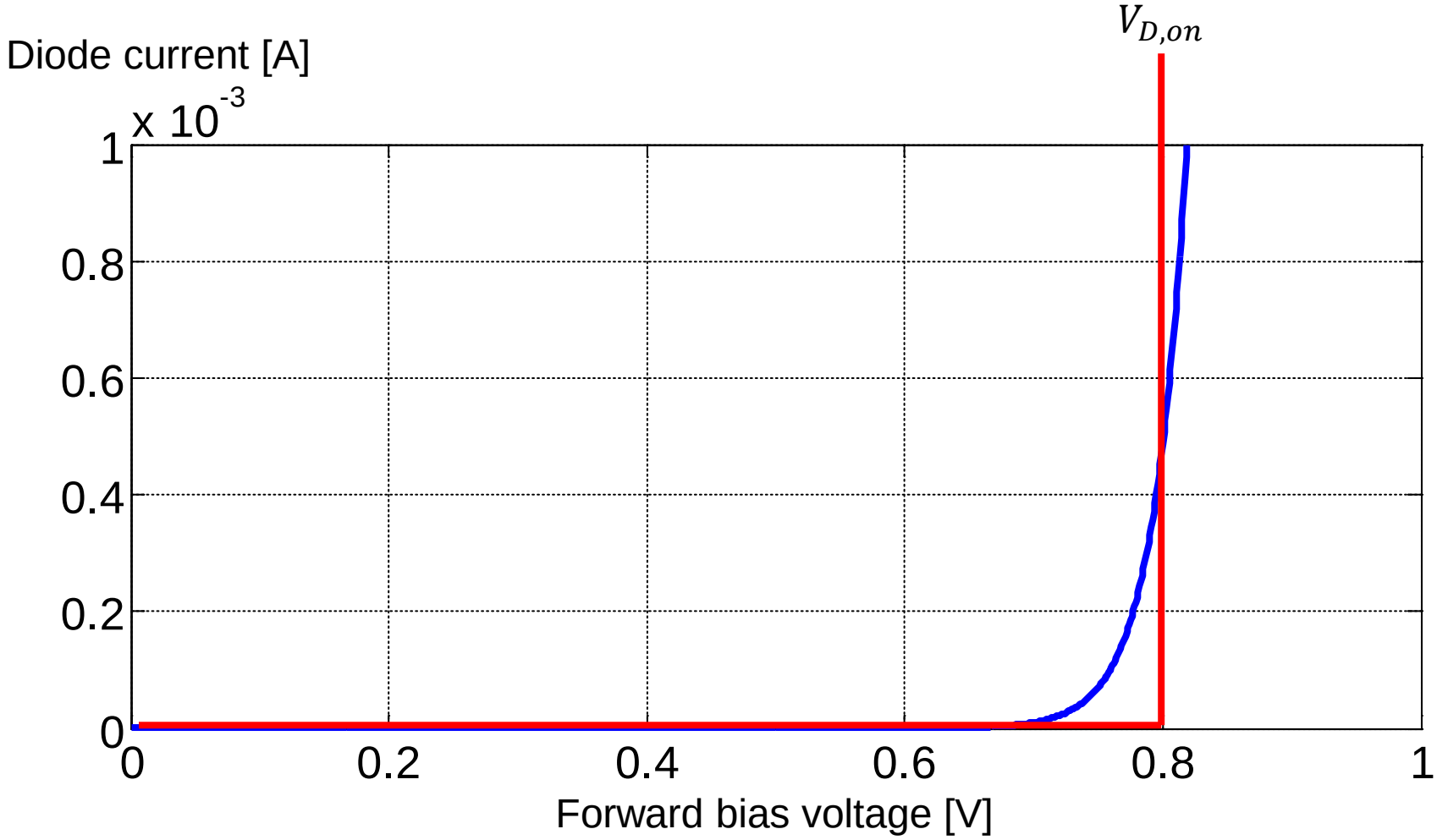
- Forward bias
  - We can easily guess that the depletion width will be reduced.
  - Potential barrier is lowered. (Equilibrium and 0.5 V)

Electric potential [V]



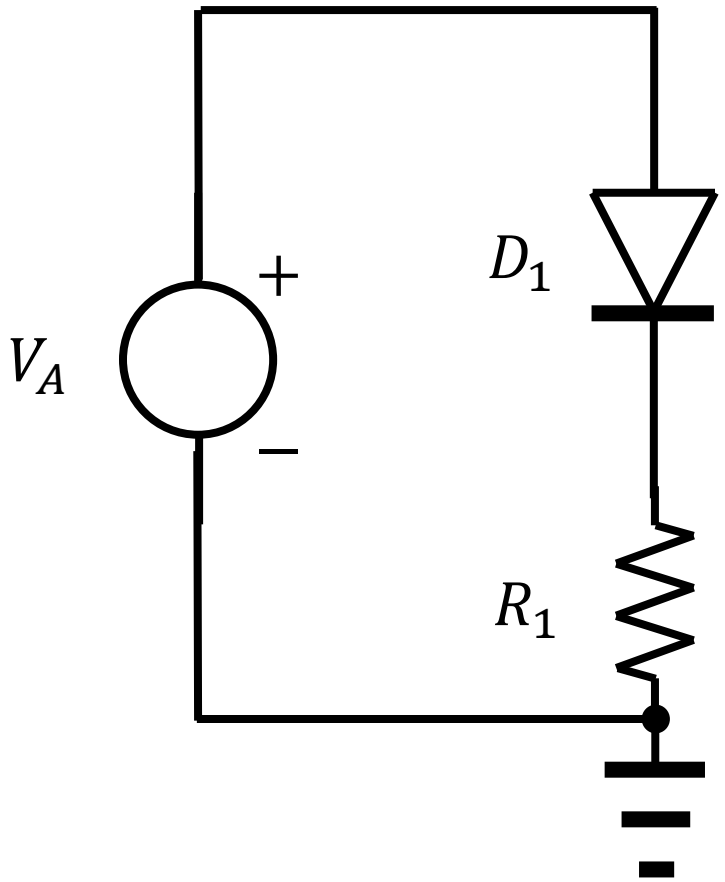
Highlights (6)

- Idealized model



Highlights (7)

- A diode-resistor combination



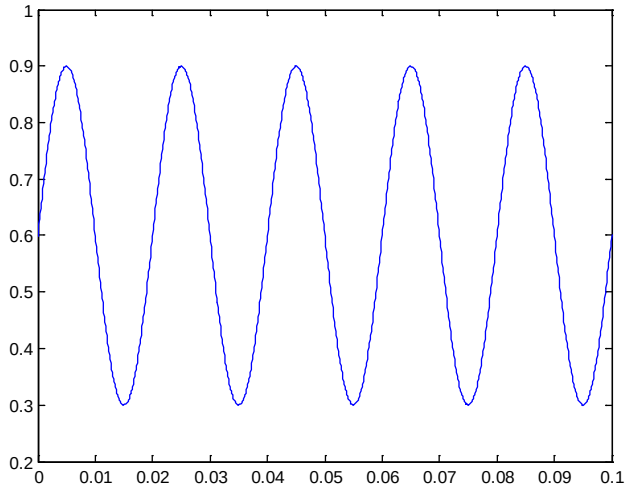
🡸 Consider two cases, $V_A > 0$ and $V_A < 0$.
🡸 Draw the IV curve.

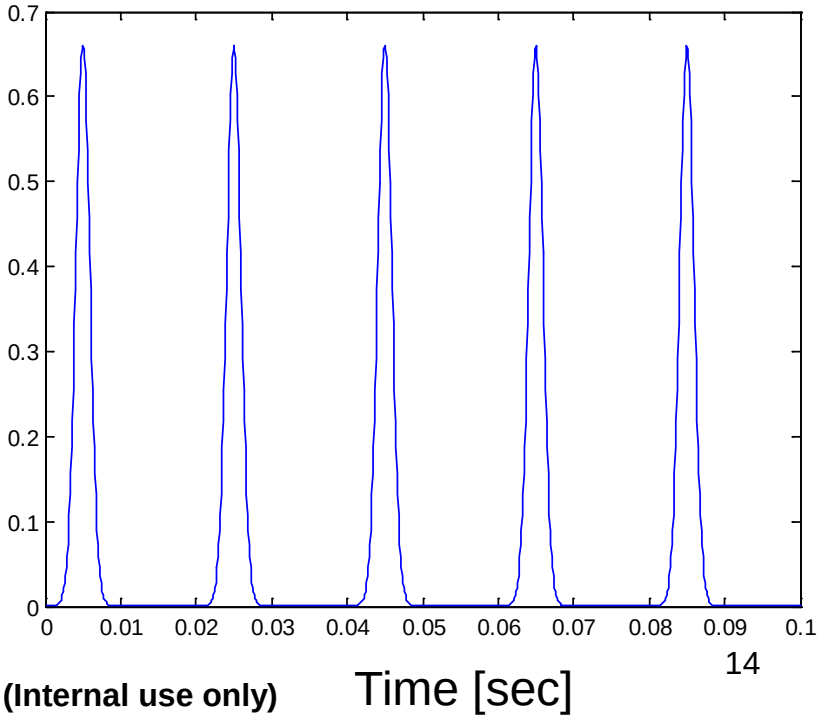
Highlights (8)

- A system (You know what it actually represents.)

$$V_{in} \longrightarrow \boxed{I_{out} = I_s \exp \frac{V_{in}}{V_T}} \longrightarrow I_{out}$$

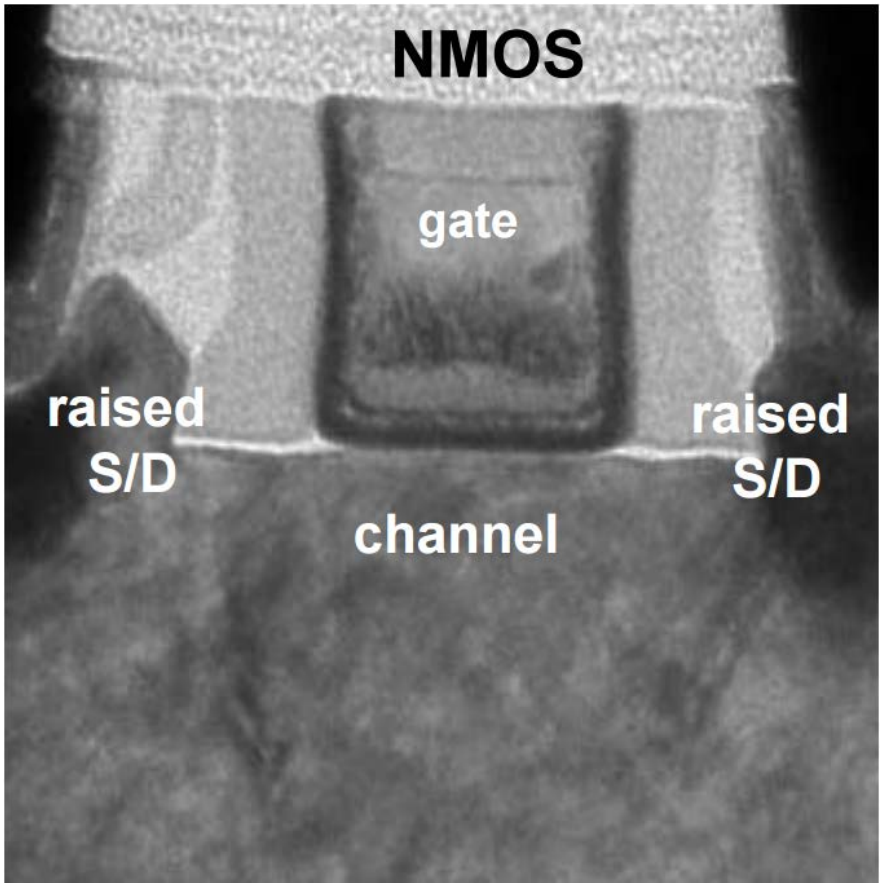
- When $V_{in} = 0.6 + 0.3 \sin 2\pi f t$,
  - Certainly, nonlinear!





Highlights (9)

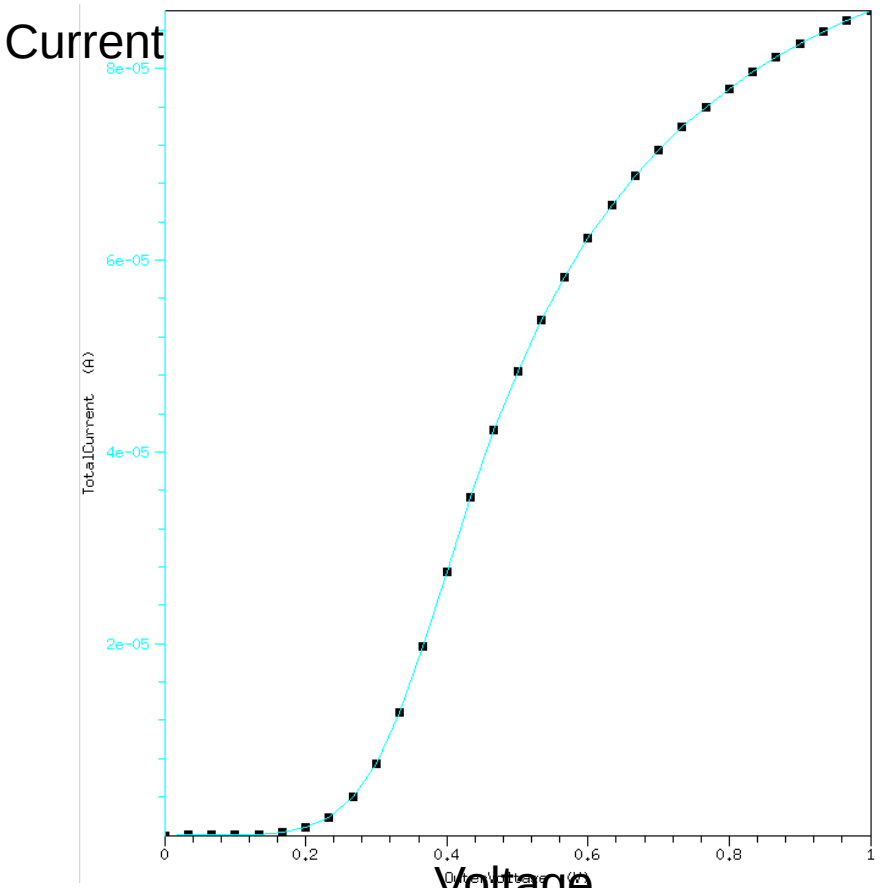
- TEM image of a MOSFET
  - 32nm node
  - (somewhat old…)



(Packan et al., IEDM 2009)

Highlights (10)

- Threshold behavior
  - Physical reason? (*See p. 248*)



A door threshold and a dog (Google images)

🡸 A typical Id-Vg curve

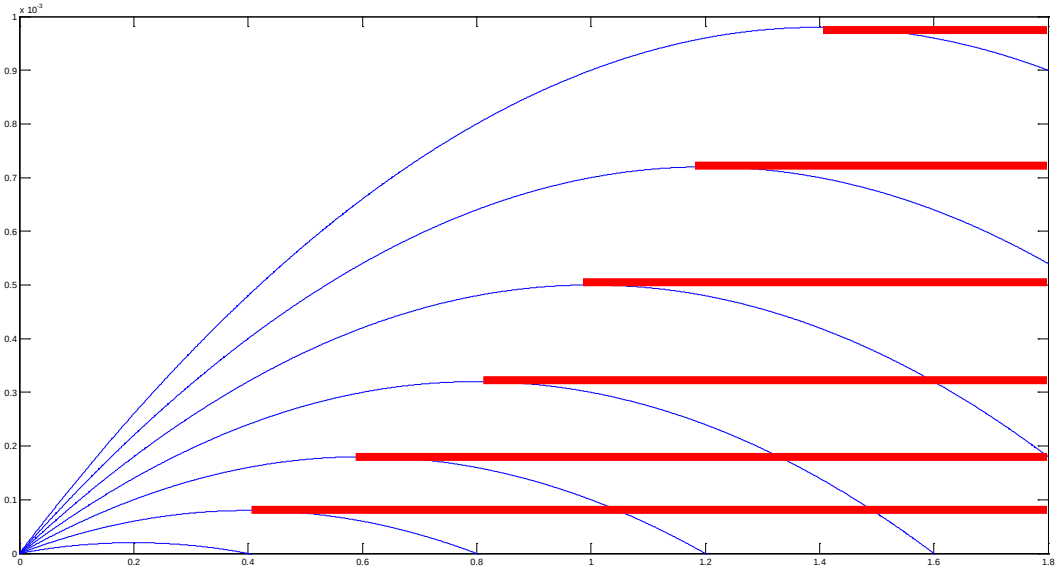
Highlights (11)

- Current usually increases as the voltage increases…
- Recall (6.3).

$$Q = WC_{ox}[V_G - V(x) - V_{TH}] \qquad (6.3)$$

  - What happens when $V(x) = V_G - V_{TH}$?
  - "Saturation region"

Current

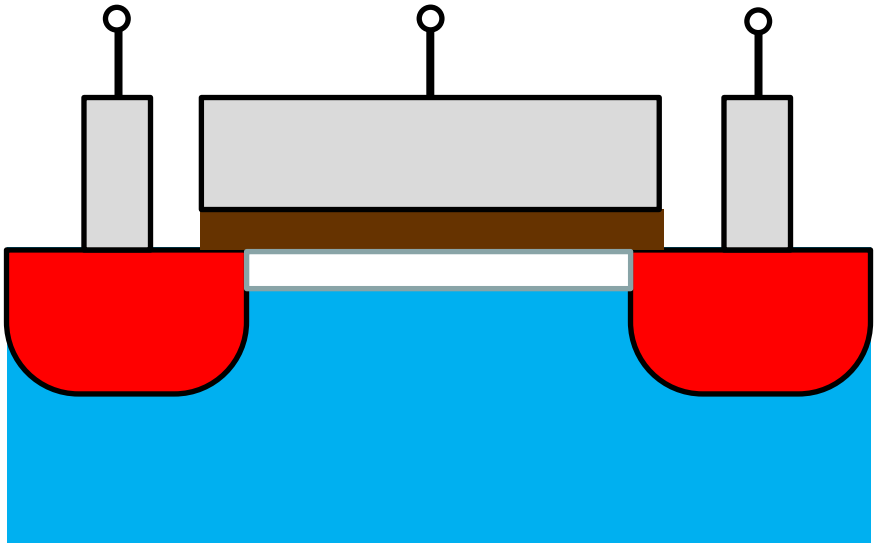


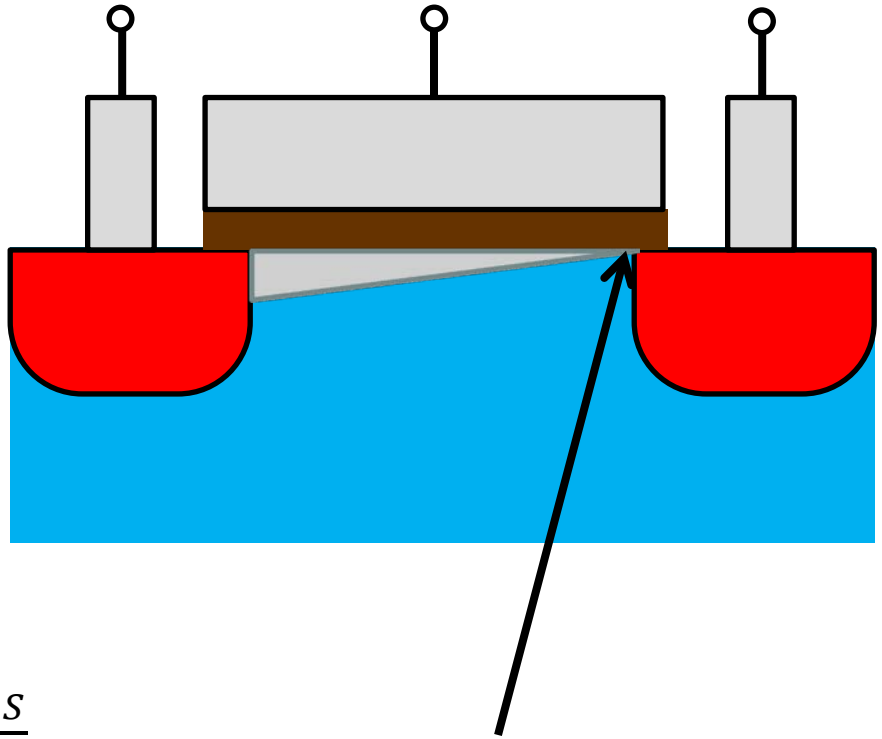
Voltage

🡸 Instead, the current is saturated. (Red lines)

Highlights (12)

- Channel length modulation





- Output resistance?

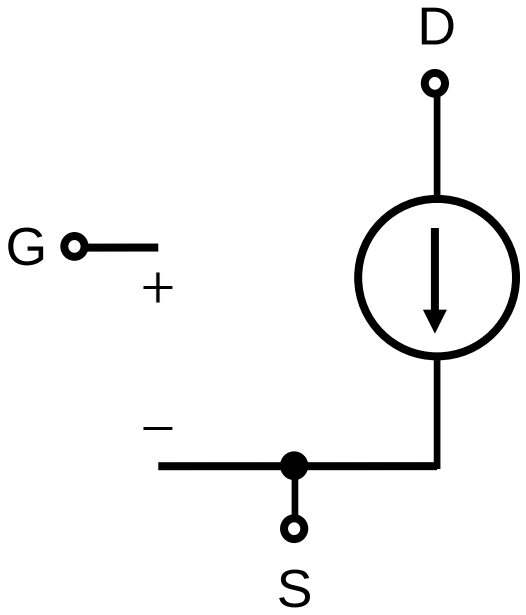
$$r_O = \frac{\Delta V_{DS}}{\Delta I_D}$$

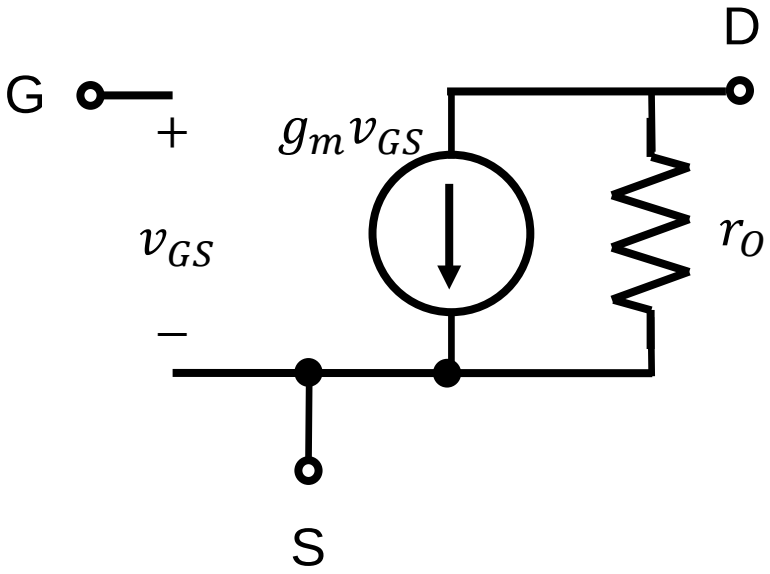
Recall that

$$Q = WC_{ox}[V_G - V(x) - V_{TH}]$$

Highlights (13)

- The large-signal model is complete (within its accuracy limitation).
  - But, for small-signal analysis, it is convenient to have the small-signal model.





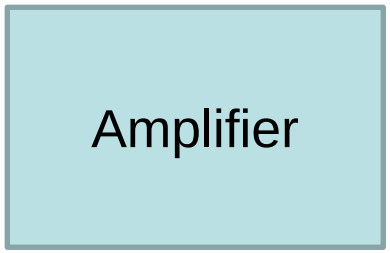
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

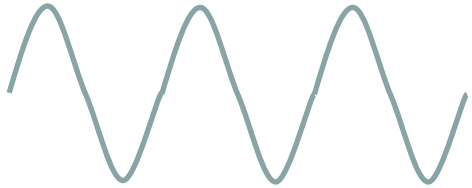
What is g_m and r_O?

Highlights (14)

- Signal amplification
  - Usually, signals are “weak.” (in the μV or mV range)
  - It is too small for reliable processing.
  - If the signal magnitude is made larger, processing is much easier.

“Weak” signal



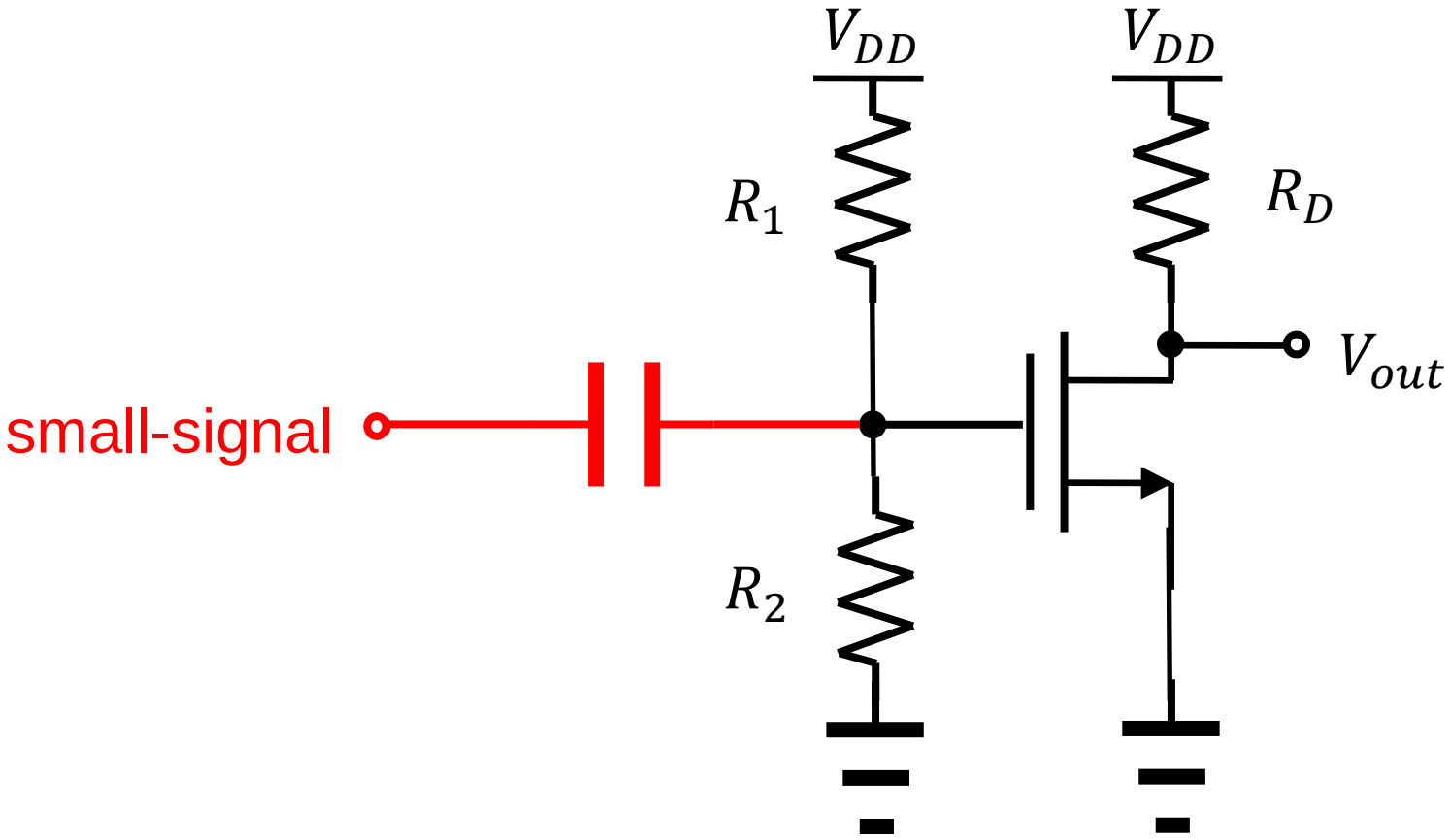


“Strong” signal

- Desirable properties
  - Low power consumption
  - High speed operation
  - Low noise

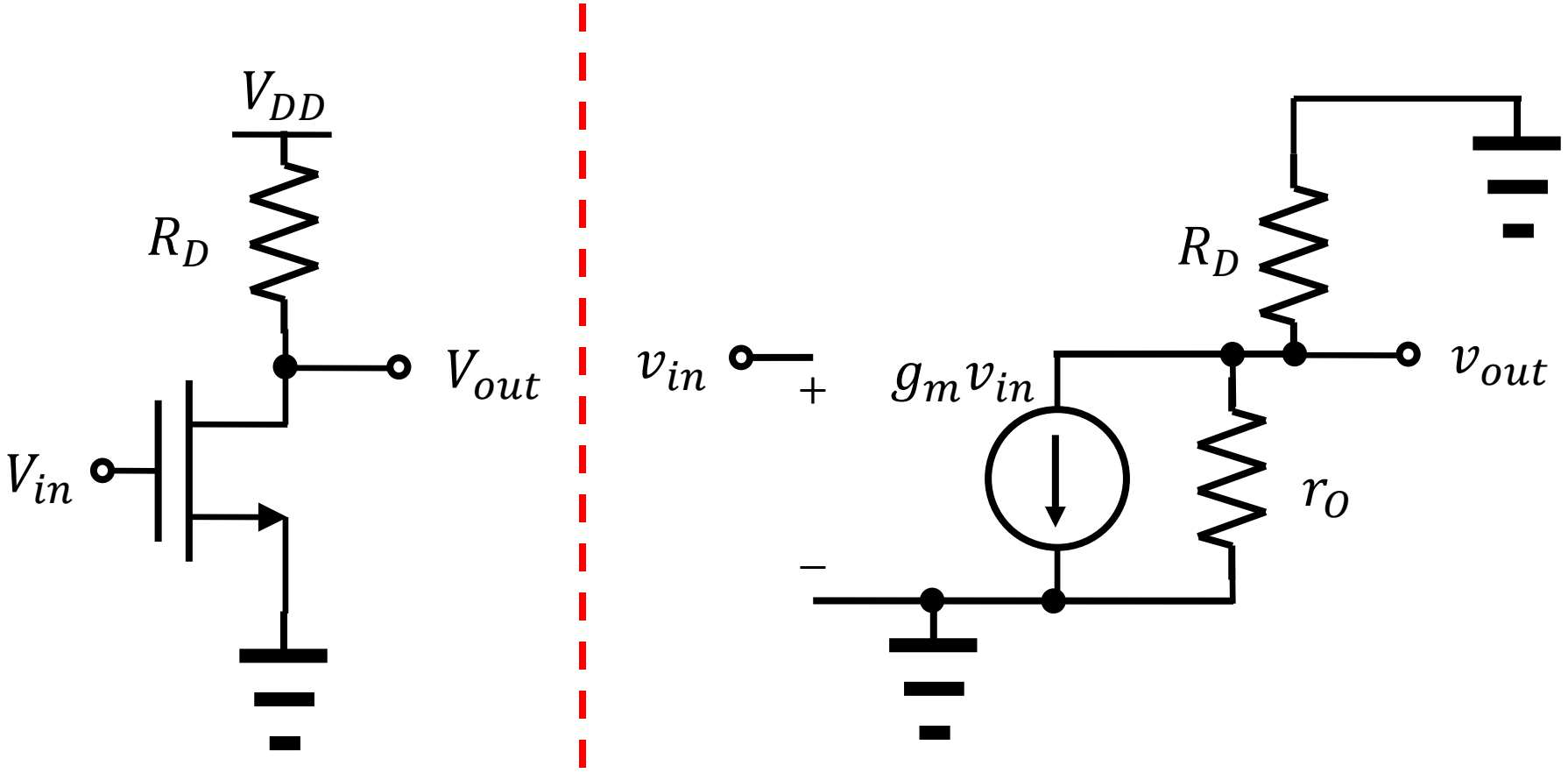
Highlights (15)

- How to apply the small-signal input
  - Use a capacitor!



Highlights (16)

- Let's draw the small-signal model together!



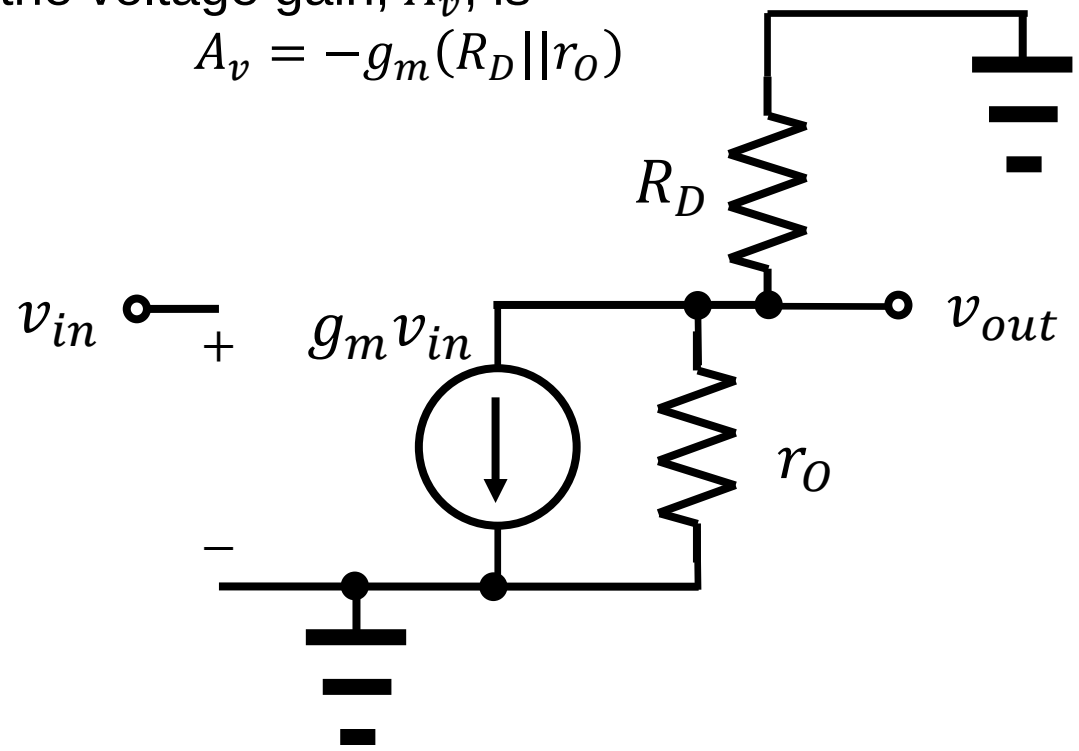
Highlights (17)

- Now, calculate the v_{out}.
  - KCL for the v_{out} node gives

$$v_{out} = -g_m(R_D||r_O)v_{in}$$

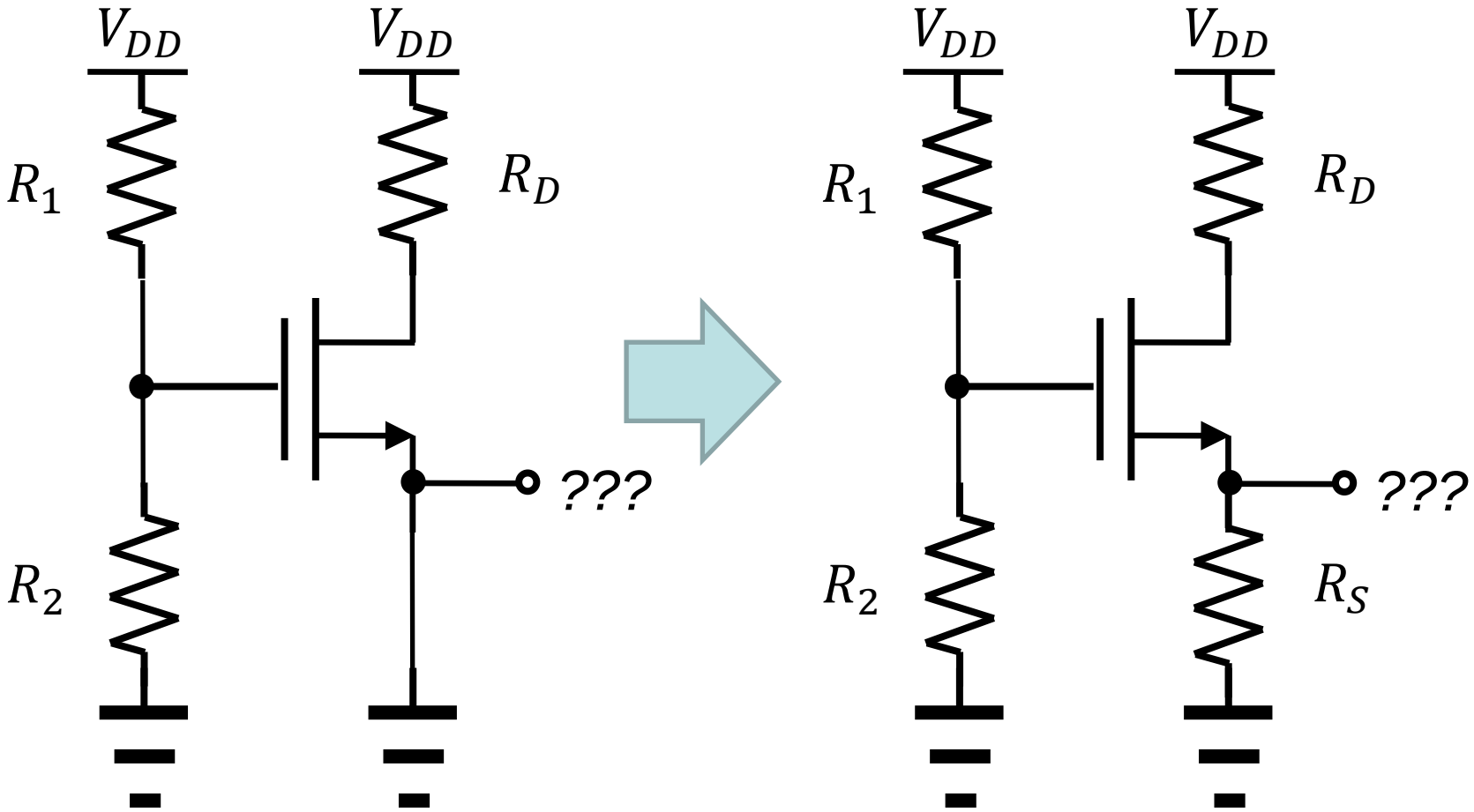
  - Therefore, the voltage gain, A_v, is

$$A_v = -g_m(R_D||r_O)$$



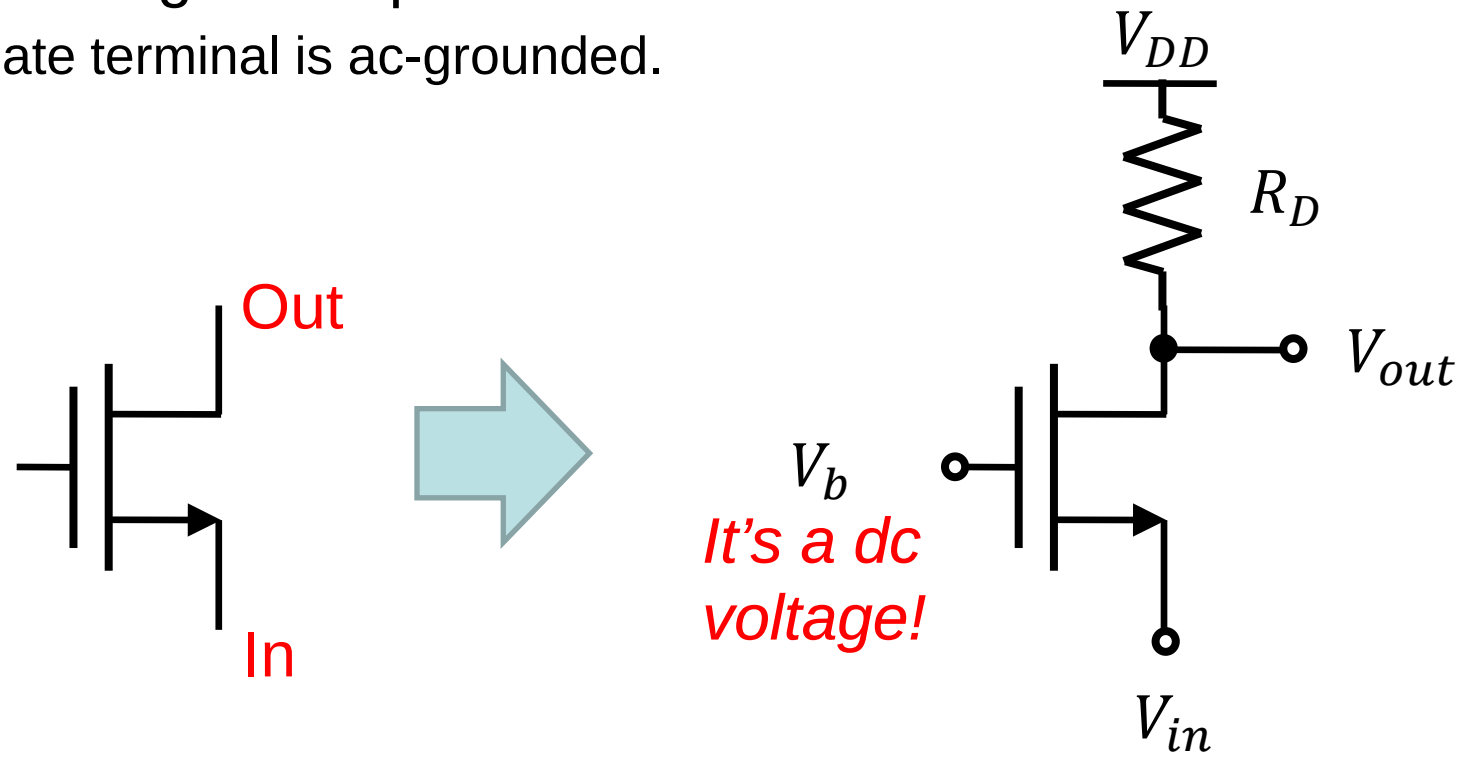
Highlights (18)

- A resistor placed in series with the source terminal



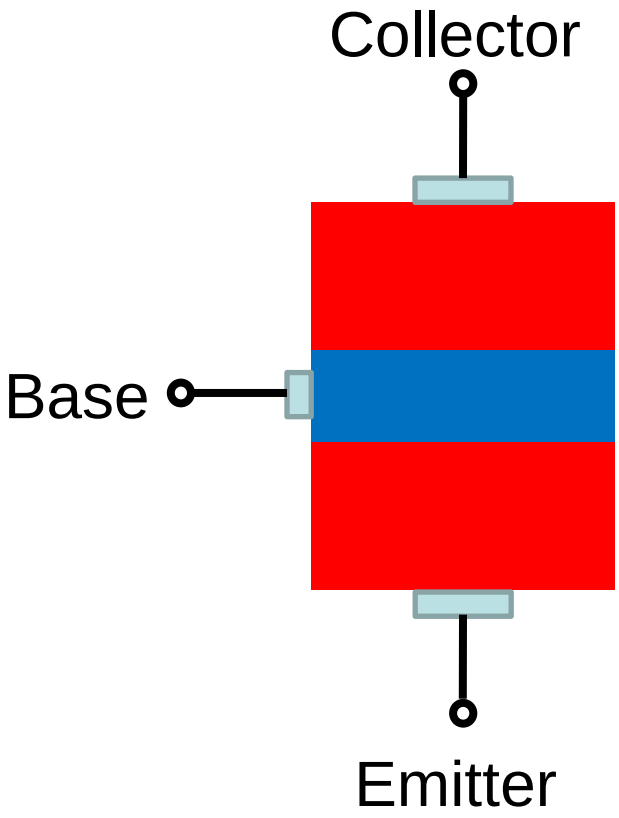
Highlights (19)

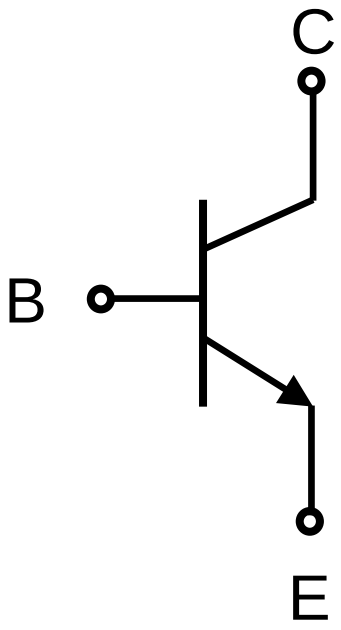
- Why do we study other amplification topologies?
  - Different circuit properties
- Common-gate amplifier
  - Gate terminal is ac-grounded.



Highlights (20)

- Bipolar junction transistor (BJT)
  - Three doped regions forming a sandwich





Highlights (21)

- IV curves for the BJT
  - Collector and base currents

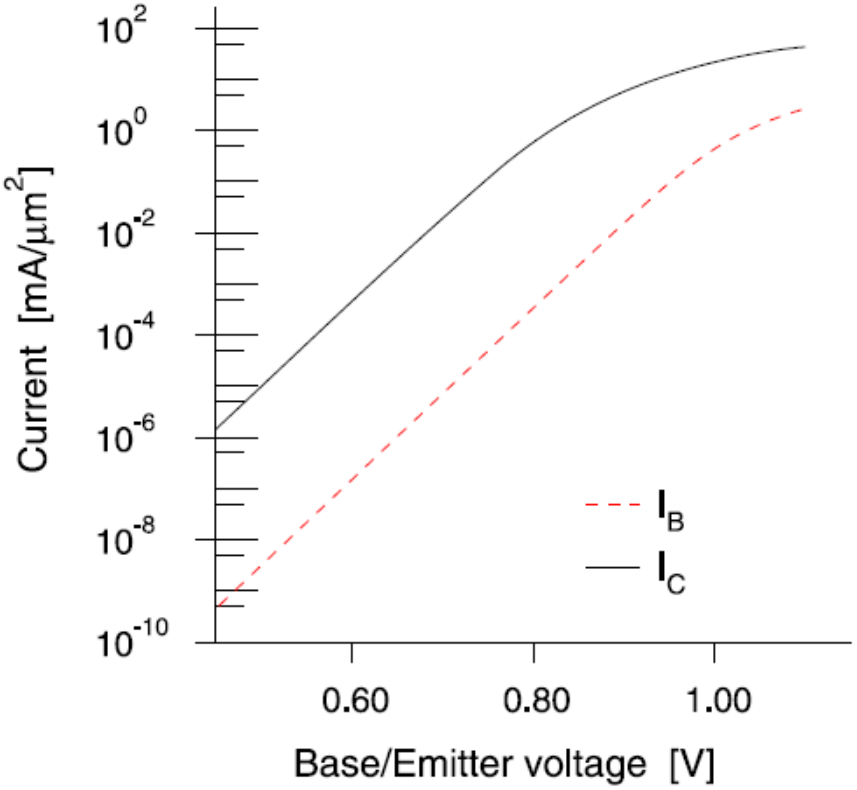
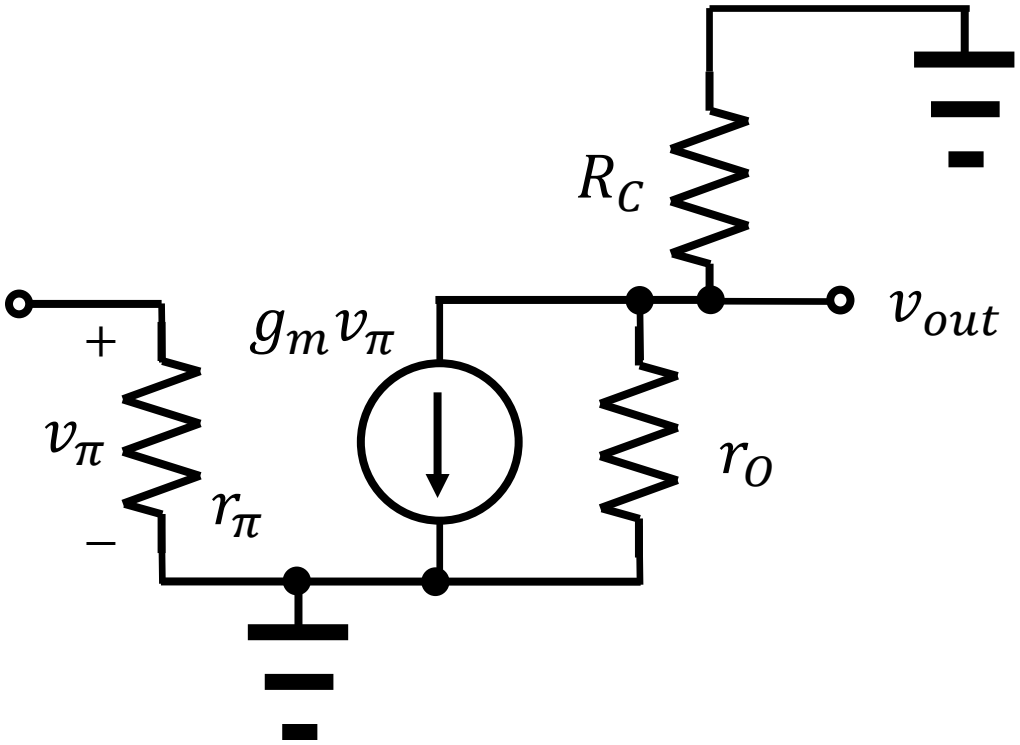


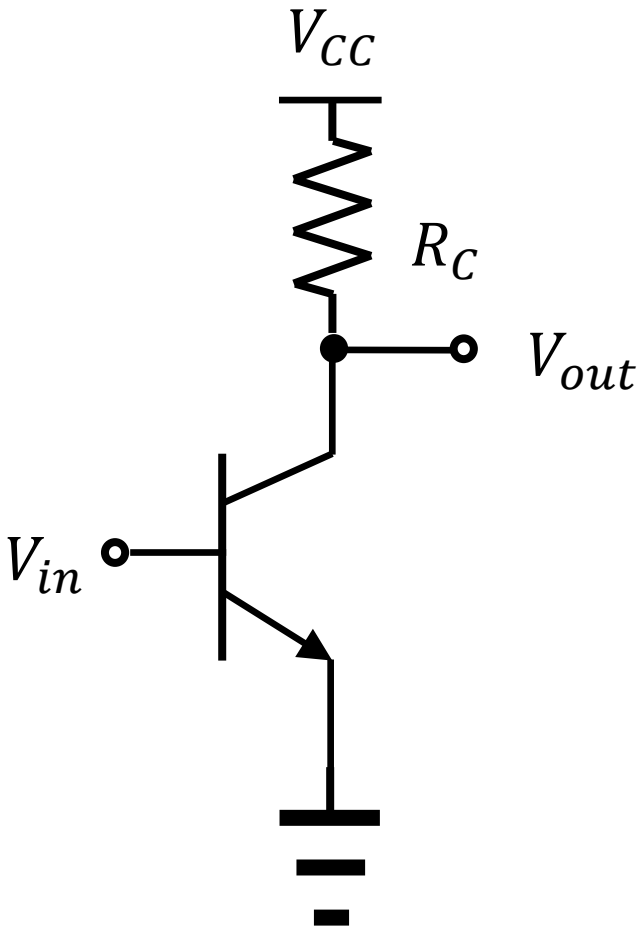
Fig. 19 Gummel plot. $V_{CB} = 0.1$ V

Simulated Gummel plot of a HBT
(Taken from Hong, JCE, vol. 8, p. 225, 2009)

Highlights (22)

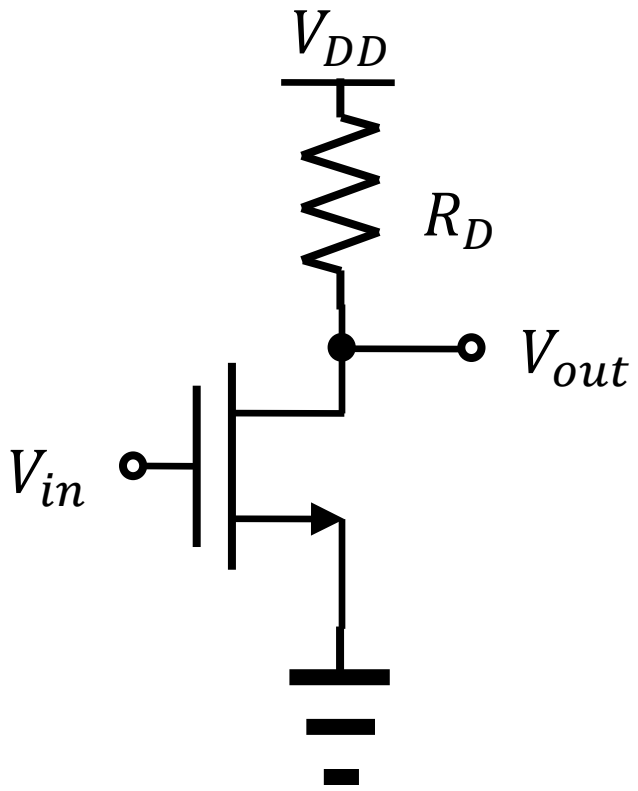
- You can easily imagine that
  - There is a common-emitter configuration.





Highlights (23)

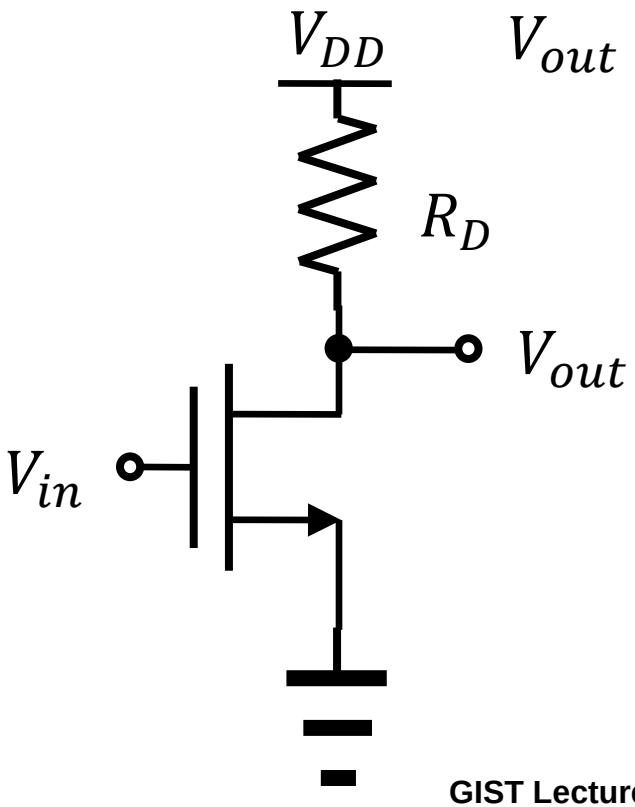
- When the output becomes 0?
  - Only when the input is high.
  - *You have seen it before!*

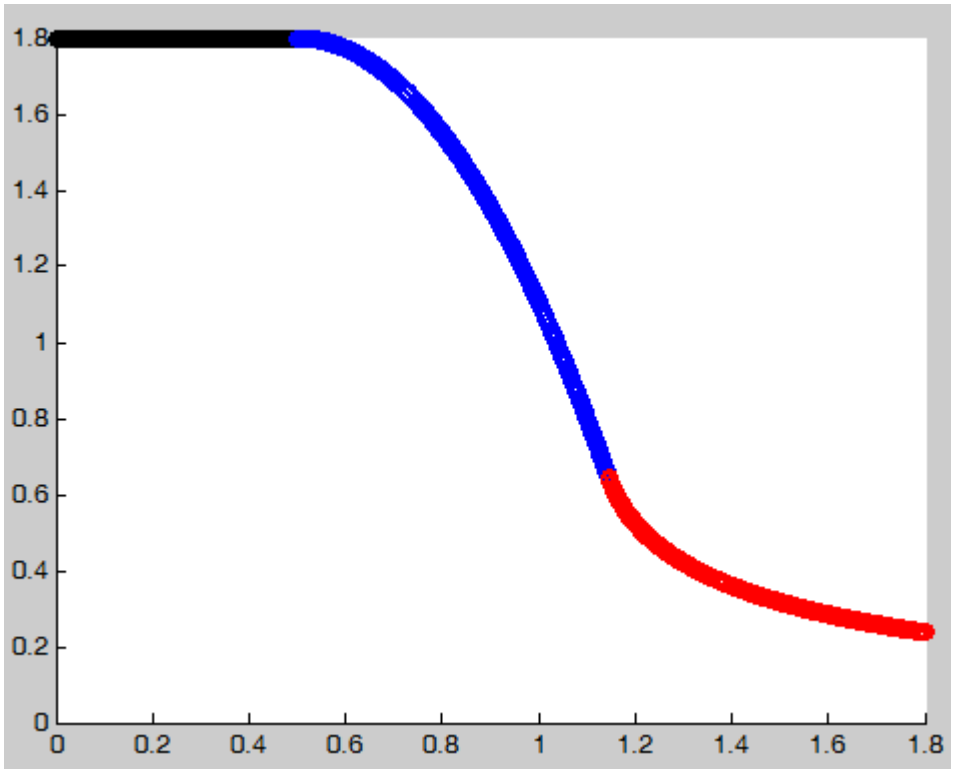


Vin	Vout
0	1
1	0

Highlights (24)

- Numeric calculation can be done with a binary system.
- Inverters and NAND gates are important.
- And, the NMOS inverter was introduced.



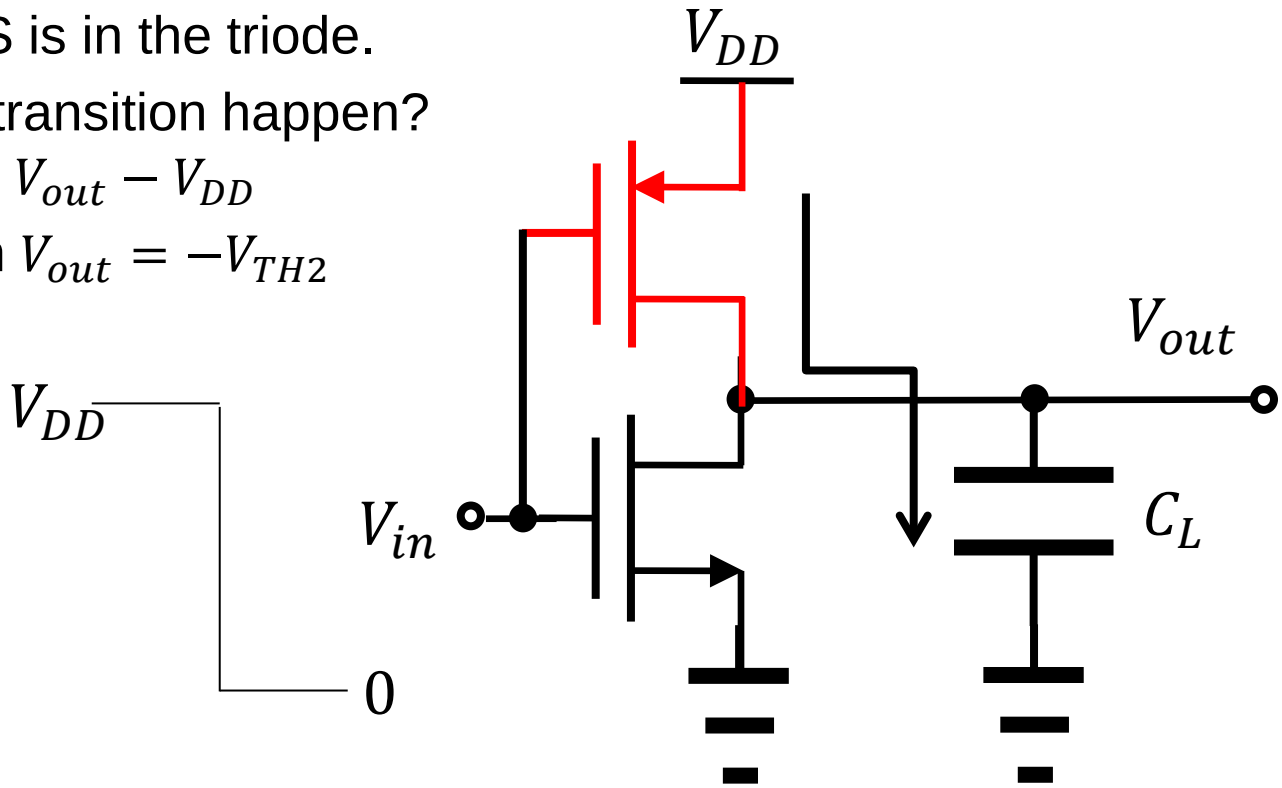


Highlights (25)

- Guess the charging speed.
  - In other words, the PMOS current ($I_{PMOS} = C_L \frac{dV_{out}}{dt}$)
  - At the beginning, the PMOS is in the saturation.
  - Later, the PMOS is in the triode.
  - When does the transition happen?

$V_{in} - V_{DD} - V_{TH2} = V_{out} - V_{DD}$

  - Therefore, when $V_{out} = -V_{TH2}$



Highlights (26)

- Load capacitor of 20 fF
  - 1 GHz signal