MAX21100
User Guide

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1 Introduction

MEMS sensors are revolutioning the way people interact with everyday technology, making it easier and more user-friendly. Maximcan leverage its analog integration expertise to develop and manufacture new break-through MEMS sensors being smaller, lower power and more accurate than ever.

Owning the entire supply chain, Maxim brings its customers complete, reliable and cost-effective solutions, ensuring prompt time-to-volume and time-to-market to effectively address high-volume applications in consumer and industrial market segments.

Thanks to its leadership in analog integration and its manufacturing expertise in MEMS, Maxim is capable of high-volume production to meet the market's demands. Maxim manufacturing expertise and highest quality standards also guarantee high performance and product reliability.

Every MEMS sensor is tested and trimmed in factory so that for most consumer applications, no additional sensor calibrations are required. The end user can quickly verify the sensor's operation without physically tilting or rotating the sensor thanks to the built-in self-test feature, which allows accelerating the time-to-market for mass production.

The purpose of this technical article is twofold. The first section will provide a clear picture of the performances of Maxim MAX21100 6-axis Accelerometer and Gyroscope combo, as well as guidelines for its use in consumer and a comprehensive description of his unique features.

The second section will present the structure of the register file, the purpose of each field or every register and 2 examples about typical programming sequences.

Enjoy using the smallest, fastest and most accurate 6 axis IMU on the market!

2 MAX21100 Description

The MAX21100 is a motion processing solution with integrated 9-Axis Sensor Fusion using proprietary Motion Merging Engine for handset and tablet applications, game controllers, motion pointer remote controls, and other consumer devices.

The MAX21100 is the industry's first 6+3 DOF Inertial Measurement Unit with 9DoF Embedded Fusion Engine available in a 3x3 package and capable of working with a supply voltage as low as 1.71V.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit, which is trimmed to match at best the sensing element characteristics.

The internal Motion Merging Engine can be flexibly configured to get the most suitable accuracy-versus-power trade-off.

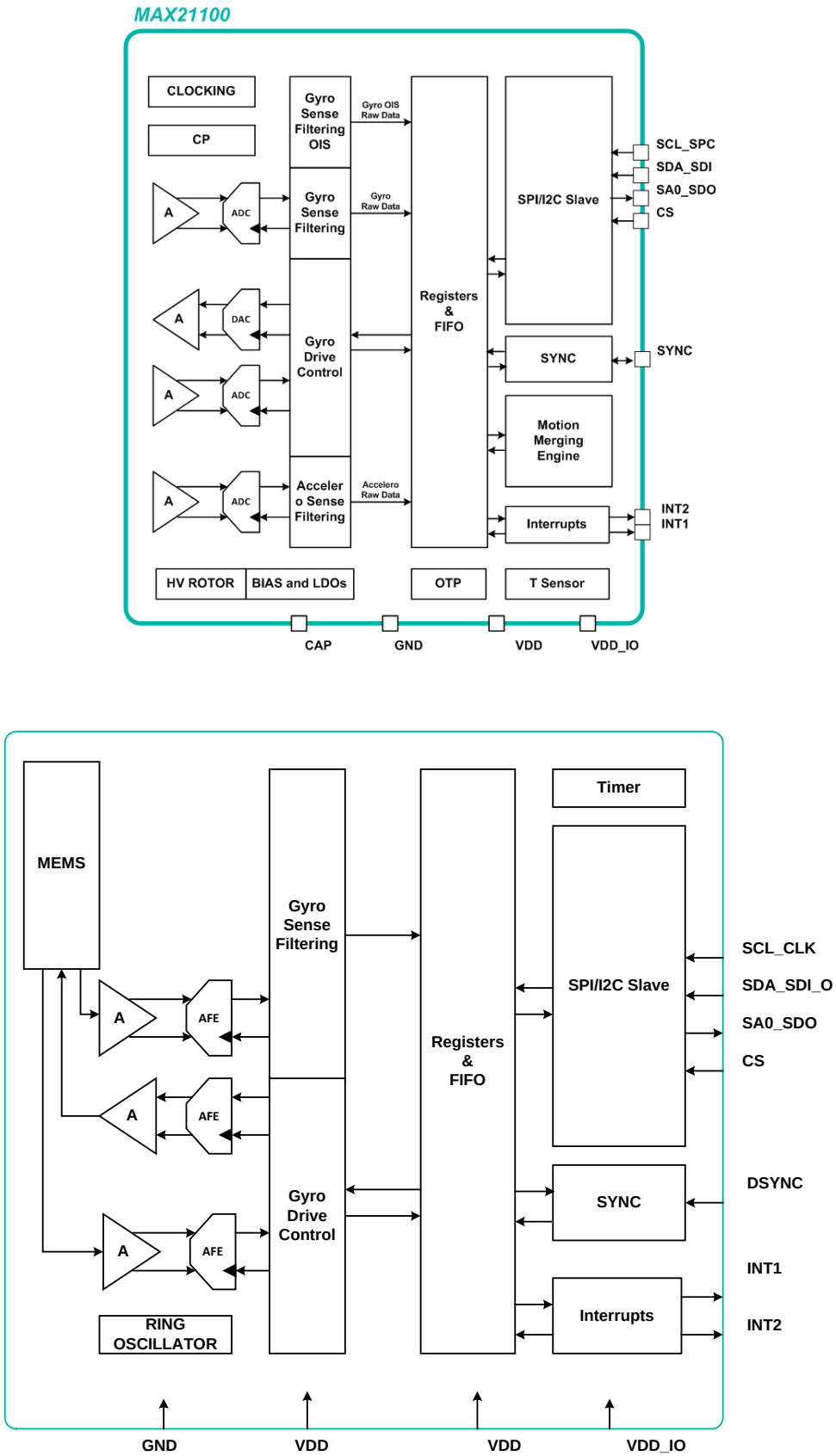


Figure 1: Block Diagram

3 MAX21100 Application Diagram

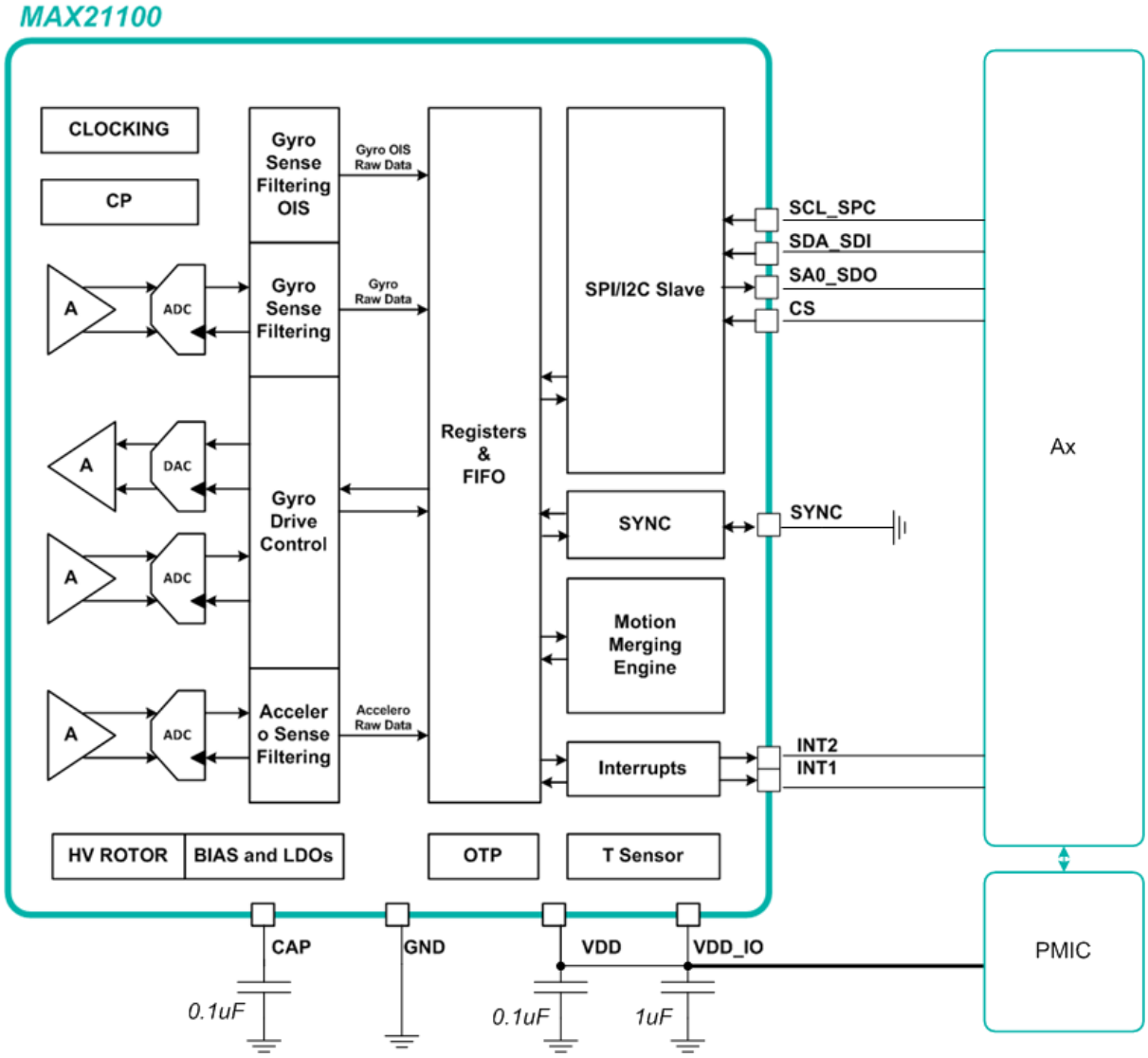


Figure 2: Application Diagram

4 Pin Description

Table 1: Pin Description

PIN	NAME	FUNCTION
1	VDDIO	Interface and interrupt Pad supply voltage. Same range of VDD. VDDIO<=VDD (diode)
2	N.C.	Not Connected
3	N.C.	Not Connected
4	SCL_CLK	SPI and I²C Clock. When in I²C mode, the IO has selectable anti-spike filter and delay to ensure correct hold time.
5	GND	Power-Supply Ground.
6	SDA_SDI_O	SPI In/Out Pin and I²C Serial Data. When in I²C mode, the IO has selectable anti-spike filter and delay to ensure correct hold time.
7	SA0_SDO	SPI Serial Data Out or I²C Slave Address LSB
8	CS	SPI Chip Select/Serial Interface Selection
9	INT2	Interrupt Line #2
10	RESERVED	Must Be Connected to GND
11	INT1	Interrupt Line #1
12	DSYNC	Data Synchronization Pin. Used to wake up the MAX21100 from power down/standby or to synchronize data with GPS/camera.
13	RESERVED	Leave Unconnected
14	V_{DD}	Analog Power Supply. Bypass to GND with a 0.1µF capacitor and one 10µF.
15	V_{DD}	Must be tied to V_{DD} in the application.
16	N.C.	Not Connected

5 MAX21100 I2C device address

Table 2: I2C Device addresses

I2C Base Address	SA0/SDO pin	R/W bit	Resulting Address
0x2C (6bit)	0	0	**0xB0**
0x2C	0	1	**0xB1**
0x2C	1	0	**0xB2**
0x2C	1	1	**0xB3**

6 I2C Interface

6.1 I2C Protocol

Writing to the MAX21100 using I2C requires that first the master sends a START condition (S) followed by the MAX21100's I2C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P), to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I2C slave.

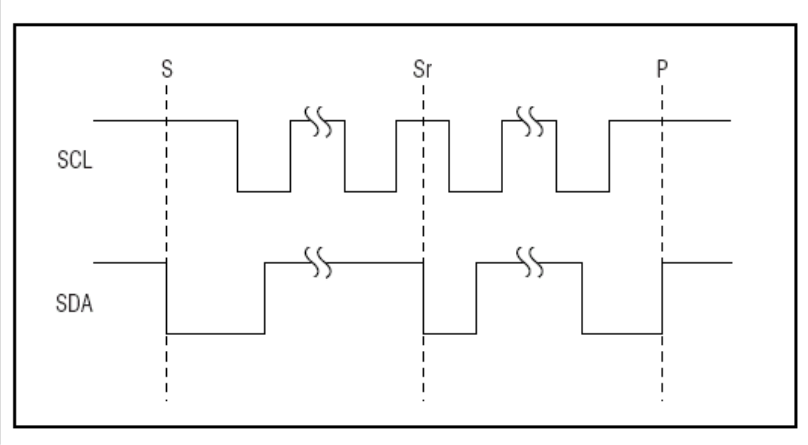


Figure 3: START/STOP/REPEATED START Conditions

6.2 SLAVE ADDRESS

The slave address is used to identify MAX21100 in I2C communications. Connect SA0_SDO to GND or VDD to select the last bit of the I2C slave address. The address is defined as the seven most significant bits (MSBs) followed by the Read/Write bit. Set the Read/Write bit to 1 to configure the MAX21100 to read mode. Set the Read/Write bit to 0 to configure the MAX21100 to write mode. The address is the first byte of information sent to the MAX21100 after the START condition.

6.3 ACKNOWLEDGE

The acknowledge bit (ACK) is a clocked 9th bit that the MAX21100 uses to handshake receipt of each byte of data when in write mode The MAX21100 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the 9th clock cycle to acknowledge the receipt of data when the MAX21100 is in read mode. An Acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX21100, followed by a STOP condition.

Note: When reading data from the MAX21100 always send a not-acknowledge from the master on the last read data byte ***or the MAX21100 will not relinquish the bus****.*

6.4 Register address

The formation of the register address is as follows:

--	MS/P	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
Don't Care	Multi Addressing or Parity; when = 0 autoincrement is enabled	Address from 0 to 64. Addresses from 0 to 32 may refer to different blocks, depending on the bank_sel bit field.					

6.5 I2C Protocols

6.5.1 Write 1 Byte

With this operation the master sends an address and one or two data byte to the slave device. This is done as follows:

1. The master sends a start condition
2. The master sends the 7 bits slave ID plus a write bit (low)
3. The addressed slave asserts an ACK on the data line
4. The master sends 8 bits Register Address.
5. The active slave asserts an ACK on the data line ***only if the address is valid (NAK if not)***
6. The master sends 8 bits data byte.
7. The slave asserts an ACK on the data line
8. The master generates a stop condition

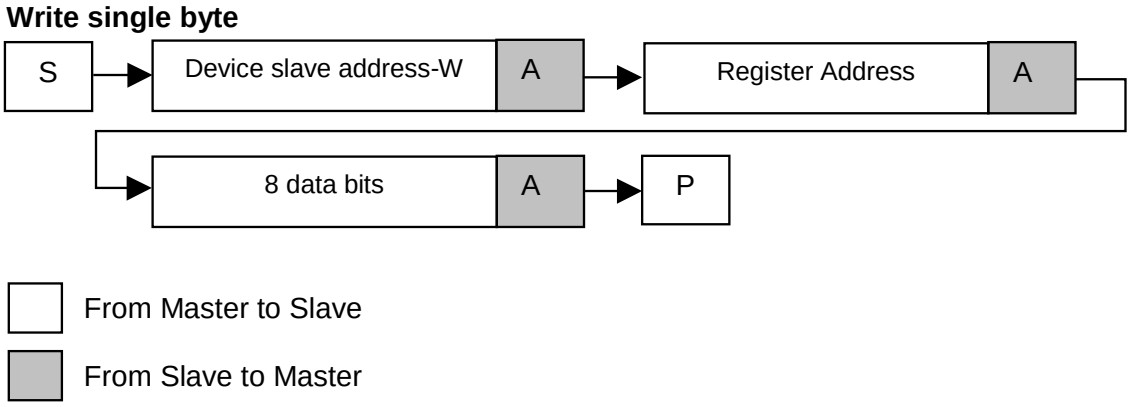


Figure 4: Write one byte

6.5.2 Burst write

The burst write protocol is the following:

1. The master sends a start condition
2. The master sends the 7 bits slave ID plus a write bit (low)
3. The addressed slave asserts an ACK on the data line
4. The master sends 8 bits of the Register Address
5. The slave asserts an ACK on the data line ***only if the address is valid (NAK if not)***
6. The master sends 8 bits of data
7. The slave asserts an ACK on the data line
8. Repeat 6 and 7 as long as needed
9. The master generates a stop condition

This protocol can be used to write a block multiple data into the register file.

Figure 5: Burst write

6.5.3 Read 1 Byte

This means:

1. The master sends a start condition
2. The master sends the 7 bits slave ID plus a write bit (low)
3. The addressed slave asserts an ACK on the data line
4. The master sends 8 data bits
5. The active slave asserts an ACK on the data line ***only if the address is valid (NAK if not)***
6. The master sends a restart condition
7. The master sends the 7 bits slave ID plus a read bit (high)
8. The addressed slave asserts an ACK on the data line
9. The slave sends 8 data bits
10. The master asserts a NACK on the data line
11. The master generates a stop condition

This protocol must be used by the master for the following purposes:

- *Read a byte from the address specified with the first written byte*.

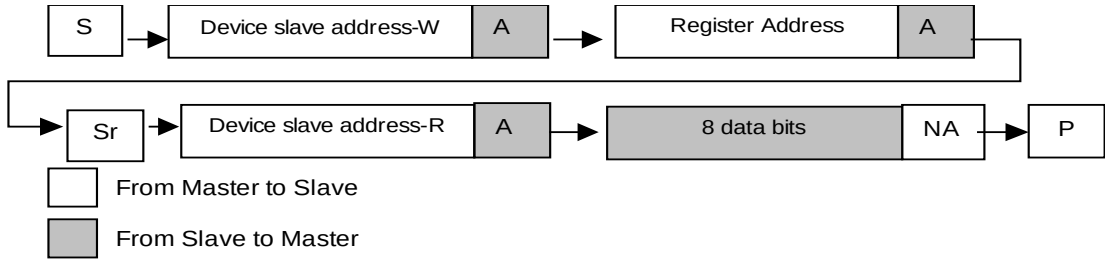


Figure 6: Read one byte

6.5.4 Burst read

The Burst read protocol is the following:

1 The master sends a start condition
2 The master sends the 7 bits slave ID plus a write bit (low)
3 The addressed slave asserts an ACK on the data line.
4 The master sends 8 bits of the Register Address
5 The slave asserts an ACK on the data line ***only if the address is valid (NAK if not)***
6 The master sends a repeated start condition.
7 The master sends the 7 bits slave ID plus a read bit (high)
8 The slave asserts an ACK on the data line
9 The slave sends 8 bits of data.
10 The master asserts an ACK on the data line
11 Repeat 9 and 10 as long as needed
12 The master generates a stop condition

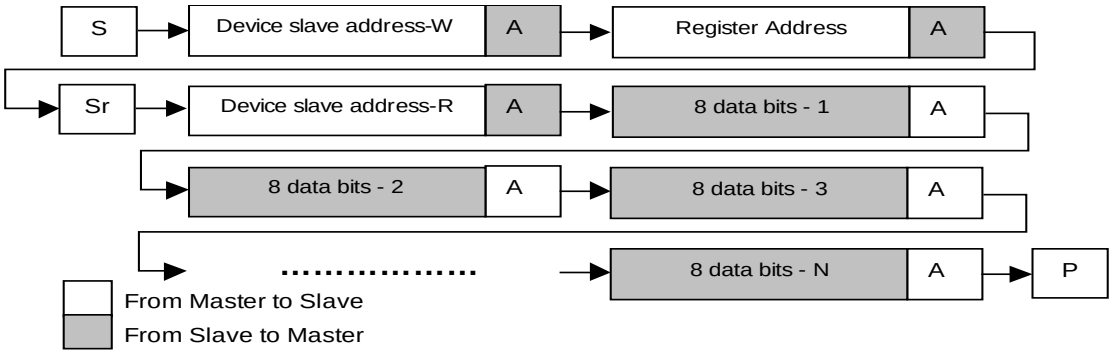


Figure 7: Burst read

7 SPI Interface

7.1 SPI Read and Write Protocol

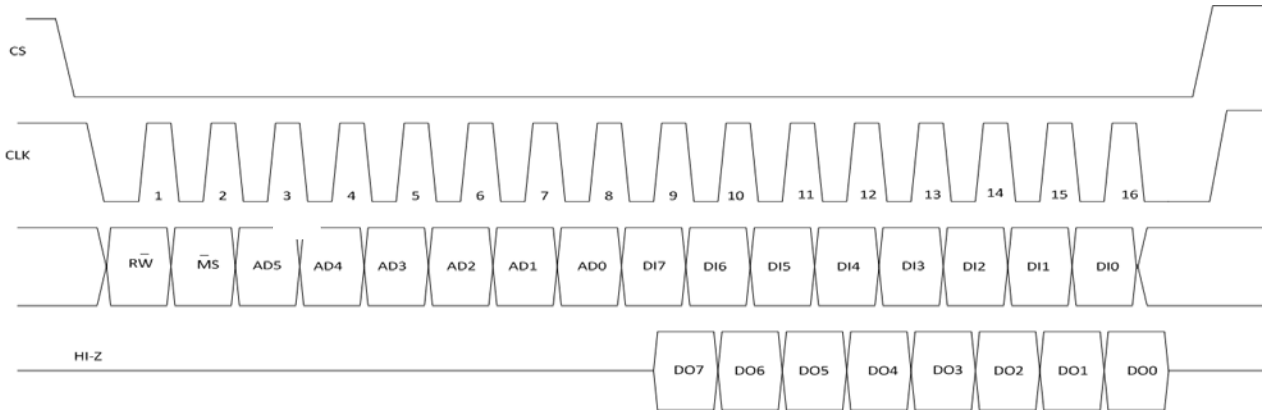


Figure 8: SPI Read and Write Protocol

CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end.
CLK is the serial port clock and is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are, respectively, the serial port data input and output. These lines are driven at the falling edge of CLK and should be captured at the rising edge of CLK.

Both the read register and write register commands are completed in 16 clock pulses, or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of CLK.

The first bit (bit 0) starts at the first falling edge of CLK after the falling edge of CS while the last bit (bit 15, bit 23, etc.) starts at the last falling edge of CLK just before the rising edge of CS.

- Bit 0: RW bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives SDO at the start of bit 8.
- Bit 1: MS/P bit. Depending on the configuration of if_parity this bit may either be used to operate in multi-addressing standard mode or to check the parity with the register address.
- If used as MS Bit, When 1, the address remains unchanged in multiple read/write commands, whilst when 0, the address is auto-incremented in multiple read/write commands.
- Bit 2-7: address AD(5:0). This is the address field of the indexed register.
- Bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).
- Bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the MS bit is 1, the address used to read/write data remains the same for every block.
When the MS bit is 0, the address used to read/write data is incremented at every block.
The function and the behavior of SDI and SDO remain unchanged.

8 Register Map

8.1 COMMON BANK

Table 3: Common Bank

Name	Register Address	Type	Default Value	Comment
WHO_AM_I	*0x20*	R	1011 0001	Device ID (0xB1)
REVISION_ID	*0x21*	R	0000 0001	Revision ID Register
BANK_SELECT	*0x22*	R/W	0000 0000	Register Bank Selection
SYSTEM_STATUS	*0x23*	R	Data	System Status Register
GYRO_X_H	*0x24*	R	Data	Bits [15:8] of X measurement, Gyro
GYRO_X_L	*0x25*	R	Data	Bits [07:0] of X measurement, Gyro
GYRO_Y_H	*0x26*	R	Data	Bits [15:8] of Y measurement, Gyro
GYRO_Y_L	*0x27*	R	Data	Bits [07:0] of Y measurement, Gyro
GYRO_Z_H	*0x28*	R	Data	Bits [15:8] of Z measurement, Gyro
GYRO_Z_L	*0x29*	R	Data	Bits [07:8] of Z measurement, Gyro
ACC_X_H	*0x2A*	R	Data	Bits [15:8] of X measurement, Accel.
ACC_X_L	*0x2B*	R	Data	Bits [07:0] of X measurement, Accel.
ACC_Y_H	*0x2C*	R	Data	Bits [15:8] of Y measurement, Accel.
ACC_Y_L	*0x2D*	R	Data	Bits [07:0] of Y measurement, Accel.
ACC_Z_H	*0x2E*	R	Data	Bits [15:8] of Z measurement, Accel.
ACC_Z_L	*0x2F*	R	Data	Bits [07:8] of Z measurement, Accel.
MAG_X_H	*0x30*	R	Data	Bits [15:8] of X measurement, Mag.
MAG_X_L	*0x31*	R	Data	Bits [07:0] of X measurement, Mag.
MAG_Y_H	*0x32*	R	Data	Bits [15:8] of Y measurement, Mag.
MAG_Y_L	*0x33*	R	Data	Bits [07:0] of Y measurement, Mag.
MAG_Z_H	*0x34*	R	Data	Bits [15:8] of Z measurement, Mag.
MAG_Z_L	*0x35*	R	Data	Bits [07:8] of Z measurement, Mag.
TEMP_H	*0x36*	R	Data	Bits [15:8] of T measurement
TEMP_L	*0x37*	R	Data	Bits [07:8] of T measurement
RFU	*0x38*	R	0000 0000	
RFU	*0x39*	R	0000 0000	
RFU	*0x3A*	R	0000 0000	
RFU	*0x3B*	R	0000 0000	
FIFO_COUNT	*0x3C*	R	0000 0000	Available number of FIFO samples
FIFO_STATUS	*0x3D*	R	0000 0000	FIFO Status Flags
FIFO_DATA	*0x3E*	R	Data	FIFO Data, to be read in burst mode
RST_REG	*0x3F*	W & Reset	0000 0000	Reset Register

- Go to USER BANK #0
- Go to USER BANK #1
- Go to USER BANK #2

8.1.1 WHO_AM_I

REG Name	WHO_AM_I: Device Identifier							
REG Address	Bank COMMON - 0x20 (Hex) - 32 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-10110001							
Content	WHOAMI							

Description

Device Identifier register. This number uniquely identifies the device type.

Parameters

- **WHOAMI**: Device Identifier 0xB1 (Hex)

8.1.2 REVISION_ID

REG Name	REVISION_ID: Revision ID Register							
REG Address	Bank 1- 0x21 (Hex) – 33 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type – Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	REVISION_ID							

Description

Revision ID register. This register provides the information about the silicon revision. The WHO_AM_I register wouldn't change in case on a new silicon revision, whilst the REVISION_ID register would track that.

Parameters

- **REVISION_ID** : Revision ID Register

8.1.3 BANK_SELECT

REG Name	BANK_SELECT: Bank Selector							
REG Address	Bank COMMON - 0x22 (Hex) - 34 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0000				RW-0000			
Content	RFU				BANK_SEL			

Description

User Bank selection register. It is used to have at any time 32 locations available for read and write operations, although more than 32 registers are available. The locations from 0x20 up to 0x3F (Common Bank) are always available, while locations from 0x00 to to 0x1F can be selected using the BANK_SEL parameter.

Parameters

- **BANK_SEL**: These four bits allow addressing 16 different pages of register other than the common bank. Page size is of 32 byte. Default bank is the user (0h) bank. Valid Combinations are:

0000 -> Bank 0 (User bank)
0001 -> Bank 1 (Interrupt bank)
Banks beyond Bank 1 are reserved.

8.1.4 SYSTEM_STATUS

REG Name	SYSTEM_STATUS: System Status							
REG Address	Bank COMMON - 0x23 (Hex) - 35 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	QUAT_ERR	QUAT_DR	MAGN_ERR	MAGN_DR	ACC_ERR	ACC_DR	GRYO_ERR	GYRO_DR

Description

This is the System Status register. It reports two fundamental flags necessary to properly manage the communication with the MAX21100. Ideally, every new data-reading operation from the MAX21100 should only take place when at least a new DATA_READY event has occurred. Failure to have a data reading every DATA_READY may result in either reading twice the same data or missing the data. That is particularly true when the FIFO is disabled.
The DR_ERR flag indicates the occurence of either one of the events described above.
If the FIFO is used, multiple data can be read safely, according to the FIFO_COUNT (0x3C) register, even though many DATA_READY have been generated.
The way the DATA_READY flag is reset can be configured using register DR_CFG (0x13).
Every Two bits express the Data ready bit and Error Flag or Quanternion, Magnetometer, Accelerometer and Gyrometer

Parameters

- **GYRO_ERROR**: This bit goes high when a new data is generated before or during gyro meter data reading
- **GYRO_DR**: Gyro meter data ready flag: it goes high when a new set of gyroscope data is available
- **ACC_ERROR**: This bit goes high when a new data generates before or during accelerometer data reading.
- **ACC_DR**: Accelerometer data ready flag: it goes high when a new set of accelerometer data is available.
- **MAGN_ERR**: This bit goes high when a new data generates before or during magnetometer data reading.
- **MAGN_DR**: Magnetometer data ready flag: it goes high when a new set of magnetometer data is available.
- **QUAT_ERR**: This bit goes high when a new data generates before or during quaternion data reading.
- **QUAT_DR**: Magnetometer data ready flag: it goes high when a new set of quaternion data is available.

8.1.5 GYRO_X_H

REG Name	**GYRO_X_H: Gyro Data, X-axis, MSB**							
REG Address	Bank COMMON - 0x24 (Hex) - 36 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_X_MSB							

Description

This register stores the most recent gyroscope measurement, specifically the MSB of the X-axis.

Gyroscope measurements are written to these registers at the Output Data Rate as defined in Register GYRO_CFG2.

The user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready bit, optionally configured as interrupt source..

Each 16-bit gyroscope measurement has a full scale defined in POWER_CFG.

Parameters

- **GYRO_X_MSB**: Gyroscope X output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.6 GYRO_X_L

REG Name	**GYRO_X_L: Gyro Data, X-axis, LSB**							
REG Address	Bank COMMON - 0x25 (Hex) - 37 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_X_LSB							

Description

LSB of the X-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_X_LSB**: Gyroscope X output (LSBs). These bits become MSBs if Endian = 1.

8.1.7 GYRO_Y_H

REG Name	GYRO_Y_H: Gyro Data, Y-axis, MSB							
REG Address	Bank COMMON - 0x26 (Hex) - 38 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Y_MSB							

Description

MSB of the Y-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Y_MSB**: Gyroscope Y output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.8 GYRO_Y_L

REG Name	GYRO_Y_L: Gyro Data, Y-axis, LSB							
REG Address	Bank COMMON - 0x27 (Hex) - 39 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Y_LSB							

Description

LSB of the Y-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Y_LSB**: Gyroscope Y output (LSBs). These bits become MSBs if Endian bit = 1.

8.1.9 GYRO_Z_H

REG Name	GYRO_Z_H: Gyro Data, Z-axis, MSB							
REG Address	Bank COMMON - 0x28 (Hex) - 40 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Z_MSB							

Description

MSB of the Z-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Z_MSB**: Gyroscope Z output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.10 GYRO_Z_L

REG Name	**GYRO_Z_L: Gyro Data, Z-axis, LSB**							
REG Address	Bank COMMON - 0x29 (Hex) - 41 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	GYRO_Z_LSB							

Description

LSB of the Z-axis. See GYRO_X_H for additional details.

Parameters

- **GYRO_Z_LSB**: Gyroscope Z output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.11 ACC_X_H

REG Name	**ACC_X_H: Accelerometer Data, X-axis, MSB**							
REG Address	Bank COMMON - 0x2A (Hex) - 42 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	ACC_X_MSB							

Description

This register stores the most recent acclerometer measurement, specifically the MSB of the X-axis.

Accelerometer measurements are written to these registers at the Output Data Rate as defined in Register ACC_CFG1.

The user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready bit, optionally configured as interrupt source..

Each 16-bit accelerometer measurement has a full scale defined in PWR_ACC_CFG.

Parameters

- **ACC_X_MSB**: Accelerometer X output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.12 ACC_X_L

REG Name	**ACC_X_L: Accelerometer Data, X-axis, LSB**							
REG Address	Bank COMMON - 0x2B (Hex) - 43 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	ACC_X_LSB							

Description

LSB of the X-axis. See ACC_X_H for additional details.

Parameters

- **ACC_X_LSB**: Accelerometer X output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.13 ACC_Y_H

REG Name	**ACC_Y_H: Accelerometer Data, Y-axis, MSB**							
REG Address	Bank COMMON - 0x2C (Hex) - 44 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	ACC_Y_MSB							

Description

MSB of the Y-axis. See ACC_X_H for additional details.

Parameters

- **ACC_Y_MSB**: Accelerometer Y output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.14 ACC_Y_L

REG Name	**ACC_Y_L: Accelerometer Data, Y-axis, LSB**							
REG Address	Bank COMMON - 0x2D(Hex) - 45 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	ACC_Y_LSB							

Description

LSB of the Y-axis. See ACC_X_H for additional details.

Parameters

- **ACC_Y_LSB**: Accelerometer Y output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.15 ACC_Z_H

REG Name	**ACC_Z_H: Accelerometer Data, Z-axis, MSB**							
REG Address	Bank COMMON - 0x2E (Hex) - 46 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	ACC_Z_MSB							

Description

MSB of the Z-axis. See ACC_X_H for additional details.

Parameters

- **ACC_Z_MSB**: Accelerometer Z output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.16 ACC_Z_L

REG Name	**ACC_Z_L: Accelerometer Data, Y-axis, LSB**							
REG Address	Bank COMMON - 0x2F (Hex) - 47 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	ACC_Z_LSB							

Description

LSB of the Z-axis. See ACC_X_H for additional details.

Parameters

- **ACC_Z_LSB**: Accelerometer Z output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.17 MAG_X_H

REG Name	**MAG_X_H: Magnetometer Data, X-axis, MSB**							
REG Address	Bank COMMON - 0x30 (Hex) - 48 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	MAG_X_MSB							

Description

This register stores the most recent acclerometer measurement, specifically the MSB of the X-axis.

Accelerometer measurements are written to these registers at the Output Data Rate as defined in Register ACC_CFG2.

Parameters

- **MAG_X_MSB**: Magnetometer X output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.18 MAG_X_L

REG Name	**MAG_X_L: Magnetometer Data, X-axis, LSB**							
REG Address	Bank COMMON - 0x30 (Hex) - 48 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	MAG_X_LSB							

Description

LSB of the X-axis. See MAG_X_H for additional details.

Parameters

- **MAG_X_LSB**: Magnetometer X output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.19 MAG_Y_H

REG Name	**MAG_Y_H: Magnetometer Data, Y-axis, MSB**							
REG Address	Bank COMMON - 0x31 (Hex) - 49 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	MAG_Y_MSB							

Description

MSB of the Y-axis. See MAG_X_H for additional details.

Parameters

- **MAG_Y_MSB**: Magnetometer Y output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.20 MAG_Y_L

REG Name	**MAG_Y_L: Magnetometer Data, Y-axis, LSB**							
REG Address	Bank COMMON - 0x32 (Hex) - 50 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	MAG_Y_LSB							

Description

LSB of the Y-axis. See MAG_X_H for additional details.

Parameters

- **MAG_Y_LSB**: Magnetometer Y output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.21 MAG_Z_H

REG Name	**MAG_Z_H: Magnetometer Data, Z-axis, MSB**							
REG Address	Bank COMMON - 0x33 (Hex) - 51 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	MAG_Z_MSB							

Description

MSB of the Z-axis. See MAG_X_H for additional details.

Parameters

- **MAG_Z_MSB**: Magnetometer Z output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.22 MAG_Z_L

REG Name	**MAG_Z_L: Magnetometer Data, Y-axis, LSB**							
REG Address	Bank COMMON - 0x35 (Hex) - 53 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	MAG_Z_LSB							

Description

LSB of the Z-axis. See MAG_X_H for additional details.

Parameters

MAG_Z_LSB: Magnetometer Z output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.23 TEMP_H

REG Name	**TEMP_H: Temperature Sensor, MSB**							
REG Address	Bank COMMON - 0x36 (Hex) - 54 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	TEMP_MSB							

Description

MSB of the temperature sensor. The temperature data is provided as an absolute value expressed in Celsius degrees. The sensitivity is 256 LSB/deg, which means that the TEMP_H registers changes whenever the temperature varies by 1 degree.
Temperature data cannot be read through the FIFO, it must be read using data registers.

Parameters

- **TEMP_MSB**: Temperature sensor output (MSBs). These bits become LSBs if Endian bit = 1.

8.1.24 TEMP_L

REG Name	**TEMP_L: Temperature Sensor, LSB**							
REG Address	Bank COMMON - 0x37 (Hex) - 55 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	TEMP_LSB							

Description

LSB of the temperature sensor.

Parameters

- **TEMP_LSB**: Temperature sensor output (LSBs).These bits become MSBs if Endian bit = 1.

8.1.25 FIFO_COUNT

REG Name	**FIFO_COUNT: Number of samples available in the FIFO**							
REG Address	Bank COMMON - 0x3C (Hex) - 60 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	FIFO_CNT							

Description

FIFO Count Register. This register should be read whenever the FIFO is enabled to make sure that the data read from the FIFO are only valid data. In fact, attention must be paid to the The completed procedure to read data from the FIFO is described in the Programming Examples section.

Parameters

- **FIFO_CNT**: The content of this register is the number of samples available

8.1.26 FIFO_STATUS

REG Name	**FIFO_STATUS: Status of the FIFO**					
REG Address	Bank COMMON - 0x3D (Hex) - 61 (Dec)					
	Bit 7:5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-000	R-0	R-0	R-0	R-0	R-0
Content	RFU	FIFO_WR_FULL	FIFO_ RD_EMPTY	FIFO_TH	FIFO_FULL	FIFO_EMPTY

Description

FIFO status register. This register gathers all the bits defining the status of the FIFO.
Bits [7:5] are unused.

Parameters

- **FIFO_WR_FULL** : At least one data was written (and lost) whilst the FIFO was full
- **FIFO_ RD_EMPTY** : At least one read has occurred whilst the FIFO was empty
- **FIFO_TH** : The FIFO contains data above the threshold
- **FIFO_FULL** : The FIFO is full
- **FIFO_EMPTY** : The FIFO is empty

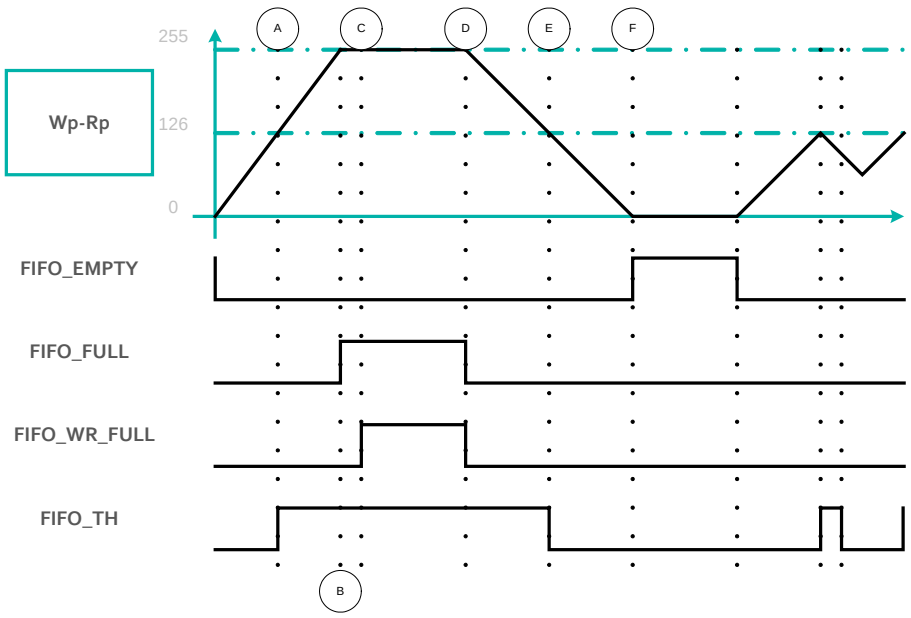


Figure 9: FIFO Flags

A) The difference between the Write Pointer and the Read Pointer reaches the programmed threshold
B) FIFO is full, next write operation will cause data to be lost
C) At least one data has been lost
D) Read access clears FIFO_FULL and FIFO_WR_FULL flags
E) Wp-Rp < programmed threshold
F) FIFO is empty: all the available new data have been read

8.1.27 FIFO_DATA

REG Name	**FIFO_DATA: Gyroscope data available through the FIFO**							
REG Address	Bank COMMON - 0x3E (Hex) - 62 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	FIFO_DAT							

Description

This register is used to read and write data from the FIFO buffer.
The contents of the sensor data registers are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN .
If the FIFO buffer has overflowed, the status bit **FIFO_WR_FULL** is automatically set to 1. This bit is located in the FIFO_STATUS (0x3D) register. When the FIFO buffer has overflowed, the oldest data will be lost and new data will be written to the FIFO if the override bit is set in the FIFO_CFG (0x18) register .
If the FIFO buffer is empty, reading this register will return the last byte that was previously read from the FIFO until new data is available. The user should check FIFO_COUNT (0x3C) to ensure that the FIFO buffer is not read when empty.

Parameters

- **FIFO_DAT**: When FIFO enables reading this address with burst reading, all the data stored in the FIFO are readable.
- Burst reading allows FIFO address to increment and the FIFO memory to be scrolled

8.1.28 RST_REG

REG Name	**RST_REG: Reset Register**							
REG Address	Bank COMMON - 0x3F (Hex) - 63 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000					RW-0	RW-0	RW-0
Content						PAR_RST	HPF_A_RST	HPF_G_RST

Description
Parity and High Pass filters reset register.

Parameters

- **PAR_RST**: Writing '1' resets the I2C/SPI parity error flag.
- **HPF_A_RESET**: Writing '1' the accelerometer HP filter is reset and output is restored to baseline
- **HPF_G_RESET**: Writing '1' the gyroscope HP filter is reset and output is restored to baseline

8.2 USER BANK #0 (Bank_sel = 0000)

Table 4: User Bank 0

Name	Register Address	Type	Default Value	Comment
POWER_CFG	*0x00*	RW	0000 0111	Power mode configuration
GYRO_CFG1	*0x01*	RW	0010 1000	Gyro configuration : LP and OIS
GYRO_CFG2	*0x02*	RW	0000 0100	Gyro configuration : ODR
GYRO_CFG3	*0x03*	RW	0000 0000	Gyro configuration : HP
PWR_ACC_CFG	*0x04*	RW	0000 0111	Accel. Power configuration
ACC_CFG1	*0x05*	RW	0000 0010	Accel. Configuration : ODR
ACC_CFG2	*0x06*	RW	0000 0000	Accel. Configuration : HP
MAG_SLV_CFG	*0x07*	RW	0000 0110	Magnetometer Slave Configuration
MAG_SLV_ADD	*0x08*	RW	0000 0000	Magnetometer Slave Address
MAG_SLV_REG	*0x09*	RW	0000 0000	Magnetometer Slave Register
MAG_MAP_REG	*0x0A*	RW	0000 0000	Magnetometer Mapping Register
I2C_MST_ADD	*0x0B*	RW	0000 0000	I2C Register Address
I2C_MST_DATA	*0x0C*	RW	0000 0000	I2C Register Data
MAG_OFS_X_MSB	*0x0D*	RW	0000 0000	Magnetometer Offset X, LSB
MAG_OFS_X_LSB	*0x0E*	RW	0000 0000	Magnetometer Offset X, MSB
MAG_OFS_Y_MSB	*0x0F*	RW	0000 0000	Magnetometer Offset Y, MSB
MAG_OFS_Y_LSB	*0x10*	RW	0000 0000	Magnetometer Offset Y, LSB
MAG_OFS_Z_MSB	*0x11*	RW	0000 0000	Magnetometer Offset Z, MSB
MAG_OFS_Z_LSB	*0x12*	RW	0000 0000	Magnetometer Offset Z, LSB
DR_CFG	*0x13*	RW	0000 0001	Data Ready configuration
IO_CFG	*0x14*	RW	0000 0000	Input/Output configuration
I2C_PAD	*0x15*	RW	0000 0100	I2C Pads configuration Register
I2C_CFG	*0x16*	RW	0000 0000	I2C configuration
FIFO_TH	*0x17*	RW	0000 0000	FIFO Threshold configuration
FIFO_CFG	*0x18*	RW	0000 0000	FIFO Mode configuration
RFU	*0x19*	R	0000 0000	
DSYNC_CFG	*0x1A*	RW	0000 0000	DSYNC Configuration
DSYNC_CNT	*0x1B*	RW	0000 0000	DSYNC Counter
ITF_OTP	*0x1C*	RW	0000 0000	Interface & OTP Status Configuration
RFU	*0x1D*	R	0000 0000	
RFU	*0x1E*	R	0000 0000	
RFU	*0x1F*	R	0000 0000	

8.2.1 POWER_CFG

REG Name	**POWER_CFG: Power Configuration**							
REG Address	Bank 0 - 0x00 (Hex) - 0 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	RW-0	RW-0000				RW-1	RW-1	RW-1
Content	PWR_SEL	PWR_MODE				SNS_EN_Z	SNS_EN_Y	SNS_EN_X

Description

Full Scale, Power Mode and axes configuration register.

Parameters

- **PWR_MODE**: configuration of the power mode of the:

Table 5: Power Mode Configuration

PWR_SEL	PWR_MODE	Power Mode
0	0000	powerdown mode (default)
0	0001	gyro sleep mode
0	0010	gyro spot mode
0	0011	gyro normal mode
0	0100	not used
0	0101	not used
0	0110	not used
0	0111	not used
0	1000	accelero spot mode
0	1001	not used
0	1010	not used
0	1011	not used
0	1100	accelero normal mode
0	1101	accelero normal + gyro sleep mode
0	1110	accelero normal + gyro spot mode
0	1111	accelero normal + gyro normal mode
1	0000	powerdown <-> accelero spot
1	0001	powerdown <-> accelero normal
1	0010	powerdown <-> gyro spot
1	0011	powerdown <-> gyro normal
1	0100	powerdown <-> accelero normal + gyro normal
1	0101	powerdown <-> acclero normal + gyro spot
1	0110	gyro sleep <-> gyro normal
1	0111	gyro sleep <-> accelero normal + gyro normal
1	1000	gyro spot <-> accelero normal + gyro normal
1	1001	accelero spot <-> accelero normal + gyro spot
1	1010	accelero normal <->accelero normal + gyro normal
1	1011	accelero normal <-> accelero normal + gyro spot
1	1100	accelero normal <-> accelero normal + gyro normal
1	1101	accelero normal + gyro sleep <-> accelero normal + gyro spot
1	1110	accelero normal + gyro sleep <-> accelero normal + gyro normal

1	1111	accelero normal + gyro spot <-> accelero normal + gyro normal

- **PWR_SEL:** When 1, PWR_MODE becomes a transition between power modes controllable by DSYNC pin.
- **SNS_EN_Z**: Z direction enable bit. '1' means enabled.
- **SNS_EN_Y**: Y direction enable bit. '1' means enabled.
- **SNS_EN_X**: X direction enable bit. '1' means enabled.

8.2.2 GYRO_CFG1

REG Name	**GYRO_CFG1: Sensing chain configuration register #1**							
REG Address	Bank 0 - 0x01 (Hex) - 1 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00		RW-1010				RW-00	
Content	SELF_TEST		SNS_LPF_CFG				SNS_DOUT_FSC	

Description

Low Pass filter, OIS and Self Test configuration register.

Parameters

- **SELF_TEST** : Bit 6 is used to activate the self-test mode. When activated, an offset is generated on the digital output whose amount depends on the full scale selected. Bit 7 can be used to invert the sign of the self-test output. The output of this parameter is affected by a strong spread, in the order of +/- 50%. This test allows detecting both electrical and mechanical issues. The table below summarizes the expected values.
  00-> disabled (default)
  01-> positive sign
  1x-> negative sign

Table 6: Self-Test Output

Axis	FS= 2000	FS= 1000	FS=500	FS=250
X[dps]	450	225	110	55
Y[dps]	-450	-225	-110	-55
Z[dps]	450	225	110	55

- **SNS_LPF_CFG**: Output bandwidth selection bits when SNS_GYR_OIS_LPF=0

Table 7: Bandwidth configuration

SNS_LPF_CFG	BW
0	2Hz
1	4Hz
2	6Hz
3	8Hz

4	10Hz
5	14Hz
6	22Hz
7	32Hz
8	50Hz
9	75Hz
10	100Hz (default)
11	150Hz
12	200Hz
13	250Hz
14	300Hz
15	400Hz

When SNS_GYR_OIS_LPF =1
0xxx = 1kHz
1xxx = 2kHz

- **SNS_DOUT_FSC**: Full scale configuration bits:

Table 8: Full Scale configuration

SNS_DOUT_FSC	FS
00	2000 dps (default)
01	1000 dps
10	500 dps
11	250 dps

8.2.3 GYRO_CFG2

REG Name	**GYRO_CFG2: Sensing chain configuration register #2**							
REG Address	Bank 0 - 0x02 (Hex) - 2 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00		RW-0	RW-0	RW-0100			
Content	RFU		SNS_GYR_OIS_LPF	SNS_GYR_HPF	SNS_ODR			

Description

Output Data Rate configuration register. This register selects the preferred Output Data Rate (ODR) according to the description that follows.

Bit 5 is used to activate/de-activate the gyroscope low-pass filter for OIS mode.
Bit 4 is used to activate/de-activate the gyroscope hi-pass filter.
Bits [7:6] are reserved.

Parameters

- **SNS_GYR_OIS_LPF**: the selection of the low-pass results as follow:

0 -> off, at the meantime, the SNS_LPF_CFG (GYRO_CFG1) set as gyro low-pass filter
1 -> on

- **SNS_DOUT_CFG**: the selection of the high-pass results as follow:

0 -> hi-pass filter deactivated
1 -> hi-pass filter activated

- **SNS_ODR**

SPOT MODE ENABLED	SNS_ODR	Selected Output Data Rate
No	0000	gyr_odr = 8 KHz
No	0001	gyr_odr = 4 KHz
No	0010	gyr_odr = 2 KHz
No	0011	gyr_odr = 1 KHz
No	0100	gyr_odr = 500 Hz (default)
No	0101	gyr_odr = 250 Hz
No	0110	gyr_odr = 125 Hz
No	0111	gyr_odr = 62.5 Hz
No	1000	gyr_odr = 31.25 Hz
No	1001	gyr_odr = 15.625 Hz
No	1010	gyr_odr = 7.8125 Hz
No	1011-1111	gyr_odr = 3.90625 Hz
Yes	0000-0101	gyr_odr = 250 Hz
Yes	0110	gyr_odr = 125 Hz
Yes	0111	gyr_odr = 62.5 Hz
Yes	1XXX	gyr_odr = 31.25 Hz

8.2.4 GYRO_CFG3

REG Name	GYRO_CFG3: Sensing chain configuration register #3							
REG Address	Bank 0 - 0x03 (Hex) - 3 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-000			RW-00		RW-000		
Content	RFU			WAIT_DATA_MODE		SNS_HPF_CFG		

Description

High Pass filter and Wait Data Mode configuration register.
3 LSBs are used to select the cut-off frequency of the high-pass filter.

Bits [7:5] are reserved.

Parameters

- **WAIT_DATA_MODE** : the control trigger for wait data modes,
  00 Data cost 1/ODR time to get a gyro_data_ready
  11 Data cost at least 1 data is ready to get a gyro_data_ready

- **SNS_HPF_CO**: Configuration for the HP filter cutoff frequency:

Table 9: High Pass Filter configuration

SNS_HPF_CFG	BW
0	0 = 0.08Hz
1	1 = 0.24Hz
2	2 = 0.8Hz
3	3 = 2Hz
4	4 = 5Hz
5	5 = 10Hz
6	6 = 20Hz
7	7 = 50Hz

8.2.5 PWR_ACC_CFG

REG Name	**PWR_ACC_CFG: Accelerometer Power Configuration**							
REG Address	Bank 0 - 0x04 (Hex) - 4 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	RW-00		RW-000			RW-1	RW-1	RW-1
Content	SNS_ACC_FSC		ACC_SELF_TEST			SNS_EN_Z	SNS_EN_Y	SNS_EN_X

Description

Full Scale, Power Mode and axes configuration register.

Parameters

- **SNS_ACC_FSC**: Full scale configuration bits:

Table 10: Full Scale configuration

SNS_ACC_FSC	FS
00	16g (Default)
01	8g
10	4g
11	2g

- **ACC_SELF_TEST**: Activate the accelerometer self-test, describes as following:

000 ->No test
0xx ->Positive Force
1xx -> Negative Force
x01 -> X Axis Self-test
x10 -> Y Axis Self-test
x11 -> Z Axis Self-test

- **SNS_EN_Z**: Z direction enable bit . '1' means enabled.
- **SNS_EN_Y**: Y direction enable bit . '1' means enabled.
- **SNS_EN_X**: X direction enable bit . '1' means enabled.

8.2.6 ACC_CFG1

REG Name	ACC_CFG1: Accelerometer configuration register #1							
REG Address	Bank 0 - 0x05 (Hex) - 5 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00		RW-00		RW-0010			
Content	SNS_ACC_HPF_CFG		SNS_ACC_LPF_CFG		SNS_ACC_ODR			

Description

Accelerometer configuration register #1. This register selects the preferred Output Data Rate (ODR) , the High Pass and Low Pass bandwidths according to the description that follows.

Parameters

- **SNS_ACC_HPF_CFG**: Configuration for the Accelerometer HP filter cutoff frequency:

Table 11: High Pass Filter configuration

SNS_ACC_HPF_CFG	BW
0	ODR/400 (default)
1	ODR/200
2	ODR/100
3	ODR/50

- **SNS_ACC_LPF_CFG**: Output bandwidth selection bits

Table 12: Bandwidth configuration

SNS_ACC_LPF_CFG	BW
0	ODR/48 (default)
1	ODR/22
2	ODR/9
3	ODR/3

- **SNS_ACC_ODR**

SPOT MODE ENABLED	SNS_ODR	Selected Output Data Rate
No	0000	acc_odr = 2 KHz
No	0001	acc_odr = 1 KHz
No	0010	acc_odr = 500 Hz (default)
No	0011	acc_odr = 250 Hz
No	0100	acc_odr = 125 Hz
No	0101	acc_odr = 62.5 Hz
No	0110-1111	acc_odr = 31.25 Hz
Yes	0000-0011	acc_odr = 250Hz(default)
Yes	0100	acc_odr = 125Hz
Yes	0101	acc_odr = 62.5Hz
Yes	0110	acc_odr = 31.25Hz
Yes	0111	acc_odr = 15.625Hz
Yes	1000	acc_odr = 7.8125Hz
Yes	1001	acc_odr = 3.90625Hz
Yes	1010	acc_odr = 1.953125Hz
Yes	1011-1111	acc_odr = 0.9765625Hz

-

8.2.7 ACC_CFG2

REG Name	**ACC_CFG2: Accelerometer configuration register #2**							
REG Address	Bank 0 - 0x06 (Hex) – 6 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0000				RW-000			RW-0
Content	RFU				SNS_MAG_ODR			ACC_HP_EN

Description

Accelerometer configuration register #2. This register enables/disables the accelerometer HP filter and selects the preferred Output Data Rate (ODR) for the magnetometer.

Parameters

- **SNS_MAG_ODR**: Magnetometer ODR Frequency = ACC_ODR / 2^SNS_MAG_ODR

SNS_MAG_ODR	Magnetometer ODR Frequency
000	ACC_ODR
001	ACC_ODR /2
010	ACC_ODR /4
011	ACC_ODR /8
100	ACC_ODR /16
101	ACC_ODR /32
110	ACC_ODR /64
111	ACC_ODR/128

- **SNS_ACC_LPF_CFG**: Output bandwidth selection bits

Table 13: Bandwidth configuration

ACC_HP_EN	Effect
0	Accelerometer HP Filter disabled (default)
1	Accelerometer HP Filter enabled

8.2.8 MAG_SLV_CFG

REG Name	**MAG_SLV_CFG: Magnetometer I2C Slave configuration**							
REG Address	Bank0 - 0x07 (Hex) - 7 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bi
Type - Def. Value	RW-0	RW-0	RW-0	RW-0	RW-0	RW-110		
Content	MAG_EN	MAG_SWAP	MAG_SAFE	MAG_GRP	I2C_STD	MAG_I2C_LEN		

Description

External Magnetometer I2C Slave configuration

Parameters

- **MAG_EN**: External Magnetometer Enable (1) /Disable (0)
- **MAG_SWAP**: MSB First (0) /Last(1)

- **MAG_SAFE:** Reg ON (0)/OFF (1)
- **MAG_GRP:** Group Even (0)/Odd(1)
- **I2C_STD:** 400kHz(0)/100kHz(1)
- **MAG_I2C_LEN:** Number of bytes to transfer at every I2C access performed by the I2C Master at the ODR selected for the magnetometer.

8.2.9 MAG_SLV_ADD

REG Name	**MAG_SLV_ADD: Magnetometer I2C Slave address**							
REG Address	Bank 0 - 0x08 (Hex) - 8 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	RW-0000000						
Content	RSU	MAG_SLV_ADD						

Description

External Magnetometer I2C Slave address

Parameters

MAG_SLV_ADD: External Magnetometer I2C Slave address.

8.2.10 MAG_SLV_REG

REG Name	**MAG_SLV_REG: Magnetometer I2C Slave register**							
REG Address	Bank0 - 0x09 (Hex) - 9 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	MAG_SLV_REG							

Description

External Magnetometer I2C Slave register address

Parameters

- **MAG_SLV_REG**: External Magnetometer I2C Slave register address

8.2.11 MAG_MAP_REG

REG Name	**MAG_MAP_REG: I2C Master Mapping Configuration**							
REG Address	Bank 0 - 0x0A (Hex) - 10 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00		RW-000			RW-0	RW-0	RW-0
Content	RFU		MAG_CH_MAP			INV_Z	INV_Y	INV_X

Description

Magnetometer I2C master Mapping configuration

Parameters

- **MAG_CH_MAP**: Channel mapping

MG_CH_MAP	Channel mapping
000	[Xi , Yi , Zi] <= [A , B , C]
001	[Xi , Yi , Zi] <= [A , C , B]
010	[Xi , Yi , Zi] <= [B , A , C]
011	[Xi , Yi , Zi] <= [C , A , B]
100	[Xi , Yi , Zi] <= [B , C , A]
101	[Xi , Yi , Zi] <= [C , B , A]
110	[Xi , Yi , Zi] <= [A , B , C]
111	[Xi , Yi , Zi] <= [A , B , C]

- **INV_Z:** Invert Z
- **INV_Y:** Invert Y
- **INV_X:** Invert X

8.2.12 I2C_MST_ADD

REG Name	**I2C_SLV_ADD: I2C Slave address register**							
REG Address	Bank 0 - 0xB (Hex) - 11 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	I2C_MST_ADD							

Description

External Peripheral register address

Parameters

I2C_MST_ADD: External Magnetometer Master I2C Address Register

8.2.13 I2C_MST_DATA

REG Name	**I2C_SLV_DATA: I2C Slave register data register**							
REG Address	Bank0 - 0x0C (Hex) - 12 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	I2C_MST_DATA							

Description

External Peripheral master I2C data read/write register

Parameters

- **I2C_SLV_DATA**: External Magnetometer I2C Slave register address

8.2.14 MAG_OFS_X_MSB

REG Name	**MAG_OFS_X_MSB: Magnetometer Offset compensation**							
REG Address	Bank 0 - 0x0D (Hex) - 13 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	MAG_OFS_X_MSB							

Description

External Magnetometer X Offset compensation (MSB)

Parameters

- **MAG_OFS_X_MSB**: External Magnetometer X Offset compensation (MSB)

8.2.15 MAG_OFS_X_LSB

REG Name	**MAG_OFS_X_LSB: Magnetometer Offset compensation**							
REG Address	Bank 0- 0x0E (Hex) - 14 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	MAG_OFS_X_LSB							

Description

External Magnetometer X Offset compensation (LSB)

Parameters

- **MAG_OFS_X_LSB**: External Magnetometer X Offset compensation (LSB)

8.2.16 MAG_OFS_Y_MSB

REG Name	**MAG_OFS_Y_MSB: Magnetometer Offset compensation**							
REG Address	Bank 0 - 0x0F (Hex) - 15 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	MAG_OFS_Y_MSB							

Description

External Magnetometer Y Offset compensation (MSB)

Parameters

- **MAG_OFS_Y_MSB**: External Magnetometer Y Offset compensation (MSB)

8.2.17 MAG_OFS_Y_LSB

REG Name	**MAG_OFS_Y_LSB: Magnetometer Offset compensation**							
REG Address	Bank 0 - 0x10 (Hex) - 16 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	MAG_OFS_Y_LSB							

Description

External Magnetometer Y Offset compensation (LSB)

Parameters

- **MAG_OFS_Y_LSB**: External Magnetometer Y Offset compensation (LSB)

8.2.18 MAG_OFS_Z_MSB

REG Name	**MAG_OFS_Z_MSB: Magnetometer Offset compensation**							
REG Address	Bank 0 - 0x11 (Hex) - 17 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	MAG_OFS_Z_MSB							

Description

External Magnetometer Z Offset compensation (MSB)

Parameters

- **MAG_OFS_Z_MSB**: External Magnetometer Z Offset compensation (MSB)

8.2.19 MAG_OFS_Z_LSB

REG Name	**MAG_OFS_Z_LSB: Magnetometer Offset compensation**							
REG Address	Bank 0 - 0x12 (Hex) - 18 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	MAG_OFS_Z_LSB							

Description

External Magnetometer Z Offset compensation (LSB)

Parameters

MAG_OFS_Z_LSB: External Magnetometer Z Offset compensation (LSB)

8.2.20 DR_CFG

REG Name	DR_CFG: Data Ready Configuration							
REG Address	Bank 0 - 0x13 (Hex) - 19 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0	R-0	RW-0	RW-0	RW-00		RW-0	RW-1
Content	BYP_EN	RFU	RW_SEL	SNGL_EN	DR_RST_MODE		COARSE_TEMP	TEMP_EN

Description

Data Ready configuration register.

Parameters

- **BYP_EN** : '0' is I2C_MASTER active, '1' is bypass
- **RW_SEL** : '0' is Write, '1' Read
- **SNGLE_EN** : Enable (1) or Disable (0) single R or single Write
- **DR_RST_MODE**: These bits control the way the DATA_READY is reset and the way the data updated. 3 available modes:

00 : ALL - DATA_READY is cleared when all the active channels are read.
Data Set updates only when all the data are read.

01 : ANY - DATA_READY is cleared when at least one half active channel is read.
Data Set is not guaranteed because data can be updated immediately

10: STATUS - DATA_READY is cleared when status register is read.
Data Set is maintained until status register is read.

- **COARSE_TEMP** : '0' is fine, '1' is for coarse. If "fine", temperature data updates only when both bytes are read. If "coarse", reading MSB enables the data update.
- **TEMP_EN** : Enable (1) or Disable (0) the temperature sensor

8.2.21 IO_CFG

REG Name	**IO_CFG: Input/output Configuration**						
REG Address	Bank 0 - 0x14 (Hex) - 20 (Dec)						
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	1:0
Type - Def. Value	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	R-00
Content	DSYNC_PD_EN	DSYNC_PU_EN	INT1_PD_EN	INT1_PU_EN	INT2_PD_EN	INT2_PU_EN	I2C_CFG

Description

I/O configuration Register. This register controls the pull-up and pull-down resistors of the pins DSYNC, INT1 and INT2.

Parameters

- **DSYNC_PD_EN**: When 1, the internal pull down of the pad is connected
- **DSYNC_PU_EN**: When 1, the internal pull up of the pad is connected
- **INT1_PD_EN**: When 1, the internal pull down of the pad is connected
- **INT1_PU_EN**: When 1, the internal pull up of the pad is connected
- **INT2_PD_EN**: When 1, the internal pull down of the pad is connected
- **INT2_PU_EN**: When 1, the internal pull up of the pad is connected
- **I2C_CFG[1]**: I2C_CFG[1]: Enable (0) or Disable (1) Master I2C Pull-ups
- **I2C_CFG[0]**: I2C_CFG[0]: Enable (0) or Disable (1) Slave I2C Pull-ups

8.2.22 I2C_PAD

REG Name	**I2C_PAD: I2C Pads Configuration**							
REG Address	Bank 0 - 0x15 (Hex) - 21 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000					RW-1	RW-0	RW-0
Content	RFU					SLV_STG	MST_STG	INT_STG

Description

I2C Pads configuration Register. This register controls the electrical behaviour
Bit [7:3] is reserved.

Parameters

- **SLV_STG**: When 1, SDA/SCL Slave drivers are faster, requiring more current
- **MST_STG**: When 1, SDA/SCL Master drivers are faster, requiring more current
- **INT_STG** When 1, INT driver is faster, requiring more current

8.2.23 I2C_CFG

REG Name	**I2C_CFG: I2C Configuration**							
REG Address	Bank 0 - 0x16 (Hex) - 22 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00		R-000			RW-0	RW-0	RW-0
Content	MST_I2C_CFG		RFU			SPI_3_WIRE	ENDIAN	I2C_OFF

Description

I2C configuration register.

Parameters

- **MST_I2C_CFG** Change the I/O configuration according to the following table:

Table 14: I/O Current Configuration

DRIVE		IOs Configuration
0	0	MST_I2C without anti-spike filter
0	1	MST_I2C standard configuration
1	0	MST_I2C without filters and delays
1	1	Reserved

- **SPI_3_WIRE** : 3 or 4 wires SPI mode. When set SPI 3 wire is enabled
- **ENDIAN**: Big little endian configuration bit.
  - 0 is for big endian (MS Byte, LS Byte),
  - 1 for little (LS Byte, MS Byte)
- **I2C_OFF**: This bit is used for turn off the I2C interface. By default, I2C is active. Setting to 1 this bit I2C is turned off. It may be used when connecting several SPI devices in parallel.

8.2.24 FIFO_TH

REG Name	**FIFO_TH: FIFO threshold for the interrupt generation**							
REG Address	Bank 0 - 0x17 (Hex) - 23 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	FIFO_SAMPLES							

Description

FIFO Threshold configuration register. This register defines the number of samples that should be used as threshold to set the FIFO_OVTHOLD bit

Parameters

- **FIFO_SAMPLES**: When the number of samples yet to be read stored in FIFO crosses this number, an interrupt is generated on FIFO_OVTHOLD

Note: This parameter specifies the number of Gyroscope output samples expressed in words (16-bit OR 2 bytes). It does not refer to one single axis but to the overall number of samples coming from entire set the selected axis.

8.2.25 FIFO_CFG

REG Name	FIFO_CFG: FIFO configuration bits						
REG Address	Bank 0 - 0x18 (Hex) - 24 (Dec)						
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Type - Def. Value	RW-00		RW-0	RW-0	RW-0	RW-0	RW-0
Content	FIFO_MODE		FIFO_INT_SEL	FIFO_OVERRUN	FIFO_STORE_QUAT	FIFO_STORE_MAG	FIFO_STORE_ACC

Description

FIFO configuration register. This register determines which sensor measurements are loaded into the FIFO buffer and selects the desired FIFO behavior.

Data stored inside the sensor data registers will be loaded into the FIFO buffer if a sensor's respective FIFO_store bit is set to 1 in this register. The behavior of FIFO writes when the FIFO buffer is full can be configured with the FIFO_MODE bit. In order to read the data in the FIFO buffer, the FIFO_MODE must be set to a value >0.

When the FIFO_STORE_{QUAT,MAG,ACC,GYR} bit is enabled in this register, data will be loaded into the FIFO buffer for the corresponding input data.

Parameters

- **FIFO_MODE**: These bits are used to configure the FIFO mode:

00 -> OFF
01 -> NORMAL
10 -> INTERRUPT
11 -> INTERRUPT TOGGLE

- **FIFO_INT_SEL**: When an interrupt mode is selected, this bits define which kind of mask must be used:

0: use OR mask
1: use AND mask

- **FIFO_OVERRUN**: When set to TRUE, FIFO data are overwritten and oldest are lost. When FALSE, FIFO is a buffer that stops when full
- **FIFO_STORE_QUAT**: When set to TRUE, 16-bits 4 quaternion components are stored in FIFO.
- **FIFO_STORE_MAG**: When set to TRUE, 16-bits the magnetometer data are stored in FIFO.
- **FIFO_STORE_ACC**: When set to TRUE, 16-bits the accelerometer data are stored in FIFO.
- **FIFO_STORE_GYR:** When set to TRUE, 16-bits the gyroscope data are stored in FIFO.

8.2.26 DSYNC_CFG

REG Name	**DSYNC_CFG: DSYNC Configuration**							
REG Address	Bank 0 - 0x1A (Hex) – 26 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
Content	DSQ_ENR	DSQ_ENF	DSW_EDG	DSW_LOW	DS_G_ENB	DS_A_ENB	DS_M_ENB	DS_T_ENB

Description

DSYNC configuration register. This register has to be used to configure the way the MAX21100 manages events occurring on the DSYNC pin. Multiple different actions can be taken simultaneously, like changing the power mode, mapping the DSYNC pin value onto the gyroscope LSB data and concurrently triggering the capture of new data.
When the DSYNC pin is configured as active on edge and a dynamic power mode is configured, only the active edge determines the transition. The opposite transition must be done wither in SW or by reversing the active edge.

Parameters

- **DSQ_ENR**: When 1, enable data queuing with DSYNC rising
- **DSQ_ENF**: When 1, enable data queuing with DSYNC falling
- **DSW_EDG**: When 1, DSYNC is an active on edge. When 0, DSYNC is an active on level
- **DSW_LOW**: When 1, DSYNC is an active low level control to wake up. When 0, DSYNC is an active high level to wake up. This bit affects both the edge and the level modes.
- **DS_G_ENB**: When 1, the DSYNC signal is mapped onto the Gyro LSB, on every axis
- **DS_A_ENB**: When 1, the DSYNC signal is mapped onto the Accelerometer LSB, on every axis
- **DS_M_ENB**: When 1, the DSYNC signal is mapped onto the Magnetometer LSB, on every axis
- **DS_T_ENB**: When 1, the DSYNC signal is mapped onto the Temperature LSB

8.2.27 DSYNC_CNT

REG Name	**DSYNC_CNT: DSYNC Counter**							
REG Address	Bank - 0x1B (Hex) – 27 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000				RW-0000			
Content	RFU				DSYNC_COUNTER			

Description

DSYNC counter configuration register. This register can be used to track the evolution of the rate signal from the gyroscope immediately after an external event captured on the DSYNC pin.

Parameters

- **DSYNC_COUNTER**: This register specifies the number of samples to be stored into the FIFO upon detecting a DSYNC active edge

8.2.28 ITF_OTP

REG Name	**ITF_OTP: Interface and OTP control**						
REG Address	Bank 0 - 0x1C (Hex) - 28 (Dec)						
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Type - Def. Value	R-0	R-0	RW-00		R-00		R-0
Content	RFU	PARITY_ERROR	IF_PARITY		OTP_ECC_STAT		OTP_DOWNLOAD

Description

Interface and OTP configuration register

Parameters

- **PARITY_ERROR**: Error in SPI/I2C address
- **IF_PARITY** : Interface bit 6 configuration bits:
  - 00 -> bit 6 of the register address is used for auto increment mode (default)
  - 01 -> bit 6 of the register address represents the even parity bit
  - 10 -> bit 6 of the register address represents the odd parity bit
- **OTP_ECC_STAT**: OTP Download flags:
  - 00: OTP download OK, no error.
  - 01: OTP download OK, 1 bit corrected.
  - 10: OTP download OK after n trays.
  - 11: OTP download completed with errors.
- **OTP_DOWNLOAD** :
  0 -> internal FSM is performing the OTP download
  1 -> internal FSM is not using OTP, OTP available
- **RESTART** : Command to reload the OTP trimming values: set it to '1' to start. It automatically reverts to 0 immediately after write. Use OTP_DOWNLOAD flag to understand when OTP downloading finishes.

Note: when IF_PARITY != 0, then the burst is auto-incremental by default.

Note: ENDIAN bit only affects the way data are stored into the registers, not the way data saved into the FIFO.

8.3 USER BANK #1 (Bank_sel = 0001)

Table 15: User Bank 1

Name	Register Address	Type	Default Value	Comment
INT_REF_X	*0x00*	RW	0000 0000	Interrupt Reference for X-axis
INT_REF_Y	*0x01*	RW	0000 0000	Interrupt Reference for Y-axis
INT_REF_Z	*0x02*	RW	0000 0000	Interrupt Reference for Z-axis
INT_DEB_X	*0x03*	RW	0000 0000	Interrupt Debounce, X
INT_DEB_Y	*0x04*	RW	0000 0000	Interrupt Debounce, Y
INT_DEB_Z	*0x05*	RW	0000 0000	Interrupt Debounce, Z
INT_MSK_X	*0x06*	RW	0000 0000	Interrupt Mask, X-axis zones
INT_MSK_Y	*0x07*	RW	0000 0000	Interrupt Mask, Y-axis zones
INT_MSK_Z	*0x08*	RW	0000 0000	Interrupt Mask, Z-axis zones
INT_MASK_AO	*0x09*	RW	0000 0000	Interrupt Masks, AND/OR
INT_CFG1	*0x0A*	RW	0000 0000	Interrupt Configuration #1
INT_CFG2	*0x0B*	RW	0010 0100	Interrupt Configuration #2
INT_TMO	*0x0C*	RW	0000 0000	Interrupt Timeout
INT_STS_UL	*0x0D*	R	0000 0000	Interrupt Sources, unlatched
INT_STS	*0x0E*	R	0000 0000	Interrupt status register
INT_MSK	*0x0F*	RW	1000 0010	Interrupt mask register
RFU	*0x10*	R	0000 0000	
RFU	*0x11*	R	0000 0000	
RFU	*0x12*	R	0000 0000	
RFU	*0x13*	R	0000 0000	
RFU	*0x14*	R	0000 0000	
RFU	*0x15*	R	0000 0000	
RFU	*0x16*	R	0000 0000	
INT_SRC_SEL	*0x17*	RW	00111100	Interrupt Source Selection
RFU	*0x18*	R	0000 0000	
RFU	*0x19*	R	0000 0000	
SERIAL_5	*0x1A*	R	Variable	Unique Serial Number, Byte 5
SERIAL_4	*0x1B*	R	Variable	Unique Serial Number, Byte 4
SERIAL_3	*0x1C*	R	Variable	Unique Serial Number, Byte 3
SERIAL_2	*0x1D*	R	Variable	Unique Serial Number, Byte 2
SERIAL_1	*0x1E*	R	Variable	Unique Serial Number, Byte 1
SERIAL_0	*0x1F*	R	Variable	Unique Serial Number, Byte 0

8.3.1 INT_REF_X

REG Name	**INT_REF_X: Interrupt Reference for X-axis, MSB**							
REG Address	Bank 1 - 0x00 (Hex) - 0 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_REF_X							

Description

Motion Interrupt Reference, X-axis.

Parameters

- **INT_REF_X**: These are the 8 MSB of the reference for interrupt of X direction. 8 LSB are assumed = 0x00. If INT_SINGLE_REF = '1', then the reference is { INT_REF_X, INT_REF_Y }, with **INT_REF_X** used as MSB and **INT_REF_Y** used as LSB.

8.3.2 INT_REF_Y

REG Name	**INT_REF_Y: Interrupt Reference for Y-axis, MSB**							
REG Address	Bank 1- 0x01 (Hex) - 1 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_REF_Y							

Description

Motion Interrupt Reference, Y-axis.

Parameters

- **INT_REF_Y**: These are the 8 MSB of the reference for interrupt of Y direction. 8 LSB are assumed = 0x00. If INT_SINGLE_REF = '1', then the reference is {INT_REF_X, INT_REF_Y}, with **INT_REF_X** as MSB and **INT_REF_Y** as LSB.

8.3.3 INT_REF_Z

REG Name	**INT_REF_Z: Interrupt Reference for Z-axis, MSB**							
REG Address	Bank 1- 0x02 (Hex) - 2 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	INT_REF_Z							

Description

Motion Interrupt Reference, Z-axis.

Parameters

- **INT_REF_Z**: These are the 8 MSB of the reference for interrupt of Z direction. 8 LSB are assumed = 0x00. If INT_SINGLE_REF = '1' the reference is {INT_REF_X, INT_REF_Y}, with **INT_REF_X** used as MSB and **INT_REF_Y** used as LSB.

8.3.4 INT_DEB_X

REG Name	**INT_DEB_X: Interrupt Debounce on X-axis**							
REG Address	Bank 1- 0x03(Hex) - 3 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000				RW-0000			
Content	RFU				INT_DEB_X			

Description

Motion Interrupt debounce register on X-axis.

This register determines how long (measured in number of samples) the selected AND/OR Motion Interrupt configuration has to stay asserted before the corresponding interrupt source bit is set and the interrupt on either INT1 or INT2 is eventually generated.

When the selected AND/OR Motion Interrupt configuration de-asserts (goes to 0) the corresponding interrupt source bit de-asserts immediately, without debounce.

Bits [7:4] is reserved.

Parameters

- **INT_DEB_X**: This register allows to count the number of samples (@ODR) requested to generate the Motion Interrupt signal for the X direction. If INT_SINGLE_DEB = '1' the debounce is {INT_DEB_X, INT_DEB_Y}, with INT_DEB_X used as MSB and INT_DEB_Y used as LSB.

8.3.5 INT_DEB_Y

REG Name	INT_DEB_Y: Interrupt Debounce on Y-axis							
REG Address	Bank - 0x04 (Hex) - 4 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000				RW-0000			
Content	RFU				INT_DEB_Y			

Description

Motion Interrupt debounce register on Y-axis.
This register determines how long (measured in number of samples) the selected AND/OR Motion Interrupt configuration has to stay asserted before the corresponding interrupt source bit is set and the interrupt on either INT1 or INT2 is eventually generated.
When the selected AND/OR Motion Interrupt configuration de-asserts (goes to 0) the corresponding interrupt source bit de-asserts immediately, without debounce
Bits [7:4] is reserved.

Parameters

- **INT_DEB_Y**: This register allows to count the number of samples (@ODR) requested to generate the interrupt signal for the Y direction. If INT_SINGLE_DEB = '1' the debounce is {INT_DEB_X, INT_DEB_Y}, with INT_DEB_X used as MSB and INT_DEB_Y used as LSB.

8.3.6 INT_DEB_Z

REG Name	INT_DEB_Z: Interrupt Debounce on Z-axis							
REG Address	Bank 1- 0x05 (Hex) - 5 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000				RW-0000			
Content	RFU				INT_DEB_Z			

Description

Motion Interrupt debounce register on Z-axis.
This register determines how long (measured in number of samples) the selected AND/OR Motion Interrupt configuration has to stay asserted before the corresponding interrupt source bit is set and the interrupt on either INT1 or INT2 is eventually generated.
When the selected AND/OR Motion Interrupt configuration de-asserts (goes to 0) the corresponding interrupt source bit de-asserts immediately, without debounce
Bits [7:4] is reserved.

Parameters

- **INT_DEB_Z**: This register allows to count the number of sample s(@ODR) requested to generate the interrupt signal for the Z direction. If INT_SINGLE_DEB = '1' the debounce is {INT_DEB_X, INT_DEB_Y}, with INT_DEB_X used as MSB and INT_DEB_Y used as LSB.

8.3.7 INT_MSK_X

REG Name	INT_MSK_X: Interrupt Mask X-axis							
REG Address	Bank 1- 0x06 (Hex) - 6 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000				R-0	R-0	R-0	R-0
Content	INT_MASK_X				X_HIGH_POS	X_LOW_POS	X_HIGH_NEG	X_LOW_NEG

Description

Motion Interrupt, X-axis configuration register.
This register comprises 2 fields. The 4 LSBs are read-only one-hot encoded bits which indicate whether the rate is positive or negative and whether it is above or below the rate threshold. The 4 MSBs are writable bits which enable, when set to 1, the generation of interrupts based on configurable AND/OR combination of some of them.

Parameters

- **INT_MASK_X**: For each bit, enables ('1') or disables ('0') the interrupt generation for the threshold event detection on the X-axis.
  - Bit4: enable ('1')/ disable ('0') the event X_LOW_NEG.
  - Bit5: enable ('1')/ disable ('0') the event X_HIGH_NEG.
  - Bit6: enable ('1')/ disable ('0') the event X_LOW_POS.
  - Bit7: enable ('1')/ disable ('0') the event X_HIGH_POS.

For example, writing INT_MASK_X = 4'b0100 enables the condition with X_LOW_POS only active to generate an interrupt.

- **X_HIGH_POS:** Signal is positive, above threshold
- **X_LOW_POS:** Signal is positive, below threshold
- **X_HIGH_NEG:** Signal is negative, above threshold
- **X_LOW_NEG:** Signal is negative, below threshold

See also Interrupt Zones drawing.

8.3.8 INT_MSK_Y

REG Name	INT_MSK_Y: Interrupt Mask Y-axis							
REG Address	Bank 1- 0x07 (Hex) – 7 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000				R-0	R-0	R-0	R-0
Content	INT_MASK_Y				Y_HIGH_POS	Y_LOW_POS	Y_HIGH_NEG	Y_LOW_NEG

Description

Motion Interrupt, Y-axis configuration register.
This register comprises 2 fields. The 4 LSBs are read-only one-hot encoded bits which indicate whether the rate is positive or negative and whether it is above or below the rate threshold.
The 4 MSBs are writable bits which enable, when set to 1, the generation of interrupts based on configurable AND/OR combination of some of them.

Parameters

- **INT_MASK_Y**: For each bit, enables ('1') or disables ('0') the interrupt generation for threshold event detection on the Y-axis.
  - Bit4: enable ('1')/ disable ('0') the event Y_LOW_NEG.
  - Bit5: enable ('1')/ disable ('0') the event Y_HIGH_NEG.
  - Bit6: enable ('1')/ disable ('0') the event Y_LOW_POS.
  - Bit7: enable ('1')/ disable ('0') the event Y_HIGH_POS.

For example, writing INT_MASK_Y = 4'b0100 enables the condition with Y_LOW_POS only to generate an interrupt.

Here is the meaning of the other bits:

- **Y_HIGH_POS:** Signal is positive, above the threshold
- **Y_LOW_POS:** Signal is positive, below threshold
- **Y_HIGH_NEG:** Signal is negative, above threshold
- **Y_LOW_NEG:** Signal is negative, below threshold

See also Interrupt Zones drawing.

8.3.9 INT_MSK_Z

REG Name	INT_MSK_Z: Interrupt Mask Z-axis							
REG Address	Bank 1- 0x08 (Hex) - 8 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0000				R-0	R-0	R-0	R-0
Content	INT_MASK_Z				Z_HIGH_POS	Z_LOW_POS	Z_HIGH_NEG	Z_LOW_NEG

Description

Motion Interrupt, Z-axis configuration register.
This register comprises 2 fields. The 4 LSBs are read-only one-hot encoded bits which indicate whether the rate is positive or negative and whether it is above or below the rate threshold. The 4 MSBs are writable bits which enable, when set to 1, the generation of interrupts based on configurable AND/OR combination of some of them.

Parameters

- **INT_MASK_Z**: For each bit, enables ('1') or disables ('0') the interrupt generation for the threshold event detection on the Z-axis.
  - Bit4: enable ('1')/ disable ('0') the event Z_LOW_NEG.
  - Bit5: enable ('1')/ disable ('0') the event Z_HIGH_NEG.
  - Bit6: enable ('1')/ disable ('0') the event Z_LOW_POS.
  - Bit7: enable ('1')/ disable ('0') the event Z_HIGH_POS.

For example, writing INT_MASK_Z = 4'b0100 enables the condition with Z_LOW_POS only to generate an interrupt.

Here is the meaning of the other bits:

- **Z_HIGH_POS:** Signal is positive, above threshold
- **Z_LOW_POS:** Signal is positive, below threshold
- **Z_HIGH_NEG:** Signal is negative, above threshold
- **Z_LOW_NEG:** Signal is negative, below threshold

See also Interrupt Zones drawing.

8.3.10 INT_MSK_AO

REG Name	INT_MASK_AO: Interrupt AND and Interrupt OR masks							
REG Address	Bank 1- 0x09 (Hex) - 9 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	RW-0	RW-000			RW-000		
Content	RFU	INT_FREEZE	INT_MASK_XYZ_AND			INT_MASK_XYZ_OR		

Description

Interrupt AND/OR masks register.

Parameters

- **INT_FREEZE:**

0 -> disables interrupts on threshold freeze;
1 -> enables interrupts on threshold freeze.

When INT_FREEZE = '1' the {X,Y,Z}_{HIGH,LOW}_{NEG,POS} flags hold values until interrupt will be cleared. The INT_FREEZE bit does not affect the behavior of the Interrupt Status Registers at locations 0x0E and 0x0F.

- **INT_MASK_XYZ_AND**: When the bit is set to 1 it's indicates that the corresponding direction is used in AND
- **INT_MASK_XYZ_OR**: When the bit is set to 1 it's indicates that the corresponding direction is used in OR

8.3.11 INT_CFG1

REG Name	**INT_CFG1: Interrupt 1 Configuration Register**							
REG Address	Bank 1- 0xA (Hex) – 10 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	RW-00		RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
Content	SNS_INTP_FSC		INT1_CLK_OUT	INT2_CLK_OUT	INT_SINGLE_DEB	INT_SINGLE_REF	SNS_INTP_HPF	RFU

Description

Interrupt 1 configuration register.

Parameters

- **SNS_INTP_FSC**: These two bits are used for set the Full scale used by Motion Interrupts:
  - 00 - 2000 dps (default)
  - 01 - 1000 dps
  - 10 - 500 dps
  - 11 - 250 dps
- **INT1_CLK_OUT**: INT1 pad drives out the internal clock (8.8MHz)
- **INT2_CLK_OUT**: INT2 pad drives out the internal clock (8.8MHz)
- **INT_SINGLE_DEB**: Single duration is used for all the direction.
  - int_deb_x used as MSB
  - int_deb_y used as LSB
- **INT_SINGLE_REF:** Single threshold is used for all the direction.
  - int_ref_x used as MSB
  - int_ref_y used as LSB
- **SNS_INTP_CFG:** activate the gyro interrupt data hi-pass filter:
  - 0 -> without hi-pass filtering
  - 1 -> with hi-pass filtering

8.3.12 INT_CFG2

REG Name	**INT_CFG2: Interrupt 2 Configuration Register**							
REG Address	Bank 1- 0xB (Hex) – 11 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type - Def. Value	R-0	RW-0	RW-1	RW-0	RW-0	RW-1	RW-0	RW-0
Content	RFU	MERGE_INT	INT1_ENABLE	INT1_ACT_LVL	INT1_MODE	INT2_ENABLE	INT2_ACT_LVL	INT2_MODE

Description

Interrupt 2 configuration register. This register determines how the interrupt lines INT1 and INT2 will behave in terms of :

- Merge Interrupts
- Being enabled/disabled
- Push-Pull vs Open-Drain configuration
- Active level

When the interrupt lines are disabled, they will stay at the selected un-active level regardless the settings in the INT_MSK registers.

Parameters

- **MERGE_INT** :
  - 0 -> INT1 and INT2 are separated
  - 1 -> INT2 is merged with INT1. Interrupt INT1 changes its outputs with both INT1 and INT2
- **INT1_ENABLE** :
  - 0 -> disable interrupt on INT1
  - 1 -> enable interrupt on INT1
- **INT1_ACT_LVL :**
  - 0 -> INT1 active High
  - 1 -> INT1 active low
- **INT1_ MODE :**
  - 0 -> push pull configuration
  - 1 -> open drain configuration
- **INT2_ENABLE** :
  - 0 -> disable interrupt on INT2
  - 1 -> enable interrupt on INT2
- **INT2_ ACT_LVL :**
  - 0 -> INT2 active High
  - 1 -> INT2 active low
- **INT2_ MODE :**
  - 0 -> push pull configuration
  - 1 -> open drain configuration

8.3.13 INT_TMO

REG Name	INT_TMO: Interrupt timeout and interrupt mode configuration							
REG Address	Bank 1- 0x0C (Hex) - 12 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00		RW-00		RW-0000			
Content	INT1_LATCH_MODE		INT2_LATCH_MODE		INT_TIMEOUT			

Description

Interrupt Timeout and Interrupt Mode configuration register.

This register allows to configure the interrupt lines to operate as either un-latched, latched or timed.

As un-latched, they can be further configured in such a way that interrupt sources (INT1_STS and INT2_STS) can be cleared when they are read or cleared when they are written with a logic 1.

Clearing an interrupt source by writing a logic 1 allows clearing single bits rather than the entire register.

#

Parameters

- **INT1_LATCH_MODE**:
  - 00 -> interrupt is not latched
  - 01 -> latched mode. Interrupt is maintained until cleared on Read
  - 10 -> latched mode. Interrupt is maintained until cleared on Write
  - 11 -> timed.
- **INT2_LATCH_MODE**:
  - 00 -> interrupt is not latched
  - 01 -> latched mode. Interrupt is maintained until cleared on Read
  - 10 -> latched mode. Interrupt is maintained until cleared on Write
  - 11 -> timed.

INT_TIMEOUT: Interrupt temporary period. This is sharing between INT1 and INT2:

- 0000 Temporary: 100us
- 0001 Temporary: 200us
- 0010 Temporary: 500us
- 0011 Temporary: 1ms
- 0100 Temporary: 2ms
- 0101 Temporary: 5ms
- 0110 Temporary: 10ms
- 0111 Temporary: 20ms
- 1000 Temporary: 50ms
- 1001 Temporary: 100ms
- 1010 Temporary: 200ms
- 1011 Temporary: 500ms

8.3.14 INT_STS_UL

REG Name	INT_STS_UL: Interrupt sources, unlatched							
REG Address	Bank 1- 0x0D (Hex) - 13 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	STS_UL_DATA_RDY	STS_UL_FIFO_EMPTY	STS_UL_FIFO_OVR	STS_UL_FIFO_TH	STS_UL_INT_AND	STS_UL_INT_OR	STS_UL_OTP_DOWNLOAD	STS_UL_DSYNC

Description

Interrupt sources, un-latched. These bits are the un-latched version of the interrupt status registers; as these signals are shared by the INT1 generator and the INT2 generator, there is a unique register shared.

This register is the actual source for the interrupt lines when the interrupts are configured as un-latched.

When the interrupt lines are configured as latched, be it both or just one of them, these bits can be used to keep monitoring the status of an interrupt source, previously identified by means of its latched version, to see how it changes after the event.

Parameters

- **STS_UL_DATA_RDY** : DATA_READY status bit (0x22[0])
- **STS_UL_FIFO_EMPTY** : FIFO empty status bit (0x3D[0])
- **STS_UL_FIFO_OVR** : FIFO overrun status bit (0x3D[4])
- **STS_UL_FIFO_TH** : FIFO threshold status bit (0x3D[2])
- **STS_UL_INT_AND** : Motion Interrupt OR status
- **STS_UL_INT_OR** : Motion Interrupt AND status
- **STS_UL_ OTP_DOWNLOAD** : OTP download status (0x1C[0])
- **STS_UL_DSYNC** : data sync pin status, according to DSYNC_CFG

8.3.15 INT_STS

REG Name	INT_STS: Interrupt status register (latched)							
REG Address	Bank 1- 0x0E (Hex) - 14 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
Content	STS_I1_DATA_RDY	STS_I1_FIFO_EMPTY	STS_I1_FIFO_OVR	STS_I1_FIFO_TH	STS_I2_INT_AND	STS_I2_INT_OR	STS_I2_OTP_DOWNLOAD	STS_1_DSYNC

Description

Interrupt status register. These are the latched interrupt sources.

When INT is configured to operate as latched, it can be cleared, when asserted, in two ways:

- Clear-On-Read: by reading the entire INT_STS register
- Clear-On-Write: by selectively writing with ‚1' the specific interrupt source bit in INT_STS register, until they are all cleared. Many bits can be cleared at once by forming the appropriate mask.

When INT is configured to operate as either latched or timed, these registers are set to 0.

Parameters

- **STS_I1_DATA_RDY** : DATA_READY status bit (always unlatched)
- **STS_I1_FIFO_EMPTY** : FIFO empty status bit (unlatched if INT1_LATCHED_MODE is configured to be timed)
- **STS_I1_FIFO_OVR** **:** FIFO overrun status bit
- **STS_I1_FIFO_TH** **:** FIFO threshold status bit
- **STS_I2_INT_AND** **:** Motion Interrupt OR status
- **STS_I2_INT_OR** **:** Motion Interrupt AND status
- **STS_I2_OTP_DOWNLOAD** **:** OTP download status
- **STS_I2_DSYNC** **:** data sync pin status, according to DSYNC_CFG

8.3.16 INT_MSK

REG Name	INT_MSK: Interrupt mask register (latched)							
REG Address	Bank 1- 0x0F (Hex) - 15 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-1	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1	RW-0
Content	MSK_I1_DATA_RDY	MSK_I1_FIFO_EMPTY	MSK_I1_FIFO_OVR	MSK_I1_FIFO_TH	MSK_I2_INT_AND	MSK_I2_INT_OR	MSK_I2_RESTART	MSK_I2_DSYNC

Description

Interrupt mask register. This register is meant to be used to enable selected interrupt sources in the INT_STS (0x0E) register to activate the INT interrupt line. Interrupt sources are masked (prevented from generating an interrupt) as long as the corresponding bit in the mask register is 0.

Valid configurations are with None, One, Multiple or Every bit set to 1; having multiple possible interrupt sources will require the Interrupt Service routine to identify the correct one(s).

Parameters

- **MSK_I1_DATA_RDY** : DATA_READY mask bit
- **MSK_I1_FIFO_EMPTY** : FIFO empty mask bit
- **MSK_I1_FIFO_OVR** **:** FIFO overrun mask bit
- **MSK_I1_FIFO_TH** **:** FIFO threshold mask bit
- **MSK_I2_INT_AND** **:** Motion Interrupt OR mask bit
- **MSK_I2_INT_OR** **:** Motion Interrupt AND mask bit
- **MSK_I2_ OTP_DOWNLOAD** **:** OTP download mask bit
- **MSK_I2_DSYNC** **:** data sync pin mask bit, according to DSYNC_CFG

8.3.17 INT_SRC_SEL

REG Name	INT_SRC_SEL: Motion Interrupt Source Selection							
REG Address	Bank 1- 0x17 (Hex) - 23 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-0	RW-0	RW-1	RW-1	RW-1	RW-1	RW-00	
Content	RFU	RFU	MSK_GYR_INT_D_RDY	MSK_ACC_INT_D_RDY	MSK_MAG_INT_D_RDY	MSK_QUA_INT_D_RDY	INT_SRC_SEL	

Description

Motion Interrupt Source selection register.

Parameters

- **MSK_GYR_INT_D_RDY** : When '1' a new gyro data set contributes to data ready interrupt assertion
- **MSK_ACC_INT_D_RDY** : When '1' a new accelerometer data set contributes to data ready interrupt assertion
- **MSK_MAG_INT_D_RDY** : When '1' a new magnetometer data set contributes to data ready interrupt assertion
- **MSK_QUA_INT_D_RDY** : When '1' a new quaternion data set contributes to data ready interrupt assertion

- **INT_SRC_SEL** =
  - 00: gyr_x, gyr_y, gyr_z
  - 10: norm(a_hpf), norm(a_hpf), norm(a_pre_hpf)
  - 11: norm(a_hpf), norm(a_pre_hpf), norm(a_pre_hpf)

8.3.18 SERIAL_5

REG Name	**SERIAL_5: Serial Number byte 5**							
REG Address	Bank 1- 0x1A (Hex) – 26 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_5							

Description

Serial number, byte 5 register. SERIAL_X registers (with X going from 0 to 5) are 6 registers used to assign a unique identifier to every single MAX21100 sample to enable a complete track-ability of each of them, in terms of LOTs, Assembly history and Test equipment.

Parameters

- **SERIAL_5** : Serial number, byte 5

8.3.19 SERIAL_4

REG Name	**SERIAL_4: Serial Number byte 4**							
REG Address	Bank 1- 0x1B (Hex) – 27 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_4							

Description

Serial number, byte 4 register.

Parameters

- **SERIAL_4** : Serial number, byte 4

8.3.20 SERIAL_3

REG Name	**SERIAL_3: Serial Number byte 3**							
REG Address	Bank 1- 0x1C (Hex) – 28 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_3							

Description

Serial number, byte 3 register.

Parameters

- **SERIAL_3** : Serial number, byte 3

8.3.21 SERIAL_2

REG Name	**SERIAL_2: Serial Number byte 2**							
REG Address	Bank 1- 0x1D (Hex) – 29 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_2							

Description

Serial number, byte 2 register. SERIAL_X registers (with X going from 0 to 5) are 6 registers used to assign a unique identifier to every single MAX21100 sample to enable a complete track-ability of each of them, in terms of LOTs, assembly history and Test equipment.

Parameters

- **SERIAL_2** : Serial number, byte 2

8.3.22 SERIAL_1

REG Name	**SERIAL_1: Serial Number byte 1**							
REG Address	Bank – 0x1E (Hex) – 30 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_1							

Description

Serial number, byte 1 register.

Parameters

- **SERIAL_1** : Serial number, byte 1

8.3.23 SERIAL_0

REG Name	**SERIAL_0: Serial Number byte 0**							
REG Address	Bank 1- 0x1F (Hex) – 31 (Dec)							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Type – Def. Value	R	R	R	R	R	R	R	R
Content	SERIAL_0							

Description

Serial number, byte 0 register.

Parameters

- **SERIAL_0** : Serial number, byte 0

8.4 USER BANK #2 (Bank_sel = 0010)

Table 16: User Bank 2

Name	Register Address	Type	Default Value	Comment
QUAT0_H	*0x00*	R	0000 0000	MSB of QUATERNION 0
QUAT0_L	*0x01*	R	0000 0000	LSB of QUATERNION 0
QUAT1_H	*0x02*	R	0000 0000	MSB of QUATERNION 1
QUAT1_L	*0x03*	R	0000 0000	LSB of QUATERNION 1
QUAT2_H	*0x04*	R	0000 0000	MSB of QUATERNION 2
QUAT2_L	*0x05*	R	0000 0000	LSB of QUATERNION 2
QUAT3_H	*0x06*	R	0000 0000	MSB of QUATERNION 3
QUAT3_L	*0x07*	R	0000 0000	LSB of QUATERNION 3
RFU	*0x08*	R	0000 0000	
RFU	*0x09*	R	0000 0000	
RFU	*0x0A*	R	0000 0000	
RFU	*0x0B*	R	0000 0000	
RFU	*0x0C*	R	0000 0000	
RFU	*0x0D*	R	0000 0000	
RFU	*0x0E*	R	0000 0000	
RFU	*0x0F*	R	0000 0000	
RFU	*0x10*	R	0000 0000	
RFU	*0x11*	R	0000 0000	
RFU	*0x12*	R	0000 0000	
BIAS_GYRO_X_H	*0x13*	RW	0000 0000	GYRO Bias Compensation, X-MSB
BIAS_GYRO_X_L	*0x14*	RW	0000 0000	GYRO Bias Compensation, X-LSB
BIAS_GYRO_Y_H	*0x15*	RW	0000 0000	GYRO Bias Compensation, X-MSB
BIAS_GYRO_Y_L	*0x16*	RW	0000 0000	GYRO Bias Compensation, X-LSB
BIAS_GYRO_Z_H	*0x17*	RW	0000 0000	GYRO Bias Compensation, X-MSB
BIAS_GYRO_Z_L	*0x18*	RW	0000 0000	GYRO Bias Compensation, X-LSB
BIAS_COMP_ACC_X	*0x19*	RW	0000 0000	ACC Bias Compensation, X
BIAS_COMP_ACC_Y	*0x1A*	RW	0000 0000	ACC Bias Compensation, Y
BIAS_COMP_ACC_Z	*0x1B*	RW	0000 0000	ACC Bias Compensation, Z
FUS_CFG0	*0x1C*	RW	0000 0000	Fusion Engine Configuration Reg. 0
FUS_CFG1	*0x1D*	RW	0101 1000	Fusion Engine Configuration Reg. 1
RFU	*0x1E*	R	0000 0000	
GYR_ODR_TRIM	*0x1F*	RW	0000 0000	Output ODR Trimming Register

8.4.1 QUAT0_H

REG Name	**QUAT0_H: Quaternion Data, MSB**							
REG Address	Bank 2- 0x00 (Hex) – 0 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_0_MSB							

Description

This register stores the most recent quaternion measurement, specifically the MSB of the component 0 of the quaternion.

Parameters

- **QUATERNION_0_MSB**

8.4.2 QUAT0_L

REG Name	**QUAT0_L: Quaternion Data, LSB**							
REG Address	Bank 2- 0x01 (Hex) – 1 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_0_LSB							

Description

This register stores the most recent quaternion measurement, specifically the LSB of the component 0 of the quaternion.

Parameters

- **QUATERNION_0_LSB**

8.4.3 QUAT1_H

REG Name	**QUAT1_H: Quaternion Data, MSB**							
REG Address	Bank 2- 0x02 (Hex) – 2 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_1_MSB							

Description

This register stores the most recent quaternion measurement, specifically the MSB of the component 1 of the quaternion.

Parameters

- **QUATERNION_1_MSB**

8.4.4 QUAT1_L

REG Name	**QUAT1_L: Quaternion Data, LSB**							
REG Address	Bank 2- 0x03 (Hex) – 3 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_1_LSB							

Description

This register stores the most recent quaternion measurement, specifically the LSB of the component 1 of the quaternion.

Parameters

- **QUATERNION_1_LSB**

8.4.5 QUAT2_H

REG Name	**QUAT2_H: Quaternion Data, MSB**							
REG Address	Bank 2- 0x04 (Hex) – 4 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_2_MSB							

Description

This register stores the most recent quaternion measurement, specifically the MSB of the component 2 of the quaternion.

Parameters

- **QUATERNION_2_MSB**

8.4.6 QUAT2_L

REG Name	**QUAT1_L: Quaternion Data, LSB**							
REG Address	Bank 2- 0x05 (Hex) – 5 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_2_LSB							

Description

This register stores the most recent quaternion measurement, specifically the LSB of the component 2 of the quaternion.

Parameters

- **QUATERNION_2_LSB**

8.4.7 QUAT3_H

REG Name	**QUAT3_H: Quaternion Data, MSB**							
REG Address	Bank 2- 0x06 (Hex) – 6 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_3_MSB							

Description

This register stores the most recent quaternion measurement, specifically the MSB of the component 2 of the quaternion.

Parameters

- **QUATERNION_3_MSB**

8.4.8 QUAT3_L

REG Name	**QUAT3_L: Quaternion Data, LSB**							
REG Address	Bank 2- 0x07 (Hex) – 7 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-00000000							
Content	QUATERNION_3_LSB							

Description

This register stores the most recent quaternion measurement, specifically the LSB of the component 2 of the quaternion.

Parameters

QUATERNION_3_LSB

8.4.9 BIAS_GYRO_X_H

REG Name	**BIAS_GYRO_X_H: GYRO Bias Compensation, X-MSB**							
REG Address	Bank 2- 0x13 (Hex) – 19 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-000			RW-00000				
Content	RFU			BIAS_GYRO_X_H				

Description

This register stores the MSB of the GYRO bias estimate, X axis.

Parameters

- BIAS_GYRO_X_H

8.4.10 BIAS_GYRO_X_L

REG Name	**BIAS_GYRO_X_L: GYRO Bias Compensation, X-LSB**							
REG Address	Bank 2- 0x14 (Hex) – 20 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	BIAS_GYRO_X_L							

Description

This register stores the LSB of the GYRO bias estimate, X axis.

Parameters

- BIAS_GYRO_X_L

8.4.11 BIAS_GYRO_Y_H

REG Name	**BIAS_GYRO_Y_H: GYRO Bias Compensation, Y-MSB**							
REG Address	Bank 2- 0x15 (Hex) – 21 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-000			RW-00000				
Content	RFU			BIAS_GYRO_Y_H				

Description

This register stores the MSB of the GYRO bias estimate, Y axis.

Parameters

- BIAS_GYRO_Y_H

8.4.12 BIAS_GYRO_Y_L

REG Name	**BIAS_GYRO_Y_L: GYRO Bias Compensation, Y-LSB**							
REG Address	Bank 2- 0x16 (Hex) – 22 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	BIAS_GYRO_Y_L							

Description

This register stores the LSB of the GYRO bias estimate, Y axis.

Parameters

- BIAS_GYRO_Y_L

8.4.13 BIAS_GYRO_Z_H

REG Name	**BIAS_GYRO_Z_H: GYRO Bias Compensation, Z-MSB**							
REG Address	Bank 2- 0x17 (Hex) – 23 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-000			RW-00000				
Content	RFU			BIAS_GYRO_Z_H				

Description

This register stores the MSB of the GYRO bias estimate, Z axis.

Parameters

- BIAS_GYRO_Z_H

8.4.14 BIAS_GYRO_Z_L

REG Name	**BIAS_GYRO_Z_L: GYRO Bias Compensation, Z-LSB**							
REG Address	Bank 2- 0x18 (Hex) – 24 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-00000000							
Content	BIAS_GYRO_Z_L							

Description

This register stores the LSB of the GYRO bias estimate, Z axis.

Parameters

- BIAS_GYRO_Z_L

8.4.15 BIAS_COMP_ACC_X

REG Name	**BIAS_COMP_ACC_X: Accelerometer Bias Compensation, X-axis**							
REG Address	Bank 2- 0x19 (Hex) – 25 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	RW-00000000						
Content	RFU	BIAS_COMP_ACC_X						

Description

This register stores the the accelerometer bias estimate, X axis.

Parameters

- BIAS_COMP_ACC_X

8.4.16 BIAS_COMP_ACC_Y

REG Name	**BIAS_COMP_ACC_Y: Accelerometer Bias Compensation, Y-axis**							
REG Address	Bank 2- 0x1A (Hex) – 26 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	RW-00000000						
Content	RFU	BIAS_COMP_ACC_Y						

Description

This register stores the accelerometer bias estimate, Y axis.

Parameters

- BIAS_COMP_ACC_Y

8.4.17 BIAS_COMP_ACC_Z

REG Name	**BIAS_COMP_ACC_Z: Accelerometer Bias Compensation, Z-axis**							
REG Address	Bank 2- 0x1B (Hex) – 27 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0	RW-00000000						
Content	RFU	BIAS_COMP_ACC_Z						

Description

This register stores the accelerometer bias estimate, Z axis.

Parameters

- BIAS_COMP_ACC_Z

8.4.18 FUS_CFG_0

REG Name	**FUS_CFG_0: Fusion Configuration 0**							
REG Address	Bank 2- 0x1C (Hex) – 28 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-000			RW-0	RW-0	RW-00		RW-0
Content	FUS_ ODR			FUS_GR_HD	FUS_AUTO_MODE	FUS_MODE		FUS_EN

Description

The fusion configuration 0

Parameters

- FUS_ODR: Fusion ODR ratio

FUS_ ODR	ODR ratio
000	SNS_ODR(default)
001	SNS_ODR /2
010	SNS_ODR /4
011	SNS_ODR /8
100	SNS_ODR 16
101	SNS_ODR /32
110	SNS_ODR /64
111	SNS_ODR /128

- FUS_GR_HD: when set to '1', gravity and heading estimation is enabled and outputed in place of quaternion
- FUS_AUTO_MODE: when set to '1', the fusion mode is automatically managed according to power modes and sensor anormalies
- FUS_MODE : Four modes in total which is described as following:
  00 -> Gryo + Accelerometer + Magnetometer
  01 -> Accelerometer + Magnetometer
  10 -> Gryo
  11 -> Gyro + Accelerometer + Magnetermeter
- FUS_EN: when set to '1', activate the fusion generation

8.4.19 FUS_CFG_1

REG Name	**FUS_CFG_1: Fusion Configuration 1**							
REG Address	Bank 2- 0x1D (Hex) – 29 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	RW-010			RW-11		RW-0	RW-0	RW-0
Content	FUS_ALPHA0_TRIM			FUS_ALPHA1_TRIM		FORCE_MAG_ABNORMAL	MAG_A BNORMAL_MON	MAG_SW

Description

The fusion configuration 1

Parameters

- FUS_ALPHA0_TRIM : the parameter alpha 0 of adaptive filter

FUS_ALPHA0_TRIM	Parameter alpha 0 of adaptive filter
000	0.95
001	0.96
010	0.97(default)

011	0.98
100	0.99
101	0.994
110	0.997
111	0.999

- FUS_ALPHA1_TRIM : the parameter alpha 1 of adaptive filter

FUS_ALPHA1_TRIM	Parameter alpha 1 of adaptive filter
0	alpha0
1	alpha0 *2/3 +1/3
2	alpha0 *1/3 +2/3
3	1(default)

- **FORCE_MAG_ABNORMAL** : When set high, magnetometer abnormality is emulated by SW
- **MAG_ABNORMAL_MON** : When set high, Mag X read data LSB is used as active high magnetometer abnormal monitor information.
- **MAG_SW** : When set high, magnetometer data is provided externally via SW on ofset fileds after SW compensation.

8.4.20 GYR_ODR_TRIM

REG Name	**GYR_ODR_TRIM: Output ODR correction**							
REG Address	Bank 2- 0x1F(Hex) – 31 (Dec)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Type - Def. Value	R-0000				R-0	R-0	R-0	RW-0
Content	GYR_ODR_CORR				GYR_OK	ACC_OK	MAG_OK	RFU

Parameters

- FUS_ODR: Fusion ODR ratio

GYR_ODR_CORR	Real gryo ODR correction factor
0000	GYR_ODR_CORR = 0.901(real gyro ODR is 11 % higher than expected)
0001	GYR_ODR_CORR = 0.915
0010	GYR_ODR_CORR = 0.928
0011	GYR_ODR_CORR = 0.942
0100	GYR_ODR_CORR = 0.956
0101	GYR_ODR_CORR = 0.971
0110	GYR_ODR_CORR = 0.985
0111	GYR_ODR_CORR = 1.000
1000	GYR_ODR_CORR = 1.015
1001	GYR_ODR_CORR = 1.030

1010	GYR_ODR_CORR = 1.046
1011	GYR_ODR_CORR = 1.061
1100	GYR_ODR_CORR = 1.077
1101	GYR_ODR_CORR = 1.093
1110	GYR_ODR_CORR = 1.110
1111	GYR_ODR_CORR = 1.126(real gyro ODR is 12.6% lower than expected)

- GYR_OK: read back infomation, gyro drive loop is locked in amplitude and gyro sense chain is active
- ACC_OK: read back information, accelerometer sense chain is active.
- MAG_OK: read back information, magnetometer is active and no magnetic abnormal is detected.

9 FIFO Modes description

The MAX21100 embeds a 256-slot of a 16-bit data FIFO for each of the three output channels, yaw, pitch, and roll. This allows a consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. When configured in Snapshot mode, it offers the ideal mechanism to capture the data following a Motion Interrupt event.
This buffer can work according to four main different modes: Off, Normal, Interrupt and Snapshot.
Both Normal and Interrupt modes can be optionally configured to operate in Overrun Mode, depending on whether, in case of buffer under-run, newer or older data are lost.

9.1 FIFO OFF mode

In this mode, the FIFO is turned off; data are stored only in the data registers (0x23 to 0x28.
No data are available from FIFO if read. When the FIFO is turned OFF, there are two options to use the device: synchronous and asynchronous reading.

9.2 Synchronous Reading

In this mode, the processor reads the data set (e.g. 6 bytes for a 3 axes configuration) generated by the MAX21100 every time that DATA_READY is set. The processor must read once and only once the data set in order to avoid data inconsistencies.
Benefits of using this approach include the perfect reconstruction of the signal coming the gyroscope and minimum data traffic.

9.3 Asynchronous Reading

In this mode, the processor reads the data generated by the MAX21100 regardless the status of the DATA_READY flag. To minimize the error caused by different samples being read a different number of times, the access frequency to be used must be higher than the selected ODR. Depending on whether the DATA_READY flag is checked or not, the reading frequency can be in order of 2X or must be 10X higher to limit the adverse effect of unevenly resampled data. This approach normally requires much higher BW.

9.4 FIFO Normal mode

9.4.1 Overrun = false

- FIFO is turned on.
- FIFO is filled with the data at the selected Output Data Rate (ODR).
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, all the new incoming data will be discharged. Reading only a subset of the data already stored into the FIFO keeps locked the possibility for new data to be written.
- Only if all the data are read the FIFO will restart saving data.
- If communication speed is high, data loss can be prevented.
- In order to prevent a “FIFO-full” condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be lost.

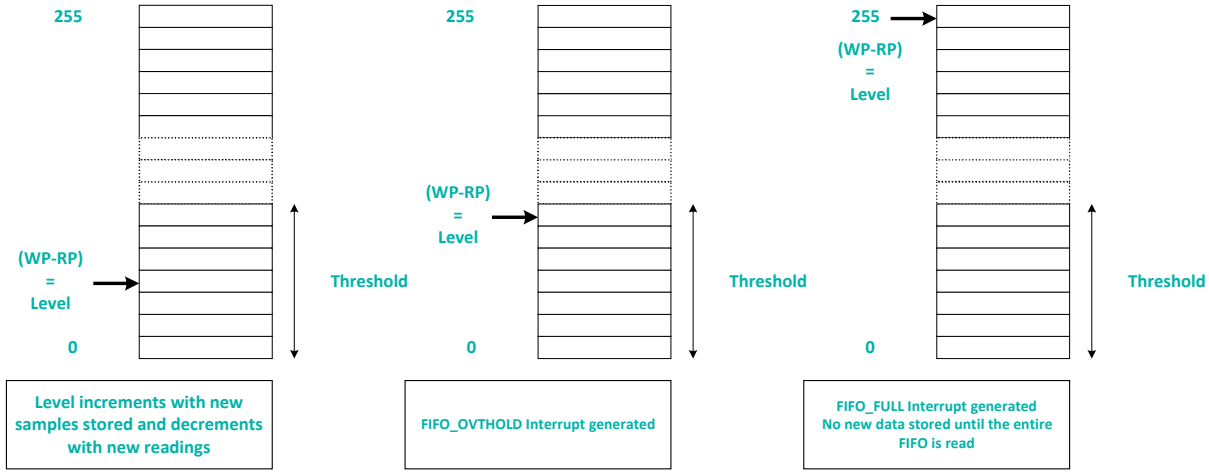


Figure 10: FIFO Normal mode, Overrun = False

9.4.2 Overrun = true

- FIFO is turned on.
- FIFO is filled with the data at the selected ODR.
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, the oldest data will be overwritten with the new ones.
- If communication speed is high, data integrity can be preserved.
- In order to prevent a DATA_LOST condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be overwritten.
- When an overrun condition occurs the Reading pointer is forced to Writing Pointer -1, to make sure only older data are discarded and newer data have a chance to be read.

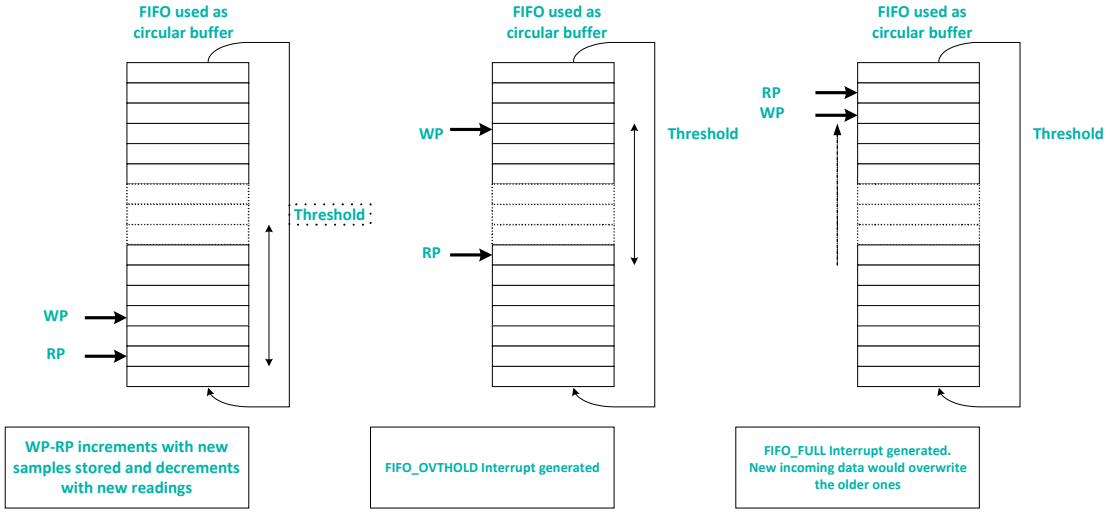


Figure 11: FIFO Normal mode, Overrun = True

9.5 Interrupt Mode

9.5.1 Overrun = false

- FIFO is initially disabled. Data are stored only in the data registers.
- When a Motion Interrupt (either OR or AND) is generated, the FIFO is turned automatically. It stores the data at the selected ODR. Motion Interrupt are documented starting from INT_REF_X.
- When FIFO is full, all the new incoming data will be discharged. Reading only a subset of the data already stored into the FIFO keeps locked the possibility for new data to be written.
- Only if all the data are read the FIFO will restart saving data.
- If communication speed is high, data loss can be prevented.
- In order to prevent a "FIFO-full" condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be lost.

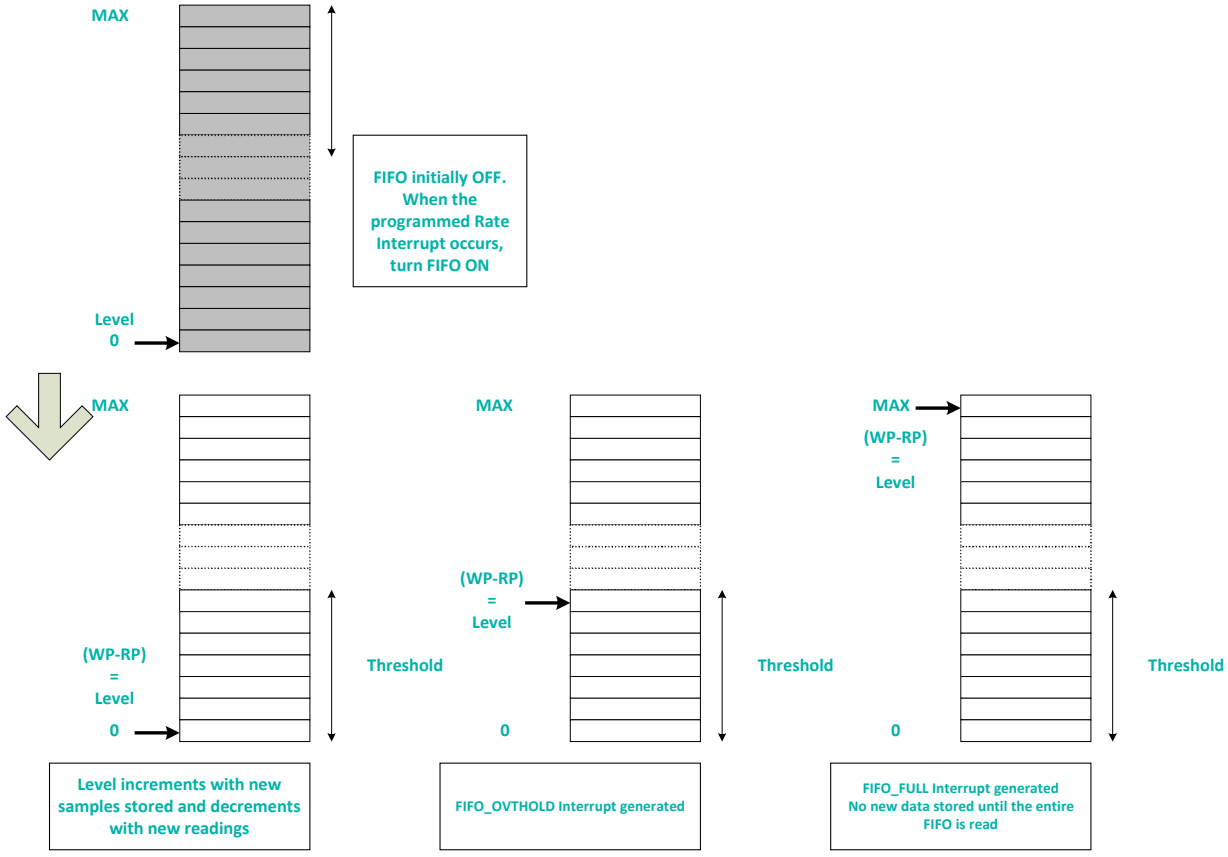


Figure 12: FIFO Interrupt mode, Overrun = False

9.5.2 Overrun = true

- FIFO is initially disabled. Data are stored only in the data registers.
- When a Motion Interrupt (either OR or AND) is generated, the FIFO is turned automatically. It stores the data at the selected ODR. Motion Interrupt are documented starting from INT_REF_X.
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, the oldest data will be overwritten with the new ones.
- If communication speed is high, data integrity can be preserved.
- In order to prevent a DATA_LOST condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be overwritten.
- When an overrun condition occurs the Reading pointer is forced to Writing Pointer -1, to make sure only older data are discarded and newer data have a chance to be read.

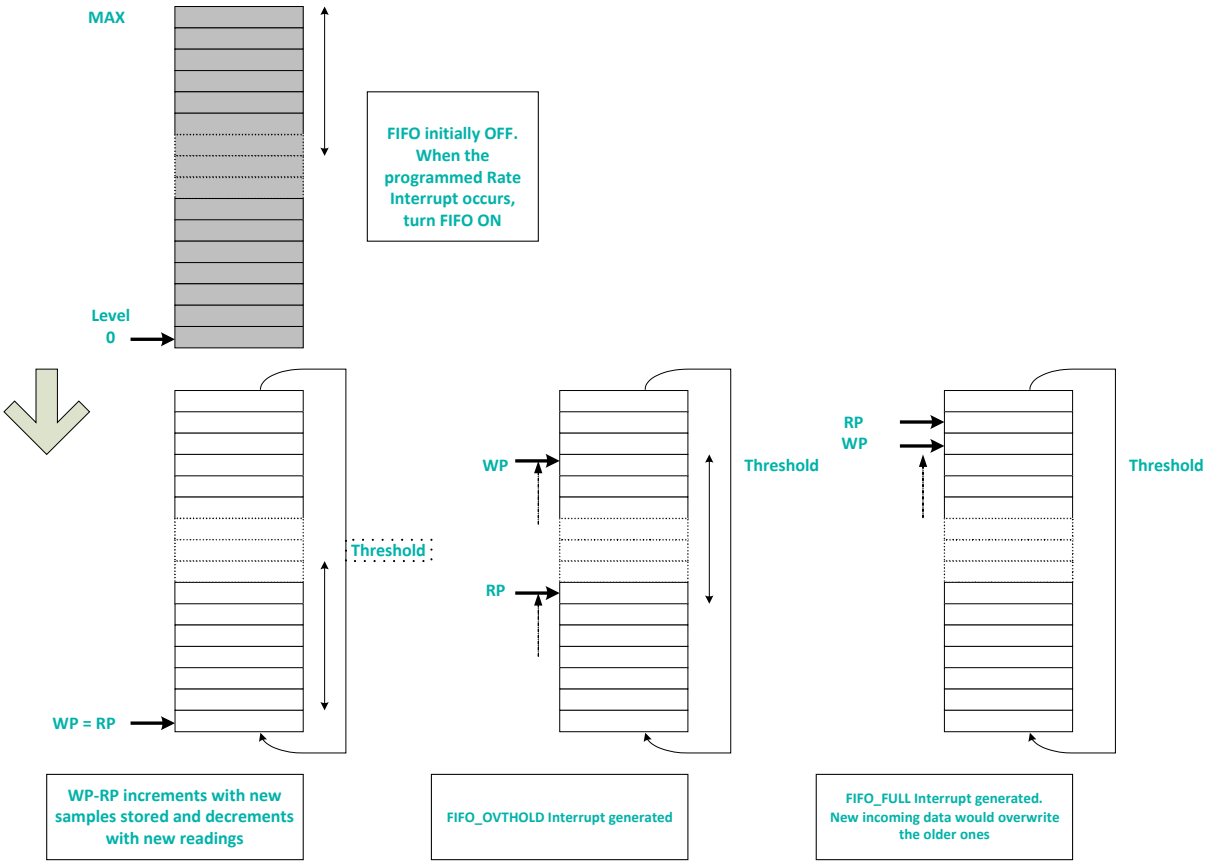


Figure 13: FIFO Interrupt mode, Overrun = True

9.6 Snapshot Mode

- FIFO is initially in normal mode with overrun enabled.
- When a Motion Interrupt (either OR or AND) is generated, the FIFO switches automatically to not-overrun mode. It stores the data at the selected ODR until the FIFO becomes full.
- When FIFO is full, an interrupt can be generated.
- When FIFO is full, all the new incoming data will be discharged. Reading only a subset of the data already stored into the FIFO keeps locked the possibility for new data to be written.
- Only if all the data are read the FIFO will restart saving data.
- If communication speed is high, data loss can be prevented.
- In order to prevent a “FIFO_FULL” condition, the required condition is to complete the reading of the data set before the next DATA_READY occurs.
- If this condition is not guaranteed, data can be lost.

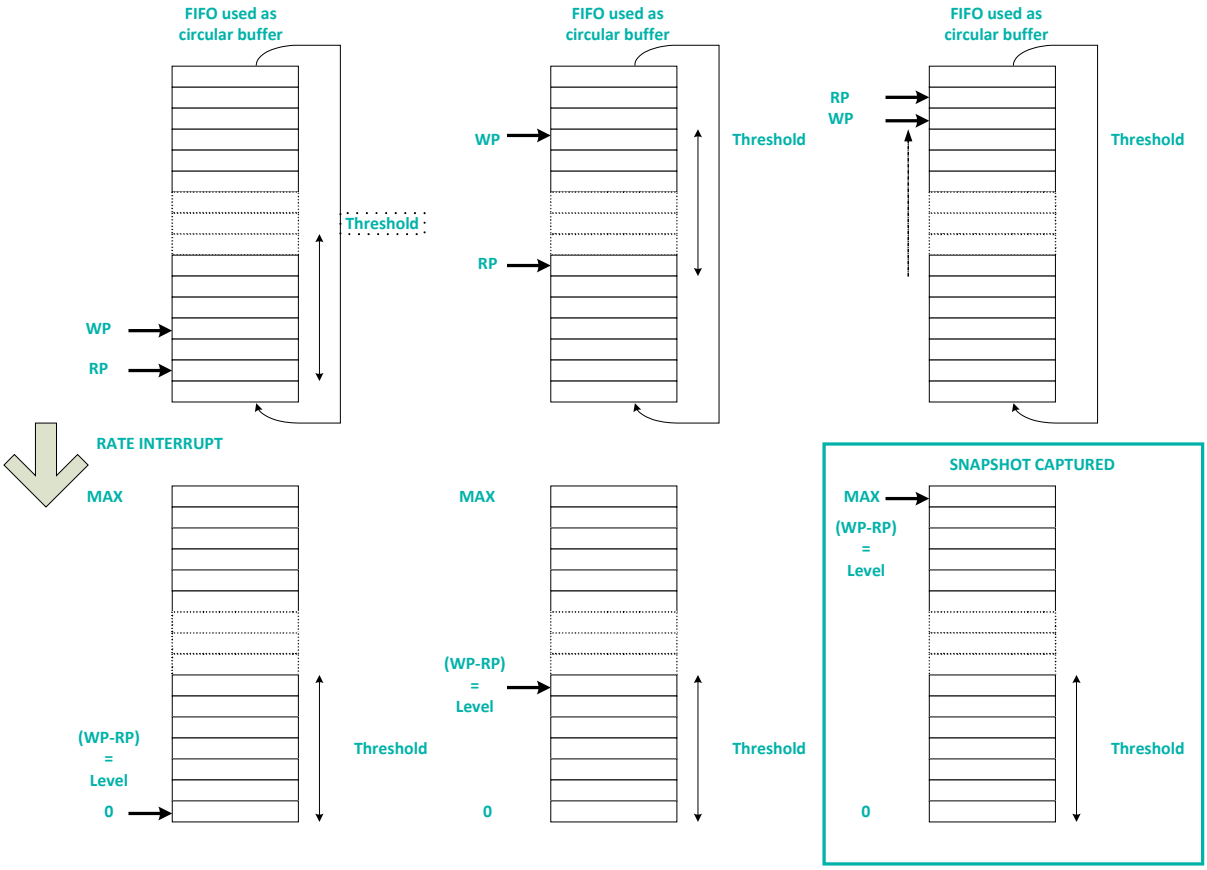


Figure 14: FIFO Snapshot mode

10 Rate Zones for Motion Interrupt generation

The following diagram shows how the bits in registers 0x06, 0x07 and 0x08 are generated based on the threshold defined at registers 0x00, 0x01 and 0x02.

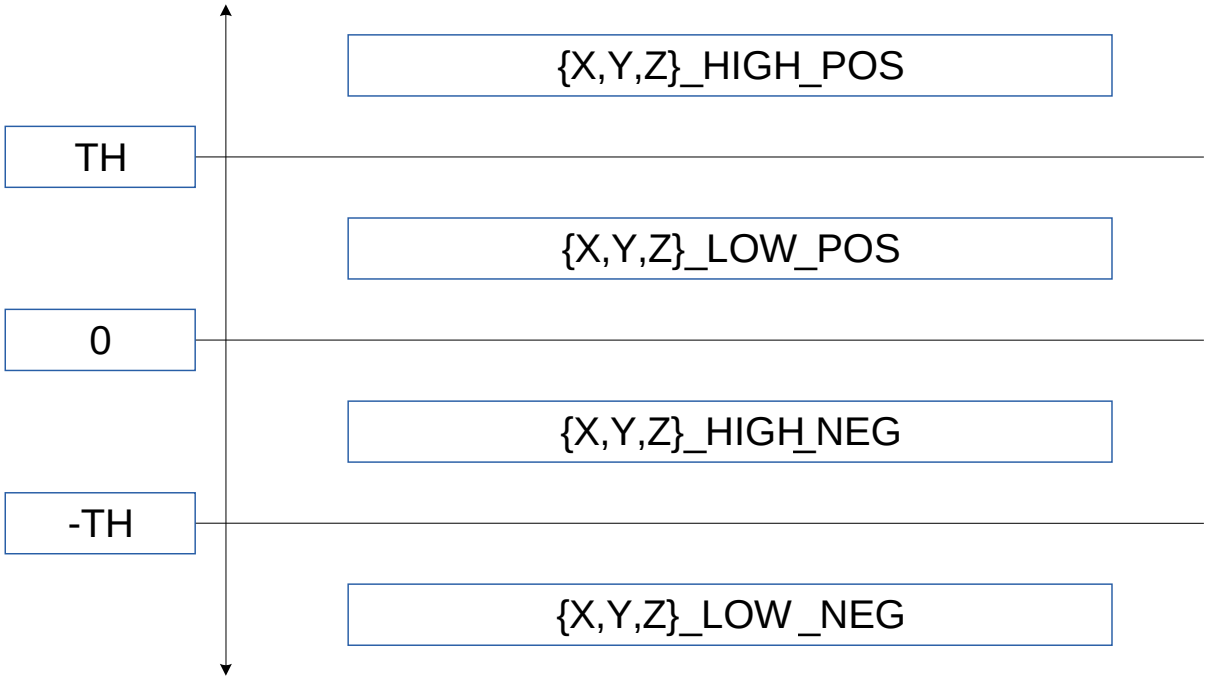
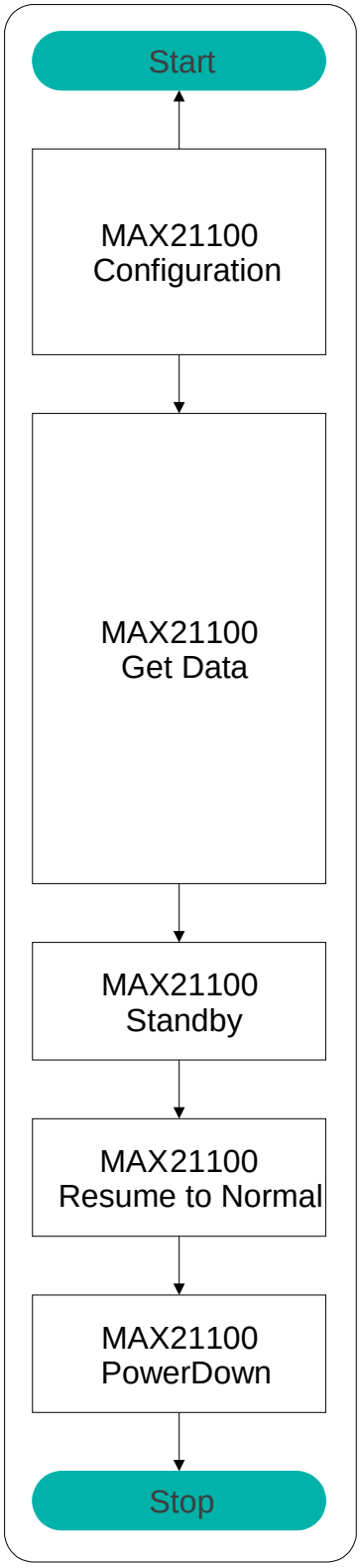


Figure 15: Interrupt Zones

11 Programming Examples

11.1 Simple read-out sequence, no FIFO, no Interrupts




```
MAX21100_Write (ADD_34, 00h) // BNK 00
MAX21100_Write (ADD_00, 07h) // 2kdps FS, 3D
MAX21100_Write (ADD_01, 10h) // 10Hz BW
MAX21100_Write (ADD_02, 01h) // 4 KHz ODR
MAX21100_Write (ADD_00, 17h) // Normal Mode
```

```
While (keep_reading_flag) {
While (
 MAX21100_Read (ADD_35) // wait DATA_READY
    ==00
) {}
X_H = MAX21100_Read (ADD_36)// MSB X
X_L = MAX21100_Read (ADD_37)// LSB X
Y_H = MAX21100_Read (ADD_38)// MSB Y
Y_L = MAX21100_Read (ADD_39)// LSB Y
Z_H = MAX21100_Read (ADD_40)// MSB Z
Z_L = MAX21100_Read (ADD_41)// LSB Z
}
```

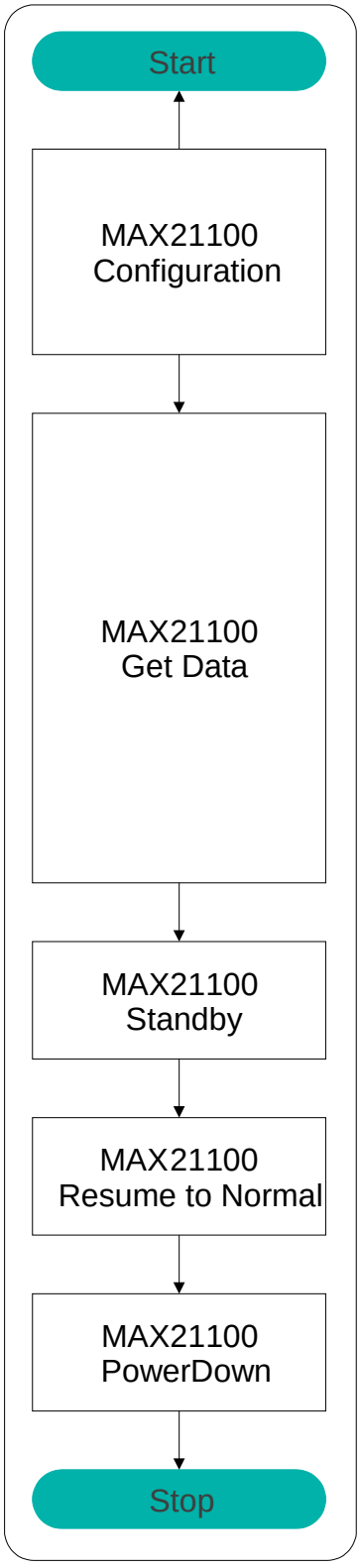
```
MAX21100_Write (ADD_00, 0Fh) // Standby Mode
```

```
MAX21100_Write (ADD_00, 0Fh) // Normal Mode
```

```
MAX21100_Write (ADD_00, 00h) // PowerDown Mode
```

Figure 16: MAX21100 Programming Example #1

11.2 Simple read-out sequence, FIFO normal mode, no Interrupts




```
MAX21100_Write (ADD_34, 00h) // BNK 00
MAX21100_Write (ADD_00, 07h) // 2kdps FS, 3D
MAX21100_Write (ADD_01, 10h) // 10Hz BW
MAX21100_Write (ADD_02, 01h) // 4 KHz ODR
MAX21100_Write (ADD_00, 17h) // Normal Mode
MAX21100_Write (ADD_26, 3Eh) // FIFO Thr. = 126
MAX21100_Write (ADD_24, 41h) // FIFO Mode = NORM
& store Gyro data

While (keep_reading_flag) {
While (
  MAX21100_Read (ADD_61) // wait FIFO Thr.
    !Over_threshold
) {}
DATA_VEC =
MAX21100_BURST_Read_NO_AUTO_INCR (ADD_62,
threshold)
for(cnt = 0; cnt< threshold; cnt+=6) {
X[n] = DATA_VEC(cnt)  << 8 OR DATA_VEC(cnt+1)// X
Y[n] = DATA_VEC(cnt+2)<< 8 OR DATA_VEC(cnt+3)//
Y
Z[n] = DATA_VEC(cnt+4)<< 8 OR DATA_VEC(cnt+5)//
Z
}
}
```

```
MAX21100_Write (ADD_00, 0Fh) // Standby Mode
```

```
MAX21100_Write (ADD_00, 17h) // Normal Mode
```

```
MAX21100_Write (ADD_00, 00h) // // PowerDown
Mode
```

Figure 17: MAX21100 Programming Example #2

12 Example of FIFO Read/Write Pointers evolution

The following drawing assumes:

1) A reading frequency roughly twice the writing frequency (ODR)
2) A FIFO threshold = 126d

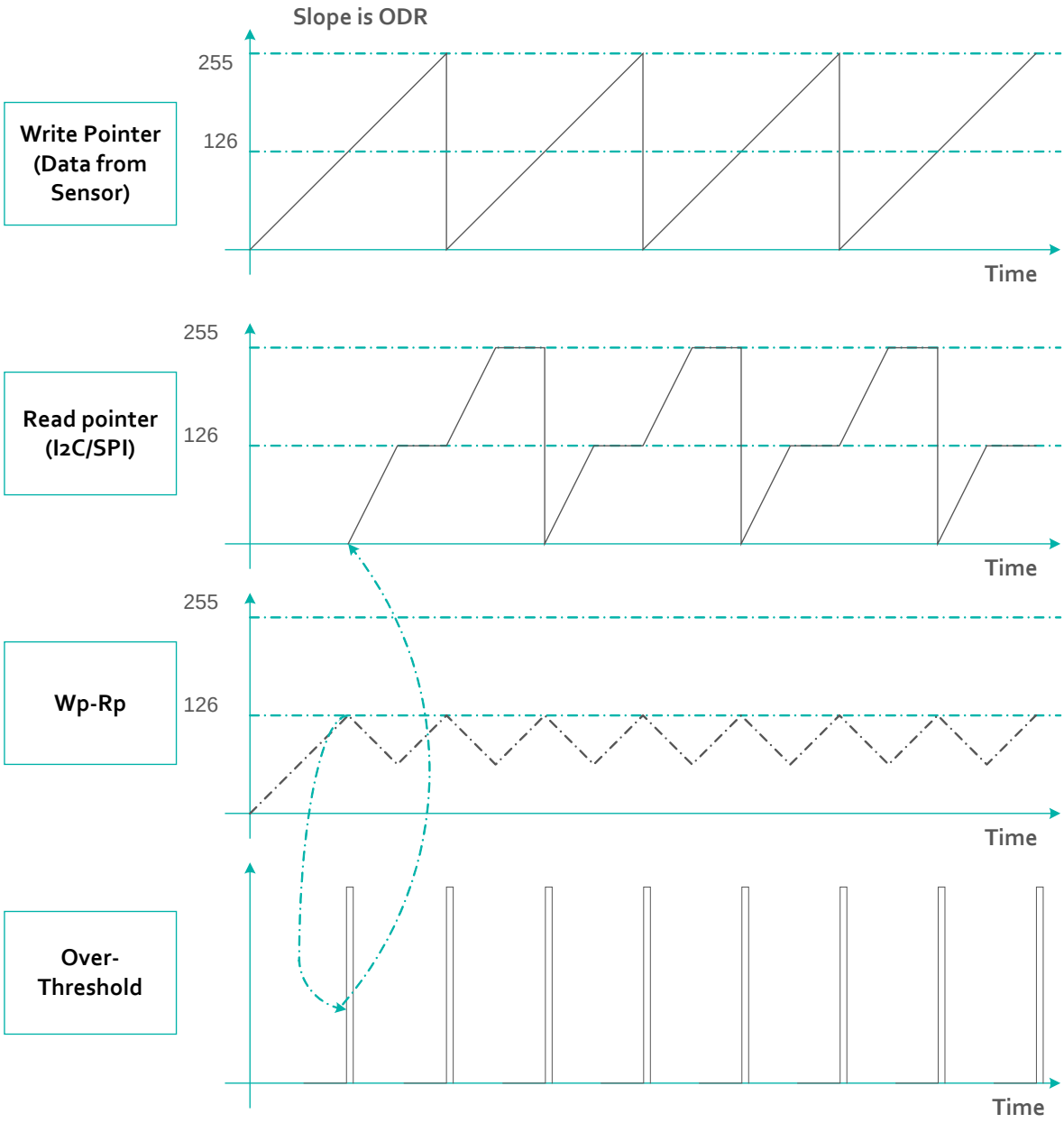


Figure 18: FIFO Pointers in FIFO wi

13 Application Schematic

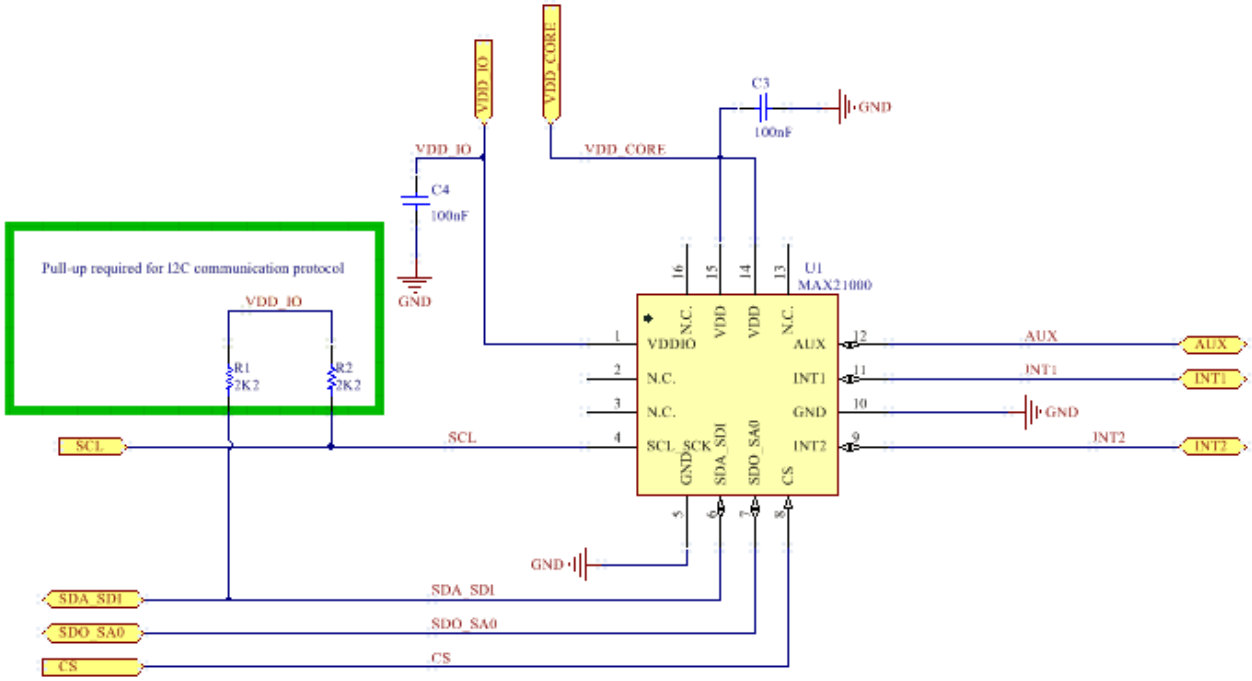


Figure 19: Application Schematic

14 Soldering Guidelines

MEMS based sensors are sensitive to Printed Circuit Board (PCB) reflow processes. For minimum Zero-Rate-Level drift after PCB mounting, care must be taken to PCB layout and reflow conditions. The purpose of this section is to provide the guidelines meant to minimize the stress of the package after soldering and board mounting.

Information provided here is based on experiments executed on LGA devices. They do not represent exact conditions present at a customer site. Hence, information herein should be used as a guidance only and process and design optimizations are recommended to develop an application specific solution.

1. The PCB land should be designed with Non Solder Mask Defined (NSMD).
2. PCB land pad is 0.8mm x 0.45mm which is the size of the package pad plus 0.1mm.
3. The area below the sensor (on the same side of the board) must be defined as keep-out area. It is strongly recommended to not place any structure in top metal layer underneath the sensor.
4. The solder mask opening is equal to the size of the PCB land pad plus an extra 0.1mm.
5. Do not place any components or vias at a distance less than 2mm from the package land area. This may cause additional package stress if it is too close to the package land area.
6. Signal traces connected to pads should be as symmetric as possible. Symmetry and balance for pad connection will help component self alignment and will lead to a better control of solder paste reduction after reflow.
7. Put dummy traces on N/C pads in order to have same length of exposed trace for all pads. Signal traces with 0.1mm width and min. 0.5mm length for all PCB land pads near the package are recommended. Wider trace can be continued after the 0.5mm zone.
8. It is recommended to use a cleanable solder paste with an additional cleaning step after SMT mount.
9. Do not use a screw down or stacking to fix the PCB into an enclosure because this could bend the PCB putting stress on the package.
10. The stencil aperture size is equal to the PCB land pad – 0.025mm. Also note that for the 4 corner pads the aperture size must be larger for solder.
11. Stencil aperture should have rectangular shape with dimension up to 25 µm (1 mil) smaller than PCB land.
12. The openings of the stencil for the signal pads should be between 70% and 90% of the PCB pad area.
13. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
14. The fine pitch of the IC leads requires accurate alignment of the stencil to the printed circuit board. The stencil and printed circuit assembly should be aligned to within 25 µm (1 mil) prior to application of the solder paste.
15. The recommended peak temperature for the solder paste for lead free (Pb-free) is 245°C - 250°C and for the tin-lead (Sn-Pb), 215°C - 225°C.

16. The PCB should be rated for the multiple lead-free reflow condition with max 260°C temperature.

15 Definitions

Power supply [V]: This parameter defines the operating DC power supply voltage range of the MEMS gyroscope. Although it is always a good practice to keep Vdd clean with minimum ripple, unlike most of the competitors, who require an ultra-low noise, low-dropout regulator to power the MEMS gyroscope, the MAX21100 can not only operate at 1.71V but that supply can also be provided by a switching regular, to minimize the system power consumption.
Power supply current [mA]: This parameter defines the typical current consumption when the MEMS gyroscope is operating in normal mode.
Power supply current in Standby mode [mA]: This parameter defines the current consumption when the MEMS gyroscope is in Standby mode. To reduce power consumption and have a faster turn-on time, in Standby mode only an appropriate subset of the sensor is turned off.
Power supply current in ECO mode [mA]: This parameter defines the current consumption when the MEMS gyroscope is in a special mode named ECO Mode. Whilst in ECO Mode, the MAX21100 reduces significantly the power consumption, at the price of a slightly higher RND.
Power supply current in stand-by mode [µA]: This parameter defines the current consumption when the MEMS gyroscope is powered down. In this mode, both the mechanical sensing structure and reading chain are turned off. Users can configure the control register through the I2C/SPI interface for this mode. Full access to the control registers through the I2C/SPI interface is guaranteed also in power-down mode.
Full-scale range [dps]: This parameter defines the measurement range of the gyroscope in degrees per second (dps). When the applied angular velocity is beyond the full-scale range, the gyroscope output signal will be saturated.
Zero-rate level [LSBs]: This parameter defines the zero rate level when there is no angular velocity applied to the gyroscope.
Sensitivity [mdps/LSB]: Sensitivity (mdps/LSB) is the relationship between 1 LSB and milli dps. It can be used to convert a digital gyroscope's measurement in LSBs to angular velocity.
Sensitivity change vs. Temperature [%/°C]: This parameter defines the sensitivity change in percentage (%) over the operating temperature range specified in the datasheet.
Zero-rate level change vs. Temperature [dps/°C]: This parameter defines defines the zero-rate level change in dps/°C over the operating temperature range.
Non-linearity [% FS]: This parameter defines the maximum error between the gyroscope's outputs and the best-fit straight line in percentage with respect to the full-scale (FS) range.
System bandwidth [Hz]: This parameter defines the frequency of the angular velocity signal from DC to the built-in bandwidth (BW) that the gyroscopes can measure. A dedicated register can be modified to adjust the gyroscope's bandwidth.

Rate noise density [dps/√ Hz]: This parameter defines the standard resolution that users can get from the gyroscopes outputs together with the BW parameter.
Self-test [dps]: This feature can be used to verify if the gyroscope is working properly or in order to not physically rotate the gyroscope after it is assembled on a PCB. When the self test is enabled, an internal electrostatic force is generated to move the masses to simulate the Coriolis effect. If the gyroscope's outputs are within the specified self-test values in the datasheet, then the gyroscope is working properly. Therefore, the self-test feature is an important consideration in a user's end-product mass production line.

16 Document History

Version	Date	Author/Changes	Modifications
1.0	03/06/2013	I.Binda	
1.1	04/07/2013	I.Binda/C.Iascone/L.Sala/W. Wu	update the fusion registers
1.2	07/15/2013	W. Wu	update the registers description to the V103B
1.2	07/31/2013	W. Wu / L.Sala	General Description updated Block diagram updated Application diagram updated Package size corrected Typos corrected
1.4	1/24/2014	W.Wu	changes to description