Capstone Project

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Efficient filtering and Processing Technique based on Adaptive Rate Sampling

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Introduction

- **Motivation :** Smart embedded systems for mobile applications

  Reduced cost, size, processing noise, electromagnetic emission and especially power consumption

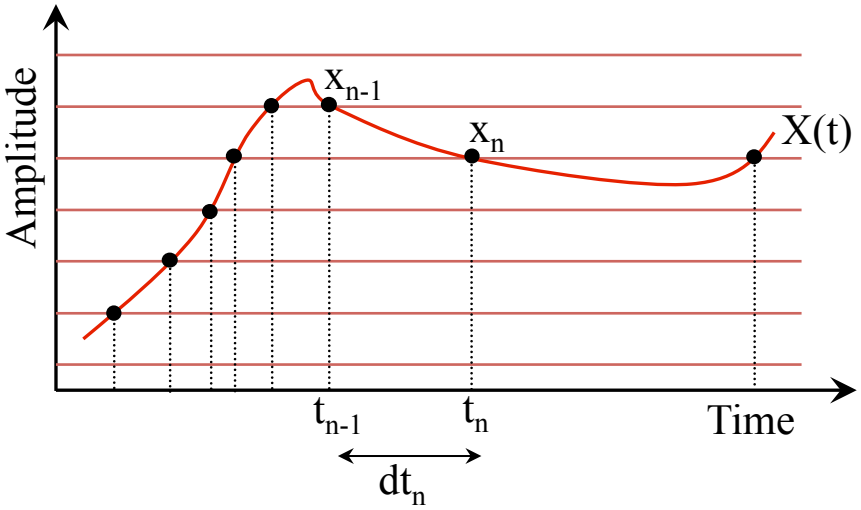
- **Project focus:** Enhance the digital filtering techniques often involves trade-offs

- **Solution :** Reorganize the signal processing theory ands architecture

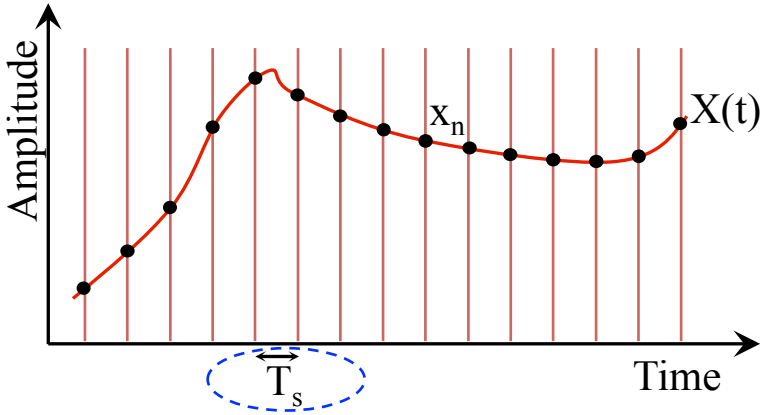
  Signal driven acquisition and processing with smart circuit design

Proposed Sampling Approach: Event driven sampling (EDS)

- EDS (Event-Driven Sampling), which adapts the sampling rate according to the input signal local variations and thus reduces the processing activity.
- (only relevant number of samples to process).



EDS Sampling



Classical Sampling

Proposed Filtering Approach

The FIR Filtering Process:

FIR filters are one primary type of digital filters used in Digital Signal Processing (DSP) applications. "FIR" means "Finite Impulse Response". If you put in an impulse, that is, a single "1" sample followed by many "0" samples, zeroes will come out after the "1" sample has made its way through the delay line of the filter.

-Time domain implementation

P is the filter order.

$$y_n = h_k * x_n = \sum_{k=0}^{P} h_k . x_{n-k}$$

-Frequency domain implementation

$$Y(f) = H(f).X(f)$$

Event driven filtering

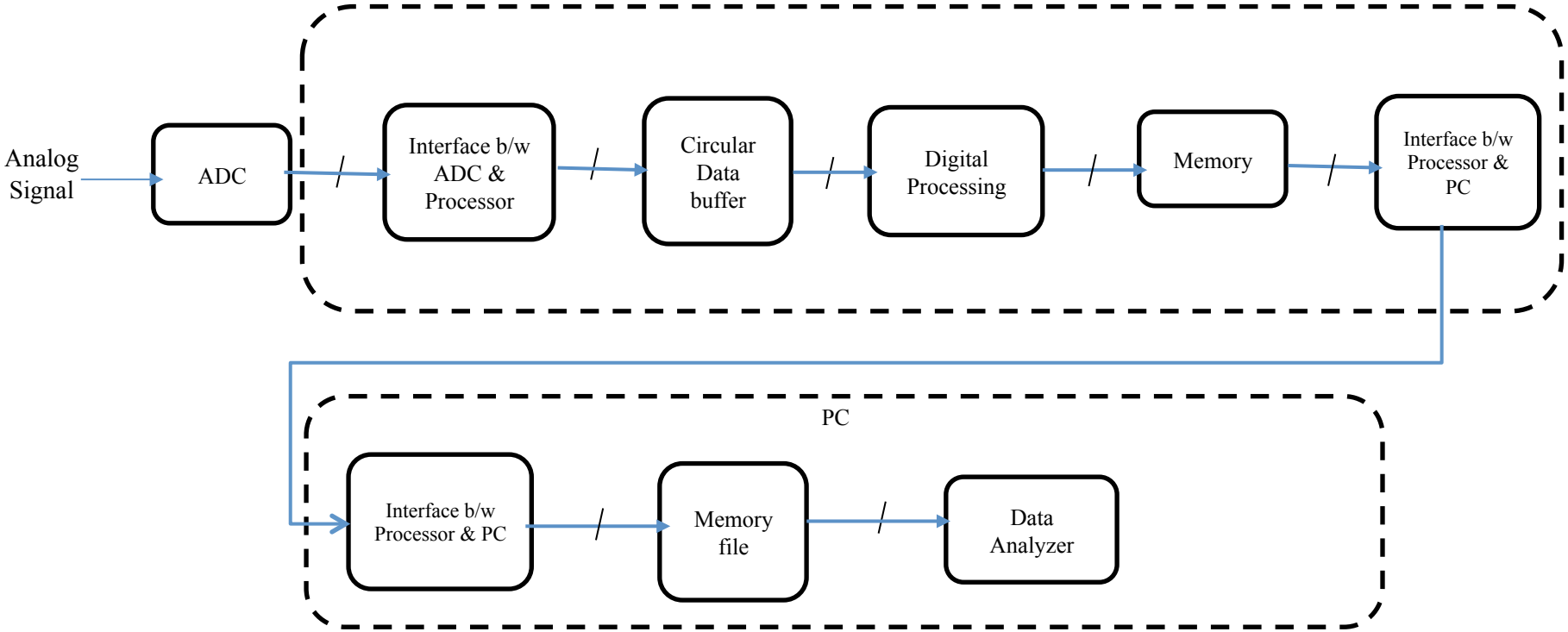
- Event driven filtering (only relevant number of operation to deliver per filtered output).

Advantages of Event Driven Filtering

$$y_n = h_k * x_n = \sum_{k=0}^{P} h_k . x_{n-k}$$

- Computational complexity
  - CLASSICAL CASE: N.P+1 MULTIPLICATIONS AND N.P Additions
  - EDF case: M.P+1 MULTIPLICATIONS AND M.P Additions
- Here M<N.
- In case of speech communication the activity is 25% of the overall communication duration

Principle Block Diagram



1. ADC

The conversion process starts by sampling the input analog signal (discretizing) and then rounding off these samples amplitudes (quantization) that will produce the quantized signal.

- Quantization Error

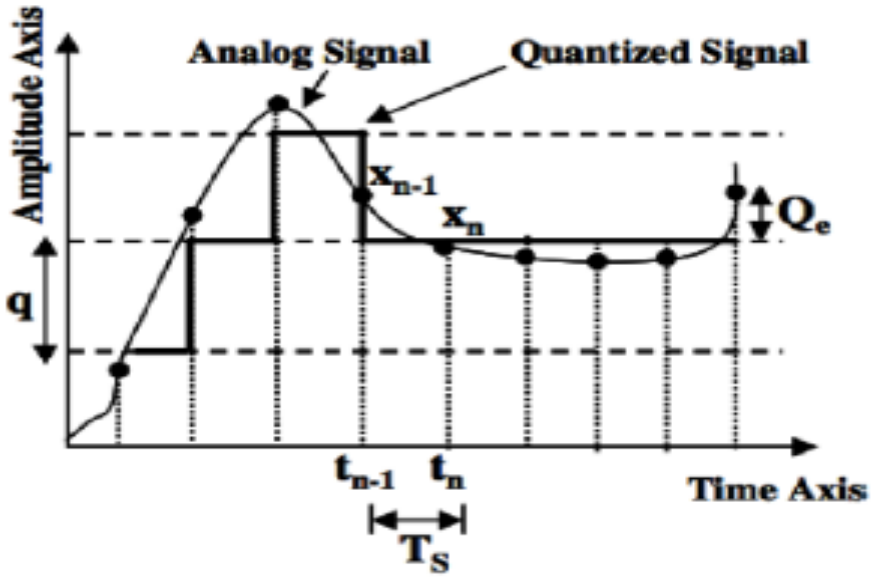
$$RMS(Q_e(t)) = \frac{q}{\sqrt{12}}$$

- SNR:

- $$SNR(dB) = 6.02.M + 1.76$$

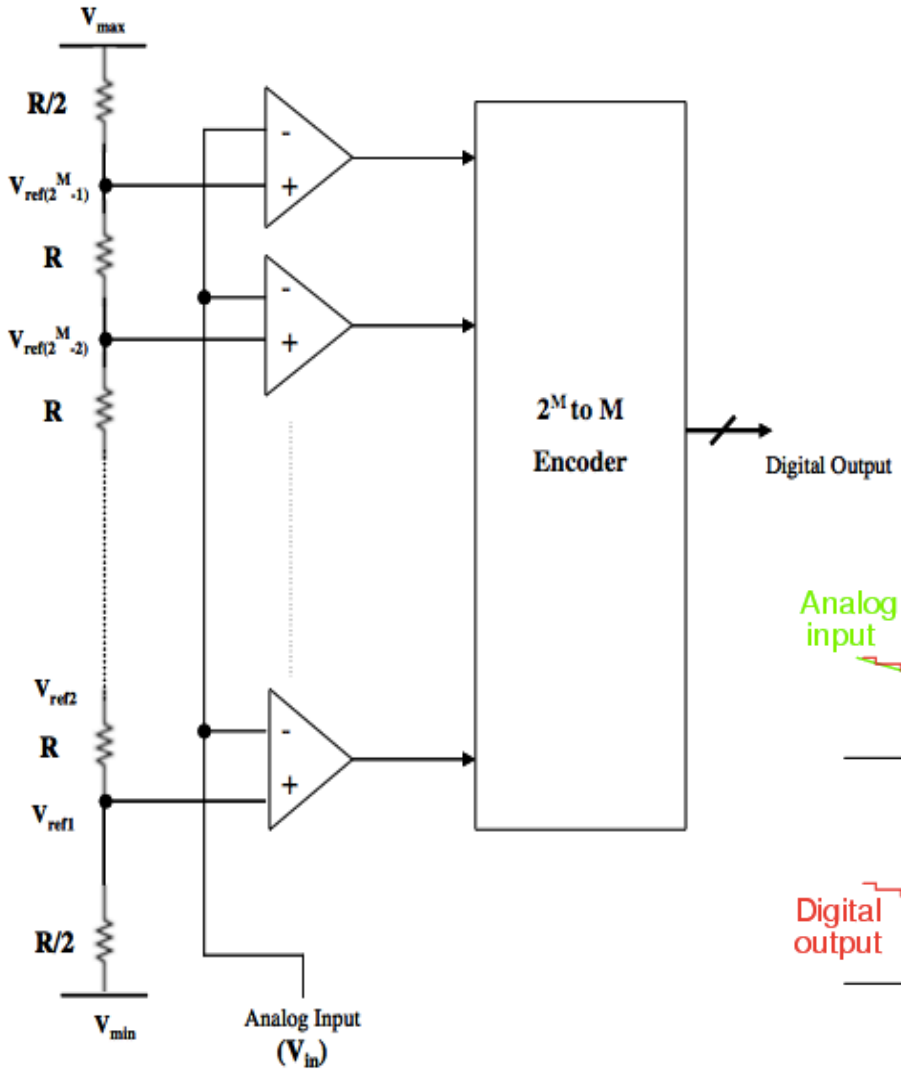
- THD:

$$THD = \frac{\sum Harmonics\ Power}{Fundamental\ Component\ Power}$$

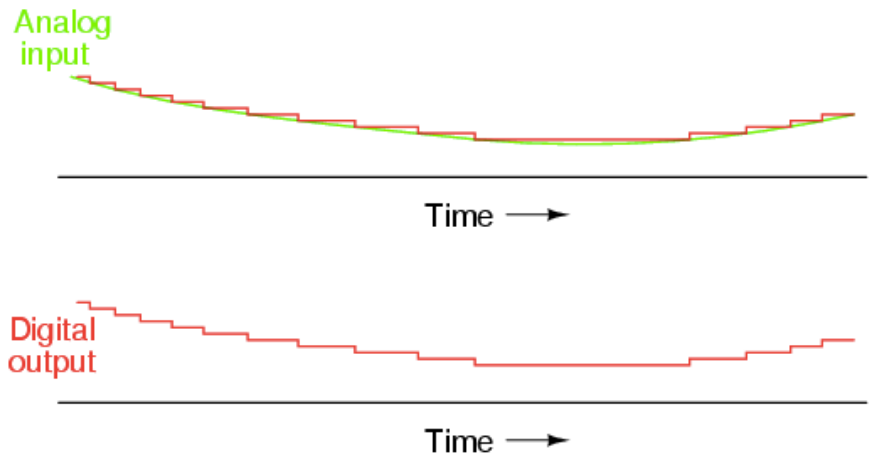


1.1 Flash ADC

Architecture :



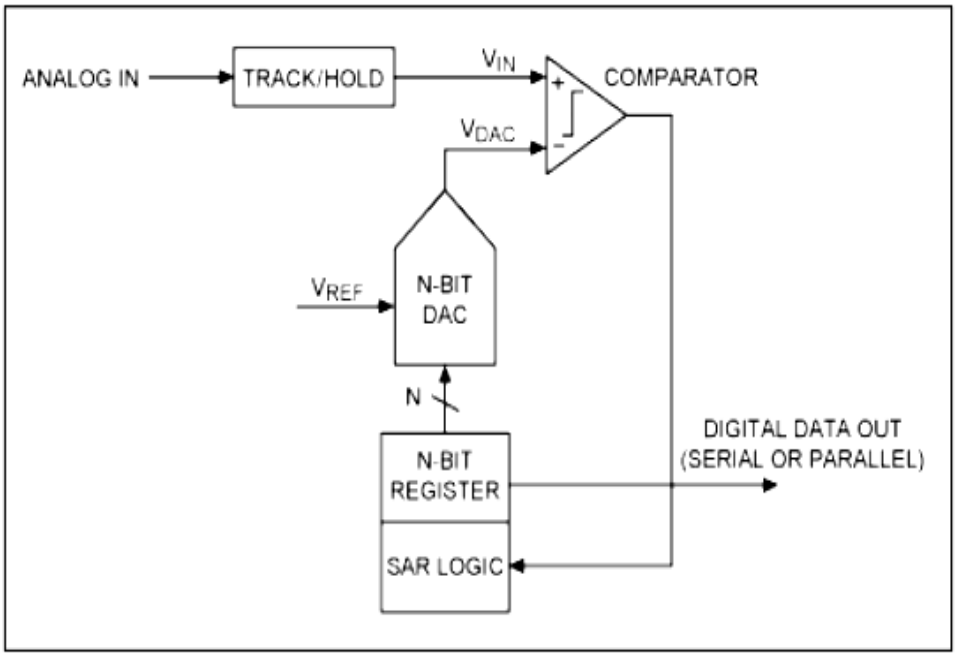
- Vrefrance for each comparator is one LSB greater than the reference voltage for the comparator below it.
- Comparator compare between Vref and V input , when Vinput > Vref comparator produce 1 otherwise gives 0.
- Output of comparator then goes to 2^M to M encoder producing a digital output. The Digital output would look like figure 4.



1.2 SAR ADC

- A type of analog to digital converter that operates using a binary search algorithm.

- Uses a successive approximation register that counts by going through all possible combinations starting from the most significant bit and finishing with the least significant bit.

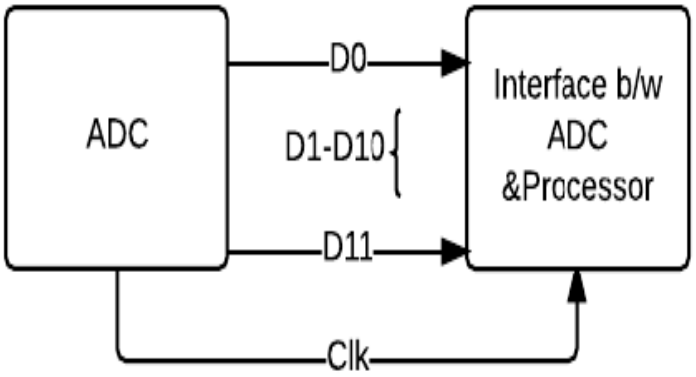


2. ADC to Processor Interface

Single Data Rate (SDR)

- Single data rate (SDR) is very common for lower speed data interfaces, typically under 200 MHz.

- Data is transitioned on one edge of the clock by the transmitter and received by the receiver on the other clock edge.



2. ADC to Processor Interface

Double Data Rate (DDR)

- In the case on DDR, the transmitter transitions data on both clock edges. This allows for twice as much data to be transferred in the same amount of time as SDR

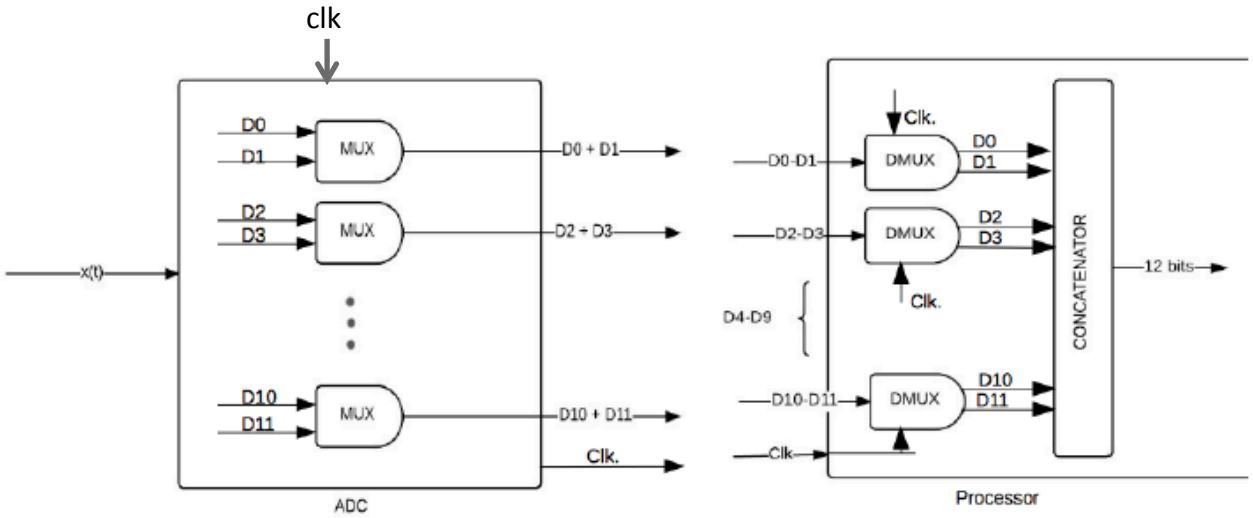


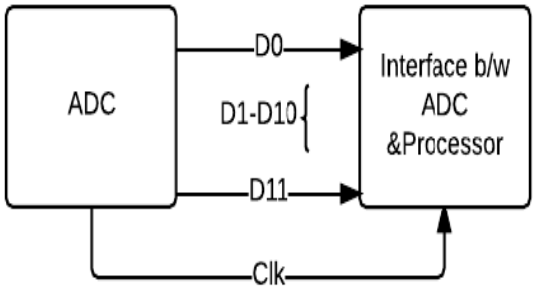
Figure 4: Double data rate (DDR)

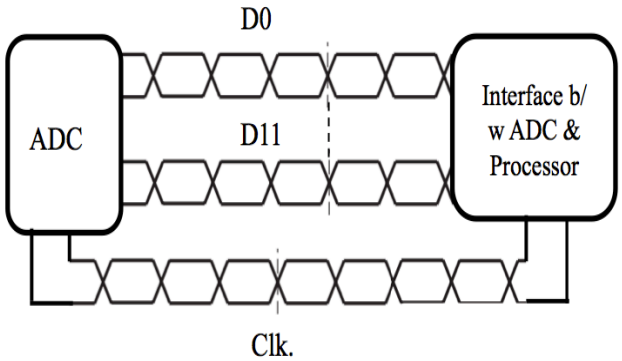
SDR vs DDR

- ADCs use a variety of digital interface standards.

Single Data Rate (SDR)	Double Data Rate (DDR)
Lower speed data interfaces (typically under 200 MHz).	Higher speed data interfaces.
Data is transitioned on one edge of the clock by the transmitter and received by the receiver on the other clock edge.	Transmitter transitions data on both clock edges.
Enough time provided for the data to dispose before sampling.	It divides the number of physical channels by 2 hence allowing more data to pass in the same amount of time

Single ended vs Differential ended





The main benefit of a differential measurement is noise rejection, because the noise is added to both wires and can then be filtered out by the common mode rejection of the data acquisition system.

In low voltage differential signals (LVDS), the bit clock rate for two-wire interface:

$$\frac{ADC Resolution \times SampleRate}{2} = BitClock(MHz)$$

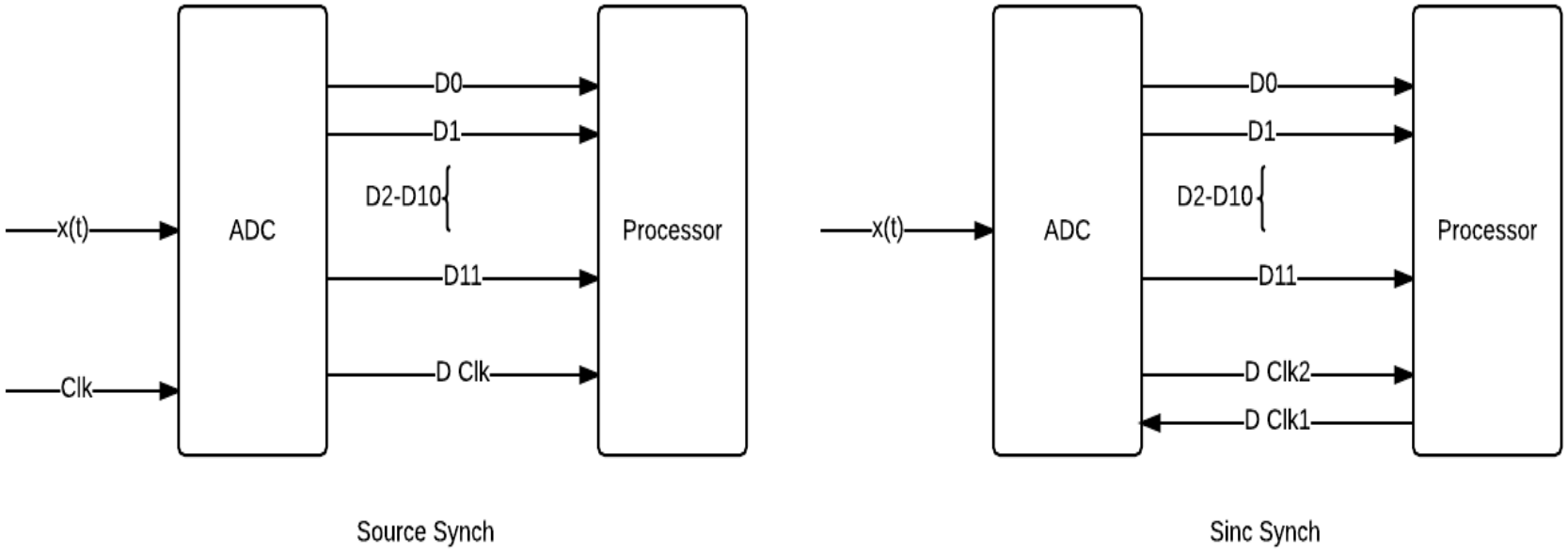
$$\frac{\frac{ADC Resolution}{2} \times SampleRate}{2} = BitClock(MHz)$$

In this project:

$$\frac{\frac{12bits}{2} \times 200MHz}{2} = 600MHz)$$

Sink vs Source

- Each of the 2 types of wiring can have the clock be synched either using source or sink.

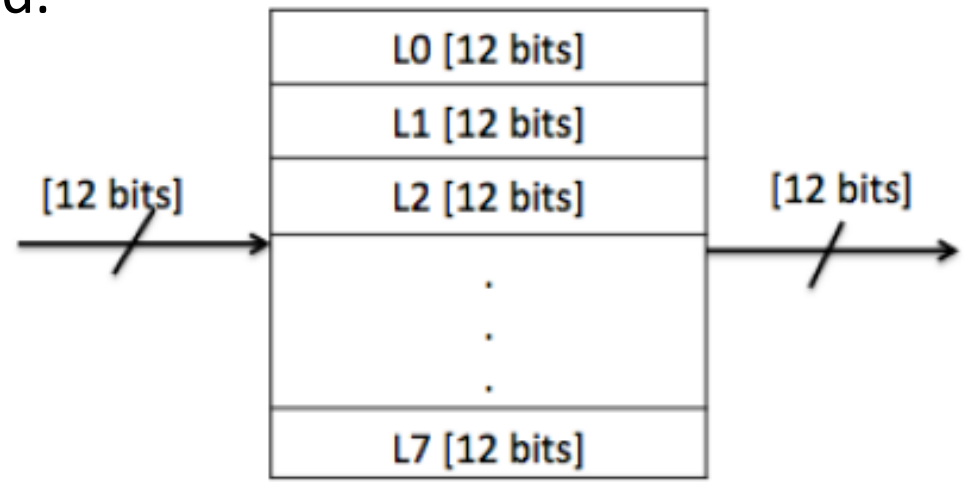


3. Circular Buffer

- Circular buffers are commonly used in embedded systems to provide synchronization between the data and the clock.

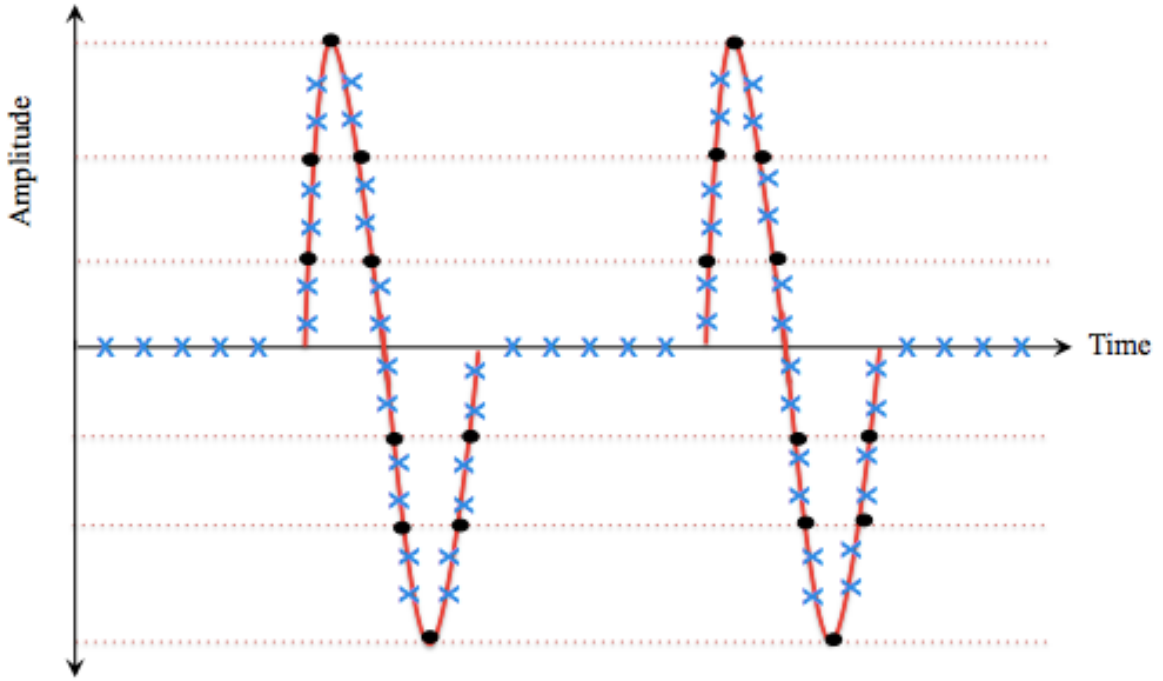
- FIFO is used to store the sampled signal temporarily before being processed.

Change the diagram



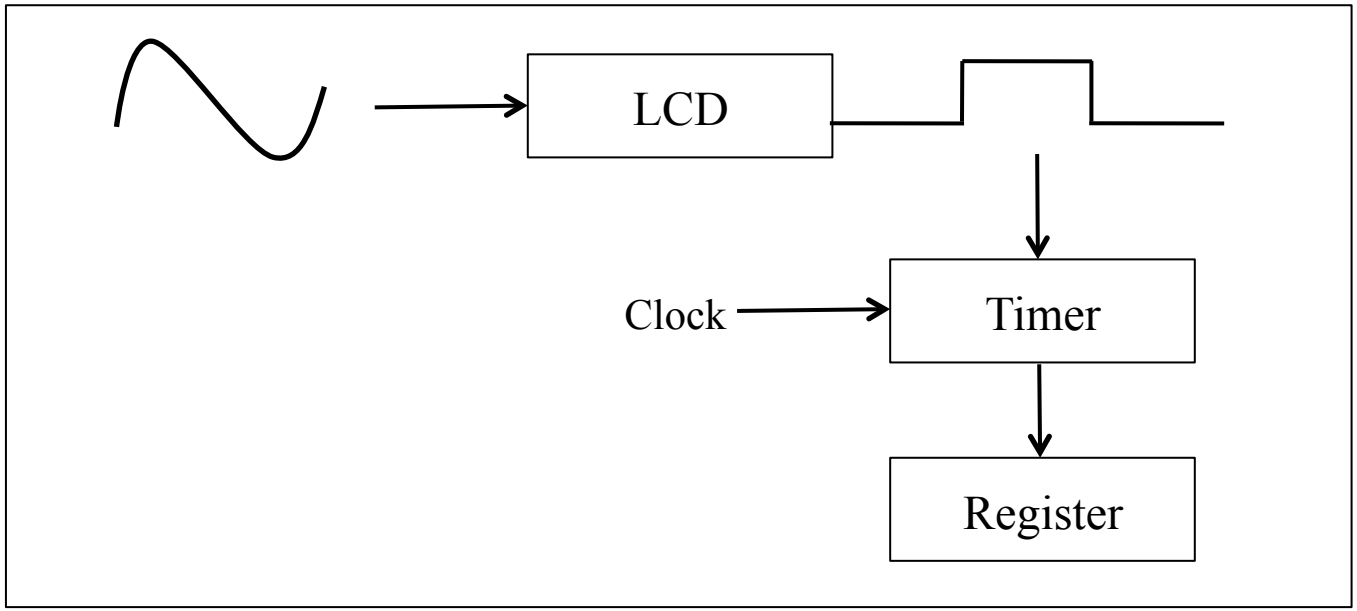
4. Digital Signal Processing

- The digital signal is processed using Level Crossing Sampling Scheme, which is also known as Event Driven Sampling

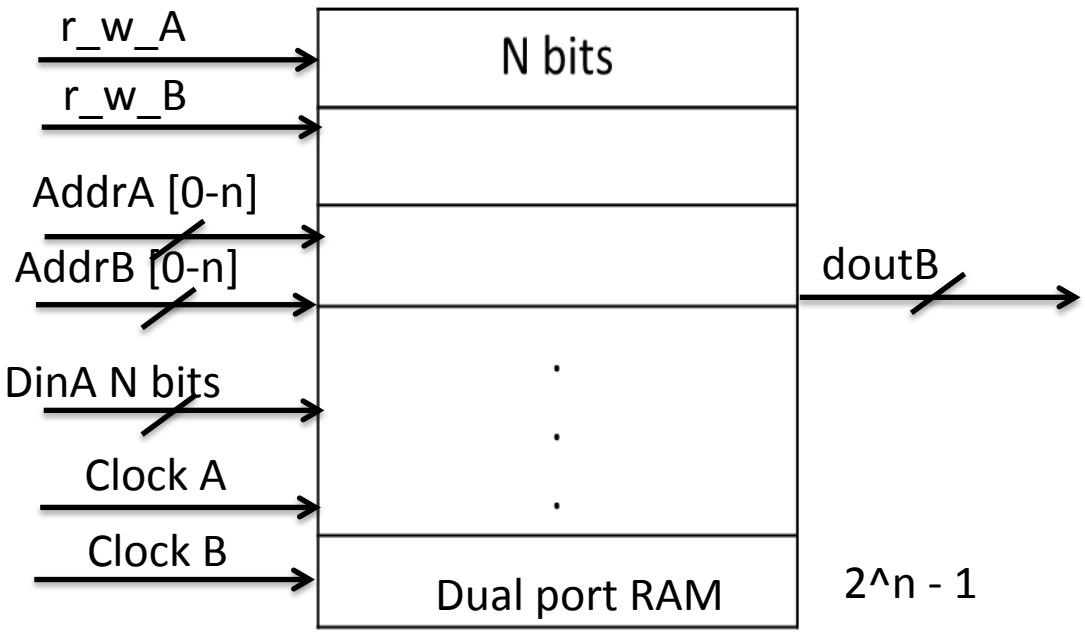


4. Digital Signal Processing

The following figure illustrates the Event Driven Sampling on a circuit level.



5. Simple Dual-Port RAM



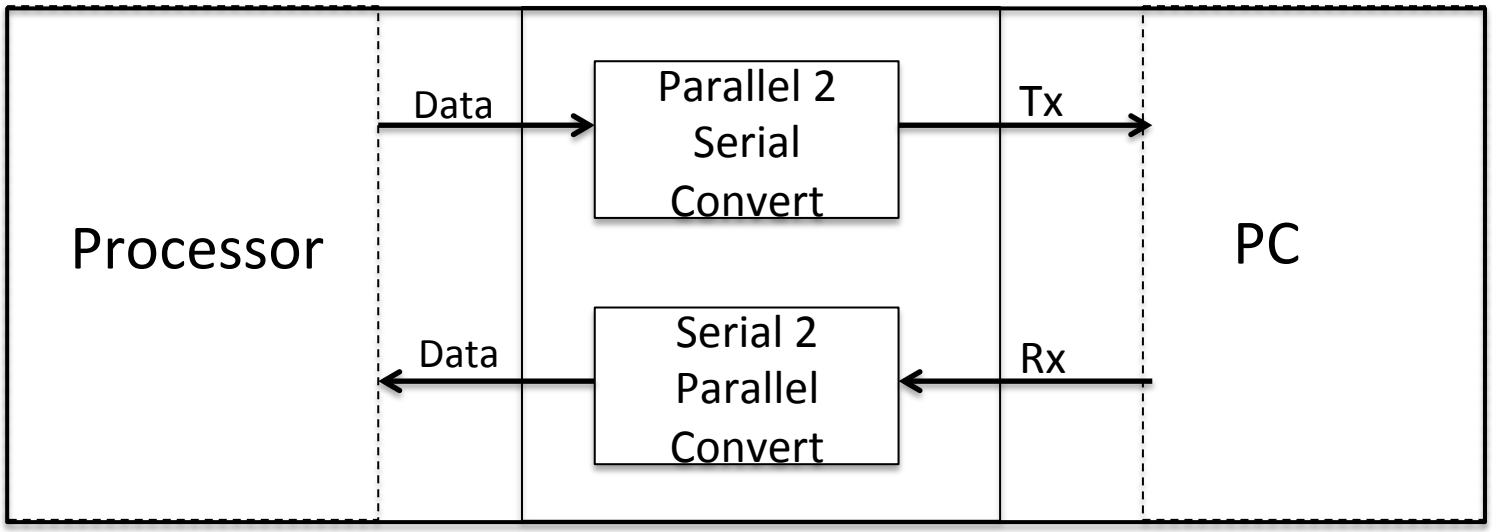
6. Processor to PC Interface

Data exchange:

- Serial or Parallel,
- Synchronous or Asynchronous (Using an agreed upon timing).
- Full duplex, Half duplex, simplex

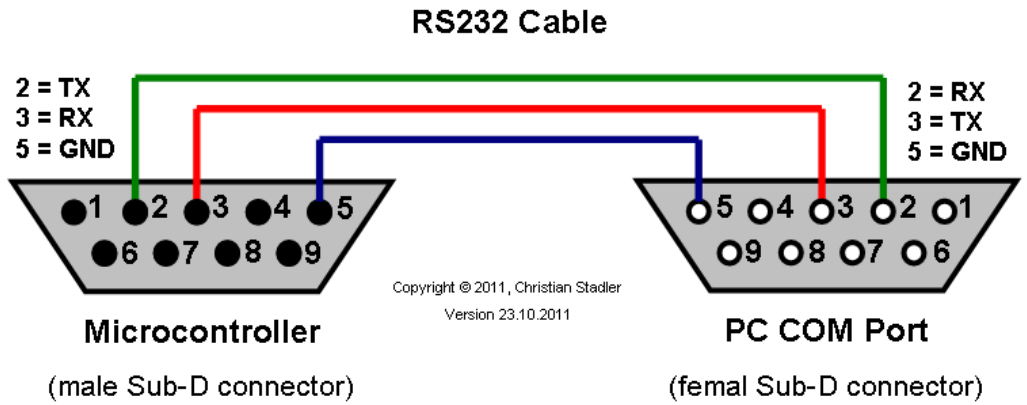
UART

- Universal Asynchronous Receiver/Transmitter
- TX: pins that transmit
- RX: pins that receives
- BAUD rate: Baud is a measurement of transmission speed in asynchronous communication.



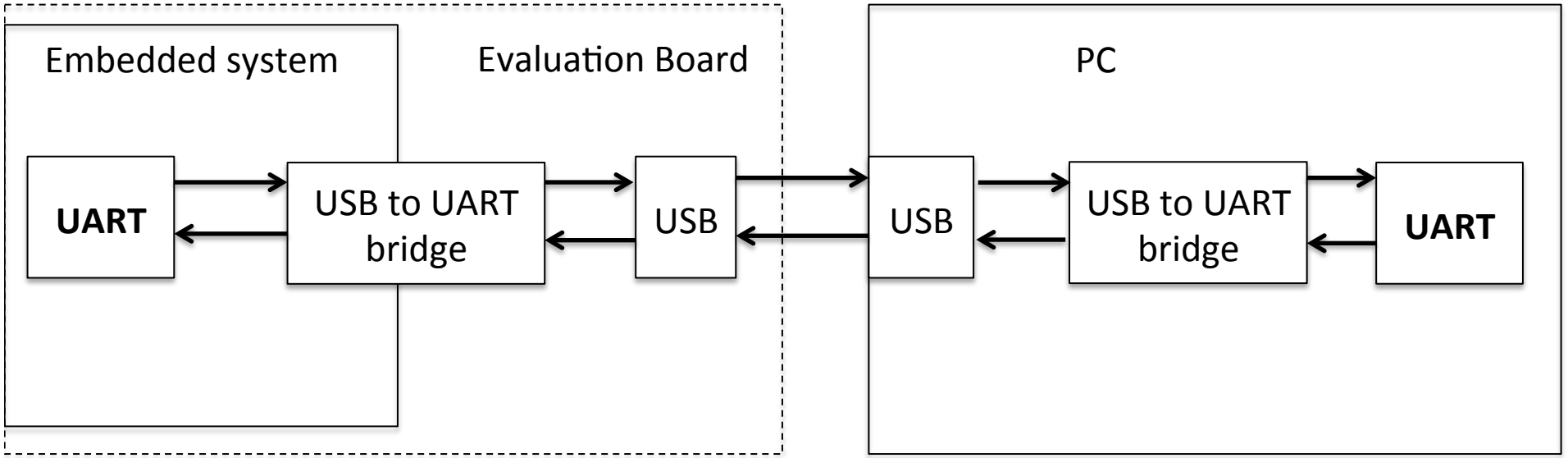
RS232 interface

- RS232 is standard for voltage signaling.
- It defines the electrical characteristics and timing of signals, the meaning of signals, and the physical size and pinout of connectors.



Start Bit	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Stop Bit	Next Start Bit	Next Data frame

USB to UART Bridge



System Design and Implementation

- First the design will be studied at software level. MATLAB is a good candidate to analyze and test the implementation of the proposed design.
- Second stage is to implement the designed solution at embedded level.

Component Specifications

Part Number	Description	Specifications	Unit Price	Place of Purchase
AD9613-250EBZ	Evaluation Board for the selected ADC	Number of Bits: 12 Sampling Rate: 250M Data Interface: SPI# of A/D Converters: 2	1224.82 SAR	Digi-Key Corporation Website
CVT-ADC-FMC-INTPZB-ND	Interposer (Interface between ADC and embedded system)	Related Products: Xilinx FMC-Supported Boards	429.86 SAR	Digi-Key Corporation Website
EK-S6-SP601-G	Spartan-6 FPGA SP601 Evaluation Kit	200MHz Oscillator (Differential), Serial (UART) to USB Bridge, DDR2 Component Memory 128MB, IIC 8Kb IIC EEPROM, FMC-LPC connector (68 single-ended or 34 differential user defined signals)	1268.94 SAR	

Project Risk Management and cost optimization

- Components availability
- Cost consideration
- Asynchronous components libraries implementation.
- Outsourcing and shipment lead time

Proposed Implementation Plan

Task	Deadline
Develop the algorithm for event driven sampling	Mid March
Develop the MATLAB code for event driven sampling	Mid of March
Test the MATLAB code	Mid of March
Purchase the hardware needed for implementation	Beginning of May
Finalize project, project report and presentation	End of May

Conclusion and Prospect

- In conclusion, a technique to enhance the digital filtering chain required in remote systems has been designed and shall be implemented in the next stage.

Prospects:

- Employ the developed techniques to biomedical applications like Electroencephalogram, MRI scanners, PET scanners, etc.
- Audio and imaging applications.