# 1.

**NO CONCEPTUAL QUESTIONS/WORK**

**Results and summary:**

In this experiment, the core.c file/emulator was once again reworked in order to emulate the functionality of a pipelined processor and the various pipeline stages. Using a provided trace file and predefined register values, the expected output was calculated by hand in order to verify the functionality of the emulator, which was correct. This experiment demonstrates how pipelining can increase efficiency in a processor.