

November 1988 Revised December 1999

74AC14 • 74ACT14 Hex Inverter with Schmitt Trigger Input

General Description

The 74AC14 and 74ACT14 contain six inverter gates each with a Schmitt trigger input. They are capable of transforming slowly changing input signals into sharply defined, jitterfree output signals. In addition, they have a greater noise margin than conventional inverters.

The 74AC14 and 74ACT14 have hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

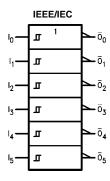
- I_{CC} reduced by 50%
- Outputs source/sink 24 mA
- 74ACT14 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74AC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MS-153, 4.4mm Wide
74AC14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT14SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74ACT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MS-153, 4.4mm Wide
74ACT14PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

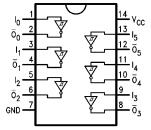
Logic Symbol



Pin Descriptions

Pin Names	Description
I _n	Inputs
Ō _n	Outputs

Connection Diagram



Function Table

Input	Output
Α	О
L	Н
Н	L

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Absolute Maximum Ratings(Note 1)

-0.5V to +7.0V

140°C

DC Input Diode Current (I_{IK})

Supply Voltage (V_{CC})

 $V_{I} = -0.5V$ -20 mA +20 mA

 $V_I = V_{CC} + 0.5V$ DC Input Voltage (V_I) -0.5V to $V_{CC} + 0.5V$

DC Output Diode Current (I_{OK})

 $V_{O} = -0.5V$ -20 mA $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) -0.5V to $V_{CC} + 0.5V$

DC Output Source

or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current

per Output Pin (I_{CC} or I_{GND}) ±50 mA Storage Temperature (T_{STG}) -65°C to +150°C

Junction Temperature (T_J)

PDIP

Recommended Operating Conditions

Supply Voltage (V_{CC})

AC 2.0V to 6.0V ACT 4.5V to 5.5V 0V to $V_{\mbox{\footnotesize CC}}$ Input Voltage (V_I) Output Voltage (V_O) 0V to V_{CC}

-40°C to +85°C Operating Temperature (T_A)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} T _A =		+25°C	$T_A = -40^{\circ}C$ to $+85^{\circ}C$	Units	Conditions	
Зушьог	Farameter	(V)	Тур	Gua	aranteed Limits	Ullis	Conditions	
V _{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9			
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
		3.0		2.56	2.46		I _{OH} = 12	
		4.5		3.86	3.76	V	$I_{OH} = 24 \text{ mA}$	
		5.5		4.86	4.76		I _{OH} = 24 mA (Note 2)	
V _{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1			
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
		3.0		0.36	0.44		I _{OL} = 12	
		4.5		0.36	0.44	V	I _{OL} 24 mA	
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 2)	
I _{IN} (Note 4)	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}$, GND	
V _{t+}	Maximum Positive	3.0		2.2	2.2			
	Threshold	4.5		3.2	3.2	V	T _A = Worst Case	
		5.5		3.9	3.9			
V _{t-}	Minimum Negative	3.0		0.5	0.5			
	Threshold	4.5		0.9	0.9	V	T _A = Worst Case	
		5.5		1.1	1.1			
V _{H(MAX)}	Maximum Hysteresis	3.0		1.2	1.2			
		4.5		1.4	1.4	V	T _A = Worst Case	
		5.5		1.6	1.6			
V _{H(MIN)}	Minimum Hysteresis	3.0		0.3	0.3			
		4.5		0.4	0.4	V	T _A = Worst Case	
		5.5		0.5	0.5			
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 3)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μА	$V_{IN} = V_{CC}$ or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

AC Electrical Characteristics for AC

		V _{CC}		$T_A = +25^{\circ}C$		T _A = -40°	C to +85°C	
Symbol Parameter (V)		$C_L = 50 \text{ pF}$			$C_L = 50 \text{ pF}$			
		(Note 5)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.5	15.0	ns
		5.0	1.5	7.0	10.0	1.5	11.0	115
t _{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.5	13.0	ns
		5.0	1.5	6.0	8.5	1.5	9.5	115

Note 5: Voltage Range 3.3 is $3.3V \pm 0.3V$ Voltage Range 5.0 is $5.0V \pm 0.5V$

DC Electrical Characteristics for ACT

Symbol	Parameter	v _{cc}	T _A =	+25°C	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Symbol	Farameter	(V)	Тур	Gua	aranteed Limits	Units		
V _{IH}	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$	
	Input Voltage	5.5	1.5	2.0	2.0	V	or V _{CC} – 0.1V	
V _{IL}	Maximum LOW Level	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$	
	Output Voltage	5.5	1.5	0.8	0.8	V	or V _{CC} – 0.1V	
V _{OH}	Minimum HIGH Level	4.5	4.49	434	4.4	V	I _{OUT} = -50μA	
	Output Voltage	5.5	5.49	5.4	5.4	V	100Τ = -30μΑ	
							$V_{IN} = V_{IL}$ or V_{IH}	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		I _{OH} = -24 mA (Note 6)	
V _{OL}	Maximum LOW Level	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
	Output Voltage	5.5	0.001	0.1	0.1	V	1 _{OUT} = 50 μA	
							$V_{IN} = V_{IL}$ or V_{IH}	
		4.5		0.36	0.44	V	I _{OL} = 24 mA	
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 6)	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}$, GND	
V _{H(MAX)}	Maximum Hysteresis	4.5		1.4	1.4	V	T _A = Worst Case	
		5.5		1.6	1.6	v	I A – Worst Case	
V _{H(MIN)}	Minimum Hysteresis	4.5		0.4	0.4	V	T _A = Worst Case	
		5.5		0.5	0.5	V	I A = Worst Case	
V _{t+}	Maximum Positive	4.5		2.0	2.0	V	T _A = Worst Case	
	Threshold	5.5		2.0	2.0	V	I A = Worst Case	
V _{t-}	Minimum Negative	4.5		0.8	0.8	V	T _A = Worst Case	
	Threshold	5.5		0.8	0.8	V	I A = Worst Case	
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	$V_{I} = V_{CC} - 2.1V$	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 7)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		2.0	20.0	μΑ	$V_{IN} = V_{CC}$ or GND	

Note 6: All outputs loaded; thresholds on input associated with output under test.

Note 7: Maximum test duration 2.0 ms, one output loaded at a time.

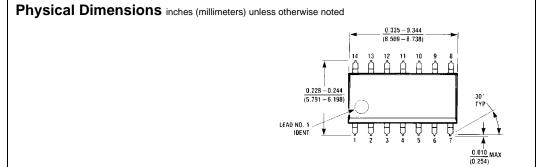
AC Electrical Characteristics for ACT

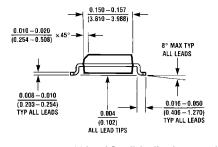
Symbol	Parameter	V _{CC} (V)	T _A = +25°C C ₁ = 50 pF			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_1 = 50 \text{ pF}$		Units
Symbol	raianielei	(V) (Note 8)	Min	Typ	Max	Min	Мах	Offics
t _{PLH}	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns
t _{PHL}	Propagation Delay Data to Output	5.0	3.0	8.0	10.0	3.0	11.0	ns

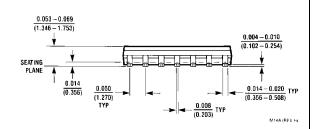
Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

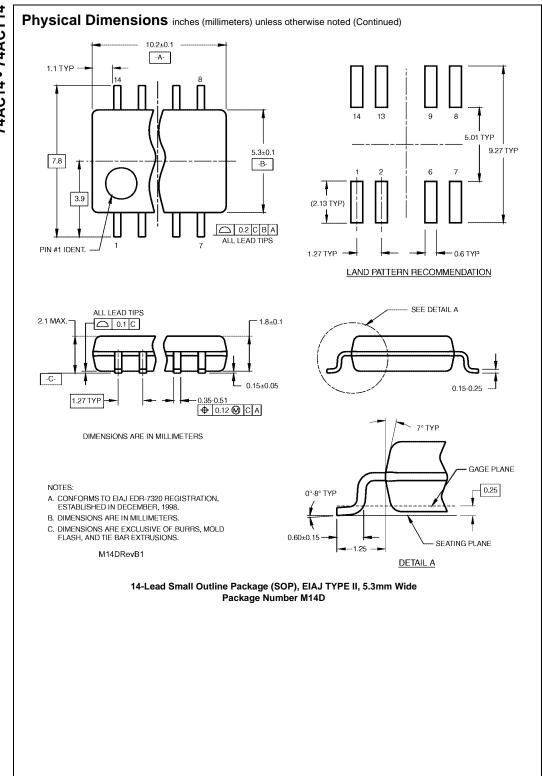
Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance for AC	25.0	pF	V _{CC} = 5.0V
	for ACT	80	ρı	ACC = 2.0 A







14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 -A-7.72 4.16 6.4 4.4±0.1 -B-3.2 0.2 C B A 0.65 ALL LEAD TIPS LAND PATTERN RECOMMENDATION PIN #1 IDENT. SEE DETAIL A ALL LEAD TIPS 1.2 MAX - 0.90 +0.15 - 0.09-0.20 -C-- 0.10±0.05 0.19 - 0.30 **♦** 0.13 **№** A B**⑤** C**⑤** -12.00° TOP & BOTTOM R0.09 MIN-GAGE PLANE NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93. 0.25 B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. -1.00-R0.09 MIN MTC14RevC3 DETAIL A 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\frac{0.630 - 8.128}{(7.620 - 8.128)}$ 0.060 0.145 - 0.2004° TYP Optional (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 (0.508) 0.125 - 0.150 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ (1.905 ± 0.381) (7.112) MIN 0.014 - 0.0230.100 ± 0.010 (2.540 ± 0.254) (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 ^{+0.040} -0.015

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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8.255 + 1.016

N144 (REV.F)

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