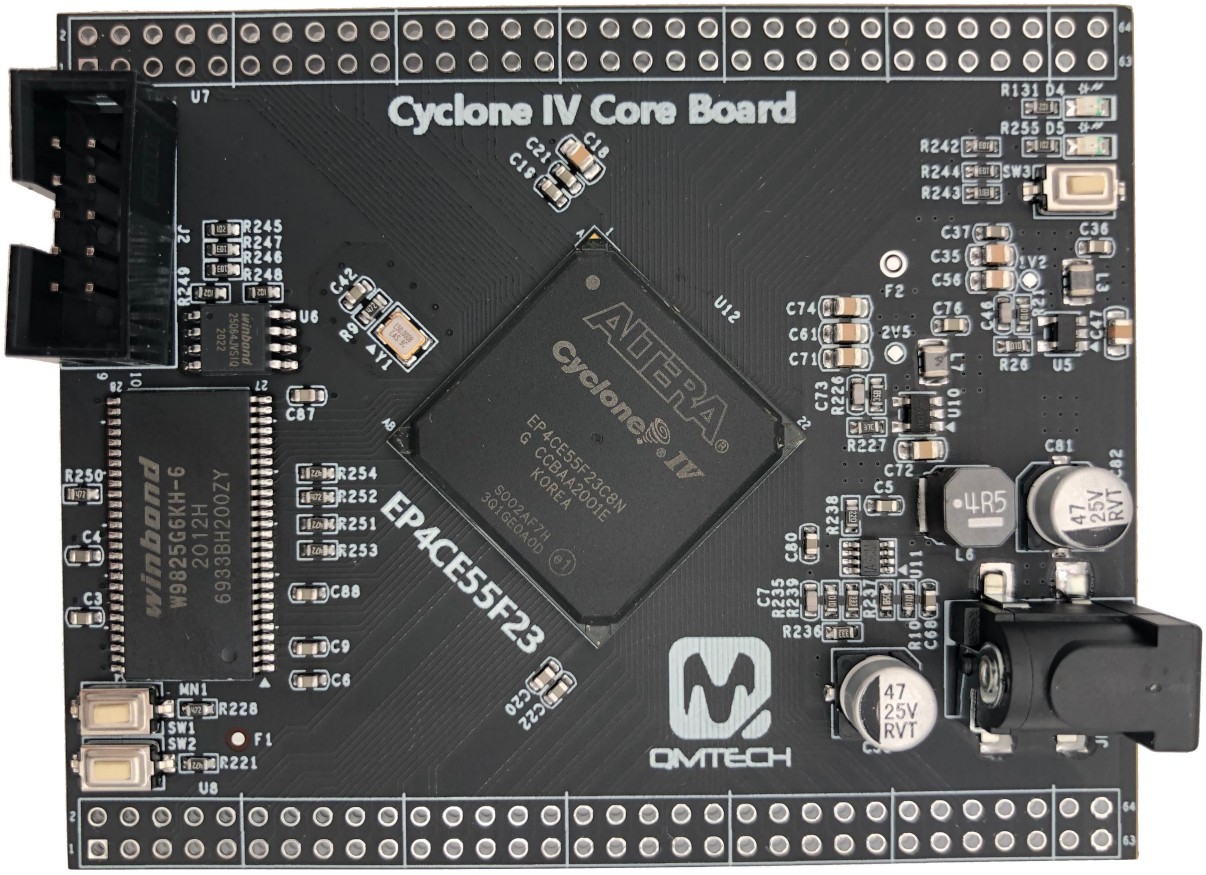
CYCLONE IV EP4CE55 CORE BOARD

USER MANUAL



Preface

The QMTech® Cyclone IV Core Board uses Intel(Altera) EP4CE55F23 device to demonstrate Intel's leadership in offering power-efficient FPGAs. With enhanced architecture and silicon, advanced semiconductor process technology, and power management tools, power consumption for Cyclone IV FPGAs has been reduced by up to 25 percent compared to Cyclone® III FPGAs. The result is the lowest power consumption of any comparable FPGA.

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1. Introduction

1.1 Document Scope

This demo user manual introduces the Cyclone IV EP4CE55 core board and describes how to setup the core board running with application software Altera Quartus II 15.1. Users may employee the on board rich logic resource FPGA EP4CE55F23C8N and large SDRAM memory W9825G6KH-6 to implement various applications. The core board also has 108 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the Cyclone IV EP4CE55:

- On-Board FPGA: EP4CE55F23C8N;
- On-Board FPGA external crystal frequency: 50MHz;
- EP4CE55F23C8N has rich block RAM resource up to 2.3Mb;
- EP4CE55F23C8N has 55K Logic elements;
- On-Board W25Q64 SPI Flash, 8M bytes for user configuration code;
- On-Board 32MB Winbond SDRAM, W9825G6KH-6;
- On-Board 3.3V power supply for FPGA by using MP2315 wide input range DC/DC;
- EP4CE55 core board has two 64p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- EP4CE55 core board has 3 user switches;
- EP4CE55 core board has 2 user LEDs;
- EP4CE55 core board has JTAG interface, by using 10p, 2.54mm pitch header;
- EP4CE55 core board PCB size is: 6.7cm x 8.4cm;
- Default power source for core board is: 1A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

1.3 Kit Top View

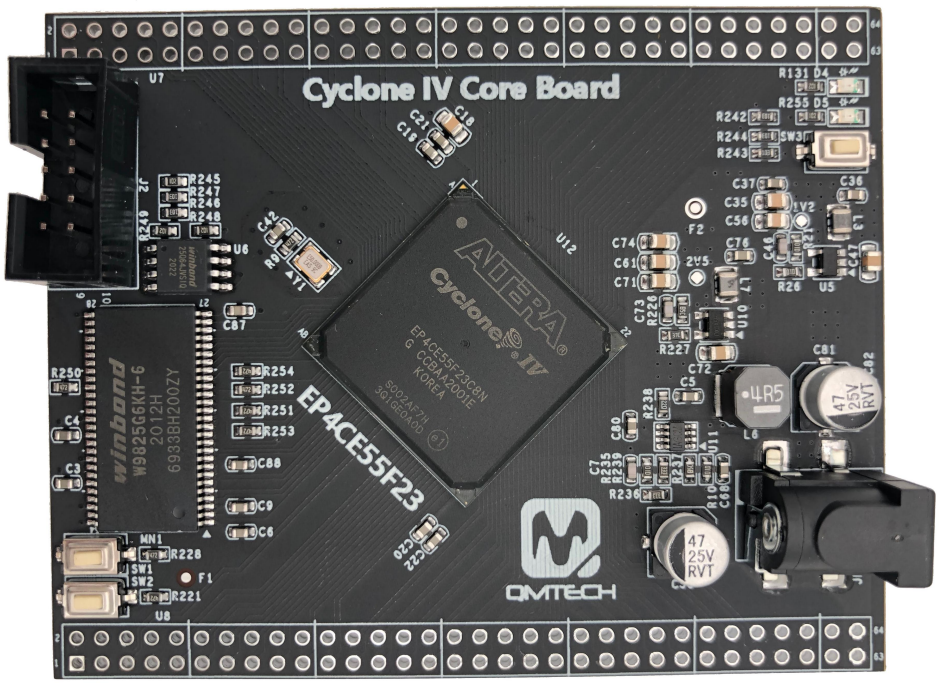


Figure 1-1. Cyclone IV EP4CE55 Top View

2. Getting Started

Below image shows the dimension of the Cyclone IV EP4CE55 core board: 67.1mm x 84.1mm. The unit in below image is millimeter(mm).

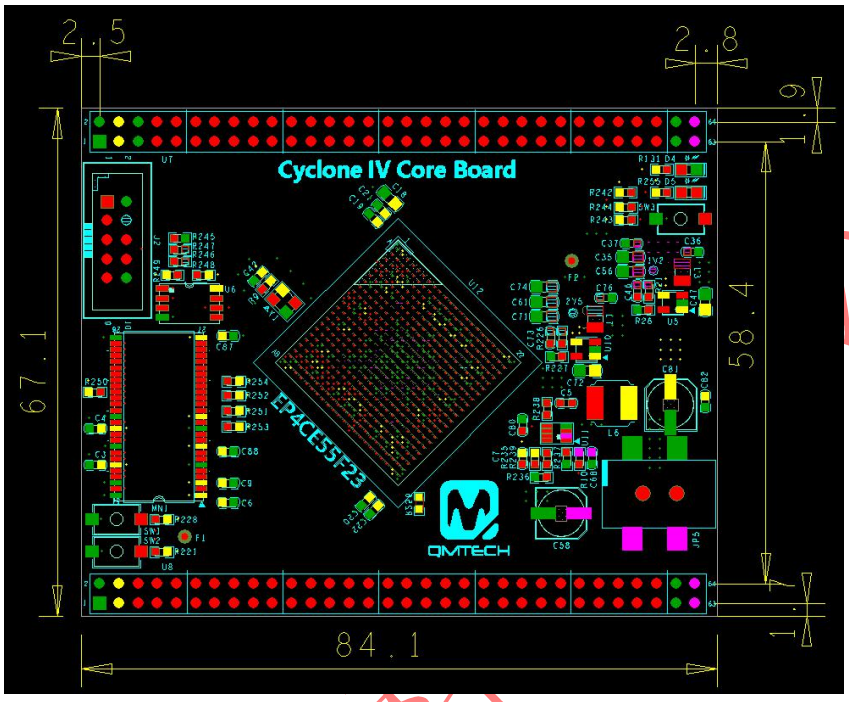
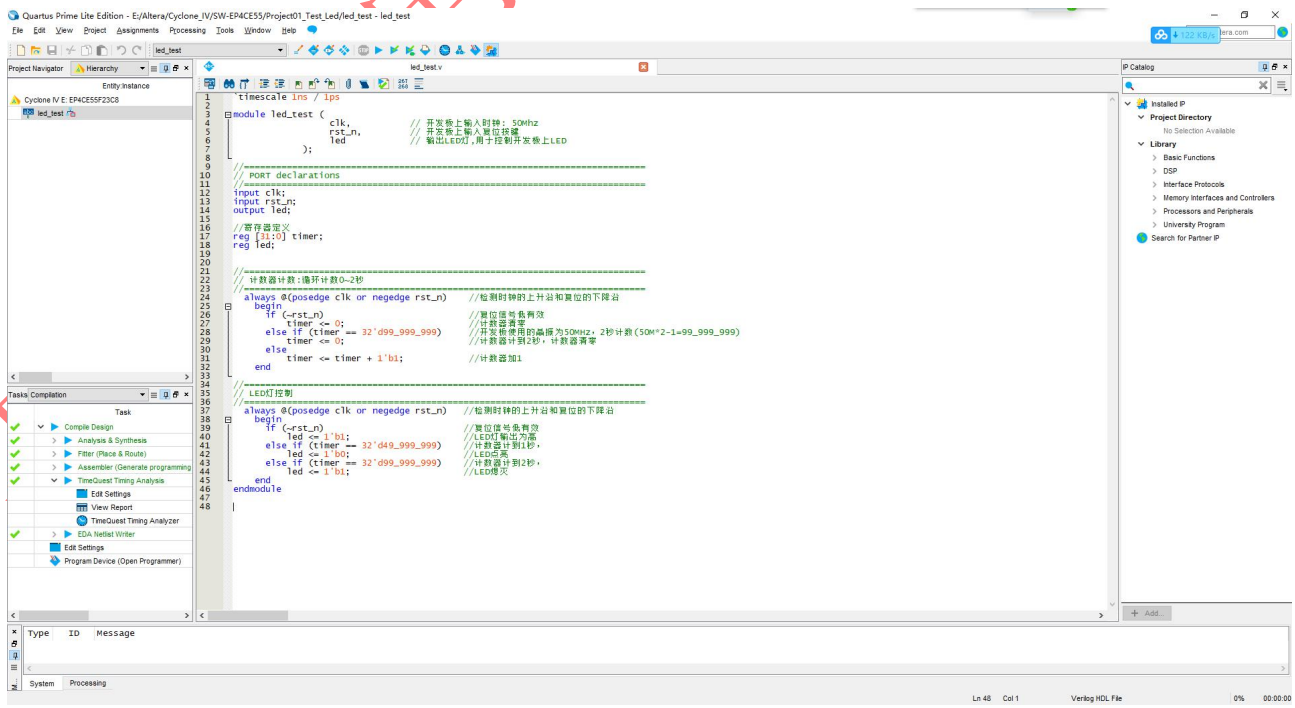


Figure 2-1. Cyclone IV EP4CE55 Dimension

The Cyclone IV EP4CE55 core board tool chain consists of Altera Quartus II 15.1, Altera USB Blaster cable, EP4CE55 core board and 5V DC power supply. Below image shows the Altera Quartus II 15.1 development environment which could be downloaded from Altera(Intel) office website:



2.2 Cyclone IV EP4CE55 Hardware Design

2.2.1 Cyclone IV EP4CE55 Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header or the 64P header U7/U8. Users may refer to the hardware schematic for the detailed design. The on board LED D4 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V.

Note: FPGA core supply 1.2V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.

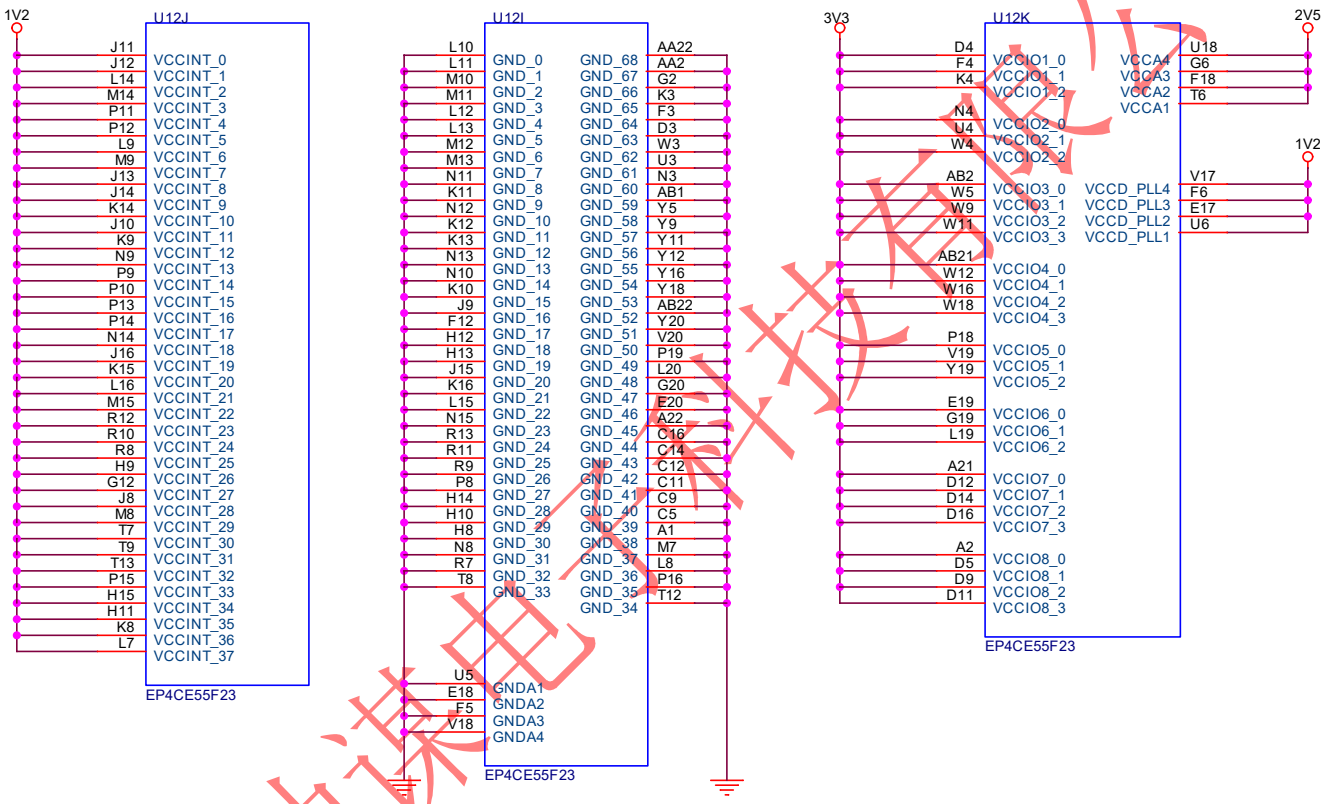


Figure 2-2. Power Supply for the FPGA

2.2.2 Cyclone IV EP4CE55 SDRAM Memory

Cyclone IV EP4CE55 has on board 16bit width data bus, 32MB memory size W9825G6KH-6 SDRAM provided by Winbond. Below image shows the detailed hardware design:

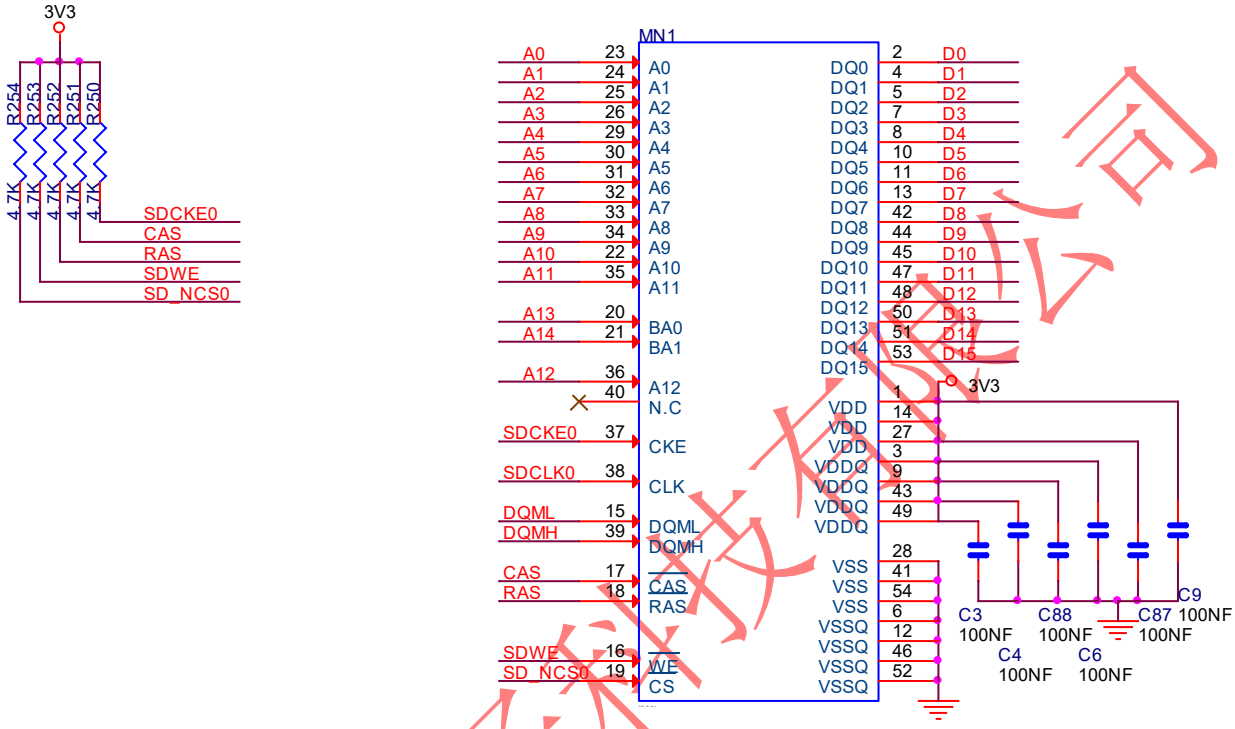


Figure 2-3. SDRAM

2.2.3 Cyclone IV EP4CE55 SPI Boot

Cyclone IV EP4CE55 boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using W25Q64 manufactured by Winbond, with 64Mbit memory storage.

Note: The SPI Flash is designed with x1 mode.

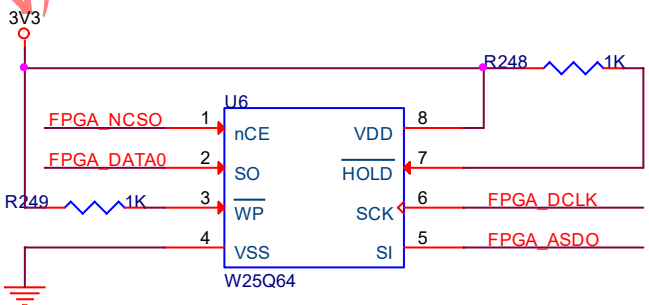


Figure 2-4. SPI Flash

Below image shows the hardware configuration of MSEL[3:0]: 0010, in which way will make the FPGA boot from Active Serial (x1 or x4) Standard Mode:

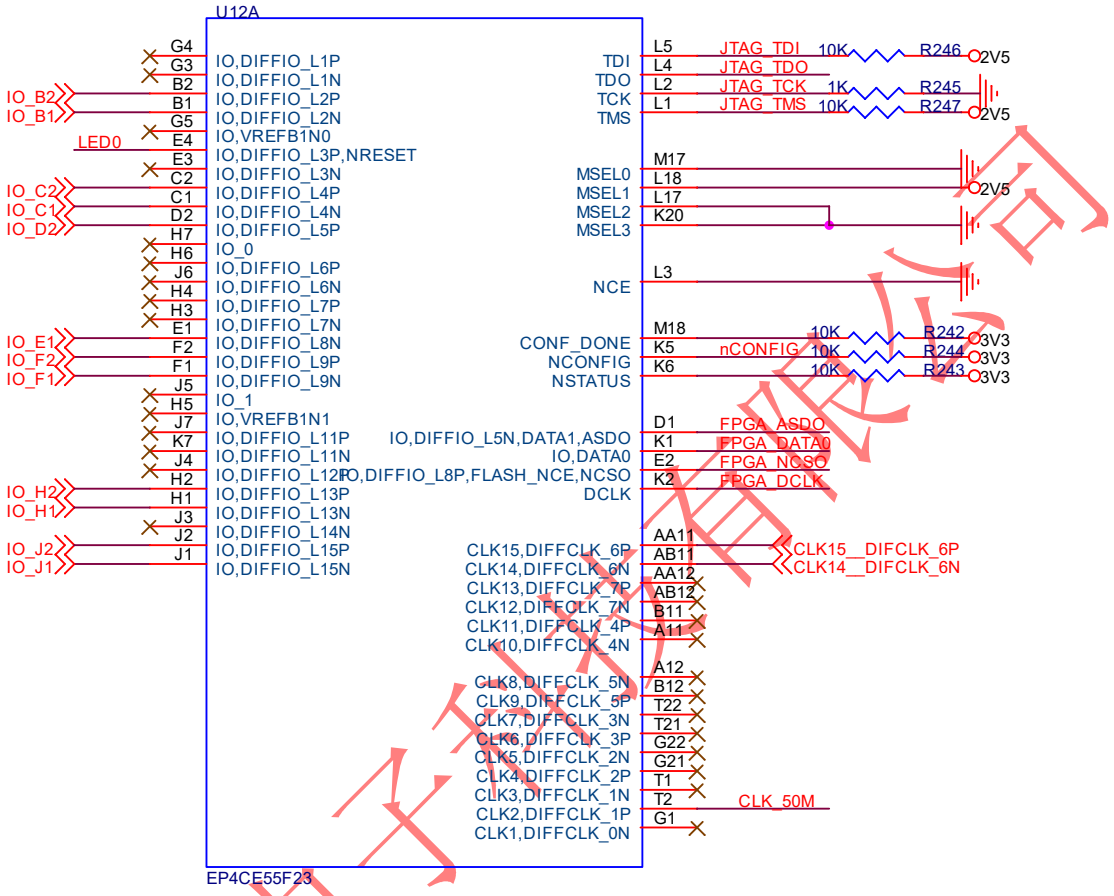


Figure 2-5. MSEL Settings

2.2.4 Cyclone IV EP4CE55 System Clock

The Cyclone IV EP4CE55 has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/°c. Below image shows the detailed hardware design:

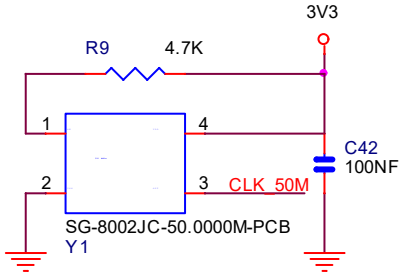


Figure 2-6. 50MHz System Clock

2.2.1 Cyclone IV EP4CE55 JTAG Port

The on board JTAG port uses 10P 2.54mm pitch header which could be easily connected to Altera USB blaster cable. Below image shows the hardware design of the JTAG port:

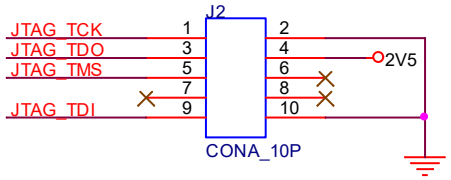


Figure 2-7. JTAG Port

2.2.2 Cyclone IV EP4CE55 Power Supply

The core board's 3.3V power supply is using high efficiency DC/DC chip MP2315 provided by MPS Inc. The MP2315 supports wide voltage input range from 4.5V to 24V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the MP2315 hardware design:

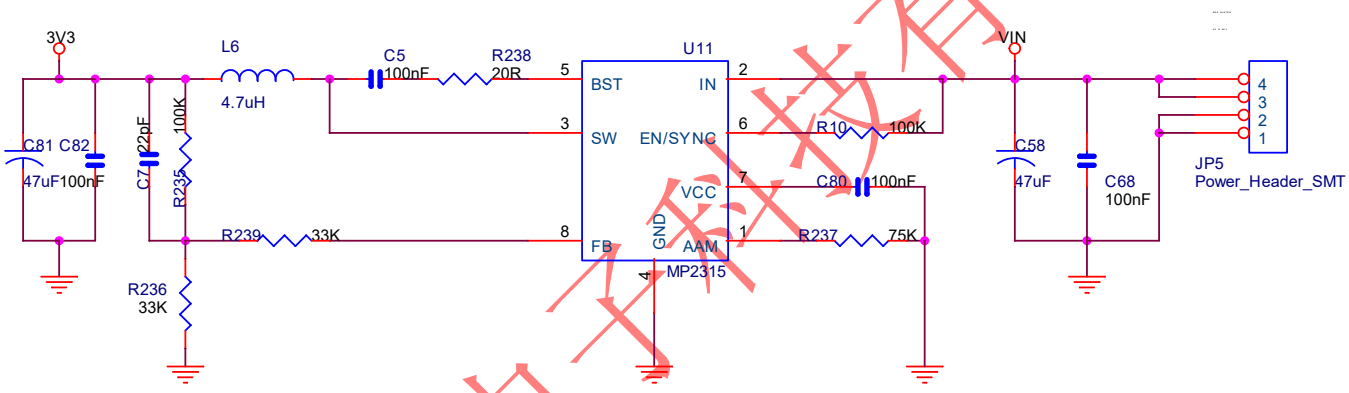
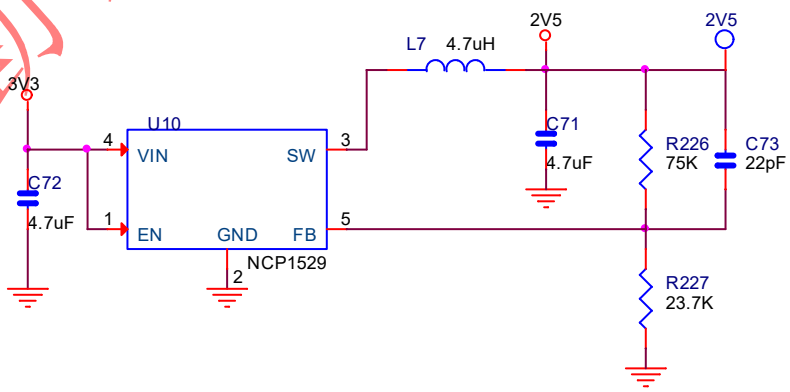


Figure 2-8. MP2315 Hardware Design

The core board's 2.5V and 1.2V FPGA core voltage power supply is using high efficiency DC/DC chip NCP1529 provided by On-Semi Inc.



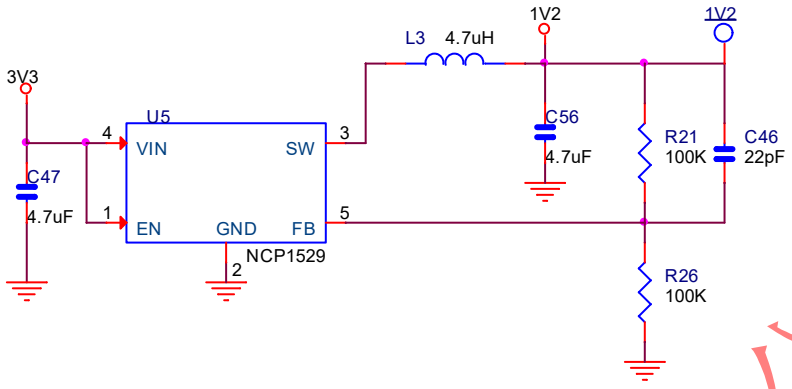


Figure 2-9. NCP1529 Hardware Design

2.2.3 Cyclone IV EP4CE55 Extension IO

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

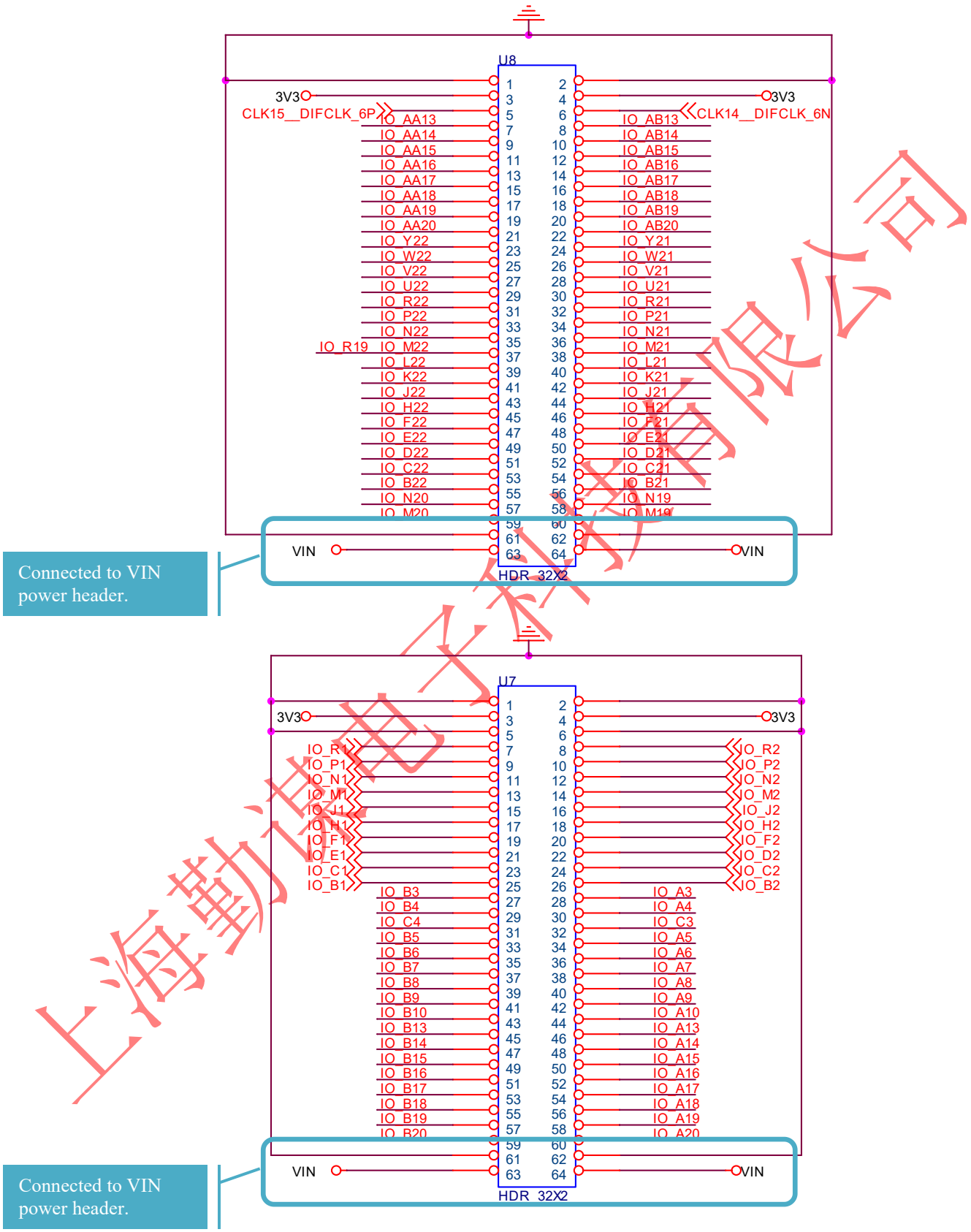


Figure 2-10. Extension IO

2.2.4 Cyclone IV EP4CE55 User LED

Below image shows one user LED and 3.3V power supply indicator:

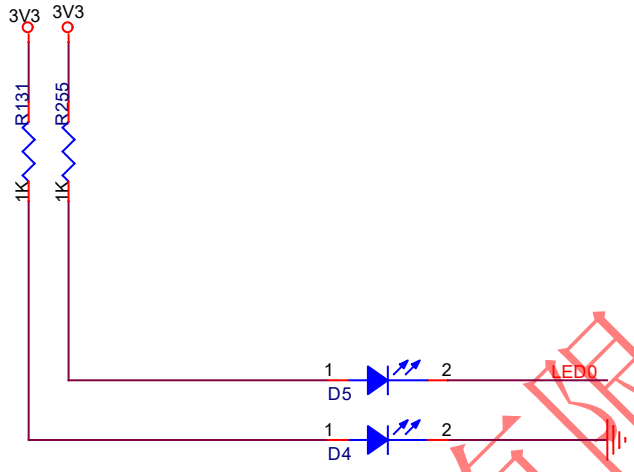


Figure 2-11. User LEDs

2.2.5 Cyclone IV EP4CE55 User Key

Below image shows the nCONFIG key and two user keys:

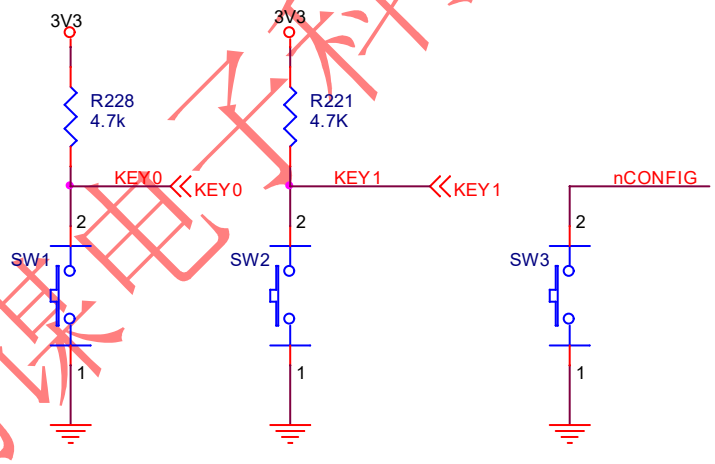


Figure 2-12. User Keys

3. Reference

[1] ep4ce55f23-sdram.pdf
[2] an592.pdf
[3] an592_ch.pdf
[4] cyiv-5v1.pdf
[5] cyiv-5v2.pdf
[6] cyiv-5v3.pdf
[7] pcg-01008.pdf

4. Revision

Doc. Rev.	Date	Comments
0.1	10/06/2020	Initial Version.
1.0	06/08/2020	V1.0 Formal Release.