Product Data Sheet **PL2303GC**

PL2303GC USB to Full UART IC with GPIO
Single-chip USB to Asynchronous Serial Data Interface

USB Interface

- Fully Compliant with USB 2.0 specification (Full-Speed Mode).
- USB-IF certified (USB logo compliant) with TID 40001838.
- UHCI/OHCI (USB 1.1), EHCI (USB 2.0), xHCI (USB 3.1) Host Controller Compatible.
- Provides royalty-free USB to Virtual Com Port (VCP) drivers for Windows, Mac, Linux, and Android.
- Highly integrated USB 1.1 FS Transceiver. Integrated termination resistors and pull-up resistor to reduce PCB external components.
- Supports 256-byte OTPROM (One-Time Programmable ROM) for USB device descriptors and GPIO custom configuration. OTPROM can be programmed directly through USB port.
- Each IC has unique ID (for Serial Number).
- Supports bus-power, self-power and high-power USB device configuration.
- Supports Windows USB Selective Suspend (Remote Wakeup enabled).
- Supports VBUS input detect function to attach USB host after VBUS is detected.
- Supports 3.3V VBUS voltage operation.

GPIO Interface

- Versatile GPIO functions and routing logic provides easy to use multi-I/O functions.
- Configurable I/O pin output driving strength.
- Total 16 General Purpose I/O (GPIO) pins can be used after configured.
- Optional Clock Output to external MCU.

UART Interface

- Supports Serial UART Interface:
  - RS232, RS422, RS485
  - Flexible baud rate support up to 12Mbps
  - 5, 6, 7 or 8 data bits
  - Odd, Even, Mark, Space, None parity mode
  - One, one and a half, or two stop bits
  - Hardware Flow Control (CTS/RTS and/or DSR/DTR)
  - Software Flow Control (XON/XOFF)
  - Configurable Remote Wakeup Pin
- 1024-byte bi-directional data FIFO buffers (768-byte receive/256-byte transmit) for faster data throughput. Configurable in OTPROM.
- Configurable Transmit and Receive LED pins.
- Suspend Pin control for RS232 transceiver.
- UART inverted signal configurable option.

Battery Charger Detection

- Supports Battery Charger (BC1.2) Detection to enable fast charging of batteries.

Miscellaneous

- Integrated self-generated precise clock generator. External crystal is optional.
- Integrated Power-on-Reset (POR) circuit.
- Integrated 5V to 3.3V LDO that can support 80mA for external components.
- Low operating power and USB suspend current.
- Wide I/O voltage range (1.8V/2.5V/3.3V/5V).
- -40°C to 85°C Operating Temperature.
- 28-pin SSOP and 24-pin UQFN IC package (RoHS compliant and Pb-free Green Compound).
- Pin-compatible with PL2303HXD chip (SSOP28).

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1. Product Applications

- Single-chip upgrade solution for Legacy RS232 devices to USB interface
- USB to RS232/RS422/RS485 interface converters/cables/dongles/adapters
- MCU-based devices to USB host interface
- Point-of-Sale (POS) Terminals/Printers/Pole Displays
- USB Barcode/Smart Card Readers
- PC I/O Docking Station/Port Replicators
- Healthcare/Medical USB Interface Data Transfer Cable
- Serial-over-IP Wireless Solution
- Cellular/PDA USB Interface Data Transfer Cable
- GPS/Navigation USB Interface
- Industrial / Instrumentation / Automation Control USB Interface
- USB Modem / Wireless / Zigbee USB Interface
- Set-Top Box (STB) / Home Gateway USB Interface
- Battery Charger Detection for high-current and quick charging of batteries.

2. Royalty-Free Driver Support

- Windows 10, 8, 7, Vista, XP, (Microsoft Certified WHQL Drivers)
  - Windows Update Driver installation available in Windows 7 and above (32/64-bit)
- Windows Server 2003, 2008, 2008 R2, 2012, 2016
- Windows Embedded Industry, Point-of-Service (WEPOS), and POSReady
- Windows Embedded Compact, Windows Embedded CE, Windows CE
- Mac OS X
- Linux OS
- Android 3.2 and above

3. Ordering Information

Chip Product Name	Package Type	Ordering Part Number	MPQ
PL2303GC	28-pin SSOP	PL2303G4ZJG7P2	48pcs / tube
		PL2303G4ZJG8P2	2000pcs / reel
	24-pin UQFN	PL2303G4FIG7P2	490pcs / tray
		PL2303G4FIG8P2	4000pcs / reel

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4. Block Diagram

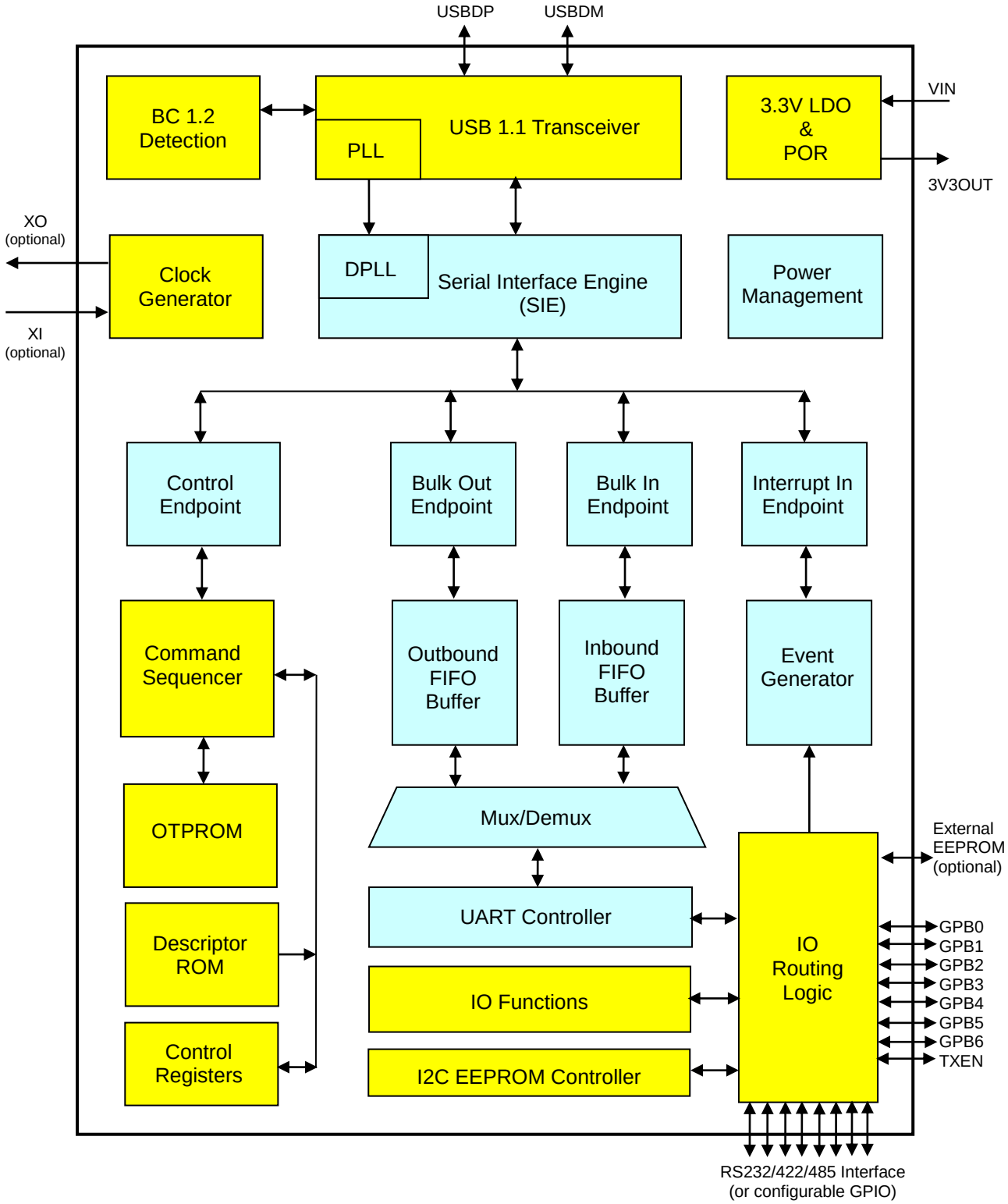

Figure 4-1 PL2303GC Block Diagram

5. USB Logo Certification

The PL2303GC IC has been certified by the USB-IF organization with TID 40001838 to be fully compliant with the USB 2.0 specification.

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6. Overview

The new PL2303GC chip is one of the latest G-Series IC product added to the popular PL2303 USB to Serial (UART) Bridge Controller family, replacing the PL2303HXD mainstream chip. It provides an advanced full-featured single-chip bridge solution for connecting a full-duplex UART asynchronous serial interface device to any Universal Serial Bus (USB) capable host. The PL2303GC provides highly compatible USB drivers to simulate the traditional COM port (via virtual COM Port) on most operating systems allowing existing serial UART applications based on legacy COM port to easily migrate and be made USB ready.

The new PL2303GC is pin-to-pin compatible with the popular PL2303HXD chip (SSOP28). It also integrates an internal precise clock generator (no external crystal required), USB 1.1 transceiver, Serial Interface Engine (SIE), LDO voltage regulator, power-on- reset (POR), FIFO data buffers, and OTPROM.

The PL2303GC added several new features and enhancements:

- Integrated termination resistors and pull-up resistor to reduce PCB external components.
- New USB drivers for different OS platforms with faster performance and advanced features.
- Precise baud rate generator (up to 12Mbps).
- OTPROM can be programmed directly through USB (no high voltage generator required).
- Larger TX/RX FIFO data buffers (1024-byte).
- Up to 16 configurable GPIO pins.
- Versatile GPIO functions and routing logic (TX/RX LED, VBUS_DET, USB_CFG, CLK_OUT, etc.).
- Supports 3.3V VBUS voltage operation.
- Wide I/O voltage range (1.8V/2.5V/3.3V/5V).
- Configurable I/O pin output driving strength.
- UART inverted signal configurable option.
- Unique USB Serial Number for each IC.
- Supports Battery Charger (BC1.2) Detection to enable fast charging of batteries.

The PL2303GC is designed to support a wide-range of serial application domain including mobile, embedded, industrial, consumer, healthcare, navigation, and wearable solutions in mind. It provides a small footprint that could easily fit in to any connectors and handheld devices. With very small power consumption in either operating or suspend mode, the PL2303GC is perfect for bus powered operation with plenty of power left for the attached devices. Flexible signal level requirement on the RS232-like serial port side also allows the PL2303GC to connect directly to any 5V~1.8V range devices.

The PL2303GC is available in two small footprint Pb-free (RoHS compliant) green compound packages: 28-pin SSOP and 24-pin UQFN packages.

6.1 PL2303 G-Series USB to Serial Family Product Table

Prolific's new PL2303 G-series USB to Serial family product line offers a variety of new advanced features for USB serial interface product design. The PL2303 G-series are redesigned to provide accurate and flexible baud rate support as well as plenty of I/O functions that can be easily configured in OTPROM memory.

PL2303 G-Series USB to Serial (UART) Family Product Line					
Product	**PL2303GC**	**PL2303GS**	**PL2303GE**	**PL2303GT**	**PL2303GL**
Description	**USB to Full UART (Integrated Clock)**	USB to Full UART (Integrated Clock)	USB to Full UART (High ESD Protection)	USB to RS232 (Internal RS232 Transceiver)	USB to Basic UART (Low-Pin Count)
Packages	**SSOP28 UQFN24**	SSOP16	SSOP28	SSOP28	SOP8
UART Interface	**RS232 RS422/RS485**	RS232 RS422/RS485	RS232 RS422/RS485	RS232 Only	RS232 (TX-RX Only)
Max. Data Rates	**12Mbps**	12Mbps	12Mbps	1Mbps	115200bps
Dedicated GPIO Pins	**6**	0	6	4	0
Shared GPIO (with UART pins)	**9**	9	9	0	0
Clocking	**Internal[1]**	Internal	Internal[1]	Internal	Internal
OTPROM[2]	**USB Data + Configurable GPIO Function**	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	USB Data + Configurable GPIO Function	USB Data
External EEPROM Option	**YES[3]**	YES[3]	YES[3]	YES[3]	NO
Android OS Support	**YES**	YES	YES	YES	YES
Configurable Data Buffer[4]	**768-byte (RX) 256-byte (TX)**	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)	768-byte (RX) 256-byte (TX)
Battery Charger Detection Option	**YES**	YES	YES	No	No
I/O Voltage Range	**I/O levels from 1.8V to 5V**	I/O levels from 1.8V to 5V	I/O levels from 1.8V to 5V	3.3V	I/O levels from 1.8V to 5V
Pin Compatible	**PL2303HXD (SSOP28 only)**	New design	PL2303EA	PL2303RA	PL2303SA

[1] – Also supports external crystal clock source to bypass internal clock.

[2] – OTPROM allows setting the USB data descriptors. Also allows setting of multi-function GPIO options.

[3] – External EEPROM (when enabled in OTPROM) will override OTPROM settings.

[4] – TX/RX data buffers are configurable in OTPROM (PL2303GC, PL2303GS, and PL2303GE); or by driver customization.

7. Pin Diagram and Description

7.1 SSOP28 Pin Diagram

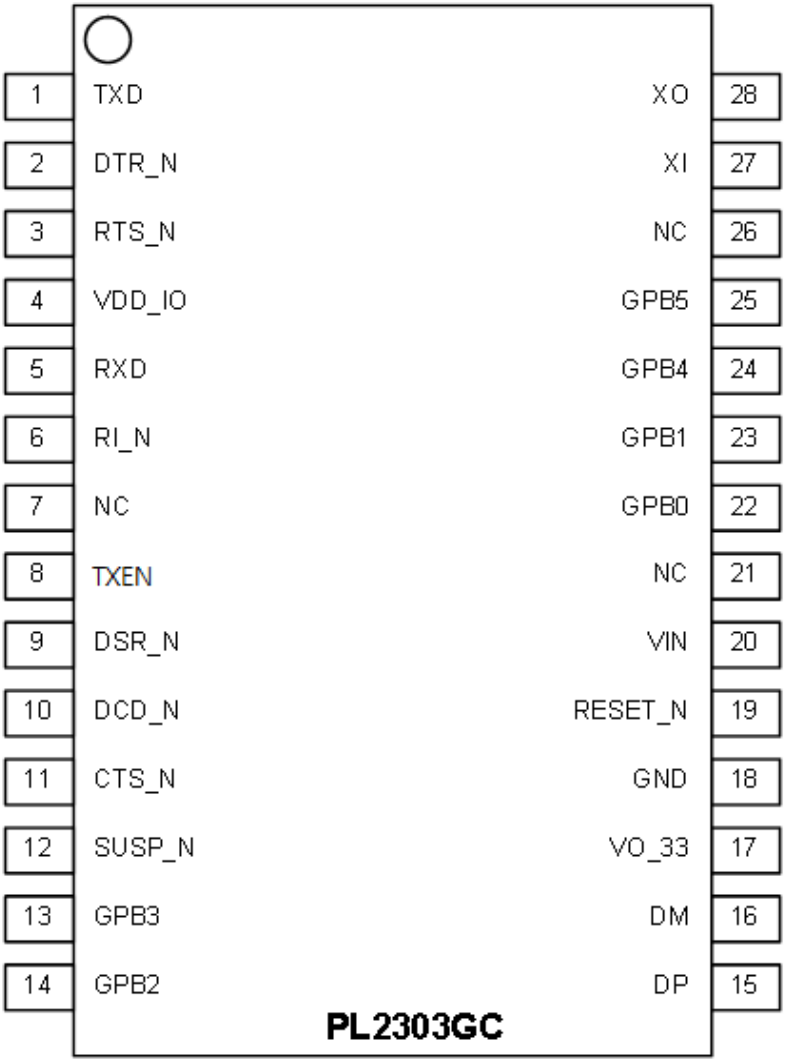


Figure 7-1 PL2303GC Pin Diagram (SSOP28)

7.2 UQFN24 Pin Diagram

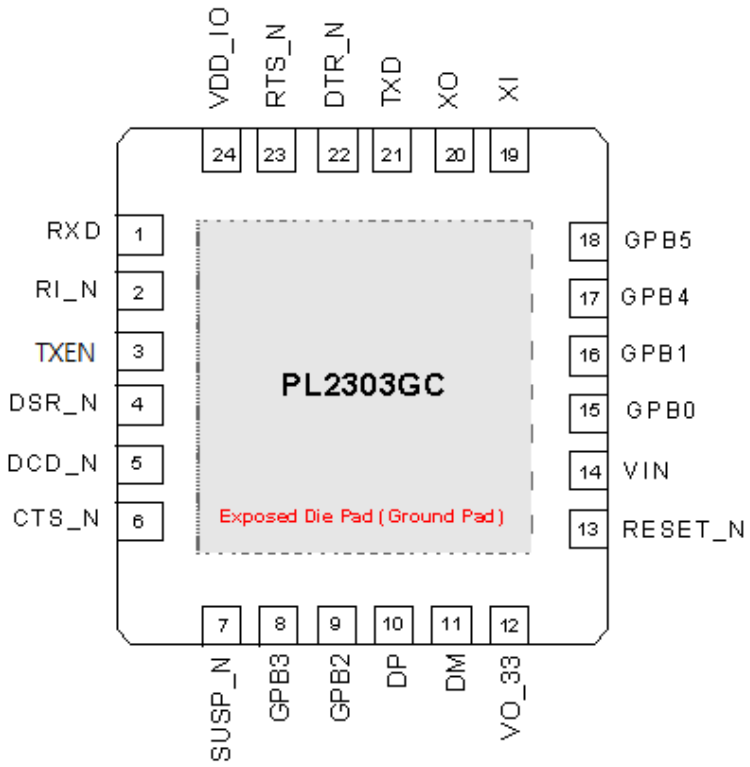


Figure 7-2 PL2303GC Pin Diagram (UQFN24)

7.3 Pin Out Description

Table 7-1: USB Data Interface Pins

Pin Name	SSOP28 Pin No.	UQFN24 Pin No.	Type	Description
DP	15	10	I/O	USB Port Data Plus (D+) Signal.
DM	16	11	I/O	USB Port Data Minus (D-) Signal.

Table 7-2: UART (Serial Port) Interface Pins

Pin Name	SSOP28 Pin No.	UQFN24 Pin No.	Type	Description
TXD	1	21	Output	Serial Port: Transmitted Data Output
DTR_N	2	22	Output	Serial Port: Data Terminal Ready Control Output
RTS_N	3	23	Output	Serial Port: Request To Send Control Output
RXD	5	1	Input	Serial Port: Received Data Input
RI_N	6	2	Input	Serial Port: Ring Indicator (Remote Wakeup) Control Input
DSR_N	9	4	Input	Serial Port: Data Set Ready Control Input
DCD_N	10	5	Input	Serial Port: Data Carrier Detect Control Input
CTS_N	11	6	Input	Serial Port: Clear To Send Control Input

Table 7-3: Configurable GPIO Pins – Group A (Shared with Serial Port Pins)

Pin Name	SSOP28 Pin No.	UQFN24 Pin No.	Type	Description
GPA0	1	21	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is TXD serial port output pin.**
GPA1	5	1	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is RXD serial port input pin.**
GPA2	3	23	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is RTS_N serial port output pin.**
GPA3	11	6	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is CTS_N serial port input pin.**
GPA4	2	22	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is DTR_N serial port output pin.**
GPA5	9	4	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is DSR_N serial port input pin.**
GPA6	10	5	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is DCD_N serial port input pin.**
GPA7	6	2	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is RI_N serial port input pin.**

Table 7-4: Configurable GPIO Pins – Group B

Pin Name	SSOP28 Pin No.	UQFN24 Pin No.	Type	Description
GPB0	22	15	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB1	23	16	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB2	14	9	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB3	13	8	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB4	24	17	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB5	25	18	I/O	Configurable GPIO Pin. (see Section 7.4)
GPB6	12	7	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is SUSP_N output pin.**
GPB7	8	3	I/O	Configurable GPIO Pin. (see Section 7.4) **Factory default is TXEN output pin**

NOTE: All GPB pins are default Input mode (except GPB6).

Table 7-5: Power and Ground Pins

Pin Name	SSOP28 Pin No.	UQFN24 Pin No.	Type	Description
VDD_IO	4	24	Power	+1.8V to +5V I/O signal power input pin. **Note: VDD_IO voltage should not larger than VIN voltage.**
VO_33	17	12	Power	+3.3V output power from integrated LDO regulator. For self-powered design, supply +3.3V to this pin.
GND	18	Exposed Pad	Power	Ground
VIN	20	14	Power	USB port VBUS input power supply. For self-powered design, supply +3.3V to this pin.

Table 7-6: Miscellaneous Pins

Pin Name	SSOP28 Pin No.	UQFN24 Pin No.	Type	Description
SUSP_N	12	7	Output	Active low Shutdown control pin. Can be used to shutdown external RS232 transceiver.
RESET_N	19	13	Input	Active low Reset pin. Can be used by external device to reset the PL2303GC. NOTE: This pin has internal pull-high. It can be pull up to VIN or VDD_IO.
XI	27	19	Input	Optional. 12MHz crystal oscillator input. If not used, leave pin floating.
XO	28	20	Output	Optional. 12MHz crystal oscillator output. If not used, leave pin floating.
NC	7, 21, 26	-	NC	No internal connection. Leave floating.

7.4 GPIO Multi-Function Options

The PL2303GC chip (SSOP28 package) provides a total of 16 configurable GPIO (General Purpose I/O) pins. The pins are grouped into GPA and GPB set of pins. The table below shows the possible functions that can be configured for each GPIO pin. These special functions can be easily configured in the OTPROM of the PL2303GC or to an external I2C EEPROM using the Prolific OTPROM/EEPROM software tool. When these pins are configured as standard GPIO pins, customers can refer to the Prolific GPIO SDK (software development kit) to develop software to control the GPIO pins for customer application desired functions.

Table 7-7: Configurable GPIO Multi-Function Pins

GPIO	SSOP28 Pin No.	UQFN24 Pin No.	Factory Default	Configurable Options (using OTPROM Tool)				
GPA0	1	21	TXD					
GPA1	5	1	RXD					
GPA2	3	23	RTS	TX_LED	CLK_OUT	SUSP_N	USB_CFG	TXEN
GPA3	11	6	CTS	RX_LED	TRX_LED	WAKEUP	VBUS_DET	BC_DET
GPA4	2	22	DTR	TX_LED	CLK_OUT	USB_CFG	EE_SDA	
GPA5	9	4	DSR	RX_LED	TRX_LED	BC_SUSP_N	EE_SCL	
GPA6	10	5	DCD	VBUS_DET	BC_DET	TXEN		
GPA7	6	2	RI (WAKEUP)					
GPB0	22	15	GPIO Input Pin	TX_LED	CLK_OUT			
GPB1	23	16	GPIO Input Pin	RX_LED	TRX_LED			
GPB2	14	9	GPIO Input Pin	VBUS_DET	EE_SDA			
GPB3	13	8	GPIO Input Pin	USB_CFG	EE_SCL			
GPB4	24	17	GPIO Input Pin	CLK_OUT	BC_SUSP_N			
GPB5	25	18	GPIO Input Pin	BC_DET				
GPB6	12	7	SUSP_N	USB_CFG	WAKEUP	CLK_OUT		
GPB7	8	3	TXEN Pin	GPIO Input				

Table 7-8: GPIO Multi-Function Option Descriptions

GPIO Function	SSOP28 GPIO Pins	UQFN24 GPIO Pins	Type	Description
TX_LED	GPA2 (Pin 3) GPA4 (Pin 2) GPB0 (Pin 22)	GPA2 (Pin 3) GPA4 (Pin 2) GPB0 (Pin 22)	Output	Serial Port: TXD Access LED.
RX_LED	GPA3 (Pin 11) GPA5 (Pin 9) GPB1 (Pin 23)	GPA3 (Pin 11) GPA5 (Pin 9) GPB1 (Pin 23)	Output	Serial Port: RXD Access LED.

TRX_LED	GPA3 (Pin 11) GPA5 (Pin 9) GPB1 (Pin 23)	GPA3 (Pin 11) GPA5 (Pin 9) GPB1 (Pin 23)	Output	Serial Port: TXD and RXD Access LED.
VBUS_DET	GPA3 (Pin 11) GPA6 (Pin 10) GPB2 (Pin 14)	GPA3 (Pin 11) GPA6 (Pin 10) GPB2 (Pin 14)	Input	When this pin is set to VBUS_DET mode, the device will not attach to USB until VBUS_DET input pin goes to high level. There must be only one pin configured as VBUS_DET pin.
USB_CFG	GPA2 (Pin 3) GPA4 (Pin 2) GPB3 (Pin 13) GPB6 (Pin 12)	GPA2 (Pin 3) GPA4 (Pin 2) GPB3 (Pin 13) GPB6 (Pin 12)	Output	When device is attached to USB port and configured by USB host, this USB_CFG pin will output to high level. This pin can be used to enable system function after USB is configured.
TXEN	GPA2 (Pin 3) GPA6 (Pin 10) GPB7 (Pin 8)	GPA2 (Pin 3) GPA6 (Pin 10) GPB7 (Pin 8)	Output	Transmit Data Enable Pin can be used to enable RS485/RS422 transceiver when data is being transmitted.
SUSP_N	GPA2 (Pin 3) GPB6 (Pin 12)	GPA2 (Pin 3) GPB6 (Pin 12)	Output	Active low Shutdown control pin. This pin has two options to choose. One is to indicate chip suspend state by USB bus state. The other option (factory default) is to indicate chip un-configured state and chip suspend state. These two options can be configured in OTPROM or EEPROM.
WAKEUP	GPA3 (Pin 11) GPA7 (Pin 6) GPB6 (Pin 12)	GPA3 (Pin 11) GPA7 (Pin 2) GPB6 (Pin 12)	Input	The remote wakeup function is to wake up chip from suspended state when this pin toggle in suspend state. There must be only one pin configured as WAKEUP pin. The factory default is RI (GPA7) pin.
BC_DET	GPA3 (Pin 11) GPA6 (Pin 10) GPB5 (Pin 25)	GPA3 (Pin 11) GPA6 (Pin 10) GPB5 (Pin 25)	Output	Battery Charge Detect pin. This active high pin indicates BC 1.2 DCP/CDP is detected.
BC_SUSP_N	GPA5 (Pin 9) GPB4 (Pin 24)	GPA5 (Pin 9) GPB4 (Pin 24)	Output	This pin has same function as SUSP_N except this pin will be forced inactive in chip suspend state when BC 1.2 DCP/CDP is detected.
CLK_OUT	GPA2 (Pin 3) GPA4 (Pin 2) GPB0 (Pin 22) GPB4 (Pin 24) GPB6 (Pin 12)	GPA2 (Pin 3) GPA4 (Pin 2) GPB0 (Pin 22) GPB4 (Pin 24) GPB6 (Pin 12)	Output	This pin can generate clock output up to 12MHz. Clock rates can be configured in OTPROM/EEPROM or customized driver. **Note: Only one GPIO pin can be configured as CLK_OUT function.**
EE_SDA	GPA4 (Pin 2) GPB2 (Pin 14)	GPA4 (Pin 2) GPB2 (Pin 14)	Input/ Output	External I2C EEPROM interface serial data signal.
EE_SCL	GPA5 (Pin 9) GPB3 (Pin 13)	GPA5 (Pin 9) GPB3 (Pin 13)	Input/ Output	External I2C EEPROM interface serial clock signal.

8. Functional Description

This section details the functional block diagram description of the PL2303GC.

8.1 BC 1.2 Detection

This function is used to detect VBUS power supply capability of USB host port and provides charging control to battery charging IC. This function is enabled in OTPROM by setting GPIO pin to BC_DET option. This pin will indicate if BC 1.2 DCP/CDP is detected when device is attached to the USB port. The external battery charging IC uses the USB_CFG and SUSP_N signal pins to control its charging current support or the BC_DET signal pin to enable fast charging current mode.

8.2 USB 1.1 FS Transceiver

The USB Transceiver provides the USB full-speed electrical signal requirements and USB physical interface (DP/DM). This block also includes one precise internal oscillator for PLL. The PLL provides the clock to other logic functions. This block also includes the internal USB series termination resistors on the USB data lines and pull-up resistor for the DP signal.

8.3 LDO Regulator

This block is the 5V to 3.3V LDO regulator to power and drive the USB transceiver. It also includes 3.3V brownout detection output signals that will be used by digital circuit to reset the chip. The LDO 5V to 3.3V can supply 100mA for chip internal and external components.

8.4 Clock Generator

The clock generator module generates the 48MHz and 12MHz reference clock signals for internal chip logic. The internal clocks will be stopped while in suspend state.

8.5 USB FS SIE

The USB Full-Speed Serial Interface Engine (SIE) block performs the processing of USB DP/DM signals. It translates the internal parallel data to serial data and outputs to USB FS transceiver to generate external USB DP/DM signals timing. It also translates external USB DP/DM signals pass through USB FS transceiver to parallel data for internal circuit. This block supports USB packet decoding and encoding. It also generates and check packet CRC, bit stuffing, SYNC and EOP frame signal. The DPLL module will use the internal 48MHz clock to synchronize external DP/DM transitions to generate 12MHz clock for USB interface related circuit.

8.6 Power Management

This module will monitor the USB attachment and DP/DM signals state to create reset state, running state, suspend state, wakeup state, etc.

8.7 Control Endpoint

The Control Endpoint module handles control endpoint packet transfer protocols such as SETUP packet, DATA packet and return status packet.

8.8 Bulk Out Endpoint

The Bulk Out Endpoint module handles bulk-out endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers USB host bulk-out data to chip outbound FIFO.

8.9 Bulk In Endpoint

The Bulk In Endpoint module handles bulk-in endpoint packet transfer protocols such as DATA packet and return status packet. It also transfers data inside the chip inbound FIFO to USB host through bulk-in DATA packet.

8.10 Interrupt In Endpoint

The Interrupt In Endpoint module handles interrupt-in endpoint packet transfer protocols such as DATA packet and return status packet. It transfers interrupt data generated inside the chip to USB host through interrupt-in DATA packet.

8.11 Command Sequencer

This module handles the USB standard requests and vendor requests. It dispatches control signals to relative peripheral modules and gather information from peripheral modules. When it received USB standard request commands, it may check ROM data or data latched from OTP and return them to USB host. When vendor requests are received, it dispatches to peripherals to set or get something.

8.12 Outbound FIFO

This buffer receives data from Bulk Out Endpoint and provides data to peripheral modules. It handles read and write pointers and calculate full and empty conditions. There are also near empty threshold check to notify peripheral module that FIFO is going to empty.

8.13 Inbound FIFO

This buffer receives data from peripheral modules and provides data to Bulk In Endpoint. It handles read and write pointers and calculate full and empty conditions. There are also near full threshold check to notify peripheral module that FIFO is going to full.

8.14 Event Generator

This module provides interrupt data to Interrupt In Endpoint. This module senses interrupt event toggle from UART peripheral and GPIO module.

8.15 Internal OTPROM

The OTPROM (One-Time Programming Read-Only Memory) is used to store chip function settings, GPIO pin function setting and USB descriptor related data. A one-time programming user area of the memory is available to allow customization of settings. The user area of the PL2303GC OTPROM can now be easily programmed using the Prolific OTPROM software through USB port without any additional voltage converter requirement. Refer to Section 9.0 for more information on the OTPROM configuration settings.

8.16 Mux/Demux

This module is designed to pass data between FIFO and UART peripheral module.

8.17 Descriptor ROM

This block contains the USB descriptor data for returning to USB host.

8.18 UART Control

The UART Control module handles the data transfer according to RS232 format and interface. Full set flow control is implemented including RTS/CTS, DTR/DSR and software flow control. Flow control circuit will check FIFO near full or near empty status to activate flow control signals. This module includes a precise baud rate generator that can generate baud rates up to 12Mbps. The baud rate is set from USB command.

8.19 Control Registers

The Control Registers module contains the chip control registers read and set, and initially loads from OTPROM. USB host will use USB vendor command to read and write control registers to set chip function.

8.20 IO Functions

The IO Functions block implements generic GPIO function and many configurable I/O functions such as TX access LED and RX access LED features, clock output features, and others (see Section 7.4).

8.21 I/O Routing Logic

The PL2303GC has many versatile I/O functions. Each GPIO pin is provided with multiple functions that can be configured in the OTPROM. This module multiplexes I/O functions to different chip I/O pins. It also handles I/O pin polarity, open-drain, pull-up/pull-down, and I/O pin drive capability functions.

8.22 I2C EEPROM Controller

The I2C EEPROM Controller provides an optional alternative solution to the OTPROM that allows an external I2C EEPROM to be attached through GPIO pins 2 and 9 (GPA4/GPA5); or pins 14 and 13 (GPB2/GPB3) for the SDA and SCL interface. Using the PL2303G OTPROM/EEPROM Writer program, customer can also write the chip function settings, GPIO pin function settings, and USB descriptor related data to external I2C EEPROM. The advantage of using an external EEPROM is that it can be written several times. The Prolific OTPROM/EEPROM software works by plugging the device through USB port without any additional voltage converter requirement. Refer to Section 9.0 for more information on the OTPROM/EEPROM configuration settings.

9. Chip Function Configuration

The default configuration descriptors are stored in the chip internal memory which will be loaded during power-on reset or USB bus reset whenever OTPROM is empty. Several of the USB and configuration descriptors could be modified and programmed one-time into the chip's OTPROM using the PL2303GC OTPROM/EEPROM Writer utility program. These descriptors include Vendor ID, Product ID, Serial Number, Product String, UART settings, GPIO configurations, and other configuration descriptors. The PL2303GC chip also provides an option to use an external I2C EEPROM to write the configurations several times.

9.1 USB Data Configuration

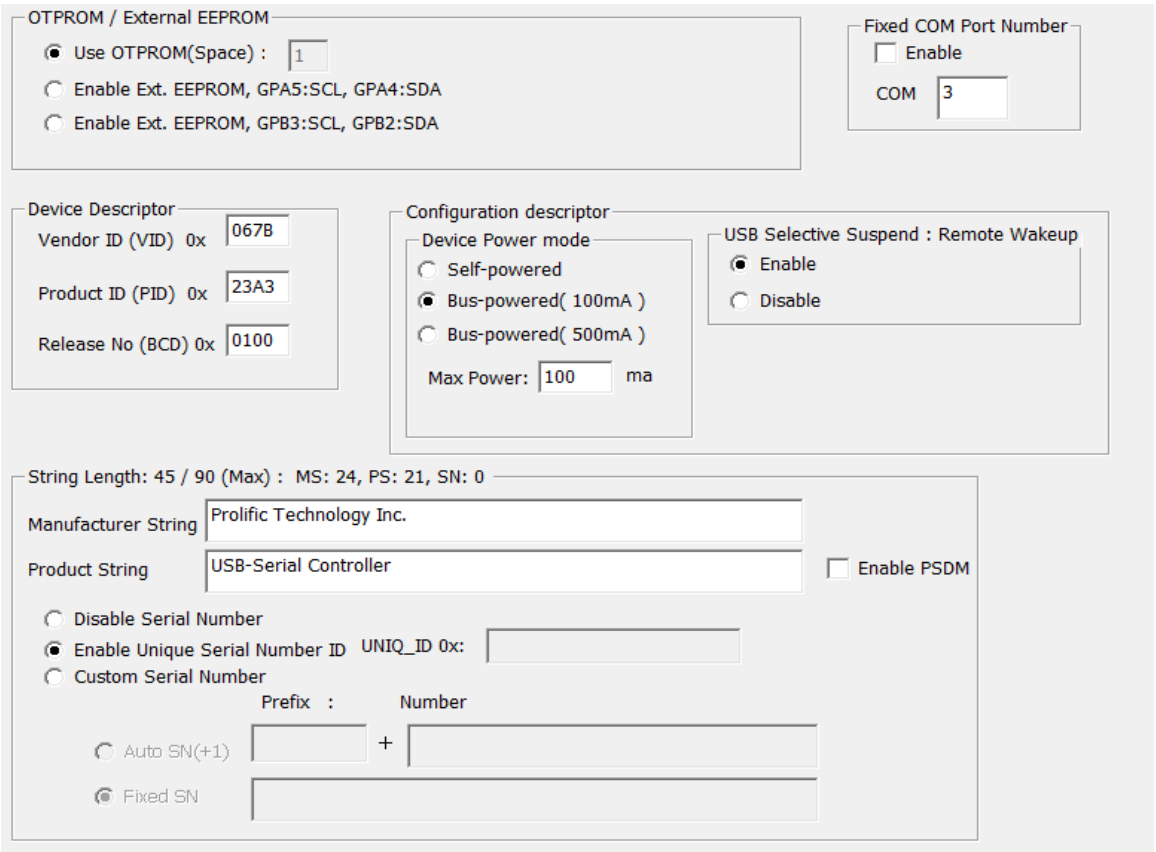


Table 9-1 USB Descriptor Configuration

Descriptors	Default Value	Description
OTPROM / External EEPROM	Use OTPROM	This field allows writing the chip configuration settings either into the OTPROM or to an external EEPROM. • Use OTPROM – this option will write the new settings into the chip's OTPROM. The OTPROM can only be written once. If the Space box denotes a 1, it means it can be written. • Enable Ext. EEPROM (GPA5:SCL, GPA4:SDA) – this option can be used if there is an external I2C EEPROM attached to pins GPA5 and GPA4 of PL2303GC. Settings will be written to the external

		EEPROM and can be written several times. • Enable Ext. EEPROM (GPB3:SCL, GPB2:SDA) – this option can be used if there is an external I2C EEPROM attached to pins GPB3 and GPB2 of PL2303GC. Settings will be written to the external EEPROM and can be written several times. **NOTE: PL2303GC chip can only allow a one-time switch from OTPROM to Ext EEPROM or vice-versa.**
Vendor ID (VID)	067B (hex)	USB unique Vendor ID of Company or Manufacturer. This ID is applied and registered from USB-IF. Refer to this website for applying VID: http://www.usb.org/developers/vendor/
Product ID (PID)	23A3 (hex)	USB Product ID assigned by Manufacturer.
Release No. (BCD)	0100 (hex)	This field reports the release number of the USB device chip. This item is not allowed to be modified.
Device Power Mode	Bus Powered (100mA)	This field sets the USB device if bus-powered or self-powered device.
Max Power	100mA	This field sets the USB device maximum power that can be drawn by the device from the USB host. Enter the value here if it is not 100mA or 500mA. Expressed in 2 mA units (i.e., 50 = 100 mA).
USB Selective Suspend	Enable	This field enables/disables the USB Selective Suspend function. When enabled, Windows OS will suspend the device when idle for few seconds (COM port not open).
Manufacturer String	Prolific Technology Inc.	This field contains the product manufacturer string.
Product String	USB-Serial Controller	This field when entered will be the device string displayed by Windows and other OS when device is first detected and before driver is loaded or driver not installed. After driver is loaded, Windows will show the product string written inside the driver INF file.

Serial Number	Enable Unique Serial Number ID	• Disable Serial Number – this option will disable the Serial Number. Operating System will assign a random serial number for the device.
		• Enable Unique Serial Number ID – this default option enables the unique serial number pre-programmed inside the chip.
		• Custom Serial Number – this option allows the customer to set own product serial numbering:
		  ○ Auto SN: allows to add prefix while the numbers auto increment after each write.
		  ○ Fixed SN: this will write the same number.
		Device with serial number enabled allows the device to be assigned with the same COM port number even when plug to other USB ports of the same PC.

NOTE: The total string length for the manufacturer + product + serial number string is up to 90 characters.

9.2 UART Configuration

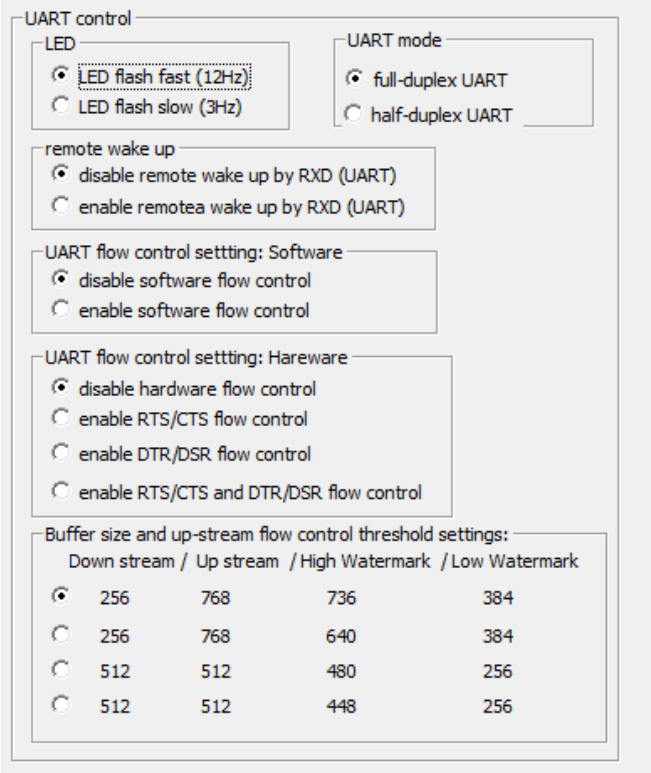


Table 9-2 UART Startup Configuration

Functions	Default Value	Description
LED Flash	Fast	This option sets the flashing speed of the access LED when configured using the TX_LED, RX_LED, TRX_LED GPIO pins. Fast 11.4Hz and slow 2.8Hz.
UART Mode	Full-duplex UART	• Full-Duplex UART – this default setting allows simultaneous transmission of TX and RX lines. • Half-Duplex UART – this option only allows for one-way transmission at a time. When there is no data transmission, TXD will be tri-state.
Remote Wakeup (RXD)	Disable	This allows using the RXD pin as remote wakeup. The received data from RXD may be wrong while chip is waking up.
Software Flow Control	Disable	This option allows setting the software flow control (Xon/Xoff) during chip initial startup. In general, this option need not enabled because driver or software can control this option.
Hardware Flow Control	Disable	This option allows setting the hardware flow control (RTS/CTS, DTR/DSR, Both) during chip initial startup. In general, this option need not enabled because driver or software can control this option.
Buffer Size Configuration	256(TX) - 768(RX) 736(HW) - 384(LW)	This sets the internal buffer size configuration for TX (downstream) and RX (upstream) as well as the high and low watermark threshold levels.

9.3 GPIO (GPA) Configuration

Also refer to Section 7.4 for the complete GPIO Multi-Function options description.

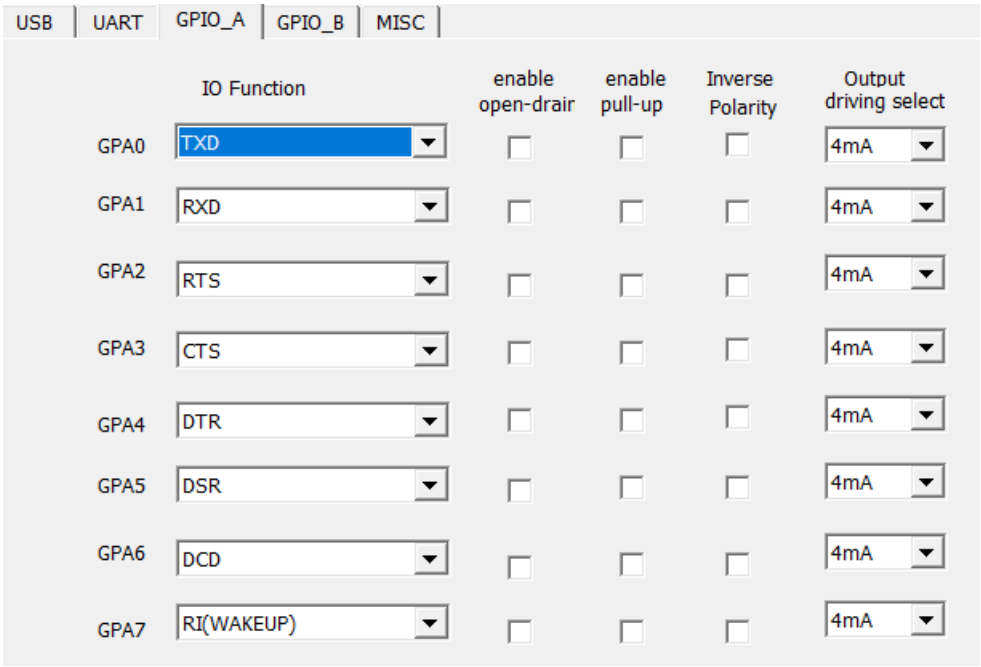


Table 9-3 GPIO (GPA Group) Configuration

GPIO Function	Default Value	Default I/O	Description
GPA0	TXD	Output	This field also allows setting the pin as a standard GPIO. • TXD (default) • GPIO (General Purpose I/O)
GPA1	RXD	Input	This field also allows setting the pin as a standard GPIO. • RXD (default) • GPIO (General Purpose I/O)
GPA2	RTS	Output	This field allows setting the pin as a standard GPIO or any of the following function: • RTS (default) • TX_LED • CLK_OUT[1] (also refer to MISC folder) • SUSP_N (also refer to MISC folder) • USB_CFG • TXEN • GPIO (General Purpose I/O)
GPA3	CTS	Input	This field allows setting the pin as a standard GPIO or any of the following function: • CTS (default) • RX_LED • TRX_LED • WAKEUP

			• VBUS_DET (also refer to MISC folder) • BC_DET • GPIO (General Purpose I/O)
GPA4	DTR	Output	This field allows setting the pin as a standard GPIO or any of the following function: • DTR (default) • TX_LED • CLK_OUT[1] (also refer to MISC folder) • USB_CFG • EE_SDA • GPIO (General Purpose I/O)
GPA5	DSR	Input	This field allows setting the pin as a standard GPIO or any of the following function: • DSR (default) • RX_LED • TRX_LED • BC_SUSP_N • EE_SCL • GPIO (General Purpose I/O)
GPA6	DCD	Input	This field allows setting the pin as a standard GPIO or any of the following function: • DCD (default) • VBUS_DET (also refer to MISC folder) • BC_DET • TXEN • GPIO (General Purpose I/O)
GPA7	RI (Wakeup)	Input	This field also allows setting the pin as a standard GPIO. • RI (default) • GPIO (General Purpose I/O)
Enable Open-Drain	Disabled		This field sets the selected I/O pin to open-drain output mode.
Enable-Pull Up	Disabled		This field enables the selected I/O pin weak pull-up. **NOTE: The weak pull-up resistor is pull-up to VDD_IO. When enabling pull-up for input pins, the input signal voltage should not be higher than the VDD_IO voltage.**
Inverse Polarity	Disabled		This field inverts the selected I/O pin input and output signal polarity.
Output Driving Strength	4mA		This field sets the output driving strength of the selected pin. (4mA up to 8mA) @VDDIO3.3V

[1] **Note: Only one GPIO pin can be configured as CLK_OUT function.**

9.4 GPIO (GPB) Configuration

Also refer to Section 7.4 for the complete GPIO Multi-Function options description.

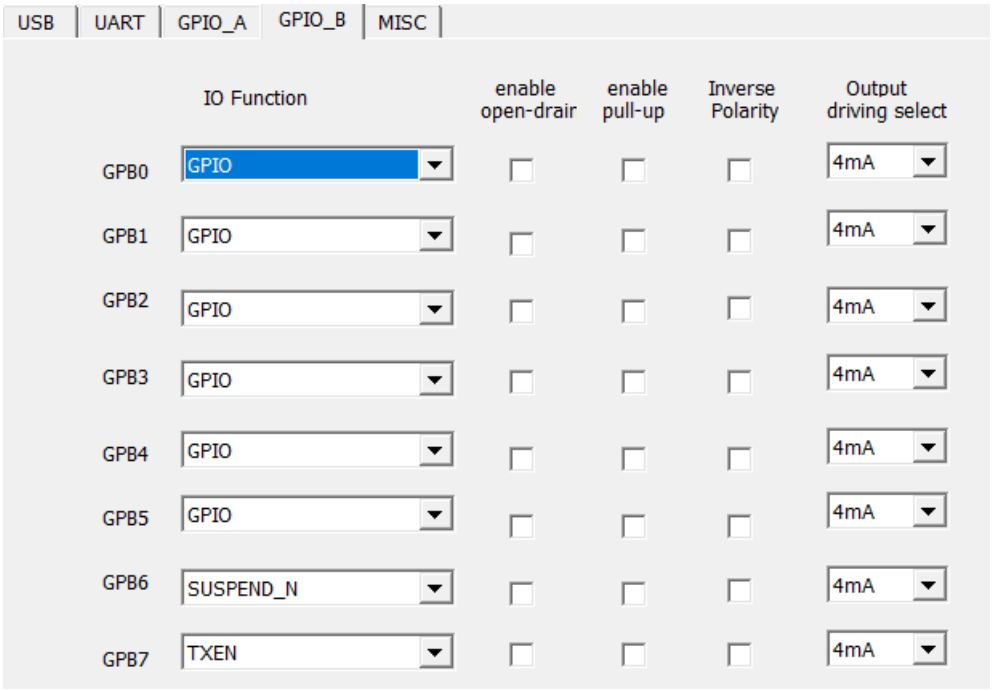


Table 9-4 GPIO (GPB Group) Configuration

GPIO Function	Default Value	Default I/O	Description
GPB0	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • TX_LED • CLK_OUT[1] (also refer to MISC folder)
GPB1	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • RX_LED • TRX_LED
GPB2	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • VBUS_DET (also refer to MISC folder) • EE_SDA
GPB3	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • USB_CFG • EE_SCL

GPB4	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • CLK_OUT[1] (also refer to MISC folder) • BC_SUSP_N
GPB5	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • BC_DET
GPB6	SUSP_N	Output	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • USB_CFG • WAKEUP • CLK_OUT[1] (also refer to MISC folder)
GPB7	GPIO	Input	This field allows setting the pin as a standard GPIO or any of the following function: • GPIO (General Purpose I/O) • TXEN
Enable Open-Drain	Disabled		This field sets the selected I/O pin to open-drain output mode.
Enable-Pull Up	Disabled		This field enables the selected I/O pin weak pull-up. **NOTE: The weak pull-up resistor is pull-up to VDD_IO. When enabling pull-up for input pins, the input signal voltage should not be higher than the VDD_IO voltage.**
Inverse Polarity	Disabled		This field inverts the selected I/O pin input and output signal polarity.
Output Driving Strength	4mA		This field sets the output driving strength of the selected pin. (4mA up to 8mA) @VDDIO3.3V

[1] **Note: Only one GPIO pin can be configured as CLK_OUT function.**

9.5 Miscellaneous (MISC) Configuration

This folder includes other miscellaneous chip configuration options including VBUS_DET, chip I/O suspend state, SUSP_N, USB chip suspend, and clock output frequency divider options.

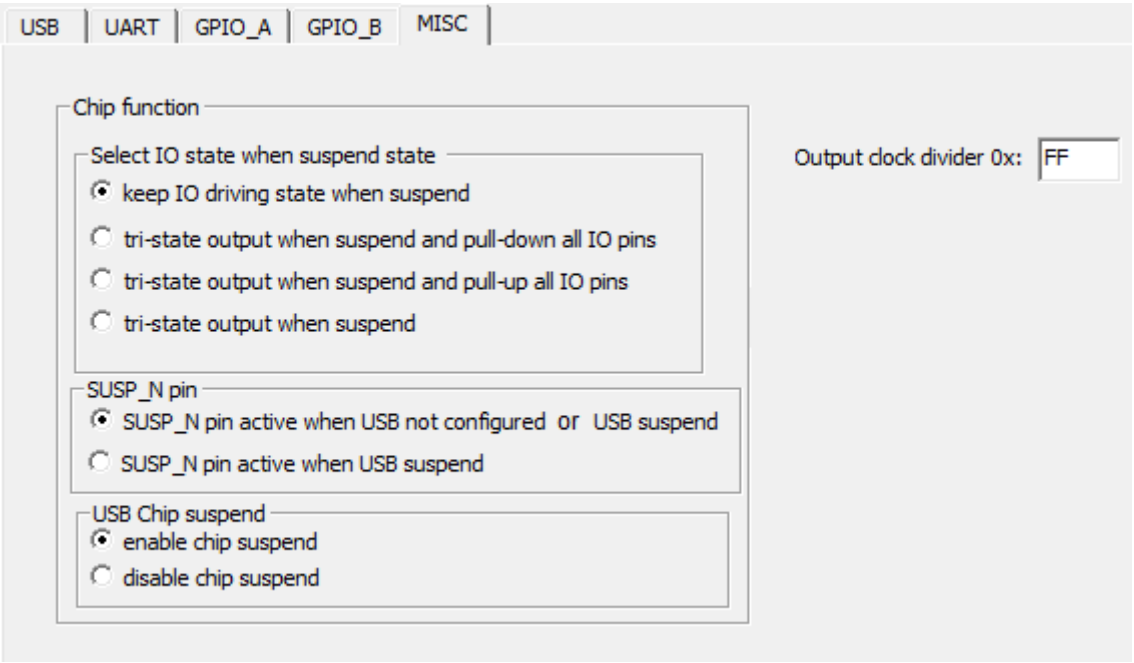


Table 9-5 Miscellaneous Configuration

Functions	Default Value	Description
Suspend Mode I/O State	Keep I/O Driving State	This option allows setting the I/O state when chip is in suspend mode.
SUSP_N Pin	Active when both USB not configured and USB suspend	This option allows setting the SUSP_N pin behavior when USB is not configured and in suspend state.
USB Chip Suspend	Enabled	This option can enable or disable the USB chip to suspend.
Output Clock Divider	0xFF	This field sets the output clock divider value. When value is 0, output clock pin will stay at low state. When value is 0xff, output clock pin will stay at high state. When other value, output clock rate is 24MHz / (1 + clock divider value). The default value can be kept as is and let customer driver or user tool through SDK to dynamic change the clock divider rate. **Note: Only one GPIO pin can be configured as CLK_OUT function.**

10. Design Application Examples

This section illustrates conceptual design application examples using the PL2303GC.

10.1 USB Bus Powered Design

The PL2303GC has a built-in 3.3V regulator. USB device power (pin VIN) can be supplied directly from USB VBUS pin. The capacitor behind the USB connector on VBUS is a defined requirement of USB specification. If the regulator output VO_33 needs to be maintained at 3.3V, VIN should be larger than 3.6V. It is also recommended to add capacitor at VO_33 pin, please refer to schematic.

This built-in 3.3V regulator can supply 100mA in addition to providing chip operating power around 10mA. It is also possible to supply power to external components under the range limit.

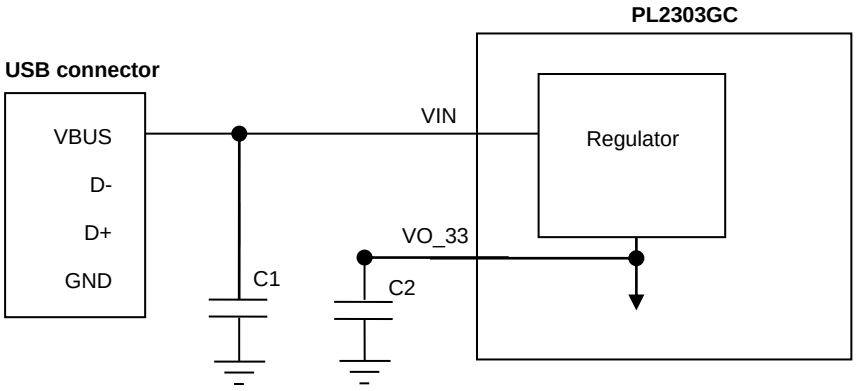


Figure 10-1 USB Bus Powered Design Example

10.2 Self Powered Design

The PL2303GC can also use external power supply. There are two possible ways to use external power source. The first is to use system power source to connect to VIN, and the chip's internal 3.3V regulator will generate the 3.3V power output VO_33 for chip operations and external components. Below Figure 10-2a shows this case. The second is to disable the internal regulator where the system should provide the same 3.3V voltage to VIN and VO_33. Under this condition, the chip will use this external 3.3V power as operating power source. See Figure 10-2b.

For USB self-powered design, it is also recommended to enable the VBUS_DET GPIO input pin function because the PL2303GC DP pin will be pulled up after power on even if USB is not attached yet. USB specification states that a DP pull-up means to attach USB. If the VBUS_DET pin function is turned on and connected to VBUS pin, the chip will only pull-up the DP pin to USB bus when VBUS_DET is active.

To use self-powered design, USB power mode descriptor in the OTPROM or EEPROM of the PL2303GC chip should also be programmed to self-powered mode to match this kind of configuration. USB hosts can read the USB descriptor of the device to know if it is a self-powered device.

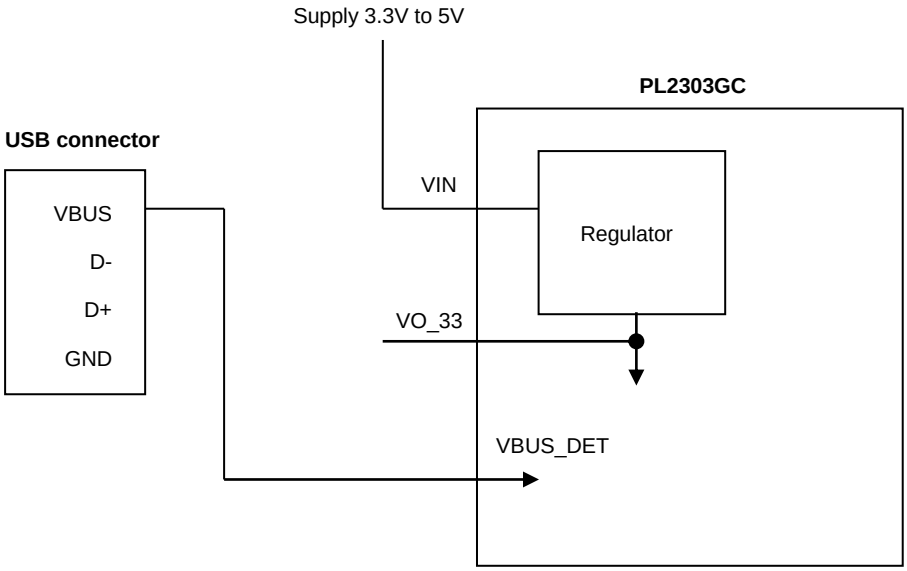


Figure 10-2a USB Self Powered Design Example 1

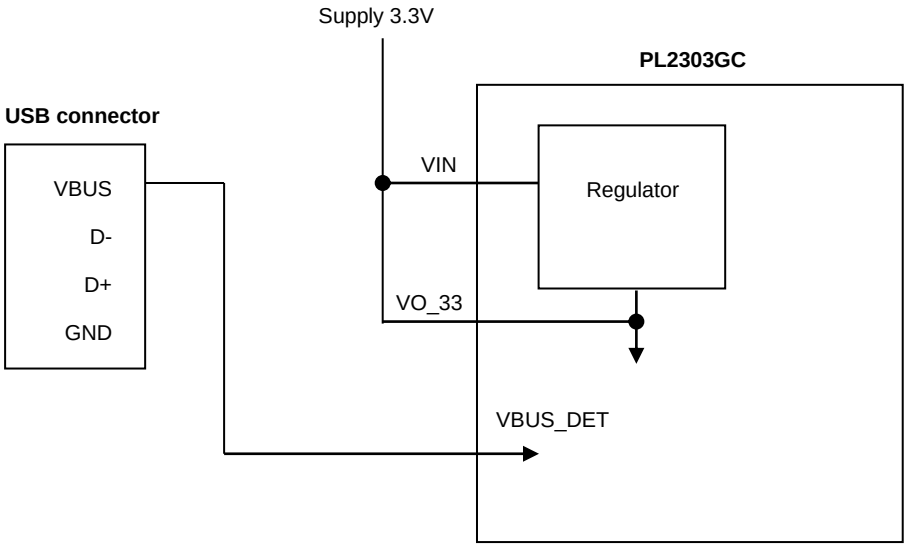


Figure 10-2b USB Self Powered Design Example 2

10.3 Chip Reset Control

The PL2303GC has an internal power on reset circuit; therefore, external reset control circuit is optional. External reset control (RESET_N pin) can help system designs to make sure of chip operation start time.

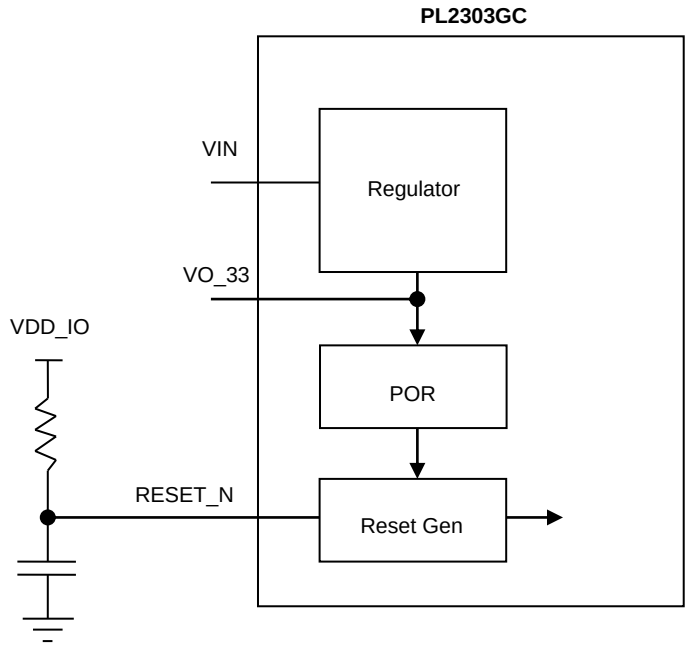


Figure 10-3a Chip Reset Control Application

The power ramp-up time shall keep below than 1ms as shown in diagram below.

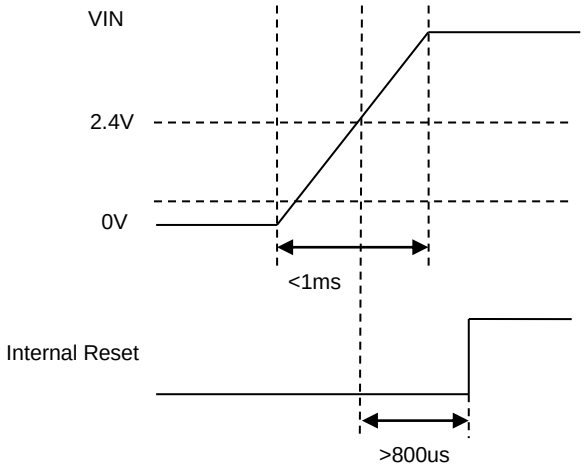


Figure 10-3b Chip Power Reset Timing Diagram

10.4 I/O Power Supply to PL2303GC

The PL2303GC supports a wide range of I/O voltage. The simple way to supply IO voltage is to directly connect VDD_IO to VO_33 pin to provide 3.3V I/O voltage. Add capacitor to VDD_IO can help to reduce I/O noise. Please refer to schematic for the detailed capacitor value.

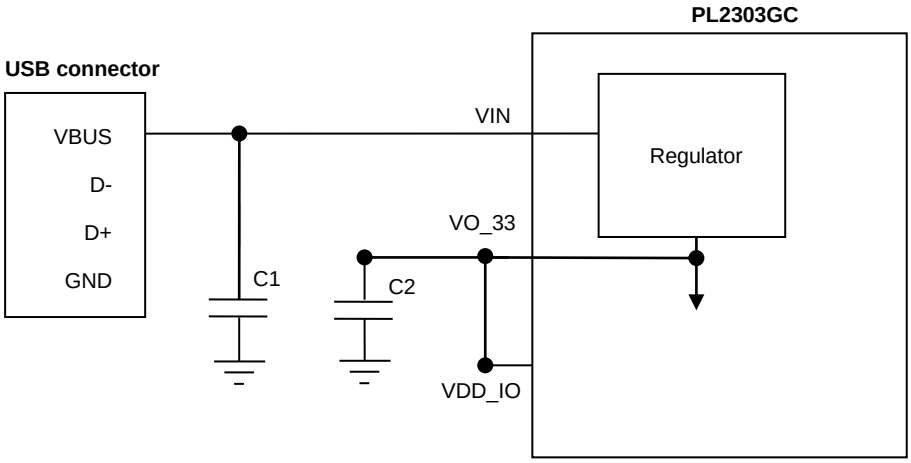


Figure 10-4a IO Power Supply

VDD_IO can also be supplied from other power source to provide different I/O voltage. All of the PL2303GC I/O pins, including UART signals, use the same VDD_IO voltage. The I/O pins does not support mixed I/O voltages. Unless open-drain option is enabled, the I/O connection between two chips shall use the same VDD_IO voltage. PL2303GC I/O pin also supports 5V tolerance which allows 5V input signal level in different VDD_IO voltage. {**Note:** VDD_IO voltage should not be larger than VIN voltage.}

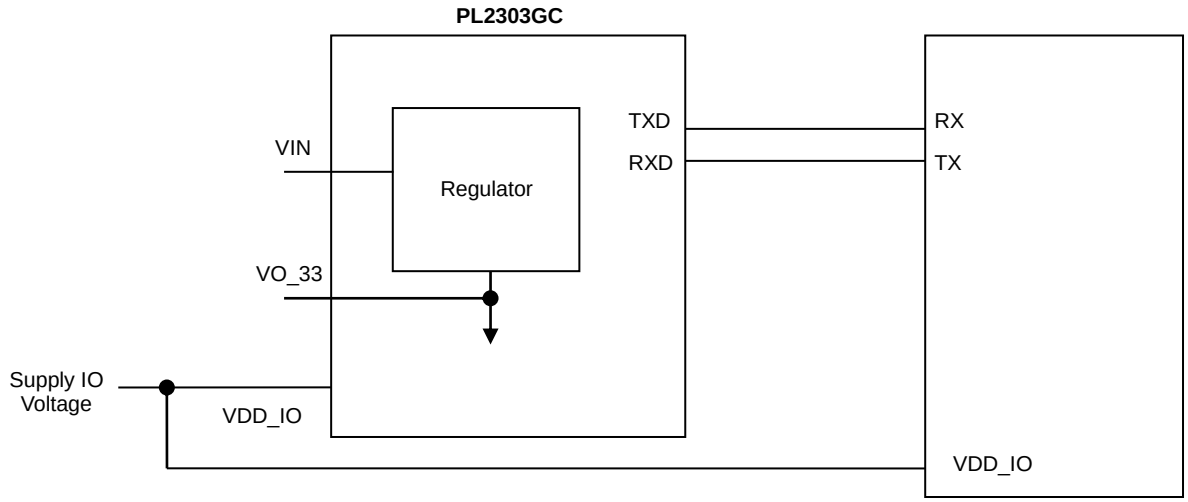


Figure 10-4b VDD_IO Voltage Supply

10.5 USB to RS232 Cable Design

The most common design application for the PL2303GC is the USB to RS232 converter cable or adapter shown in the diagram below. This design pairs the PL2303GC with an RS232 transceiver chip (ex. SIPEX SP213EHCA) to convert the PL2303GC TTL levels serial interface to RS232 level signals. The design below includes the use of the SUSP_N pin (SHTDN#) to power down the transceiver chip to sleep mode when in USB suspend mode. The default OTPROM supports this function directly and no need to program the OTP for special GPIO setting. Below diagram also shows an access LED example on how to make use of GPB0 and GPB1 pins which are configured as TX and RX access LED.

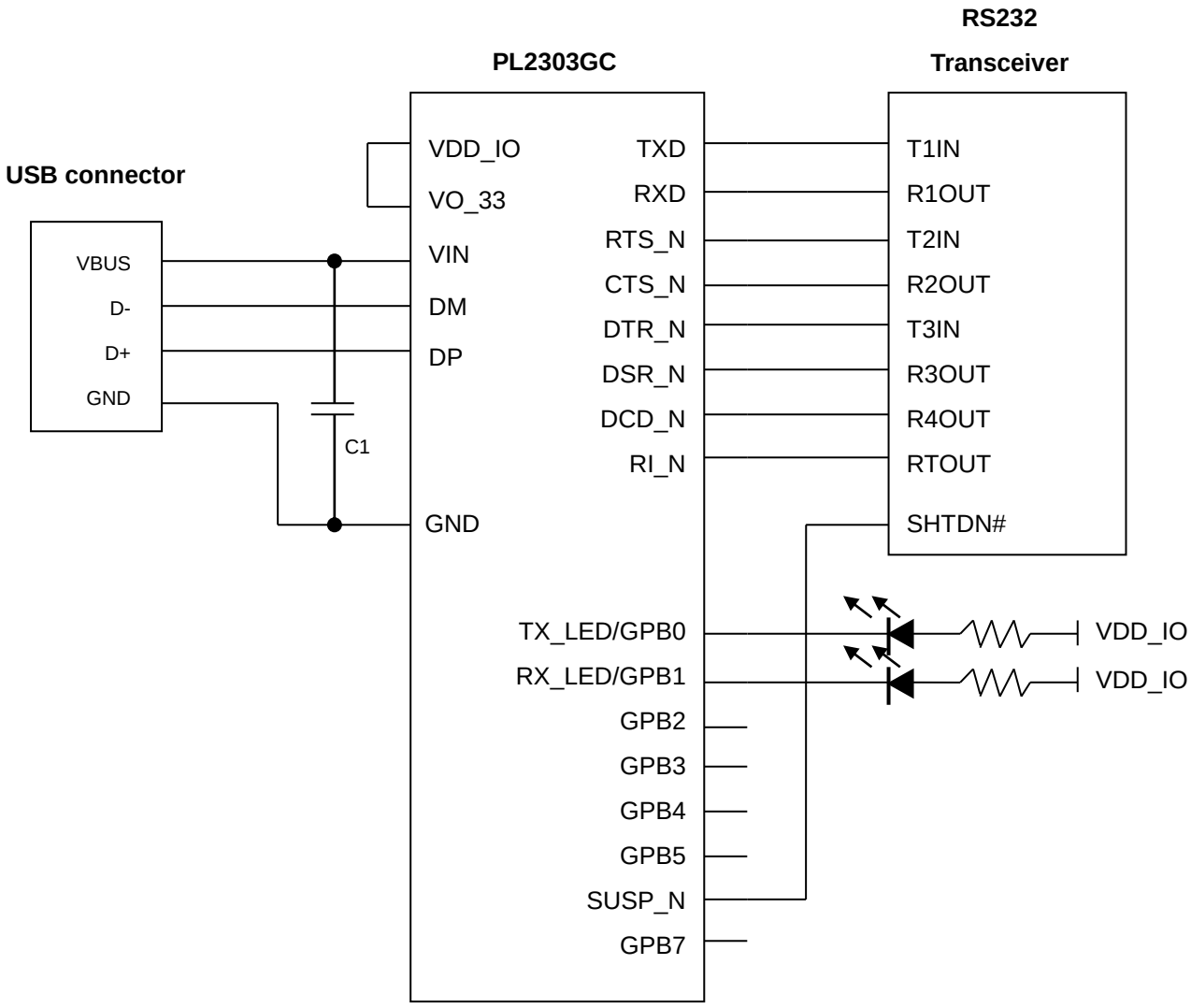


Figure 10-5 USB to RS232 Design Example

10.6 USB to RS485/RS422

Another popular application for the PL2303GC is the USB to RS485/422 design. For RS485, the chip is paired with an RS485 transceiver chip to convert the serial interface of the PL2303GC to RS485 levels. RS485 transceivers are only enabled when data is being transmitted. Hence, it needs to use the TX_EN (transmit enable) GPB7 GPIO pin to connect to the RS485 transceiver output enable pin and enable this pin function using the OTPROM software. This application can also make use of the GPB0 and GPB1 pins configured as TX and RX access LED.

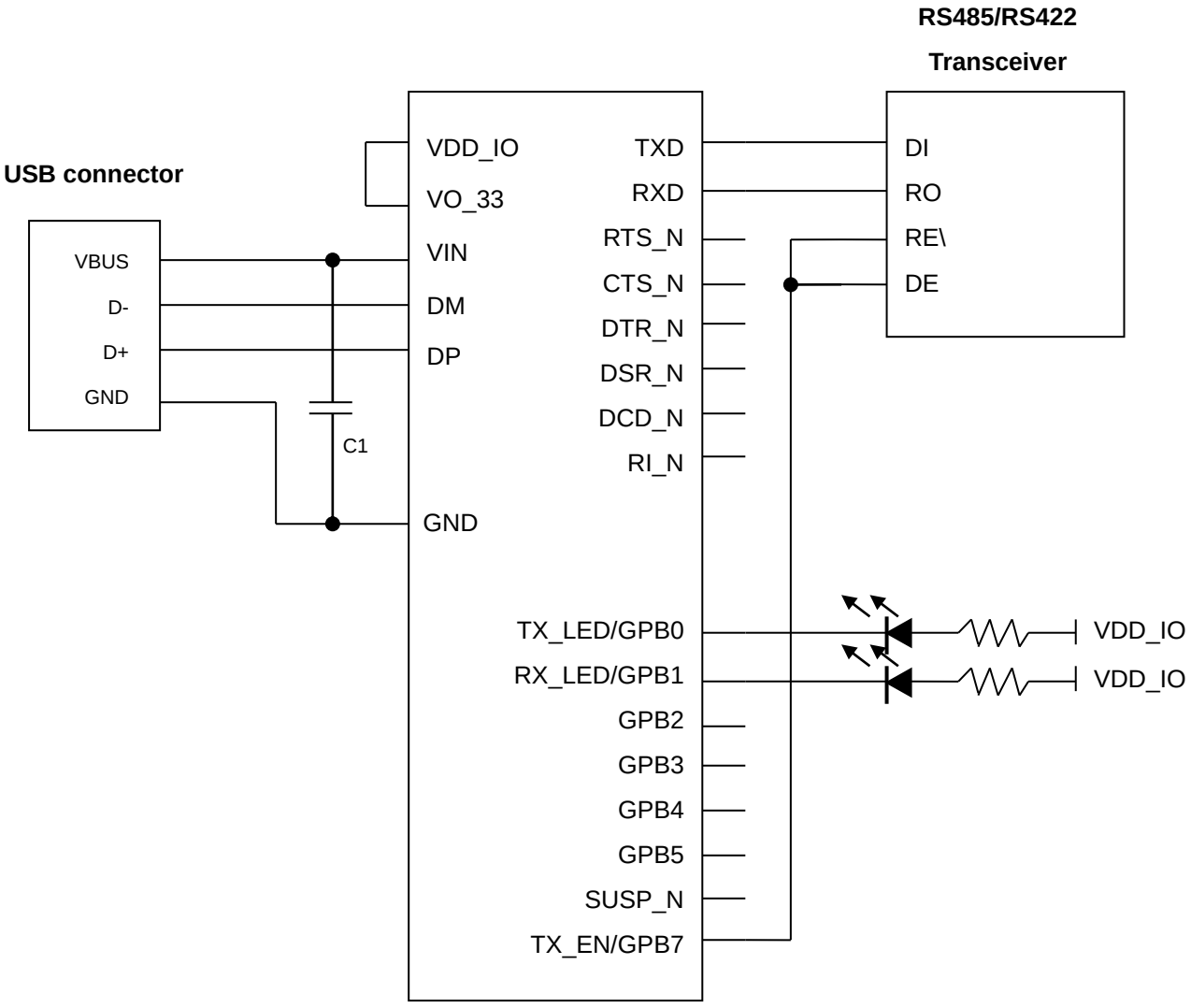


Figure 10-6 USB to RS485/422 Design Example

10.7 Battery Charging Support

The PL2303GC supports USB battery charging specification (BC1.2) where in battery charging controller can use signals from PL2303GC to control the charging current. An example of charging control concept is shown in below diagram.

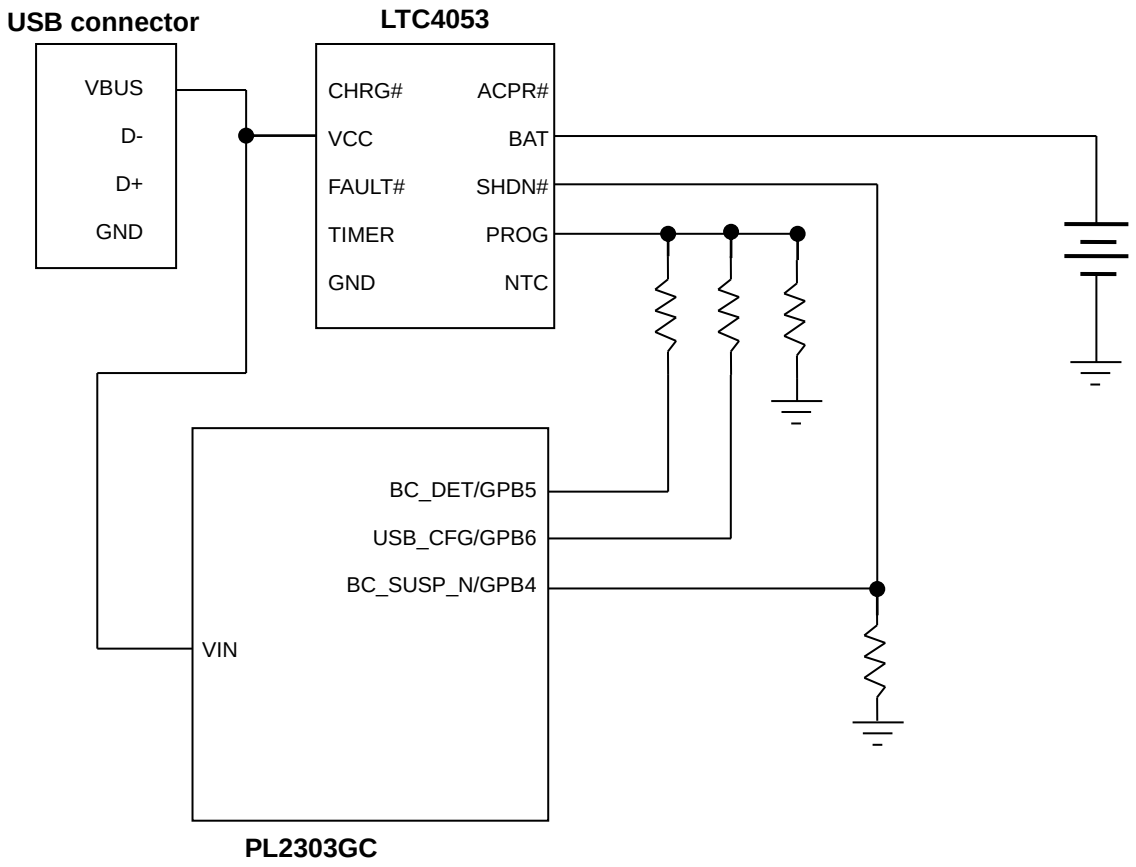


Figure 10-7a Battery Charging Design Example #1

This concept diagram uses the GPB5 GPIO pin configured as BC_DET (battery charge detect pin) signal and this pin need to set to inverse polarity and open-drain mode. GPB6 GPIO pin is configured as USB_CFG and is also set to inverse polarity and open-drain mode. GPB4 GPIO pin is configured as BC_SUSP_N function and connected to shutdown signal of charging controller. All above signals can achieve charging conditions as below table.

Charging Condition	Charging Current (max)	BC_SUSP_N	USB_CFG	BC_DET
Suspend	2.5mA	0	x	x
Un-configured	100mA	1	1	1
Operation	500mA	1	0	1
Fast Charging	1500mA	1	1	0

Below is another example of charging controller support concept.

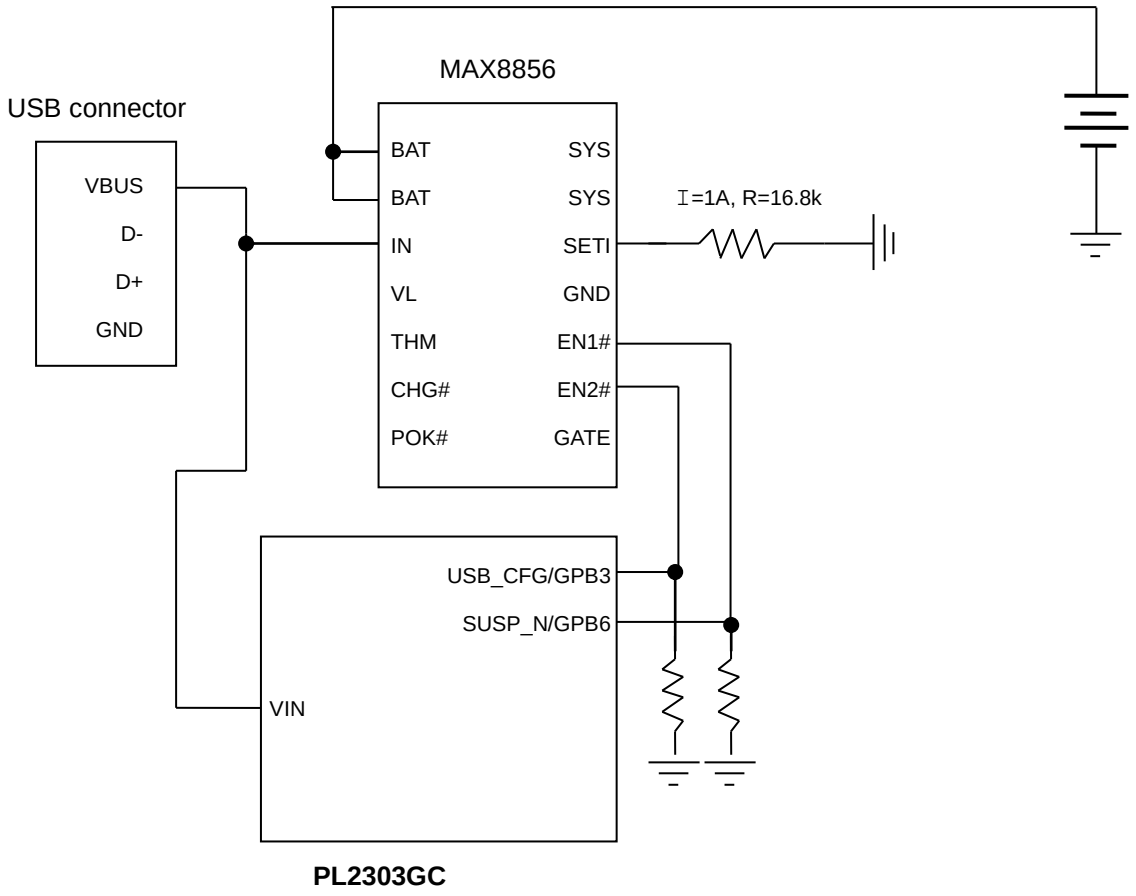


Figure 10-7b Battery Charging Design Example #2

The above concept diagram uses GPB3 pin as USB_CFG and set to normal polarity and push-pull I/O mode as default. GPB6 pin is configured as SUSP_N and set to inverse polarity and push-pull IO mode. The SUSP_N option is also set active during USB bus suspend state only, and not when USB is not configured. This concept diagram can achieve charging conditions as below table.

Charging Condition	Charging Current (max)	SUSP_N	USB_CFG
Suspend	2.5mA	1	1
Un-configured	100mA	0	0
Operation	500mA	0	1
Fast Charging	1000mA	1	0

10.8 External I2C EEPROM Support

The PL2303GC can also support an external I2C EEPROM to override the OTPROM settings. To use an external EEPROM, it needs to program the OTPROM to enable the external I2C EEPROM support. There are two options, one is to use the GPB2 pin as I2C SDA and the GPB3 pin as I2C SCL; the other option is to use GPA4(DTR_N) pin as I2C SDA and GPA5(DSR_N) pin as I2C SCL.

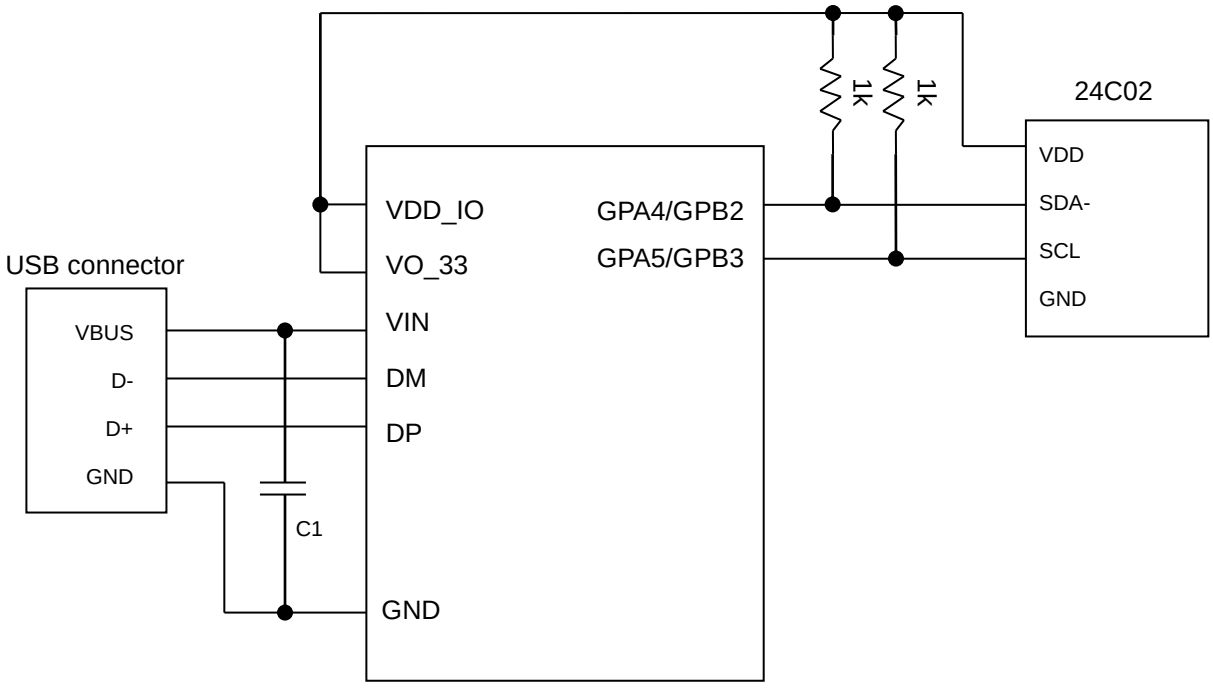


Figure 10-8 External I2C EEPROM Design Example

There is signature field in external EEPROM space. When this field content is valid, the PL2303GC will load the external EEPROM contents and override the settings defined in the OTPROM. Detailed information can be checked with OTPROM and EEPROM software programming tool. The supported external I2C EEPROM size is 256 bytes.

11. DC & Temperature Characteristics

11.1 Absolute Maximum Ratings

Table 11-1 Absolute Maximum Ratings

Items	Ratings
Power Supply Voltage – VIN	-0.3 to 6.0 V
Input Voltage of VDD_IO	-0.3 to VIN+0.3 V
Input Voltage of I/O pins with 5V Tolerance I/O	-0.3 to 6.0 V
Storage Temperature	-40 to 150 °C
Thermal Resistance (θ jc)	19 °C/W (UQFN24)
Thermal Resistance (θ jc)	31 °C/W (SSOP28)

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. These are stress rating only, and functional operation should be restricted to within the conditions. Exposure to absolute maximum rating conditions for extended periods may affect the device's reliability.

11.2 DC Characteristics

11.2.1 Operating Voltage and Suspend Current

Table 11-2a Operating Voltage and Suspend Current

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	VIN	2.8	5	5.5	V
Power Supply for I/O Pins	VDD_IO	1.8	3.3	VIN+0.3	V
Output Voltage of Regulator	VO_33	2.97	3.3	3.63	V
Operating Current(1) (Power Consumption)	I_{DD}	-	9.5	15	mA
Suspend Current	I_{SUS}	-	250	450	μA

Note: (1) – No device connected.

11.2.2 I/O Pins

Table 11-2b I/O Pins

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (CMOS)					
Low	V_{IL}	--	--	0.4	V
High	V_{IH}	0.7* VDD_IO	--	--	V
Output Voltage					
Low	V_{OL}	--	--	0.4	V
High	V_{OH}	0.7*VDD_IO	--	--	V

11.3 Temperature Characteristics

Table 11-3 Temperature Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature (ambient)	--	-40	--	85	°C
Junction Operation Temperature	T_J	-40	25	125	°C

11.4 Baud Rate Characteristics

Table 11-4 Baud Rate Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Baud rate @ VDD_IO = 5V	--	1	--	12M	bps
Baud rate @ VDD_IO = 3.3V	--	1	--	12M	bps
Baud rate @ VDD_IO = 1.8V	--	1	--	6M	bps

12. Outline Diagram

12.1 SSOP28 Package

Table 12-1 Package Dimension

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
b	0.22		0.38	0.009		0.015
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
L	0.55	0.75	0.95	0.021	0.030	0.037
R1	0.09			0.004		
D	9.9	10.2	10.5	0.390	0.402	0.413
A			2.0			0.079
e		0.65			0.0256	
L1		1.25			0.050	
A1	0.05			0.020		
A2	1.65	1.75	1.85	0.065	0.069	0.073

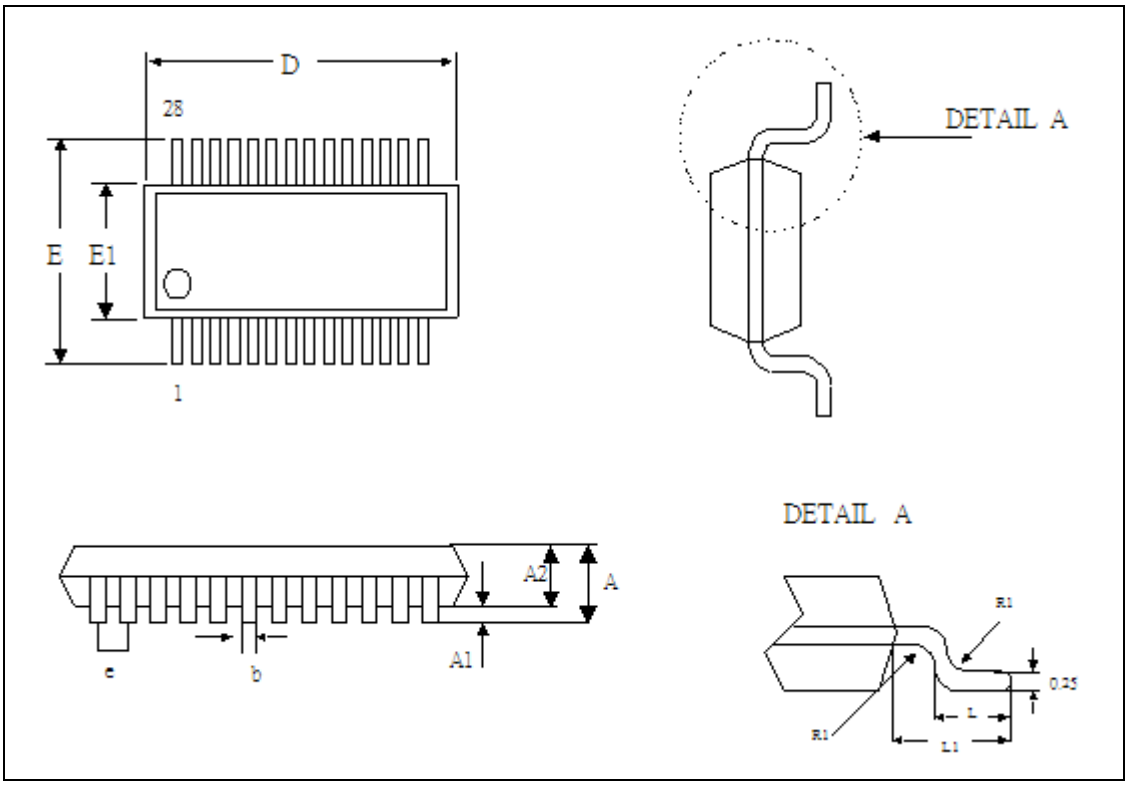
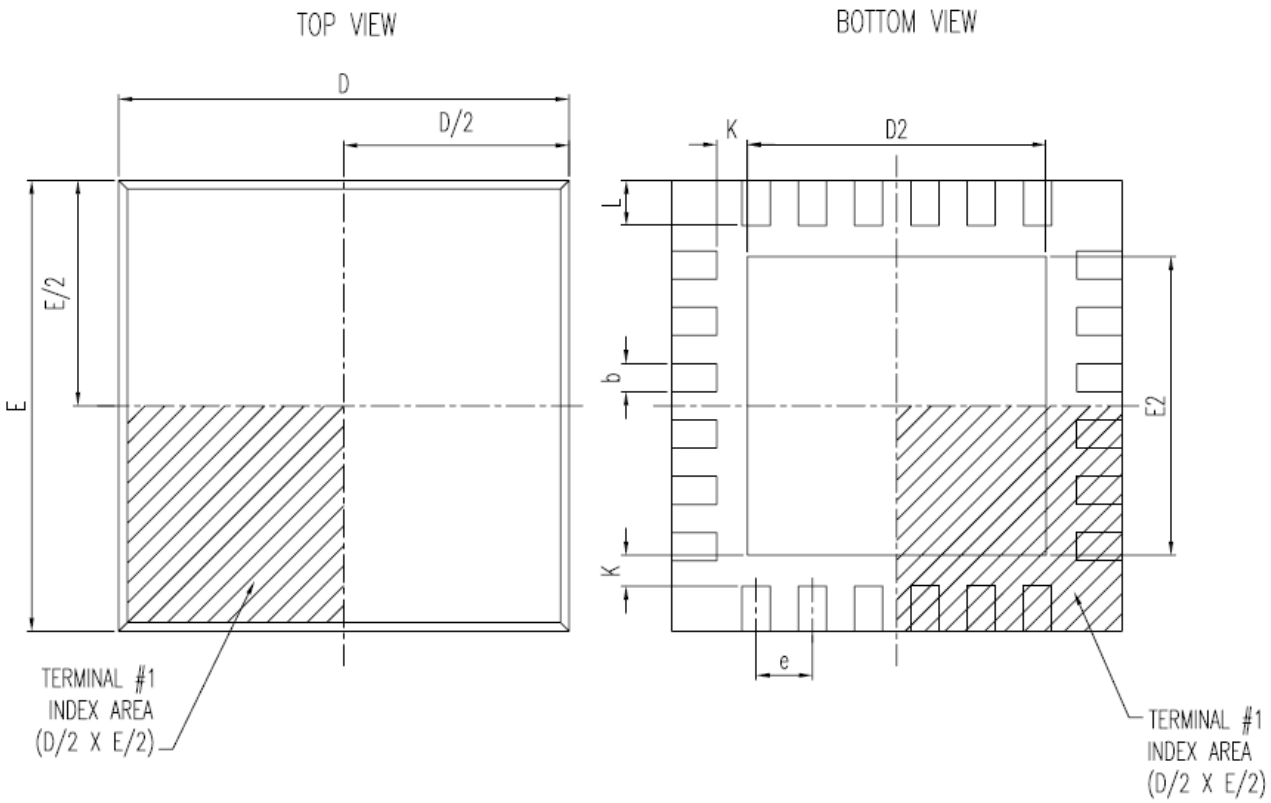
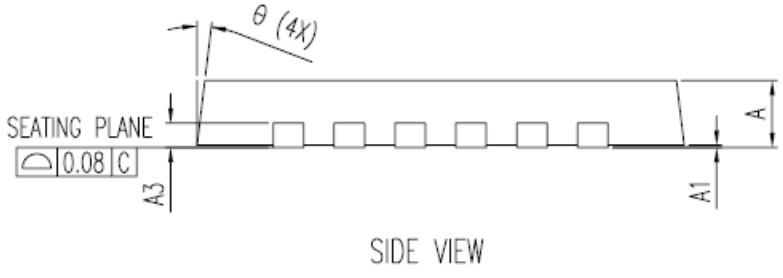


Figure 12-1 PL2303GC Outline Diagram (SSOP28)

12.2 UQFN24 Package





SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.20 REF.	
D		4.00 BASIC	
D2	2.50	2.65	2.80
E		4.00 BASIC	
E2	2.50	2.65	2.80
e		0.50 BASIC	
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20		
θ	0°		14°
JEDEC	MO-220 (Variation VGGD-6)		

Figure 12-2 PL2303GC Outline Diagram (UQFN24) 4 x 4 mm

13. Packing Information

13.1 Carrier Tape (SSOP-28)

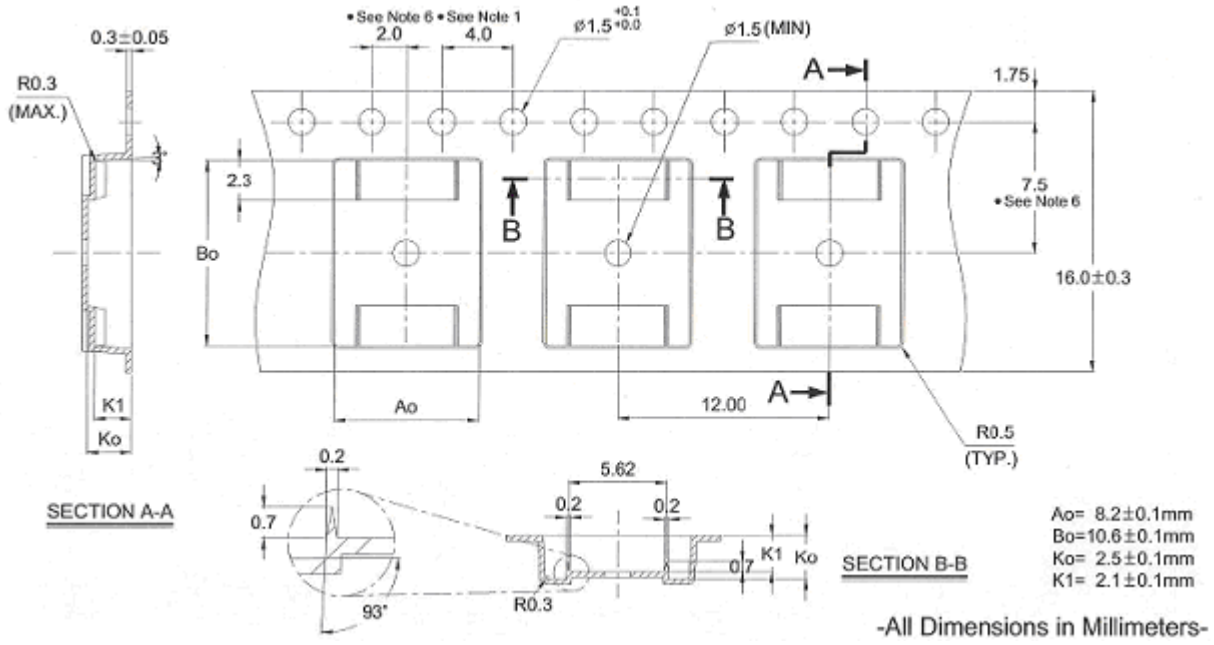


Figure 13-1a SSOP28 Carrier Tape

Notes:

- 10 sprocket hole pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm in 100mm.
- Material: Black Polystyrene.
- A_o and B_o measured on a plane 0.3mm above the bottom of the pocket.
- K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
- IC quantity per one reel: 2,000 pieces (MOQ)

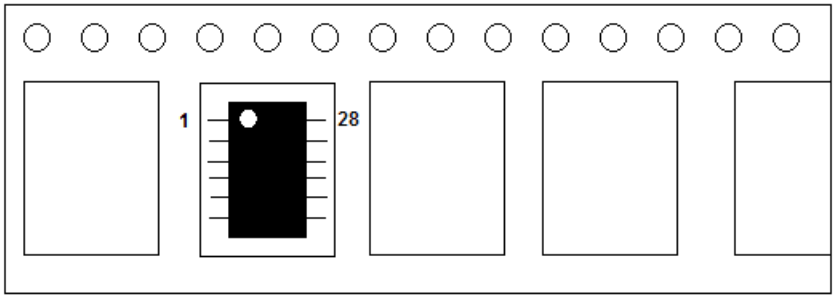
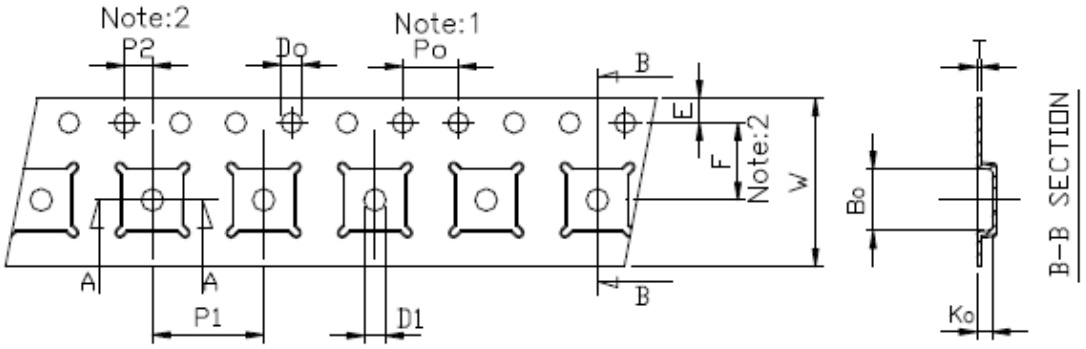
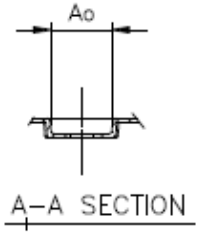


Figure 13-1b IC Reel Placements

13.2 Carrier Tape (UQFN24)





Ao= 4.35±0.10 mm
Bo= 4.35±0.10 mm
Ko= 1.10±0.10 mm

Unit: mm

Symbol	Spec.
Po	4.0±0.10
P1	8.0±0.10
P2	2.0±0.05
Do	1.55±0.05
D1	1.50(MIN)
E	1.75±0.10
F	5.50±0.05
10Po	40.0±0.10
W	12.0±0.20
T	0.30±0.05

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.1mm
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

Figure 13-2 UQFN24 Carrier Tape

13.3 Reel Dimension

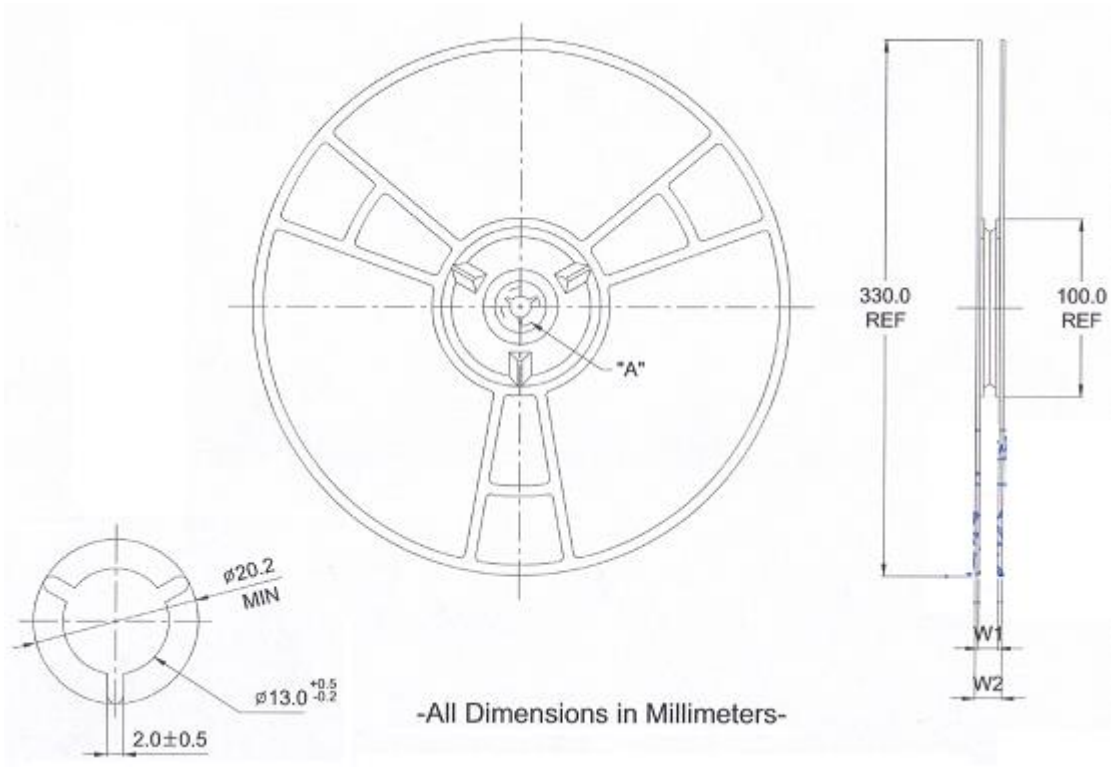


Figure 13-3 Reel Dimension

Table 13-1 Reel Part Number Information

Package	Part Number	Normal Hub Width	W1 +0.3mm -0.2mm	W2 Max
UQFN24	RD33008SW-T + RD33004SW-T	12mm	12.8mm	18.2mm
SSOP28	RD33008SW-T + RD33008SW-T	16mm	16.8mm	22.2mm

13.4 Tube Packing

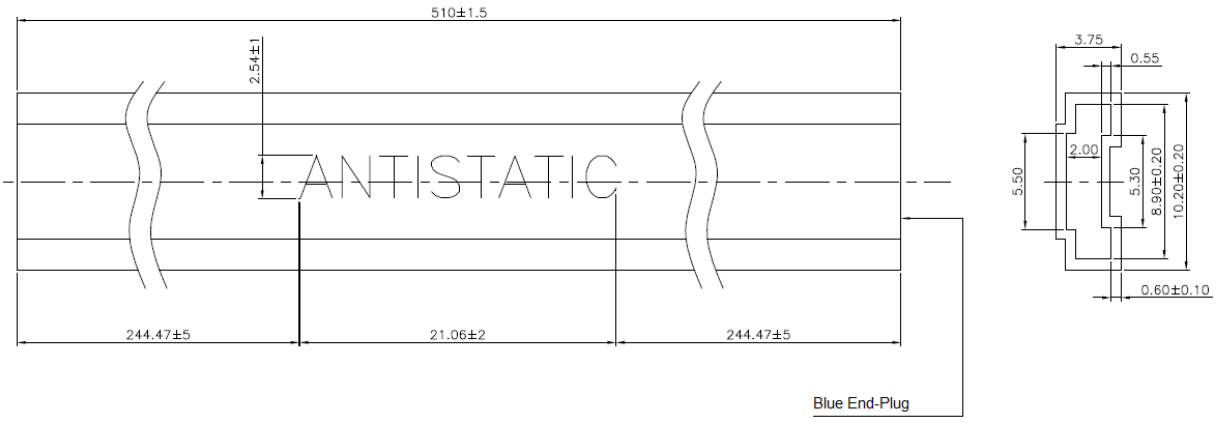


Figure 13-4 Tube Packing Dimension

REMARK :

1.TUBE MT'L : PVC,COATING WITH ANTISTATIE LIQUID.
2.COLOR : TUBE - TRANSPARENT ; MARK - BLUE
3.SURFACE RESISTANCE : 10^{8} ~10^{11} • /□
4.NO BURR AT CUTTING AREA.
5.THE TUBE SHALL WITH BLUE END-PLUG(3088-060-01681) FROM VENDOR, TAIL DOWNWARD AND THE OTHER ONE ENCLOSE TOGETHER WITH SHIPMENT.

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