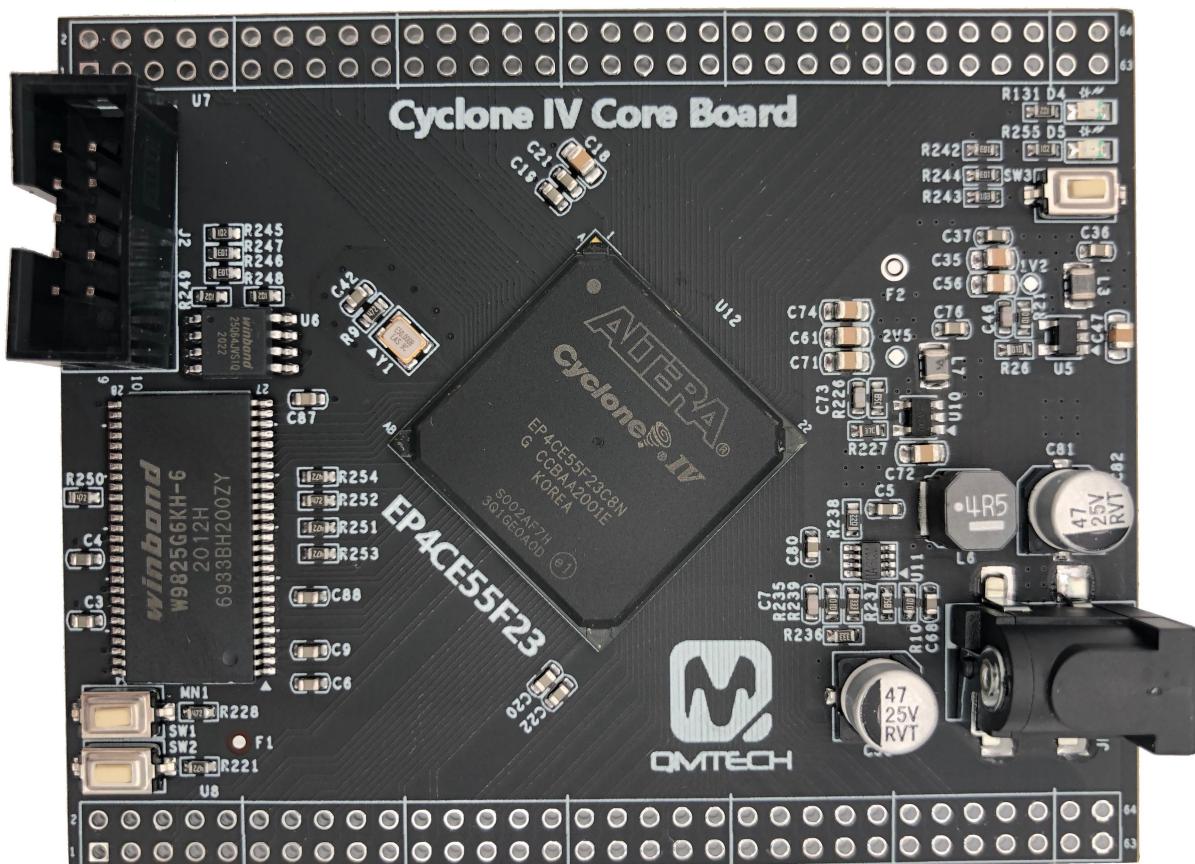


# CYCLONE IV EP4CE55 CORE BOARD

## USER MANUAL(QUARTUS 15.1)



### Preface

The QMTech® Cyclone IV Core Board uses Intel(Altera) EP4CE55F23 device to demonstrate Intel's leadership in offering power-efficient FPGAs. With enhanced architecture and silicon, advanced semiconductor process technology, and power management tools, power consumption for Cyclone IV FPGAs has been reduced by up to 25 percent compared to Cyclone® III FPGAs. The result is the lowest power consumption of any comparable FPGA.

## Table of Contents

---

1. QUARTUS PRIME 15.1 INSTALLATION.....	3
2. FPGA PROJECT COMPILE AND *.SOF DOWNLOAD.....	7
2.1 CREATE NEW PROJECT.....	7
2.2 COMPILE THE PROJECT.....	13
2.3 PIN ASSIGNMENT.....	14
2.4 DOWNLOAD *.SOF INTO FPGA.....	16
2.5 DOWNLOAD *.JIC INTO SPI FLASH.....	19
3. SignalTap II LOGIC ANALYZER.....	23
4. REFERENCE.....	27
5. REVISION.....	28

上海勤谋电子科技有限公司



QMTECH

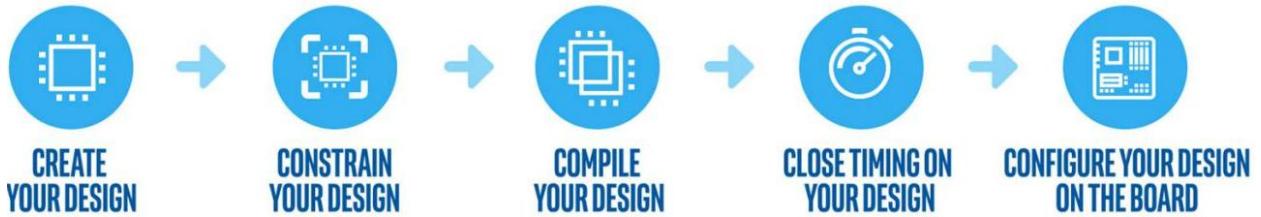
Cyclone IV EP4CE55 Core Board

User Manual-V01

## 1. Quartus Prime 15.1 Installation

The revolutionary Intel® Quartus® Prime Design Software includes everything you need to design for Intel® FPGAs, SoCs, and CPLDs from design entry and synthesis to optimization, verification, and simulation. Dramatically increased capabilities on devices with multi-million logic elements are providing designers with the ideal platform to meet next-generation design opportunities.

The Intel® Quartus® Prime Software design flow comprises of the following high-level steps:



The Quartus Prime software version 15.1 supports the following device families: Stratix IV, Stratix V, Arria II, Arria V, Arria V GZ, Arria 10, Cyclone IV, Cyclone V, MAX II, MAX V, and MAX 10 FPGA. Below image shows the startup UI of Quartus II Prime 15.1:

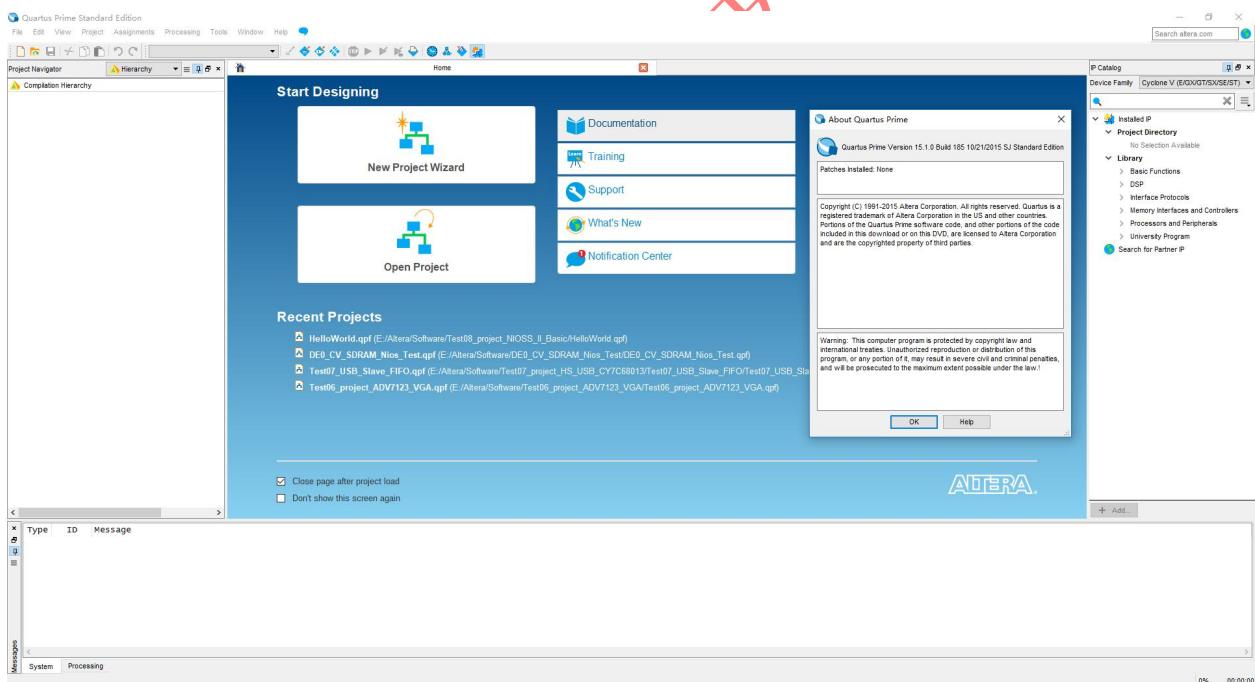


Figure 1-1. Quartus II Prime 15.1

After the Quartus II Prime 15.1 is correctly installed, users still need to install the device package from Intel official website. Below lists the download center address:

<https://www.intel.com/content/www/us/en/programmable/downloads/download-center.html>

In the Intel Download Center website, select the tab of ‘Select by Device’ and then all the available device packages will be listed as below image. The device used in this user manual is Cyclone IV E series and the detailed chip part number is EP4CE55F23C8N, so please download the device package for Quartus II 15.1: cyclone-15.1.0.185.qdz.

## Software Selector

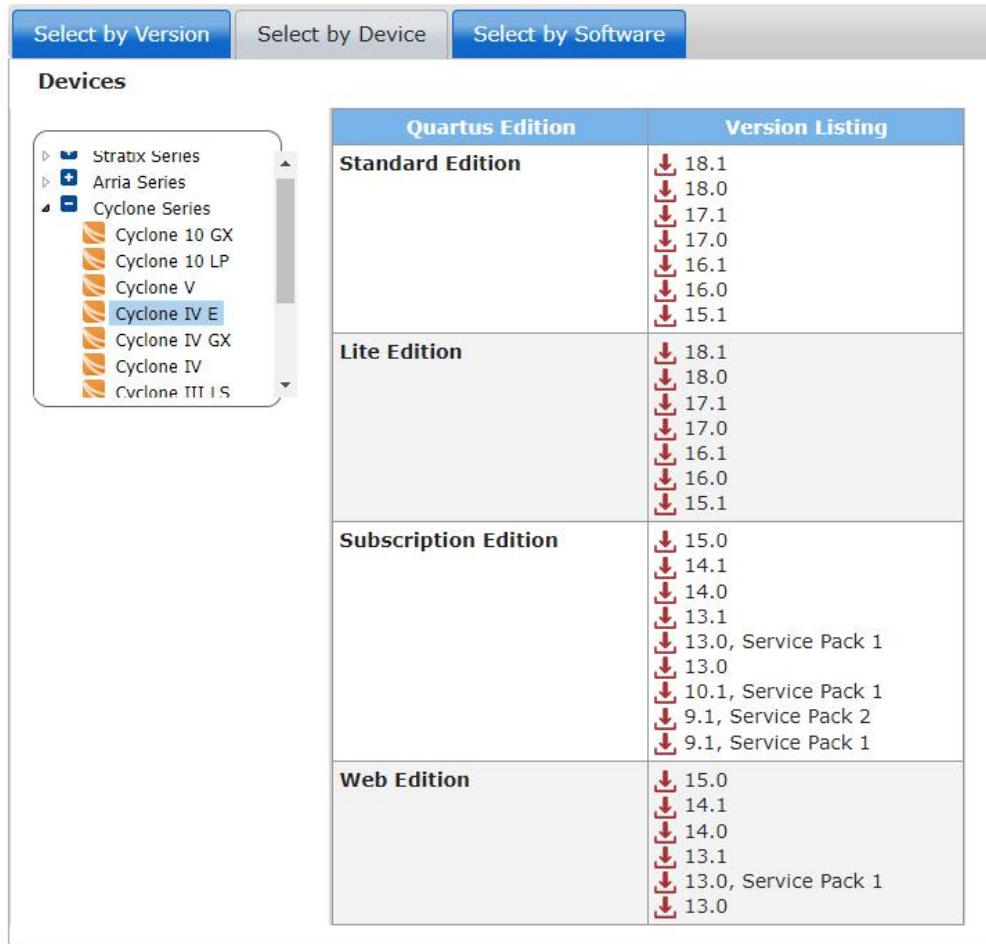


Figure 1-2. Download Device Package

Open Quartus II 15.1, Click Tools → Install Device and then select the downloaded device package:

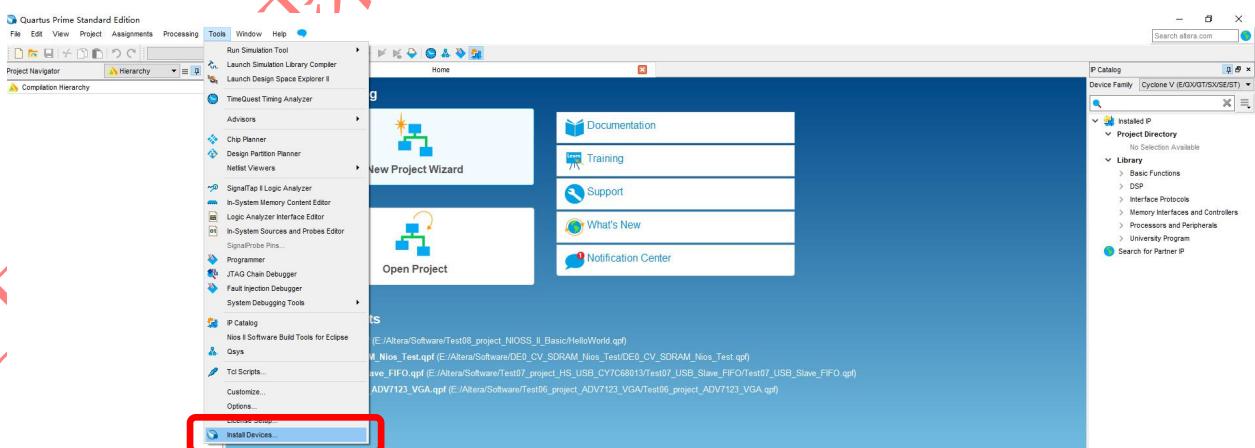
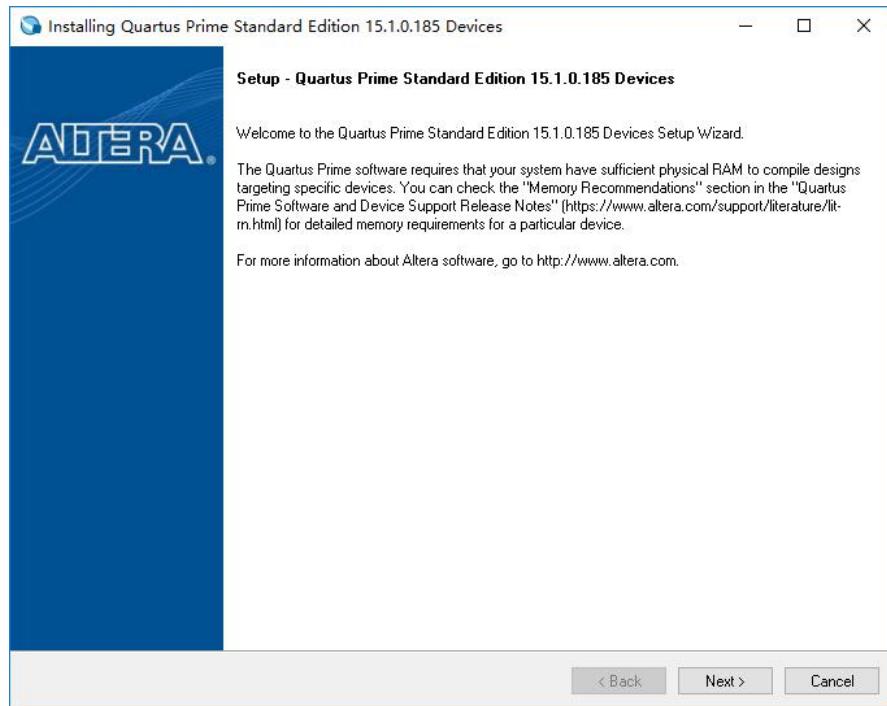


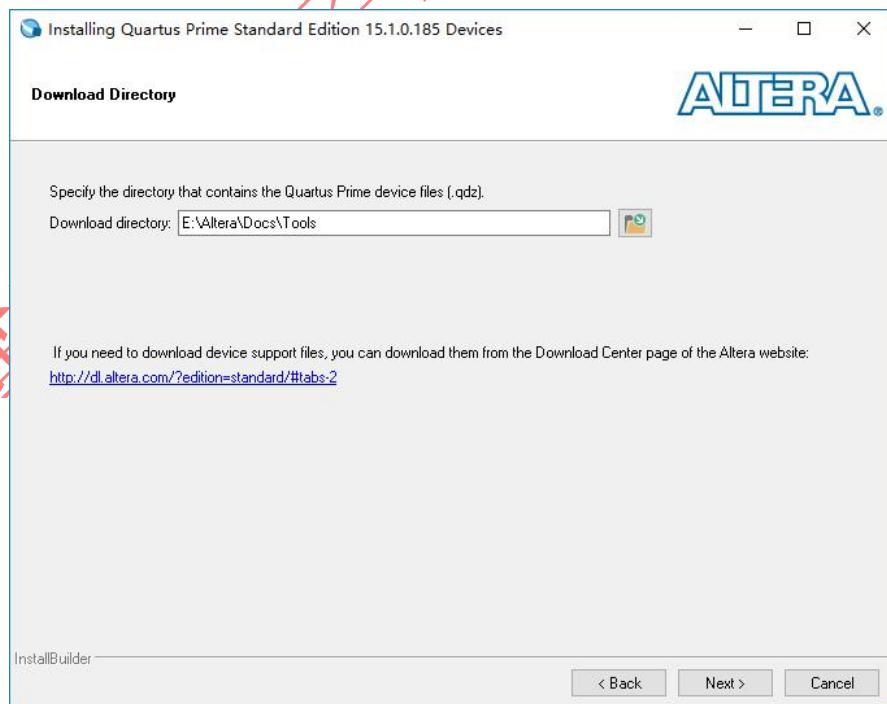
Figure 1-3. Install Device Package

Below window will pop up and click Next:



**Figure 1-4. Install Device Package**

Choose the Download Directory where contains the cyclone-15.1.0.185.qdz file:



**Figure 1-5. Choose Device Package**

Choose the device package needs to be installed and click Next:

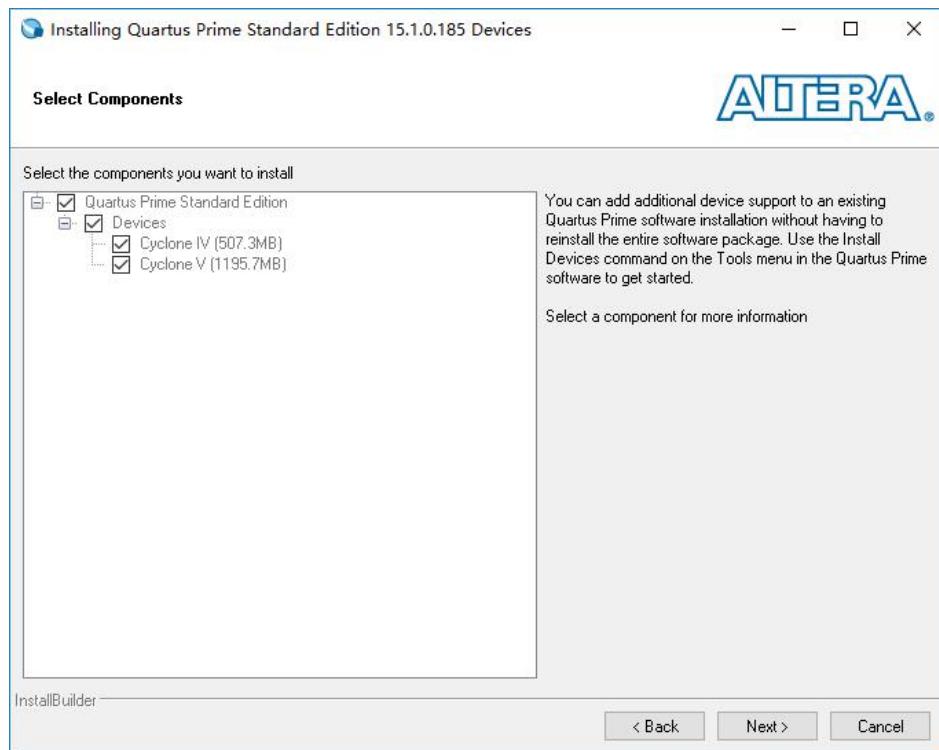


Figure 1-6. Install the Device Package

User could also install the device package by using Quartus II Prime 15.1 Device Installer directly:

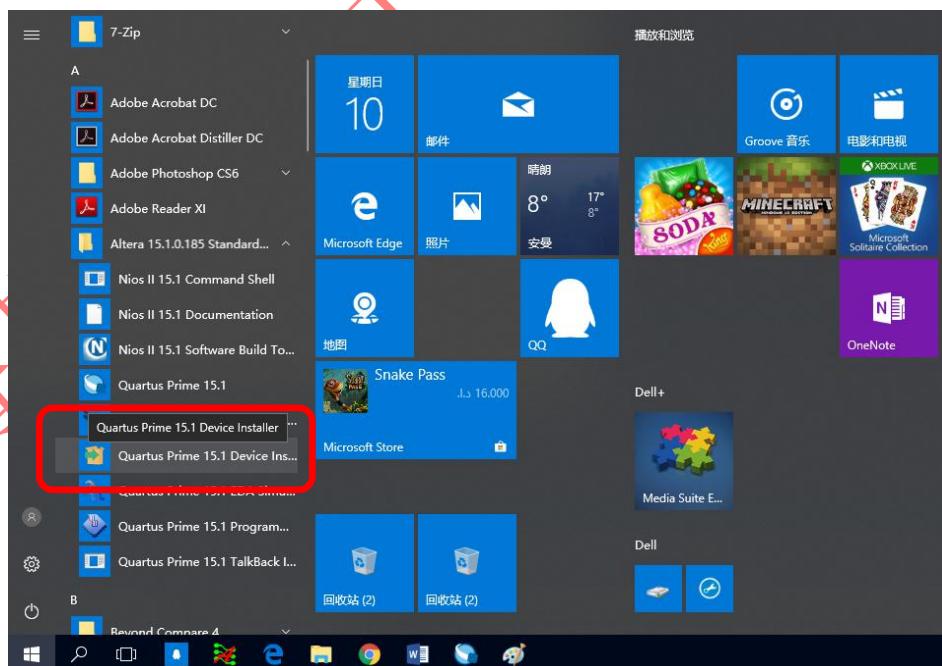


Figure 1-7. Device Installer



QMTECH

Cyclone IV EP4CE55 Core Board

User Manual-V01

## 2. FPGA Project Compile and \*.sof Download

### 2.1 Create New Project

Click 【File】→【New Project Wizard...】 to create a new project:

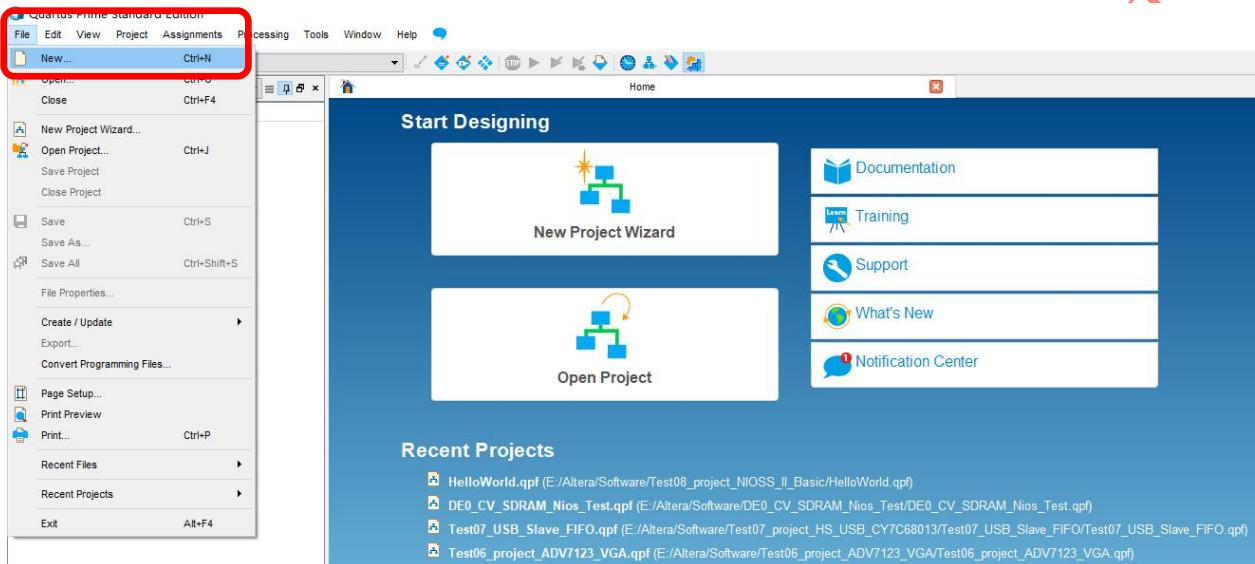


Figure 2-1. Create New Project

Choose 【New Quartus Prime Project】:

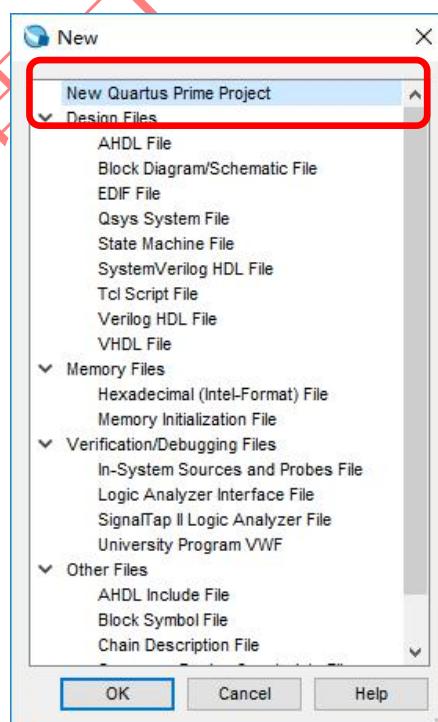
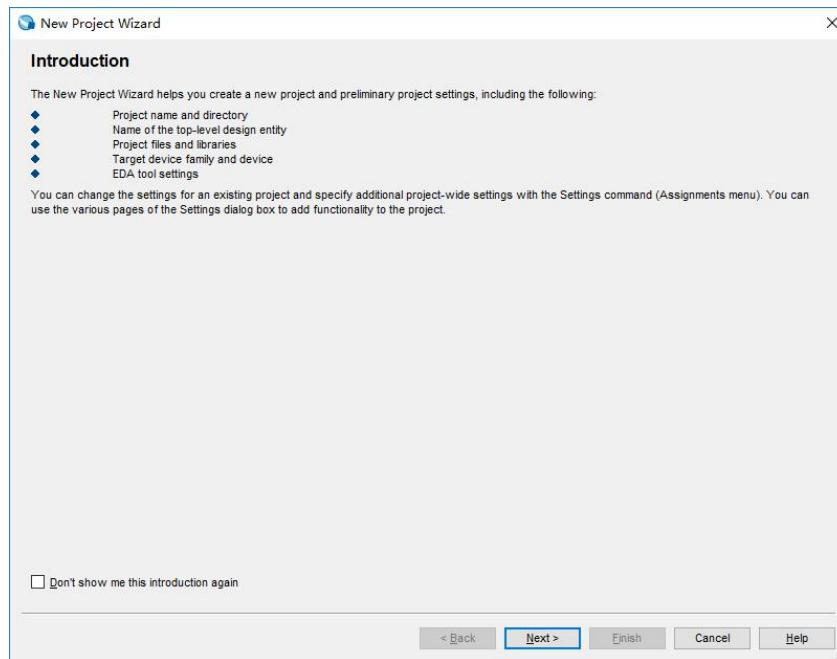


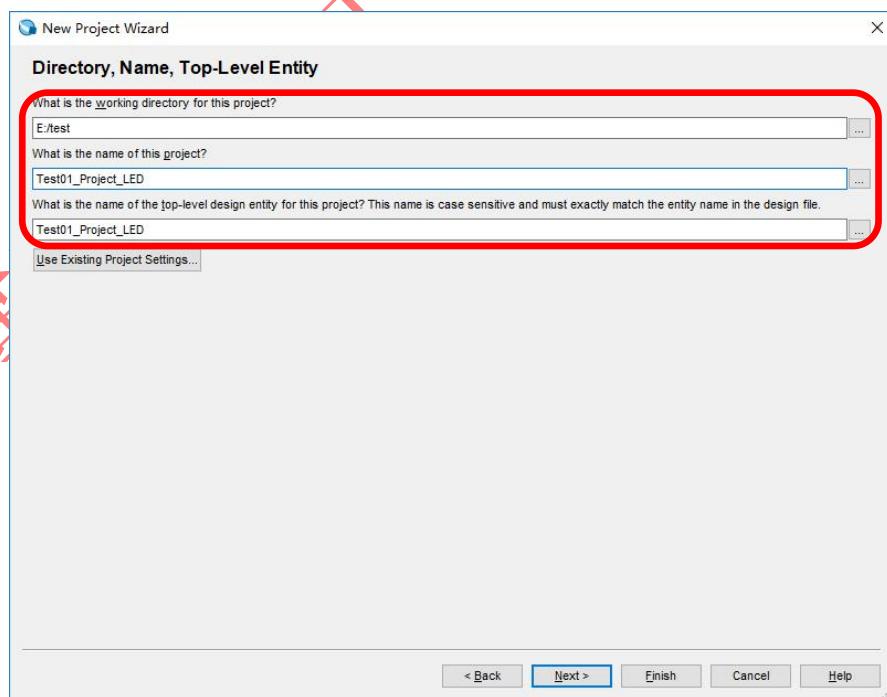
Figure 2-2. New Quartus Prime Project

In below 【New Project Wizard】 page, choose Next:



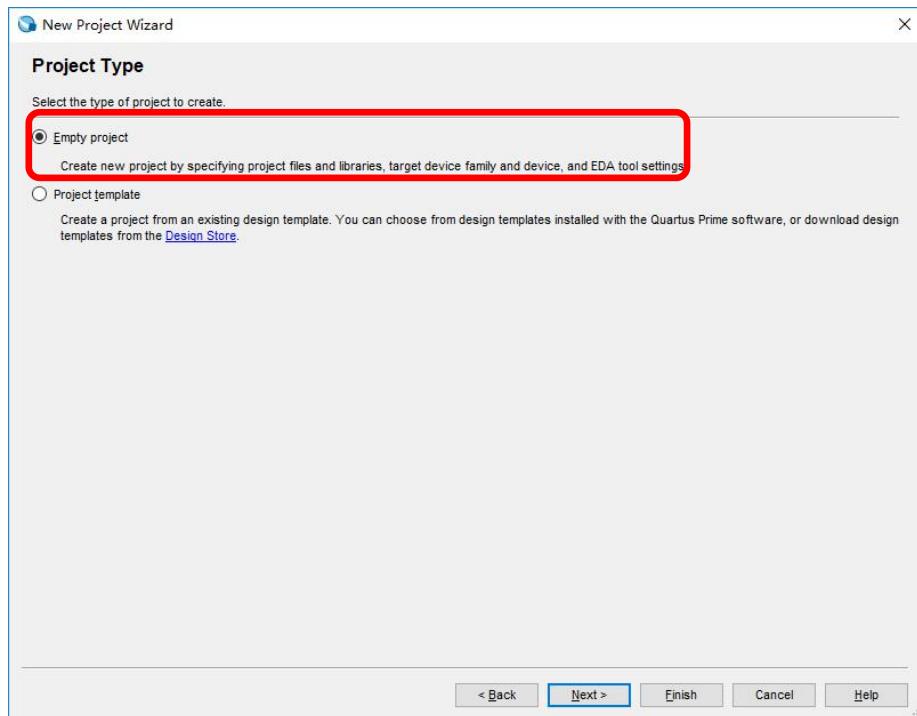
**Figure 2-3. New Project Wizard**

Set the target working folder below 【What is the working directory for this project?】 . Set the new project name below 【What is the name of this project?】 . And finally set the example project name: Test01\_Project\_LED shown as below.



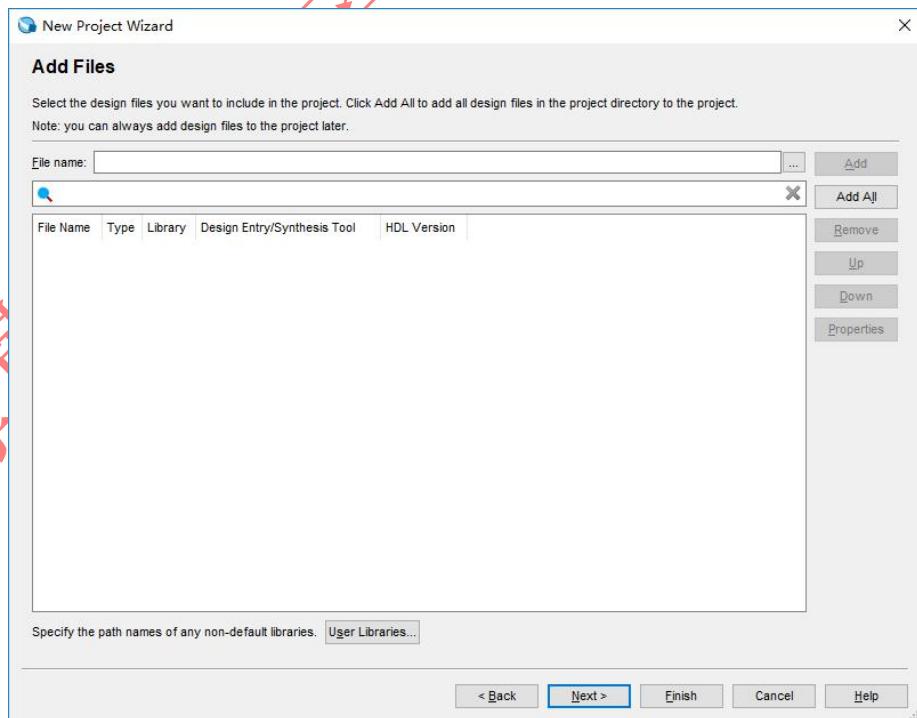
**Figure 2-4. Set Working Directory and Project Name**

Select 【Empty Project】 and then click Next:



**Figure 2-5. Create Empty Project**

If user already has some source code, please add all these necessary files in this step:



**Figure 2-6. Add Source Code**

Choose the FPGA Chip number: EP4CE55F23C8N.

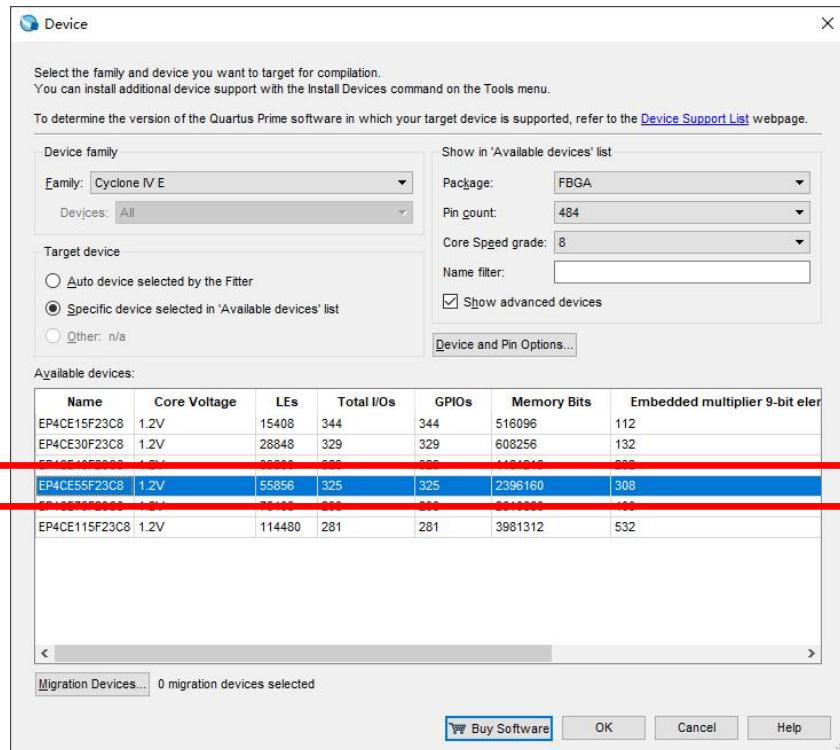


Figure 2-7. Select Device

Summary page will be shown and click **【Finish】** if there's nothing needs to be changed:

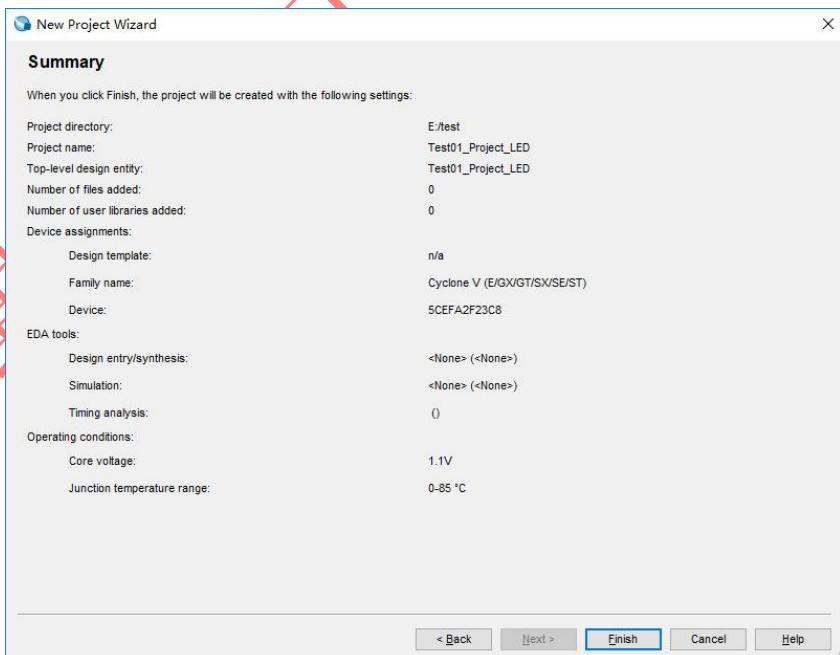


Figure 2-8. Project Summary Page

After the Empty Project created, below image will be shown:

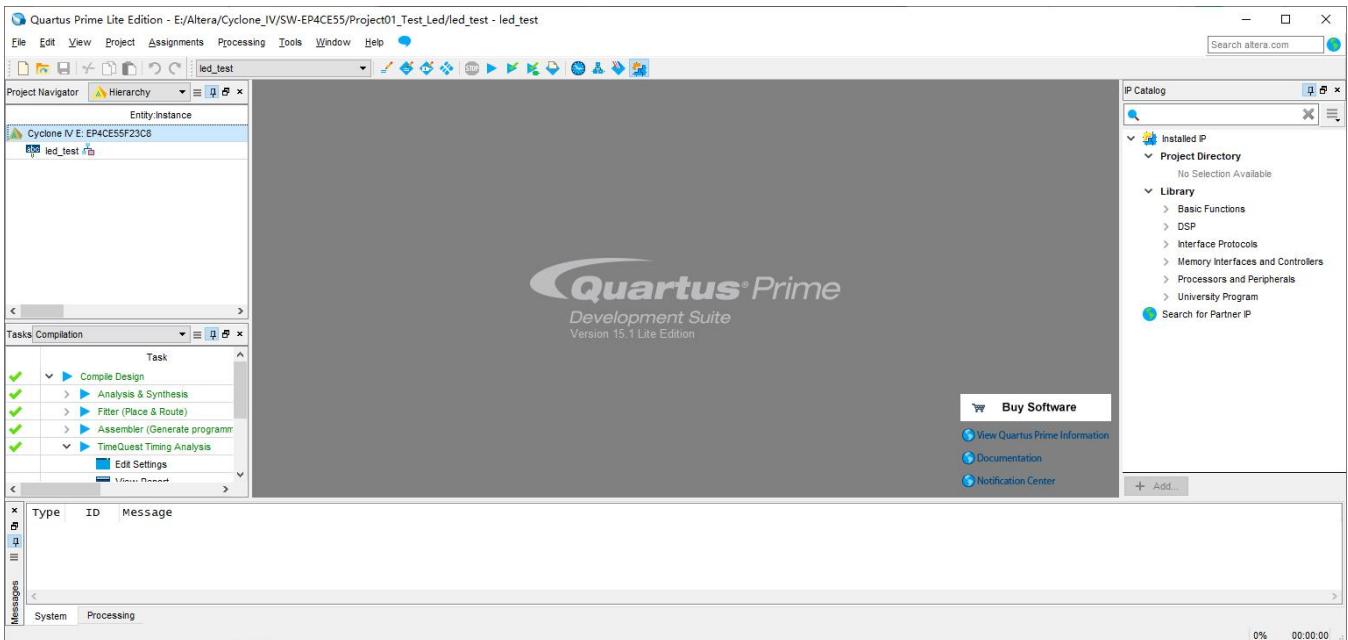


Figure 2-9. Empty Project

Users may add example source file Test01\_Project\_LED.v into this Empty Project shown as below:

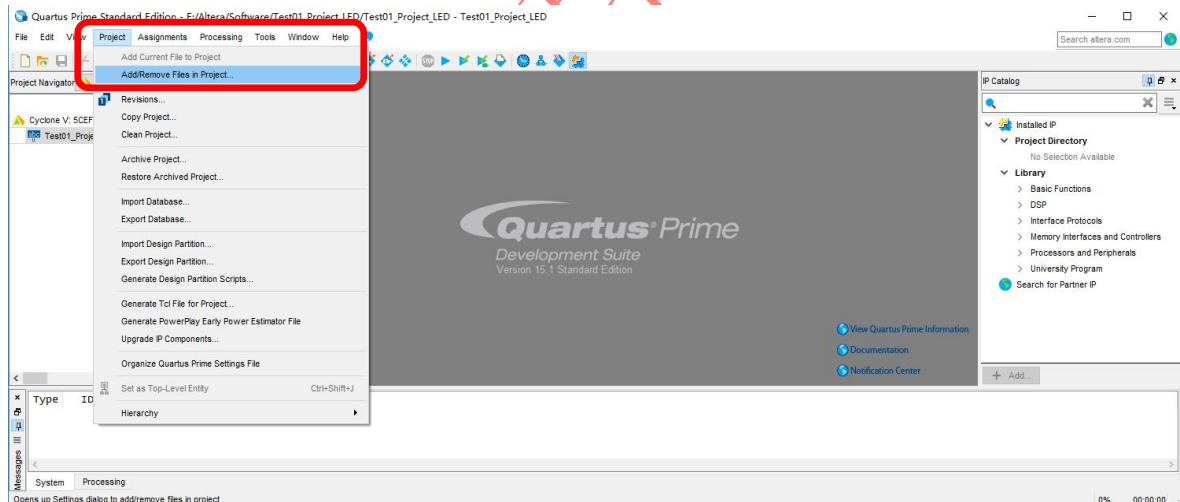
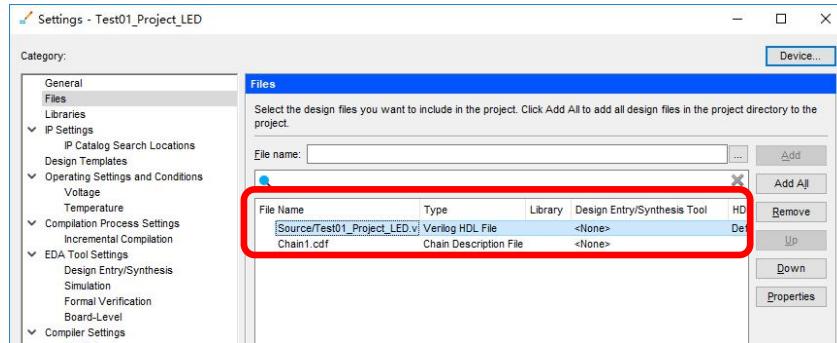


Figure 2-10. Add Source File



**Figure 2-11. Add Source File**

After the newly added source file loaded into project, user can view the source code shown as below:

```

1 //timescale 1ns /1ps
2
3 module led_test (
4     input  clk,
5     input  rst_n,
6     output led
7 );
8
9 //PORT declarations
10
11 input clk;
12 input rst_n;
13 output led;
14
15 //寄存器定义
16 reg [31:0] timer;
17 reg led;
18
19
20
21
22 //计数器计数:循环计数0~2秒
23
24 always @(posedge clk or negedge rst_n) //检测时钟的上升沿和复位的下降沿
25 begin
26     if (~rst_n) //复位信号有效
27         timer <= 0; //计数器清零
28     else if (timer == 32'd99_999_999) //开发板使用的晶振为50MHz, 2秒计数(50M*2-1=99_999_999)
29         timer <= 0; //计数器清零
30     else
31         timer <= timer + 1'b1; //计数器加1
32 end
33
34
35 //LED灯控制
36
37 always @(posedge clk or negedge rst_n) //检测时钟的上升沿和复位的下降沿
38 begin
39     if (~rst_n) //复位信号有效
40         led <= 1'b0; //LED灯灭
41     else if (timer == 32'd49_999_999) //计数器计到1秒,
42         led <= 1'b1; //LED点亮
43     else if (timer == 32'd99_999_999) //计数器计到2秒,
44         led <= 1'b0; //LED熄灭
45 end
46
47
48 endmodule

```

**Figure 2-12. View of Source Code**

## 2.2 Compile the Project

Users could use the button 【Start Compilation – Ctrl + L】 shown in below image to compile the project:

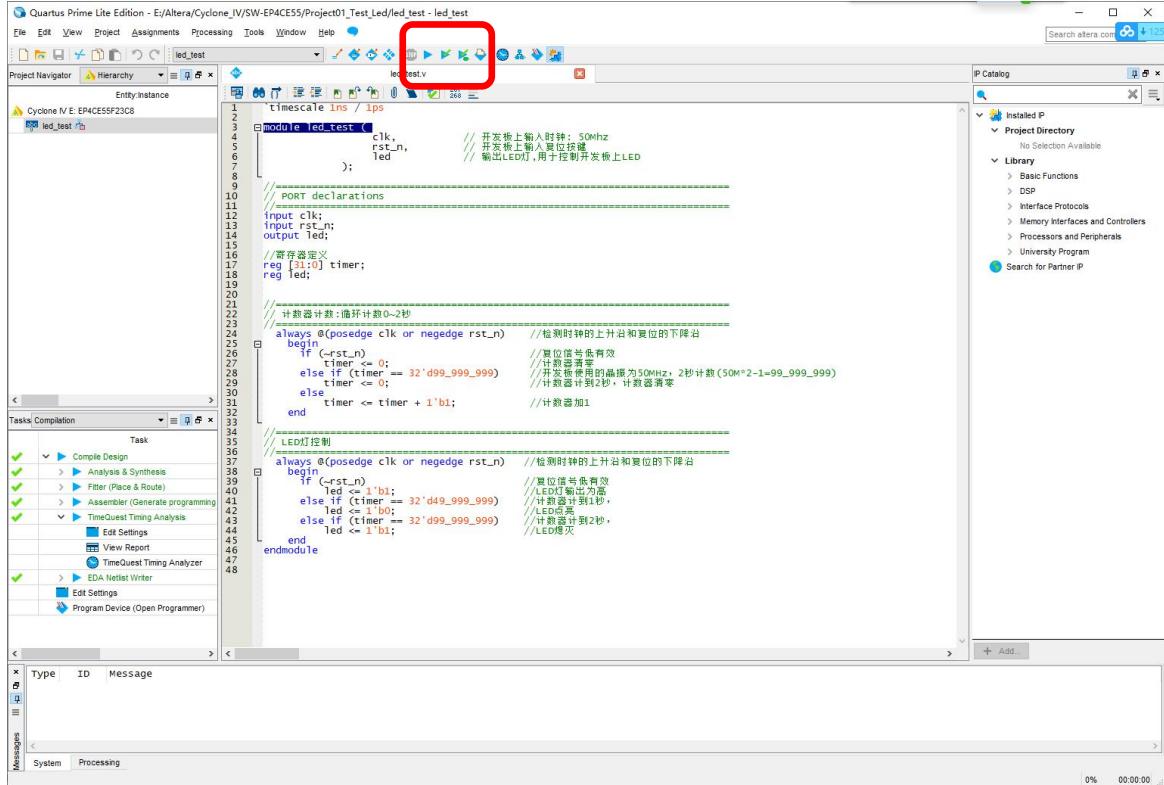


Figure 2-13. Compilation

There will be compilation report after the compile finished, in which shows the info like logical element resource usage, how many PLLs are used, etc. Below image shows an example Compilation Report:

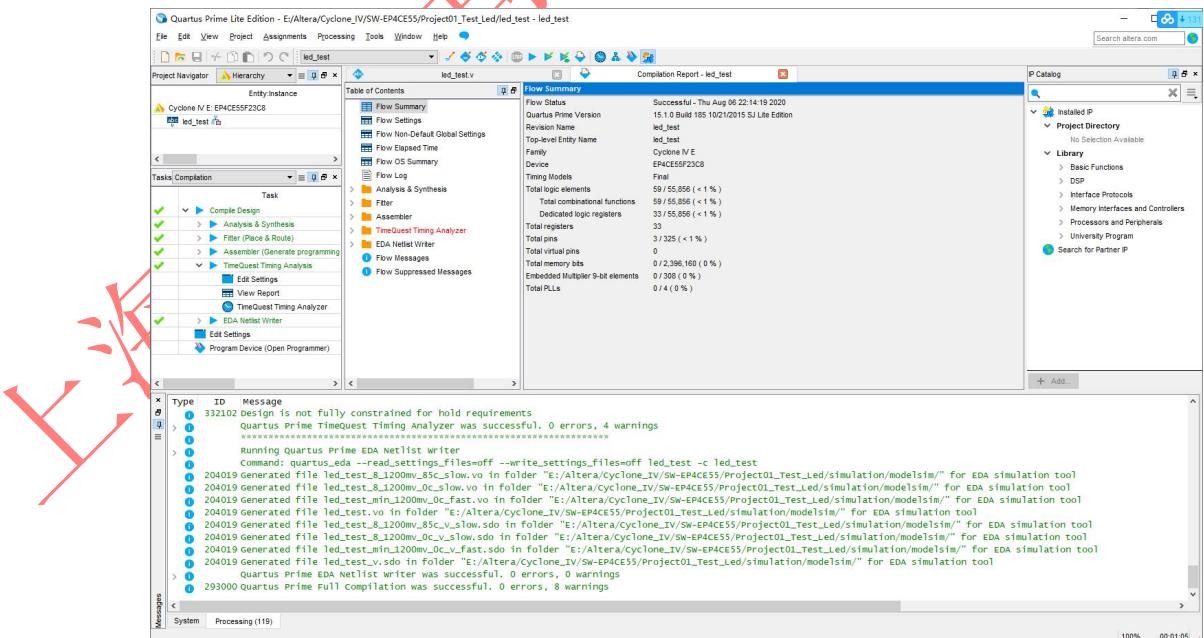
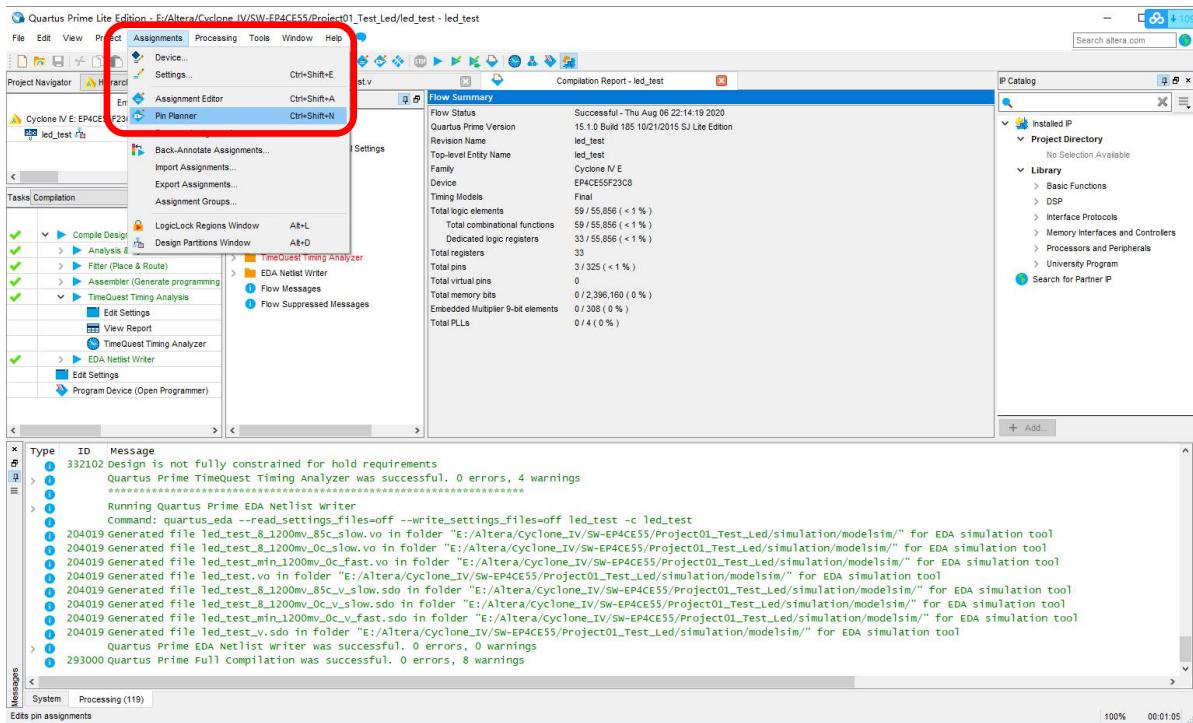


Figure 2-14. Compilation Report

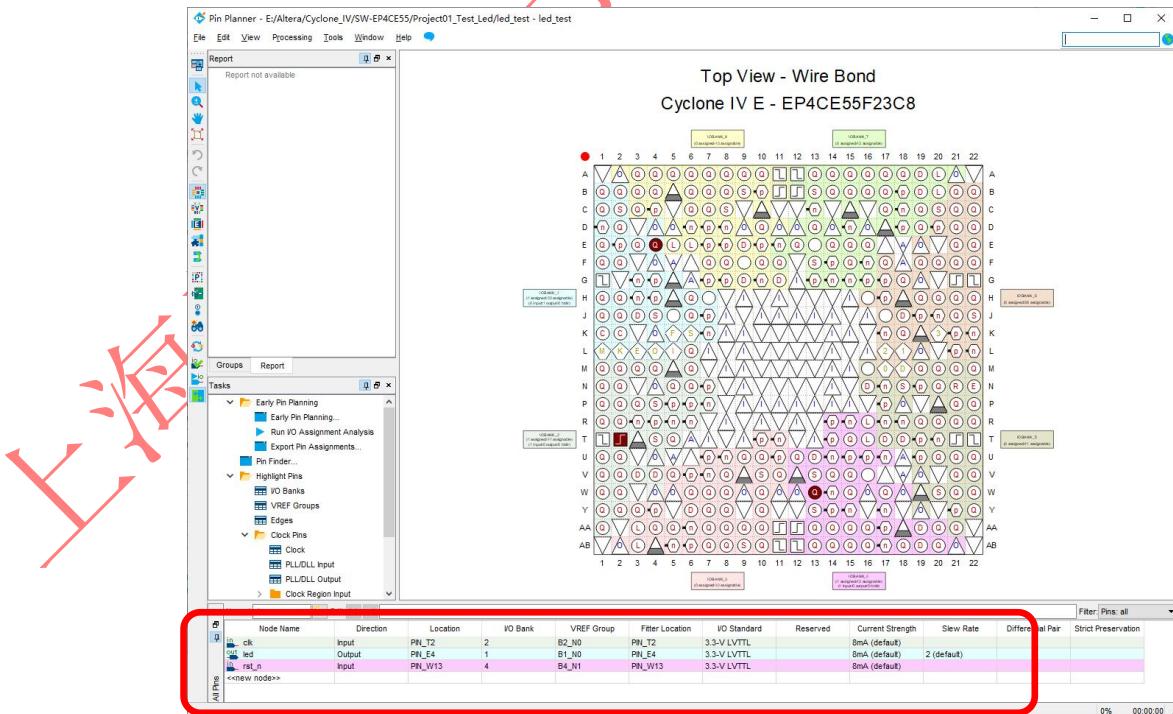
## 2.3 PIN Assignment

There are several ways to assign the Pins for the example project. Method 1: Choose 【Assignment】→【Pin Planner】:



**Figure 2-15. Pin Planner**

Below image shows PIN settings for this test example:



**Figure 2-16. PIN Assignment**

Method 2: Prepare a \*.csv file from other project, then use 【Assignment】 → 【Import Assignment】 to import the existing \*.csv file to allocate the Pin assignment:

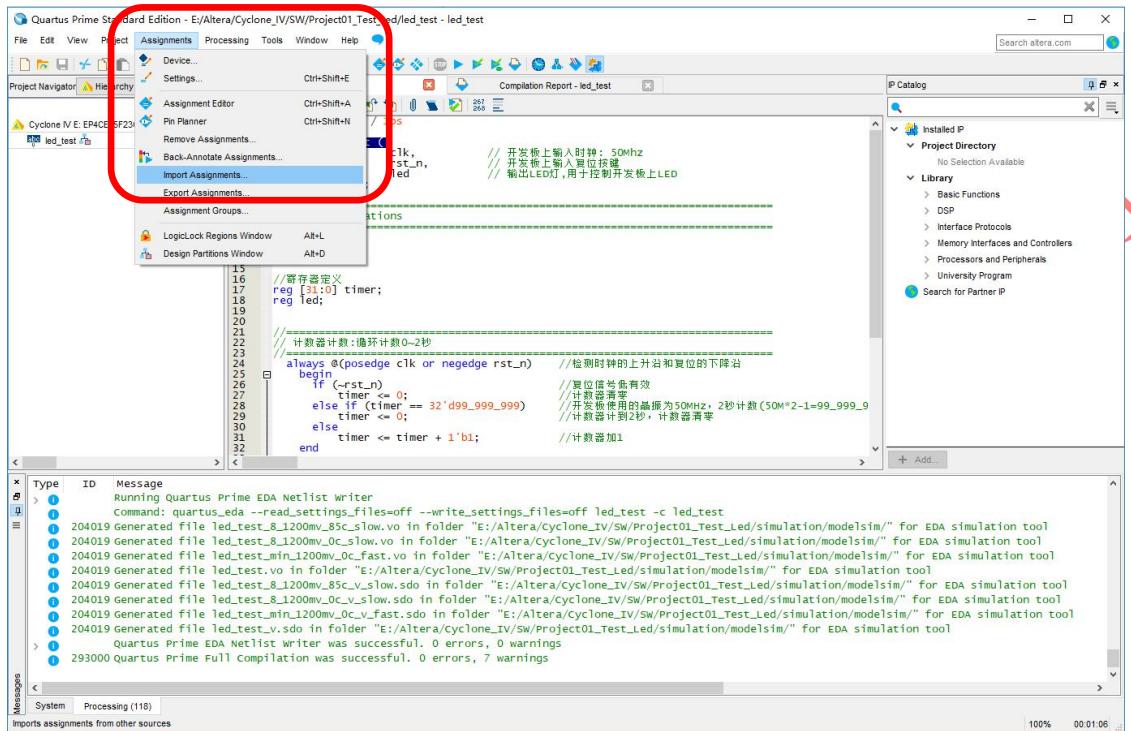


Figure 2-17. Import Assignment

## 2.4 Download \*.sof into FPGA

After the test example correctly compiled, the Quartus will generate a \*.sof file which could be directly loaded into FPGA to check whether implemented functions perform as expected. User could use 【Tools】 → 【Programmer】 to start a new download:

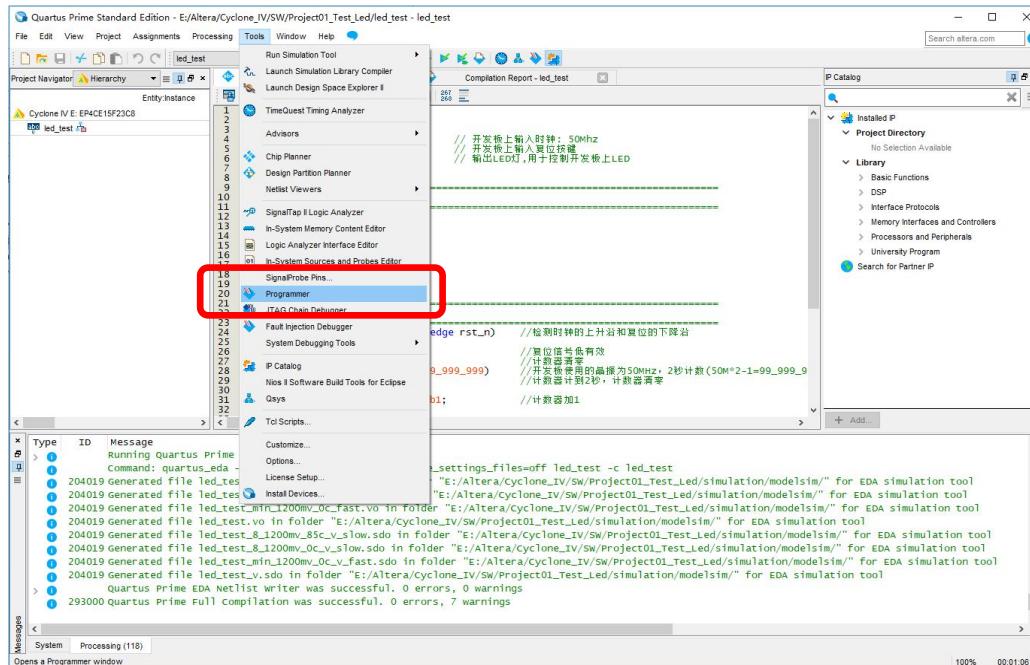


Figure 2-18. Programmer

Make sure the USB Blaster's cable are correctly connected to FPGA's JTAG port before using Programmer to download \*.sof file. Then click 【Auto Detect】 to check the hardware setup is okay or not:

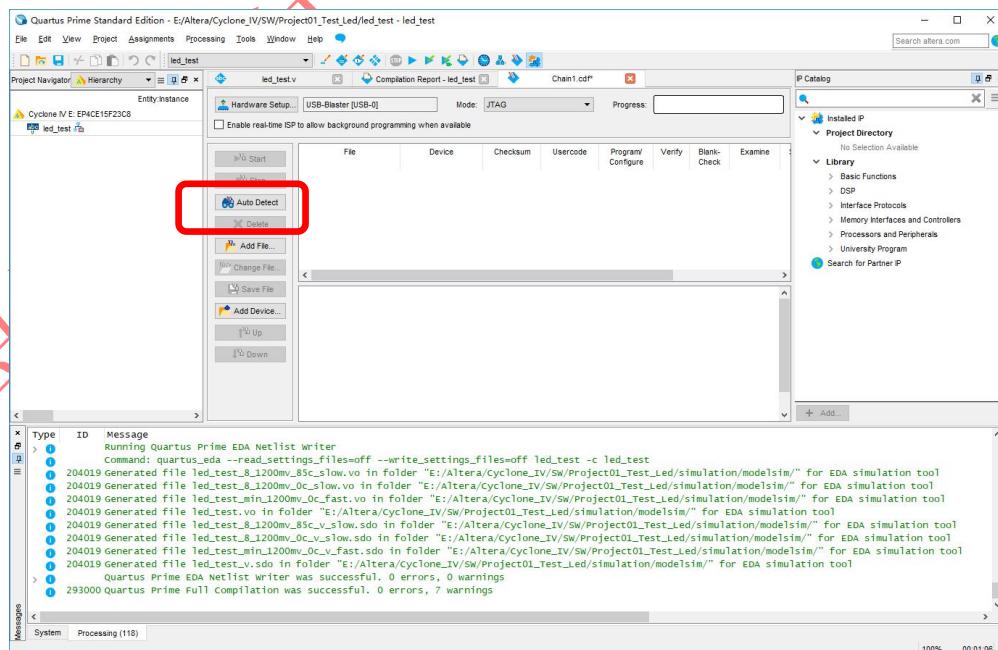
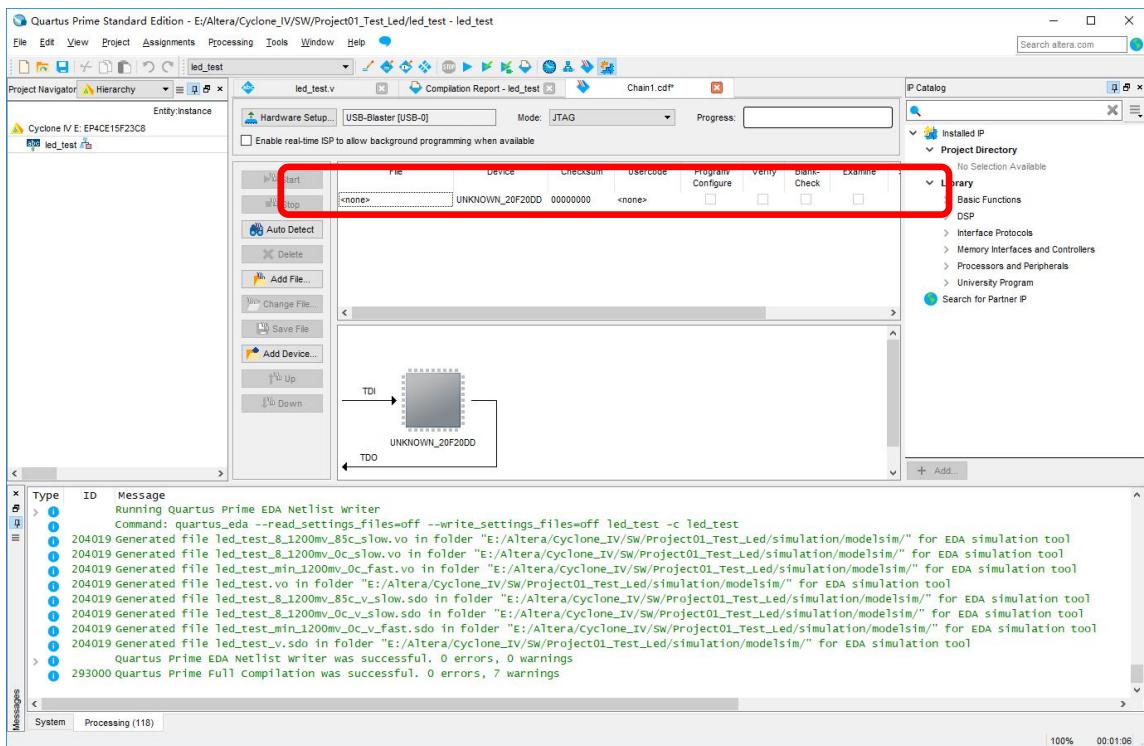


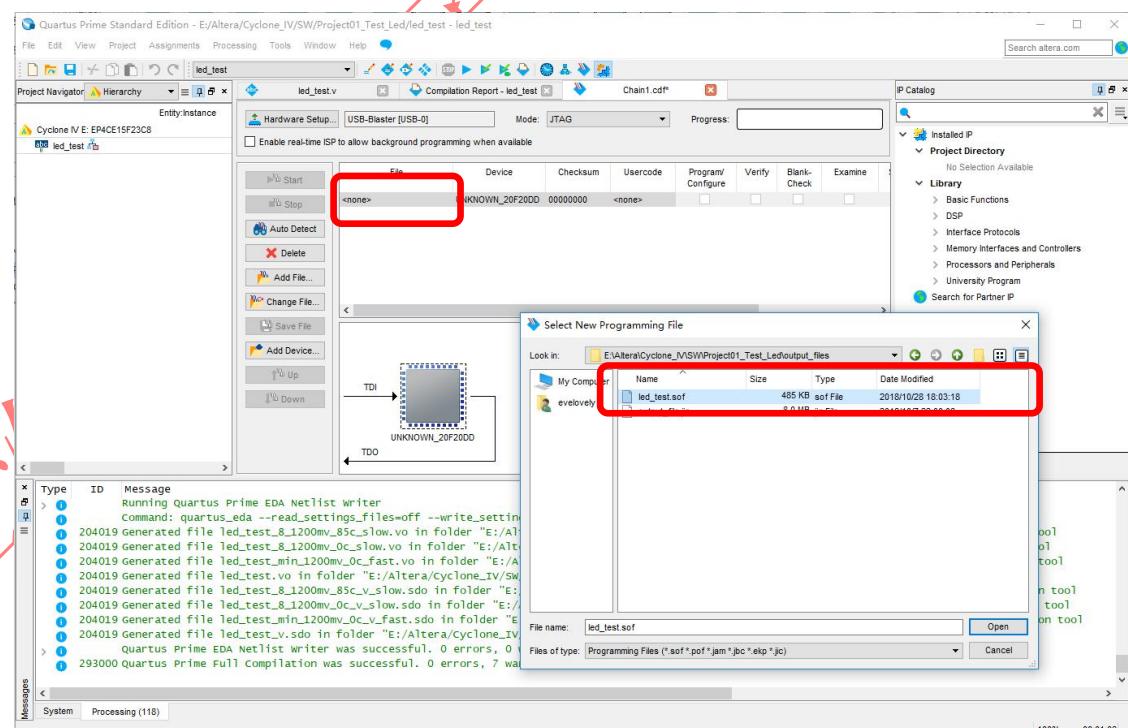
Figure 2-19. JTAG Setup

Below image shows the FPGA has been detected by the Programmer:



**Figure 2-20. Detect FPGA**

Users click 【None】 column to choose the \*.sof file to be loaded into FPGA.



**Figure 2-21. Choose \*.sof File**



QMTECH

Cyclone IV EP4CE55 Core Board

User Manual-V01

Then toggle 【Program/Configure】 and click the 【Start】 button to start a new program:

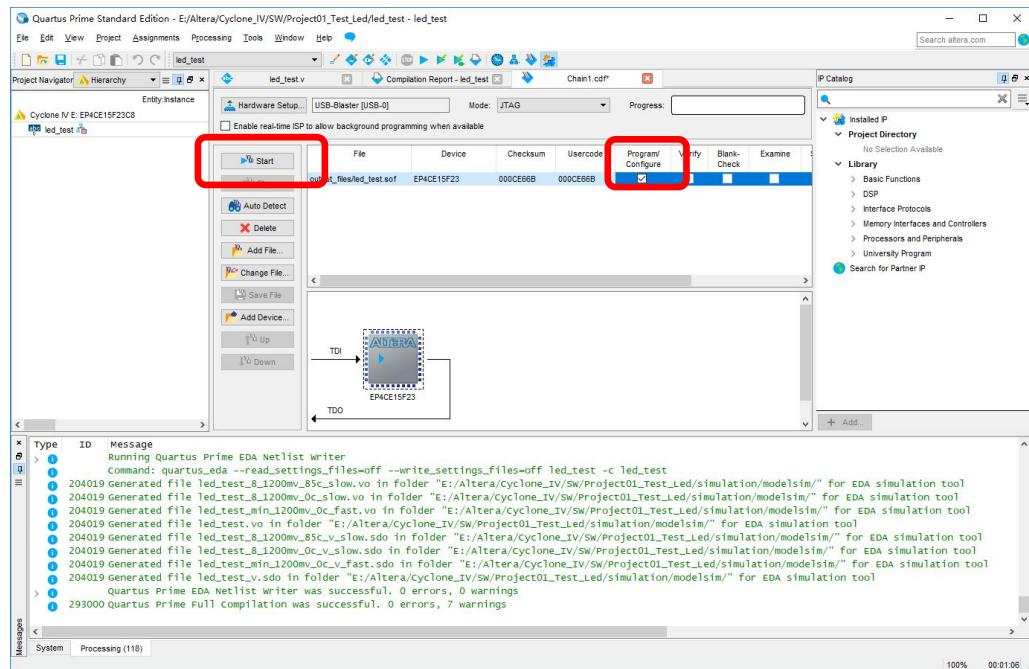


Figure 2-22. Program \*.sof

If the \*.sof file is correctly programmed, the Progress bar will show info like: 100% (Successful). Then users could check whether the LEDs on FPGA board blinking or not.

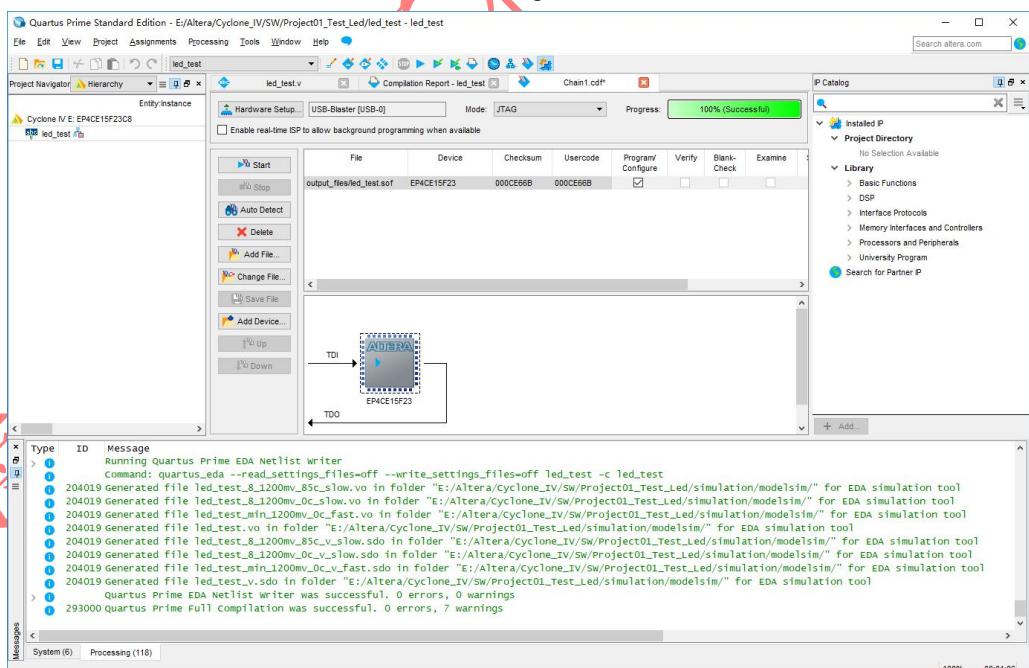
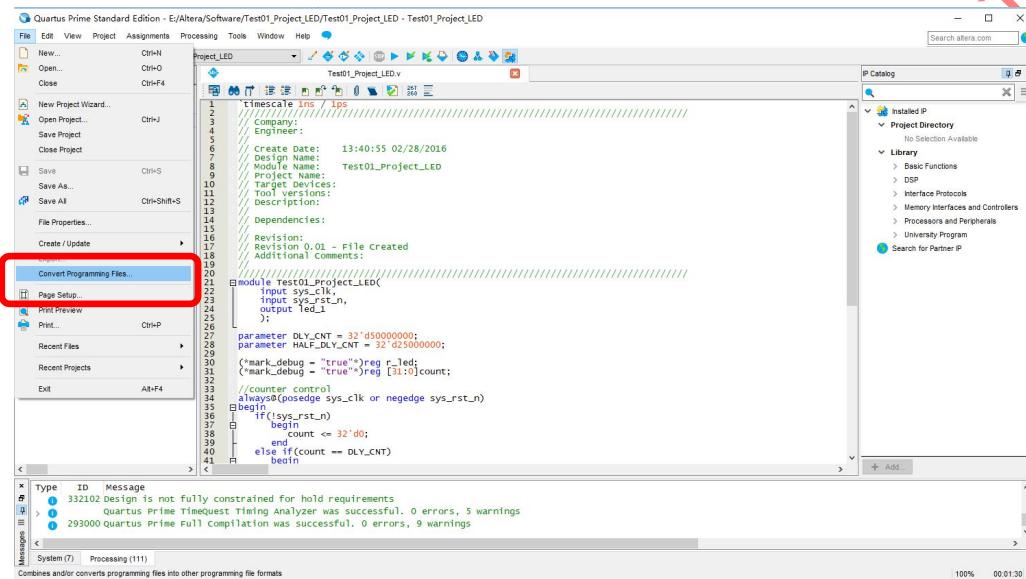


Figure 2-23. Program Successful

## 2.5 Download \*.jic into SPI Flash

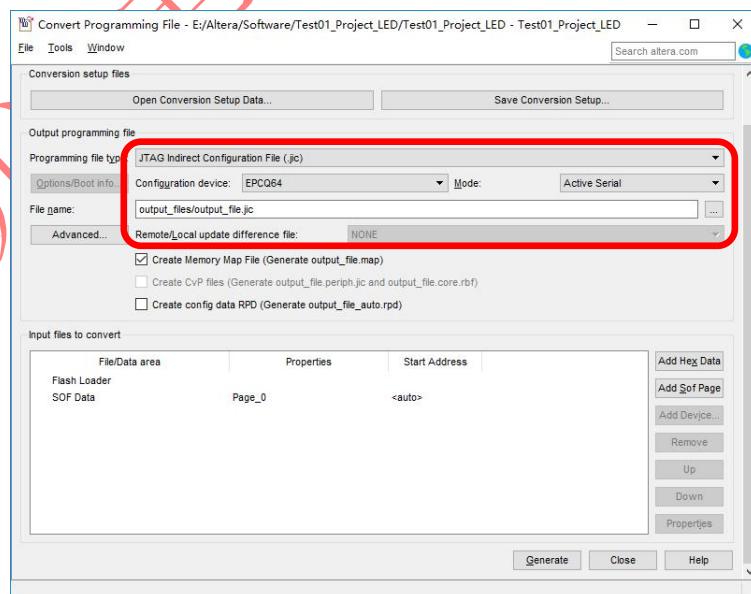
Cyclone IV EP4CE55 core board has mounted an external SPI Flash with 8MB capacity. The hardware design chooses Active Serial x 1 method to make the FPGA could boot up from external SPI Flash after power on. In this section, it describes how to program eternal SPI Flash through JTAG port. The SPI Flash is non-volatile device which means the programmed \*.jic file will never lose its content after power down.

The SPI Flash programming file \*.jic is converted by \*.sof file described in previous chapter. So make sure \*.sof could be correctly running on FPGA before performing below steps. Step1: choose the Quartus II Prime 15.1 file convert tool by click 【File】→【Convert Programming File】:



**Figure 2-24. Convert Programming File Tool**

Change the settings following below figure: choose EPCQ64, generated file name output\_file.jic, etc.



**Figure 2-25. Configure Convert Programming File Tool**

Click the 【Advanced...】 option, and set these below two options in the red rectangle in Disable status:

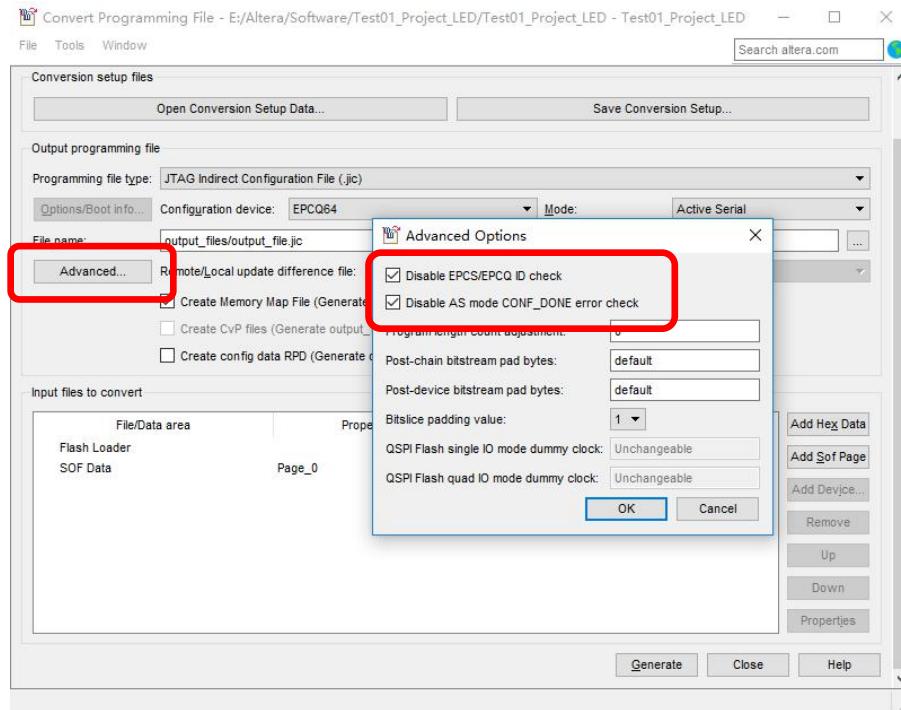


Figure 2-26. Advanced Options

Select 【Flash Loader】 and then click 【Add Device】 button:

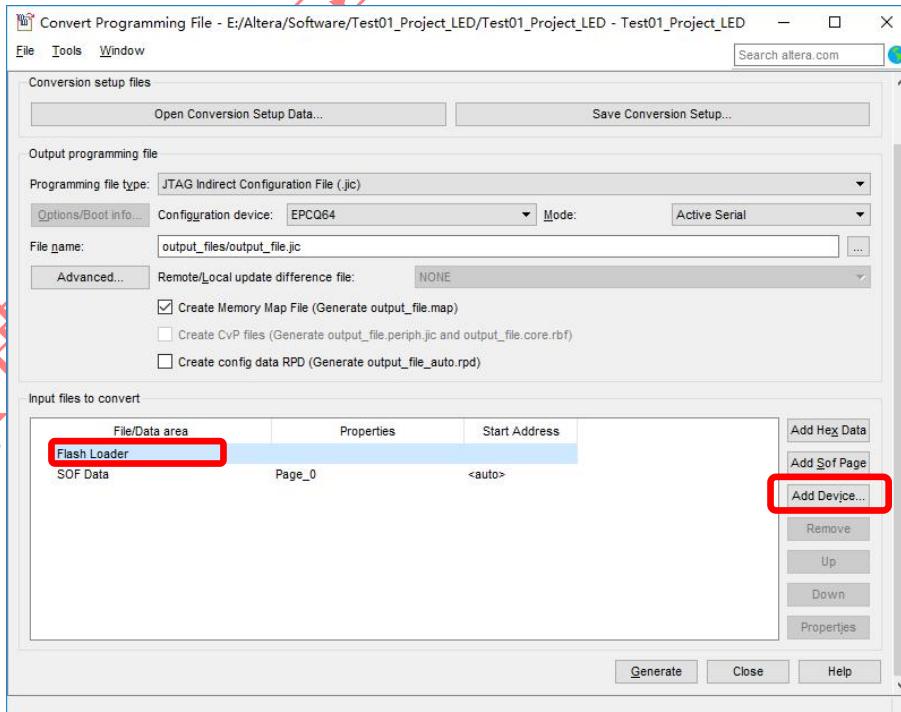
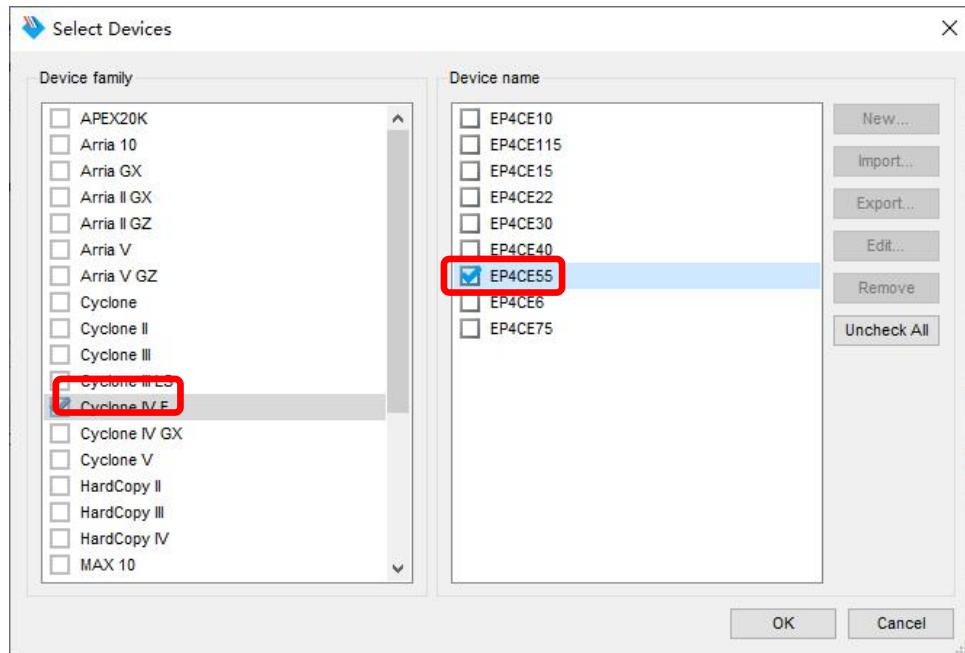


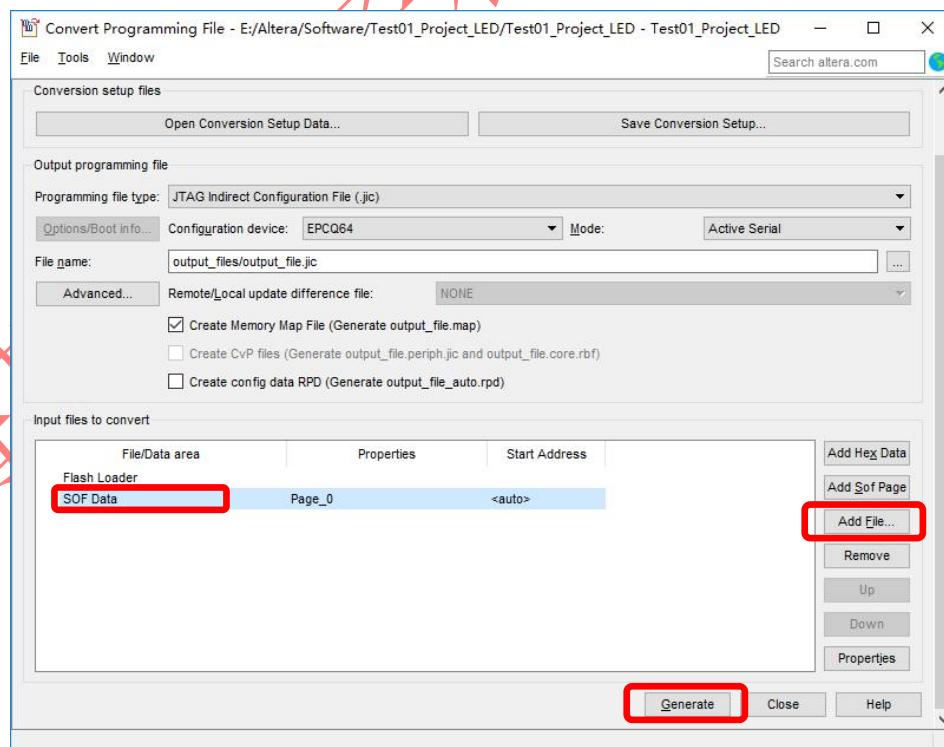
Figure 2-27. Flash Loader

Choose the target Flash Loader device: EP4CE55:



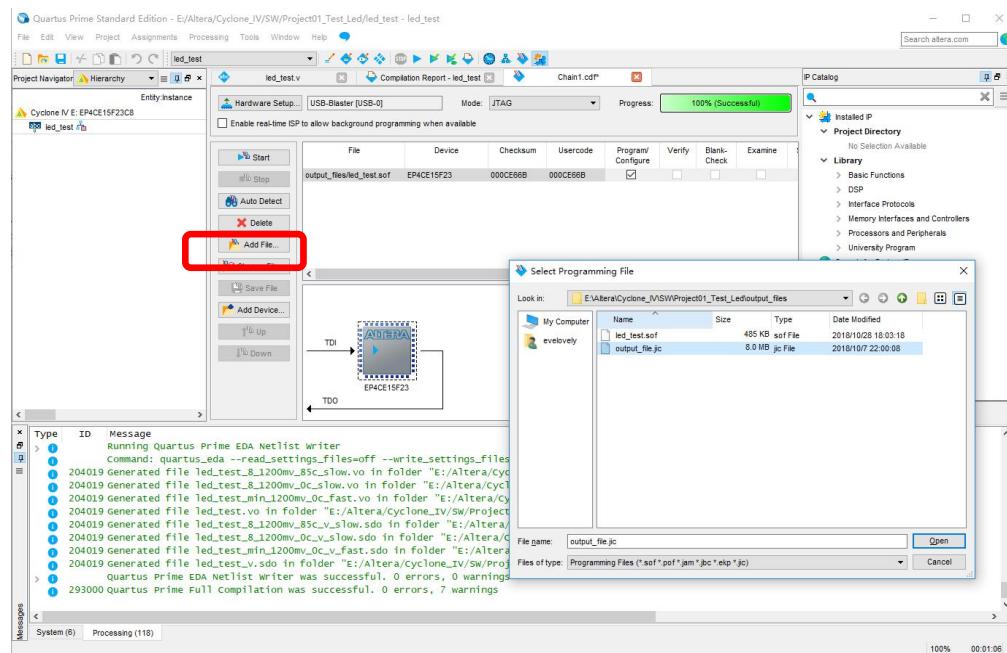
**Figure 2-28. Flash Loader for EP4CE55**

Select 【SOF Data】 and then choose 【Add File...】 to add the verified \*.sof file. And then click 【Generate】 to generate the output\_file.jic file:



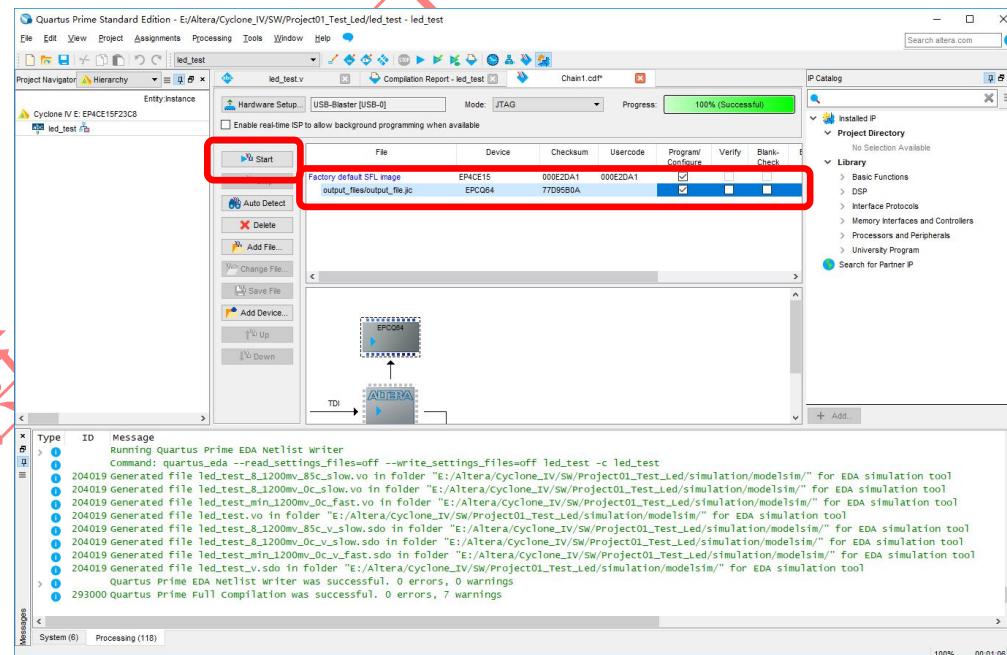
**Figure 2-29. Generate \*.jic File**

After the output\_file.jic correctly generated, run the 【Tools】→【Programmer】. And then click 【Add File...】 to choose the output\_file.jic.



**Figure 2-30. Choose \*jic File**

Toggle 【Program/Configure】 and then click 【Start】 button to program the external SPI Flash. Program status will be shown in the 【Progress】 bar. After the \*.jic correctly programmed, user may repower on the board to check whether the FPGA could boot from external SPI Flash.



**Figure 2-31. Program \*.jic**

### 3. SignalTap II Logic Analyzer

The SignalTap II Embedded Logic Analyzer is a system-level debugging tool that captures and displays signals in circuits designed for implementation in Intel's FPGAs. The user is expected to have access to a computer that has Quartus II 15.1 software installed. The detailed example in this chapter was obtained using Quartus II version 15.1, but newer versions of the software can also be used.

After successfully compiling the Project04\_SDRAM project and setting pin assignments, select SignalTap II Logic Analyzer from the tools dropdown menu (as shown below). Ensure the JTAG programmer (USB Byte Blaster) is connected between the board and the computer.

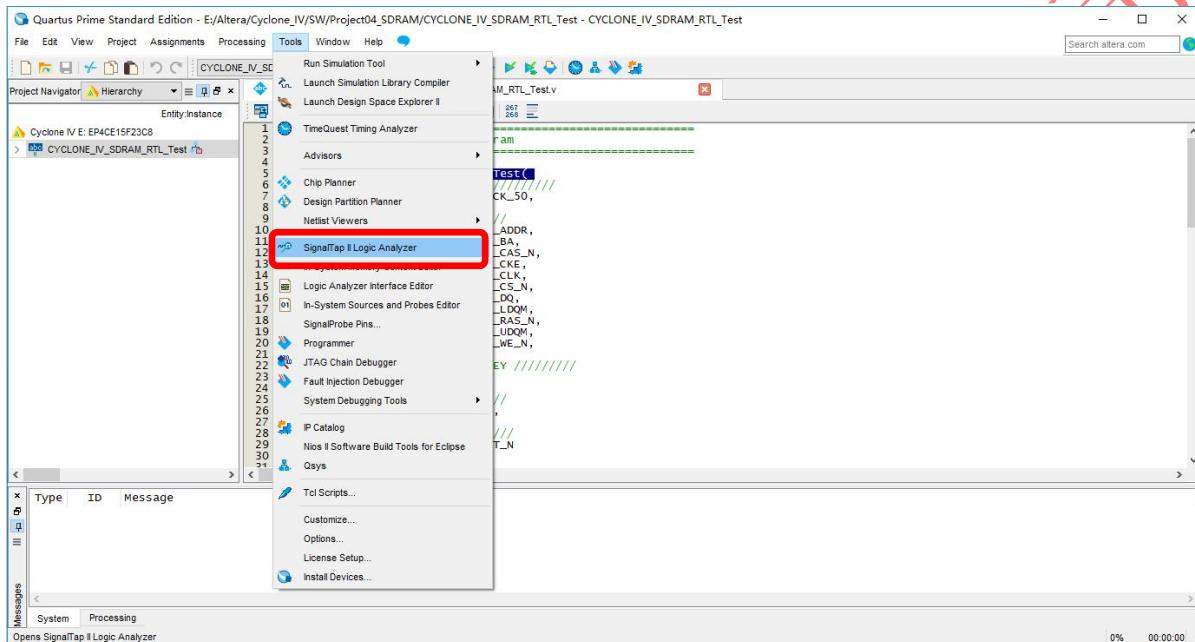


Figure 3-1. Open SignalTap II Logic Analyzer

Below image shows the UI of the SignalTap II:

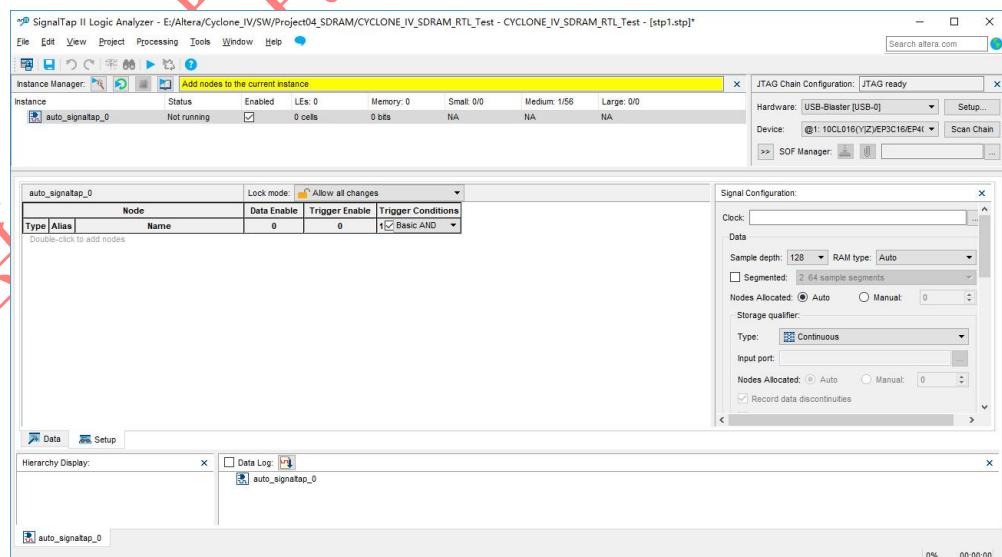


Figure 3-2. SignalTap II Logic Analyzer sUI

Below image shows the settings of the Project04\_SDRAM example project:

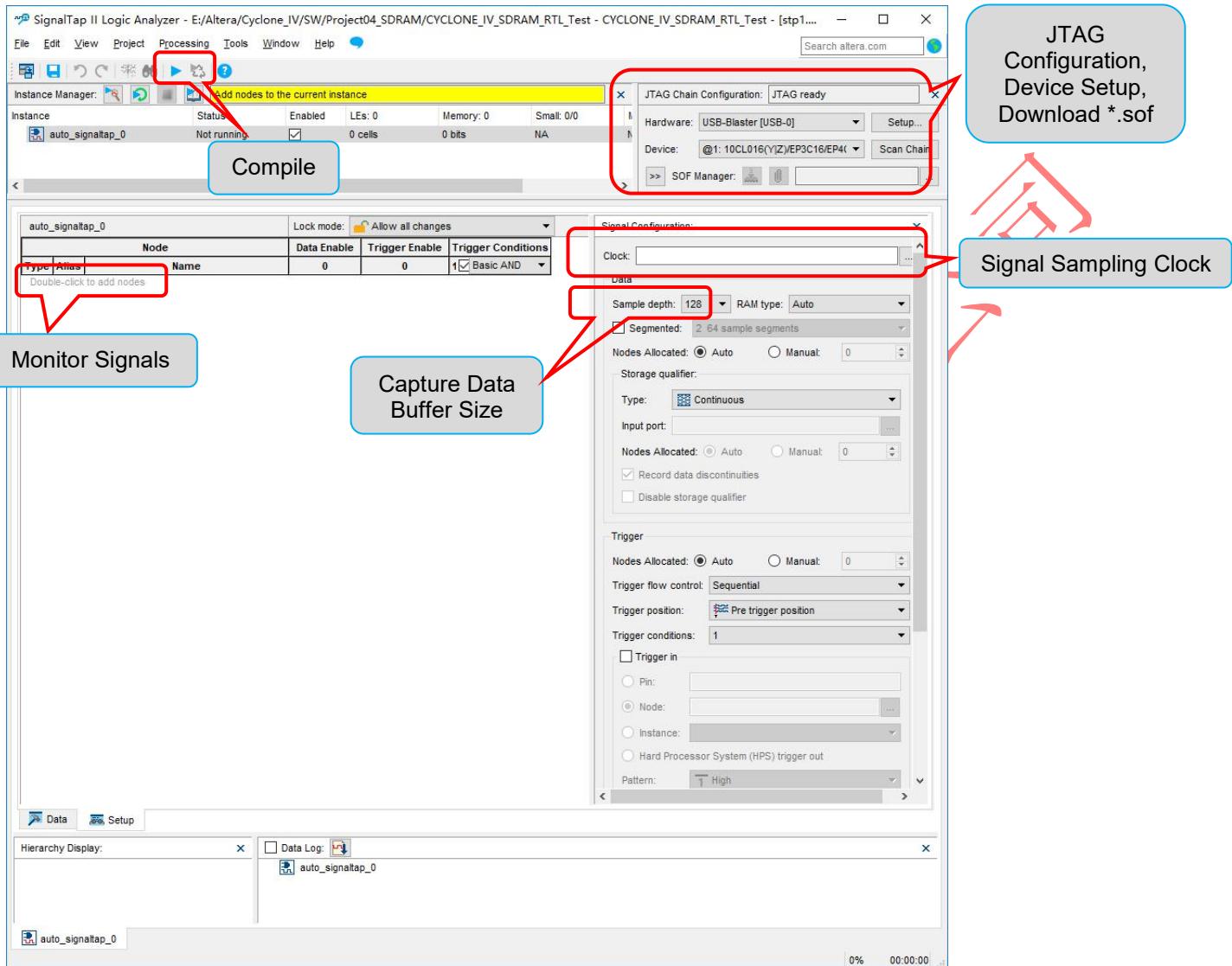
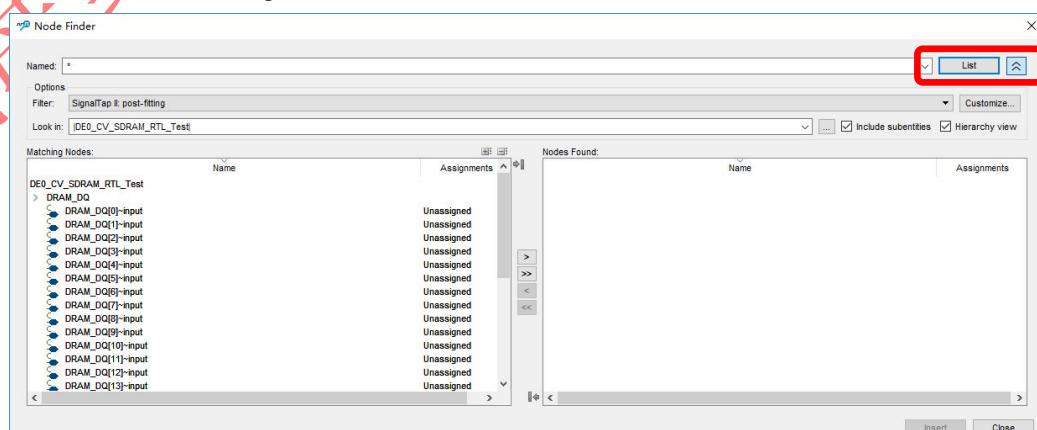
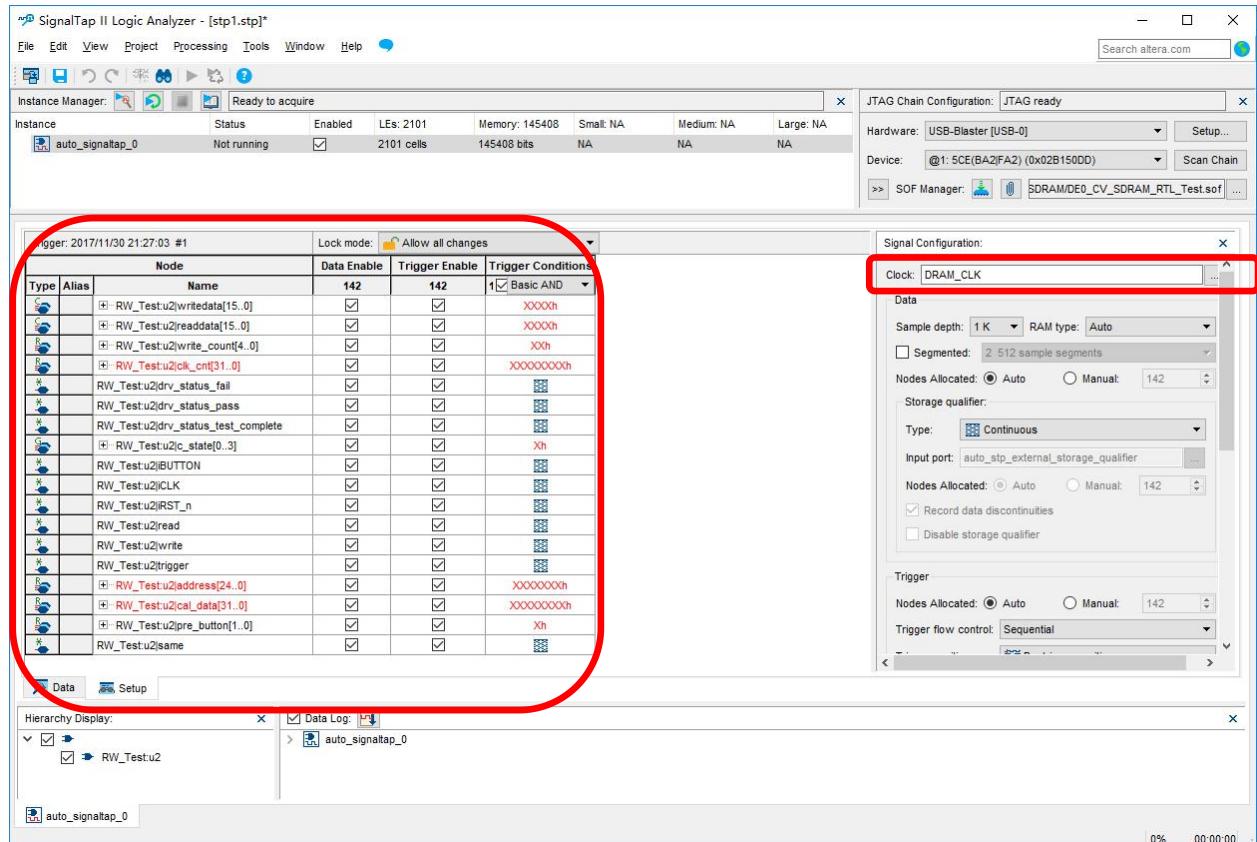


Figure 3-3. SignalTap II Logic Analyzer Main Window

Double click the **【Node】** column shown in the above image. Below window will pop up and user clicks the **【List】** button to add the signals need to be monitored:

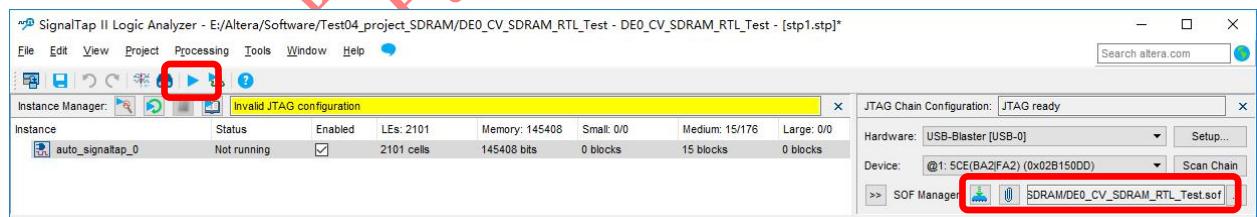


All the signals added in the above step will be displayed in the **【setup】** page. Please also select the signal sampling clock **【DRAM\_CLK】** :



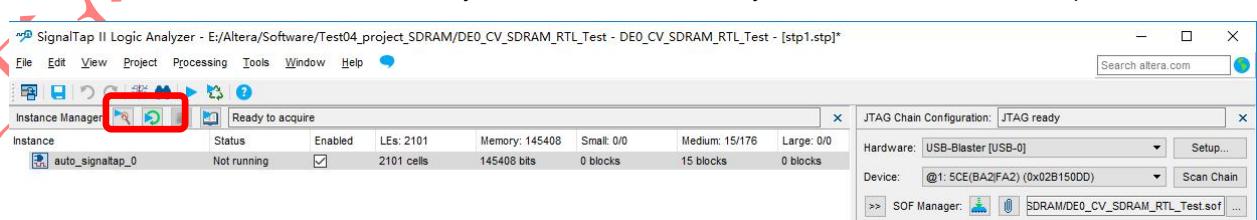
**Figure 3-4. Sampling Signals and Clocks**

User needs to click the **【Compile】** button shown in the below image to recompile the whole project. Then user may download the newly compiled \*.sof into FPGA.



**Figure 3-5. Compile the SignalTap II Projects**

User could click the button **【AutoRun Analysis】** or button **【Run Analysis】** to start the waveform capture:



**Figure 3-6. Start Capture**

Below two images show the SDRAM data write and SDRAM data read:

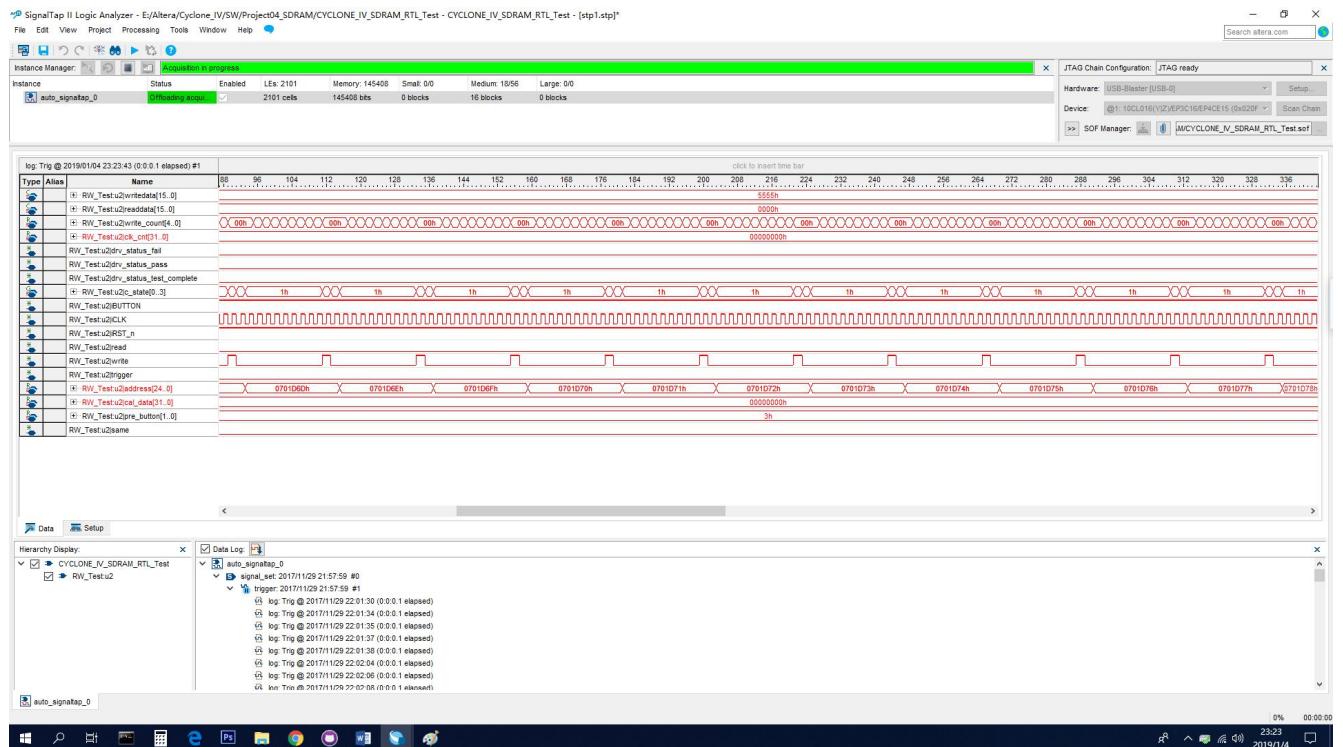


Figure 3-7. Waveform for Writing Data into SDRAM

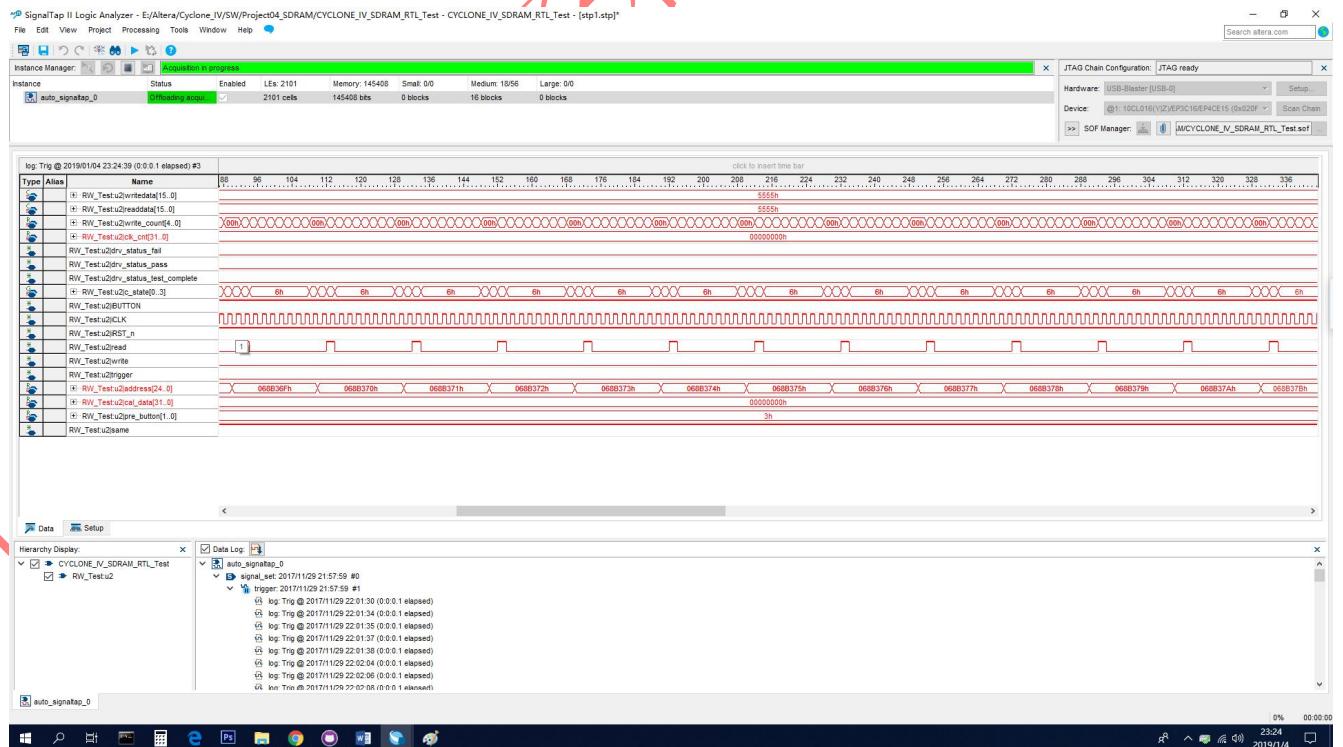


Figure 3-8. Waveform for Reading Data from SDRAM

#### 4. Reference

- [1] ep4ce55f23-sdram.pdf
- [2] an592.pdf
- [3] an592\_ch.pdf
- [4] cyiv-5v1.pdf
- [5] cyiv-5v2.pdf
- [6] cyiv-5v3.pdf
- [7] pcg-01008.pdf

上海勸謀電子科技有限公司



QMTECH

Cyclone IV EP4CE55 Core Board

User Manual-V01

## 5. Revision

Doc. Rev.	Date	Comments
0.1	10/06/2018	Initial Version.
1.0	06/08/2019	Formal Release.

上海勸謀電子科技有限公司

