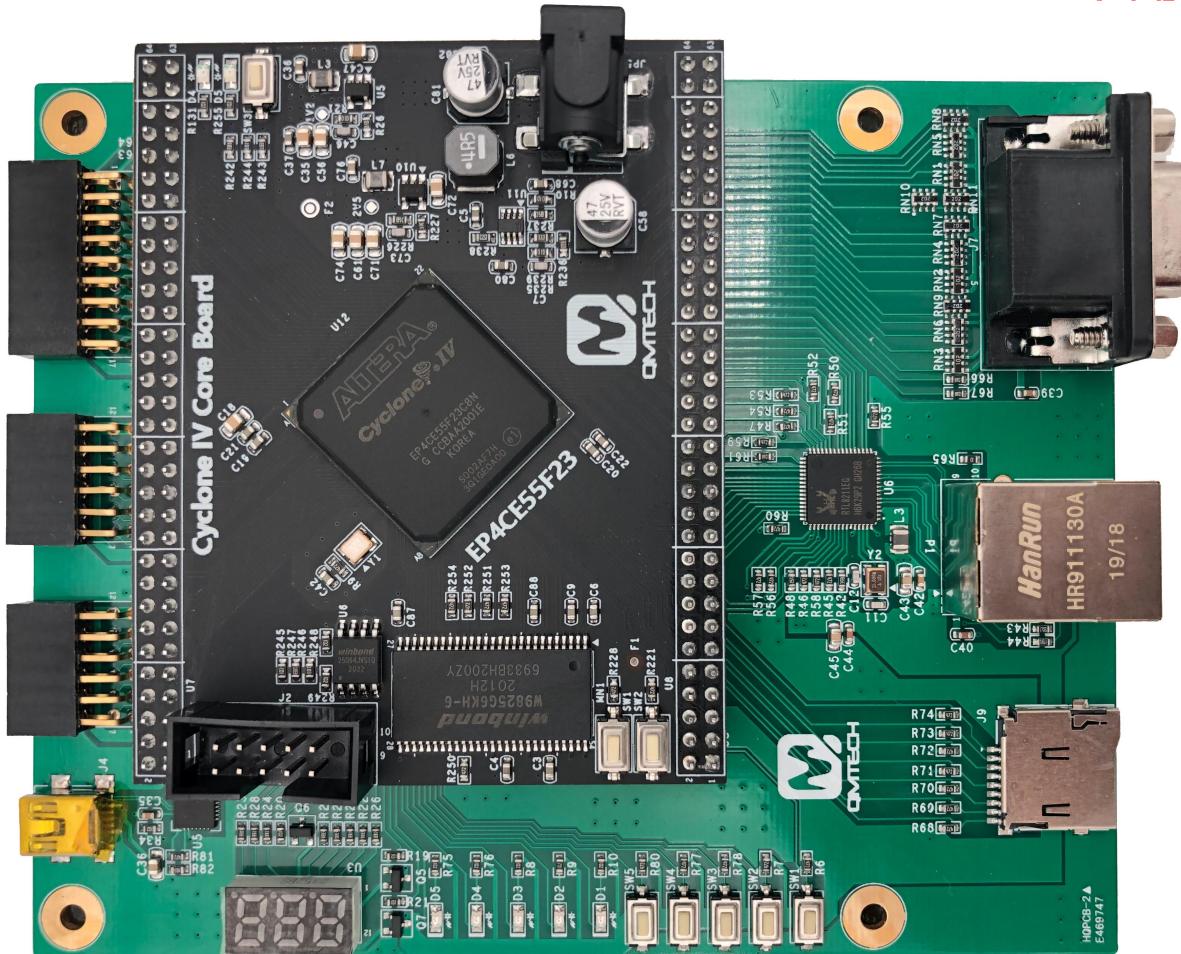


QMTECH_CYCLONE_IV_EP4CE55 DB

USER MANUAL



Preface

The QMTECH® Cyclone IV SDRAM Development Board uses Intel(Altera) EP4CE55F23 device to demonstrate Intel's leadership in offering power-efficient FPGAs. With enhanced architecture and silicon, advanced semiconductor process technology, and power management tools, power consumption for Cyclone IV FPGAs has been reduced by up to 25 percent compared to Cyclone® III FPGAs. The result is the lowest power consumption of any comparable FPGA.



QMTECH

QMTECH_CycloneIV_EP4CE55 Daughter Board User Manual

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QMTECH_CycloneIV_EP4CE55 Daughter Board

User Manual-V01

1. QMTECH_CycloneIV_EP4CE55 DB Introduction

1.1 Kit Overview

QMTECH_CycloneIV_EP4CE55 provides several user interfaces to meet different customer needs. Below section lists the detailed info of these user interfaces:

- USB to UART Serial Port, by using Silicon Labs' CP2102-GMR chip.
- 16bit(RGB565) VGA display interface, by using resistor dividers;
- GMII ethernet interface, by using Realtek's RTL8211EG chip;
- CMOS/CCD camera interface, by using 18pin female header;
- Two Digilent PMOD standard compatible female headers;
- MicroSD card slot;

1.2 Daughter Board Top View

Below figure shows the daughter board of QMTECH_CycloneIV_EP4CE55 development kit. The daughter board's dimension is 108.71mm x 134.62mm. All the functional chips' power supply is injected from the 64P female connector, detailed connection refer to the hardware schematic.

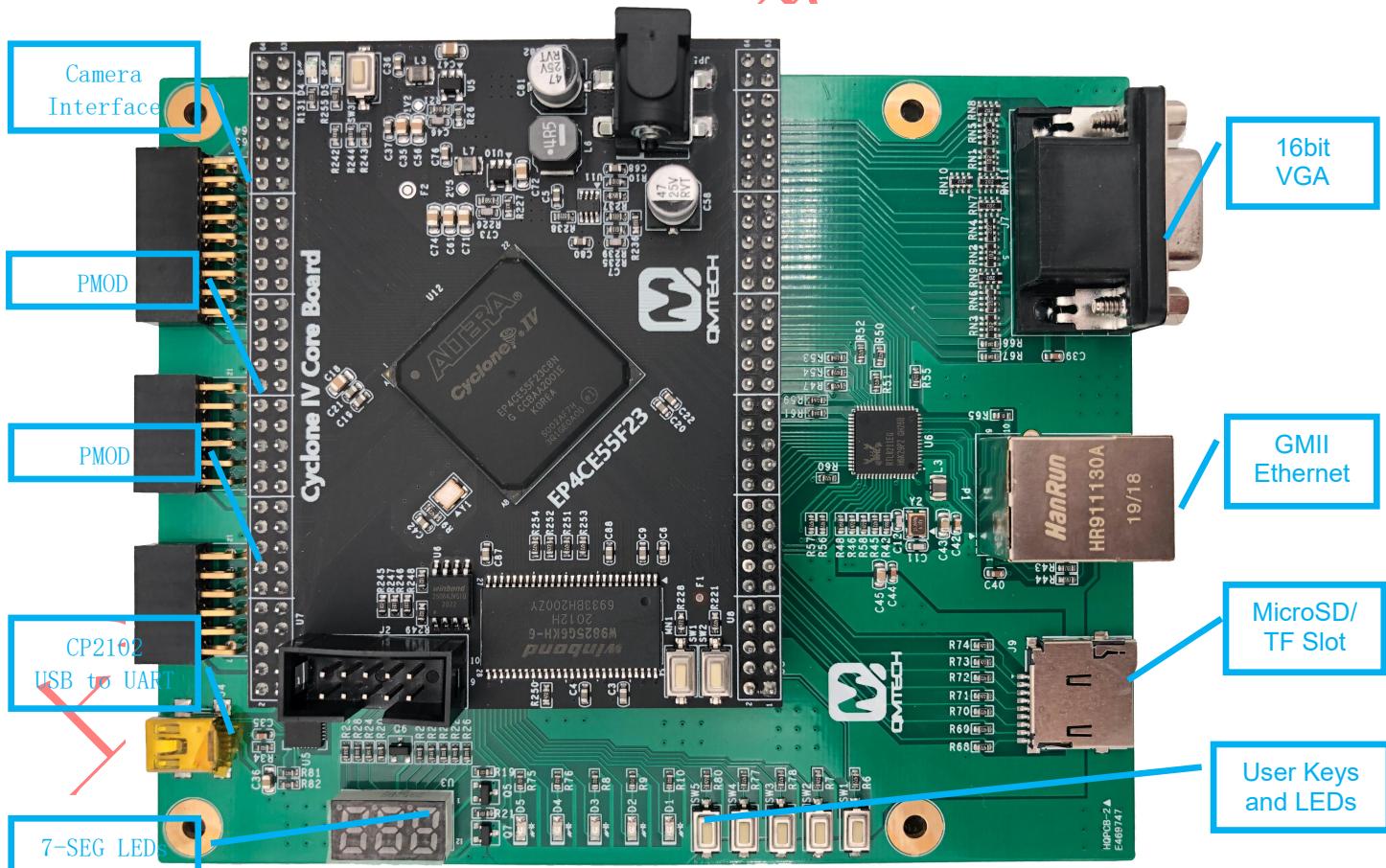


Figure 1-1. QMTECH_CycloneIV_EP4CE55 Daughter Board

2. Experiment (1): USB to Serial Port

The CP2102-GMR is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102-GMR includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components required for development. Below figure shows the hardware design of CP2102-GMR on the QMTECH_CycloneIV_EP4CE55 daughter board.

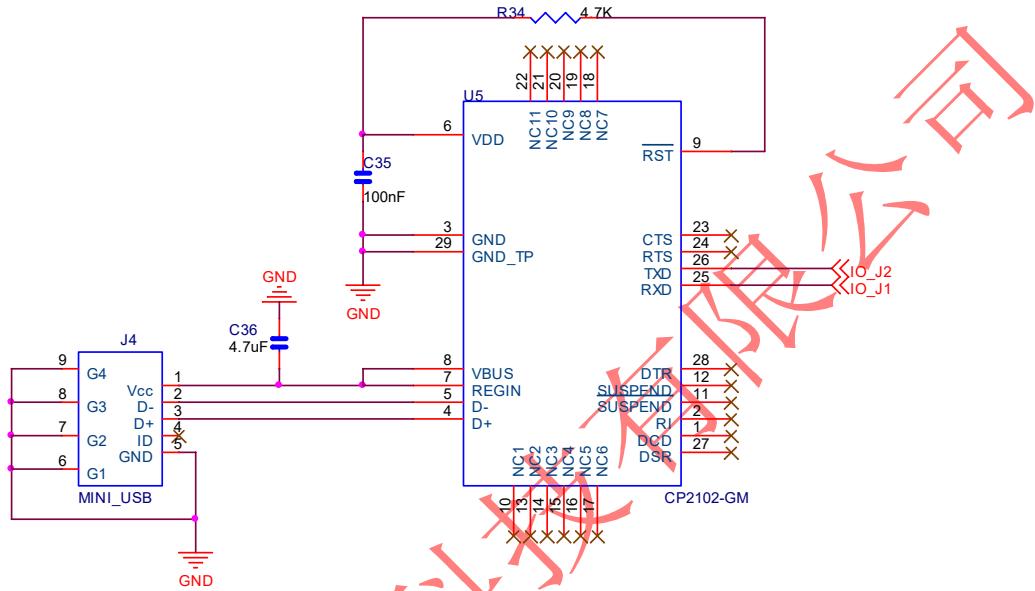
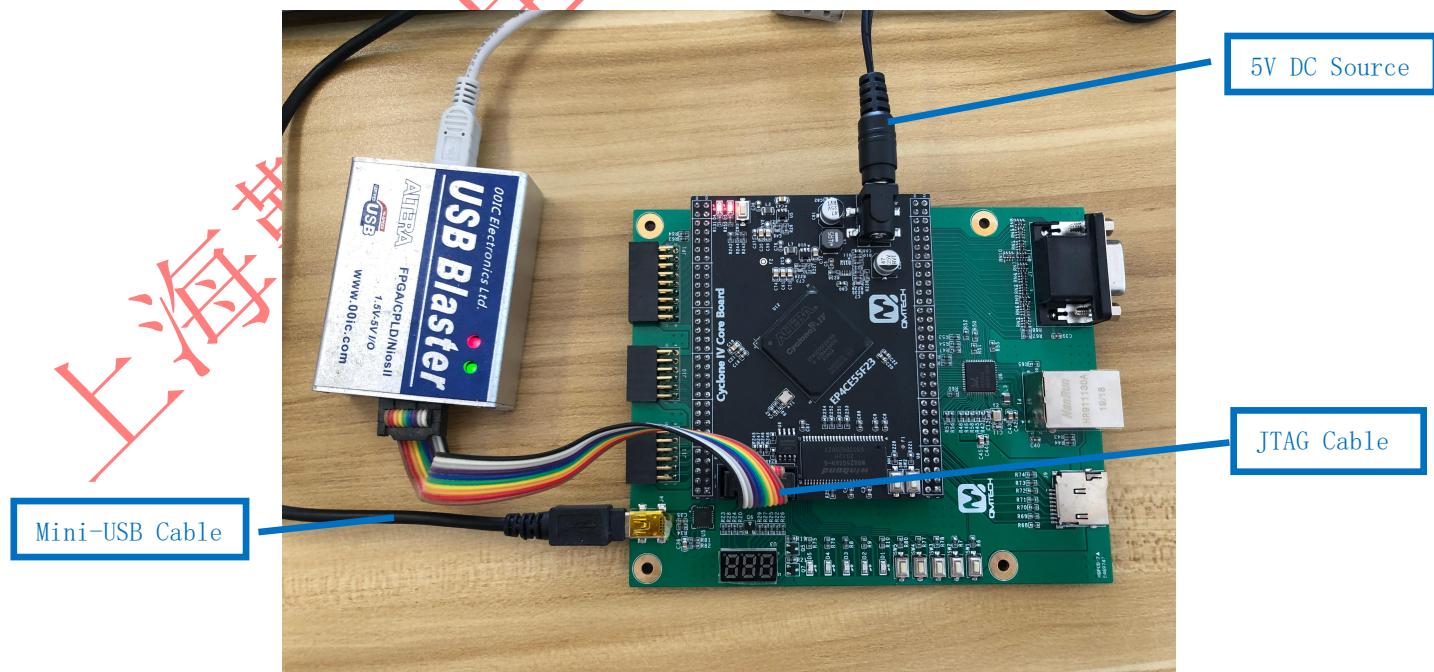


Figure 2-1. CP2102 Hardware Design

Before start to test the CP2102-GMR's USB to UART serial communication function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to QMTECH_CycloneIV_EP4CE55 core board's JTAG interface. Then power on the development kit with 5V DC power source and plug the Mini-USB cable in the daughter board, below figure shows an example hardware setup:



All the test examples are developed in the Quartus II 15.1 environment. Open the CP2102 test project located in this release folder: /Software/ Project05_CP2102_UART_V2. Below figure shows the example project of **uart_top**:

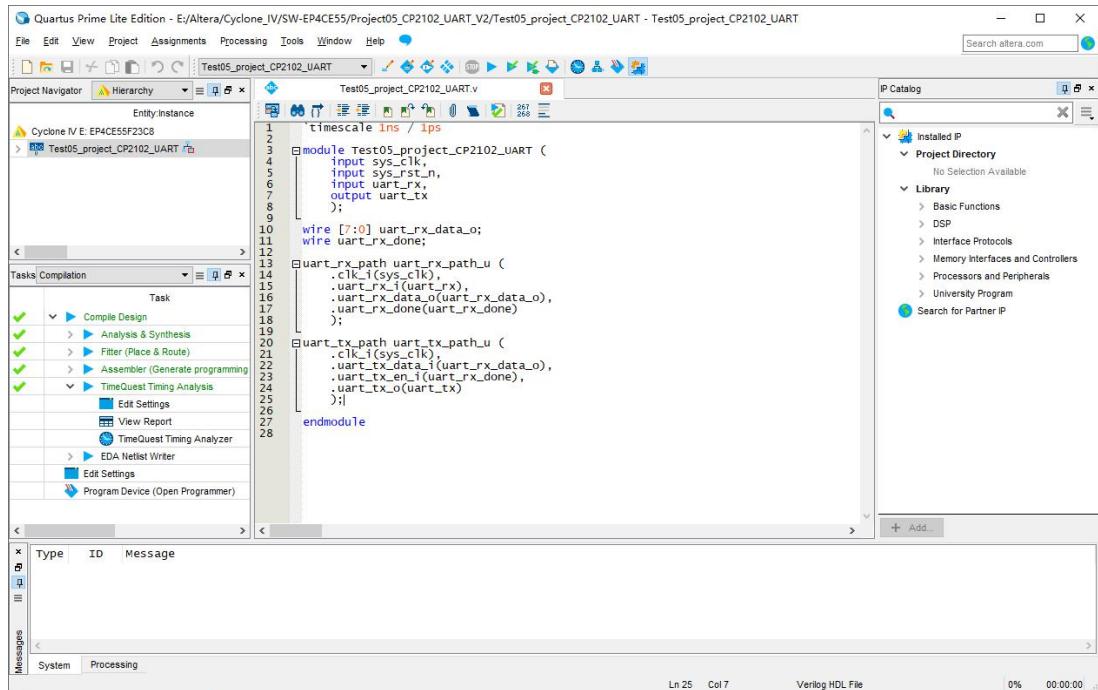


Figure 2-2. CP2102 UART Communication Test Example

In this example project, the default communication parameters are: 9600bps, 8 data bit, No Parity Check, 1 stop bit. If users want to test other communication parameters, change the source code accordingly.

```

uart_rx_path.v
1 `timescale ins / ips
2
3 module uart_rx_path(
4     input clk_i,
5     input uart_rx_i,
6
7     output [7:0] uart_rx_data_o,
8     output uart_rx_done,
9     output baud_bps_tb           //for simulation
10 );
11
12 parameter [12:0] BAUD_DIV      = 13'd5208;    //波特率时钟, 9600bps, 50Mhz/9600=5208
13 parameter [12:0] BAUD_DIV_CAP = 13'd2604;    //波特率时钟中间采样点, 50Mhz/9600/2=2604
14
15 reg [12:0] baud_div=0;          //波特率设置计数器
16 reg baud_bps=0;                //数据采样点信号
17 reg bps_start=0;               //波特率启动标志
18 always@(posedge clk_i)
19 begin
20     if(baud_div==BAUD_DIV_CAP)   //当波特率计数器计数到采样点时, 产生采样信号baud_bps

```



```

uart_tx_path.v
1 `timescale ins / ips
2
3 module uart_tx_path(
4     input clk_i,
5
6     input [7:0] uart_tx_data_i,        //待发送数据
7     input uart_tx_en_i,              //发送使能信号
8
9     output uart_tx_o
10 );
11
12 parameter BAUD_DIV      = 13'd5208;    //波特率时钟, 9600bps, 50Mhz/9600=5208, 波特率可调
13 parameter BAUD_DIV_CAP = 13'd2604;    //波特率时钟中间采样点, 50Mhz/9600/2=2604, 波特率可调
14
15 reg [12:0] baud_div=0;          //波特率设置计数器
16 reg baud_bps=0;                //数据发送点信号, 高有效
17 (* MARKDEBUG = "TRUE" *) reg [9:0] send_data=10'b1111111111; //待发送数据寄存器, lbit起始信号+8bit有效信号+lbit结束信号
18 (* MARKDEBUG = "TRUE" *) reg [3:0] bit_num=0;                  //发送数据个数计数器
19 reg uart_send_flag=0;           //数据发送标志位
20 reg uart_tx_o_z=1;             //发送数据寄存器, 初始状态位高

```

After the CP2102 communication test project correctly synthesized, implemented and generated *.sof file, users could use Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

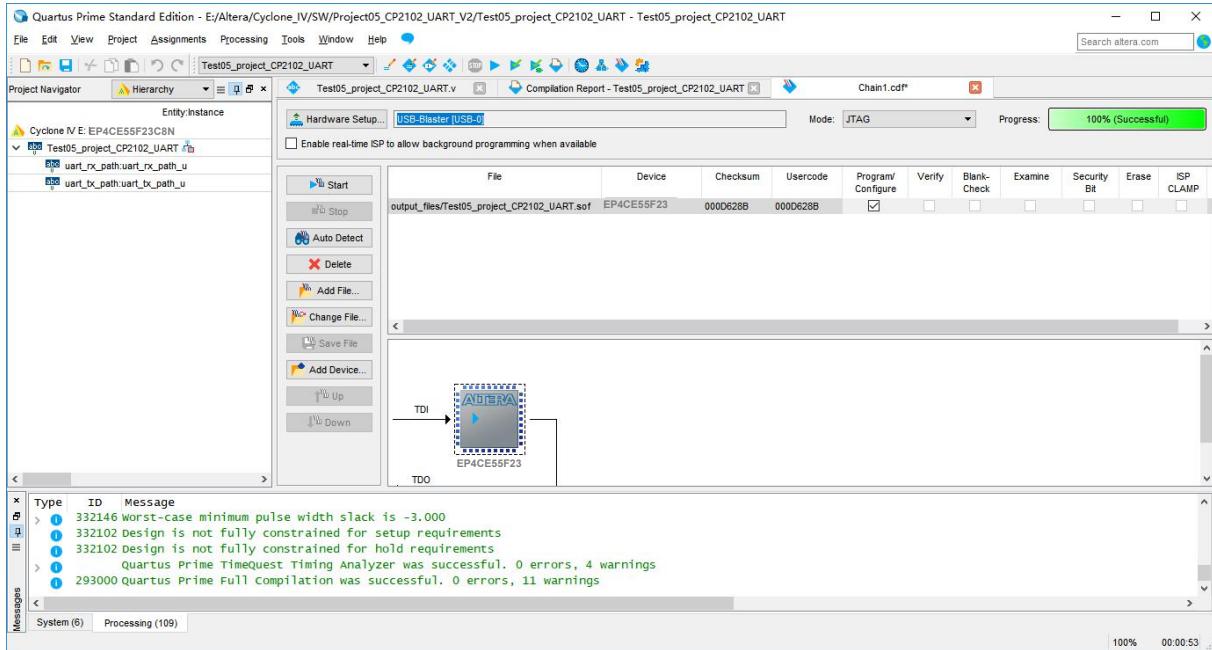


Figure 2-3. Program *.sof File

The CP2102 example test project's main functionality is performing an UART loopback communication. The FPGA program will send the received UART data back to the PC. Below figure shows user employees some PC based UART test tool to send data to FPGA: <http://www.cmsoft.cn> QQ:10865600. After a short while the PC UART test tool will receive the same data stream from FPGA, which means the CP2102 loopback test program is running correctly.



Figure 2-4. UART Loopback Test

3. Experiment (2): VGA Displays

The RGB signal accepted by the color monitor is an analog signal, one for each color, in the range 0V to 0.7V according to the VGA spec. So the digital color signal generated by the video controller should be converted to an analog signal. The daughter board uses resistor to form a voltage divider circuit in combination with the 75 ohm load resistance of VGA monitor. Below image shows the hardware design.

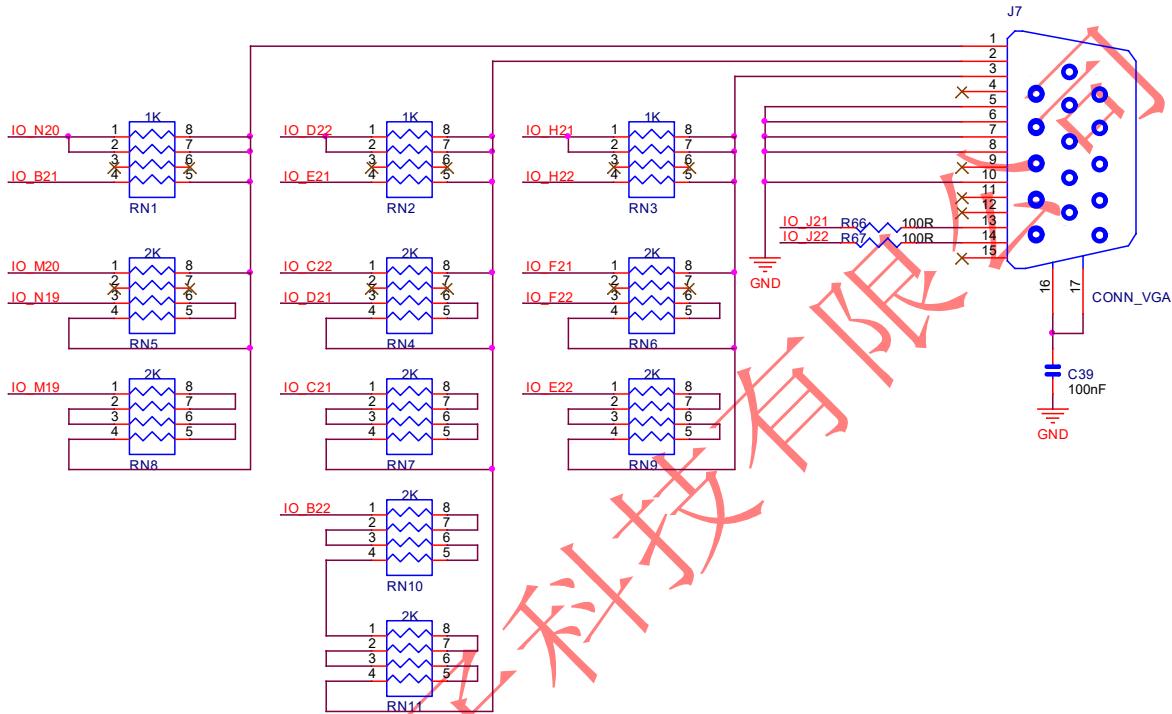
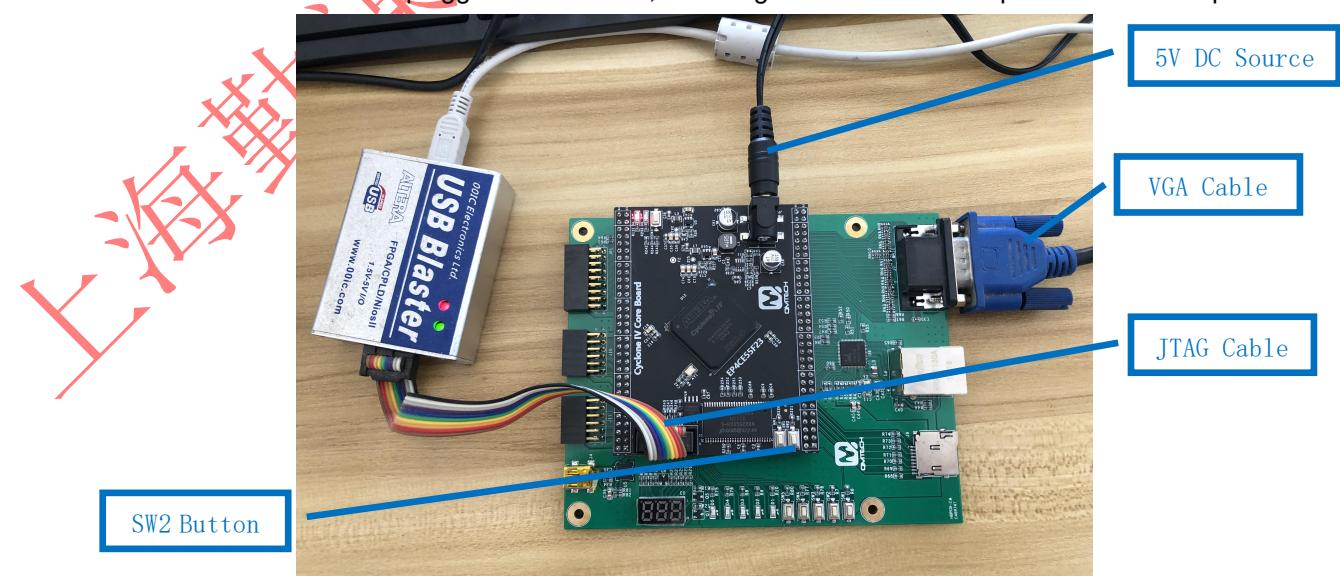


Figure 3-1. VGA Display Hardware Designs

Before start to test the VGA display function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to QMTECH_CycloneIV_EP4CE55 core board's JTAG interface. Then power on the development kit with 5V DC power source and the VGA cable shall also be plugged in the board, below figure shows an example hardware setup:



Open the VGA test project located in this release folder: /Software/ Project08_VGA. Below figure shows the example project of **VGA_test**:

```

Quartus Prime Standard Edition - E:/Altera/Cyclone_IV/SW/Project08_VGA/vga_test - vga_test
File Edit View Project Assignments Processing Tools Window Help
Project Navigator Hierarchy vga_test Compilation Report - vga_test Pin Planner vga_test.v
Entity Instance Cyclone IV E: EP4CE55F23C8N
vga_test
pli/pli_inst
Module Name: vga_test
timescale 1ns / 1ps
// Module Name: vga_test
module vga_test(
    input clk,
    input rstn,
    output vga_hs,
    output vga_vs,
    output [4:0] vga_r,
    output [5:0] vga_g,
    output [4:0] vga_b,
    input key1
);
// 水平扫描参数的设置1024*768 60Hz VGA
parameter LinePeriod =1344; //行周期数
parameter H_SyncPulse=136; //行同步脉冲 (sync a)
parameter H_BackPorch=160; //显示后沿 (Back porch b)
parameter H_ActiveVpix=1024; //显示时序段 (Display interval c)
parameter H_FrontPorch=4; //显示前沿 (Front porch d)
parameter Hde_start=296;
parameter Hde_end=1320;
// 垂直扫描参数的设置1024*768 60Hz VGA
parameter FramePeriod =806; //列周期数
parameter V_SyncPulse=6; //列同步脉冲 (sync o)
parameter V_BackPorch=29; //显示后沿 (back porch p)
parameter V_ActiveVpix=768; //显示时序段 (display interval q)
parameter V_FrontPorch=3; //显示前沿 (front porch r)
parameter Vde_start=35;
parameter Vde_end=803;
endmodule

```

Figure 3-2. VGA Display Function Test

In this example project, the default VGA output resolution parameter is 1024x768@60Hz. If users want to test other display parameters, change the source code accordingly.

```

Quartus Prime Standard Edition - E:/Altera/Cyclone_V/Software/Test12_project_VGA/vga_test - vga_test
File Edit View Project Assignments Processing Tools Window Help
Project Navigator Files vga_test
Files pli.v rlv/vga_test.v pli.qsp
16 // 水平扫描参数的设置1024*768 60Hz VGA
17 parameter LinePeriod =1344; //行周期数
18 parameter H_SyncPulse=136; //行同步脉冲 (sync a)
19 parameter H_BackPorch=160; //显示后沿 (Back porch b)
20 parameter H_ActiveVpix=1024; //显示时序段 (Display interval c)
21 parameter H_FrontPorch=4; //显示前沿 (Front porch d)
22 parameter Hde_start=296;
23 parameter Hde_end=1320;
24
25
26
27 // 垂直扫描参数的设置1024*768 60Hz VGA
28 parameter FramePeriod =806; //列周期数
29 parameter V_SyncPulse=6; //列同步脉冲 (sync o)
30 parameter V_BackPorch=29; //显示后沿 (back porch p)
31 parameter V_ActiveVpix=768; //显示时序段 (display interval q)
32 parameter V_FrontPorch=3; //显示前沿 (front porch r)
33
34
35
36
37
38 // 水平扫描参数的设置800*600 VGA
39 parameter LinePeriod =1056; //行周期数
40 parameter H_SyncPulse=102; //行同步脉冲 (sync a)
41 parameter H_BackPorch=88; //显示后沿 (back porch b)
42 parameter H_ActiveVpix=800; //显示时序段 (display interval c)
43 parameter H_FrontPorch=40; //显示前沿 (Front porch d)
44
45
46
47
48 // 垂直扫描参数的设置800*600 VGA
49 parameter FramePeriod =628; //列周期数
50

```

Figure 3-3. VGA Display Parameters

After the VGA display test project correctly synthesized, implemented and generated *.sof file, users could use Altera Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.



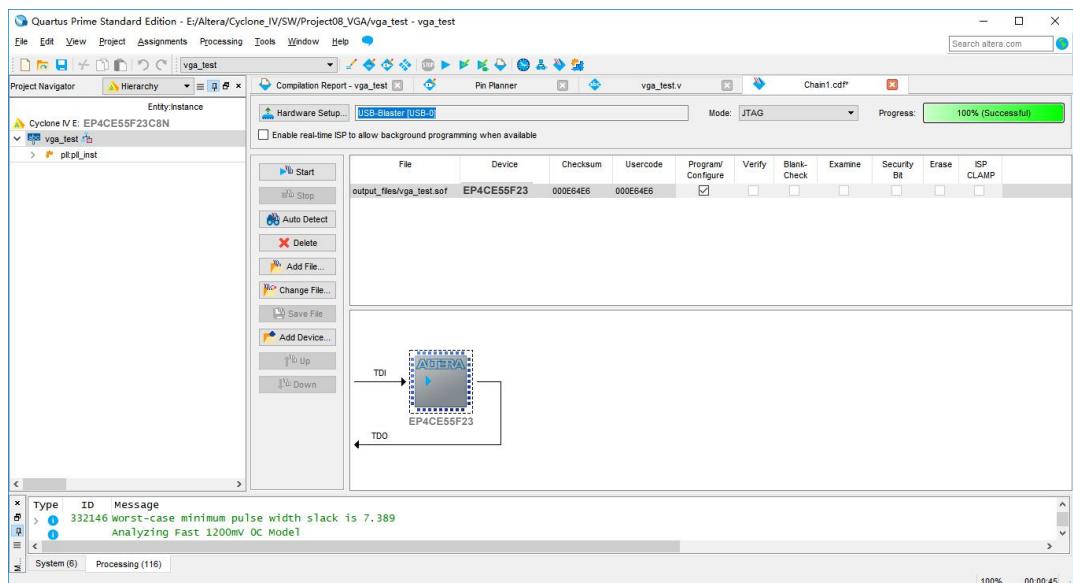


Figure 3-4. Program FPGA

After the FPGA correctly loaded the vga_test.sof file and users pressed the SW2 button on core board, the VGA monitor will display different color patterns. Below image shows the example color bar pattern.

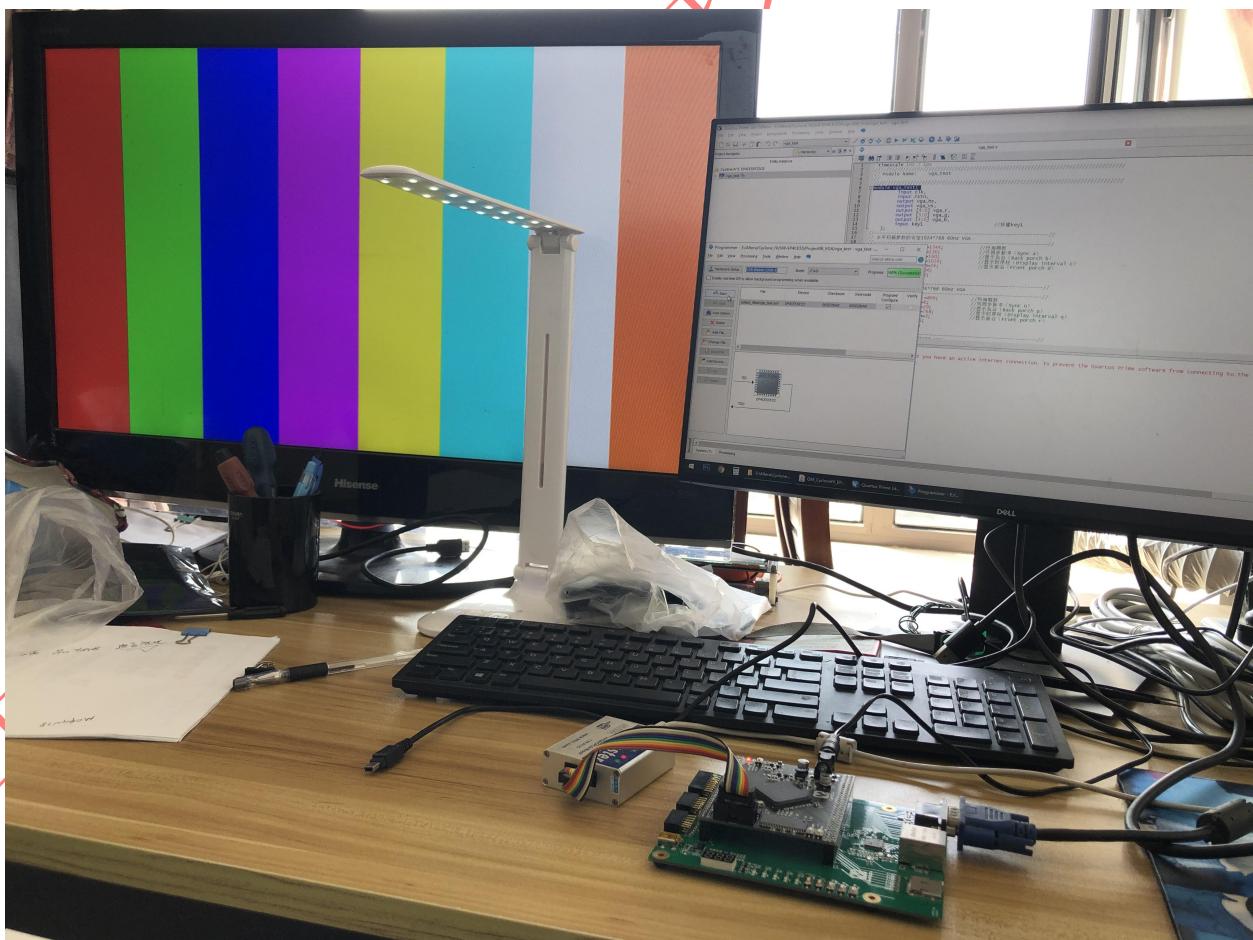


Figure 3-5. VGA Display Test

1. Experiment (3): GMII Ethernet Test

The daughter board uses RTL8211EG to implement the 10M/100M/1000M triple speed ethernet interface. It provides all the necessary physical layer functions to transmit and receive ethernet packets over the CAT.5 UTP cable. The data transfer between PHY and FPGA is via the Gigabit Media Independent Interface(GMII) for 1000Base-T. The RTL8211EG-VB chip supports 3.3V signaling for GMII interface. Below image shows the hardware design of TRL8211EG:

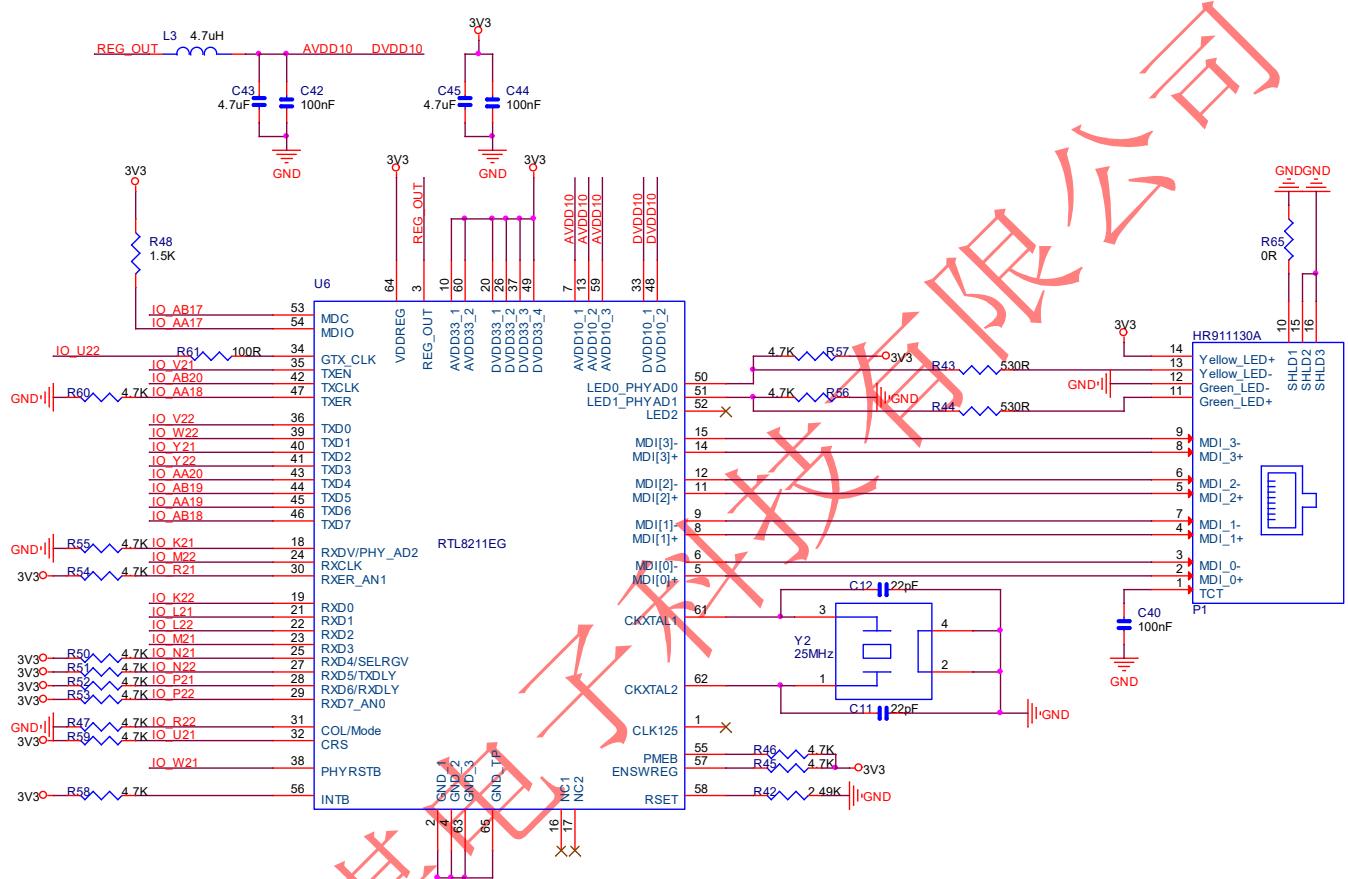


Figure 1-1. RTL8211 Hardware Design

Before start to test the GMII ethernet communication function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to QMTECH_CycloneIV_EP4CE55 core board's JTAG interface. The ethernet cable shall be plugged in the board and the test computer simultaneously. Then power on the development kit with 5V DC power source. Below figure shows an example hardware setup:





Figure 1-2. Test Setup

Use Quartus II 15.1 to open the GMII ethernet test project located in this release folder: /Software/Project09_GMII_Ethernet. Below figure shows the example project of **ethernet_test**:

The screenshot shows the Quartus Prime Standard Edition interface with the project "ethernet_test" open. The Project Navigator on the left lists the project files: Cyclone N/E EP4CE55F23C8N, ethernet_test, sd_hub_auto_hub, sd_signalap_auto_signalsAp_0, ramram_inst, and udpuf1. The main window displays the Verilog HDL code for the module "ethernet_test". The code defines a module with various inputs and outputs, including clock signals (e_fpga_clk, e_gtclk), reset signals (e_reset_n, e_ereset), and data paths for RX and TX. It also includes assignments for GTTXC and GTRESET. A note in the code indicates that GTTXC outputs a 125MHz clock. The code is annotated with comments in Chinese explaining specific parts like the 125MHz clock output.

```
timescale 1ns / 1ps
Module Name: ethernet_test
module ethernet_test(
    input reset_n,
    input fpga_clk,
    output e_reset,
    output [25:0] e_25 ASIC,
    output e_mdio,
    inout e_mdio,
    input e_rxck,
    input e_rxdv,
    input e_rxer,
    input [7:0] e_rxd,
    input e_txck,
    output e_gtxc,
    output e_txen,
    output e_txer,
    output [7:0] e_txd
);
    wire [31:0] ram_wr_data;
    wire [31:0] ram_rd_data;
    wire [8:0] ram_wr_addr;
    wire [8:0] ram_rd_addr;
    assign e_gtxc=e_rxck;
    assign e_reset = 0[6];
    wire [31:0] datain_reg;
    wire [31:0] dataout;

```



After the ethernet test project correctly synthesized, implemented and generated *.sof file, users could use Altera Quartus program tool to program the generated *.sof file into FPGA. Below image shows the FPGA program status with program tool.

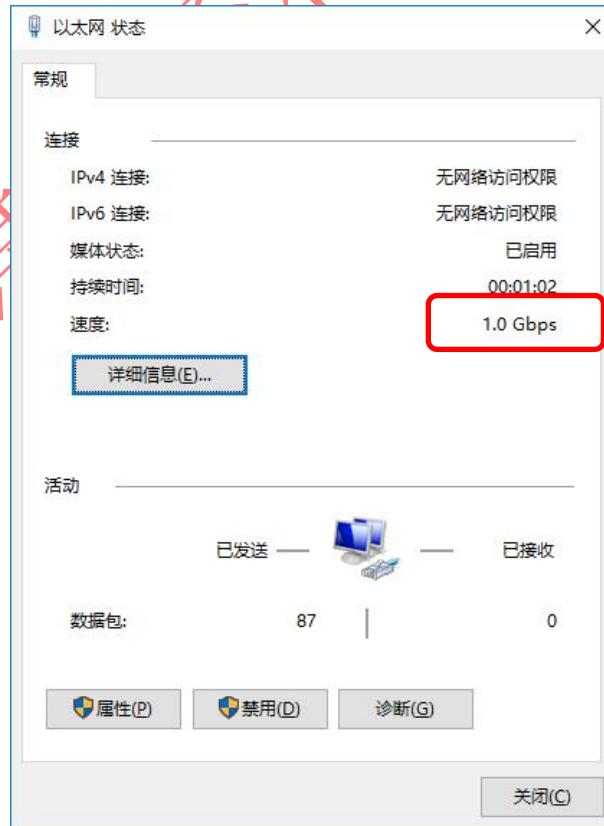
```

Quartus Prime Standard Edition - E:/Altera/Cyclone_IV/SW/Project09_GMII_Ethernet/ethernet_test - ethernet_test
File Edit View Project Assignments Processing Tools Window Help
Project Navigator Hierarchy Entity:instance
Cyclone IV E: EP4CE55F23C8N
ethernet_test
s1t_hub_auto_hub
sd1_signaltap:auto_signaltap_0
ramram_inst
udp1
Entity:instance
Module Name: ethernet_test
Module: ethernet_test
Reset: e_reset_n
Clock: fpga_oclk
Output: e_reset
Output: CLK_25 ASIC
Output: e_mdc
Input: e_mdio
Input: e_rxck
Input: e_rxck
Input: e_txer
Input: [7:0] e_rxd
// 125MHz ethernet gmii rx clock
Input: e_txck
Output: e_txck
// 25MHz ethernet mii tx clock
Output: e_txen
Output: e_txer
Output: [7:0] e_txd
);
wire [31:0] ram_wr_data;
wire [31:0] ram_rd_data;
wire [8:0] ram_wr_addr;
wire [8:0] ram_rd_addr;
assign e_gtxc=e_rxck; //gtxc输出125MHz的时钟
assign e_reset = 1'b1;
wire [31:0] datain_reg;
... (redacted)

```

Figure 1-3. FPGA Program

Users could check the ethernet connection status in the Windows OS. Below images shows the ethernet communication speed between the FPGA development board and the test computer is 1Gbps based.



In order to finish this ethernet test, users need to set the Windows's Static IP into 192.168.0.3:

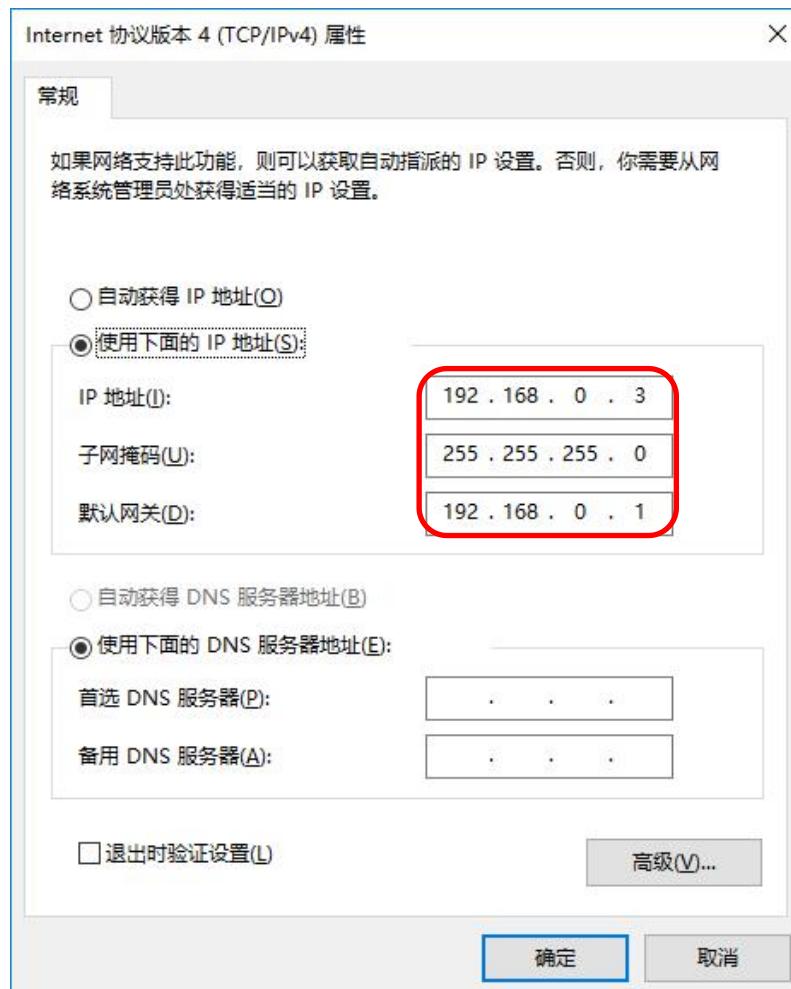


Figure 1-4. 配置电脑端 IP

Run Windows Command Console as administrator. In that DOS type command window bind the development board's IP address(192.168.0.2) and MAC address (00-0a-35-01-fe-c0) by typing command: ARP -s 192.168.0.2 00-0a-35-01-fe-c0:

The screenshot shows a Windows Command Prompt window titled '管理员: 命令提示符'. The command entered is:

```
C:\WINDOWS\system32>ARP -s 192.168.0.2 00-0a-35-01-fe-c0
```

Figure 1-5. Binding IP and MAC

Open the NetAssist ethernet debug tool and set the communication parameters as shown in below figure. Then press the 【Send】 button to send the test data <http://www.cmsoft.cn> QQ:10865600 to the FPGA development board. In response, the FPGA will send back test data "HELLO QMTECH BOARD" to the test PC.

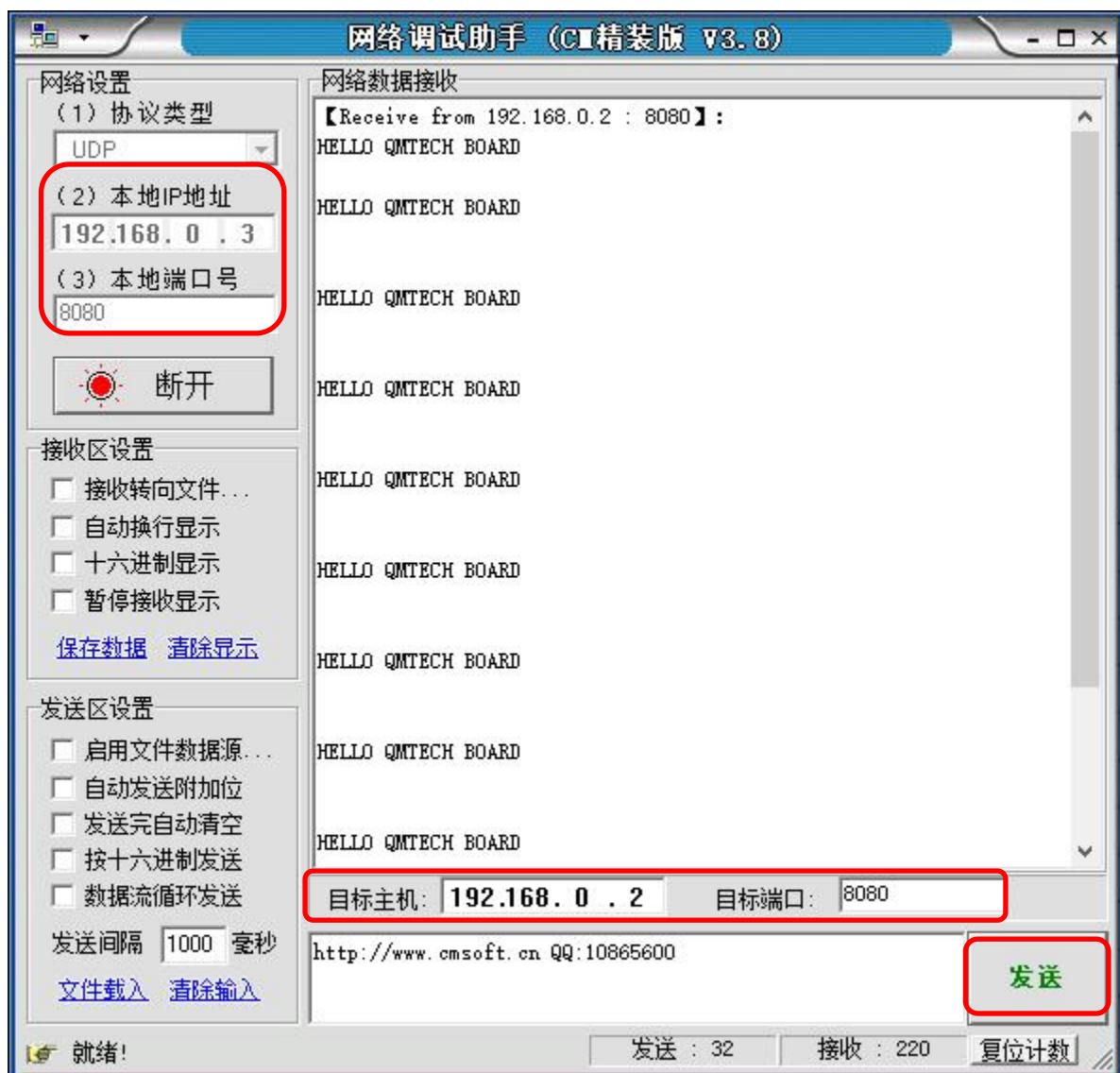


Figure 1-6. GMII Ethernet Test Result

2. Experiment (4): MicroSD Card Test

The daughter board provides a MicroSD slot to extend MicroSD or TF card. In this experiment, we uses 8GB Micro SDHC card provided by Kingston. The Micro SDHC card meets the specification of SD V2.0. Below image shows the hardware design of MicroSD slot:

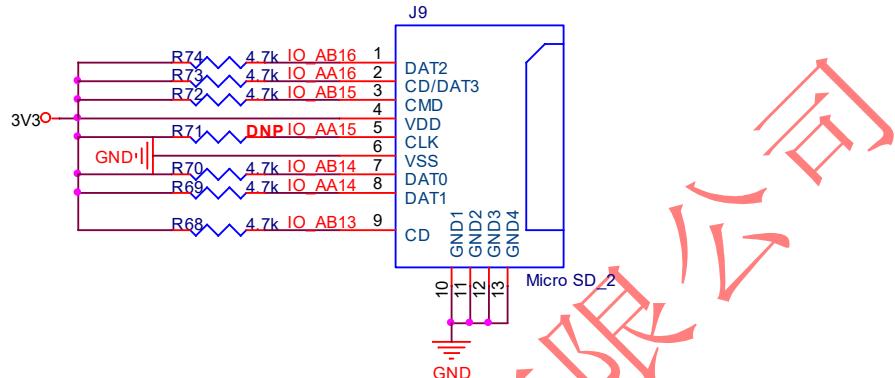


Figure 2-1. MicroSD Hardware Design

Before start to test the MicroSD read/write function, make sure all the hardware connections of the development kit are correctly connected. Altera USB Blaster's JTAG cable shall be connected to QMTECH_CycloneIV_EP4CE55 core board's JTAG interface. The Kinston 8 GB micro SD card shall be plugged in the board. Then power on the development kit with 5V DC power source. Below figure shows an example hardware setup:



Figure 2-2. Test Environment Setup

In this test example, the MicroSD card is working under SPI mode which could be easily handled by FPGA. SPI interface only has four wires: CS, MOSI, MISO, CLK. The clock frequency for the SPI interface is 25MHz which is divided by the on board 50MHz crystal directly. After Power-On, the MicroSD card enters SD mode and users need to send command to make the MicroSD switch to SPI mode. Then users need to follow the sequence shown in below figure to initialize the MicroSD card. Users may refer to the SD v2.0 spec for more details regarding to the Read and Write protocol.



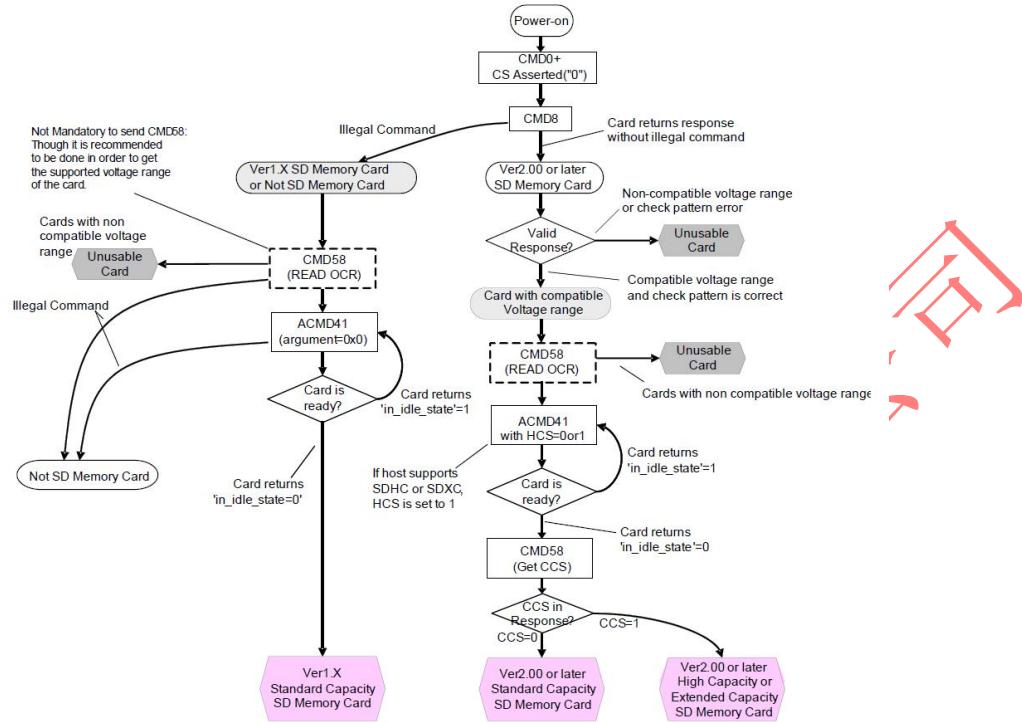
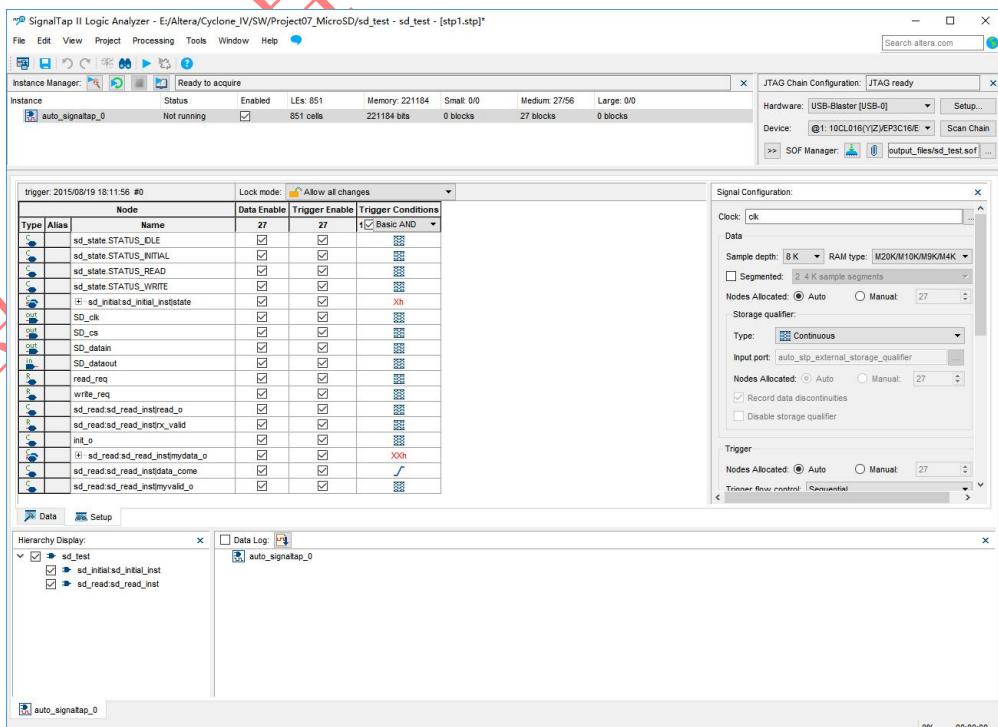


Figure 2-3. Initialize Sequence

After correctly initialized the MicroSD, the test program will write a batch of test data into the MicroSD card and then read back all these written value for further comparison. Here we use SignalTap to monitor these data transfer between the FPGA and the MicroSD card. Users may follow the SignalTap settings shown in below figure to observe the transactions. The sampling clock frequency is using on board 50MHz crystal and the trigger signal for sampling is data_come. When data_come goes high, there will be data comes from MicroSD card.



After the MicroSD test project correctly synthesized, implemented and generated *.sof file, users could use Altera Quartus SignalTap tool to program the generated *.sof file into FPGA. And then press the button SW2 on FPGA core board to trigger the test. After a short while, the SignalTap will stop capturing the data immediately after the data_come goes high. Then we can see the init_o is already in high status which means the MicroSD has already been correctly initialized. And the data signal mydata_o displays the data read out from MicroSD card.

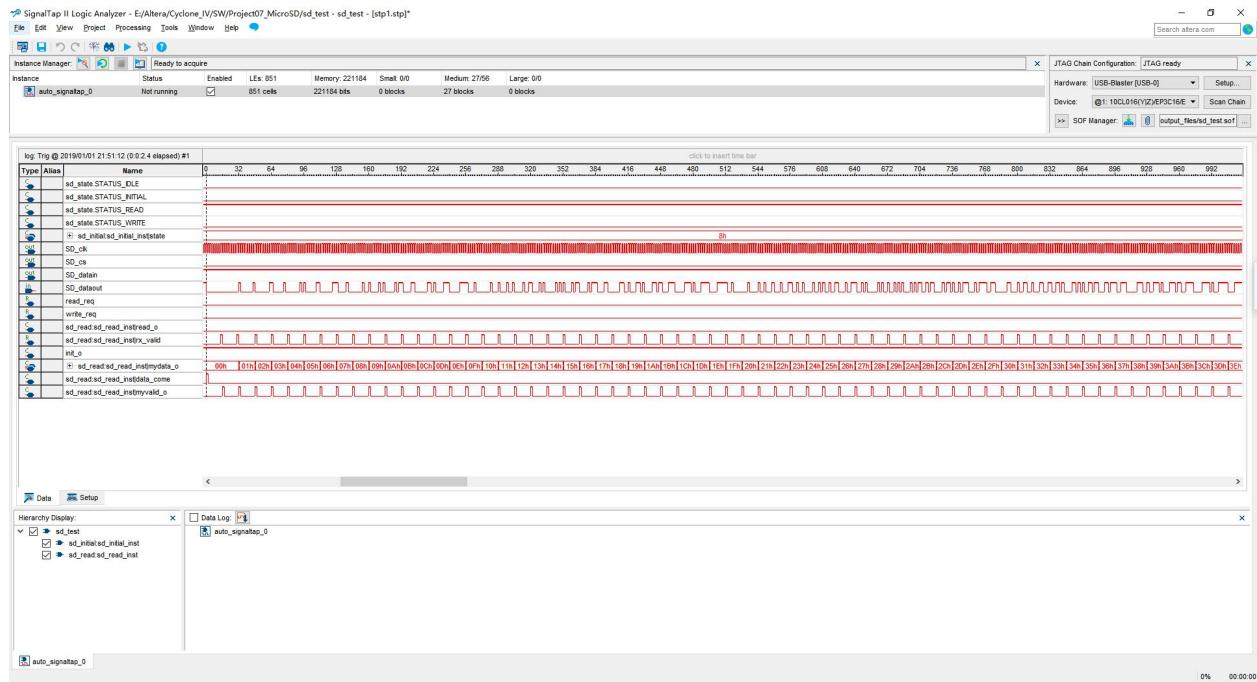


Figure 2-4. Data Write and Read Waveform

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3. Reference

- [1] ep4ce55f23-sdram.pdf
- [2] db-fpga-ep4ce55f23-v01.pdf
- [3] an592.pdf
- [4] an592_ch.pdf
- [5] cyiv-5v1.pdf
- [6] cyiv-5v2.pdf
- [7] cyiv-5v3.pdf
- [8] pcg-01008.pdf

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4. Revision

Doc. Rev.	Date	Comments
0.1	01/08/2020	Initial Version.
1.0	08/08/2020	V1.0 Formal Release.

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