SignalTap II Logic Analyzer Tutorial

INTRO:

The SignalTap Logic Analyzer allows you to probe signals inside of the fpga so you can view the waveforms. This allows you to debug your hardware. This is especially useful when you run into the situation where your mapped design works in simulation but not on the fpga.

Quartus File types:
.qpf – Quartus II Project File (Contains your project configurations)
.sof – SRAM object File (Contains your design that gets loaded onto the FPGA)
.hex – Hexadecimal Intel-Format File (Contains the program you want to run on your processor)
.stp – SignalTap II Logic Analyzer File (Contains your signal tap configuration information)

SETUP:

Navigate to your processors directory
Make a directory named “quartus_projects”
Run the command “quartus” from your processors directory
The Quartus II window will appear

SETTING UP YOUR QUARTUS PROJECT:

Click “File->New Project Wizard...”

Directory, Name, Top-Level Entity
Assign the project to your “quartus_projects” directory
Name your project “singlecycle”
Click “Next”

Add Files
Navigate to your “source” and “include” directories and add all your files
Click “User Libraries...” at the bottom of the window
Click “...” next to “Project library name:”
Navigate to your “include” directory and click “Add”, Click “OK”
Click “Next”

Family & Device Settings
For “Family” Choose “Cyclone IV E”
Choose “Specify device selected in 'Available devices' list”
Under “Available Devices”, choose “EP4CE115F29C7”
Click “Finish”

SETTING UP THE TOP LEVEL:

Under “Project Navigator” select “Files”

Right click on "../source/system_fpga.sv" and choose "Set as Top Level Entity"
On the navigation bar, choose "Assignments->Import Assignments"
Navigate to :
"/package/eda/altera/altera13.0sp1/University_Program/NiosII_Computer_Systems/DE2-115/DE2-115_Basic_Computer/verilog"
Choose the file "DE2_115_Basic_Computer.qsf"
Click "Open"
Click "OK"

BUILDING THE TOP LEVEL:

Click the purple play button at the top of the window

LOADING YOUR DESIGN ON THE FPGA:

In the navigation bar click "Tools->Programmer"
Click "Add File..." and choose "ouptut_files/singlecycle.sof"
Click "Start"

SETTING UP THE LOGIC ANALYZER:

In the navigation bar, choose "Tools->SignalTap II Logic Analyzer"

Under JTAG Chain Configuration, choose "Setup..." and double click "USB-Blaster"
Click "Close"

In the "setup" tab of the main window, double click to add nodes
Click "List" and select the signals you want. (Be sure to add the nRST signal)
Click ">" to add your selected signals
Note: After adding signals you may group them together to form a bus
Click "OK"

Right Click on the "trigger conditions" box for the signal nRST and choose the signal low selectioin (0 with a line under it) – this prevents the signal acquisition from stopping while you hold nRST low
Right Click on the "trigger conditions" box for your other signals and choose the rising or falling edge selection.

In the Signal Configuration Window:
Next to "Clock" click "..."
Click "List" and choose "CLOCK_50"
Click ">" and "OK"

In the navigation bar, choose "File->save"
Name the file "singlecycle.stp"
Click "Yes" when prompted to enable the file for the current project.

Leaving your SignalTap window open, recompile your design in the main window and re-load your design on the fpga.

Now you can Click the purple play button at the top of the SignalTap window to begin signal acquisition.

LOADING YOUR PROGRAM INTO MEMORY:

In the navigation bar of the main quartus window choose “Tools->In-System Memory Content Editor”
Under JTAG Chain Configuration, choose “USB-Blaster” for the Hardware field.
You should see your RAM filled with “?”

Right click in the box that displays your RAM data and choose “Import data from file...”
Select your “meminit.hex” file in your processors directory.

Load the data into memory by clicking the write data to In-System Memory button (looks like a sheet of paper with an arrow pointing down)

This will load the fpga's ram with your program.

PUTTING IT ALL TOGETHER

To see the signals from your design, you need to:

1. Hold nRST low on the board (KEY3).
2. Load the program into your RAM via the In-System Memory Editor
3. Click the “Run Analysis” button in the signal tap logic analyzer window (purple play button)
4. Release the nRST

Your Design will operate on the memory and when the signal tap logic notices that your signals are no longer changing, it will stop the acquisition. You can view your signals by selecting the “Data” tab in the SignalTap Logic Analyzer window.