**R32V2020 Peripheral Memory Map**

**2019-08-26**

|  |  |
| --- | --- |
| **Address Range** | **Description** |
| x0000-x07FF (2KB) | VGA Display |
| x0800-x0FFF (2KB) | Keyboard Data (Latched) |
| x1000-x17FF (2KB) | Keyboard Status (of Latched) |
| x1800-x1FFF (2KB) | UART (6850 ACIA) |
| x2000-x27FF (2KB) | Pushbutton Switches |
| x2800-x2FFF (2KB) | Individual LEDs |
| x3000-x37FF (2KB) | Seven Segment Display (4 or 8 digits) |
| x3800-x3FFF (2KB) | Timers |
| x4000-x47FF (2KB) | Music/Note |
| x4800-x4FFF (2KB) | LED Ring |
| x5000-x57FF (2KB) | I/O Latch |
| x5800-x5FFF (2KB) | External I2C Address |
| x6000-x67FF (2KB) | SPI Address |
| x6800-x6FFF (2KB) | EEPROM I2C Address |
| X7000-x77ff (2KB) | Keyboard (Polled) |
|  |  |
|  |  |

**Board Specific Data**

* [Land Boards RETRO-EP4 Board](http://land-boards.com/blwiki/index.php?title=RETRO-EP4CE6)
* [Land Boards EP2C5-DB Board](http://land-boards.com/blwiki/index.php?title=EP2C5-DB)
* [ZrTech v2.00 EP4CE6 Board](http://land-boards.com/blwiki/index.php?title=ZrTech_V2_EP4CE6_Cyclone_IV_FPGA_EP4CE6E22C8N_Development_Board_USB_V2)
* [A-C4E6 Board](http://land-boards.com/blwiki/index.php?title=A-C4E6_Cyclone_IV_FPGA_EP4CE6E22C8N_Development_Board)
* [A-C4E10 Board](http://land-boards.com/blwiki/index.php?title=A-C4E10_Cyclone_IV_FPGA_EP4CE10E22C8N_Development_Board)
* [A-ESTF V2 EP4CE22 Board](http://land-boards.com/blwiki/index.php?title=A-ESTF_V2_EP4CE22_Board)

**Features Matrix**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Board** | **VGA (r/g/b)** | **Pushbutton/ DIP Sw** | **LEDs** | **7 Seg Disp** | **Speaker/ Buzzer** | **EEPROM** |
| RETRO-EP4 | 2/2/2 | 2/0 | 4 | None | None |  |
| EP2C5-DB | 2/2/2 | None | 1 | None | None |  |
| ZrTech 2.00 | 5/6/5 | 4 |  | 4-digit | Speaker |  |
| A4-CE6 | 1/1/1 | 4 | 12 – Ring | 8-digit | Buzzer | AT24C04 |
| A4-CE6 | 1/1/1 | 4 | 12 - Ring | 8-digit | Buzzer | AT24C04 |
| A-ESTF | 5/6/6 | 3x3 PBs(K1-9) 4 PBs 8 DIP | 8x8 matrix | 8-digit | Not sure | AT24C04 |
|  |  |  |  |  |  |  |

**VGA Display**

* Character interface
* 80 rows, 25 lines
* Support ANSI escape sequences from Grant Searle’s Multicomp
  + <http://searle.hostei.com/grant/Multicomp/index.html#ANSICodes>
* 6 bits of color (64 colors) supported
  + Normal/bold colors
* Color support varies by FPGA card (wiring to VGA resistor networks)
  + RETRO-EP4
    - 6 bits color (2/2/2)
  + A4-CE6, A4-CE10
    - 3 bits color (1/1/1)
  + ZR Tech
    - Hardware has 16 bits color (5/6/5)
    - R32V2020 only supports 6 bits

**Keyboard Data**

* ANSI conversion table
* PS/2 Keyboard connector is present on all hardware
* 8-bits data

**Keyboard Status**

* D0 - Data valid
  + 1 = Data valid
    - Cleared by read of Keyboard Data
  + 0 – No data present

**UART (6850 ACIA)**

* Programmed via the 6850 ACIA interface
  + Control/Status Register
  + Read/Write data register
* A4-CE6, A4-CE10, ZrTech boards
  + Connects to USB to Serial interface
* RETRO-EP4 board
  + Connects to on-board FTDI Interface adapter
* EP2C5-DB board
  + 4-pin RX/TX/RTS/GND connector
    - Attach via serial cable to FTDI USB-TTL adapter

**Pushbutton Switches/DIP switches**

* Not all FPGA cards have pushbuttons and/or DIP switches
* Pushbutton switches and DIP switches are packed into 16-bit read value
  + D0-D2 = Pushbuttons
  + D3 = 0
  + D4-D11 = DIP switches
* (3) Pushbutton switches are de-bounced in hardware
* DIP Switches are not de-bounced in hardware
* Value of bits
  + 0 = Button pressed
  + 1 = Button not pressed
* Reset pushbutton can’t be read
  + Reset function activates when button is released
* A4-CE6, A4-CE10 boards
  + One pushbutton (K5) resets the CPU
  + Three readable pushbuttons
  + 8 position DIP switch
* RETRO-EP4 board
  + Reset and nCONFIG (not readable)
  + No pushbutton or DIP switches
* ZrTech board
  + Reset and 3 general purpose pushbutton switches

**Individual LEDs**

* Not all FPGA cards have LEDs

**Seven Segment Display**

* 32-bit data register

**Timers**

* Four Timers
* 32-bit data
* Read-Only
* Addresses

|  |  |
| --- | --- |
| Address | Timer |
| X3800 | Elapsed Time Counter   * FPGA clocks * Typically 50 MHz ticks (20 nS) |
| X3801 | MicroSeconds Counter |
| X3802 | Milliseconds Counter |
| X3803 | CPU Instruction Counter |

* Determine time by reading counter and then re-reading counter.

**Music/Note**