



# MICROCHIP 24AA024/24LC024/24AA025/24LC025

## 2K I<sup>2</sup>C™ Serial EEPROM

### Device Selection Table

Part Number	Vcc Range	Max Clock	Temp. Range	Write Protect
24AA024	1.8V - 5.5V	400 KHz <sup>(1)</sup>	I	Yes
24AA025	1.8V - 5.5V	400 KHz <sup>(1)</sup>	I	No
24LC024	2.5V - 5.5V	400 KHz	I	Yes
24LC025	2.5V - 5.5V	400 KHz	I	No

**Note 1:** 100 KHz for Vcc < 2.5V

### Features

- Single supply with operation from 1.8V to 5.5V
- Low-power CMOS technology
  - 1 mA active current typical
  - 1  $\mu$ A standby current typical at 5.5V
- Organized as a single block of 256 bytes (256 x 8)
- Hardware write protection for entire array (24XX024)
- 2-wire serial interface bus, I<sup>2</sup>C™ compatible
- 100 kHz and 400 kHz clock compatibility
- Page write buffer for up to 16 bytes
- Self-timed write cycle (including auto-erase)
- 10 ms max. write cycle time
- Address lines allow up to eight devices on bus
- 1,000,000 erase/write cycles
- ESD protection > 4,000V
- Data retention > 200 years
- 8-pin PDIP, SOIC, TSSOP and MSOP packages
  - Industrial (I): -40°C to +85°C

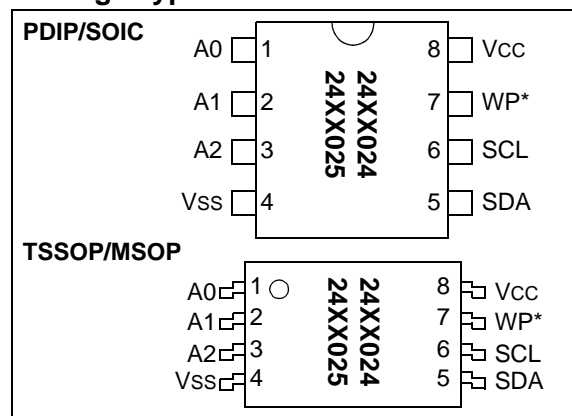
### Pin Function Table

Name	Function
Vss	Ground
SDA	Serial Data
SCL	Serial Clock
Vcc	1.8V to 5.5V Power Supply
A0, A1, A2	Chip Selects
WP	Hardware Write-Protect (24LC024)

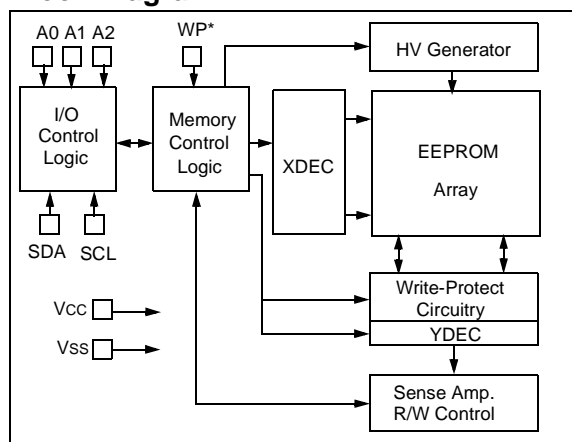
### Description

The Microchip Technology Inc. 24AA024/24LC024/24AA025/24LC025 is a 2 Kbit Serial Electrically Erasable PROM with a voltage range of 1.8V to 5.5V. The device is organized as a single block of 256 x 8-bit memory with a 2-wire serial interface. Low current design permits operation with typical standby and active currents of only 1  $\mu$ A and 1 mA, respectively. The device has a page write capability for up to 16 bytes of data. Functional address lines allow the connection of up to eight 24AA024/24LC024/24AA025/24LC025 devices on the same bus for up to 16K bits of contiguous EEPROM memory. The device is available in the standard 8-pin PDIP, 8-pin SOIC (150 mil), TSSOP and MSOP packages.

### Package Types



### Block Diagram



**Note:** \*WP pin available only on 24XX024. This pin has no internal connection on 24XX025.

# 24AA024/24LC024/24AA025/24LC025

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings <sup>(†)</sup>

V <sub>CC</sub> .....	6.5V
All inputs and outputs w.r.t. V <sub>SS</sub> .....	-0.6V to V <sub>CC</sub> +1.0V
Storage temperature .....	-65°C to +150°C
Ambient temperature with power applied.....	-40°C to +125°C
ESD protection on all pins .....	≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

<b>All parameters apply across the specified operating ranges unless otherwise noted.</b>		V <sub>CC</sub> = 1.8V to 5.5V Industrial (I): T <sub>A</sub> = -40°C to +85°C			
Parameter	Symbol	Min.	Max.	Units	Conditions
SCL and SDA pins:					
High-level input voltage	V <sub>IH</sub>	0.7 V <sub>CC</sub>	—	V	—
Low-level input voltage	V <sub>IL</sub>	—	0.3 V <sub>CC</sub>	V	—
Hysteresis of Schmitt Trigger inputs	V <sub>HYS</sub>	0.05 V <sub>CC</sub>	—	V	<b>(Note)</b>
Low-level output voltage	V <sub>OL</sub>	—	0.40	V	I <sub>OL</sub> = 3.0 mA, V <sub>CC</sub> = 4.5V I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.5V
Input leakage current	I <sub>LI</sub>	—	±1	μA	V <sub>IN</sub> = 0.1V to 5.5V, WP = V <sub>SS</sub>
Output leakage current	I <sub>LO</sub>	—	±1	μA	V <sub>OUT</sub> = 0.1V to 5.5V
Pin capacitance (all inputs/outputs)	C <sub>IN</sub> , C <sub>OUT</sub>	—	10	pF	V <sub>CC</sub> = 5.0V <b>(Note)</b> T <sub>A</sub> = 25°C, f = 1 MHz
Operating current	I <sub>CC</sub> Read	—	1	mA	V <sub>CC</sub> = 5.5V, SCL = 400 kHz
	I <sub>CC</sub> Write	—	3	mA	V <sub>CC</sub> = 5.5V
Standby current	I <sub>CCS</sub>	—	1	μA	V <sub>CC</sub> = 5.5V, SDA = SCL = V <sub>CC</sub> WP = V <sub>SS</sub> , A0, A1, A2 = V <sub>SS</sub>

**Note:** This parameter is periodically sampled and not 100% tested.

# 24AA024/24LC024/24AA025/24LC025

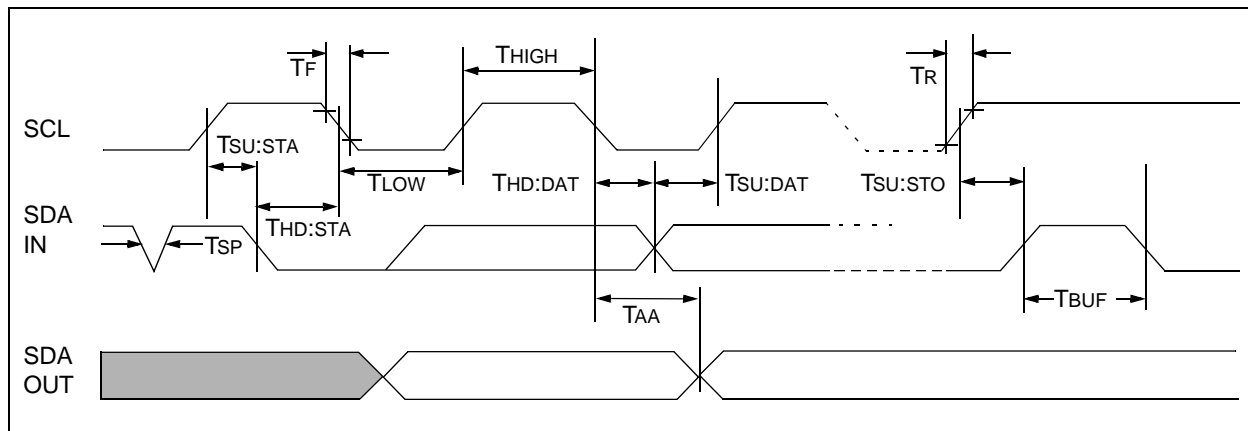
**TABLE 1-2: AC CHARACTERISTICS**

All parameters apply across the specified operating ranges unless otherwise noted.				V <sub>CC</sub> = 1.8V to 5.5V Industrial (I): T <sub>A</sub> = -40°C to +85°C		
Parameter	Symbol	STD MODE		V <sub>CC</sub> = 2.5V - 5.5V FAST MODE		Units
		Min.	Max.	Min.	Max.	
Clock frequency	FCLK	—	100	—	400	kHz
Clock high time	T <sub>HIGH</sub>	4000	—	600	—	ns
Clock low time	T <sub>LOW</sub>	4700	—	1300	—	ns
SDA and SCL rise time	T <sub>R</sub>	—	1000	—	300	ns
SDA and SCL fall time	T <sub>F</sub>	—	300	—	300	ns
Start condition hold time	T <sub>HD:STA</sub>	4000	—	600	—	ns
Start condition setup time	T <sub>SU:STA</sub>	4700	—	600	—	ns
Data input hold time	T <sub>HD:DAT</sub>	0	—	0	—	ns
Data input setup time	T <sub>SU:DAT</sub>	250	—	100	—	ns
Stop condition setup time	T <sub>SU:STO</sub>	4000	—	600	—	ns
Output valid from clock	T <sub>AA</sub>	—	3500	—	900	ns
Bus free time	T <sub>BUF</sub>	4700	—	1300	—	ns
Output fall time from V <sub>IH</sub> minimum to V <sub>IL</sub> maximum	T <sub>OF</sub>	—	250	20 + 0.1 C <sub>B</sub>	250	ns
Input filter spike suppression (SDA and SCL pins)	T <sub>SP</sub>	—	50	—	50	ns
Write-cycle time	T <sub>WC</sub>	—	10	—	10	ms
Endurance		1M	—	1M	—	cycles

**Note 1:** Not 100% tested. C<sub>B</sub> = total capacitance of one bus line in pF.

- As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- The combined T<sub>SP</sub> and V<sub>HYS</sub> specifications are due to Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T<sub>I</sub> specification for standard operation.
- This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be downloaded at [www.microchip.com](http://www.microchip.com).

**FIGURE 1-1: BUS TIMING DATA**



## 2.0 PIN DESCRIPTIONS

### 2.1 SDA Serial Data

SDA is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10 k $\Omega$  for 100 kHz, 2 k $\Omega$  for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

### 2.2 SCL Serial Clock

The SCL input is used to synchronize the data transfer from and to the device.

### 2.3 A0, A1, A2

The levels on the A0, A1 and A2 inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24AA024/24LC024/24AA025/24LC025 devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either Vcc or Vss.

### 2.4 WP (24XX024 Only)

WP is the hardware write-protect pin. It must be tied to Vcc or Vss. If tied to Vcc, hardware write protection is enabled. If WP is tied to Vss, the hardware write protection is disabled. Note that the WP pin is available only on the 24XX024. This pin is not internally connected on the 24LC025.

### 2.5 Noise Protection

The 24AA024/24LC024/24AA025/24LC025 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

## 3.0 FUNCTIONAL DESCRIPTION

The 24AA024/24LC024/24AA025/24LC025 supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24AA024/24LC024/24AA025/24LC025 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

## 4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

### 4.1 Bus Not Busy (A)

Both data and clock lines remain high.

### 4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

### 4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

### 4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited, (though only the last sixteen will be stored when performing a write operation). When an overwrite does occur, it will replace data in a first-in first-out fashion.

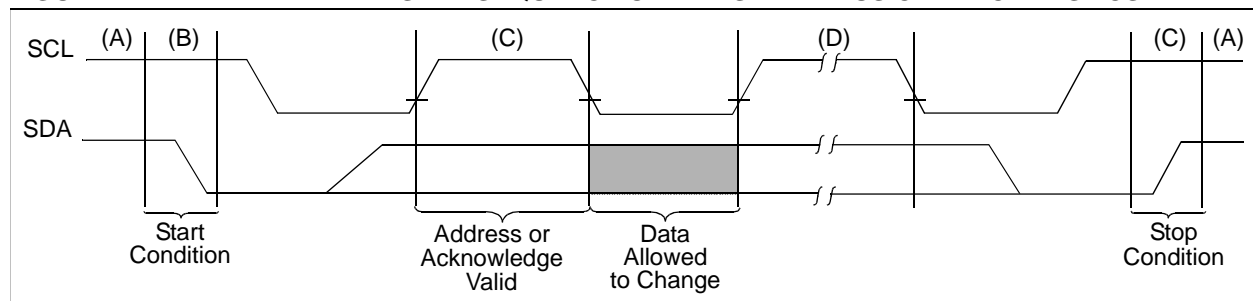
### 4.5 Acknowledge

Each receiving device, when addressed, is required to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

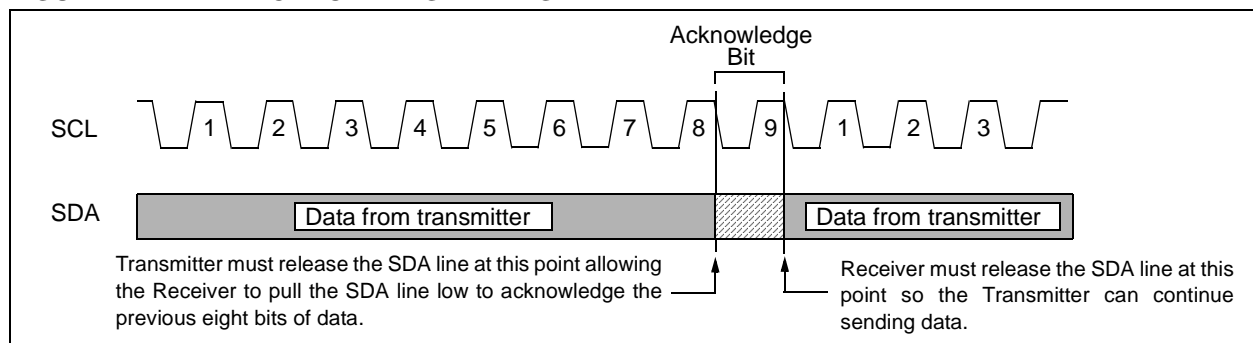
**Note:** The 24AA024/24LC024/24AA025/24LC025 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition (Figure 4-2).

**FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS CHARACTERISTICS**



**FIGURE 4-2: ACKNOWLEDGE TIMING**



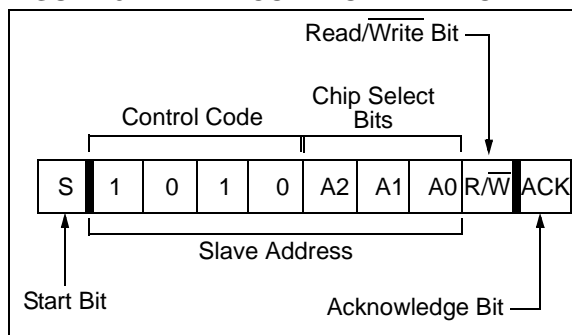
# 24AA024/24LC024/24AA025/24LC025

## 5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the master device (Figure 5-1). The control byte consists of a four-bit control code. For the 24AA024/24LC024/24AA025/24LC025, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24AA024/24LC024/24AA025/24LC025 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a one, a read operation is selected. When set to a zero, a write operation is selected. Following the Start condition, the 24AA024/24LC024/24AA025/24LC025 monitors the SDA bus checking the control byte being transmitted. Upon receiving a '1010' code and appropriate Chip Select bits, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24AA024/24LC024/24AA025/24LC025 will select a read or write operation.

FIGURE 5-1: CONTROL BYTE FORMAT



## 5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24AA024/24LC024/24AA025/24LC025 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9 and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

## 6.0 WRITE OPERATIONS

### 6.1 Byte Write

Following the Start signal from the master, the device code (4 bits), the Chip Select bits (3 bits) and the R/W bit (which is a logic-low) is placed onto the bus by the master transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the master is the word address and will be written into the address pointer of the 24AA024/24LC024/24AA025/24LC025. After receiving another Acknowledge signal from the 24AA024/24LC024/24AA025/24LC025, the master device will transmit the data word to be written into the addressed memory location. The 24AA024/24LC024/24AA025/24LC025 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and, during this time, the 24AA024/24LC024/24AA025/24LC025 will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection (24XX024 only) has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if write protection is enabled.

### 6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24AA024/24LC024/24AA025/24LC025 in the same way as in a byte write. However, instead of generating a Stop condition, the master transmits up to 15 additional data bytes to the 24AA024/24LC024/24AA025/24LC025, which are temporarily stored in the on-chip page buffer and will be written into the memory once the master has transmitted a Stop condition. Upon receipt of each word, the four lower-order address pointer bits are internally incremented by one.

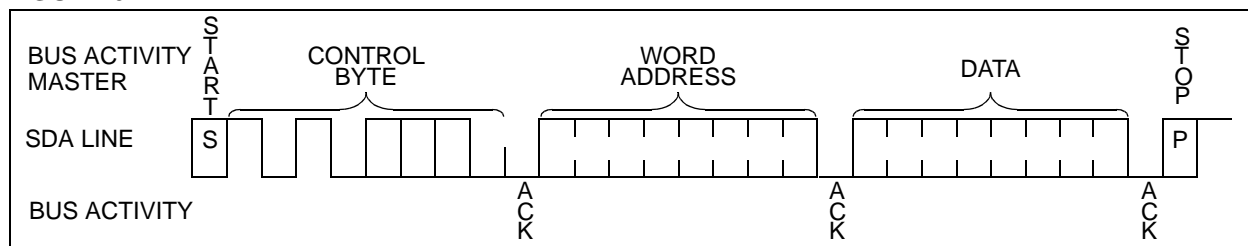
The higher-order four bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte-write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if write protection is enabled.

**Note:** Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of [page size - 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

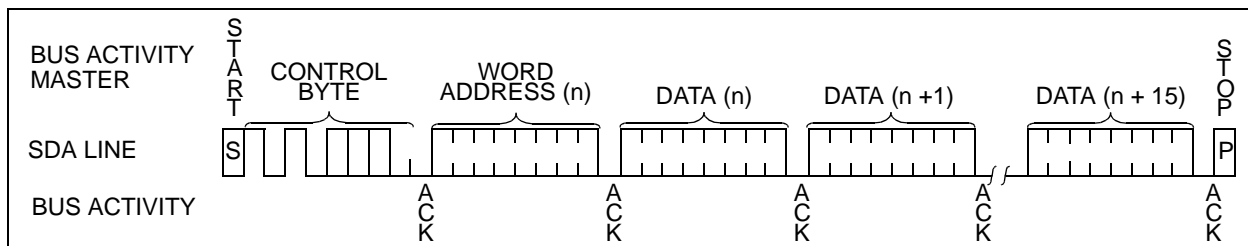
### 6.3 Write Protection

The WP pin (available on 24XX024 only) must be tied to VCC or VSS. If tied to VCC, the entire array will be write-protected. If the WP pin is tied to VSS, write operations to all address locations are allowed.

**FIGURE 6-1: BYTE WRITE**



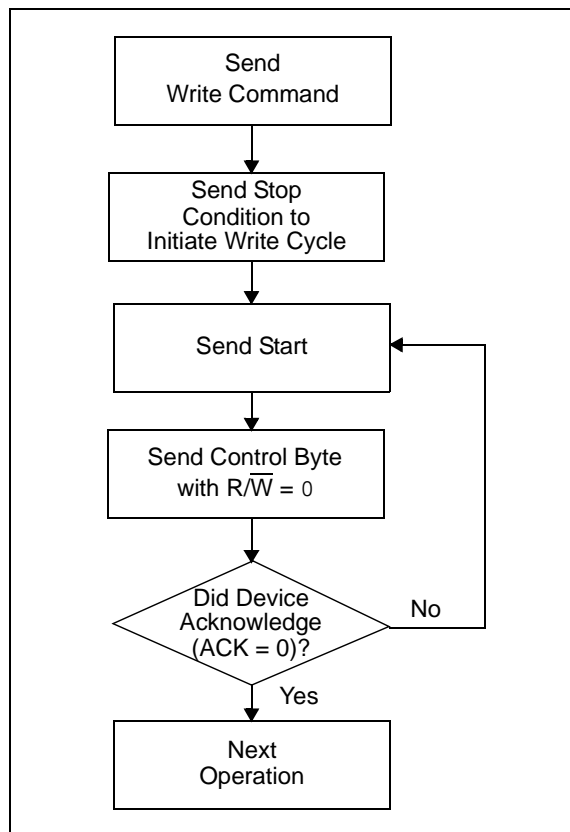
**FIGURE 6-2: PAGE WRITE**



## 7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally-timed write cycle, with ACK polling being initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command ( $R/\overline{W} = 0$ ). If the device is still busy with the write cycle, no ACK will be returned. If no ACK is returned, the Start bit and control byte must be re-sent. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 7-1 for a flow diagram of this operation.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW





## 8.0 READ OPERATIONS

Read operations are initiated in the same way as write operations, with the exception that the  $\overline{R/\overline{W}}$  bit of the slave address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 8.1 Current Address Read

The 24AA024/24LC024/24AA025/24LC025 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address  $n$ , the next current address read operation would access data from address  $n + 1$ . Upon receipt of the slave address with the  $\overline{R/\overline{W}}$  bit set to '1', the 24AA024/24LC024/24AA025/24LC025 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24AA024/24LC024/24AA025/24LC025 discontinues transmission (Figure 8-1).

### 8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24AA024/24LC024/24AA025/24LC025 as part of a write operation. Once the word address is

sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. The master then issues the control byte again, but with the  $\overline{R/\overline{W}}$  bit set to a '1'. The 24AA024/24LC024/24AA025/24LC025 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24AA024/24LC024/24AA025/24LC025 discontinues transmission (Figure 8-2). After this command, the internal address counter will point to the address location following the one that was just read.

### 8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24AA024/24LC024/24AA025/24LC025 transmits the first data byte, the master issues an acknowledge (as opposed to a Stop condition in a random read). This directs the 24AA024/24LC024/24AA025/24LC025 to transmit the next sequentially-addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24AA024/24LC024/24AA025/24LC025 contains an internal address pointer that is incremented by one upon completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation. The internal address pointer will automatically roll over from address 0FFh to address 000h.

**FIGURE 8-1: CURRENT ADDRESS READ**

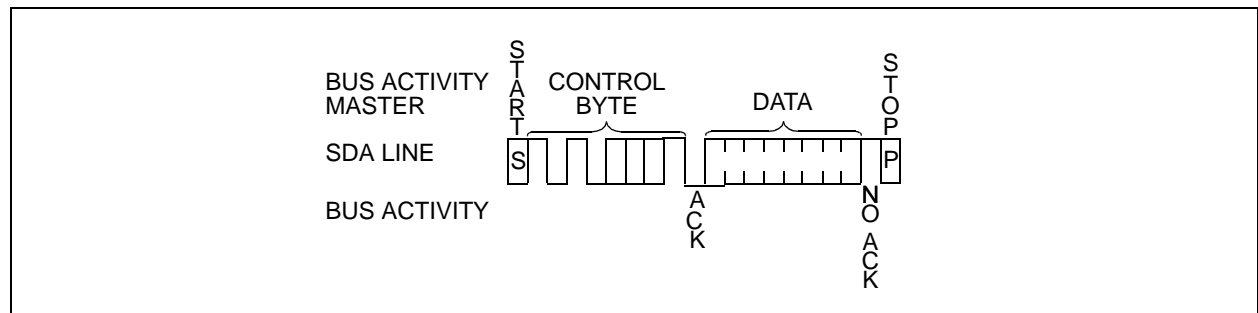


FIGURE 8-2: RANDOM READ

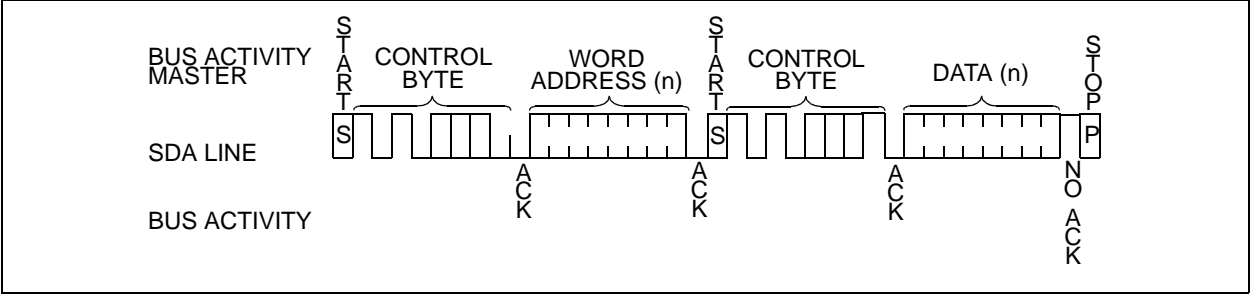
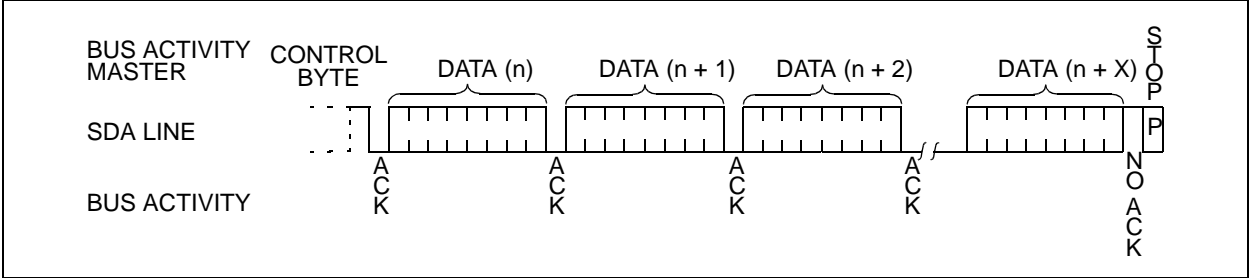


FIGURE 8-3: SEQUENTIAL READ

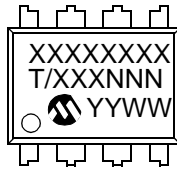


# 24AA024/24LC024/24AA025/24LC025

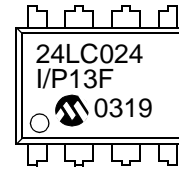
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

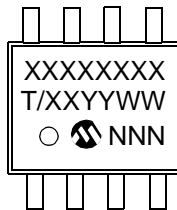
8-Lead PDIP (300 mil)



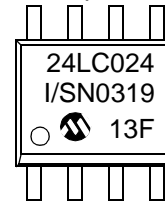
Example:



8-Lead SOIC (150 mil)



Example:

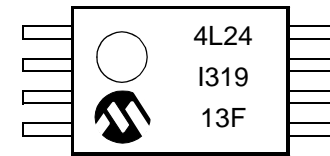


8-Lead TSSOP

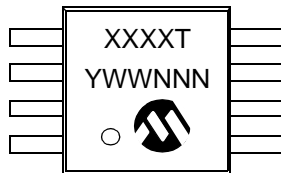


Part Number	TSSOP Marking Code
24AA024	4A24
24LC024	L24
24AA025	4A25
24LC025	L25

Example:

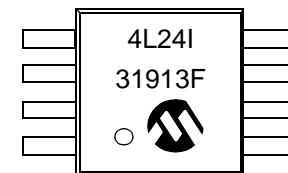


8-Lead MSOP



Part Number	MSOP Marking Code
24AA024	4A24I
24LC024	4L24I
24AA025	4A25I
24LC025	4L25I

Example:



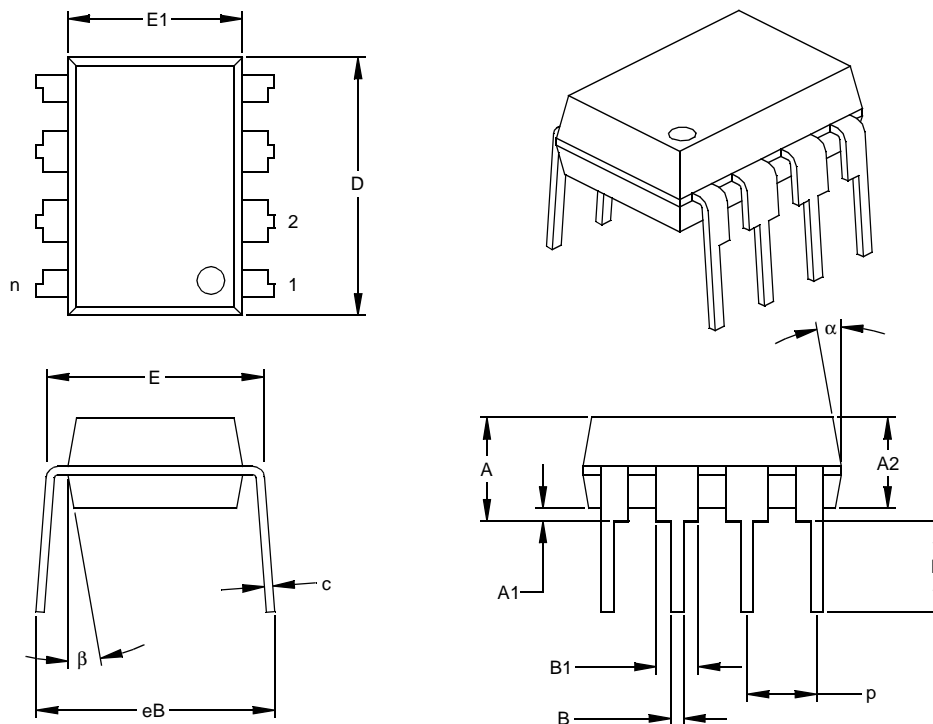
<b>Legend:</b>	XX...X	Customer specific information*
	T	Temperature grade
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

\* Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

# 24AA024/24LC024/24AA025/24LC025

## 8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter

§ Significant Characteristic

### Notes:

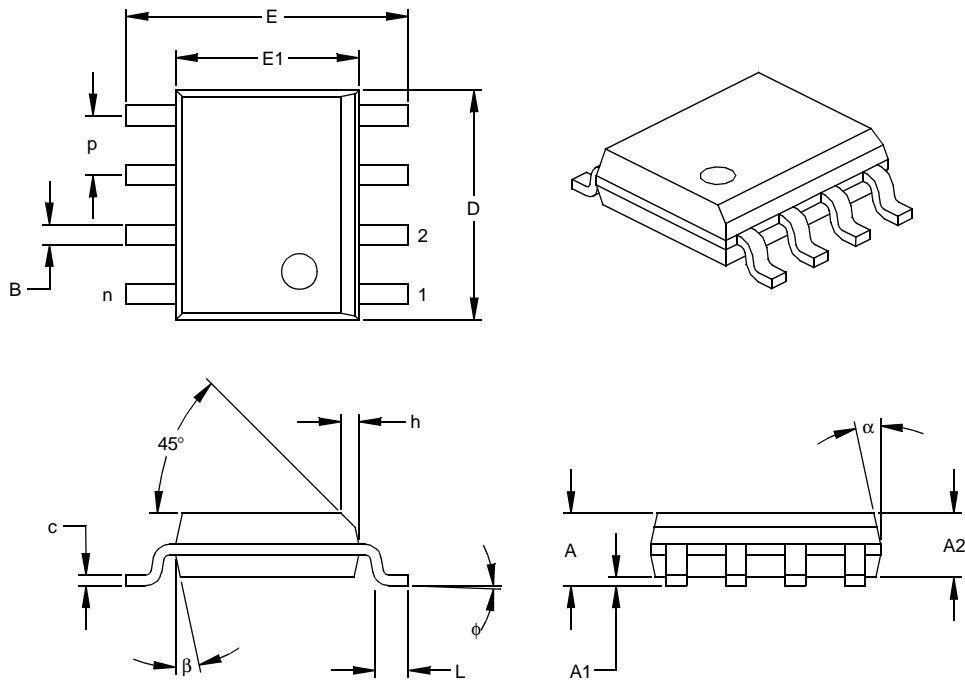
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

# 24AA024/24LC024/24AA025/24LC025

## 8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter  
§ Significant Characteristic

### Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

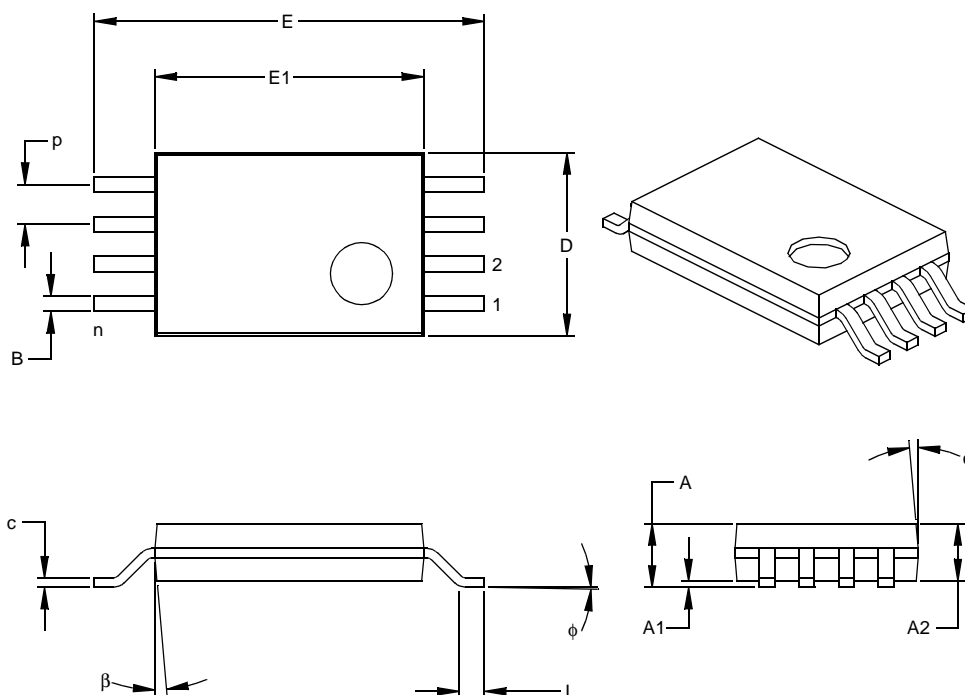
.010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

# 24AA024/24LC024/24AA025/24LC025

## 8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\* Controlling Parameter

§ Significant Characteristic

### Notes:

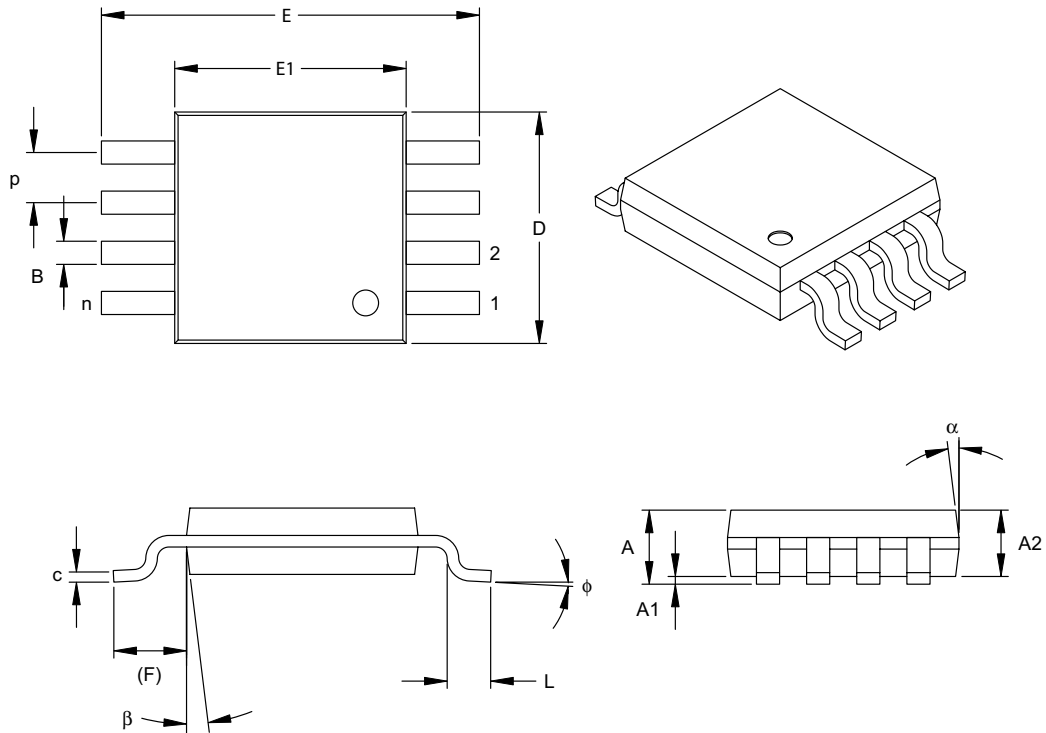
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-086

# 24AA024/24LC024/24AA025/24LC025

## 8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	P	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 TYP.			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	$\phi$	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	$\alpha$	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	$\beta$	5°	-	15°	5°	-	15°

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

## APPENDIX A: REVISION HISTORY

### Revision F

Corrections to Section 1.0, Electrical Characteristics.

### Revision G

Added part number 24AA025 to document.

Correction to Section 1.0, Ambient Temperature.



## ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

### Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

**[www.microchip.com](http://www.microchip.com)**

The file transfer site is available by using an FTP service to connect to:

**<ftp://ftp.microchip.com>**

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

## SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

042003

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager  
RE: Reader Response  
Total Pages Sent \_\_\_\_\_  
From: Name \_\_\_\_\_  
Company \_\_\_\_\_  
Address \_\_\_\_\_  
City / State / ZIP / Country \_\_\_\_\_  
Telephone: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_ FAX: (\_\_\_\_\_) \_\_\_\_\_ - \_\_\_\_\_

Application (optional):

Would you like a reply? \_\_\_Y \_\_\_N

Device: 24AA024/24LC024/24AA025/24LC025

Literature Number: DS21210G

Questions:

1. What are the best features of this document?

---

---

2. How does this document meet your hardware and software development needs?

---

---

3. Do you find the organization of this document easy to follow? If not, why?

---

---

4. What additions to the document do you think would enhance the structure and subject?

---

---

5. What deletions from the document could be made without affecting the overall usefulness?

---

---

6. Is there any incorrect or misleading information (what and where)?

---

---

7. How would you improve this document?

---

---

# 24AA024/24LC024/24AA025/24LC025

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
<div>Device: 24AA024: 1.8V, 2 Kbit Addressable Serial EEPROM with WP pin. 24AA024T: 1.8V, 2 Kbit Addressable Serial EEPROM (Tape and Reel) with WP pin. 24LC024: 2.5V, 2 Kbit Addressable Serial EEPROM with WP pin. 24LC024T: 2.5V, 2 Kbit Addressable Serial EEPROM (Tape and Reel) with WP pin. 24AA025: 1.8V, 2 Kbit Addressable Serial EEPROM with no WP pin. 24AA025T: 1.8V, 2 Kbit Addressable Serial EEPROM (Tape and Reel) with no WP pin. 24LC025: 2.5V, 2 Kbit Addressable Serial EEPROM (Tape and Reel) with no WP pin. 24LC025T: 2.5V, 2 Kbit Addressable Serial EEPROM (Tape and Reel) with no WP pin.</div> <div>Temperature Range: I = -40°C to +85°C</div> <div>Package: P = Plastic DIP, (300 mil Body), 8-lead SN = Plastic SOIC, (150 mil Body) ST = TSSOP, 8-lead MS = MSOP, 8-lead</div>		
<div><b>Examples:</b> a) 24AA024-I/P: Industrial Temperature, 1.8V, PDIP Package b) 24AA024-I/SN: Industrial Temperature, 1.8V, SOIC Package c) 24AA025T-I/ST: Industrial Temperature, 1.8V, TSSOP Package, Tape and Reel, no WP d) 24LC024-I/P: Industrial Temperature, 2.5V, PDIP Package e) 24LC024-I/MS: Industrial Temperature, 2.5V, MSOP Package, Tape and Reel f) 24LC025-T-I/SN: Industrial Temperature, 2.5V, SOIC Package, Tape and Reel, No WP</div>		

## Sales and Support

### Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site ([www.microchip.com](http://www.microchip.com))

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

### New Customer Notification System

Register on our web site ([www.microchip.com/cn](http://www.microchip.com/cn)) to receive the most current information on our products.

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELoQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rfPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rfPICDEM, Select Mode, Smart Serial, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2004, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949:2002 ==**

*Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



## WORLDWIDE SALES AND SERVICE

### AMERICAS

#### Corporate Office

2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support: 480-792-7627  
Web Address: <http://www.microchip.com>

#### Atlanta

3780 Mansell Road, Suite 130  
Alpharetta, GA 30022  
Tel: 770-640-0034  
Fax: 770-640-0307

#### Boston

2 Lan Drive, Suite 120  
Westford, MA 01886  
Tel: 978-692-3848  
Fax: 978-692-3821

#### Chicago

333 Pierce Road, Suite 180  
Itasca, IL 60143  
Tel: 630-285-0071  
Fax: 630-285-0075

#### Dallas

4570 Westgrove Drive, Suite 160  
Addison, TX 75001  
Tel: 972-818-7423  
Fax: 972-818-2924

#### Detroit

Tri-Atria Office Building  
32255 Northwestern Highway, Suite 190  
Farmington Hills, MI 48334  
Tel: 248-538-2250  
Fax: 248-538-2260

#### Kokomo

2767 S. Albright Road  
Kokomo, IN 46902  
Tel: 765-864-8360  
Fax: 765-864-8387

#### Los Angeles

18201 Von Karman, Suite 1090  
Irvine, CA 92612  
Tel: 949-263-1888  
Fax: 949-263-1338

#### San Jose

1300 Terra Bella Avenue  
Mountain View, CA 94043  
Tel: 650-215-1444  
Fax: 650-961-0286

#### Toronto

6285 Northam Drive, Suite 108  
Mississauga, Ontario L4V 1X5, Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

#### Australia

Suite 22, 41 Rawson Street  
Epping 2121, NSW  
Australia  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

#### China - Beijing

Unit 706B  
Wan Tai Bei Hai Bldg.  
No. 6 Chaoyangmen Bei Str.  
Beijing, 100027, China  
Tel: 86-10-85282100  
Fax: 86-10-85282104

#### China - Chengdu

Rm. 2401-2402, 24th Floor,  
Ming Xing Financial Tower  
No. 88 TIDU Street  
Chengdu 610016, China  
Tel: 86-28-86766200  
Fax: 86-28-86766599

#### China - Fuzhou

Unit 28F, World Trade Plaza  
No. 71 Wusi Road  
Fuzhou 350001, China  
Tel: 86-591-7503506  
Fax: 86-591-7503521

#### China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza  
223 Hing Fong Road  
Kwai Fong, N.T., Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

#### China - Shanghai

Room 701, Bldg. B  
Far East International Plaza  
No. 317 Xian Xia Road  
Shanghai, 200051  
Tel: 86-21-6275-5700  
Fax: 86-21-6275-5060

#### China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza  
No. 5022 Binhe Road, Futian District  
Shenzhen 518033, China  
Tel: 86-755-82901380  
Fax: 86-755-8295-1393

#### China - Shunde

Room 401, Hongjian Building, No. 2  
Fengxiangnan Road, Ronggui Town, Shunde  
District, Foshan City, Guangdong 528303, China  
Tel: 86-757-28395507 Fax: 86-757-28395571

#### China - Qingdao

Rm. B505A, Fullhope Plaza,  
No. 12 Hong Kong Central Rd.  
Qingdao 266071, China  
Tel: 86-532-5027355 Fax: 86-532-5027205

#### India

Divyasree Chambers  
1 Floor, Wing A (A3/A4)  
No. 11, O'Shaughnessy Road  
Bangalore, 560 025, India  
Tel: 91-80-22290061 Fax: 91-80-22290062

#### Japan

Benex S-1 6F  
3-18-20, Shinyokohama  
Kohoku-Ku, Yokohama-shi  
Kanagawa, 222-0033, Japan  
Tel: 81-45-471-6166 Fax: 81-45-471-6122

#### Korea

168-1, Youngbo Bldg. 3 Floor  
Samsung-Dong, Kangnam-Ku  
Seoul, Korea 135-882  
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or  
82-2-558-5934

#### Singapore

200 Middle Road  
#07-02 Prime Centre  
Singapore, 188980  
Tel: 65-6334-8870 Fax: 65-6334-8850

#### Taiwan

Kaohsiung Branch  
30F - 1 No. 8  
Min Chuan 2nd Road  
Kaohsiung 806, Taiwan  
Tel: 886-7-536-4818  
Fax: 886-7-536-4803

#### Taiwan

Taiwan Branch  
11F-3, No. 207  
Tung Hua North Road  
Taipei, 105, Taiwan  
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

### EUROPE

#### Austria

Durisolstrasse 2  
A-4600 Wels  
Austria  
Tel: 43-7242-2244-399  
Fax: 43-7242-2244-393

#### Denmark

Regus Business Centre  
Lautrup høj 1-3  
Ballerup DK-2750 Denmark  
Tel: 45-4420-9895 Fax: 45-4420-9910

#### France

Parc d'Activite du Moulin de Massy  
43 Rue du Saule Trapu  
Batiment A - 1er Etage  
91300 Massy, France  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

#### Germany

Steinheilstrasse 10  
D-85737 Ismaning, Germany  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

#### Italy

Via Quasimodo, 12  
20025 Legnano (MI)  
Milan, Italy  
Tel: 39-0331-742611  
Fax: 39-0331-466781

#### Netherlands

P. A. De Biesbosch 14  
NL-5152 SC Drunen, Netherlands  
Tel: 31-416-690399  
Fax: 31-416-690340

#### United Kingdom

505 Eskdale Road  
Winnersh Triangle  
Wokingham  
Berkshire, England RG41 5TU  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820

02/17/04