

altair^{T.M.} 680b
THEORY OF OPERATION MANUAL



multics

altair 680b

THEORY OF OPERATION MANUAL



minis

a subsidiary of Pertec Computer Corporation

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I. 680b SYSTEM OVERVIEW

CLOCK: The system clock is a 500 KHz asymmetrical, two phase, non-overlapping clock that runs at the VCC voltage level. Phase one ($\varnothing 1$) is used for internal chip operations. All data transfers take place during Phase two ($\varnothing 2$). Therefore, $\varnothing 2$ is used throughout the system to enable memory and interfaces such as the Asynchronous Communication Interface Adapter (ACIA).

DATA BUS: The eight-bit, bidirectional data bus of the 6800 MPU operates at standard TTL levels and is capable of directly driving one standard TTL load and 130pF. The 680b system implements the use of 74367 (8T97) tri-state buffers to provide a drive capability of 20 standard TTL loads, greatly enhancing the expansion capabilities of the Altair 680b system.

ADDRESS BUS: The sixteen bit, bidirectional address bus of the 6800 MPU operates at standard TTL levels and is capable of directly driving one standard TTL load and 130pF. The bus is split two ways. One section is tied directly to the Front Panel and peripherals, and the other is CMOS buffered just prior to the memory section (RAM and PROM) of the system.

SYSTEM CONTROL BUS

The System Control Bus consists of the following signals:

RESET: This input is used to initialize the system after a power down condition due to either an initial start-up or power failure. It is also used to reinitialize the MPU at any time after start up. When a positive edge is detected on the RESET input, which is caused by a manual front panel reset, the MPU will begin the restart sequence. Within the restart sequence, the Program Counter is loaded with the contents of the reset vector location (FFFFE, FFFF), which contains the starting address of the System Monitor.

HALT: The Halt line is used for external control of program execution. When in the high state (RUN), the MPU will fetch the instruction addressed by the program counter and begin program execution. When the Halt line is low, all of the activity within the MPU will be halted. The Bus Available (BA) signal will then go high and the Read-Write (R/W), Address and Data lines will all be in the high impedance state. With BA high, the front panel addressing and data deposit functions will be enabled.

R/W: Read/Write controls and indicates the direction of data transfer. When in the high state (READ), data is read into the MPU from memory and peripherals. When in the low state (WRITE), data is written into memory or peripherals. When the processor is halted, R/W will turn to the off (high impedance) state.

- VMA: The VMA output indicates to peripheral devices, such as the ACIA, a stable, valid memory address on the bus.
- DBE: The DBE input is the three-state control signal for the MPU data bus and will enable the bus drivers of the 6800 when in the high state. Phase 2 is used to directly drive this input. During an MPU read cycle, the data bus drivers are disabled internally, i. e., within the MPU.
- R/W-P: Read/Write-Prime is developed by NANDing the Read/Write signal and Ø2. The Read/Write-Prime signal assures that data will always be read or written while the data bus is enabled and not during periods of invalid data.
- BA: When the MPU Halt Line is high, the microprocessor is running and the Bus Available (BA) line is low indicating that the data and address busses are not available for external control. When the Halt line is in the low state (MPU halted), the BA line is high signifying that the busses are available. This signal is used in the 680b to enable the front panel addressing and data deposit functions.
- TSC: The Three-State Control input causes all address lines and the R/W line to go into the high impedance or off state. (This occurs 500 ns after TSC=2.4V). The Bus Available and Valid Memory Address signals will be forced low. TSC is used in Direct Memory Access applications.

II. PC BOARD SCHEMATICS

SHEET 1 - MPU and Clock Circuitry

The two inverters ZZ (pins 12 and 13) and ZZ (pins 10 and 11) comprise an astable multi-vibrator that oscillates at the crystal frequency of two megahertz. Inverter ZZ (pins 3 and 4) serves to improve the rise and fall times of the square wave and drives J-K flip flops TT_a and TT_b. J-K flip flops TT_a and TT_b (functioning as a synchronous Johnson Counter) and four NOR gates generate the appropriate timing for $\bar{\theta}1$ and $\bar{\theta}2$. With a divide factor of four, this circuit produces a clock frequency of 500 KHz. Phase 1 is high for 600 ns and low for 1.4 μ s. Phase 2 is high for 1 μ s and low for 1 μ s. Transistors Q4 and Q5 serve to pull the clock signals up to the proper logic levels required by the microprocessor system.

Transistors Q2 and Q3 and their associated passive components (R10, R11, R12, C6) provide the power-up reset signal. Upon initialization of power, Q3 is off (zero volts across C6) and Q2 is holding RES low. When C6 charges to approximately 0.7 volts, Q3 will turn on pulling the base of Q2 low. This causes Q2 to turn off and ends the power-up reset sequence. The collector of Q2 is OR-tied to the control board for front panel reset capability.

The data bus (D0-D7) is connected directly to the front panel via the bus. However, the data bus is buffered through WW, XX, and YY (74367's) before being channelled to memory or peripheral devices. The R/W signal is used to complementarily enable the input or output buffers while tri-stating the ones that are disabled.

The address bus is connected directly to the front panel address lines and CMOS buffered by 4050 non-inverting buffers (CC, R, S) before connection to memory.

Inverter ZZ (pins 1 and 2) is used to develop an inverted Read/Write signal which is gated with $\bar{\theta}2$ and NAND gate M. The output of M (pin 12) is a proper level Read/Write signal that occurs coincident with $\bar{\theta}2$. This signal is termed Read/Write-Prime (R/W-P) and is used to control the direction of data transfer in all memory and peripheral interfaces.

SHEET 3 - Memory Circuitry

RAM LOCATION SELECT:

Integrated circuits AA (74LS30) and BB (4449) along with their jumpers (1-6) are used to place the 1K (1024 bytes) of random access memory supplied with the Altair 680b at any desired memory address location.

When the computer memory is expanded past the initial 1K, it may be desireable to locate the original 1K of memory at a different memory address location. For example, if an 8K memory board is added, the original 1K can be located at starting address zero with the 8K board beginning at address location 1024. Or the 8K board can be located at starting address zero with the original 1K beginning at address location 8192. Depending upon the amount of additional memory, the original 1K block may be located with any starting address from address location zero to location 64,512.

PROM SELECT:

Integrated circuits HH (74LS04), FF, EE, DD (74LS20) and GG (74LS02) are used to select one of the four 256-byte PROM locations at a time. The PROMs are arrayed in a 256 x 8 configuration and are, therefore, selected individually. PROM 1 is at the highest location (FF00) and contains the 680b System Monitor along with the reset and interrupt vectors.

SHEET 2 - Power Supply and I/O Interface Circuitry

The eight input NAND gates along with inverters VV and MM comprise the address decoding logic for the 680b's interfaces, i. e., the ACIA and the Baudot interface.

When the address F000 or F001 is presented to this logic circuitry and the address lines are stable (as indicated by the VMA signal), the NAND gates LL and UU will be enabled. LL in turn provides the proper logic level (i. e., zero) to CHIP SELECT TWO (CS2) of the ACIA chip for selection. UU (pin 8) presents a logic level zero to inverter MM (pin 13). The output of MM (pin 12) provides the proper logic level (i. e., one) to CHIP SELECT ONE (CS1) of the ACIA. The proper selection levels for CS1 and CS2 occur simultaneously.

The Address Zero (A0) line is tied directly to the Register Select (RS) input of the ACIA (pin 12). When the ACIA is selected and the A0 line is at a logic level one (placing a high level on the ACIA RS input), the Transmit/Receive Data Registers are selected. When the ACIA is selected and the A0 line is at a logic level zero (placing a low level on the ACIA RS input), the Control/Status Registers are selected.

The MPU R/W signal line is connected directly to the ACIA R/W line (JJ, pin 13). The R/W signal from the MPU controls the direction of data transfer out of the ACIA to peripherals on a WRITE signal and into the ACIA from peripherals on a READ signal. All data transfers within the computer system occur on Ø2, therefore, the ACIA ENABLE input (JJ, pin 14) is tied directly to Ø2.

The IRQ (JJ, pin 7) output is tied directly to the MPU's IRQ input (NN, pin 4). The ACIA's IRQ is an active low output that is used to interrupt the MPU and remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set (see Programming Manual).

To control the rate of data transfer in and out of the ACIA, a baud rate generator is used. Integrated circuit Z is a Fairchild Programmable Bit Rate Generator, implementing a 2.4576 MHz crystal. The output of Z (pin 10) is used to drive the Receive (ACIA, pin 3) and the Transmit Clock (ACIA, pin 4) inputs of the ACIA.

The programmable inputs of the Programmable Bit Rate Generator are labelled 0, 1, 2, and 3. They are located directly to the left of integrated circuit Z.

In direct juxtaposition to these inputs is a ground plane and an adjacent (to the left) +5 volt plane. The inputs to the Baud Rate Generator are programmed by either connecting them to the ground plane (L) or to the +5 volt plane (H). The following table is the truth table for these rate select inputs.

O	1	2	3	OUTPUT RATE Z-PIN 10	
L	H	L	L	50	Baud
H	H	L	L	75	Baud
L	L	H	L	134.5	Baud
H	L	H	L	200	Baud
L	H	H	L	600	Baud
H	H	H	L	2400	Baud
L	L	L	H	9600	Baud
H	L	L	H	4800	Baud
L	H	L	H	1800	Baud
H	H	L	H	1200	Baud
L	L	H	H	2400	Baud
H	L	H	H	300	Baud
L	H	H	H	150	Baud
H	H	H	H	110	Baud

TRUTH TABLE FOR RATE SELECT INPUTS

Assuming a crystal frequency of 2.4576 MHz, the actual output frequency of the Bit Rate Generator is 16 times the indicated output rate. For example, with a programmed output of 9600 baud, the actual frequency that is supplied to the ACIA becomes $16 \times 9.6\text{KHz}$ or 153.6Khz. The frequency becomes 16×110 or 1760 Hz with a programmed output of 110 baud.

The ACIA (JJ) has a Request To Send (RTS; JJ, pin 5) output which enables the MPU to control a peripheral device via the data bus. If the RTS output is low (the active state), the output signal is fed through a 20 ma loop interface for use in controlling a paper tape reader for an ASR-33 Teletype. For more information on the use of the RTS signal in programming, consult the 680b Programming Manual.

Both the Tx DATA (transmit) and Rx DATA (receive) signal lines are connected directly to circuitry used to interface with either 20 ma TTY or RS-232 equipped peripherals. Only one such device may be used at a time. If a Teletype (20 ma loop) is connected, then an outgoing signal is presented to the input of inverter A (pin 3) and fed to the base of Q200. Q200 is biased to provide a 20 milliamp current loop necessary for proper TTY operation. When a TTY signal is inputted to E2 and E3, the signal is buffered through inverter A and fed to the Rx DATA (JJ, pin 2) input of the ACIA.

When the Baudot interface option is chosen, the ACIA (JJ) will not be used. This is because the Motorola ACIA is programmable to seven or eight bits and the Baudot interface requires a five level (or five bit) code. Therefore, in this system the serial data is clocked into and out of the system by using D-type flip-flops. Data is serially fed to the Buffered Data Zero (BDO) line upon input. The serial-to-parallel conversion occurs within the MPU itself. Upon data output, the MPU converts its parallel data to serial data which is then fed via the BDO line to the Baudot interface circuitry.

When the Baudot interface circuitry is addressed at memory address location F002, the outputs of gates KK and LL (pin 8) are driven low. These outputs cause the outputs of inverters X (pins 10 and 12) to go high, which in turn feed NAND gate Y (pins 1 and 2) and drive its output (pin 3) low. After inversion by X (pins 3 and 4) the current high level signal is used to enable one leg of three-input NAND gate M (pin 11). Pin 10 of M is driven high (on a Write signal) by the inverted Read/Write-Prime signal. The output of M is pulled to a logic level zero when $\emptyset 2$, which is fed to M (pin 9), is high. When the MPU is in the Run mode, both the Clear (CLR) and Preset (PR) inputs of D-type edge-triggered flip-flop La are high. This permits the data transfer to take place when $\emptyset 2$ returns to a logic level zero, causing the Clock (C) input of flip-flop La to go high. The Q output of La (pin 9) is fed to the Baudot driver interface circuitry.

To affect a Read operation from data entering the Data (D) input of flip-flop Lb (pin 2), data is first buffered by inverter A (pins 5 and 6). Data will be set at the Q output of Lb (pin 6) on the rising edge of $\emptyset 1$ and will remain until an input data change occurs. This change must occur before the rising edge of the next $\emptyset 1$ pulse. When a start bit [high following inversion by A (pins 5 and 6)] is fed into D (pin 2) of Lb, it will cause the Q output to go low as $\emptyset 1$ triggers the clock. Since the Q output is directly connected to the Interrupt Request (IRQ) line, an interrupt will occur in the MPU (if the mask bit is not set). The MPU will then be ready to accept data from the Baudot interface circuitry. Subsequent data will be clocked-in with $\emptyset 1$ and held during $\emptyset 2$ when the data bus is enabled. The data will be driven onto the data bus via buffer RR (pins 11 and 12) which is enabled when location F002 is addressed and a Read operation is taking place.

Integrated circuit RR (74367) is a tri-state buffer used for hardware bit programming (see 680b Operator's Manual). The enable lines for RR (pins 1 and 15) are pulled low (active state) whenever the processor addresses location F002 and a Read operation is taking place.

This occurs when:

- 1) The monitor checks to see if there is a terminal other than the front panel being used for I/O implementation.
- 2) Software initializes an I/O port to check for the number of stop bits being used.
- 3) Software checks to see if there is a Baudot terminal attached.

SHEET 4-Display/Control Board Circuitry

Address selection occurs in the normal open state of switches S1 through S16 at which time the indicator LED will light. This will occur, however, only when Bus Available (BA) is high. This prevents the front panel switches from having any effect upon the address lines while the MPU is in the Run mode. The Data switches (S17 through S24) operate exactly the same as the Address switches, except that the Data switches are enabled by the Deposit single-shot La (pin 13) and BA. The Deposit switch, via single-shot Lb (pin 5), pulls the R/W line low for a Write operation. The Reset switch triggers single-shot Kb (pin 9). The output of Kb (pin 5) holds the Reset line of the MPU low for a minimum of eight clock cycles.

When the Run switch is actuated, single-shot Ka is enabled making the Halt line high, thus activating the MPU. Ka is retriggered by Ø2 which allows the output to remain high until a Halt is initiated.

Display/Control Board Reset Modifications

When the processor attempts to execute an invalid instruction, the 680b enters an undefined state. In order to reset the system, the computer must be powered down. This is because the Bus Available (BA) signal line will not go high (valid) when an attempt is made to halt the processor. Consequently, the front panel reset cannot be enabled.

During normal operation, IC Ka (pin 13) is high when the processor is in the Halt mode, and Pin 4 (\bar{Q}) of IC K is low. Since a low signal at IC Kb (pin 9) is necessary to effect a reset, the \bar{Q} output of Ka (pin 4) is fed to the Reset switch. When the processor is in the Run mode, IC Ka (pin 13) is low, and the \bar{Q} output (pin 4) is high. When this high signal is present on the Reset switch, a reset cannot be effected.

The following modifications allow you to perform a master reset when the computer is in an undefined state without powering down. This is accomplished by transferring control of the reset function from the BA line to the Run/Halt line.

1. Delete the signal line that connects the center pins of the Reset and Deposit switches (silkscreen side of board).
2. Delete the signal line from IC I (pins 2 and 3) to the center pin of the Reset switch (non-silkscreen side of board).
3. Since Step 2 also deletes the signal line from the Deposit switch, it is necessary to connect a jumper from the land of IC I (pin 2) to the center pin of the Deposit switch.
4. Connect a jumper from IC K (pin 4) to the center pin of the Reset switch.

Halt the computer, then reset. To initiate a reset while the processor is in the Run mode or the Halt mode, complete steps 1, 2, and 3. When these steps have been completed, jumper the center pin of the Reset switch to ground. This will enable you to reset anytime, regardless of which mode the processor is in. If a reset is actuated when the processor is in the Run mode, it will jump back to the monitor, regardless of the program it was previously running.

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Altair 680b

Theory of Operation

Addenda to page 10, Display/Control Board Circuitry

Display/Control Board Reset Modifications

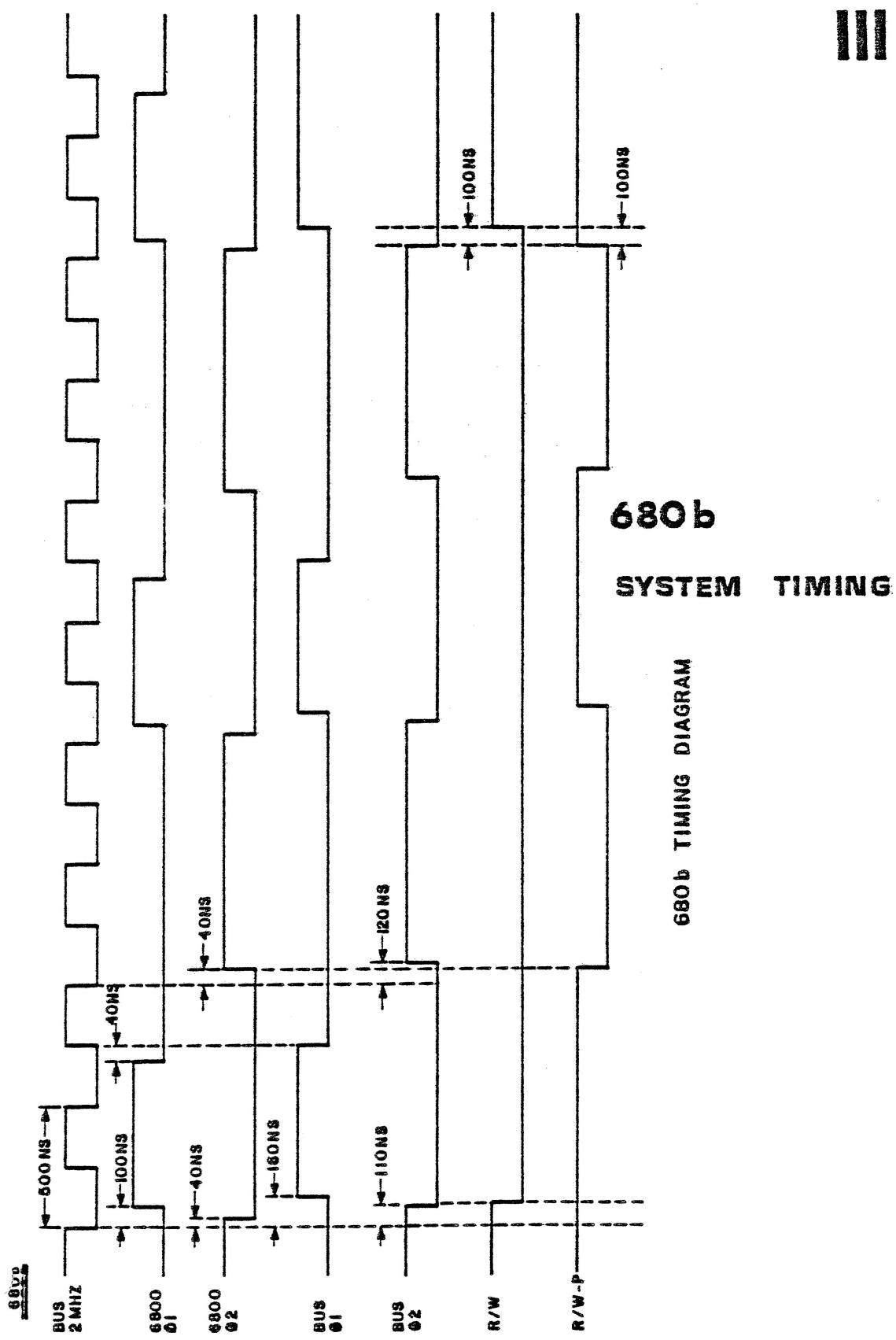
- When the processor attempts to execute an invalid instruction, the 680b enters an undefined state. In order to reset the system, the computer must be powered down. This is because the Bus Available (BA) signal line will not go HIGH (valid) when an attempt is made to halt the processor. Consequently, the front panel reset cannot be enabled.

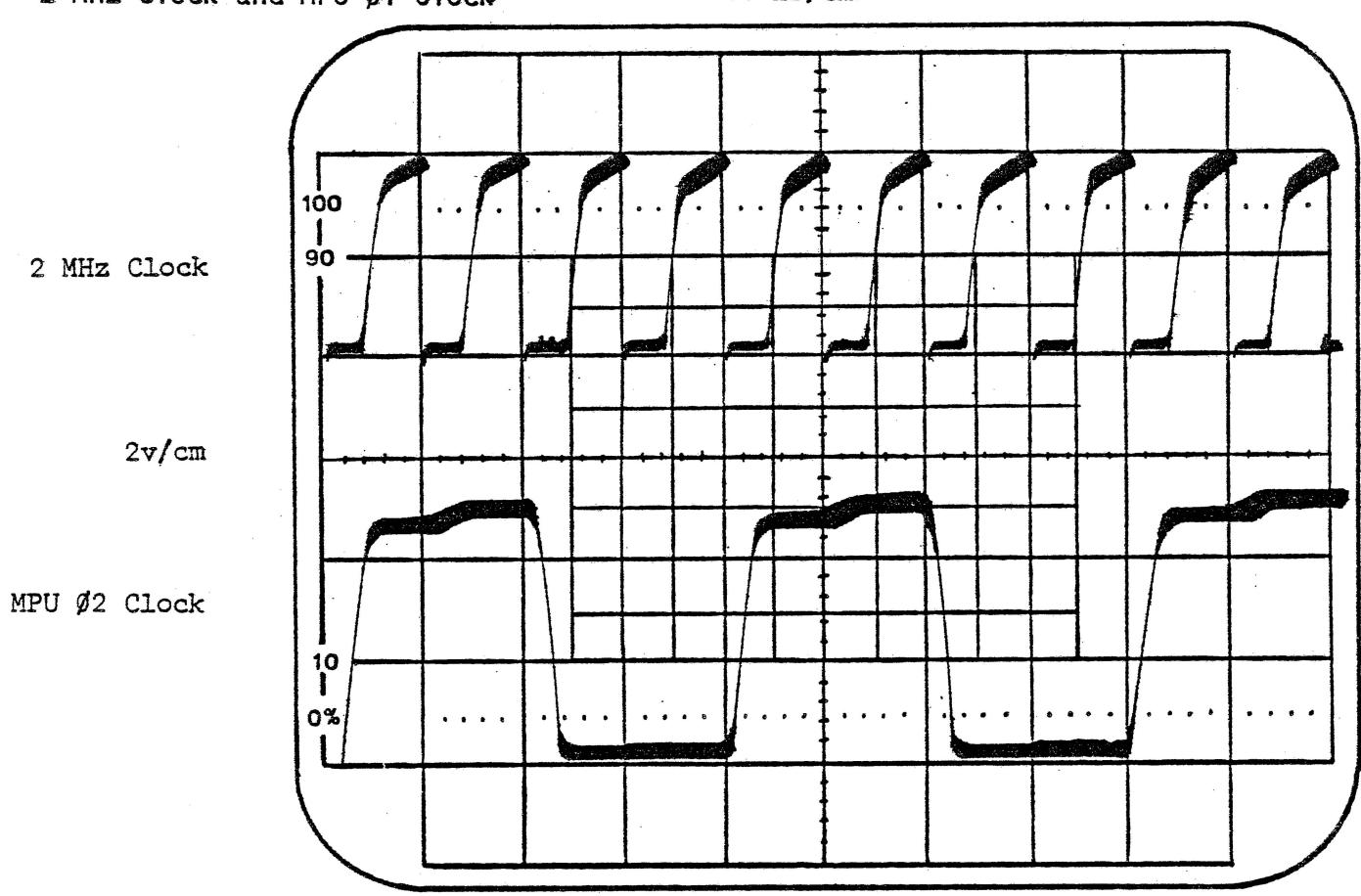
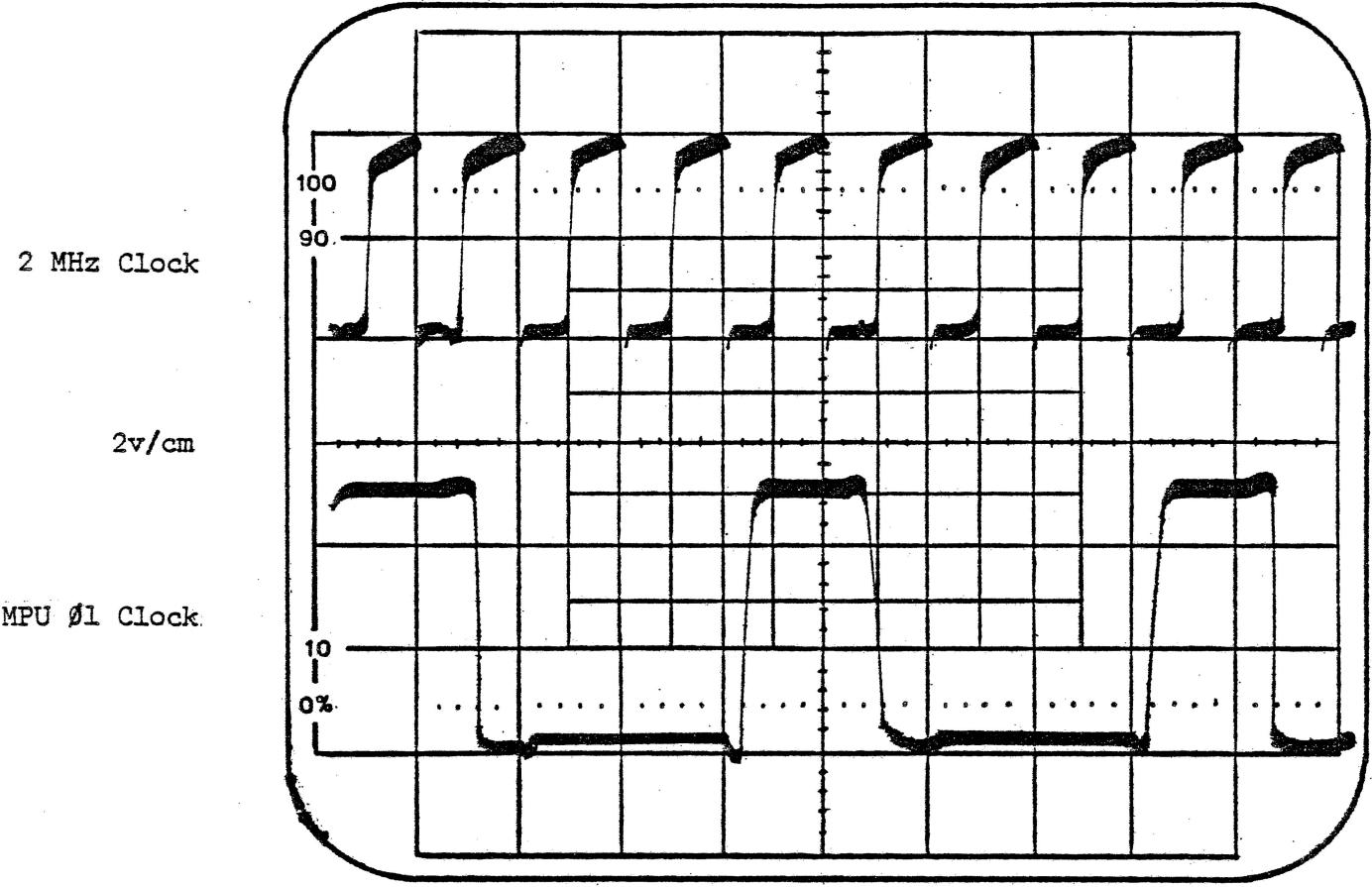
The following modifications allow you to perform a master reset when the computer is in an undefined state without powering down. This is accomplished by transferring control of the reset function from the BA line to the Run/Halt line.

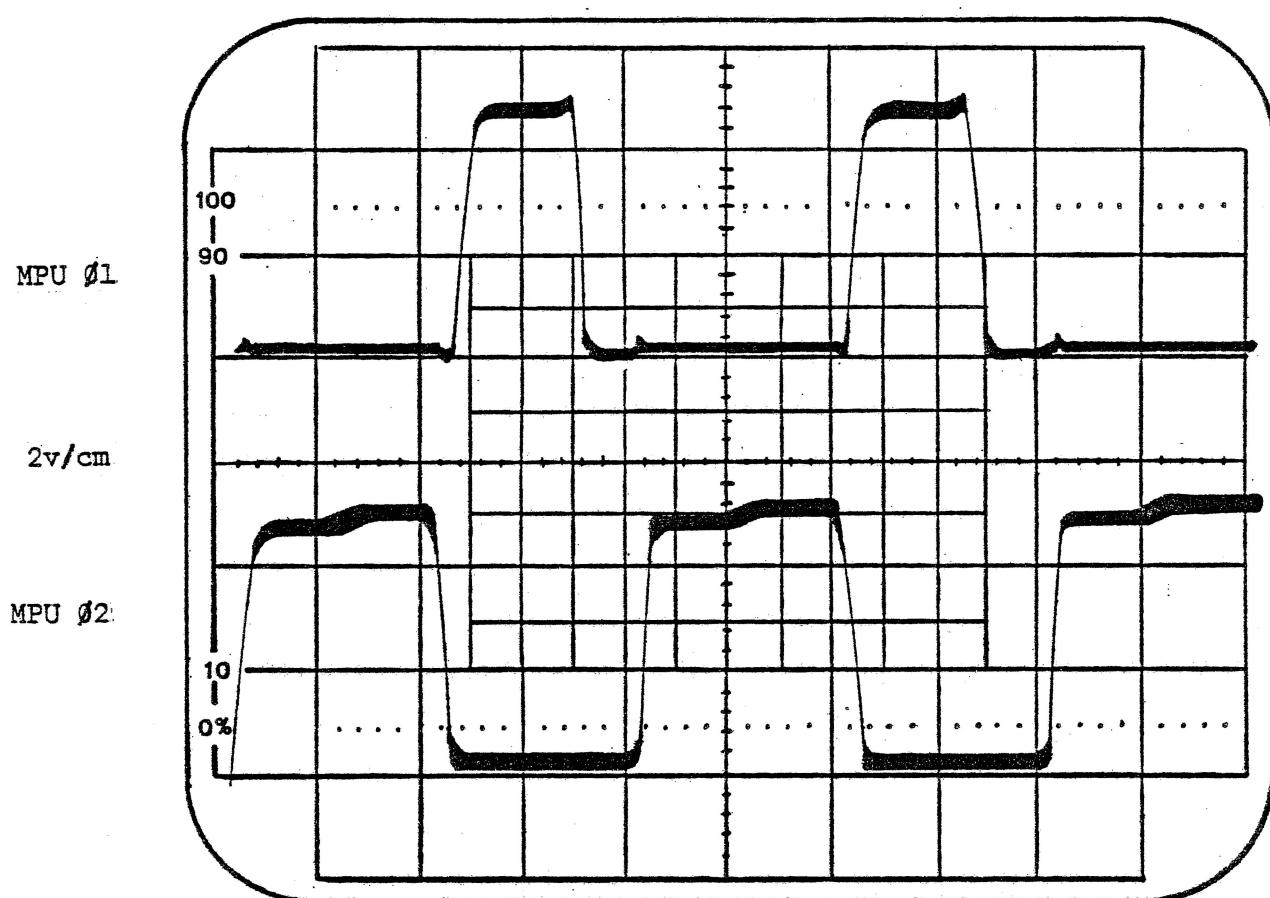
1. Delete the signal line that connects the center pins of the Reset and Deposit switches (silkscreen side of board).
2. Delete the signal line from IC I (pins 2 and 3) to the center pin of the Reset switch (non-silkscreen side of board).
3. Since Step 2 also deletes the signal line from the Deposit switch, it is necessary to connect a jumper from the land of IC I (pin 2) to the center pin of the Deposit switch.
4. Connect a jumper from IC K (pin 4) to the center pin of the Reset switch. Halt the computer, then reset.

When these modifications have been correctly completed, the circuit should operate as follows. When the processor is in the Halt mode, IC Ka, pin 13 (Q output), is HIGH and the \bar{Q} output, pin 4, is LOW. The LOW at pin 4 of IC Ka is jumpered to the center pole of the Deposit switch, thus allowing the processor to be reset. When the processor is in the Run mode and pin 4 of IC Ka is HIGH, the Reset switch is disabled.

To initiate a reset while the processor is in the Run mode or the Halt mode, complete steps 1, 2, and 3. Change Step 4 by tying the center pole of the Reset switch to ground. This will enable you to reset anytime, regardless of which mode the processor is in. If a reset is actuated when the processor is in the Run mode, it will jump back to the monitor, regardless of the program it was previously running.

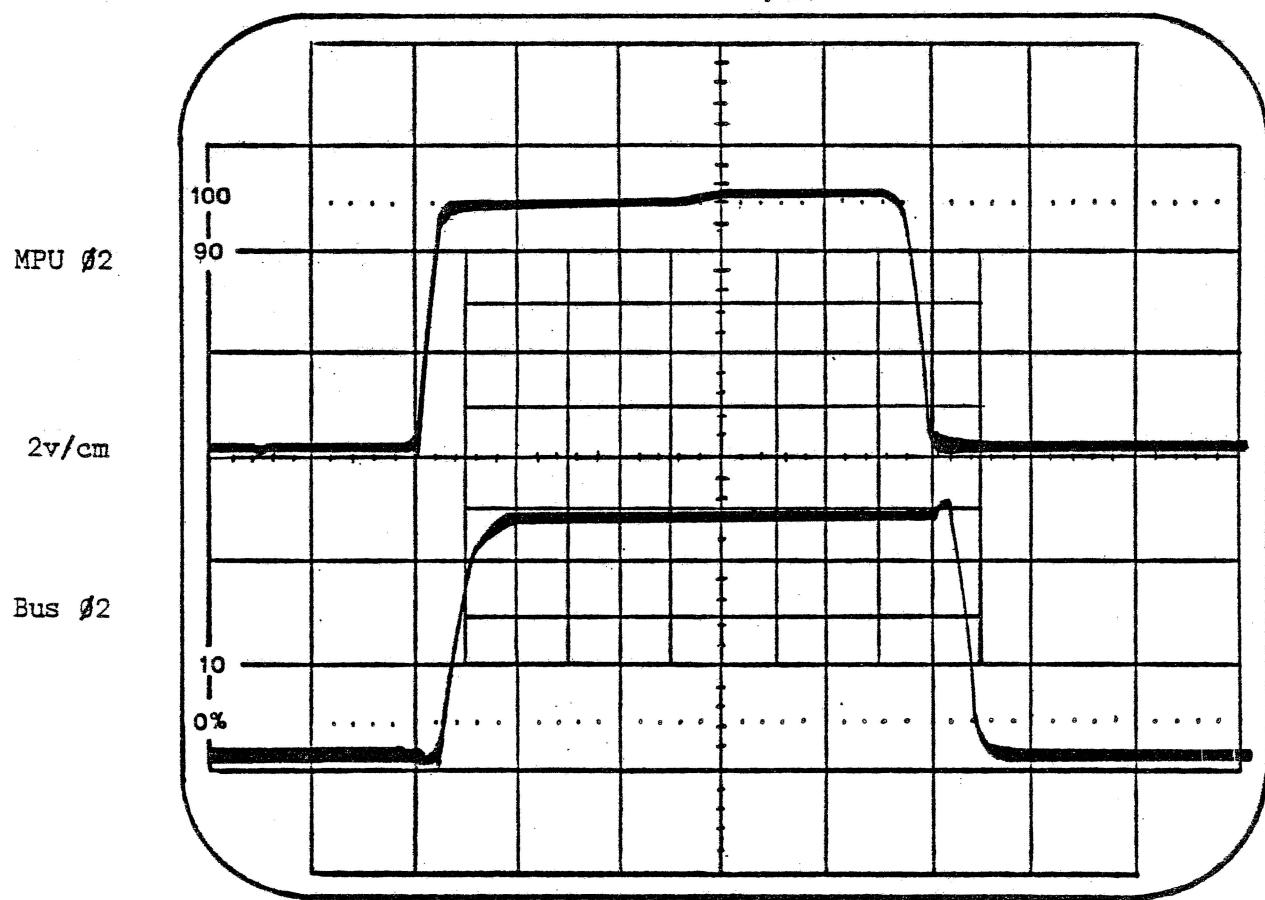






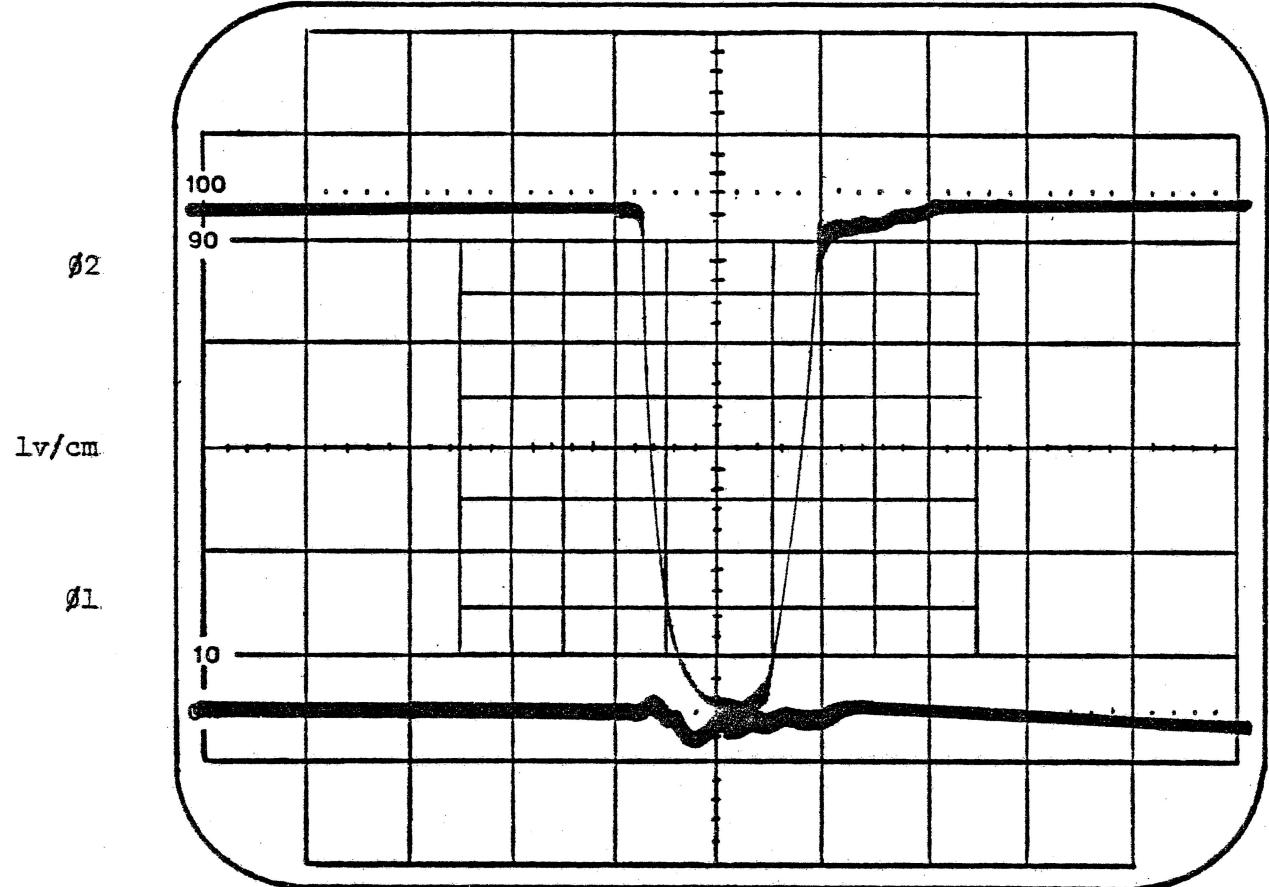
MPU Ø1 and MPU Ø2

500 ns/cm



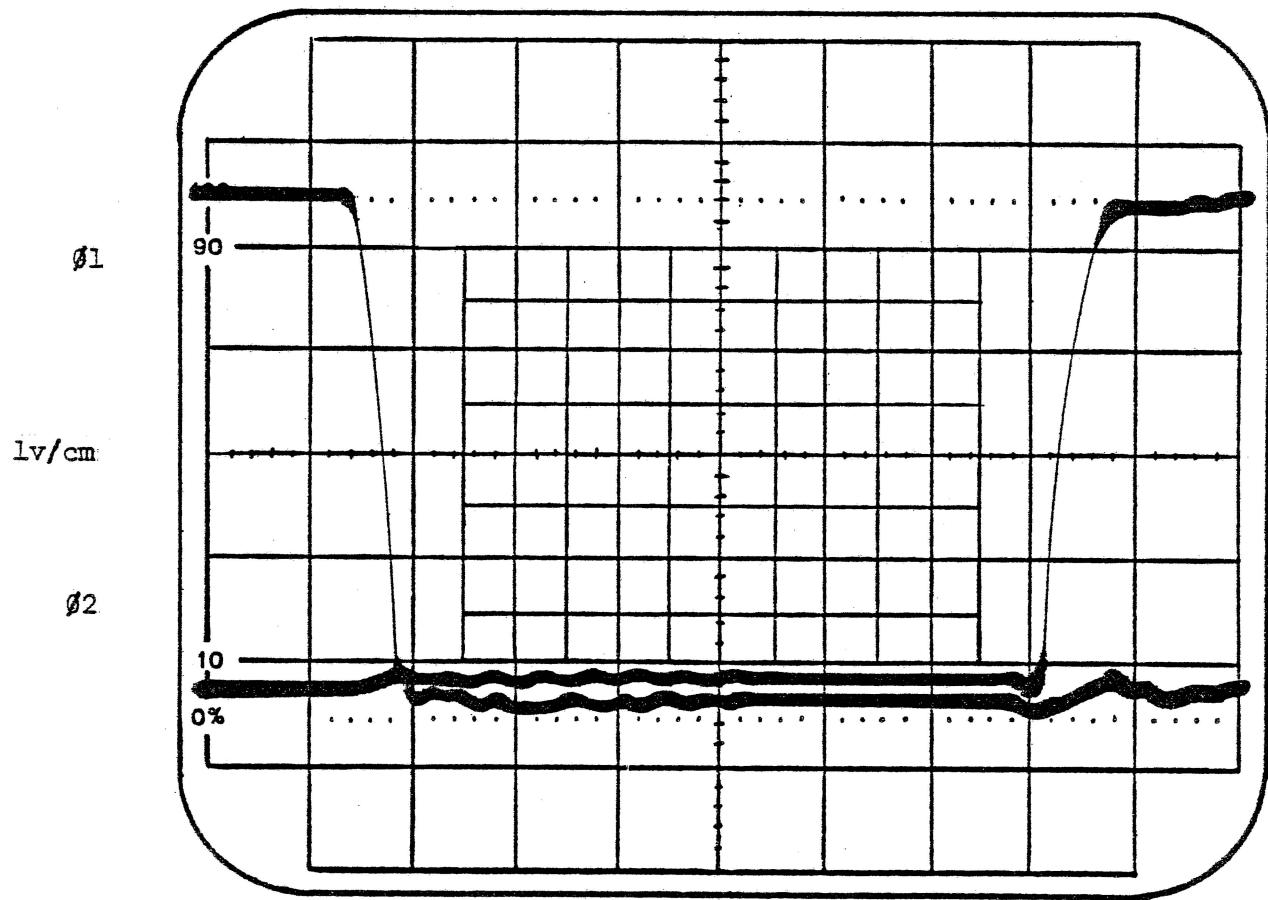
MPU Ø2 Clock and Bus Ø2

200 ns/cm



MPU Clock Non-Overlap Region

50ns/cm



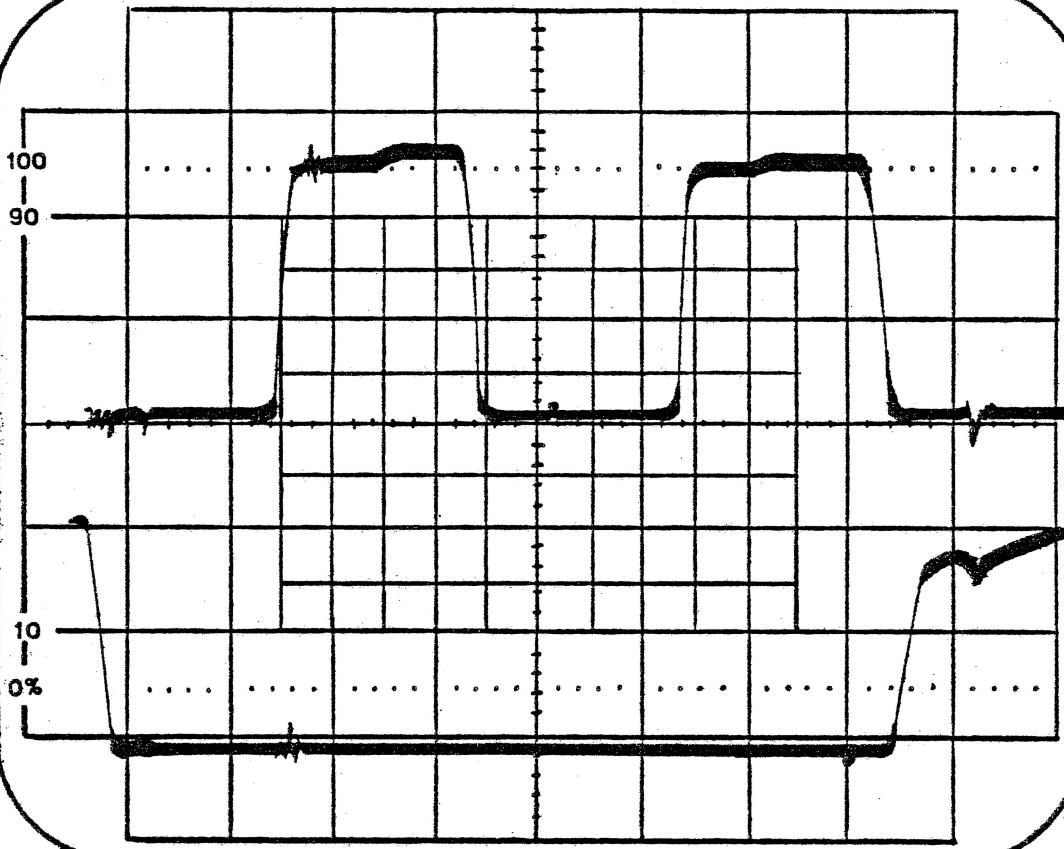
MPU Clock Non-Overlap Region

50ns/cm

MPU #2

2v/cm

R/W



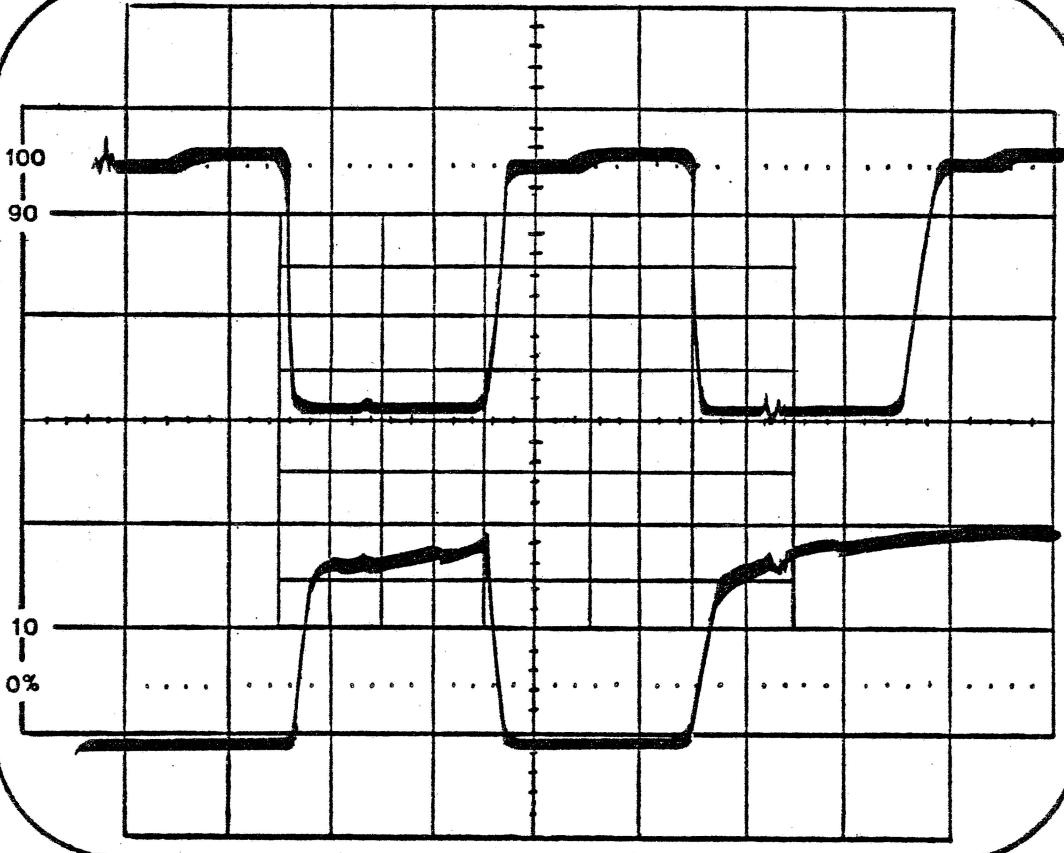
READ/WRITE During WRITE Cycle

500 ns/cm

MPU #2

2v/cm

$\overline{R/W} \cdot \#2$
(R/W-P)



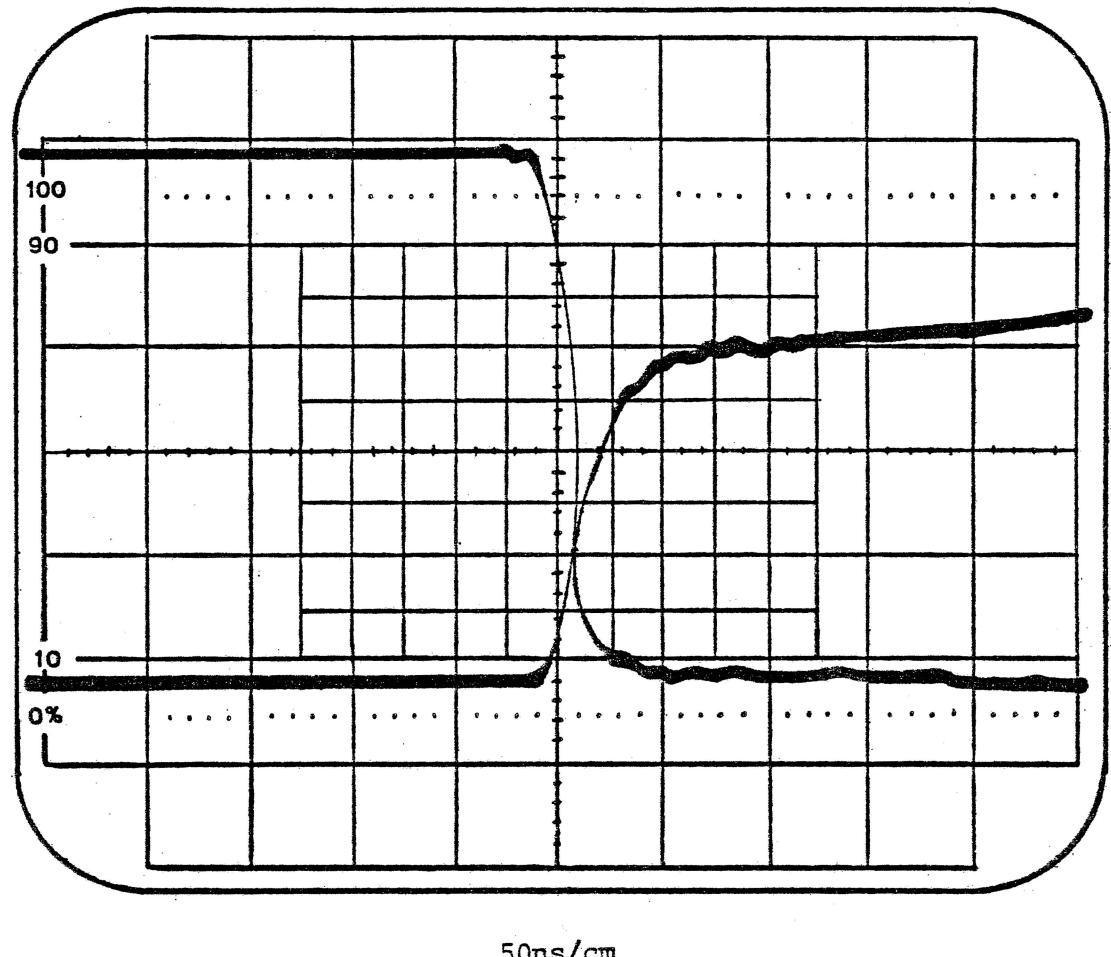
READ/WRITE PRIME During WRITE Cycle

500 ns/cm

MPU $\emptyset 2$ and DBE

2v/cm

R/W-P



50ns/cm

READ/WRITE PRIME going high as $\emptyset 2$ and
DBE go low, disenabling the data bus
and preventing data from being written
during invalid period.

IV. TROUBLESHOOTING AIDS FOR THE 680b

A. General Guide

1. Troubleshooting TTL Logic

Keep in mind the D. C. levels for TTL logic. A valid logic 0 is between -0.6v to +0.8v. A valid logic 1 is between +2.2v and +5.5v.

2. The first steps of troubleshooting the 680b are:

- a. Identify the problem(s).
 - b. Check power supply voltages. (Wrong voltages can cause many strange effects).
 - c. Isolate and repair the problems one at a time. Don't let the presence of several problems cause confusion.
3. Digital electronics is logical. If there is a situation that is not logical, you have isolated the problem or the information you have is incorrect or incomplete.

B. Specific Problems

1. Front Panel Display Board

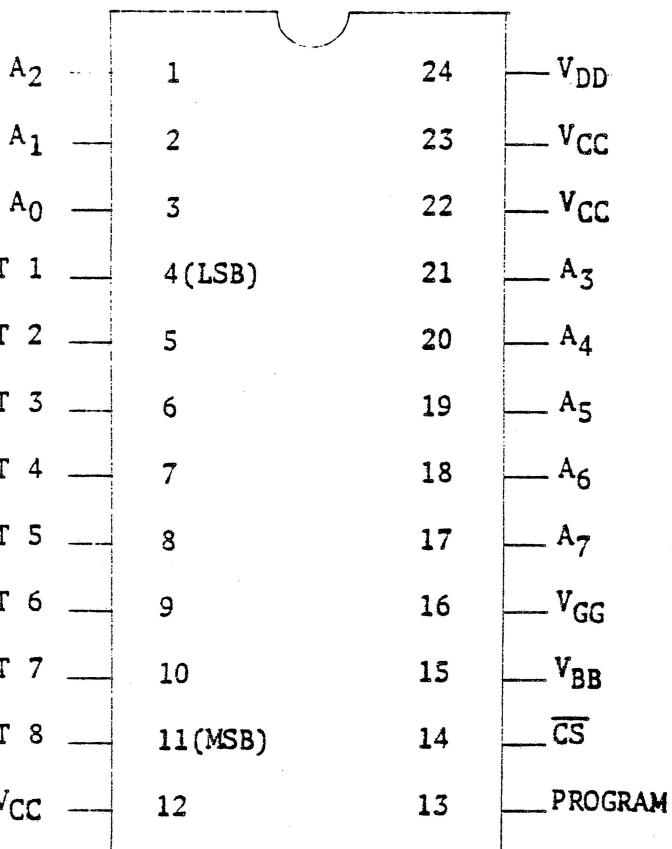
- a. If multiple LEDs turn on or off together with the actuation of only one of the appropriate switches, check for a solder bridge. These are especially common near the inputs and outputs of ICs A, B, C, D, E, F, G, and H.
- b. Be sure that the HLT jumper is soldered to pad A and not pad B.
- c. If erroneous data is continually written into memory when actuating the RUN-HALT switch, be sure that R₄₁ and C₉ are correctly installed. Check to see that the land beneath R₄₁ has been cut so that current flows through the resistor and is not shunted by the land.

d. If one of the LEDs will not light, check the function of its integrated circuit driver, (ICs E, F, G, H). Be sure that the output is the complement of the input since these drivers are inverters.

2. Main Board

- a. If unit is completely inoperative, (i. e., LEDs will not light), check power supply voltages. There should be +5 vdc at the plus side of C₃ (output of VR-1). The emitter of Q1 (TIP-30) should supply -9 vdc. If the outputs of these devices do not supply the proper voltages, check the input voltages. If these are non-existent, check the outputs and inputs of the appropriate bridge rectifiers and be sure that the transformer lines are correctly attached to the main board connector.
- b. If the Front Panel LEDs are all illuminated, yet no operations (addressing and depositing data) can be implemented, one of the system clock signals may be faulty. Check the following signals at their respectively designated locations:
 - 1) Phase 2 should appear at NN (pin 37); if it is nonexistent, check:
 - a) ZZ (pin 3); if no 2MHz square wave appears, either C12 is not 50pf, R31 and R32 are not 470 ohm, C13 is not .01μf, the crystal is bad, or ZZ (74LS04) is not functioning properly.
 - b) ZZ (pin 4). If the 2MHz clock appears at ZZ (pin 3), then it will appear at ZZ (pin 4) if ZZ is not faulty or if it is not shorted to another signal line.

- c) The 1 MHz clock at TT (pin 13).
 - d) The 500 KHz clock at TT (pin 9) and its complement at TT (pin 8).
 - e) Q4 and Q3. If these are improperly installed, drastically distorted clock waveforms will be supplied to the MPU and other system devices.
- c. If actuation of the Deposit switch fails to change the status of the DATA LEDs (that is, if the switches display data different from the LEDs), check to be sure that YY and XX (pin 1) are pulled low with actuation of DEPOSIT switch. ZZ (pins 1 and 2) and ZZ (pins 5 and 6) could be faulty if this does not occur. Also check to see if JJ (Pin 13) is pulling the R/W line low. This would indicate a faulty ACIA.
- d. If all DATA LEDs stay lit continuously, check jumpers one through six to be sure that they are correctly connected for the desired RAM starting address. Details on proper connection are given in the Operator's Manual.
- e. If one bit at a particular address location consistently will not deposit data, it is likely that a RAM is bad.
- f. If the I/O section of the computer is completely inoperative, check that:
- 1) The proper baud rate has been selected.
 - 2) XTAL 1 is functioning.
 - 3) All of the proper control signals (i. e., R/W, E and RS) are reaching the ACIA.
 - 4) The proper I/O interface circuitry has been selected.
 - 5) The proper User Programmable Bits have been selected.



PIN CONFIGURATIONS

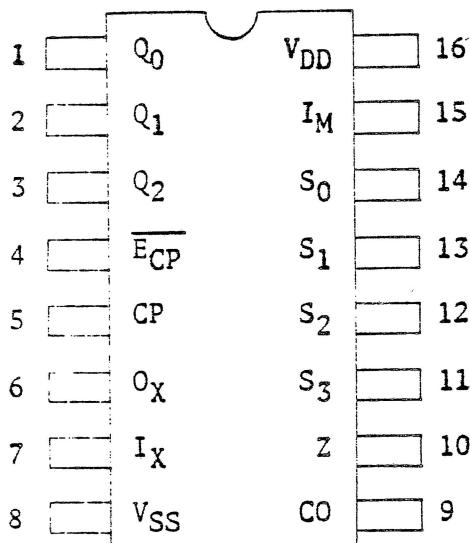
V

6850
ACIA

1	V _{SS}	CTS	24
2	Rx Data	DCD	23
3	Rx Clk	DO	22
4	Tx Clk	D1	21
5	RTS	D2	20
6	Tx Data	D3	19
7	IRQ	D4	18
8	CS0	D5	17
9	CS2	D6	16
10	CS1	D7	15
11	RS	E	14
12	V _{DD}	R/W	13

THIS PIN IS THE DATA INPUT LEAD DURING
PROGRAMMING.

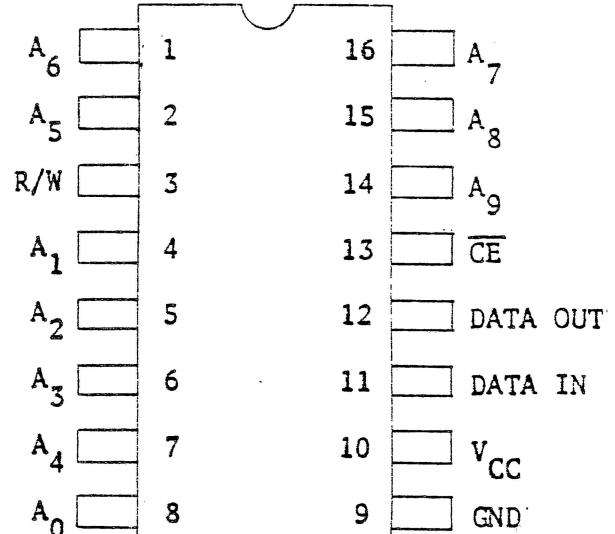
1702A
PROM



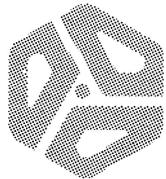
34702
Bit Rate
Generator

1	V _{SS}	Reset	40
2	Halt	TSC	39
3	φ1	N.C.	38
4	IRQ	φ2	37
5	VMA	DBE	36
6	NMI	N.C.	35
7	BA	R/W	34
8	V _{CC}	D0	33
9	A0	D1	32
10	A1	D2	31
11	A2	D3	30
12	A3	D4	29
13	A4	D5	28
14	A5	D6	27
15	A6	D7	26
16	A7	A15	25
17	A8	A14	24
18	A9	A13	23
19	A10	A12	22
20	A11	V _{SS}	21

6800 MPU



2102A
RAM



mits

2450 Alamo S.E.
Albuquerque, New Mexico 87106

USER'S DOCUMENTATION REPORT

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